FGD3050G2V

EcoSPARK® 2 Ignition IGBT

300 mJ, 500 V, N−Channel Ignition IGBT

Features

- SCIS Energy = 300 mJ at T_J = 25°C
- Logic Level Gate Drive
- AEC−Q101 Qualified and PPAP Capable
- These Device is Pb−Free and are RoHS Compliant

Applications

- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Application

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

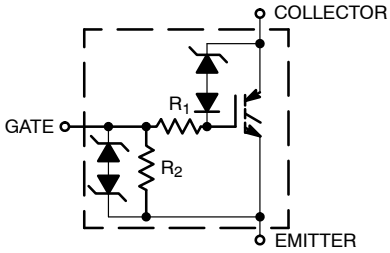
Symbol	Parameter	Value	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage (I_C = 1 mA)	500	V
BV_{ECS}	Emitter to Collector Voltage − Reverse Battery Condition (I_C = 10 mA)	20	V
E_{SCIS25}	Self Clamping Inductive Switching Energy (Note 1)	300	mJ
$E_{SCIS150}$	Self Clamping Inductive Switching Energy (Note 2)	180	mJ
I_{C25}	Collector Current Continuous at V_{GE} = 4.0 V, T_C = 25°C	32	A
I_{C110}	Collector Current Continuous at V_{GE} = 4.0 V, T_C = 110°C	27	A
V_{GEM}	Gate to Emitter Voltage Continuous	±10	V
P_D	Power Dissipation Total, T_C = 25°C	150	W
	Power Dissipation Derating, for T_C > 25°C	1.1	W/°C
T_J	Operating Junction Temperature Range	−40 to +175	°C
T_{STG}	Storage Junction Temperature Range	−40 to +175	°C
T_L	Max. Lead Temperature for Soldering (Leads at 1.6 mm from case for 10 s)	300	°C
T_{PKG}	Max. Lead Temperature for Soldering (Package Body for 10 s)	260	°C
ESD	Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV

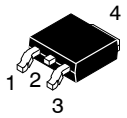
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self clamped inductive Switching Energy (ESCIS25) of 335 mJ is based on the test conditions that is starting T_J = 25°C, L = 3 mHy, ISCIS = 14.2 A, R_{GE} = 1 kΩ, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.
2. Self Clamped inductive Switching Energy (ESCIS150) of 180 mJ is based on the test conditions that is starting T_J = 150°C, L = 3mHy, ISCIS = 11 A, R_{GE} = 1 kΩ, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.

ON Semiconductor®

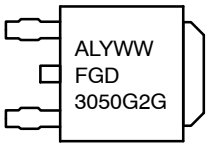
www.onsemi.com





DPAK (SINGLE GAUGE)
CASE 369C

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
FGD3050G2 = Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction−to−Case − Steady State (Drain)	$R_{\theta JC}$	0.9	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ.	Max.	Units
OFF CHARACTERISTICS							
BV_{CER}	Collector to Emitter Breakdown Voltage	I_{CE} = 2 mA, V_{GE} = 0 V, R_{GE} = 1 kΩ, T_J = −40 to 150°C		470	–	530	V
BV_{CES}	Collector to Emitter Breakdown Voltage	I_{CE} = 10 mA, V_{GE} = 0 V, R_{GE} = 0, T_J = −40 to 150°C		495	–	555	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_{CE} = −75 mA, V_{GE} = 0 V, T_J = 25°C		20	–	–	V
BV_{GES}	Gate to Emitter Breakdown Voltage	I_{GES} = ±5 mA		±12	±14	–	V
I_{CER}	Collector to Emitter Leakage Current	V_{CE} = 250 V, R_{GE} = 1 kΩ	T_J = 25°C	–	–	25	μA
			T_J = 150°C	–	–	1	mA
I_{ECS}	Emitter to Collector Leakage Current	V_{EC} = 15 V	T_J = 25°C	–	–	1	mA
			T_J = 150°C	–	–	40	
R_1	Series Gate Resistance			–	111	–	Ω
R_2	Gate to Emitter Resistance			10K	–	30K	Ω
ON CHARACTERISTICS (Note 5)							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 6 A, V_{GE} = 4 V, T_J = 25°C		–	1.1	1.2	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 10 A, V_{GE} = 4.5 V, T_J = 150°C		–	1.3	1.45	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 15 A, V_{GE} = 4.5 V, T_J = 150°C		–	1.6	1.75	V
DYNAMIC CHARACTERISTICS							
$Q_{G(ON)}$	Gate Charge	I_{CE} = 10 A, V_{CE} = 12 V, V_{GE} = 5 V		–	22	–	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_{CE} = 1 mA, V_{CE} = V_{GE}	T_J = 25°C	1.3	1.6	2.2	V
			T_J = 150°C	0.75	1.1	1.8	
V_{GEP}	Gate to Emitter Plateau Voltage	V_{CE} = 12 V, I_{CE} = 10 A		–	2.7	–	V
SWITCHING CHARACTERISTICS							
$td_{(ON)R}$	Current Turn−On Delay Time−Resistive	V_{CE} = 14 V, R_L = 1 Ω, V_{GE} = 5 V, R_G = 1 KΩ,		–	0.9	4	μs
t_{rR}	Current Rise Time−Resistive			–	1.6	7	
$td_{(OFF)L}$	Current Turn−Off Delay Time−Inductive	V_{CE} = 300 V, L = 2 mH, V_{GE} = 5 V, R_G = 1 KΩ,		–	5.4	15	
t_{fL}	Current Fall Time−Inductive			–	1.4	15	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Diameter	Tape Width	Qty†
FGD3050G2	FGD3050G2V	DPAK (Pb−Free)	330 mm	16 mm	2500

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

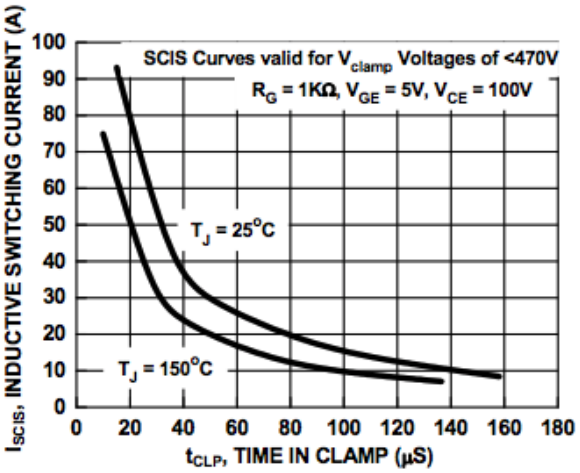


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

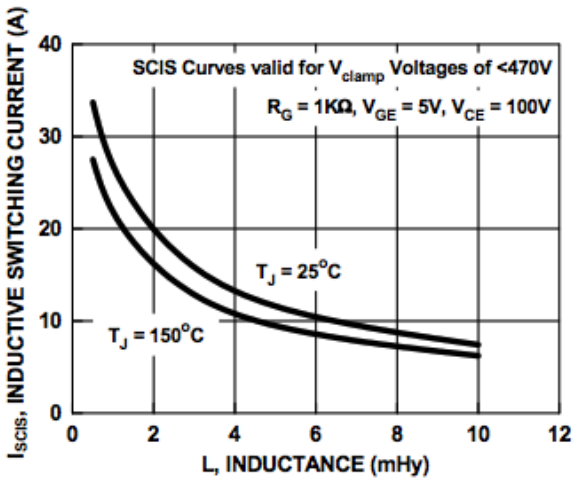


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

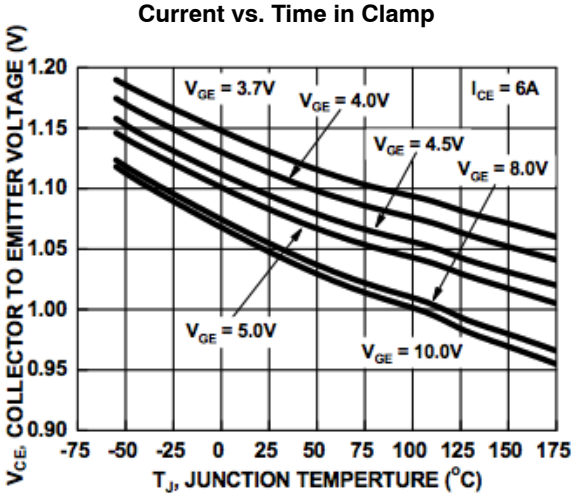


Figure 3. Collector to Emitter On−State Voltage vs. Junction Temperature

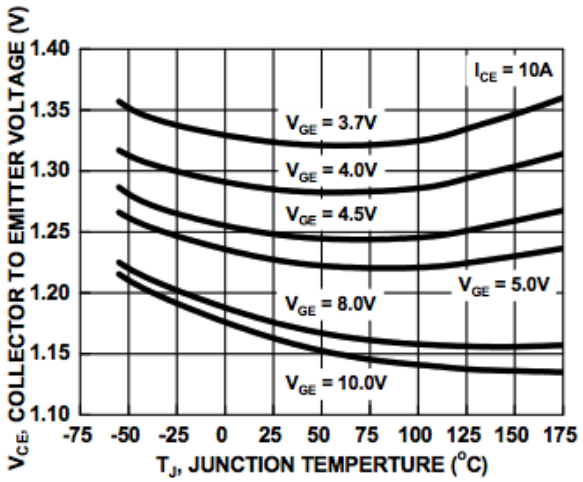


Figure 4. Collector to Emitter On−State Voltage vs. Junction Temperature

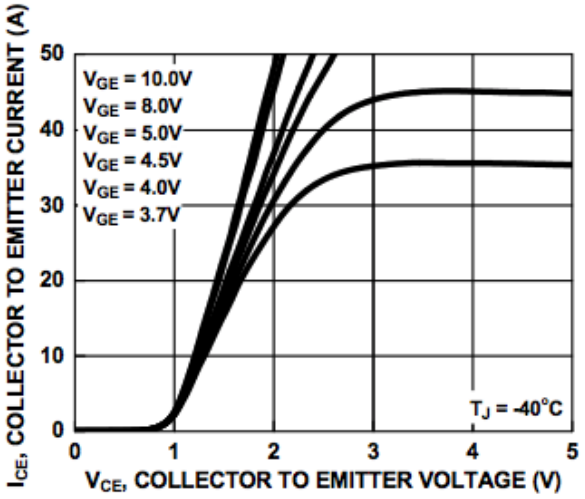


Figure 5. Collector to Emitter On−State Voltage vs. Collector Current

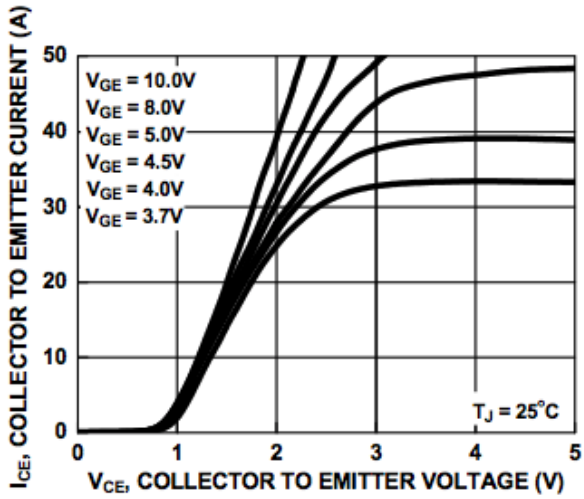


Figure 6. Collector to Emitter On−State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS (continued)

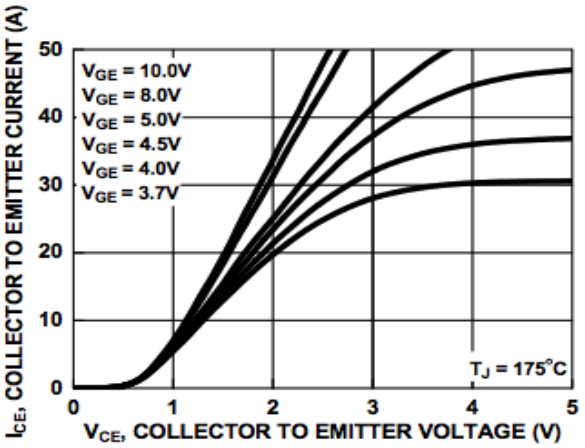


Figure 7. Collector to Emitter On−State Voltage vs. Collector Current

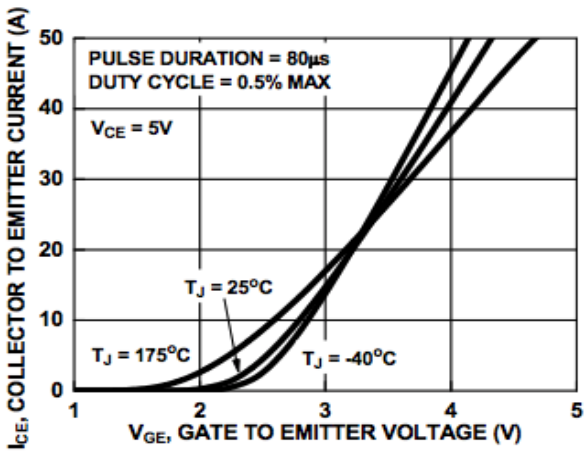


Figure 8. Transfer Characteristics

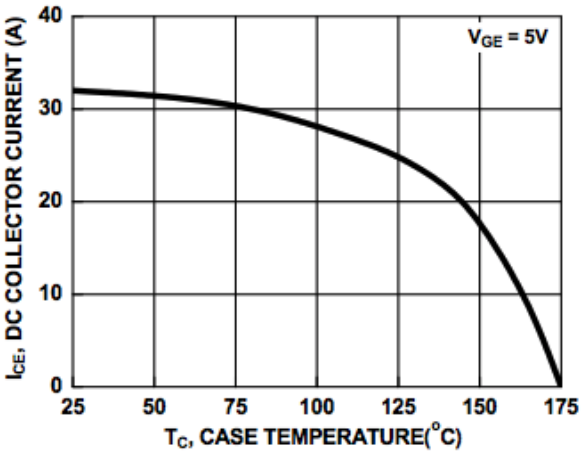


Figure 9. DC Collector Current vs. Case Temperature

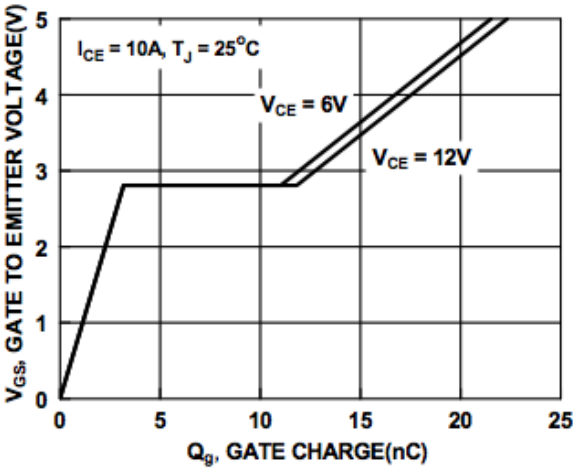


Figure 10. Gate Charge

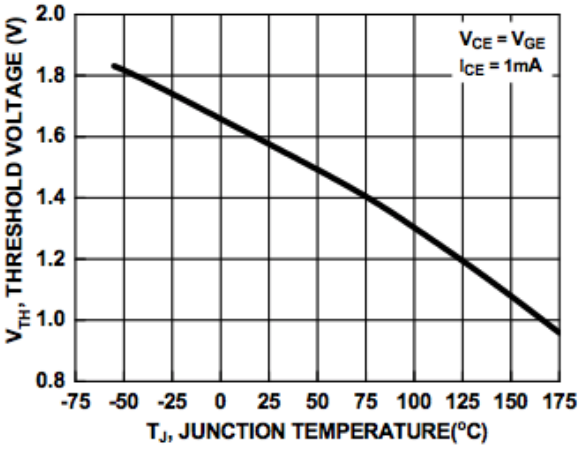


Figure 11. Threshold Voltage vs. Junction Temperature

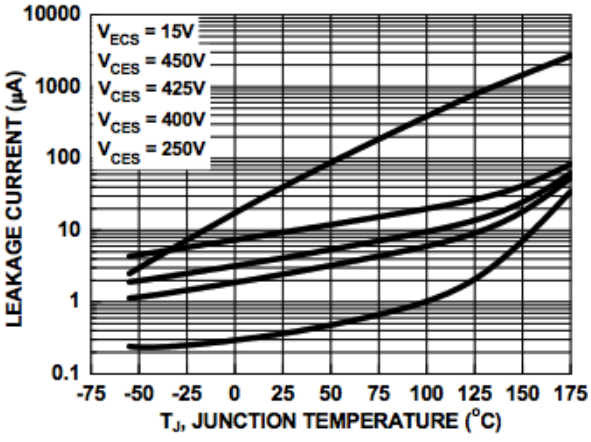


Figure 12. Leakage Current vs. Junction Temperature Temperature

TYPICAL CHARACTERISTICS (continued)

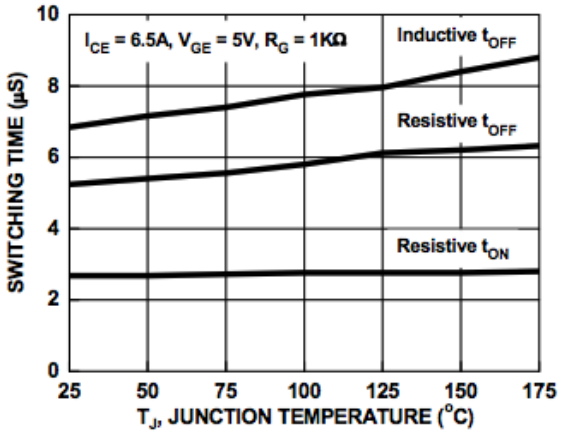


Figure 13. Switching Time vs. Junction Temperature

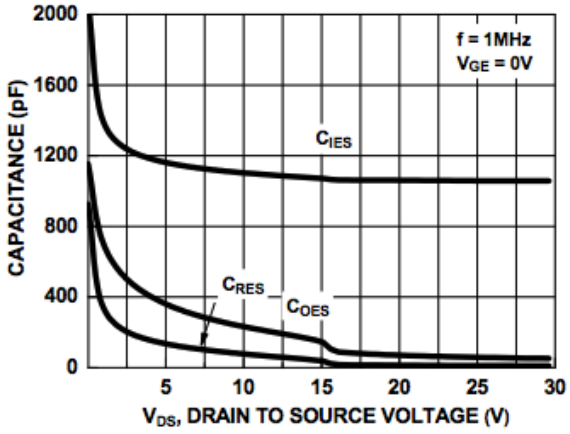


Figure 14. Capacitance vs. Collector to Emitter Voltage

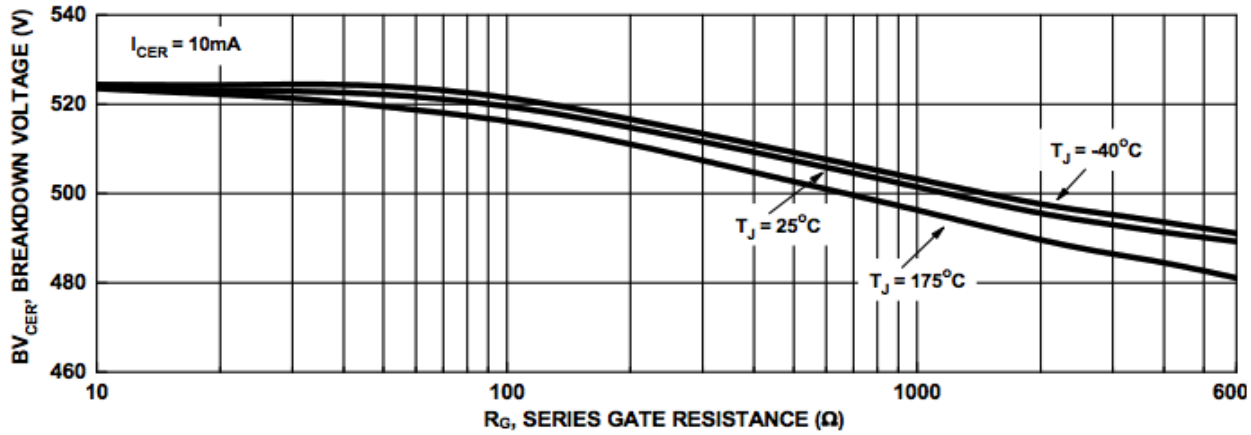


Figure 15. Break down Voltage vs. Series Resistance

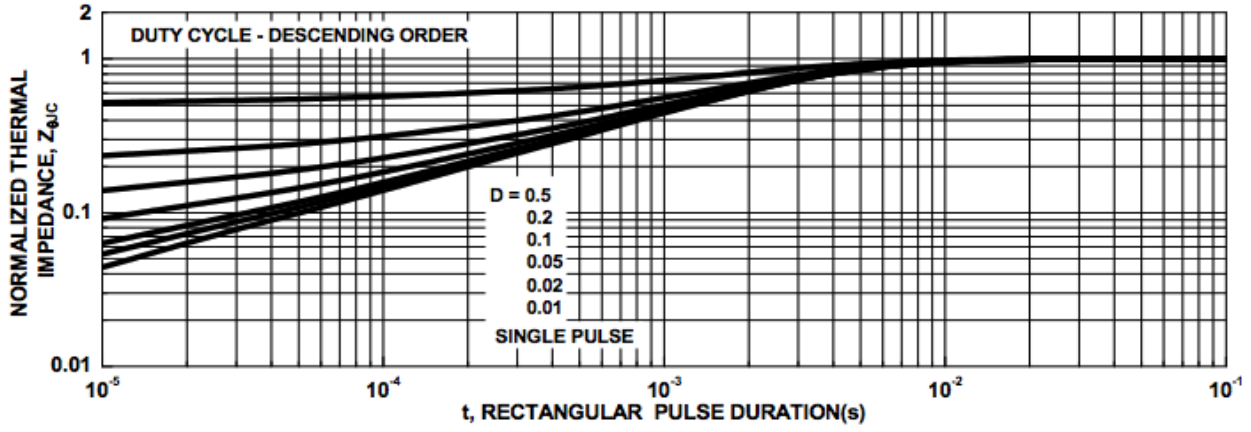
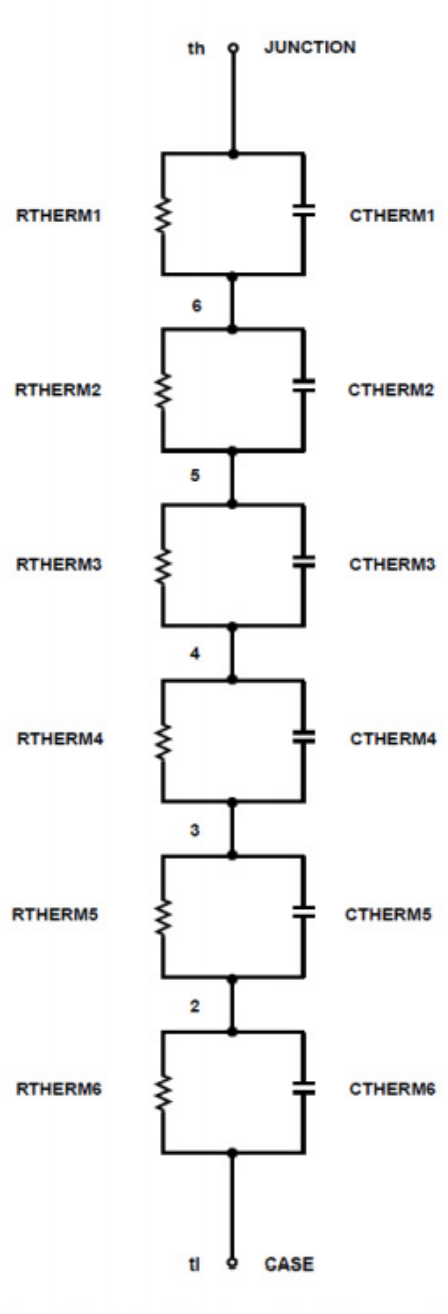


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

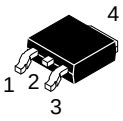
SPICE Thermal Model

CTHERM1 th 6 5.7337E-05
CTHERM2 6 5 5.3736E-03
CTHERM3 5 4 1.1141E-03
CTHERM4 4 3 2.8690E-04
CTHERM5 3 2 7.4429E-04
CTHERM6 2 tl 3.7019E-03

RTHERM1 th 6 6.6403E-03
RTHERM2 6 5 5.8449E-01
RTHERM3 5 4 5.3930E-02
RTHERM4 4 3 9.2492E-03
RTHERM5 3 2 1.5794E-02
RTHERM6 2 tl 1.7974E-01



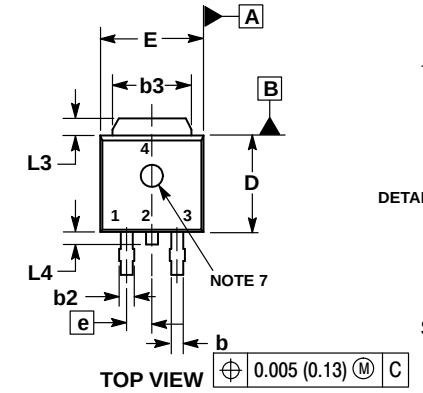
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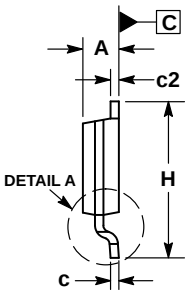
SCALE 1:1

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

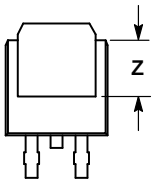
DATE 21 JUL 2015



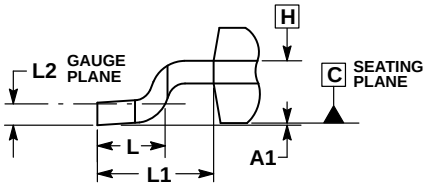
TOP VIEW



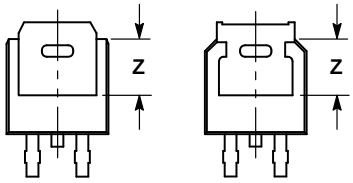
SIDE VIEW



BOTTOM VIEW



DETAIL A
ROTATED 90° CW



BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

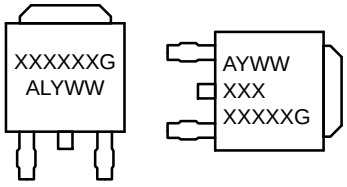
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

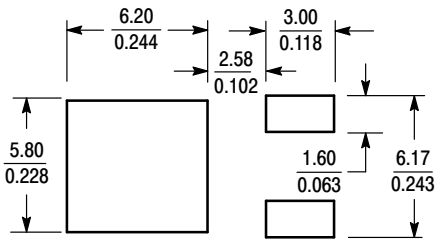


IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

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