TPS798xx-Q1 50 mA, 3 V to 50 V, Micropower, Low-Dropout Linear Regulator

1 Features

- Qualified for Automotive Applications
- Wide Input Voltage Range: 3 V to 50 V
- Low Quiescent Current: 40 µA (Typical)
- Low Dropout Voltage: 300 mV (Typical)
- Output Current: 50 mA
- No Input Protection Diodes Needed
- Adjustable Output From 1.275 V to 28 V
- 1-µA Quiescent Current in Shutdown
- Stable With 1-µF Output Capacitor
- Stable With Aluminum, Tantalum, or Ceramic Capacitors
- Reverse Input-Battery Protection
- Reverse Output Current Flow Protection
- Thermal Limiting
- Available in an 8-Pin MSOP-PowerPAD IC Package

2 Applications

- Low-Current, High-Voltage Regulators
- Regulators for Battery-Powered Systems
- Telecom
- Automotives

3 Description

The TPS798xx-Q1 is the first device in a line of 50-V high-voltage micropower low-dropout (LDO) linear regulators. This device is capable of supplying 50-mA output current with a dropout voltage of only 300 mV. Designed for low quiescent current high voltage (50 V) applications, 40 µA operating and 1 µA in shutdown makes the TPS798xx-Q1 an ideal choice for battery-powered or high-voltage systems. Quiescent current is also well-controlled in dropout.

Other features of the TPS798xx-Q1 include the ability to operate with low equivalent series resistance (ESR) ceramic output capacitors. This device is stable with only 1 µF on the output; most older devices require from 10-µF to 100-µF tantalum capacitors for stability. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse input-battery protection, reverse output current protection, current limiting, and thermal limiting to protect the device in various fault conditions.

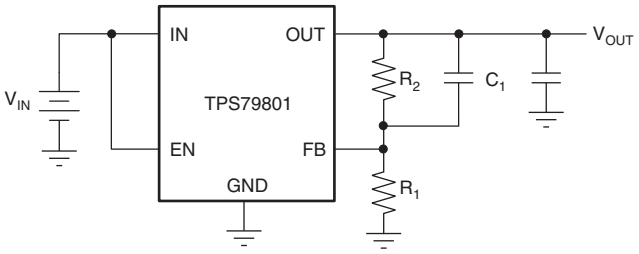
This device is available in a fixed output voltage of 5 V (TPS79850) and with an adjustable output voltage with a 1.275-V reference voltage (TPS79801). The TPS798xx-Q1 regulator is available in a 8-pin MSOP-PowerPAD (DGN) package with an exposed pad for enhanced thermal management capability.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS79801-Q1	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm
TPS79850-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



$V_{OUT} = 1.275\ V\ (1 + R_2 / R_1) + I_{FB}R_2$
$V_{FB} = 1.275\ V$
$I_{FB} = 0.2\ \mu A$ at 25°C
Output Range = 1.275 V to 28 V

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 3
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Dissipation Ratings ... 6
6.7 Typical Characteristics ... 7
7 Detailed Description ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 12
8 Application and Implementation ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 13
9 Power Supply Recommendations ... 15
9.1 Thermal Considerations ... 15
10 Layout ... 15
10.1 Layout Guidelines ... 15
10.2 Layout Example ... 15
10.3 Thermal Considerations ... 15
11 Device and Documentation Support ... 17
11.1 Related Links ... 17
11.2 Community Resources ... 17
11.3 Trademarks ... 17
11.4 Electrostatic Discharge Caution ... 17
11.5 Glossary ... 17
12 Mechanical, Packaging, and Orderable Information ... 17

4 Revision History

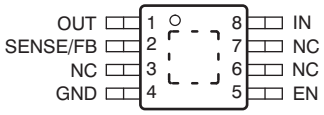
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2011) to Revision E	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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5 Pin Configuration and Functions

DGN Package
8-Pin MSOP With PowerPAD™
Top View



The exposed thermal pad is connected to ground through pin 4 (GND).

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Enable pin. Driving the EN pin high turns on the regulator over full operating range. Driving this pin low puts the regulator into shutdown mode over full operating range.
IN	8	I	Input pin. TI recommends a 0.1-µF ceramic or greater capacitor from this pin to ground to assure stability. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
GND	4	O	Ground. The exposed thermal pad is connected to ground through this pin.
OUT	1	O	Regulated output voltage pin. A small (1 µF) capacitor is needed from this pin to ground to assure stability.
SENSE/FB	2	I	This pin is the input to the control loop error amplifier; it is used to set the output voltage of the device.
NC	3, 6, 7	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN} Input voltage range	IN(2)	–65	60	V
	OUT	–0.3	28	V
	FB	–0.3	7	V
	EN(2)	–65	60	V
	Enable to IN differential	0.6	V_{IN}	V
T_J Junction temperature range(3)		–40	125	°C
T_{stg} Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient: 500 ms for V_{IN} > 50 V
(3) The junction temperature must not exceed 125ºC. See Figure 1 to determine the maximum ambient operating temperature versus the supply voltage and load current. The safe operating area curves assume a 50ºC/W thermal impedance and may need to be adjusted to match actual system thermal performance.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
	Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage	IN	–65	50	V
		OUT	–0.3	28	
		FB	–0.3	7	
		EN	–65	50	
I_{OUT}	Output current			50	mA
T_J	Operating junction temperature (1) (2) (3)		–40	125	°C
T_A	Ambient free-air temperature		–40	105	°C

(1) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.
(2) The TPS798xx-Q1 is specified to meet performance specifications from –40°C to 125°C operating junction temperature. Specifications over the full operating junction temperature range are specified by design, characterization, and correlation with statistical process controls.
(3) This device includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C (minimum) when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

6.4 Thermal Information

THERMAL METRIC (1)		TPS79801-Q1, TPS79850-Q1 DGN (MSOP-PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC 51-5 (2))	57.1	°C/W
	Junction-to-ambient thermal resistance (JEDEC 51-7 (3))	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal data is based on using JEDEC 51-5. The copper pad is soldered to the thermal land pattern and using 5 by 8 thermal array (vias). Correct attachment procedure must be incorporated.
(3) The thermal data is based on using JEDEC 51-7. The copper pad is soldered to the thermal land. No thermal vias. Correct attachment procedure must be incorporated.

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6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 1 V or 4 V (whichever is greater for either fixed or adjustable versions), I_{LOAD} = 1 mA, V_{EN} = 3 V, C_{OUT} = C_{IN} = 2.2 µF (unless otherwise noted). For TPS79801, FB pin tied to V_{OUT}. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		T_J(1)	MIN	TYP	MAX	UNIT
V_{IN}	Minimum input voltage	I_{LOAD} = 50 mA		Full range		3	4	V
Fixed V_{OUT}	Initial output voltage accuracy	V_{IN} = V_{OUT} nom + 0.5 V		25°C	–1.5%		1.5%	
	Output voltage accuracy over line, load, and full temperature range	V_{IN} = V_{OUT} nom + 1 V to 50 V, I_{LOAD} = 1 mA to 50 mA		Full range	–3%		3%	
Adjustable V_{OUT}	Initial output voltage accuracy	V_{IN} = 3 V		25°C	1.256	1.275	1.294	V
	Output voltage accuracy over line, load, and full temperature range	V_{IN} = 4 V to 50 V, I_{LOAD} = 1 mA to 50 mA		Full range	1.237	1.275	1.313	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation, adjustable V_{OUT}	ΔV_{IN} = 3 V to 50 V		Full range			13	mV
	Line regulation, TPS79850	V_{IN} = V_{OUT} nom + 0.5 V to 50 V					15	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation, adjustable V_{OUT}	ΔI_{LOAD} = 1 mA to 50 mA		25°C			20	mV
				Full range			32	
	Load regulation, fixed V_{OUT}	ΔI_{LOAD} = 1 mA to 50 mA		25°C			50	mV
				Full range			90	
Adjustable V_{OUT}	Output voltage range(2) (3)			Full range	1.275		28	V
V_{DO}	Dropout voltage(4) (5)	V_{IN} = $V_{OUT(NOM)}$ – 0.1 V		25°C		85	150	mV
				Full range			190	
		I_{LOAD} = 10 mA, V_{IN} = $V_{OUT(NOM)}$ – 0.1 V		25°C		170	260	
				Full range			350	
		I_{LOAD} = 50 mA, V_{IN} = $V_{OUT(NOM)}$ – 0.1 V		25°C		300	370	
				Full range			550	
I_{GND}	GND pin current(6)	V_{IN} = $V_{OUT(NOM)}$	I_{LOAD} = 0 mA	Full range		30	80	µA
			I_{LOAD} = 1 mA	Full range		100	180	
			I_{LOAD} = 10 mA	Full range		400	700	
			I_{LOAD} = 50 mA	Full range		1.8	3.3	mA
V_N	Output voltage noise	C_{OUT} = 10 µF, I_{LOAD} = 50 mA, BW = 10 Hz to 100 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V (adjustable used)		25°C		100		μV_{RMS}
I_{FB}	FB pin bias current(7)	V_{IN} = 3 V		25°C		0.05	0.2	µA
V_{EN}	EN pin high (enabled)(8)	OFF to ON, V_{IN} = 6 V		Full range			1.5	V
	EN pin low (shutdown)(8)	ON to OFF, V_{IN} = 6 V		25°C	0.4 V			V
	EN pin low (shutdown)(8)	ON to OFF, V_{IN} = 6 V		Full range	0.2 V			V
I_{EN}	EN pin current(8)	V_{EN} = 0 V V_{IN} = 6 V, I_{LOAD} = 0 mA		Full range		0.4	2	µA
		V_{EN} = 3 V, V_{IN} = 6 V, I_{LOAD} = 0 mA		Full range		0.4	0.5	
$I_{shutdown}$	GND pin current(6)	V_{IN} = 6 V, V_{EN} = 0 V, I_{LOAD} = 0 mA		Full range		3	25	µA
PSRR	Power-supply rejection ratio	V_{IN} = 4.3 V, V_{OUT} 3.3-V V_{RIPPLE} = 0.5 V_{PP}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 50 mA		25°C		65		dB
I_{LIMIT}	Fixed current limit(9)	ΔV_{OUT} = $V_{OUT(NOM)}$ – 0.1 V		Full range	60		200	mA
	Adjustable current limit	ΔV_{OUT} = $V_{OUT(NOM)}$ – 0.1 V		Full range	60		200	mA

(1) Full range T_J = –40°C to 125°C
(2) This parameter is tested and specified under pulse load conditions such that T_J = T_A. This device is 100% production tested at T_A = 25°C. Performance at full range is specified by design, characterization, bench to ATE correlation testing, and other statistical process controls.
(3) This device is limited by a maximum junction temperature of T_J = 125°C. The regulated output voltage specification cannot be applied to all combinations of various V_{IN}, V_{OUT}, ambient temperature, and I_{OUT} conditions. When operating with large voltage differentials across the device, the output load must be limited so as not to violate the maximum junction temperature for a given ambient temperature.
(4) In the adjustable version test, the output uses an external voltage divider. This resistor voltage divider is made up of R_1 = 215 kΩ and R2 (bottom resistor) = 340 kΩ. This configuration preloads the output with 6 µA.
(5) By definition, dropout voltage is the minimum input voltage needed to maintain a given output voltage at a specific load current. For dropout testing, minimum V_{IN} = $V_{OUT(NOM)}$ × 0.96. This specification ensures that the device is in dropout and takes into account the output voltage tolerance over the full temperature range.
(6) Ground pin current is tested with V_{IN} = $V_{OUT(NOM)}$ or 3 V, whichever is greater.
(7) FB pin current flows into the FB pin.
(8) EN pin current flows into the EN pin.
(9) Current limit is tested with V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 3 V, whichever is greater. V_{OUT} is forced to $V_{OUT(NOM)}$ – 0.1 V and the output current is measured.

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Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 1 V or 4 V (whichever is greater for either fixed or adjustable versions), I_{LOAD} = 1 mA, V_{EN} = 3 V, C_{OUT} = C_{IN} = 2.2 µF (unless otherwise noted). For TPS79801, FB pin tied to V_{OUT}. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	T_J(1)	MIN	TYP	MAX	UNIT
I_{RL}	Input reverse leakage current(reverse battery test)	V_{IN} = –60 V, V_{OUT} = open, C_{IN} open	Full range			6	mA
I_{RO}	Reverse output current(10)	V_{OUT} = $V_{OUT(NOM)}$, V_{IN} = ground	25°C		19	25	µA
T_{SD}	Thermal shutdown temperature (T_J)(11)	Shutdown, temperature increasing		135			°C
		Reset, temperature decreasing		135			

(10) Reverse output current is tested with the IN pin tied to ground and the output forced to $V_{OUT(NOM)}$ +0.1 V. This current flows into the OUT pin and out of the GND pin and then measured.
(11) Specified by design

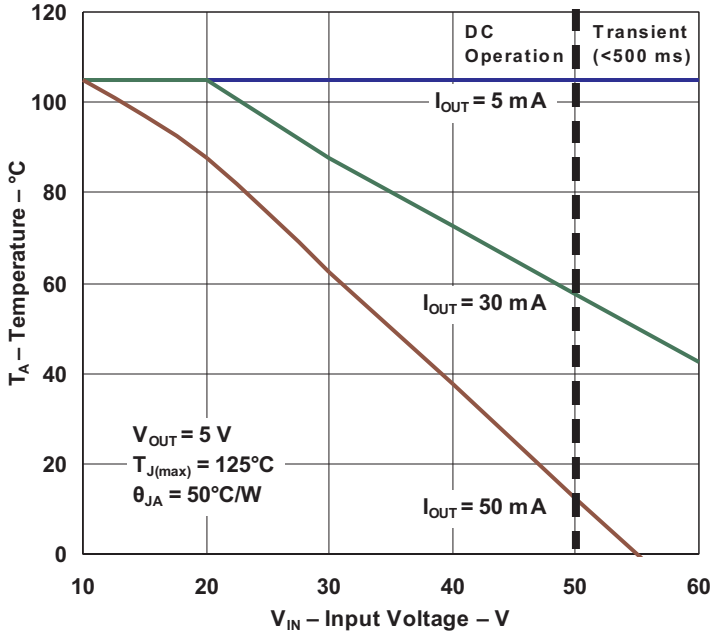


Figure 1. Safe Operating Area

6.6 Dissipation Ratings(1)

BOARD	PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
High-K(2)	DGN	16.6 mW/°C	1.83 W	1.08 W	0.833 W

(1) See *Thermal Considerations* for more information related to thermal design.
(2) The JEDEC High-K (1s) board design used to derive this data was a 4.5-inch × 3-inch, 2-layer board with 2-ounce copper traces on top of the board.

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6.7 Typical Characteristics

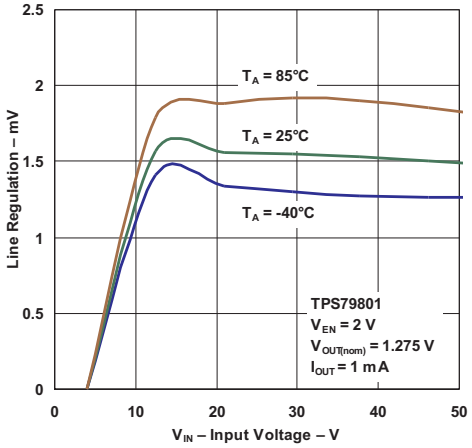


Figure 2. Line Regulation vs Input Voltage

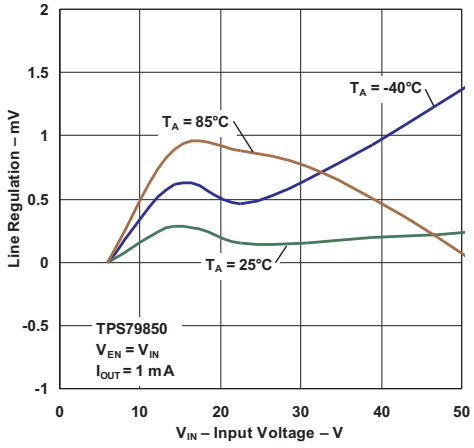


Figure 3. Line Regulation vs Input Voltage

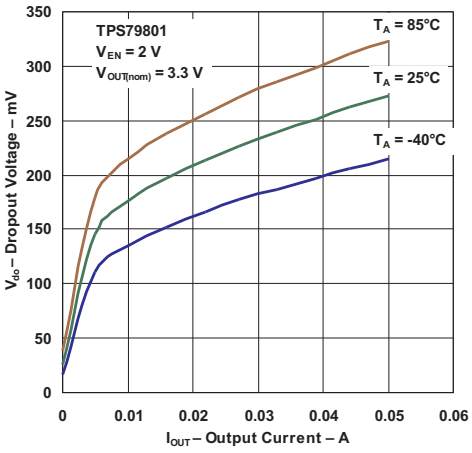


Figure 4. Dropout Voltage vs Output Current

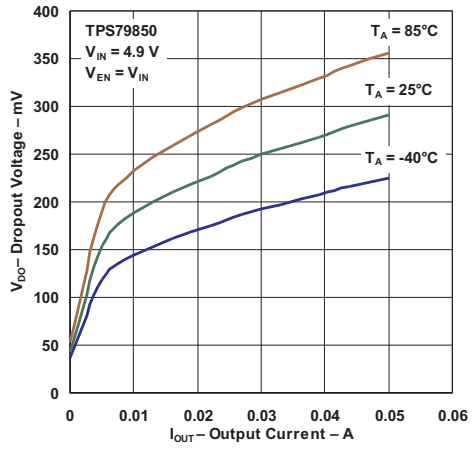


Figure 5. Dropout Voltage vs Output Current

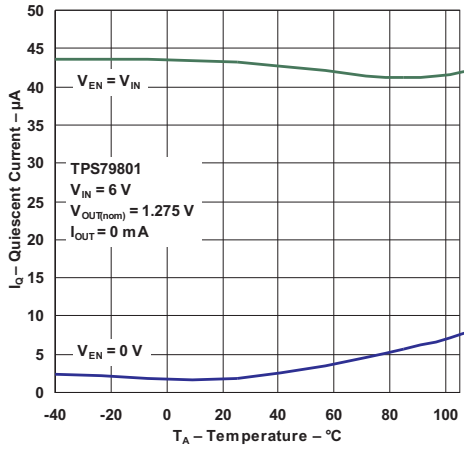


Figure 6. Quiescent Current vs Temperature

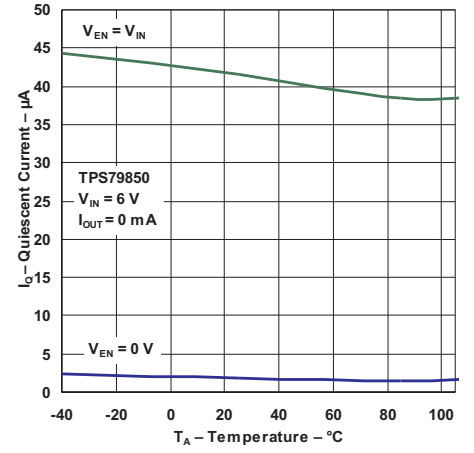


Figure 7. Quiescent Current vs Temperature

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Typical Characteristics (continued)

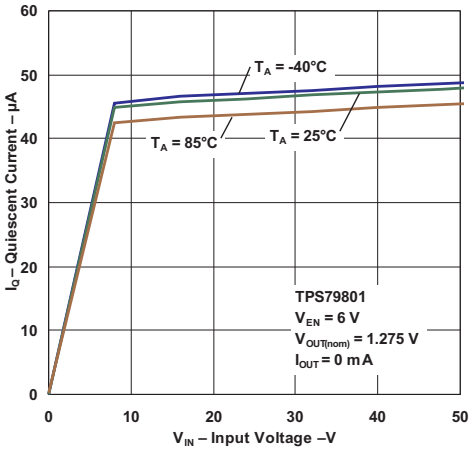


Figure 8. Quiescent Current vs Input Voltage

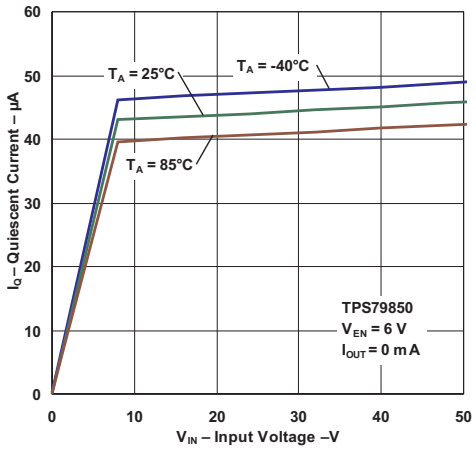


Figure 9. Quiescent Current vs Input Voltage

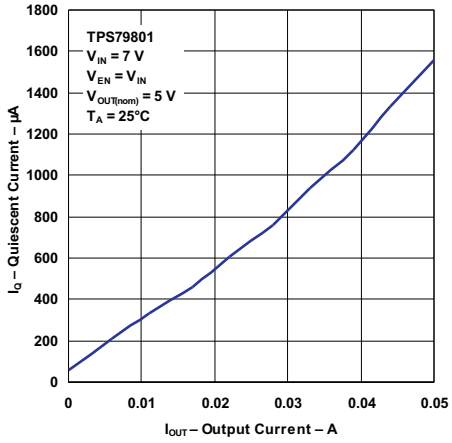


Figure 10. Quiescent Current vs Output Current

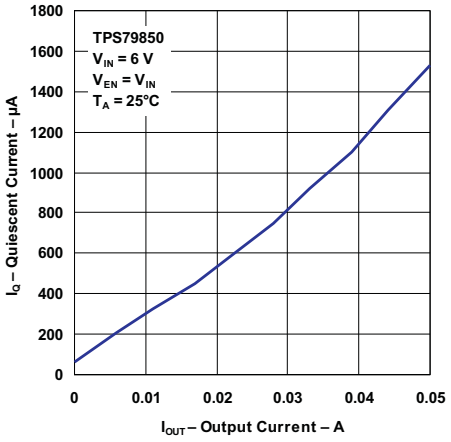


Figure 11. Quiescent Current vs Output Current

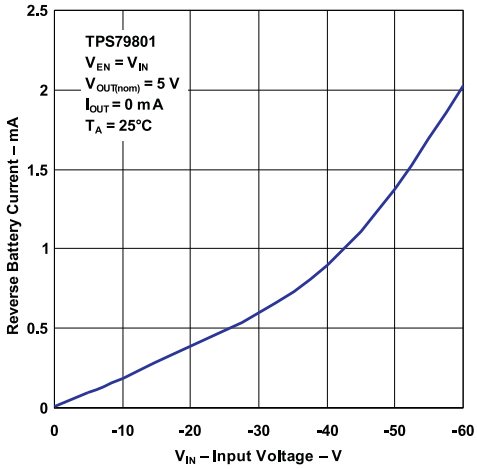


Figure 12. Reverse Battery Leakage vs Input Voltage

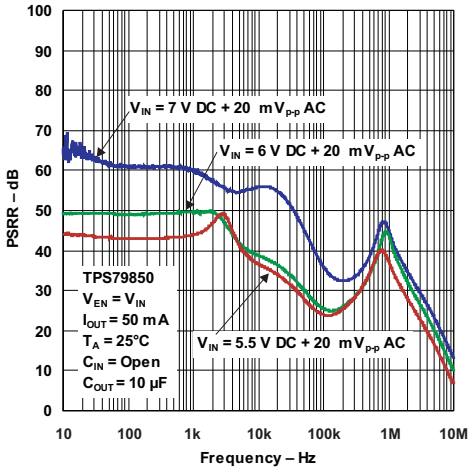


Figure 13. Power Supply Ripple Rejection vs Frequency

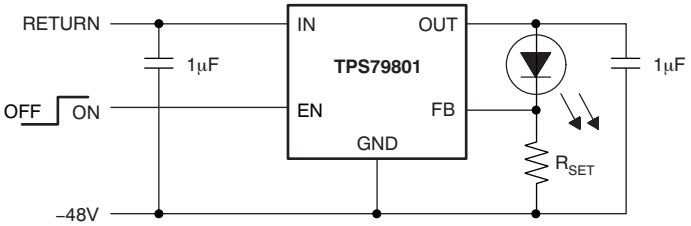
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7 Detailed Description

7.1 Overview

The TPS798xx-Q1 is a 50-mA high-voltage LDO regulator with micropower quiescent current and shutdown. The device is capable of supplying 50 mA at a dropout voltage of 300 mV (typical). The low operating quiescent current (40 µA) drops to 1 µA in shutdown. In addition to the low quiescent current, the TPS798xx-Q1 incorporates several protection features that make it ideal for battery-powered applications.

The device is protected against both reverse-input and reverse-output voltages. In battery-backup applications, where the output can be held up by a backup battery when the input is pulled to ground, the TPS798xx-Q1 acts as if it has a diode in series with its output and prevents reverse current flow. Figure 14 and Figure 15 illustrate two typical applications.



I_{LED} = 1.275 V/R_{SET}
–48 V can vary from –4 V to –50 V

Figure 14. Constant Brightness for Indicator LED Over Wide Input Voltage Range

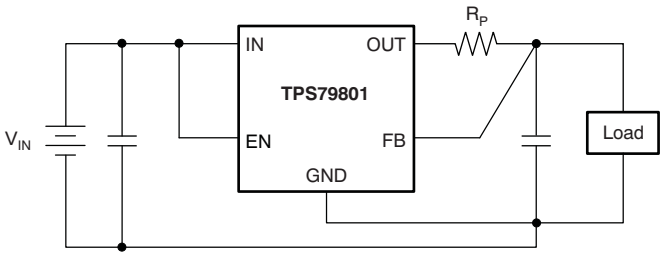


Figure 15. Kelvin Sense Connection

7.2 Functional Block Diagram

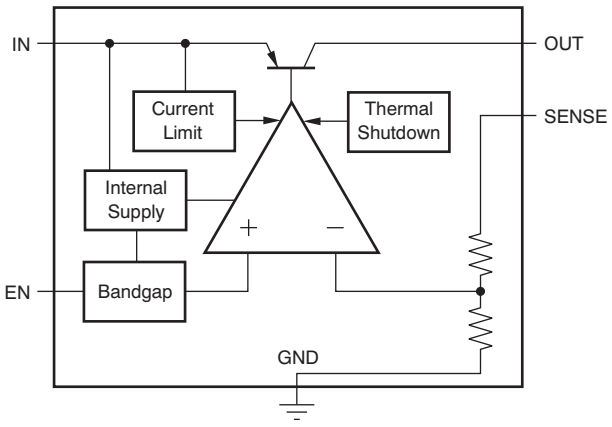


Figure 16. Fixed Voltage Output Version

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Functional Block Diagram (continued)

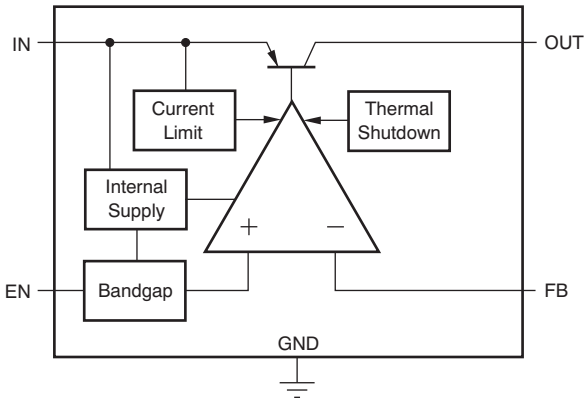
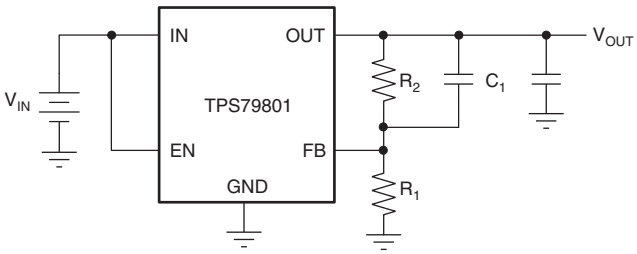


Figure 17. Adjustable Voltage Output Version

7.3 Feature Description

7.3.1 Adjustable Operation

The TPS798xx-Q1 has an output voltage range of 1.275 V to 28 V. The output voltage is set by the ratio of two external resistors as shown in Figure 18. The feedback loop monitors the output to maintain the voltage at the adjust pin at 1.275 V referenced to ground. The current in R_1 is then equal to 1.275 V/R_1, and the current in R_2 is the current in R_1 plus the FB pin bias current. The FB pin bias current, 0.2 µA at 25°C, flows through R_2 into the FB pin. The output voltage can be calculated using the formula in Figure 18. The value of R_1 should be less than 250 kΩ to minimize errors in the output voltage caused by the FB pin bias current. Note that in shutdown, the output is turned off and the divider current is zero.



$V_{OUT} = 1.275\ V\ (1 + R_2 / R_1) + I_{FB}R_2$
$V_{FB} = 1.275\ V$
$I_{FB} = 0.2\ \mu A$ at 25°C
Output Range = 1.275 V to 28 V

Figure 18. Adjustable Operation

A 100-pF capacitor (C_1) placed in parallel with the top resistor (R_2) of the output divider is necessary for stability and transient performance of the adjustable TPS798xx-Q1. The impedance of C_1 at 10 kHz should be less than the value of R_2.

The adjustable device is tested and specified with the FB pin tied to the OUT pin and a 1 mA-DC load (unless otherwise specified) for an output voltage of 1.275 V. Specifications for output voltages greater than 1.275 V are proportional to the ratio of the desired output voltage to 1.275 V (V_{OUT}/1.275 V). For example, load regulation for an output current change of 1 mA to 50 mA is –10 mV (typical) at V_{OUT} = 1.275 V.

At V_{OUT} = 12 V, load regulation is:

$$(12\ V/1.275\ V) \times (-10\ mV) = -94\ mV \quad (1)$$

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Feature Description (continued)

7.3.2 Output Capacitance and Transient Response

The TPS798xx-Q1 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. To prevent oscillations, TI recommends a minimum output capacitor of 1 µF with an ESR of 3 Ω or less. The TPS798xx-Q1 is a micropower device, and output transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS798xx-Q1, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5 V, X5R, and X7R. The Z5U and Y5 V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5 V regulator, a 10-µF Y5 V capacitor can exhibit an effective value as low as 1 µF to 2 µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals because of mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

7.3.3 Calculating Junction Temperature

Given an output voltage of 5 V, an input voltage range of 15 V to 24 V, an output current range of 0 mA to 50 mA, and a maximum ambient temperature of 50°C, the maximum junction temperature is calculated as follows.

The power dissipated (P_{DISS}) by the DGN package is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where

- $I_{OUT(MAX)}$ = 50 mA
- $V_{IN(MAX)}$ = 24 V
- V_{OUT} = 5 V
- I_{GND} at (I_{OUT} = 50 mA, V_{IN} = 24 V) = 1 mA (2)

Therefore,

$$P_{DISS} = 50\ mA\ (24\ V - 5\ V) + 1\ mA\ (24\ V) = 0.974\ W \quad (3)$$

The thermal resistance is approximately 60°C/W, based on JEDEC 51-5 profile. Therefore, the junction temperature rise above ambient is approximately equal to:

$$0.974\ W \times 60°C/W = 58.44°C \quad (4)$$

The maximum junction temperature is then equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_J\ max = 50°C + 58.44°C = 108.44°C \quad (5)$$

7.3.4 Protection Features

The TPS798xx-Q1 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse-input voltages, and reverse currents from output to input.

Current limit protection and thermal-overload protection are intended to protect the device against current overload conditions at the output of the device. The junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of –60 V. Current flow into the device is limited to less than 6 mA (typically, less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This architecture also provides protection against batteries that may be plugged in backwards.

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Feature Description (continued)

The FB pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open or grounded, the FB pin behaves as an open circuit when pulled below ground, or as a large resistor (typically, 100 kΩ) in series with a diode when pulled above ground. If the input is powered by a voltage source, pulling the FB pin below the reference voltage increases the output voltage. This configuration causes the output to go to a unregulated high voltage. Pulling the FB pin above the reference voltage turns off all output current.

In situations where the FB pin is connected to a resistor divider that would pull the FB pin above its 7-V clamp voltage if the output is pulled high, the FB pin input current must be limited to less than 5 mA. For example, a resistor divider provides a regulated 1.5-V output from the 1.275-V reference when the output is forced to 28 V. The top resistor of the resistor divider must be chosen to limit the current into the FB pin to less than 5 mA when the FB pin is at 7 V. The 21-V difference between the OUT and FB pins divided by the 5-mA maximum current into the FB pin yields a minimum top resistor value of 5.8 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open. The rise in reverse output current above 7 V occurs from the breakdown of the 7-V clamp on the FB pin. With a resistor divider on the regulator output, this current is reduced, depending on the size of the resistor divider.

When the IN pin of the TPS798xx-Q1 is forced below the OUT pin, or the OUT pin is pulled above the IN pin, input current typically drops to less than 0.6 mA. This scenario can occur if the input of the TPS798xx-Q1 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin has no effect on the reverse output current when the output is pulled above the input.

7.4 Device Functional Modes

7.4.1 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current and switch resistance. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

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8 Application and Implementation

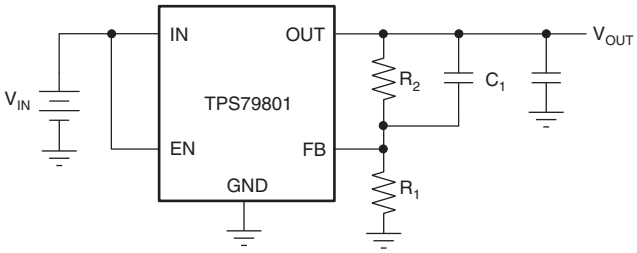
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 19 shows typical application circuits for the TPS79801-Q1 device. Based on the end-application, different values of external components can be used.

8.2 Typical Application



$V_{OUT} = 1.275\ V\ (1 + R_2 / R_1) + I_{FB}R_2$
$V_{FB} = 1.275\ V$
$I_{FB} = 0.2\ \mu A$ at 25°C
Output Range = 1.275 V to 28 V

Figure 19. Adjustable Operation Example

8.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3 V to 50 V
Output voltage	5 V
Output current rating	50 mA
Output capacitor range	1 µF to 100 µF

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

1. Input voltage range
2. Output voltage
3. Output current rating
4. Output capacitor

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8.2.3 Application Curves

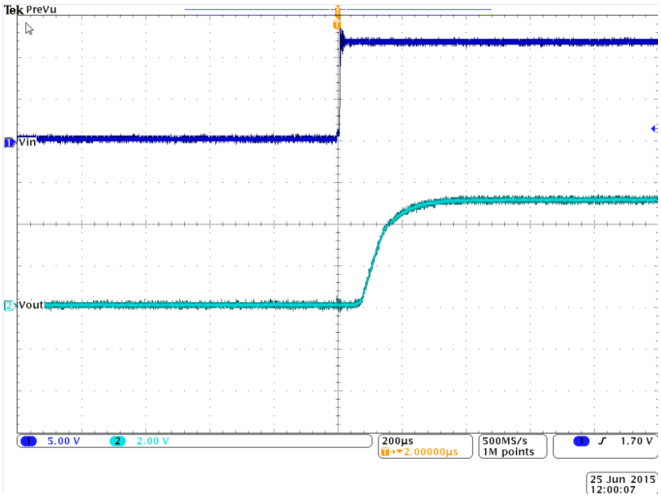


Figure 20. CH1: Vin, CH2: Vout Power-Up Waveform (Load = 50 mA)

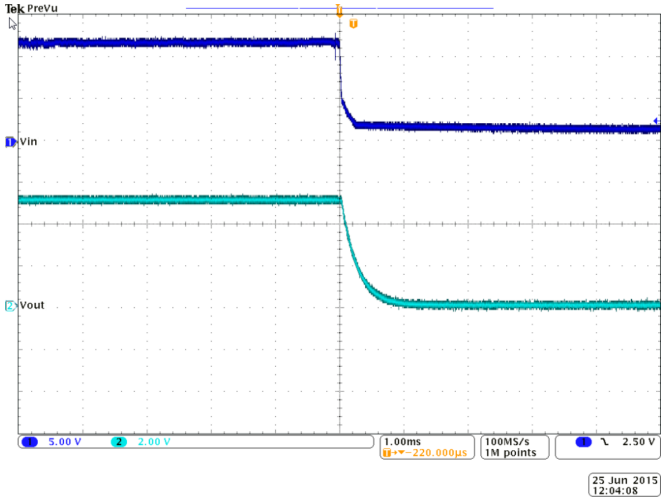


Figure 21. CH1: Vin, CH2: Vout Power-Down Waveform (Load = 50 mA)

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9 Power Supply Recommendations

9.1 Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device consists of two components:

- Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} – V_{OUT})$
- GND pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$

The GND pin current can be found by examining the GND pin current curves in the *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed previously.

The TPS798xx-Q1 series regulators have internal thermal limiting designed to protect the device during overload conditions. Do not exceed the maximum junction temperature rating of 125°C. It is important to carefully consider all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

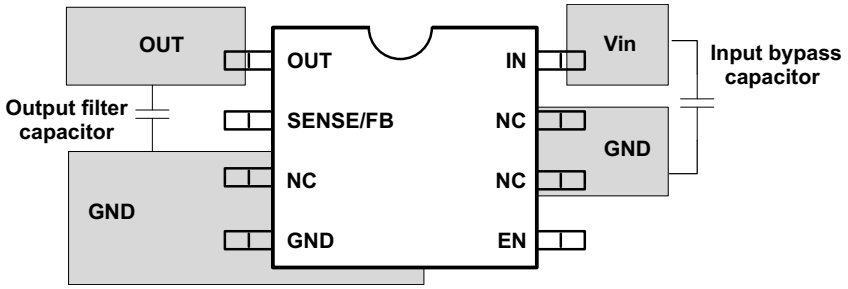
For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the printed-circuit-board (PCB) and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

10 Layout

10.1 Layout Guidelines

- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages using vias and long traces because of the negative impact on system performance. Vias and long traces can also cause instability.
- Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor must be placed as close to the device as possible and on the same side of the PCB as the regulator.

10.2 Layout Example



10.3 Thermal Considerations

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature (T_J max) above which normal operation is not assured. The operating environment must be designed so that the operating junction temperature (T_J) does not exceed the maximum junction temperature (T_J max). The two primary environmental variables that can be used to improve thermal performance are air flow and external heatsinks. The purpose of this section is to help the designer to determine the proper operating environment for a linear regulator that operates at a specific power level.

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Thermal Considerations (continued)

In general, the maximum expected power (P_D max) consumed by a linear regulator is computed as shown in Equation 6:

$$P_D max = (V_{IN(avg)} – V_{OUT(avg)}) × I_{OUT(avg)} + V_{I(avg)} × I_Q \quad (6)$$

where

- $V_{IN(avg)}$ is the average input voltage.
- $V_{OUT(avg)}$ is the average output voltage.
- $I_{OUT(avg)}$ is the average output current.
- I_Q is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)} × I_Q$ can be ignored. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature as a result of the regulator power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measurements of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the device thermal resistance.

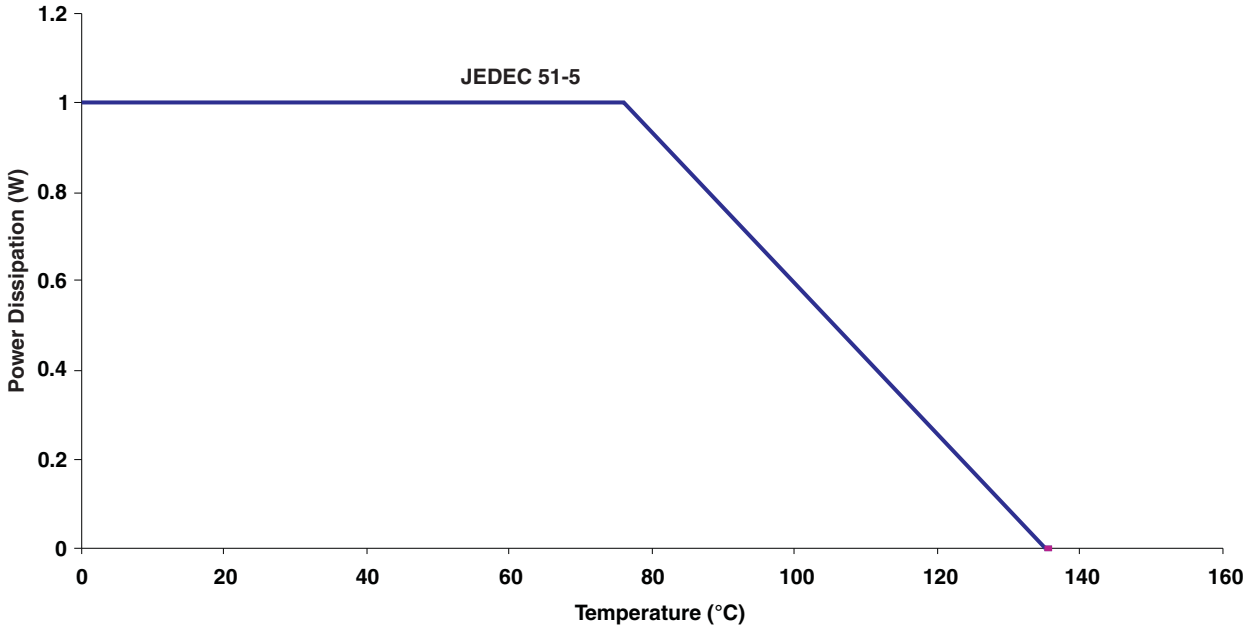


Figure 22. Power Dissipation vs Temperature

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11 Device and Documentation Support

11.1 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS79801-Q1	Click here	Click here	Click here	Click here	Click here
TPS79850-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79801QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMRQ	Samples
TPS79850QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOLQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

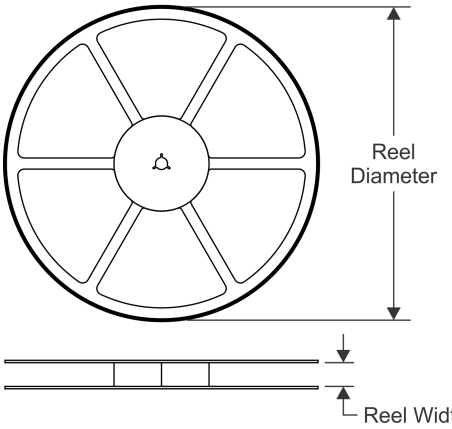
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

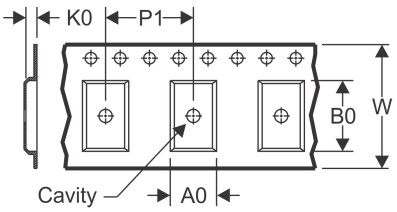
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

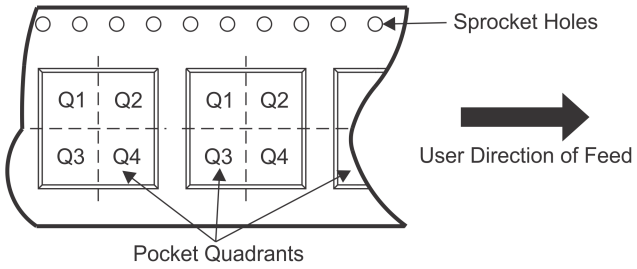


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

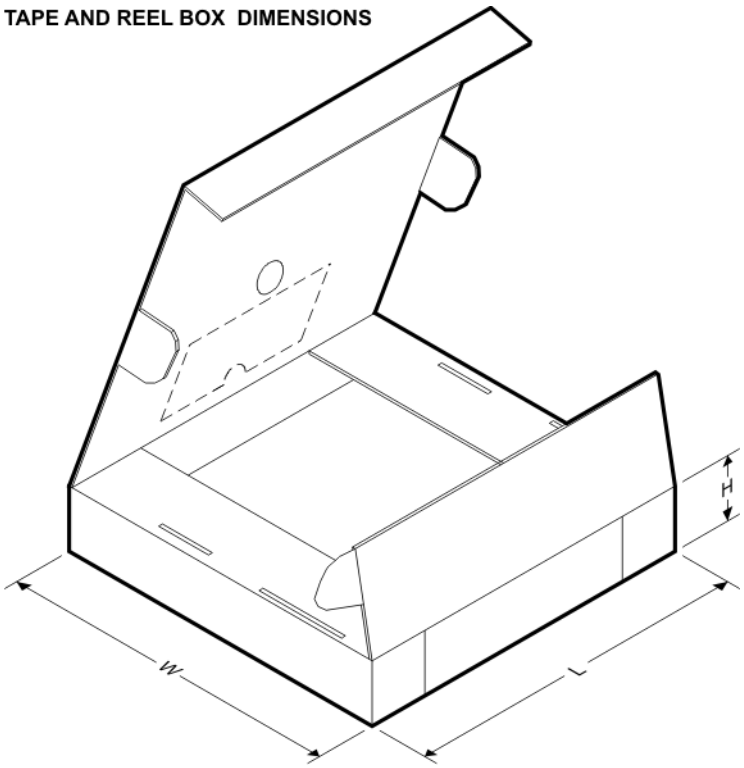
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79801QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS79850QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

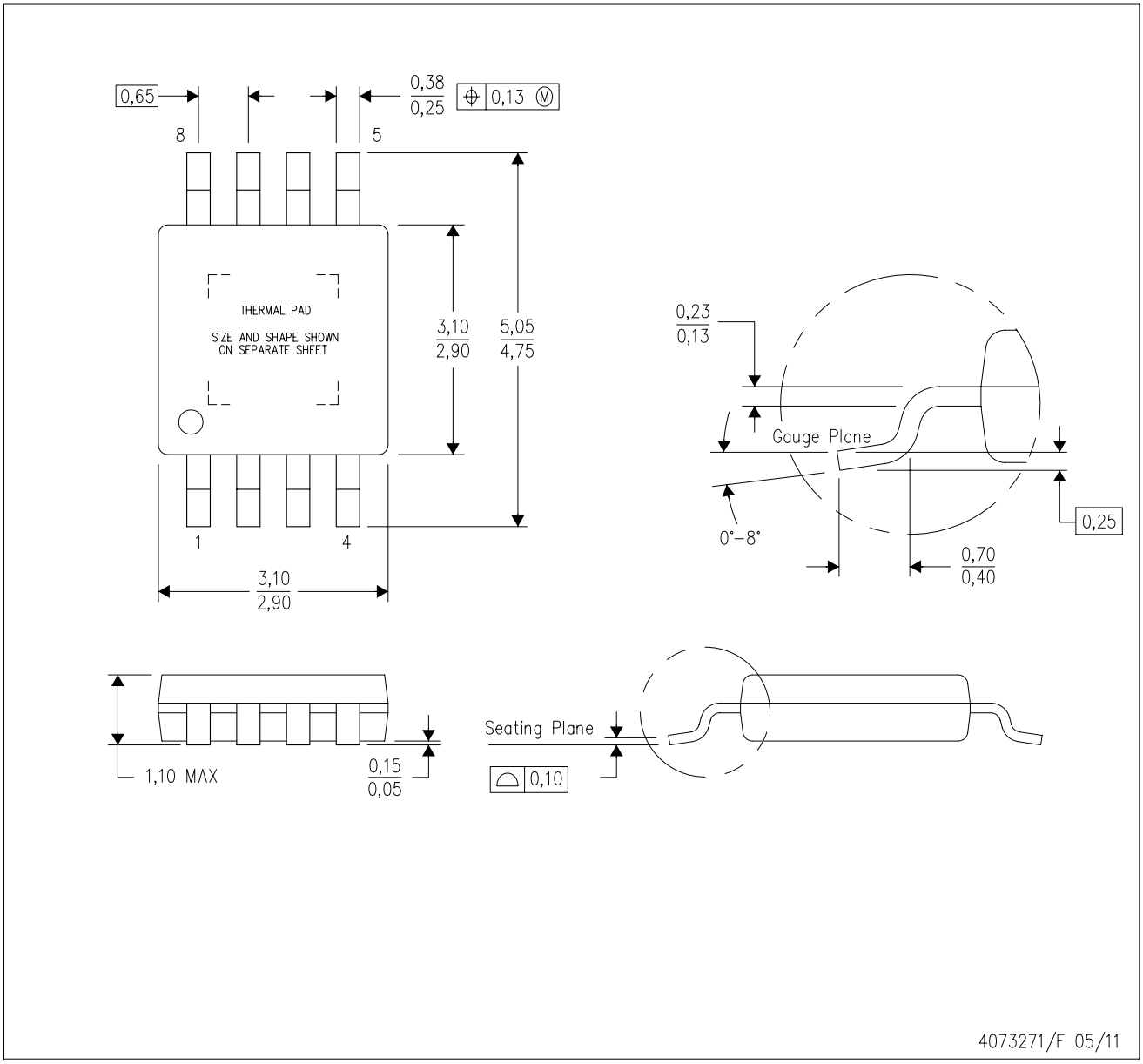
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79801QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS79850QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

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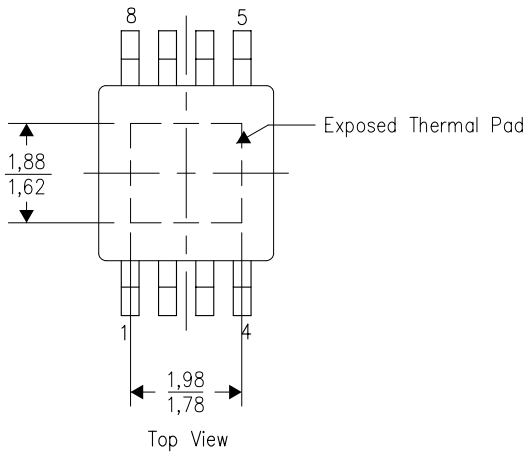
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



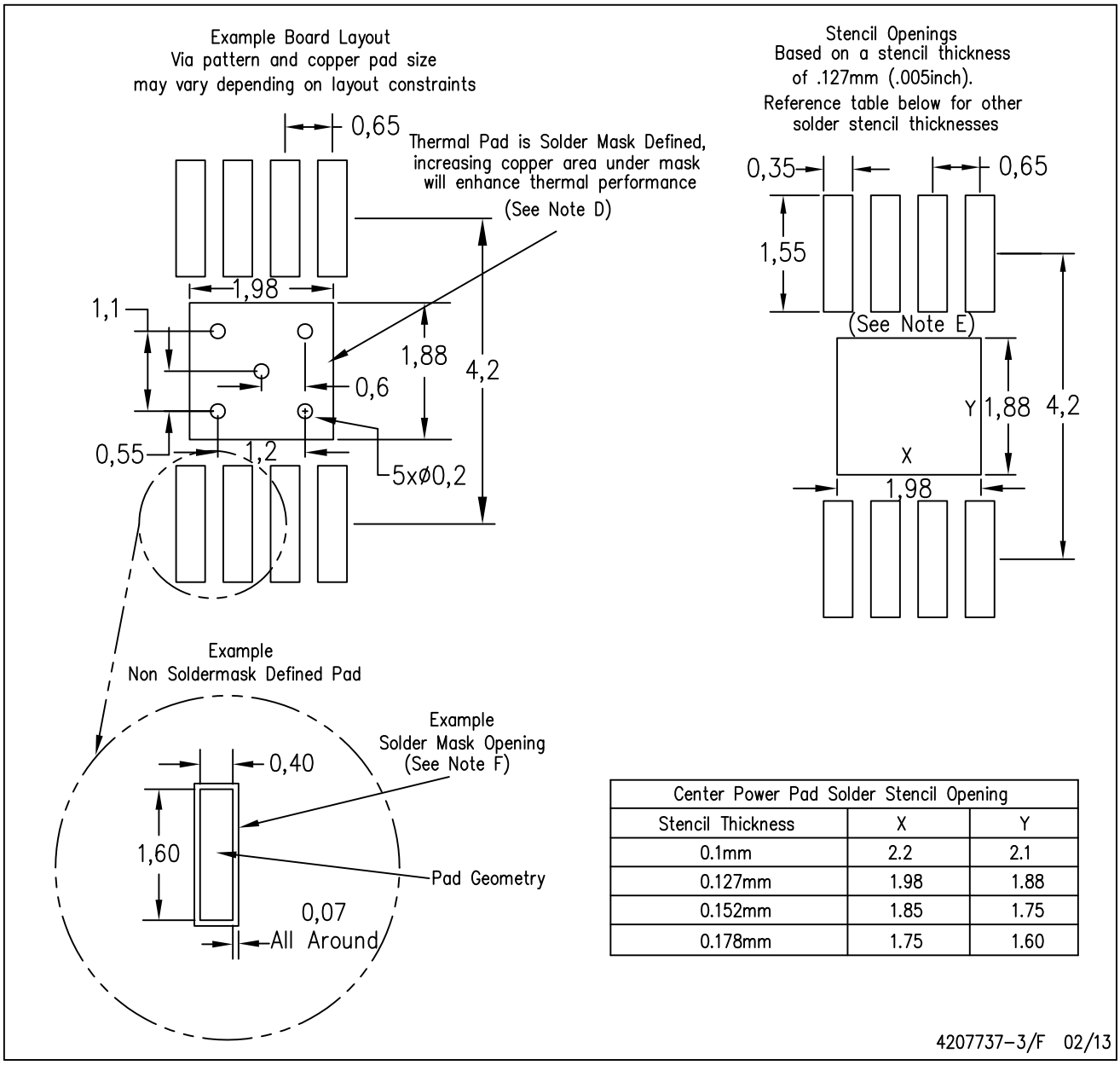
Exposed Thermal Pad Dimensions

4206323–3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737–3/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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