TPS82740x 360nA I_Q MicroSIP™ 降压转换器模块，用于低功率应用

1 特性

- 360nA 静态电流典型值
- 10µA 输出电流时的效率高达 90%
- 引脚可选输出电压，步长 100mV
- 集成转换率受控负载开关
- 高达 200mA 输出电流
- 2.2V 至 5.5V 的输入电压范围 V_{IN}
- 射频 (RF) 友好型 DCS-Control™
- 低输出电压纹波
- 自动转换至无纹波 100% 模式
- VOUT 和 LOAD 上的放电功能
- 高度不到 1.1mm 的解决方案
- 总体解决方案尺寸 < 6.7mm^2
- 小型 2.3mm x 2.9mm MicroSIP™ 封装

2 应用范围

- *Bluetooth*® 低功耗 (Low Energy)，消费类电子产品用射频 (RF4CE)，短距低功耗通信协议 (Zigbee)
- 可穿戴电子产品
- 能量采集

3 说明

TPS82740 是业界第一款降压转换器模块，此模块特有典型值为 360nA 的静态流耗。 它是一款用于超低功率应用的完整 MicroSIP™ 直流/直流降压电源解决方案。 此模块包括开关稳压器、电感器和输入/输出电容器。 将所有需要的无源组件集成在一起可实现仅为 6.7mm^2 的微型解决方案尺寸。

这款全新的基于 DCS-Control™ 的器件将轻负载效率范围拓展至 10µA 负载电流以下。 它支持高达 200mA 的输出电流。

此器件由可再充电锂离子电池，锂化学电池（例如锂亚硫酰氯 (Li-SOC12)，锂锰电池 (Li-MnO2)）和两节或三节碱性电池供电运行。 输入电压范围高达 5.5V，也可实现由 1 个 USB 端口和薄膜太阳能模块供电运行。

用户可通过三个电压选择引脚 (VSEL) 在 1.8V 至 2.5V (TPS82740A) 和 2.6V 至 3.3V (TPS82740B) 的范围内以 100mV 的步长选择输出电压。 TPS82740 特有低输出电压纹波和低噪声。 一旦电池电压接近输出电压（接近 100% 占空比），此器件进入无纹波 100% 模式运行，以防止增加输出电压纹波。 在这个情况下，此器件停止开关，并且输出被连接至输入电压。

集成的转换率受控负载开关（具有 0.6Ω 的导通电阻典型值）将已选输出电压配送至一个临时使用的子系统。

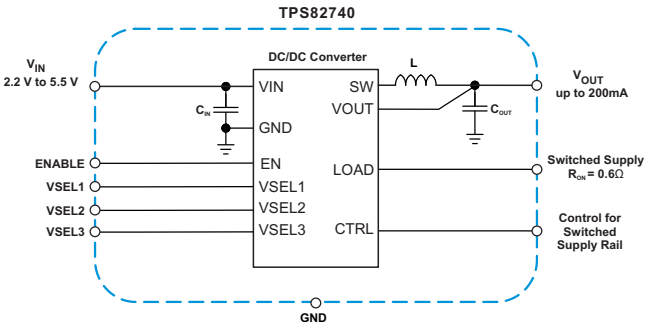
TPS82740 采用小型 9 焊锡凸点 6.7mm^2 MicroSiP™ 封装。

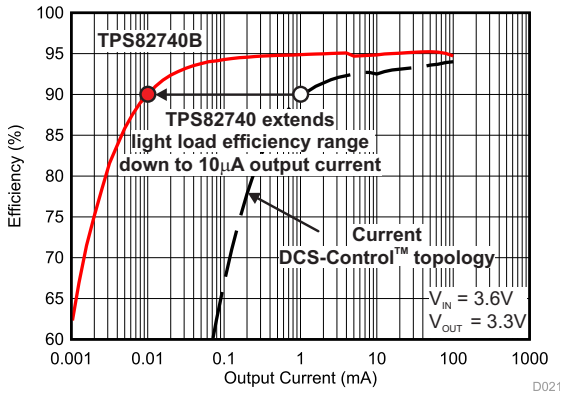
器件信息(1)

产品型号	封装	封装尺寸（标称值）
TPS82740A	µSIP	2.30mm x 2.90mm
TPS82740B	µSIP	2.30mm x 2.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型应用





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5 修订历史记录

Changes from Original (June 2014) to Revision A **Page**

- Added 150 mA Typical current specification for $I_{LIM_softstart}$, Low side MOSFET switch current limit ... 6

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6 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE SETTINGS (VSEL1, VSEL2, VSEL3)	PACKAGE MARKING
TPS82740A	1.8V to 2.5V in 100mV steps	E7
TPS82740B	2.6V to 3.3V in 100mV steps	E8

7 Pin Configuration and Functions

MicroSIP™
9 Bump

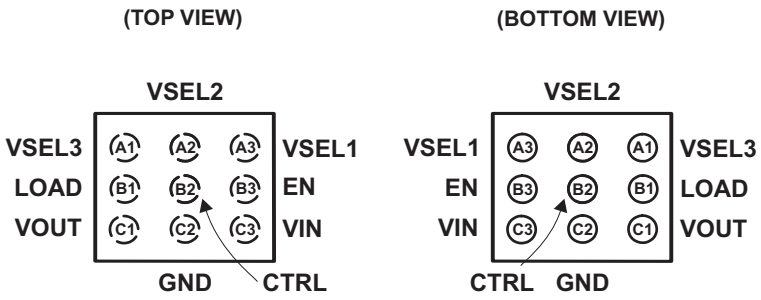


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	C3	IN	Input voltage supply pin of the module.
GND	C2	-	Ground terminal.
CTRL	B2	IN	CTRL pin controls the LOAD output pin. With CTRL = low, the LOAD output is disabled. This pin must be terminated and not left floating.
VOUT	C1	OUT	Output voltage pin of the module. An internal load switch is connected between VOUT pin and LOAD pin.
LOAD	B1	OUT	Load switch output pin controlled by the CTRL pin. With CTRL = high, an internal load switch connects the LOAD pin to the VOUT pin. The LOAD pin allows connect / disconnect other system components to the output of the DC/DC converter. This pin is pulled to GND with the CTRL pin = low. The LOAD pin features soft switching. If not used, leave the pin open.
VSEL3	A1	IN	Output voltage selection pins. See Table 2 and Table 3 for V_{OUT} selection. These pins must be terminated and can be changed during operation.
VSEL2	A2	IN	
VSEL1	A3	IN	
EN	B3	IN	High level enables the devices and low level turns the device into shutdown mode. This pin must be terminated and not left floating.

Table 2. Output Voltage Setting TPS82740A

Device	VOUT	VSEL3	VSEL2	VSEL1
TPS82740A	1.8	0	0	0
	1.9	0	0	1
	2.0	0	1	0
	2.1	0	1	1
	2.2	1	0	0
	2.3	1	0	1
	2.4	1	1	0
	2.5	1	1	1

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Table 3. Output Voltage Setting TPS82740B

Device	VOUT	VSEL3	VSEL2	VSEL1
TPS82740B	2.6	0	0	0
	2.7	0	0	1
	2.8	0	1	0
	2.9	0	1	1
	3.0	1	0	0
	3.1	1	0	1
	3.2	1	1	0
	3.3	1	1	1

8 Specifications

8.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Pin voltage (2)	VIN	–0.3	6	V
	EN, CTRL, VSEL1, VSEL2, VSEL3	–0.3	V_{IN} +0.3V	V
	VOUT, LOAD	–0.3	3.7	V
Operating ambient temperature range, T_A (3)		-40	85	°C
Operating junction temperature T_J		-40	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) In applications where ambient temperature (T_A) constantly stays above 70°C, the product life time might degrade. MLCC capacitor reliability and lifetime is depending on temperature and applied voltage conditions. At higher temperatures, MLCC capacitors are subject to stronger stress. The most critical parameter is the Insulation Resistance (IR) resulting in leakage current.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}		2.2		5.5	V
I_{OUT} + I_{LOAD}	Device output current (sum of I_{OUT} and I_{LOAD})	V_{OUTnom} + 0.7V ≤ V_{IN} ≤ 5.5V			200	mA
		V_{OUTnom} ≤ V_{IN} ≤ V_{OUTnom} +0.7V			100	
I_{LOAD}	Load current (current from LOAD pin)				100	
C_{OUT}	Additional output capacitance connected to VOUT pin (not including LOAD pin)				10	µF
C_{LOAD}	Capacitance connected to LOAD pin				10	
T_J	Operating junction temperature range		-40		90	°C
T_A	Operating ambient temperature range		-40		85	

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8.4 Thermal Information

THERMAL METRIC(1)		TPS82740 µSIP 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	
$R_{\theta JB}$	Junction-to-board thermal resistance	-	
ψ_{JT}	Junction-to-top characterization parameter	-	
ψ_{JB}	Junction-to-board characterization parameter	-	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_{IN} = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.2		5.5	V
I_Q	Operating quiescent current	EN = V_{IN}, CTRL = GND, I_{OUT} = 0µA, V_{OUT} = 1.8V / 2.6V, device not switching			360	2300	nA
		EN = V_{IN}, I_{OUT} = 0mA, CTRL = GND, V_{OUT} = 1.8V device switching			460		
		EN = V_{IN}, I_{OUT} = 0mA, CTRL = GND, V_{OUT} = 2.6V, device switching			500		
		EN = V_{IN}, I_{OUT} = 0mA., CTRL = V_{IN}, V_{OUT} = 1.8V, device not switching			12.5		µA
		EN = V_{IN}, I_{OUT} = 0mA., CTRL = V_{IN}, V_{OUT} = 2.6V, device not switching			13.5		
I_{SD}	Shutdown current	EN = GND, shutdown current into V_{IN}			70		nA
		EN = GND, shutdown current into V_{IN}, T_A = 60°C			150		
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}			2.075	2.15	V
V_{TH_UVLO-}		Falling V_{IN}			1.925	2	
INPUTS EN, CTRL, VSEL 1-3							
$V_{IH\ TH}$	High level input threshold	2.2V ≤ V_{IN} ≤ 5.5V				1.1	V
$V_{IL\ TH}$	Low level input threshold	2.2V ≤ V_{IN} ≤ 5.5V		0.4			V
I_{IN}	Input bias Current	T_A = 25°C				10	nA
		T_A = –40°C to 85°C				25	
POWER SWITCHES							
I_{LIMF}	High side MOSFET switch current limit	2.2V ≤ V_{IN} ≤ 5.5V			430		mA
	Low side MOSFET switch current limit				430		mA
OUTPUT DISCHARGE SWITCH (VOUT)							
R_{DSCH_VOUT}	MOSFET on-resistance	EN = GND, I_{OUT} = -10mA into VOUT pin			30	65	Ω
I_{IN_VOUT}	Bias current into VOUT pin	EN = V_{IN}, V_{OUT} = 2V / 2.8V, CTRL = GND	T_A = 25°C		40	660	nA
			T_A = –40°C to 85°C			1570	
LOAD OUTPUT (LOAD)							
R_{LOAD}	High side MOSFET on-resistance	I_{LOAD} = 50mA, CTRL = V_{IN}, V_{OUT} = 2.0V / 2.8V, 2.2 V ≤ V_{IN} ≤ 5.5V			0.6	1.25	Ω
R_{DSCH_LOAD}	Low side MOSFET on-resistance	CTRL = GND, 2.2V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = - 10mA			30	65	
t_{Rise_LOAD}	V_{LOAD} rise time	Starting with CTRL low to high transition, time to ramp V_{LOAD} from 0V to 95%, V_{OUT} = 1.8V / 2.6V, 2.2V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 1mA, T_A = 25°C			315	800	µs

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Electrical Characteristics (continued)

V_{IN} = 3.6V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUTO 100% MODE TRANSITION							
V_{TH_100+}	Auto 100% Mode exit detection threshold (1)	Rising V_{IN},100% Mode is left with $V_{IN} = V_{OUT} + V_{TH_100+}$, max value at T_J = 85°C		170	250	340	mV
V_{TH_100-}	Auto 100% Mode enter detection threshold (1)	Falling V_{IN}, 100% Mode is entered with $V_{IN} = V_{OUT} + V_{TH_100-}$, max value at T_J = 85°C		110	200	280	
OUTPUT							
$t_{Startup_delay}$	Regulator start up delay time	From transition EN = low to high until device starts switching			10	25	ms
$t_{Softstart}$	Softstart time with reduced switch current limit	2.2V ≤ V_{IN} ≤ 5.5V, EN = V_{IN}			400	1200	µs
$I_{LIM_softstart}$	High side MOSFET switch current limit	Reduced switch current limit during softstart		80	150	200	mA
	Low side MOSFET switch current limit				150		
V_{VOUT}	Output voltage range	Output voltages are selected with pins VSEL1, VSEL2, VSEL3	TPS82740A	1.8		2.5	V
			TPS82740B	2.6		3.3	
	Output voltage accuracy	I_{OUT} = 10mA, V_{OUT} = 1.8V / 2.6V		-2.5	0	2.5	%
		I_{OUT} = 100mA, V_{OUT} = 1.8V / 2.6V		–2	0	2	
	DC output voltage load regulation	V_{OUT} = 1.8V / 2.6V, CTRL = V_{IN}			0.001		%/mA
	DC output voltage line regulation	V_{OUT} = 1.8V / 2.6V, CTRL = V_{IN}, I_{OUT} = 10 mA, 2.5V ≤ V_{IN} ≤ 5.5V			0		%/V

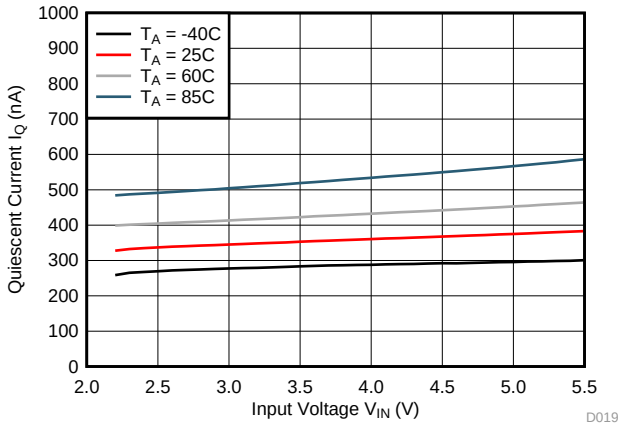
(1) V_{IN} is compared to the programmed output voltage (V_{OUT}). When V_{IN}–V_{OUT} falls below V_{TH_100-} , the device enters 100% Mode by turning the high side MOSFET on. 100% Mode is exited when V_{IN}–V_{OUT} exceeds V_{TH_100+} and the device starts switching. The hysteresis for the 100% Mode detection threshold V_{TH_100+} - V_{TH_100-} is always positive and 50 mV(typ.)

8.6 Typical Characteristics

TABLE OF GRAPHS			FIGURE
η	Efficiency	vs Output Current	Figure 3, Figure 4, Figure 5, Figure 6
η	Efficiency	vs Input Voltage	Figure 7, Figure 8, Figure 9, Figure 10
V_{OUT}	Output voltage	vs Output curent	Figure 11, Figure 12, Figure 13, Figure 14
I_Q	Operating quiescent current	vs Input voltage	Figure 1
I_{SD}	Shutdown current	vs Input voltage	Figure 2
	Automatic Transition into 100% Mode		Figure 18, Figure 19, Figure 20
F_{SW}	Switching frequency	vs Output current	Figure 15, Figure 16, Figure 17
	Line and Load Transient Performance		Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, Figure 26, Figure 27, Figure 28, Figure 29, Figure 30
	AC load regulation performance		Figure 31, Figure 32
LOAD	LOAD Output Behavior		Figure 33, Figure 34, Figure 35
	Input Voltage Ramp up / down		Figure 36, Figure 37, Figure 38, Figure 39

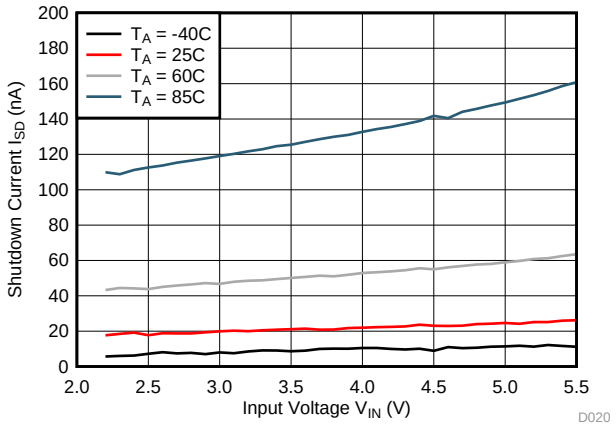
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Typical Characteristics (continued)



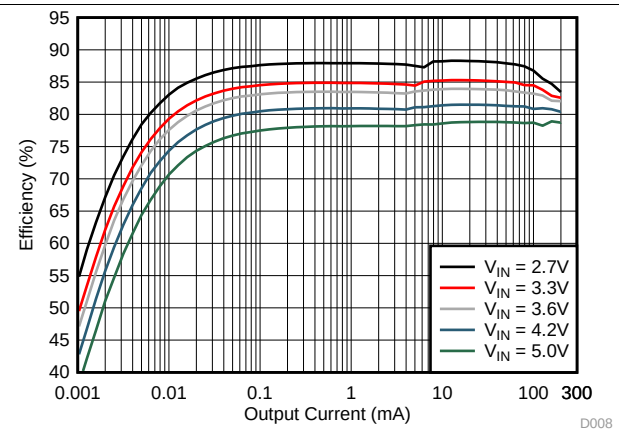
EN = VIN
CTRL = GND
Device not switching

Figure 1. TPS82740 Quiescent Current I_Q



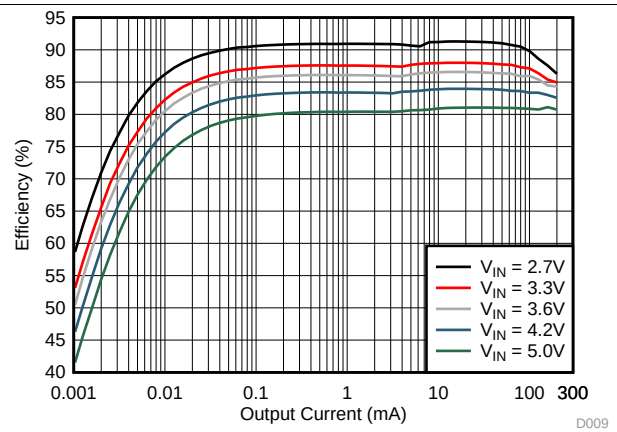
EN = GND

Figure 2. TPS82740 Shutdown current I_{SD}



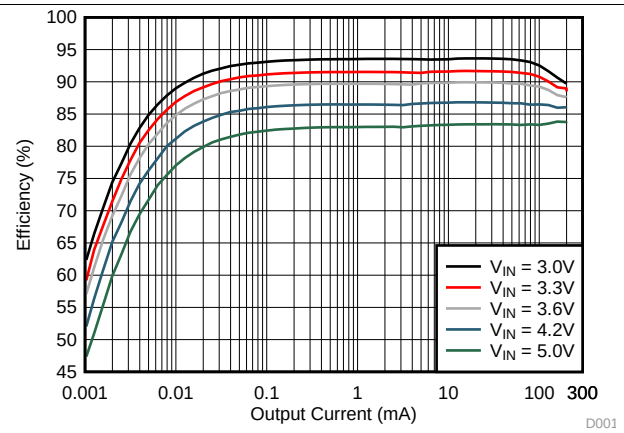
CTRL = GND

Figure 3. TPS82740A Efficiency V_{OUT} = 1.8V



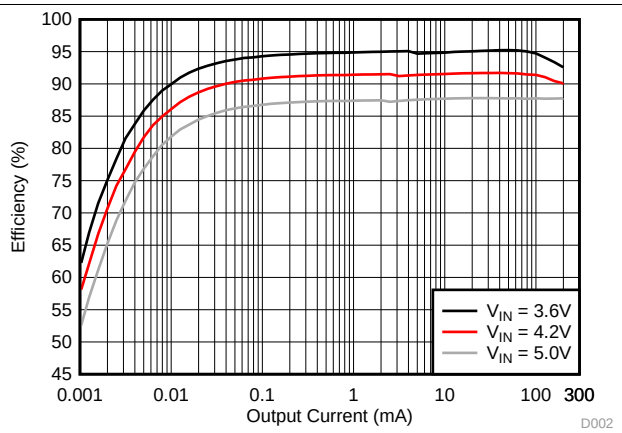
CTRL = GND

Figure 4. TPS82740A Efficiency V_{OUT} = 2.1V



CTRL = GND

Figure 5. TPS82740B Efficiency V_{OUT} = 2.6V

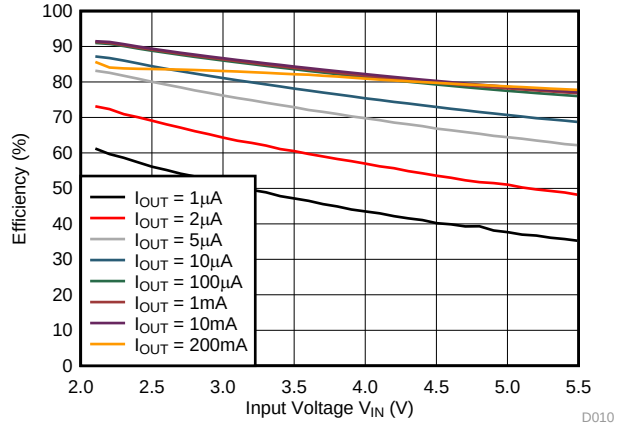


CTRL = GND

Figure 6. TPS82740B Efficiency V_{OUT} = 3.3V

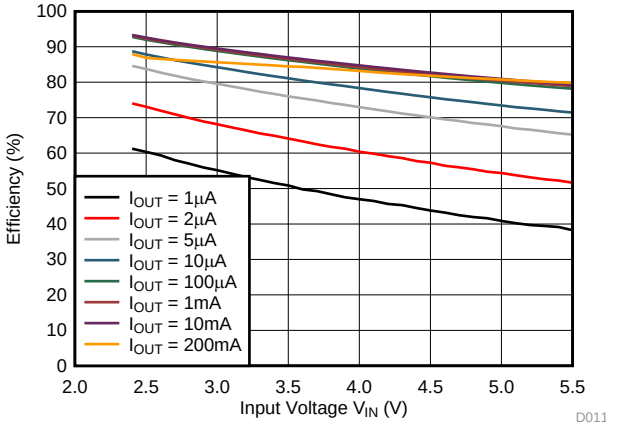
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Typical Characteristics (continued)



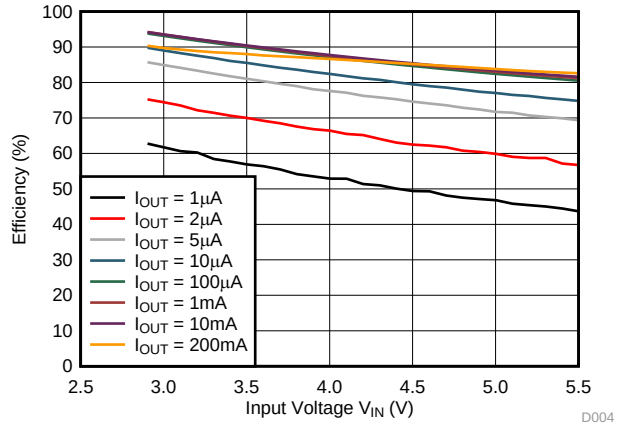
CTRL = GND

Figure 7. TPS82740A Efficiency V_{OUT} = 1.8V



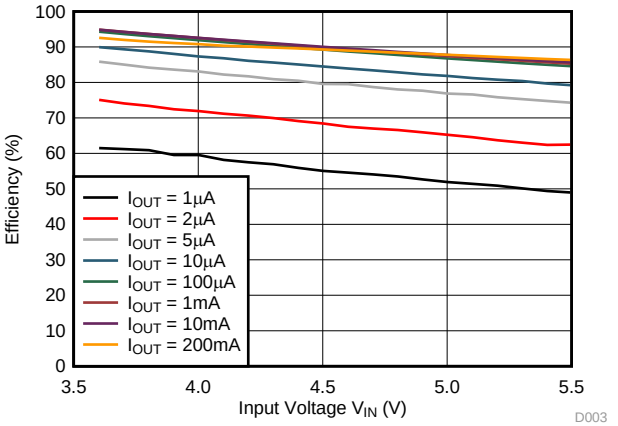
CTRL = GND

Figure 8. TPS82740A Efficiency V_{OUT} = 2.1V



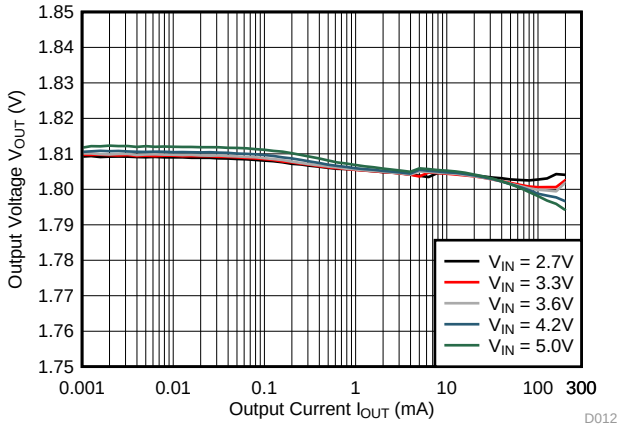
CTRL = GND

Figure 9. TPS82740B Efficiency V_{OUT} = 2.6V



CTRL = GND

Figure 10. TPS82740B Efficiency V_{OUT} = 3.3V



CTRL = GND

Figure 11. TPS82740A Output voltage V_{OUT} = 1.8V

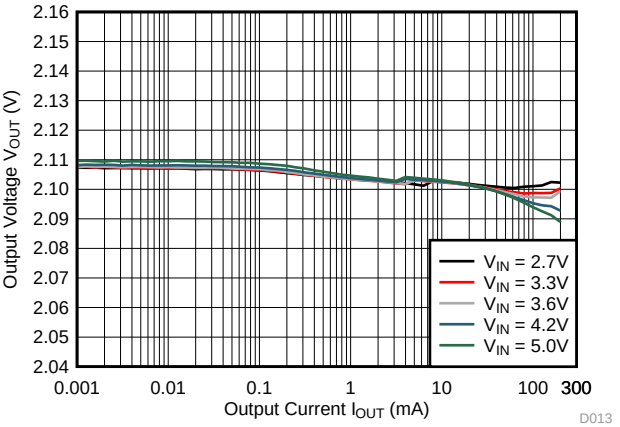
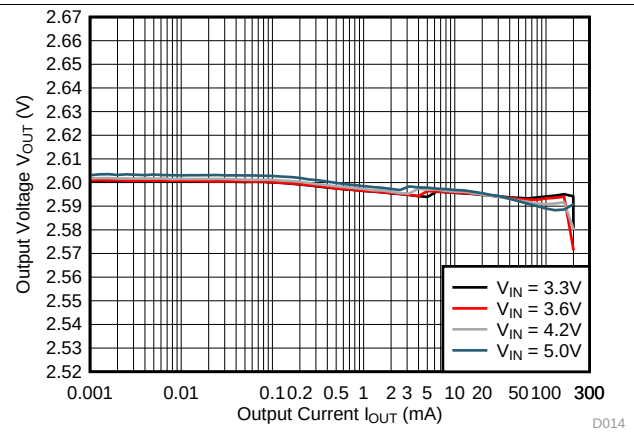


Figure 12. TPS82740A Output voltage V_{OUT} = 2.1V

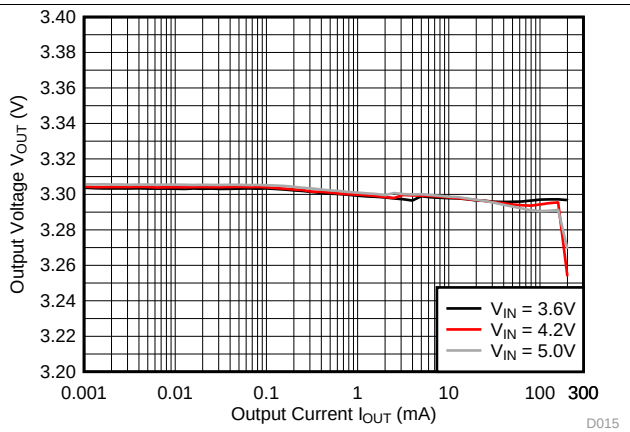
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Typical Characteristics (continued)



CTRL = GND

Figure 13. TPS82740B Output voltage V_{OUT} = 2.6V



CTRL = GND

Figure 14. TPS82740B Output voltage V_{OUT} = 3.3V

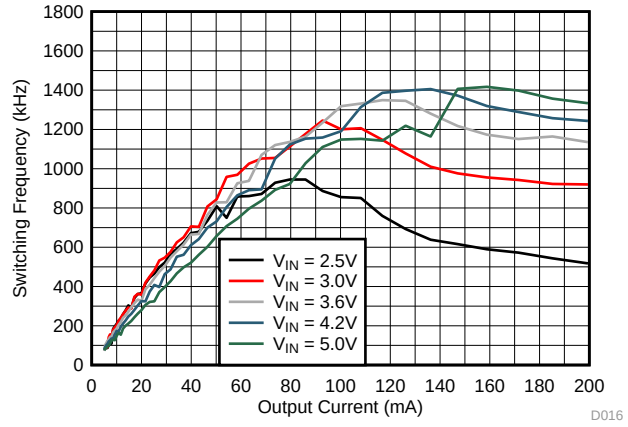


Figure 15. TPS82740A Switching frequency V_{OUT} = 1.8V

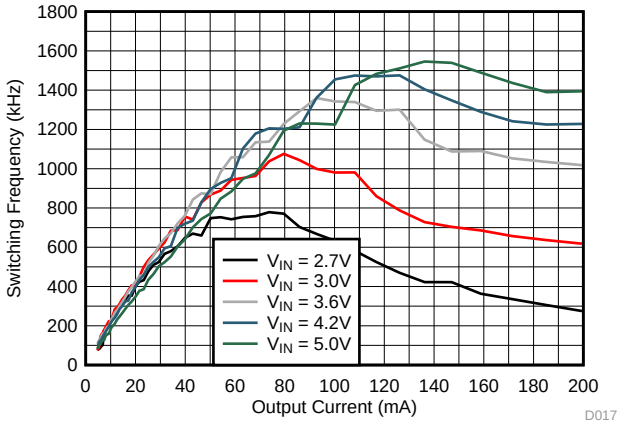


Figure 16. TPS82740A Switching frequency V_{OUT} = 2.1V

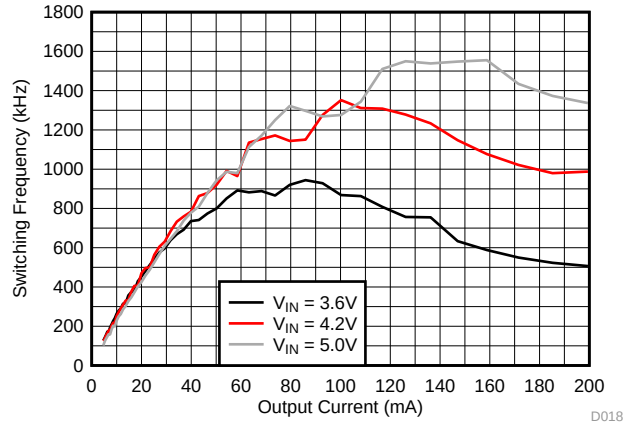


Figure 17. TPS82740B switching frequency V_{OUT} = 3.0V

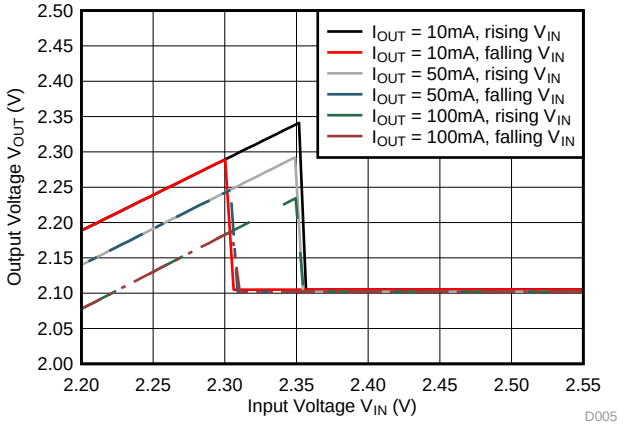


Figure 18. TPS82740A 100% Mode Transition V_{OUT} = 2.1V

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Typical Characteristics (continued)

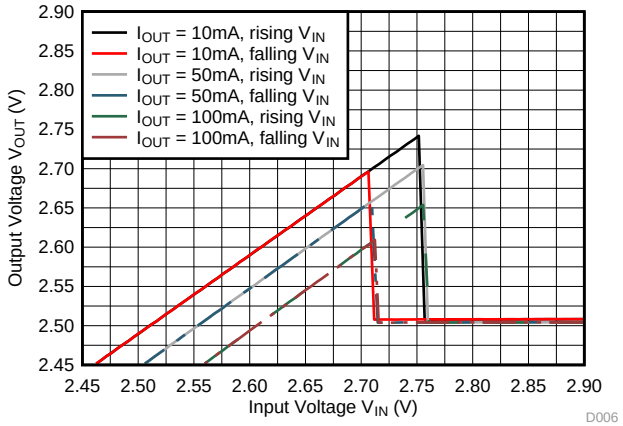


Figure 19. TPS82740A 100% Mode Transition V_{OUT} = 2.5V

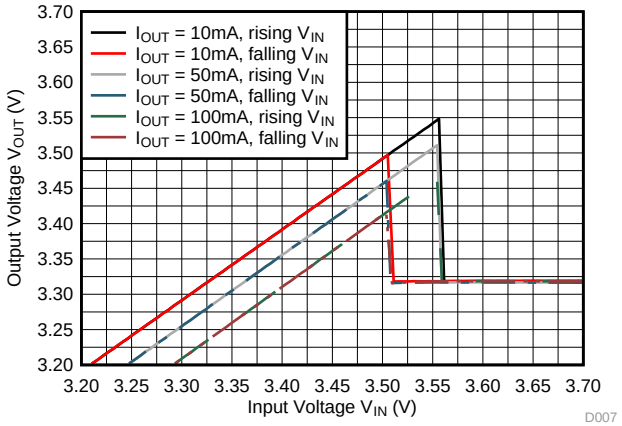


Figure 20. TPS82740B 100% Mode Transition V_{OUT} = 3.3V

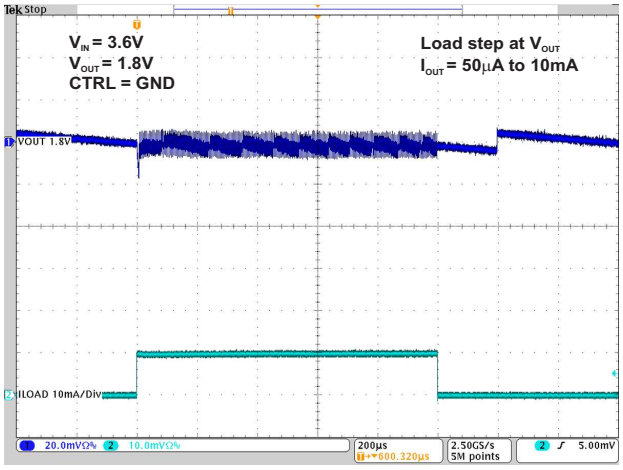


Figure 21. TPS82740A Load Transient Response V_{OUT} = 1.8V

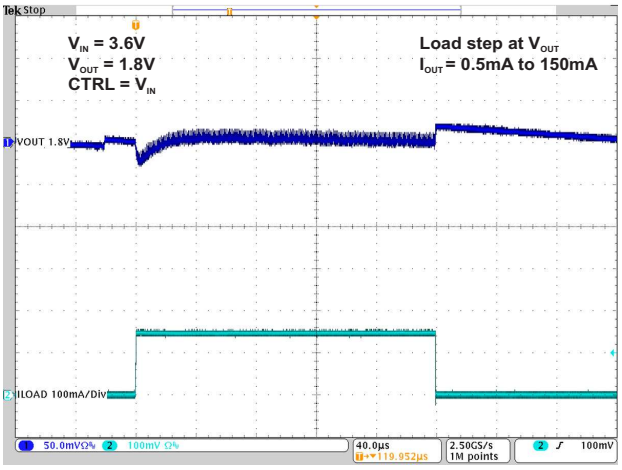


Figure 22. TPS82740A Load Transient Response V_{OUT} = 1.8V

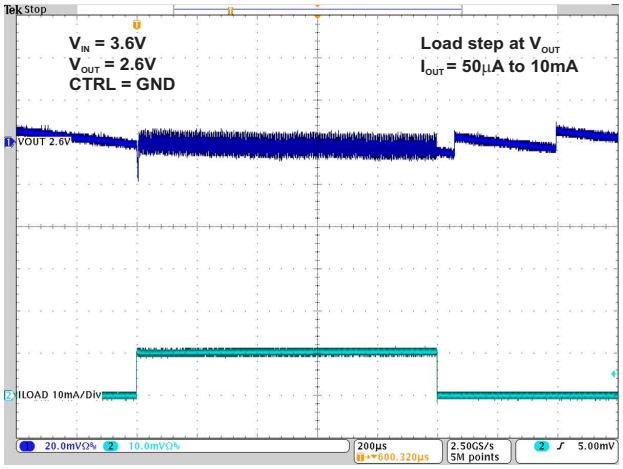


Figure 23. TPS82740B Load Transient Response V_{OUT} = 2.6V

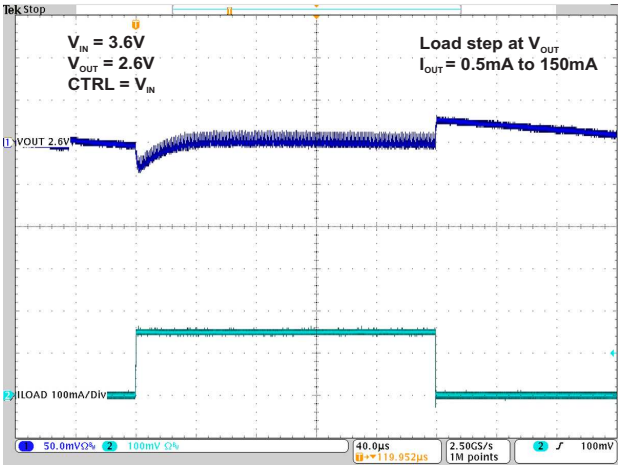


Figure 24. TPS82740B Load Transient Response V_{OUT} = 2.6V

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Typical Characteristics (continued)

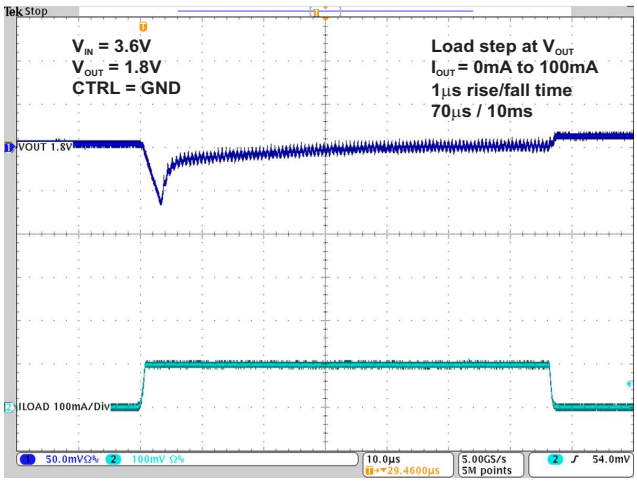


Figure 25. TPS82740A Load Transient Response V_{OUT} = 1.8V

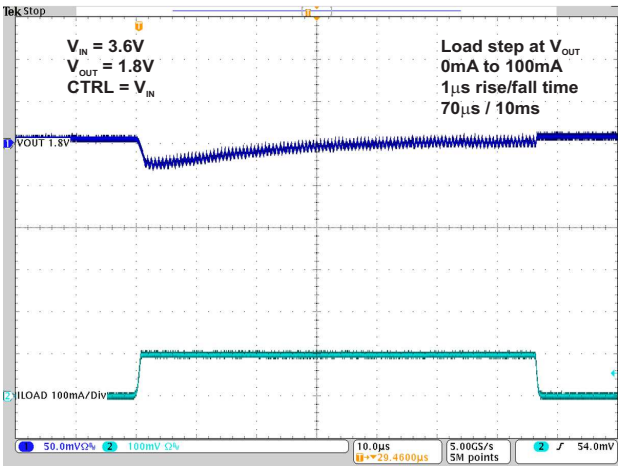


Figure 26. TPS82740A Load Transient Response V_{OUT} = 1.8V

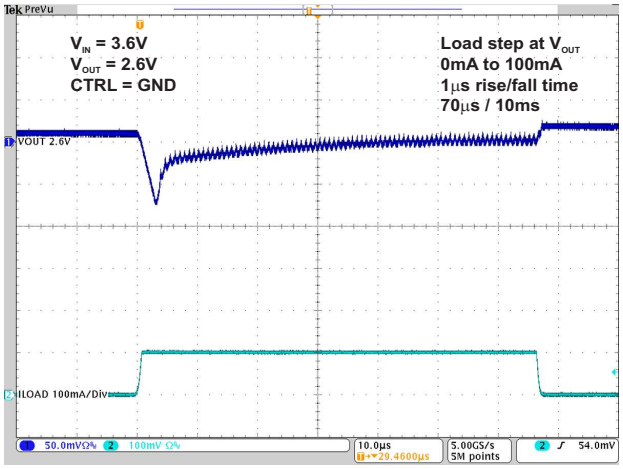


Figure 27. TPS82740B Load Transient Response V_{OUT} = 2.6V

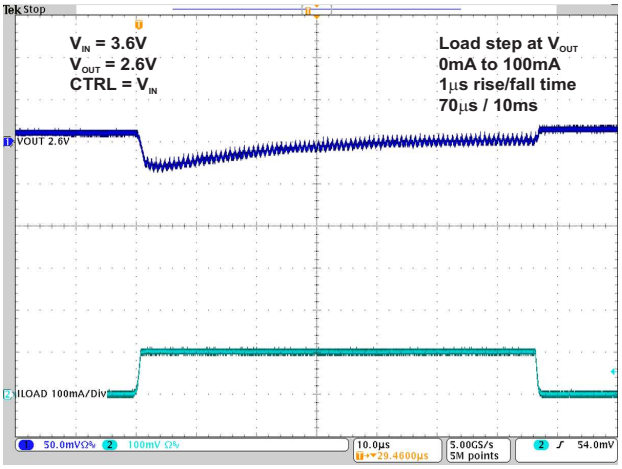


Figure 28. TPS82740B Load Transient response V_{OUT} = 2.6V

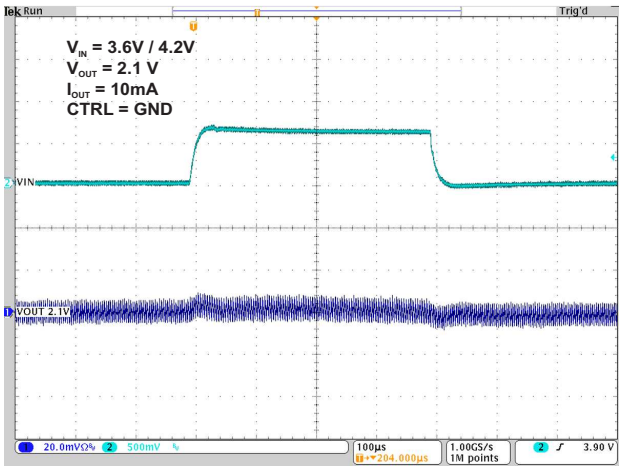


Figure 29. TPS82740A Line Transient Response I_{OUT} = 10mA

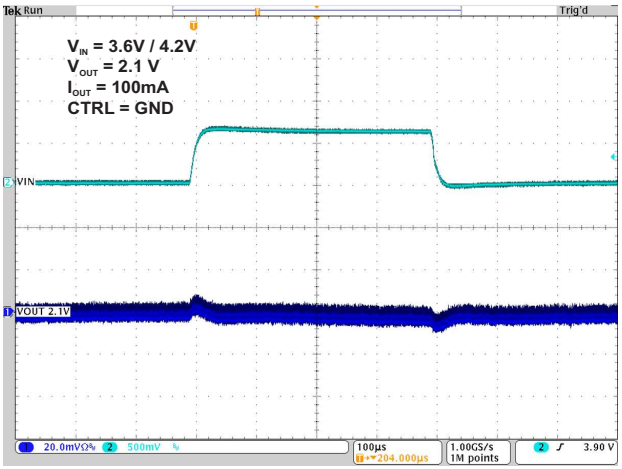


Figure 30. TPS82740A Line Transient Response I_{OUT} = 100mA

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Typical Characteristics (continued)

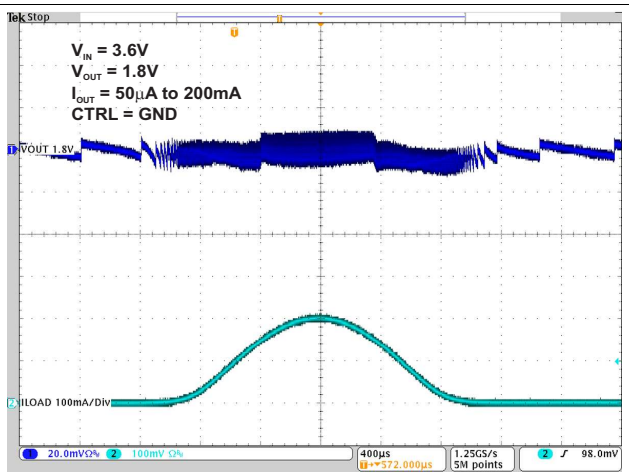


Figure 31. TPS82740A AC Load Sweep V_{OUT} = 1.8V

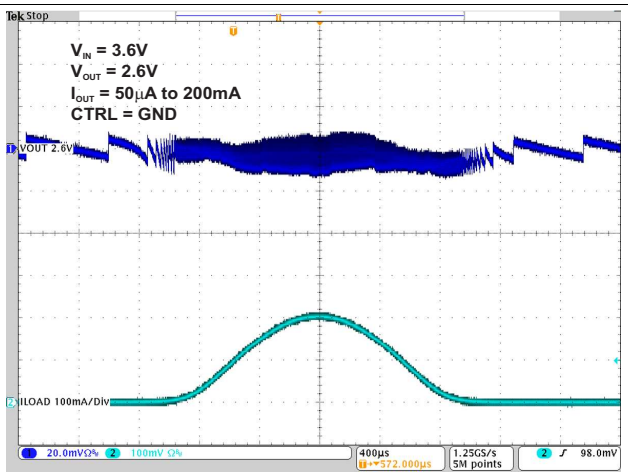


Figure 32. TPS82740B AC Load Sweep V_{OUT} = 2.6V

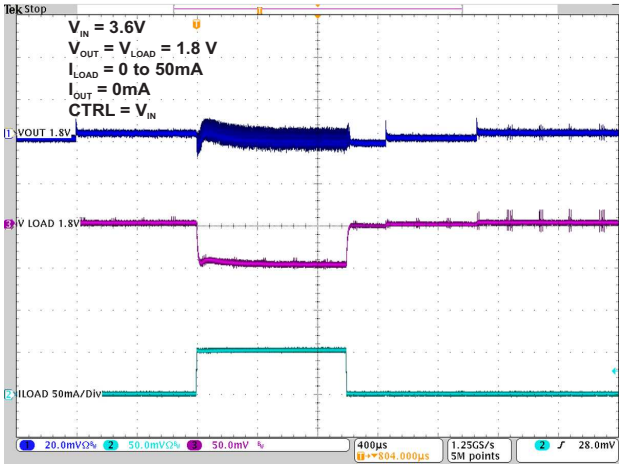


Figure 33. TPS82740A Load Step at LOAD Output

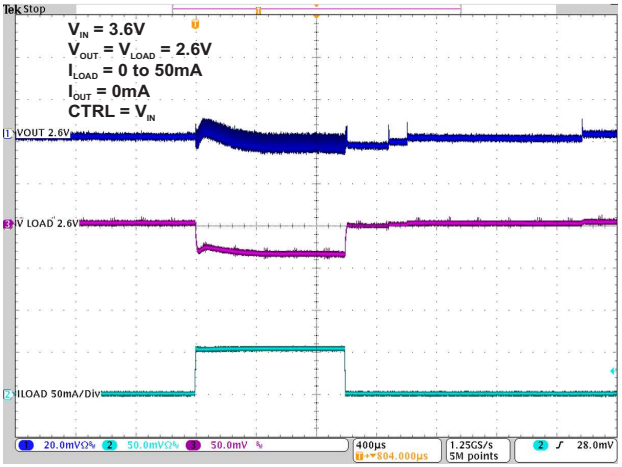


Figure 34. TPS82740B Load Step at LOAD Output

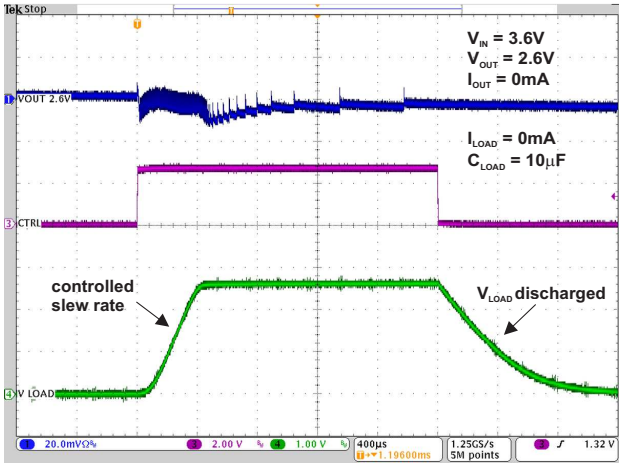


Figure 35. TPS82740B Load Output ON / OFF

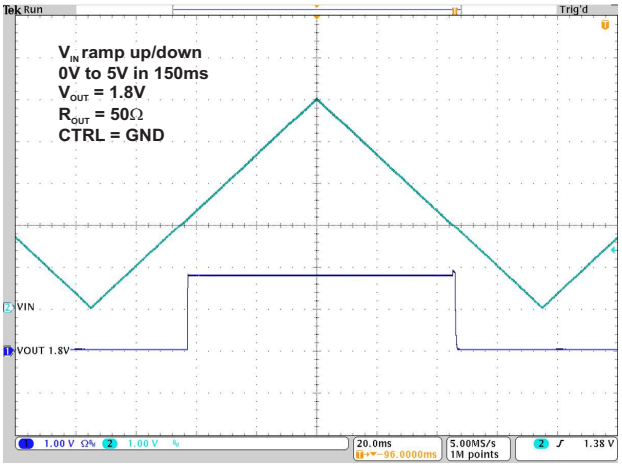


Figure 36. TPS82740A Input Voltage Ramp Up / Down

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Typical Characteristics (continued)

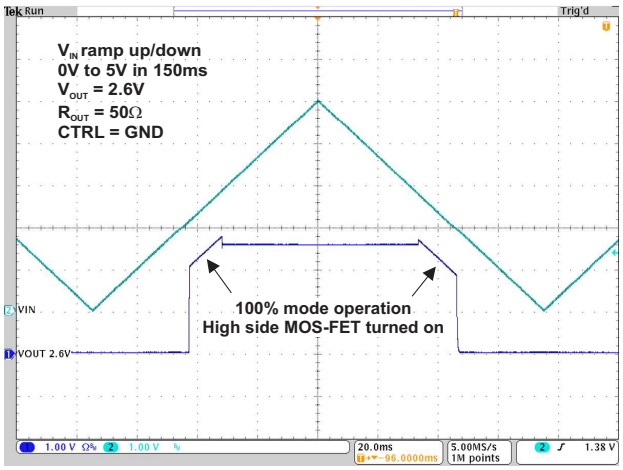


Figure 37. TPS82740B Input Voltage Ramp Up / Down

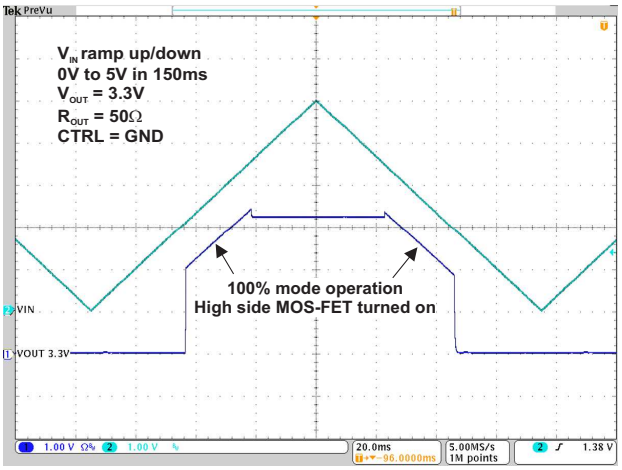


Figure 38. TPS82740B Input Voltage Ramp Up / Down

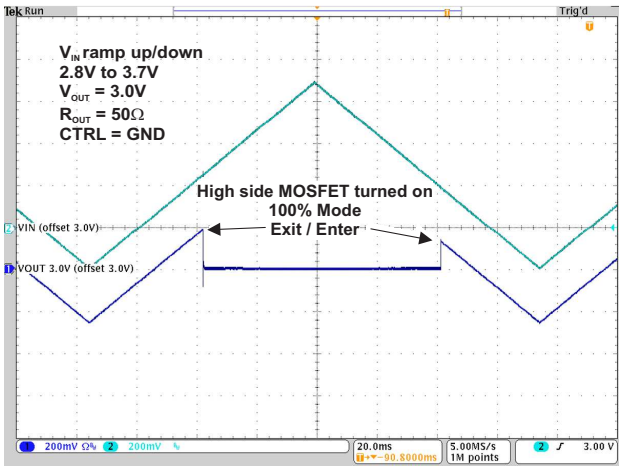
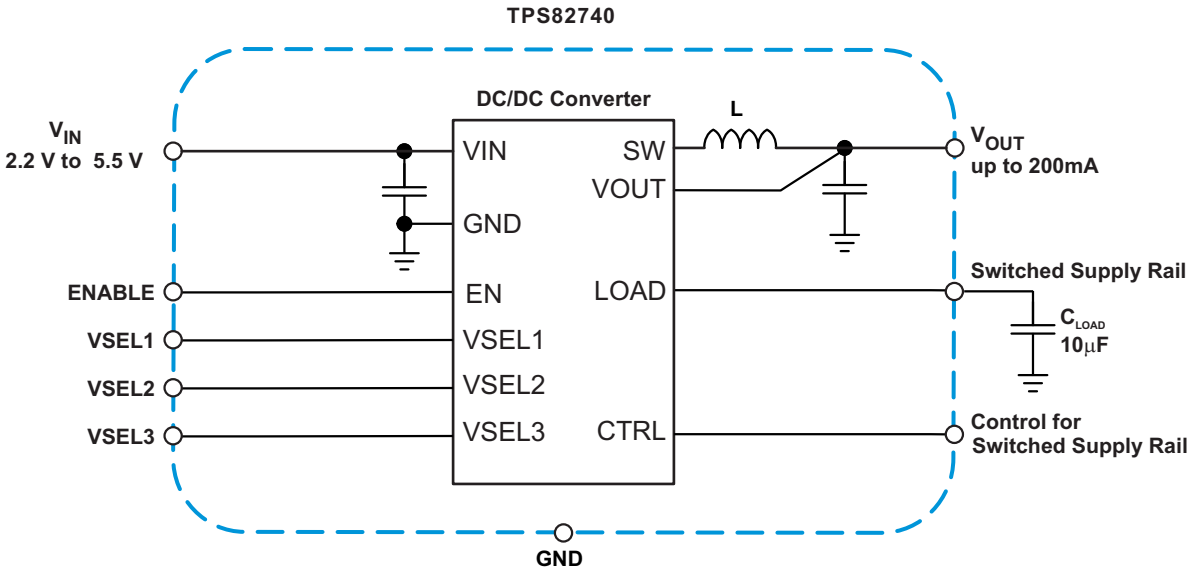


Figure 39. TPS82740B Enter / Exit 100% Mode Operation

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9 Parameter Measurement Information



Measurement Configuration with Passive Components

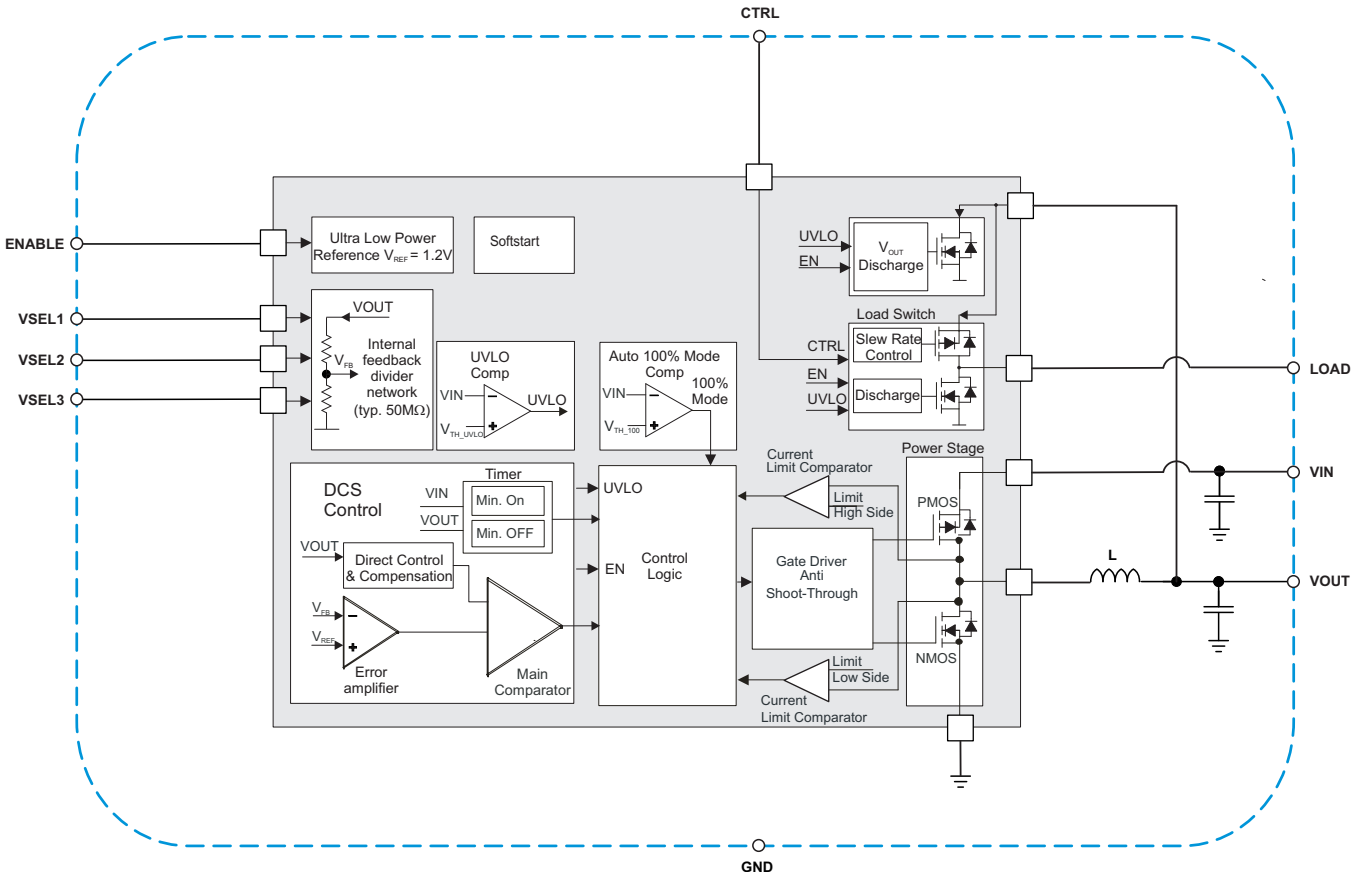
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10 Detailed Description

10.1 Overview

The TPS82740 is the first fully integrated step down converter module with an ultra low quiescent current consumption (360nA typ.) while maintaining a regulated output voltage and featuring TI's DCS-Control™ topology. The device extends high efficiency operation to output currents down to a few micro amperes.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 DCS-Control™

TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOUT pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and Power Save Mode at light loads. During PWM mode, it operates in continuous conduction. The switching frequency goes up to 1.7MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamlessly enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode, the switching frequency varies nearly linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. The TPS82740 offers both excellent DC

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Feature Description (continued)

voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits. At high load currents, the converter operates in quasi fixed frequency PWM mode operation and at light loads in PFM (Pulse Frequency Modulation) mode to maintain highest efficiency over the full load current range. In PFM Mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve the lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

During the sleep periods, the quiescent current of the TPS82740 is reduced to 360nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance (typ. 50MΩ) feedback divider network and an optimized DCS-Control™ block.

10.3.2 LOAD Switch

The LOAD pin can be used to power an additional, temporarily used sub-system. If the CTRL pin is set high, the LOAD pin is connected to the VOUT pin via an integrated load switch. The load switch is slew rate controlled to support soft switching and not impacting the regulated output VOUT. If the CTRL pin is set to low, the LOAD pin is disconnected from the VOUT pin and internally connected to GND by an internal discharge switch. The CTRL pin can be controlled by a micro controller and must be terminated. With CTRL pin high, the quiescent current is increased to improve the transient response.

10.3.3 Output Voltage Selection (VSEL1, VSEL2, VSEL3)

The TPS82740 provides an integrated, high impedance (typ. 50MΩ) feedback resistor divider network which is programmed by the pins VSEL1-3. The TPS82740A supports an output voltage range of 1.8V to 2.5V in 100mV steps, while the TPS82740B supports an output voltage range from 2.6V to 3.3V in 100mV steps. The output voltage can be changed during operation and supports a simple dynamic output voltage scaling, shown in Figure 44. The output voltage is programmed according to Table 2 and Table 3.

10.3.4 Output Discharge Function (VOUT and LOAD)

Both the VOUT pin and the LOAD pin feature a discharge circuit to connect each rail to GND, once they are disabled. This feature prevents residual charge voltages on capacitors connected to these pins, which may impact proper power up of the main- and sub-system. With the CTRL pin pulled low, the discharge circuit at the LOAD pin activates. With the EN pin pulled low, the discharge circuit at the pin VOUT activates.

10.3.5 Internal Current Limit

The TPS82740 integrates a current limit in the high side, as well as in the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the current decreases below the low side MOSFET current limit.

Table 4. Load Pin Condition Table

Pin condition			Operating condition	Remark
LOAD	**EN**	**CTRL**	**VIN**	
Connected to VOUT	high	high	> V_{UVLO}	load switch enabled and slew rate controlled
Connected to GND	high	low	> V_{UVLO}	load switch turned off
	low	high or low	> V_{UVLO}	device and load switch disabled
	high	high	< V_{UVLO}	device disabled due to UVLO

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10.3.6 CTRL / DVS (Dynamic Voltage Scaling TPS62741)

In TPS62741, the CTRL pin controls beside the load switch as well Dynamic Voltage Scaling. The CTRL pin selects between two different voltage setting banks. The voltage of each bank are set with the VSEL pins 1-4 according to .

The output LOAD is controlled with the CTRL pin. The pin is internally connected either to VOUT pin or GND and can be used to power up/down temporarily used external circuits to reduce leakage current consumption of the system.

10.4 Device Functional Modes

10.4.1 Enable / Shutdown

The TPS82740 is activated when the EN pin is set high. For proper operation, the pin must be terminated and must not be left floating. With the EN pin set low, the device enters shutdown mode with less than typ. 70nA current consumption.

10.4.2 Softstart

When the device is enabled, the internal reference is powered up and after the startup delay time $t_{Startup_delay}$ has expired, the device enters softstart, starts switching and ramps up the output voltage. During softstart, the device operates with a reduced current limit, $I_{LIM_softstart}$, of typ. 1/3 of the nominal current limit. This reduced current limit is active during the time $t_{Softstart}$. The current limit is increased to its nominal value, I_{LIMF}, once this time has expired or the nominal output voltage is reached.

10.4.3 POWER GOOD OUTPUT (PG)

The Power Good comparator features an open drain output. The PG comparator is active with EN pin set to high and V_{IN} is above the threshold V_{TH_UVLO+}. It is driven to high impedance once V_{OUT} trips the threshold V_{TH_PG+} for rising V_{OUT}. The output is pulled to low level once V_{OUT} falls below the PG hysteresis, V_{PG_hys}. The output is also pulled to low level in case the input voltage V_{IN} falls below the undervoltage lockout threshold V_{TH_UVLO-} or the device is disabled with EN = low. The power good output (PG) can be used as an indicator for the system to signal that the converter has started up and the output voltage is in regulation.

Table 5. PG condition table

Pin condition			Operating condition			Remark
PG	EN	CTRL	IOUT / ILOAD	VIN	VOUT	
hiz	high	high	don't care	> V_{UVLO}	VOUT > V_{TH_PG+}	PG comparator active, pull up resistor pulls PG to high
hiz	high	low	medium load (> 1mA)	> V_{UVLO}	VOUT > V_{TH_PG+}	PG comparator active, pull up resistor pulls PG to high
hiz	high	low	light load (< 1mA)	> V_{UVLO}	VOUT > V_{TH_PG+}	PG comparator disabled for low Iq operation, pull up resistor pulls PG to high
low	high	don't care	0mA < IOUT < 100mA	> V_{UVLO}	VOUT < V_{TH_PG-}	startup, overload or ramp down
low	low	don't care	output disabled	V_{IN} > 1.2V	VOUT = 0	device disabled
low	high	don't care	output disabled	< V_{UVLO}	VOUT not present	device disabled, due to UVLO

Table 6. VOUT Output Discharge Condition Table

VOUT pin	EN	VIN condition	remark
connected to GND, output discharged	low	1.5V < V_{IN} < V_{UVLO}	
connected to GND, output discharged	high	< V_{UVLO}	

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Table 6. VOUT Output Discharge Condition Table (continued)

VOUT pin	EN	VIN condition	remark
hiz, discharge switch disabled	high	> V_{UVLO}	during regulator start up, the discharge switch is enabled and VOUT pulled to low, until the regulator start up time t_{Start} expires. During the softstart time and later, the discharge switch is disabled.

10.4.4 Automatic Transition into 100% Mode

Once the input voltage comes close to the output voltage, the TPS82740 stops switching and enters 100% duty cycle operation. It connects the output VOUT via the inductor and the internal high side MOSFET switch to the input VIN, once the input voltage V_{IN} falls below the 100% mode enter threshold, V_{TH_100-} . In 100% mode switching stops eliminating output voltage ripple. Because the output is connected to the input, the output voltage tracks the input voltage minus the voltage drop across the internal high side switch and the inductor caused by the output current. Once the input voltage increases and trips the 100% mode exit threshold, V_{TH_100+} , the TPS82740 turns on and starts switching again. See Figure 40, Figure 18, Figure 19 and Figure 20.

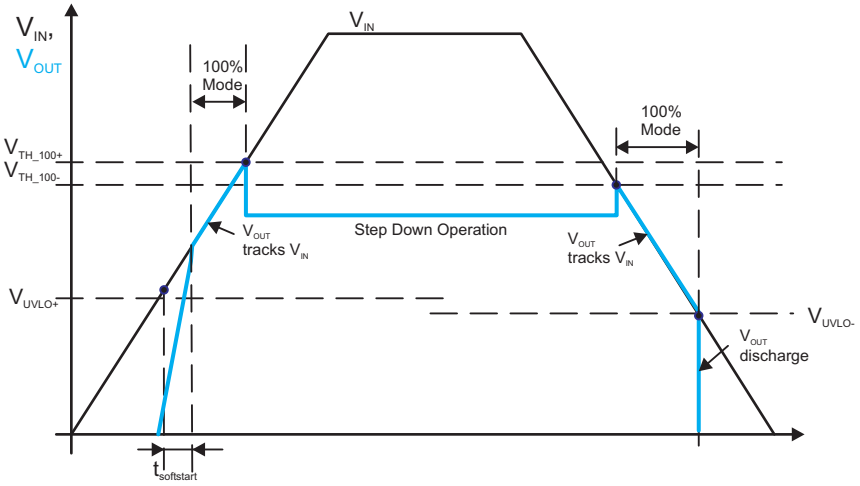


Figure 40. Automatic Transition into 100% Mode

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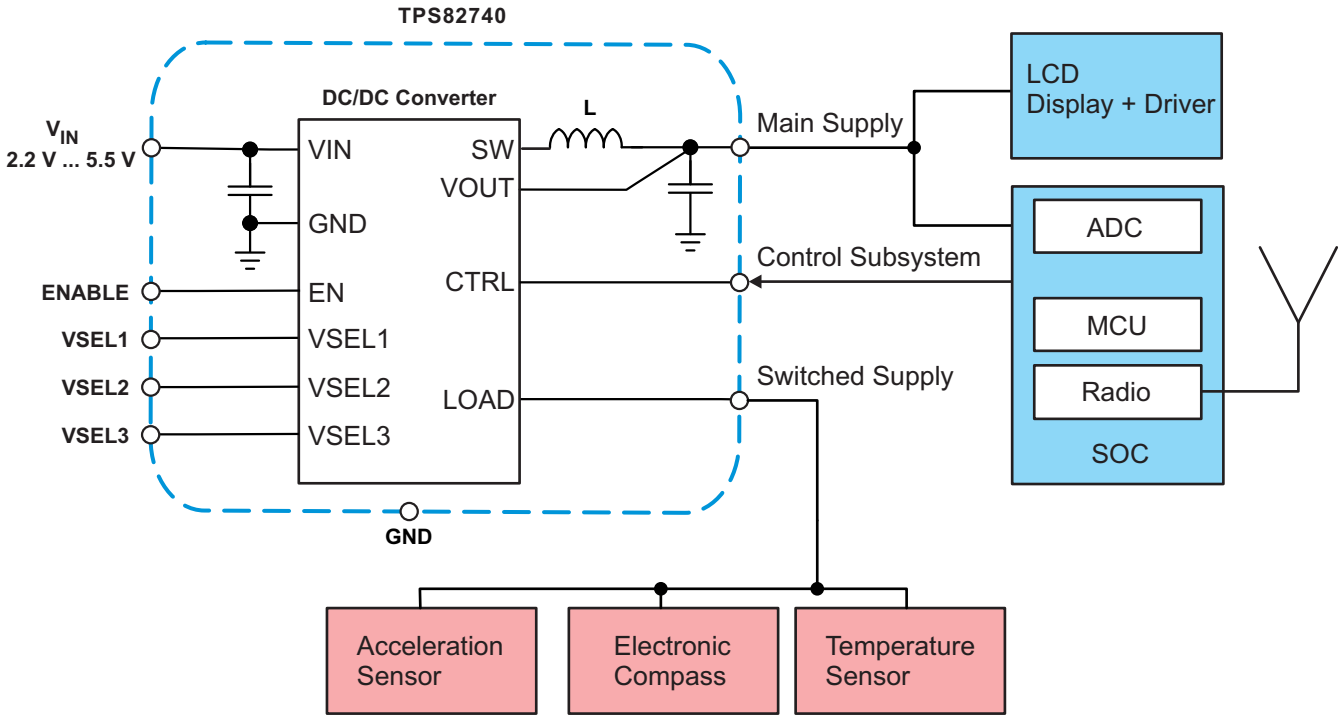
11 Application and Implementation

11.1 Application Information

The device is designed to operate from an input voltage supply range between 2.2V and 5.5V with a maximum output current of 200mA. Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. The integrated slew rate controlled load switch can distribute the selected output voltage to a temporarily used sub-system. The TPS82740 module operates in PWM mode for medium and high load conditions and in power save mode at light load currents.

At high load currents, the converter operates in quasi fixed frequency PWM mode operation. The switching frequency is up to 1.7MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamlessly enters Power Save Mode by varying the switching frequency linearly to maintain high efficiency over the full load current range. At very light load conditions the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve 360nA quiescent current consumption.

11.2 Typical Application



Example of Implementation in a SOC Based System

11.2.1 Design Requirements

TPS82740 is a complete step-down converter module including all passive components (inductor, input and output capacitor). For most applications no additional input / output capacitors are required. Use the following typical application design procedure to select additional external components in case further performance improvement of the module is desired.

11.2.2 Detailed Design Procedure

11.2.2.1 Input Capacitor Selection

For most applications, the integrated input capacitor at the VIN pin is sufficient.

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Typical Application (continued)

TPS82740 uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as that from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the module. In this circumstance, additional ceramic 'bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the module and the power source lead to reduce ringing that occurs between the inductance of the power source leads and the module.

11.2.2.1.1 Input Buffer Capacitor Selection

In addition to the small ceramic input capacitor a larger buffer capacitor C_{Buf} is recommended to reduce voltage drops and ripple voltage. When using battery chemistries like Li-SOCl2, Li-SO2, Li-MnO2, the impedance of the battery has to be considered. These battery types tend to increase their impedance depending on discharge status and often can support output currents of only a few mA. Therefore a buffer capacitor is recommended to stabilize the battery voltage during DC/DC operations e.g. for a RF transmission. A voltage drop on the input of the TPS82740 during DC/DC operation impacts the advantage of the step down conversion for system power reduction. Furthermore the voltage drops can fall below the minimum recommended operating voltage of the device and leads to an early system cut off. Both effects reduce the battery life time. To achieve best performance and to extract the most energy out of the battery a good procedure is to select the buffer capacitor value for an voltage drop below 50mVpp during DC/DC operation. The capacitor value strongly depends on the used battery type, as well the current consumption during a RF transmission as well the duration of the transmission.

11.2.2.2 Output Capacitor Selection

For most applications, the integrated output capacitor at the VOUT pin is sufficient.

In order to further reduce the output voltage ripple and improve the load transient performance an additional external output capacitance may be used. For most applications an additional 4.7µF or 10µF capacitor will be sufficient. Care should be taken that the total effective capacitance present at the output does not exceed 10µF in order to guarantee loop stability. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended.

At the LOAD output pin, no additional output capacitor is required. For applications demanding external capacitance connected to the LOAD pin, the total capacitance should not exceed 10µF.

11.2.3 Application Curves

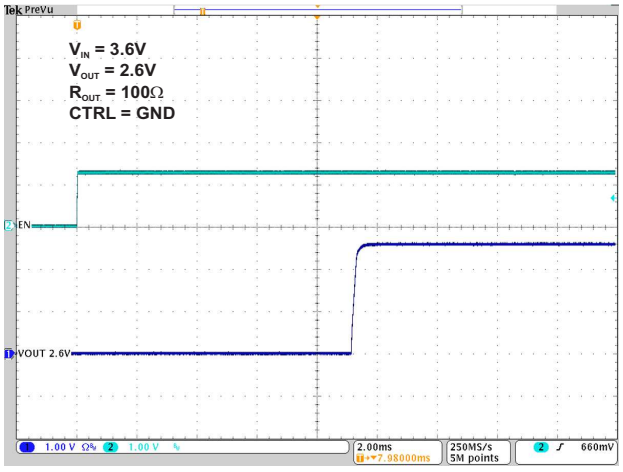


Figure 41. TPS82740B Device Enable and Start up

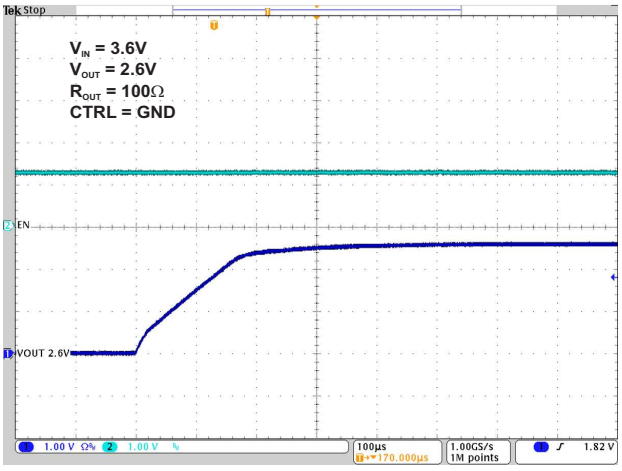


Figure 42. TPS82740B V_{OUT} Ramp after Enable

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Typical Application (continued)

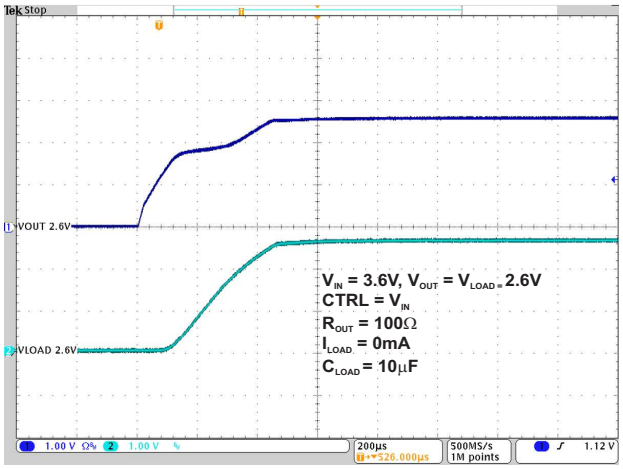


Figure 43. TPS82740B V_{OUT} Ramp with activated LOAD Switch

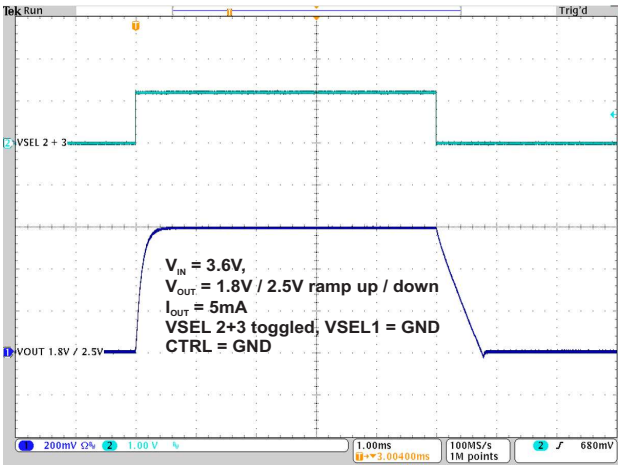


Figure 44. TPS82740A Dynamic Output Voltage Scaling: V_{OUT} = 1.8V / 2.5V

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12 Power Supply Recommendations

The TPS82740 device is a complete and optimized power supply module working within the given specification range without additional components. Please use the information given in the Application Information section to connect the input and output circuitry appropriately.

13 Layout

13.1 Layout Guidelines

In making the pad size for the uSiP LGA balls, it is recommended that the layout use a non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 45 shows the appropriate diameters for a MicroSiP™ layout. Figure 46 shows a suggestion for the PCB layout.

13.2 Layout Example

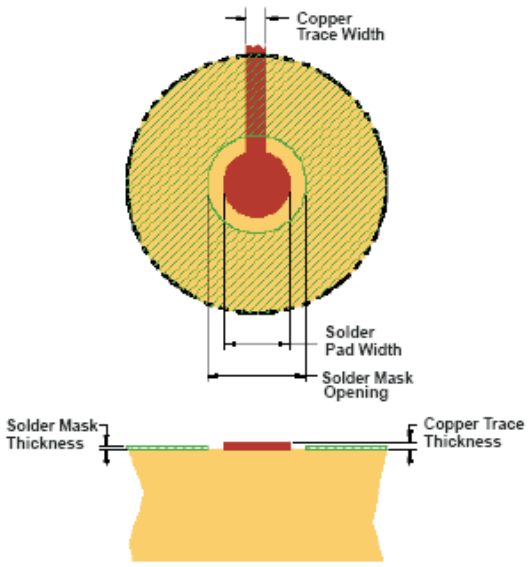


Figure 45. Recommended Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PWB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and affect reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

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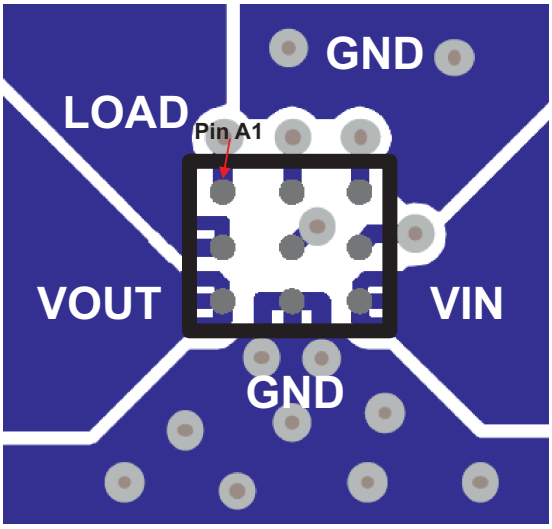


Figure 46. PCB Layout Suggestion

13.3 Surface Mount Information

The TPS82740 MicroSIP™ module uses an open frame construction for a fully automated assembly process and provides a large surface area for pick and place operations. See the "Pick Area" in the package drawing.

Package height and weight have been kept to a minimum, allowing MicroSIP™ device handling similar to a 0805 footprint component.

For reflow recommendations, see document J-STD-20 from the JEDEC/IPC standard.

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14 器件和文档支持

14.1 文档支持

14.1.1 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 7. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS82740A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS82740B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

14.2 商标

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14.3 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

15 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82740ASIPR	ACTIVE	uSiP	SIP	9	3000	Green (RoHS & no Sb/Br)	NIAU	Level-2-260C-1 YEAR	-40 to 85	E7 TXI7400EC	Samples
TPS82740ASIPT	ACTIVE	uSiP	SIP	9	250	Green (RoHS & no Sb/Br)	NIAU	Level-2-260C-1 YEAR	-40 to 85	E7 TXI7400EC	Samples
TPS82740BSIPR	ACTIVE	uSiP	SIP	9	3000	Green (RoHS & no Sb/Br)	NiAu	Level-2-260C-1 YEAR	-40 to 85	E8 TXI2740EC	Samples
TPS82740BSIPT	ACTIVE	uSiP	SIP	9	250	Green (RoHS & no Sb/Br)	NiAu	Level-2-260C-1 YEAR	-40 to 85	E8 TXI2740EC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

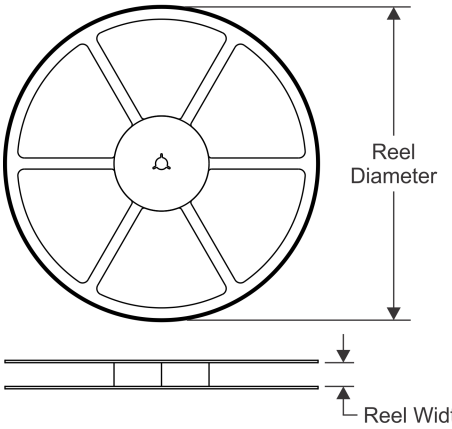
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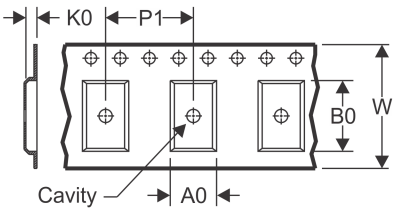
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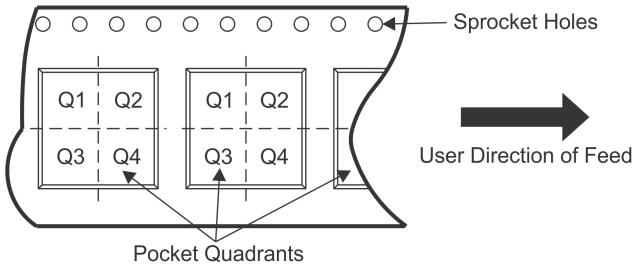


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

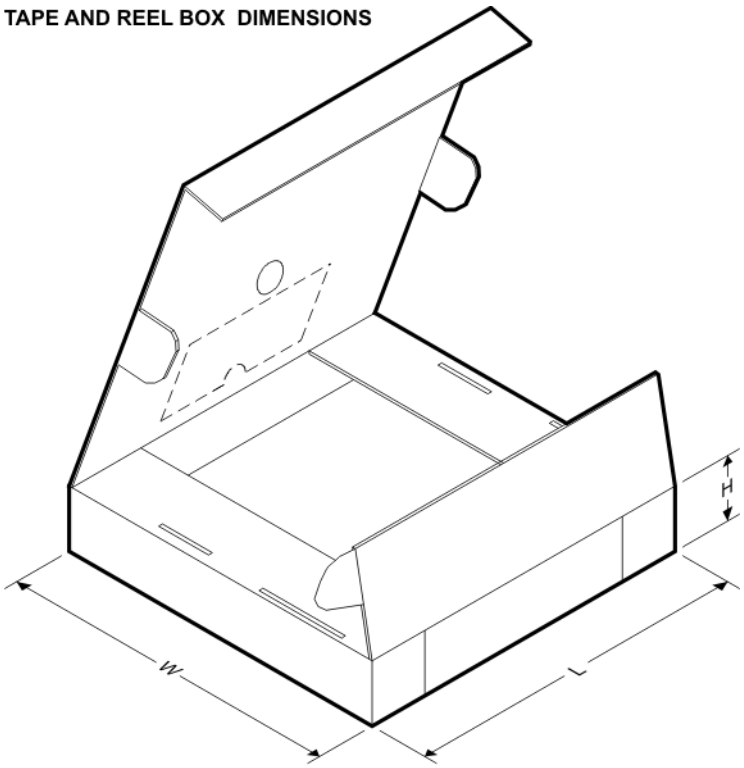
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82740ASIPR	uSiP	SIP	9	3000	180.0	8.4	0.95	1.58	0.27	2.0	8.0	Q2
TPS82740ASIPT	uSiP	SIP	9	250	180.0	8.4	0.95	1.58	0.27	2.0	8.0	Q2
TPS82740BSIPR	uSiP	SIP	9	3000	180.0	8.4	0.95	1.58	0.27	2.0	8.0	Q2
TPS82740BSIPT	uSiP	SIP	9	250	180.0	8.4	0.95	1.58	0.27	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82740ASIPR	uSiP	SIP	9	3000	210.0	185.0	35.0
TPS82740ASIPT	uSiP	SIP	9	250	182.0	182.0	20.0
TPS82740BSIPR	uSiP	SIP	9	3000	210.0	185.0	35.0
TPS82740BSIPT	uSiP	SIP	9	250	182.0	182.0	20.0

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