具有超低 I_Q 的 LM5165-Q1 3V 至 65V 输入、150mA 同步降压转换器

1 特性

- 符合 AEC-Q100 的汽车标准 应用
  - 器件温度 1 级：-40°C 至 125°C 的环境温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C5
- 3V 至 65V 宽输入电压范围
- 10.5µA 空载静态电流
- –40°C 至 150°C 结温范围
- 固定（3.3V、5V）或可调节输出电压
- 符合 EN55022/CISPR 22 EMI 标准
- 集成 2Ω P 型金属氧化物半导体 (PMOS) 降压开关
  - 支持 100% 占空比，可实现低压降
- 集成 1Ω N 型金属氧化物半导体 (NMOS) 同步整流器
  - 无需使用外部整流二极管
- 可编程的电流限制设定值（4 级）
- 可选 PFM 或 COT 模式工作
- 1.223V ±1% 内部电压基准
- 900µs 内部或可编程软启动
- 用于实现较低 EMI 的有效转换率控制
- 单调启动至预偏置输出
- 无环路补偿或自举升压组件
- 具有迟滞功能的精密使能和输入 UVLO
- 具有迟滞功能的热关断保护
- 10 引脚 VSON 和 VSSOP 封装
- 使用 WEBENCH® 电源设计器创建定制稳压器设计

2 应用

- 汽车和电池供电设备
- 高电压 LDO 替代产品
- 通用偏置电源

3 说明

LM5165-Q1 器件是一款易于使用的紧凑型 3V 至 65V、超低 I_Q 同步降压转换器，可在宽输入电压和负载电流范围内提供高效率。该器件具有集成式高侧和低侧功率 MOSFET，能够以 3.3V 或 5V 的固定输出电压或可调输出电压提供高达 150mA 的输出电流。该转换器设计旨在简化实现方案，同时优化目标应用的性能。脉频调制 (PFM) 模式可确保在轻负载条件下获得最优效率，恒定导通时间 (COT) 控制可实现近似恒定的工作频率。这两种控制方案都不需要环路补偿，同时还能够针对较高的降压转换比实现出色的线路和负载瞬态响应以及短暂的脉宽调制 (PWM) 导通时间。

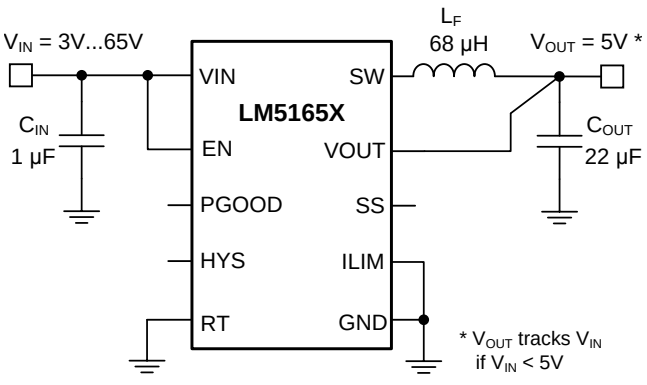
高侧 P 沟道 MOSFET 能够以 100% 占空比工作以确保最低压差电压，而且不需要使用自举电容器进行栅极驱动。另外，还可以调节电流限制设定值来优化电感器选择，从而满足特定的输出电流要求。可选和可调节启动时序选项包括最短延迟（无软启动）、内部固定值 (900µs) 以及可使用电容器进行外部编程的软启动。可以使用开漏 PGOOD 指示器进行定序、故障报告和输出电压监视。LM5165-Q1 符合汽车 AEC-Q100 1 级标准，并且采用引脚间距为 0.5mm 的 10 引脚 VSON 和 VSSOP 封装。

器件信息(1)

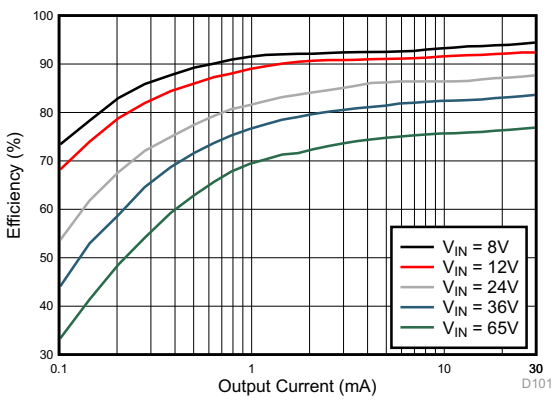
器件型号	输出	封装
LM5165-Q1	可调节	VSON (10) VSSOP (10)
LM5165X-Q1	5V 固定	
LM5165Y-Q1	3.3V 固定	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型原理图（固定电压）



典型效率 (V_{OUT} = 5V)



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 6
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 7
6.7 Typical Characteristics ... 8
7 **Detailed Description** ... 13
7.1 Overview ... 13
7.2 Functional Block Diagram ... 13
7.3 Feature Description ... 14
7.4 Device Functional Modes ... 20
8 **Applications and Implementation** ... 21
8.1 Application Information ... 21
8.2 Typical Applications ... 21
9 **Power Supply Recommendations** ... 35
10 **Layout** ... 35
10.1 Layout Guidelines ... 35
10.2 Layout Example ... 37
11 器件和文档支持 ... 38
11.1 器件支持 ... 38
11.2 文档支持 ... 38
11.3 相关链接 ... 39
11.4 接收文档更新通知 ... 39
11.5 社区资源 ... 39
11.6 商标 ... 39
11.7 静电放电警告 ... 39
11.8 Glossary ... 39
12 机械、封装和可订购信息 ... 39

4 修订历史记录

Changes from Revision A (March 2016) to Revision B **Page**

- Added VSSOP-10 package information ... 3
- Changed EN absolute maximum voltage from (VIN + 0.3 V) to 68 V ... 5
- Deleted note 5 under *Absolute Maximum Ratings* table ... 5
- Changed EN operating voltage from VIN to 65 V ... 6
- Deleted note 2 under *Recommended Operating Conditions* table ... 6
- Added thermal information data for VSSOP-10 package ... 6
- Added ILIM specifications for VSSOP-10 package ... 6
- Changed RT resistor equation divisor from 1.6 to 1.75 and updated Table 1 accordingly ... 16
- Added link to TI Design TIDA-00666 ... 21
- 已添加 在*器件和文档支持* 部分中添加了更多信息 ... 38

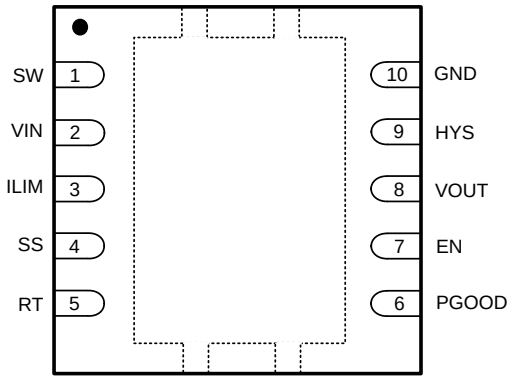
Changes from Original (February 2016) to Revision A **Page**

- 产品预览至量产数据发布 ... 1

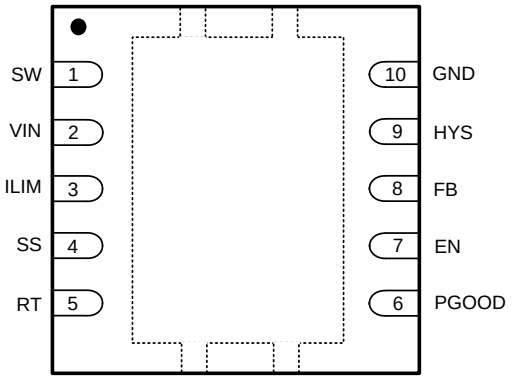
Copyright © 2016–2017, Texas Instruments Incorporated

5 Pin Configuration and Functions

DRC Package
10-Pin VSON With Exposed Thermal Pad
Top View

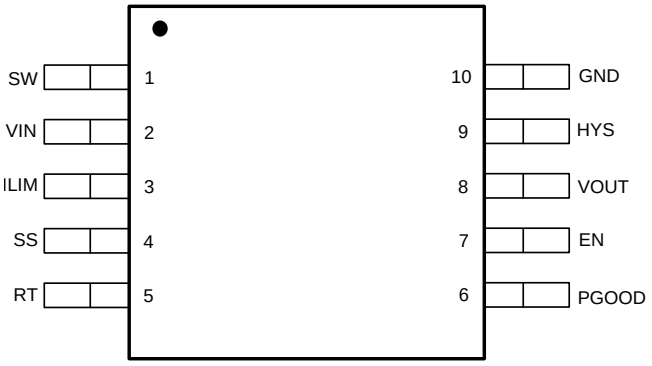


LM5165X, LM5165Y
Fixed Output Versions

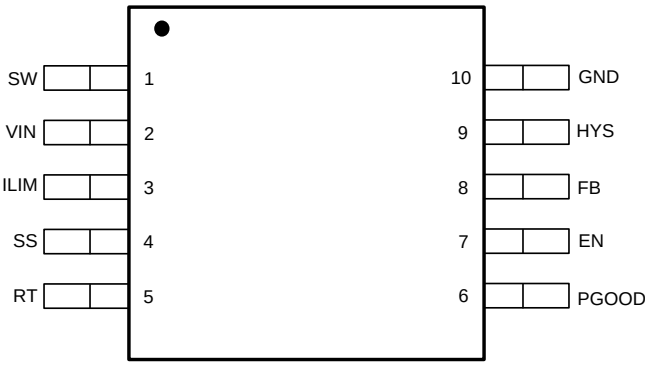


LM5165
Adjustable Output Version

DGS Package
10-Pin VSSOP
Top View



LM5165X, LM5165Y
Fixed Output Versions



LM5165
Adjustable Output Version

Copyright © 2016–2017, Texas Instruments Incorporated

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	P	Switching node that is internally connected to the drain of the high-side PMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching side of the power inductor.
2	VIN	P	Regulator supply input pin to high-side power MOSFET and internal bias rail LDO. Connect to input supply and input capacitor C_{IN}. Path from VIN to the input capacitor must be as short as possible.
3	ILIM	I	Programming pin for current limit. Connecting the appropriate resistor from ILIM to GND selects one of four preset current limit options. Short ILIM to GND for the maximum current setting.
4	SS	I	Programming pin for the soft-start time. If a 100-kΩ resistor is connected from SS to GND, the internal soft-start circuit is disabled and the FB comparator reference steps immediately from zero to full value when the regulator is enabled by the EN input. If the SS pin is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 900 µs. If an appropriate capacitance is connected to the SS pin, the soft-start time can be programmed as required.
5	RT	I	Mode selection and on-time programming pin for Constant On-Time (COT) control. Short RT to GND to select PFM (pulse frequency modulation) operation. Connect a resistor from RT to GND to program the on-time, which sets the switching frequency for COT.
6	PGOOD	O	Power Good output flag pin. PGOOD is connected to the drain of an NFET that holds the pin low when either FB or VOUT is below the regulation target. Use a pullup resistor of 10 kΩ to 100 kΩ to the system voltage rail or VOUT (no higher than 12 V).
7	EN	I	Input pin of the precision enable / UVLO comparator. The converter is enabled when the EN voltage is greater than 1.212 V.
8	VOUT/FB	I	Feedback input to voltage regulation loop. The VOUT pin connects the internal feedback resistor divider to the regulator output voltage for fixed 3.3-V and 5-V options. The FB pin connects the internal feedback comparator to an external resistor divider for the adjustable output voltage option. The FB comparator reference voltage is nominally 1.223 V.
9	HYS	O	Drain of an internal NFET that is turned off when the EN input is greater than the EN threshold. An external resistor from HYS to the EN pin UVLO resistor divider programs the input UVLO hysteresis voltage.
10	GND	G	Regulator ground return.
—	PAD	P	Exposed pad. Connect to the GND pin and system ground on PCB. Path to C_{IN} must be as short as possible.

(1) P = Power, G = Ground, I = Input, O = Output.

Copyright © 2016–2017, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).[1][2]

		MIN	MAX	UNIT
VIN, EN to GND		–0.3	68	V
SW to GND		–0.7	V_{VIN} + 0.3	V
	20-ns transient	–3		V
PGOOD, VOUT[3] to GND	Survives short to automotive battery voltage	–0.3	16	V
HYS to GND		–0.3	7	V
ILIM, SS, RT, FB[4] to GND		–0.3	3.6	V
Maximum junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Fixed output versions.
(4) Adjustable output version.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1][2]		±2000	V
		Charged device model (CDM), per AEC Q100-011[3]	All pins except 1, 5, 6, and 10	±500	
			Pin 1, 5, 6, and 10	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2016–2017, Texas Instruments Incorporated

6.3 Recommended Operating Conditions(1)

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

		MIN	MAX	UNIT
Input voltages	VIN	3	65	V
	EN	–0.3	65	
	PGOOD	–0.3	12	
	HYS	–0.3	5.5	
Output current	I_{OUT} (COT mode)	0	150	mA
	I_{OUT} (PFM mode)	0	100	
Temperature	Operating junction temperature	–40	150	°C

(1) Operating Ratings are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		LM5165-Q1		UNIT
		DRC (VSON)	DGS (VSSOP)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	157.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.9	48.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	77	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	75.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to +125°C junction temperature range. V_{IN} = 12 V (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q-SHD}	VIN DC supply current, shutdown	V_{EN} = 0 V, T_A = 25°C		4.6	6	µA
$I_{Q-SLEEP}$	VIN DC supply current, no load	V_{FB} = 1.5 V, T_A = 25°C		10.5	15	µA
$I_{Q-SLEEP-VINMAX}$	VIN DC supply current, no load	V_{FB} = 1.5 V, V_{VIN} = 65 V, T_A = 25°C		11	15	µA
$I_{Q-ACTIVE-PFM}$	VIN DC supply current, active	PFM mode		205		µA
$I_{Q-ACTIVE-COT}$	VIN DC supply current, active	COT mode, R_{RT} = 107 kΩ		300		µA
POWER SWITCHES						
R_{DSON1}	High-side MOSFET $R_{DS(on)}$	I_{SW} = –10 mA		2		Ω
R_{DSON2}	Low-side MOSFET $R_{DS(on)}$	I_{SW} = 10 mA		1		Ω
CURRENT LIMITING						
$I_{LIM1-VSON}$	High-side peak current threshold VSON-10 package	ILIM shorted to GND	220	240	264	mA
$I_{LIM2-VSON}$		R_{ILIM} = 24.9 kΩ	155	180	205	
$I_{LIM3-VSON}$		R_{ILIM} = 56.2 kΩ	100	120	145	
$I_{LIM4-VSON}$		R_{ILIM} ≥ 100 kΩ	48	60	75	
$I_{LIM1-VSSOP}$	High-side peak current threshold VSSOP-10 package	ILIM shorted to GND	215	240	270	mA
$I_{LIM2-VSSOP}$		R_{ILIM} = 24.9 kΩ	157	180	207	
$I_{LIM3-VSSOP}$		R_{ILIM} = 56.2 kΩ	100	120	146	
$I_{LIM4-VSSOP}$		R_{ILIM} ≥ 100 kΩ	41	60	81	

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \times R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in *Thermal Information*.

Copyright © 2016–2017, Texas Instruments Incorporated

Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to +125°C junction temperature range. V_{IN} = 12 V (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGULATION COMPARATOR						
V_{VOUT50}	VOUT 5-V DC setpoint	LM5165X	4.9	5	5.1	V
V_{VOUT33}	VOUT 3.3-V DC setpoint	LM5165Y	3.23	3.3	3.37	V
I_{VOUT}	VOUT pin input current	V_{VOUT} = 5 V, LM5165X-Q1		6.7		µA
		V_{VOUT} = 3.3 V, LM5165Y-Q1		3.9		
V_{REF1}	Lower FB regulation threshold (PFM, COT)	Adjustable output version	1.205	1.223	1.241	V
V_{REF2}	Upper FB regulation threshold (PFM)		1.22	1.233	1.246	
$FB_{HYS-PFM}$	FB comparator PFM hysteresis	PFM mode		10		mV
$FB_{HYS-COT}$	FB comparator dropout hysteresis	COT mode		4		mV
I_{FB}	FB pin input bias current	V_{FB} = 1 V			100	nA
$FB_{LINE-REG}$	FB threshold variation over line	V_{VIN} = 3 V to 65 V		0.001		%/V
$VOUT_{LINE-REG}$	VOUT threshold variation over line	LM5165X-Q1, V_{VIN} = 6 V to 65 V LM5165Y-Q1, V_{VIN} = 4.5 V to 65 V		0.001		%/V
POWER GOOD						
UVT_{RISING}	PGOOD comparator	FB voltage rising, relative to V_{REF1}		94%		
$UVT_{FALLING}$		FB voltage falling, relative to V_{REF1}		87%		
R_{PGOOD}	PGOOD on-resistance	V_{FB} = 1 V		80	200	Ω
$V_{INMIN-PGOOD}$	Minimum VIN for valid PGOOD	V_{VIN} falling, I_{PGOOD} = 0.1 mA, V_{PGOOD} < 0.5 V		1.2	1.65	V
I_{PGOOD}	PGOOD off-state leakage current	V_{FB} = 1.2 V, V_{PGOOD} = 5.5 V		10	100	nA
ENABLE / UVLO						
V_{IN-ON}	Turnon threshold	VIN voltage rising	2.6	2.75	2.95	V
V_{IN-OFF}	Turnoff threshold	VIN voltage falling	2.35	2.45	2.6	V
V_{EN-ON}	Enable turnon threshold	EN voltage rising	1.163	1.212	1.262	V
V_{EN-OFF}	Enable turnoff threshold	EN voltage falling	1.109	1.144	1.178	V
V_{EN-HYS}	Enable hysteresis			68		mV
V_{EN-SD}	EN shutdown threshold	EN voltage falling	0.3	0.6		V
R_{HYS}	HYS on-resistance	V_{EN} = 1 V		80	200	Ω
I_{HYS}	HYS off-state leakage current	V_{EN} = 1.5 V, V_{HYS} = 5.5 V		10	100	nA
SOFT-START						
I_{SS}	Soft-start charging current	V_{SS} = 1 V		10		µA
T_{SS-INT}	Soft-start rise time	SS floating		900		µs
THERMAL SHUTDOWN						
T_{J-SD}	Thermal shutdown threshold			170		°C
$T_{J-SD-HYS}$	Thermal shutdown hysteresis			10		°C

6.6 Switching Characteristics

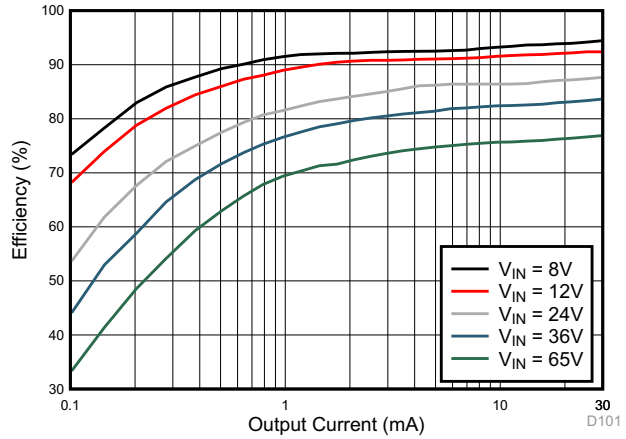
Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON-MIN}	Minimum controllable PWM on-time			180		ns
T_{ON1}	PWM on-time	16 kΩ from RT to GND		250		ns
T_{ON2}	PWM on-time	75 kΩ from RT to GND		1000		ns

Copyright © 2016–2017, Texas Instruments Incorporated

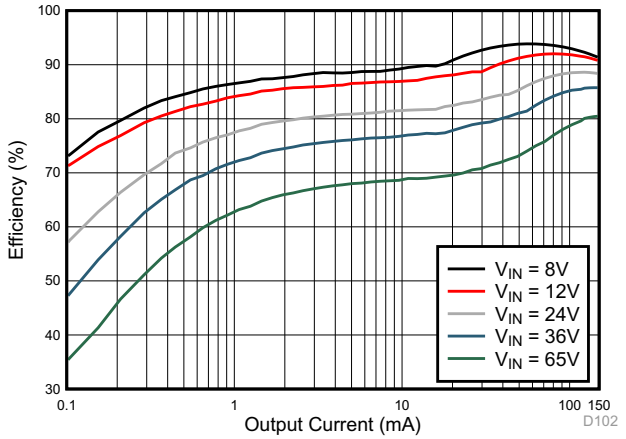
6.7 Typical Characteristics

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to *Typical Applications* for circuit designs.



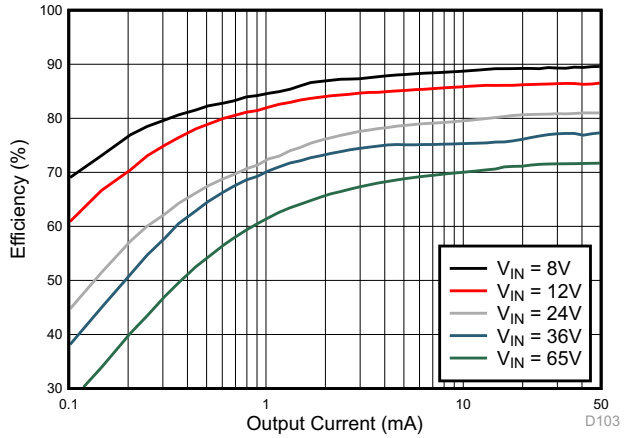
5-V, 25-mA Design | L_F = 470 µH | C_{OUT} = 47 µF | $F_{SW(nom)}$ = 100 kHz | R_{ILIM} ≥ 100 kΩ

Figure 1. Converter Efficiency: 5 V, 25 mA, PFM



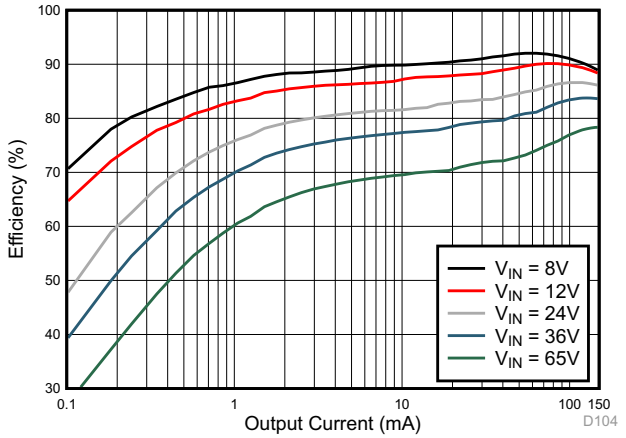
See schematic, Figure 37 | L_F = 220 µH | C_{OUT} = 22 µF | $F_{SW(nom)}$ = 230 kHz | R_{RT} = 133 kΩ

Figure 2. Converter Efficiency: 5 V, 150 mA, COT



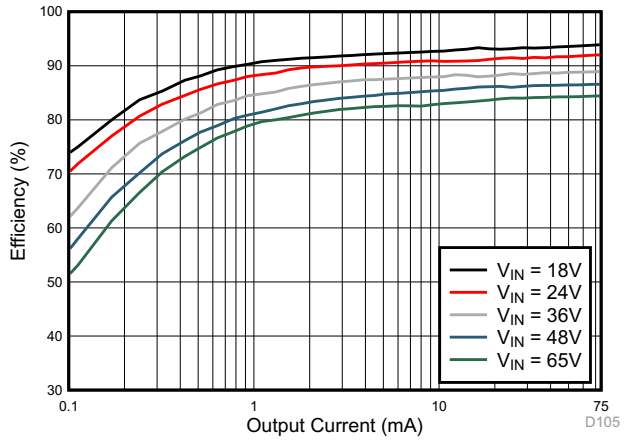
See schematic, Figure 50 | L_F = 47 µH | C_{OUT} = 10 µF | $F_{SW(nom)}$ = 350 kHz | R_{ILIM} = 56.2 kΩ

Figure 3. Converter Efficiency: 3.3 V, 50 mA, PFM



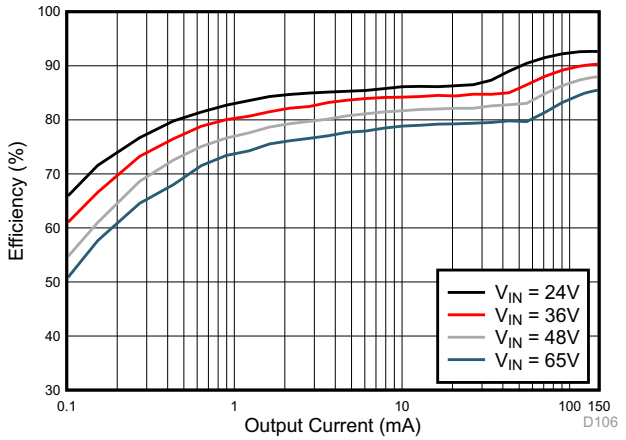
See schematic, Figure 62 | L_F = 150 µH | C_{OUT} = 22 µF | $F_{SW(nom)}$ = 160 kHz | R_{RT} = 121 kΩ

Figure 4. Converter Efficiency: 3.3 V, 150 mA, COT



See schematic, Figure 57 | L_F = 47 µH | C_{OUT} = 10 µF | $F_{SW(nom)}$ = 500 kHz | R_{ILIM} = 24.9 kΩ

Figure 5. Converter Efficiency: 12 V, 75 mA, PFM



See schematic, Figure 65 | L_F = 150 µH | C_{OUT} = 10 µF | $F_{SW(nom)}$ = 600 kHz | R_{RT} = 143 kΩ

Figure 6. Converter Efficiency: 15 V, 150 mA, COT

Copyright © 2016–2017, Texas Instruments Incorporated

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to *Typical Applications* for circuit designs.

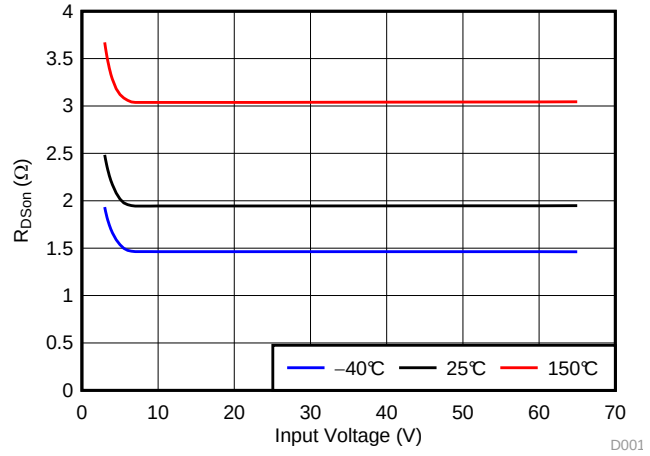


Figure 7. High-Side MOSFET On-State Resistance vs Input Voltage

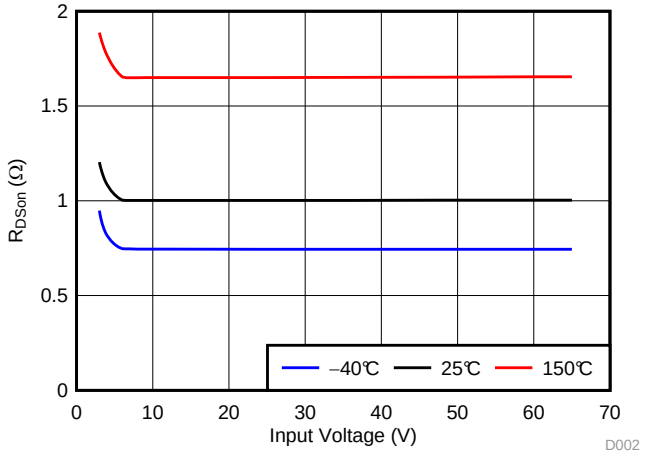


Figure 8. Low-Side MOSFET On-State Resistance vs Input Voltage

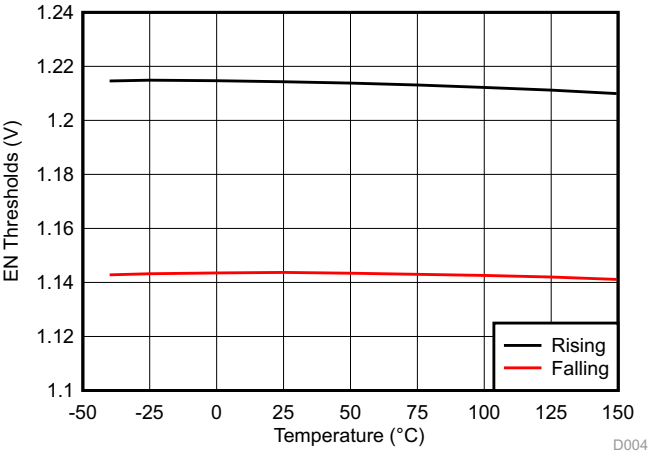


Figure 9. Enable Threshold Voltage vs Temperature

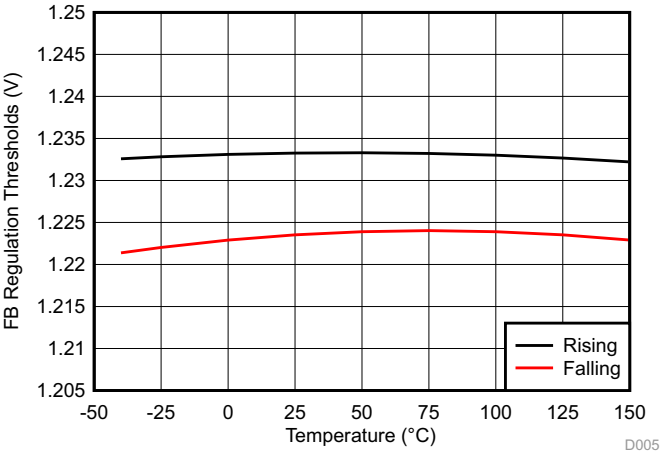
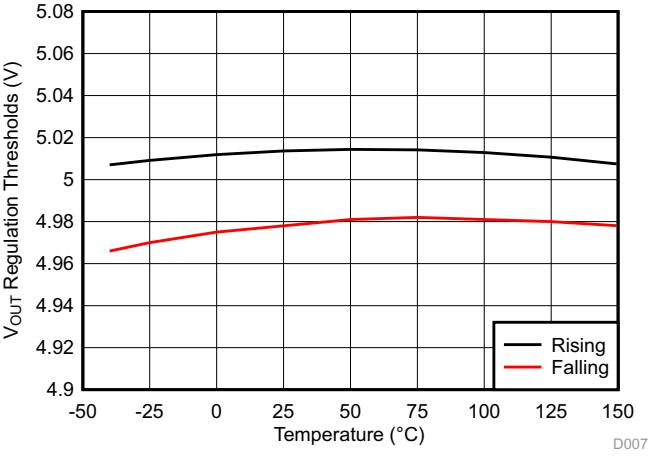
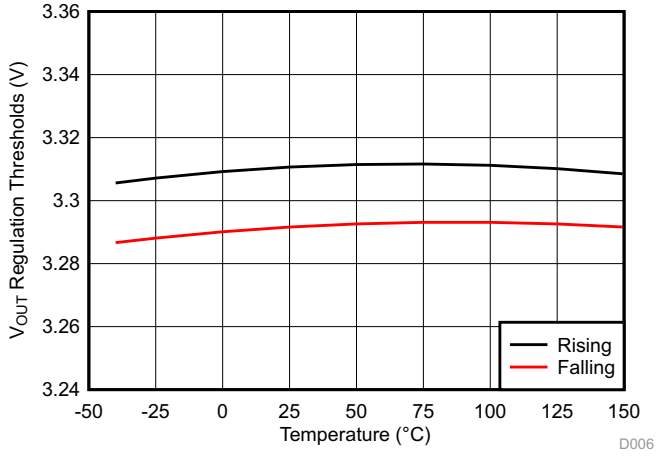


Figure 10. Feedback Comparator Voltage vs Temperature



LM5165X

Figure 11. VOUT Regulation Thresholds vs Temperature



LM5165Y

Figure 12. VOUT Regulation Thresholds vs Temperature

Copyright © 2016–2017, Texas Instruments Incorporated

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to *Typical Applications* for circuit designs.

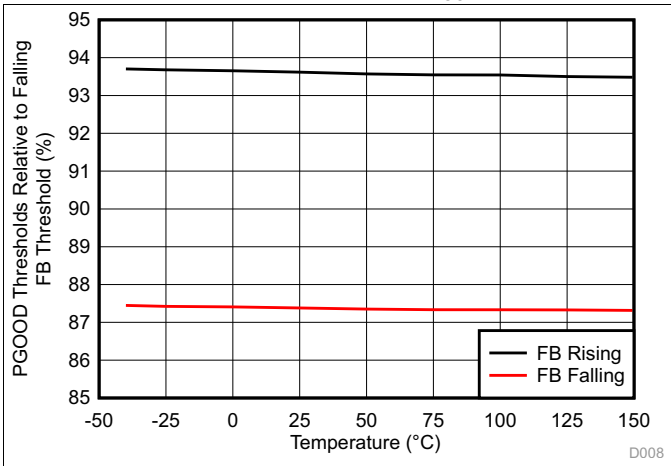


Figure 13. PGOOD Thresholds vs Temperature

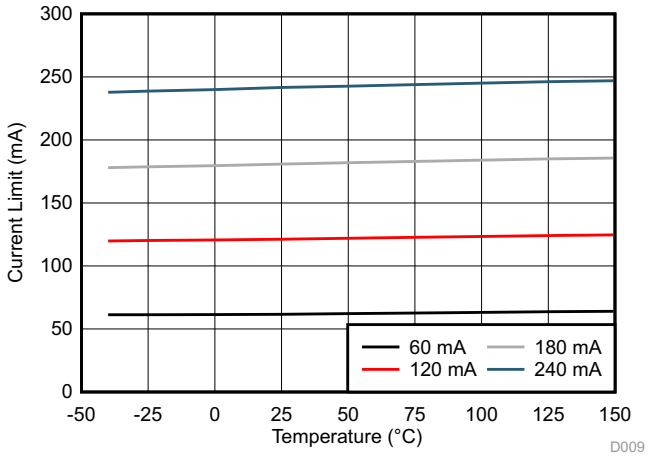


Figure 14. Peak Current Limits vs Temperature

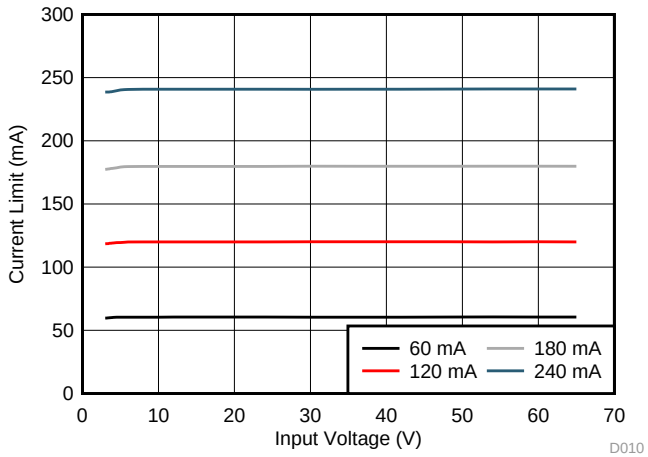


Figure 15. Peak Current Limits vs Input Voltage

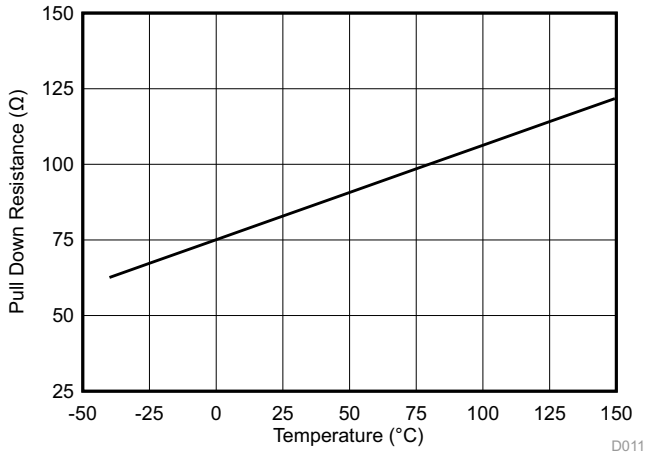


Figure 16. PGOOD and HYS Pulldown $R_{DS(on)}$ vs Temperature

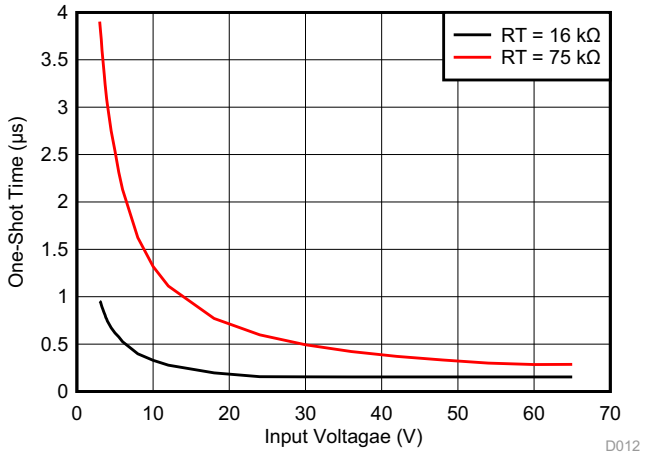


Figure 17. COT One-Shot Timer T_{ON} vs Input Voltage

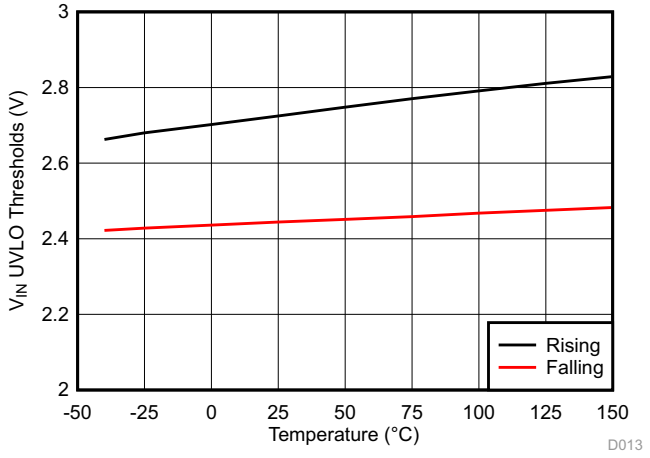


Figure 18. Internal V_{IN} UVLO Voltage vs Temperature

Copyright © 2016–2017, Texas Instruments Incorporated

Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to *Typical Applications* for circuit designs.

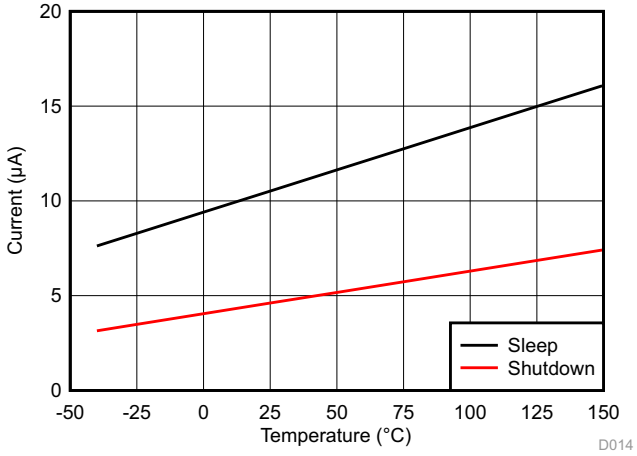


Figure 19. VIN Sleep and Shutdown Supply Current vs Temperature

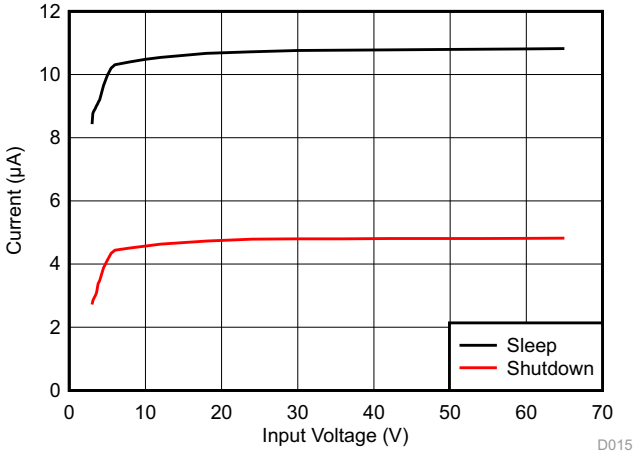
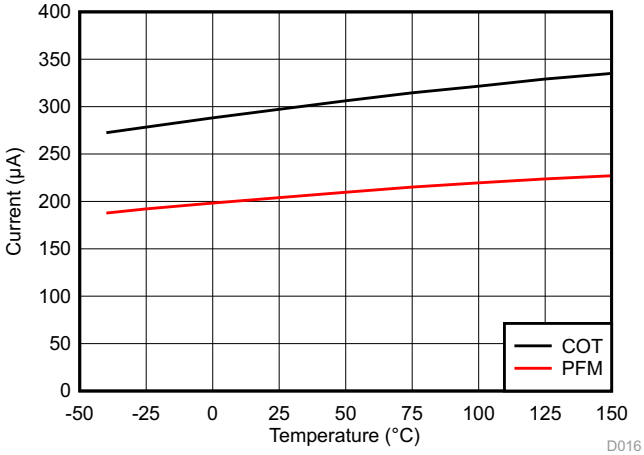
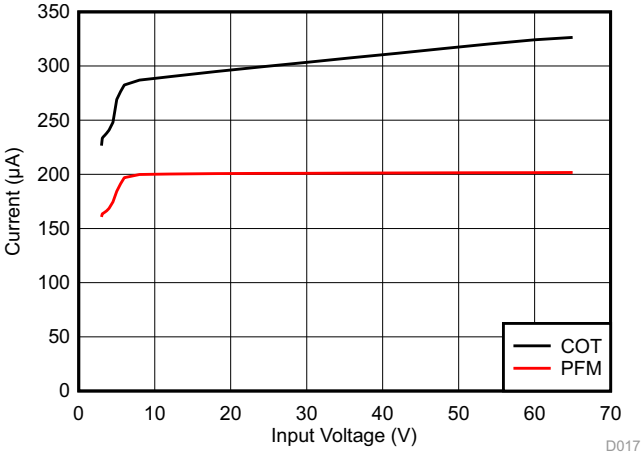


Figure 20. VIN Sleep and Shutdown Supply Current vs Input Voltage



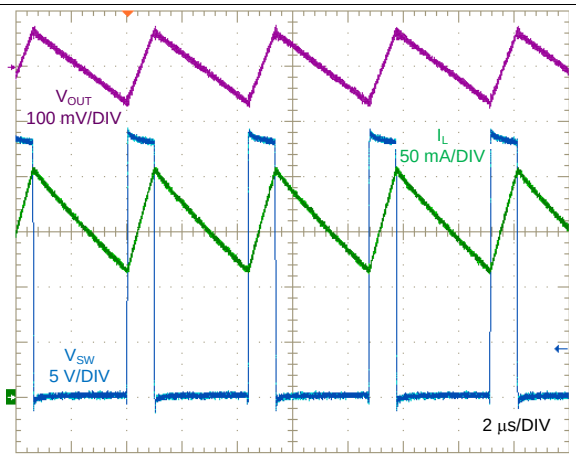
R_{RT} = 75 kΩ

Figure 21. VIN Active Mode Supply Current vs Temperature



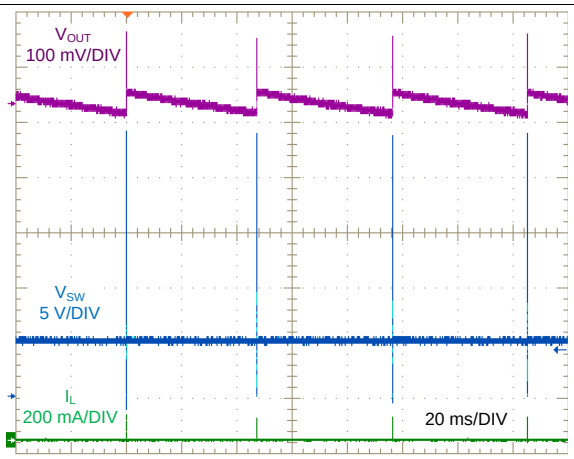
R_{RT} = 75 kΩ

Figure 22. VIN Active Mode Supply Current vs Input Voltage



5-V, 150-mA Design

Figure 23. Full Load Switching Waveforms, COT



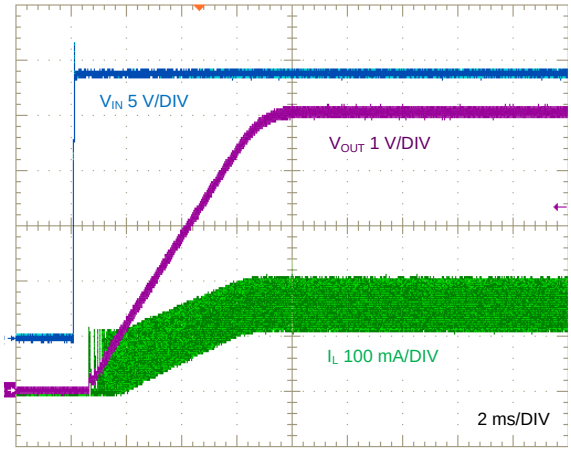
5-V, 150-mA Design

Figure 24. No Load Switching Waveforms, COT

Copyright © 2016–2017, Texas Instruments Incorporated

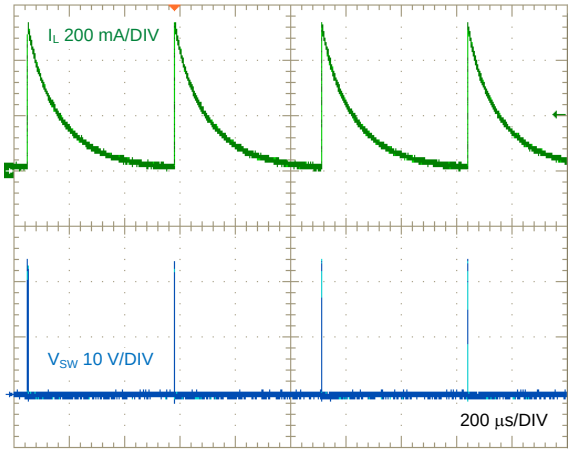
Typical Characteristics (continued)

Unless otherwise specified, V_{IN} = 12 V, V_{OUT} = 5 V. Please refer to *Typical Applications* for circuit designs.



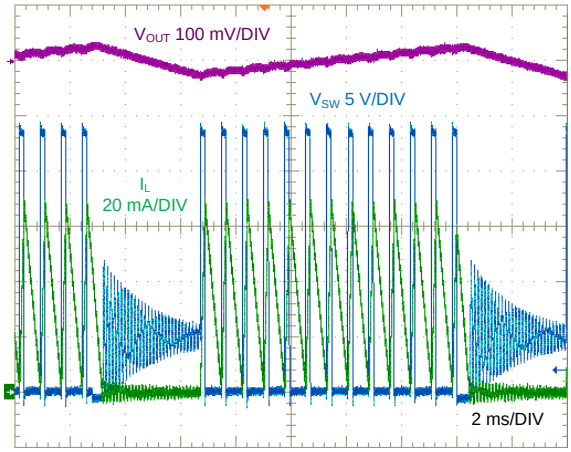
5-V, 150-mA Design

Figure 25. Full Load Start-Up, COT



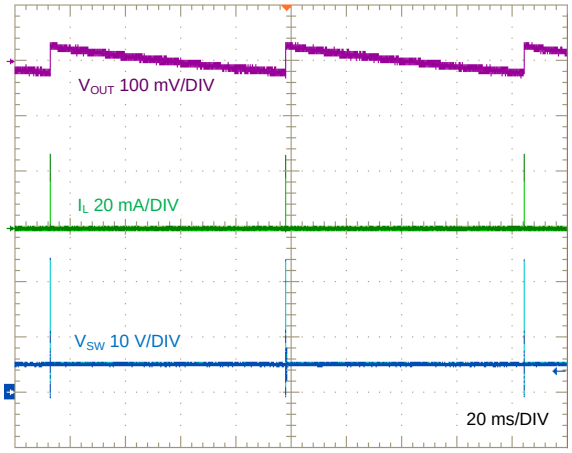
5-V, 150-mA Design

Figure 26. Short Circuit, COT



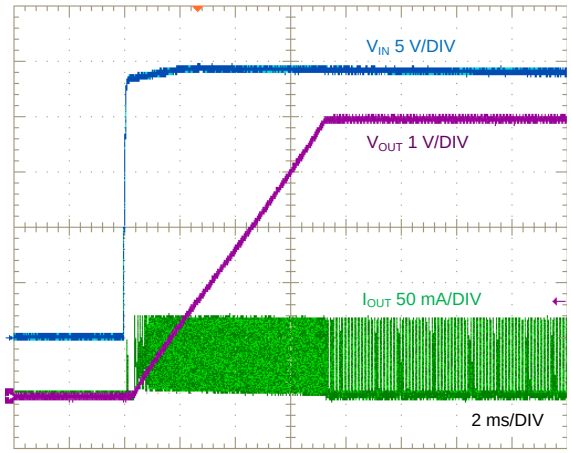
5-V, 25-mA Design

Figure 27. Full Load Switching Waveforms, PFM



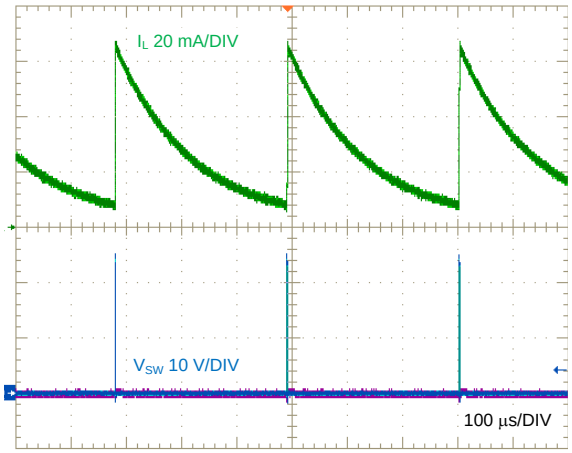
5-V, 25-mA Design

Figure 28. No Load Switching Waveforms, PFM



5-V, 25-mA Design

Figure 29. Full Load Start-Up, PFM



5-V, 25-mA Design

Figure 30. Short Circuit, PFM

Copyright © 2016–2017, Texas Instruments Incorporated

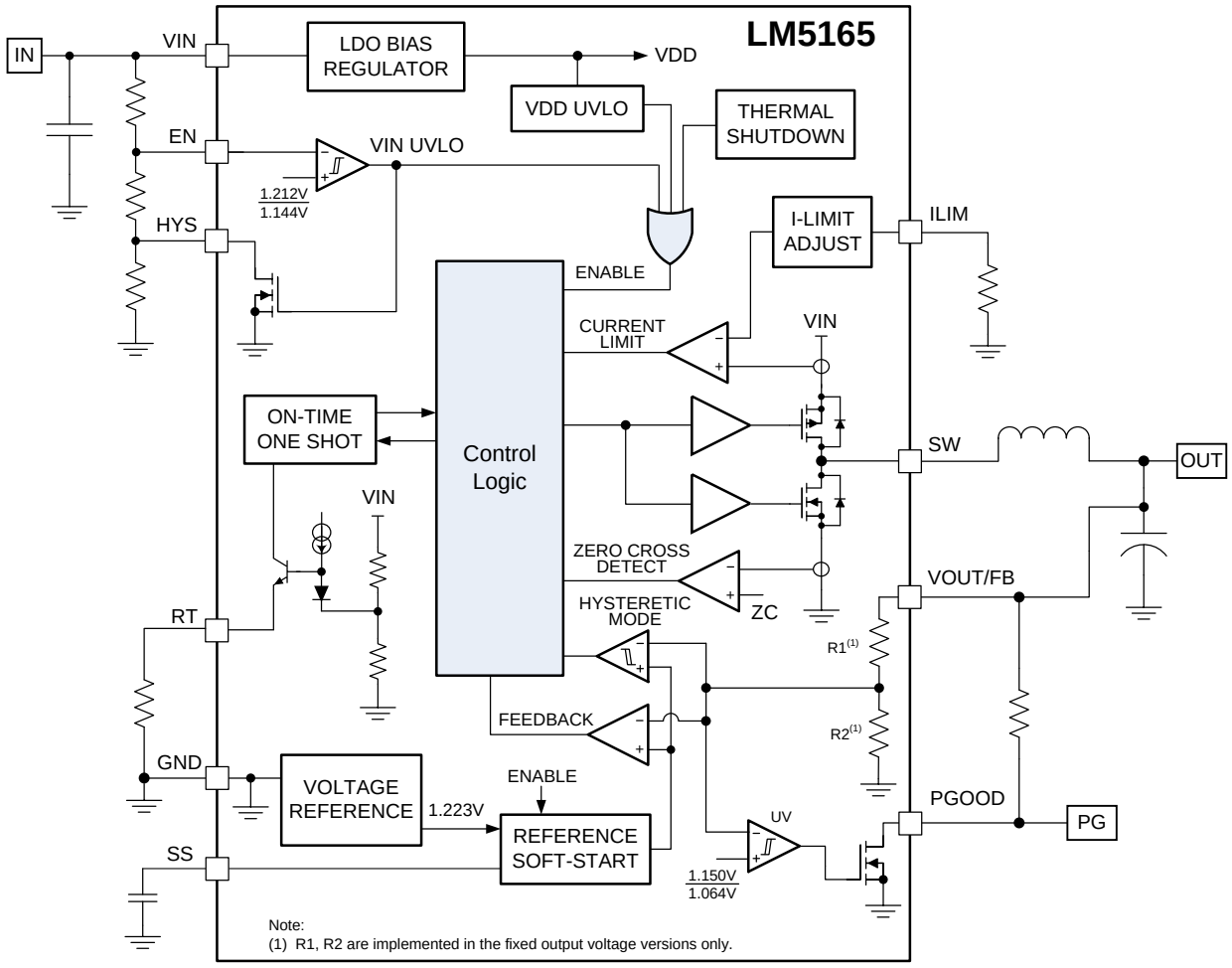
7 Detailed Description

7.1 Overview

The LM5165-Q1 converter is an easy-to-use synchronous buck DC-DC regulator that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 3.3-V, 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated high-side and low-side power MOSFETs, the LM5165-Q1 delivers up to 150-mA DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Designed for simple implementation, a choice of operating modes offers flexibility to optimize its usage according to the target application. In constant on-time (COT) mode of operation, ideal for low-noise, high current, fast load transient requirements, the device operates with predictive on-time switching pulse. A quasi-fixed switching frequency over the input voltage range is achieved by using an input voltage feedforward to set the on-time. Alternatively, pulse frequency modulation (PFM) mode, complemented by an adjustable peak current limit, achieves exceptional light-load efficiency performance. Control loop compensation is not required with either operating mode, reducing design time and external component count.

The LM5165-Q1 incorporates other features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed or externally-adjustable soft-start, monotonic start-up into prebiased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), adjustable cycle-by-cycle current limit for optimal inductor sizing, and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple *Layout*, requiring only a few external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Power MOSFETs

The LM5165-Q1 is a step-down buck converter with integrated high-side PMOS buck switch and low-side NMOS synchronous switch. During the high-side MOSFET on-time, the SW voltage V_{SW} swings up to approximately V_{IN}, and the inductor current increases with slope $(V_{IN} – V_{OUT})/L_F$. When the high-side MOSFET is turned off by the control logic, the low-side MOSFET turns on after an adaptive deadtime. Inductor current flows through the low-side MOSFET with slope $–V_{OUT}/L_F$. Duty cycle D is defined as T_{ON}/T_{SW}, where T_{ON} is the high-side MOSFET conduction time and T_{SW} is the switching period.

7.3.2 Selectable PFM or COT Mode Converter Operation

Figure 31 and Figure 32 show converter schematics for PFM and COT modes of operation.

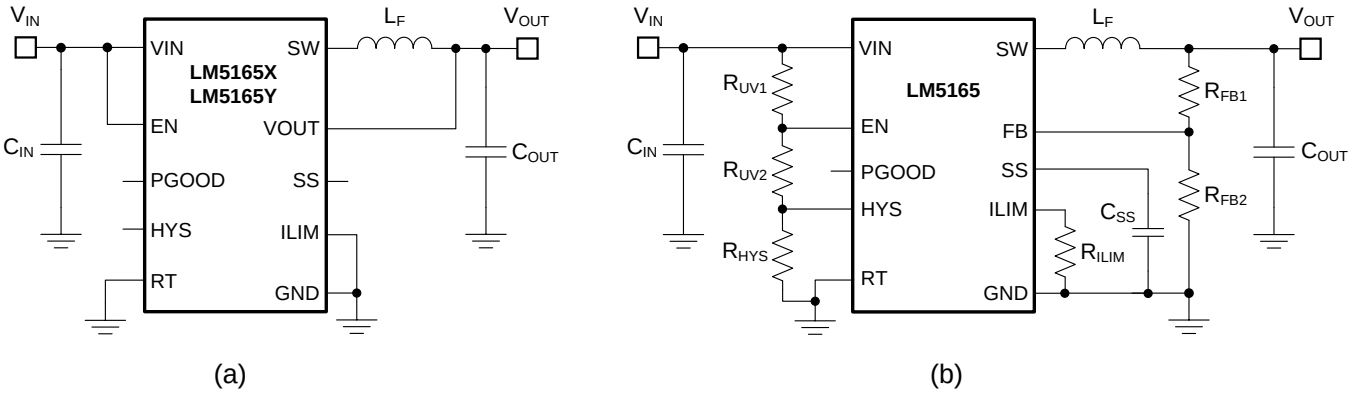


Figure 31. PFM Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage With Programmable Soft Start, Current Limit, and UVLO

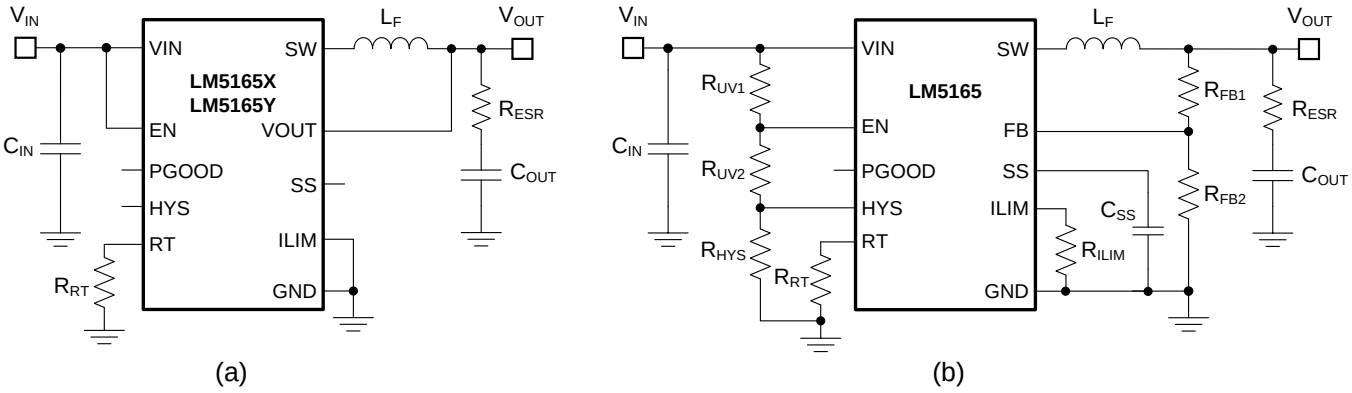


Figure 32. COT Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage With Programmable Soft Start, Current Limit, and UVLO

The LM5165-Q1 operates in PFM mode when RT is shorted to GND. Configured as such, the LM5165-Q1 behaves as a hysteretic voltage regulator operating in boundary conduction mode, controlling the output voltage within upper and lower hysteresis levels according to the PFM feedback comparator hysteresis of 10 mV. Figure 33 is a representation of the relevant output voltage and inductor current waveforms. The LM5165-Q1 provides the required switching pulses to recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut off. The load current is supported by the output capacitor during this time, and the LM5165-Q1 current consumption approaches the sleep quiescent current of 10.5 µA. The sleep period duration depends on load current and output capacitance.

Copyright © 2016–2017, Texas Instruments Incorporated

Feature Description (continued)

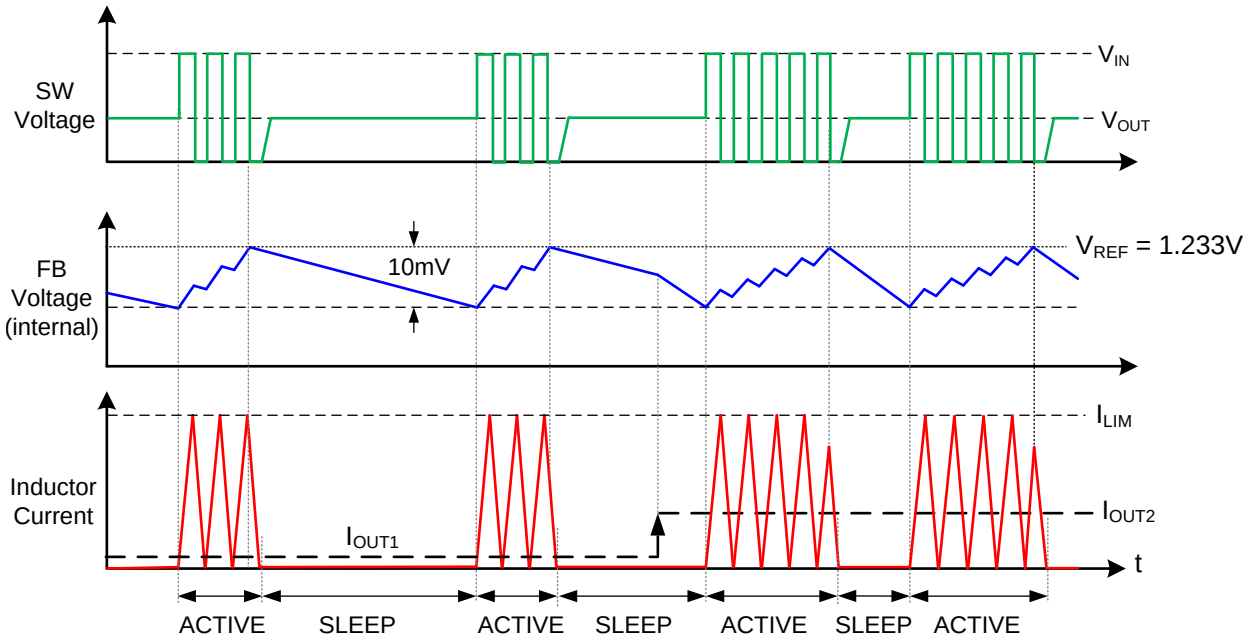


Figure 33. PFM Mode SW Node Voltage, Feedback Voltage, and Inductor Current Waveforms

When operating in PFM mode at given input and output voltages, the chosen filter inductance dictates the PFM pulse frequency in Equation 1:

$$F_{SW(PFM)} = \frac{V_{OUT}}{L_F \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

where

- $I_{PK(PFM)}$ corresponds to one of the four programmable levels for peak limit of inductor current. See *Adjustable Current Limit* for more detail.

Configured in COT mode, the LM5165-Q1 based converter turns on the high-side MOSFET with on-time inversely proportional to V_{IN} to operate with essentially fixed switching frequency when in continuous conduction mode (CCM). Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains highest efficiency at light load currents by decreasing the effective switching frequency. The COT-controlled LM5165-Q1 waveforms in CCM and DEM are represented in Figure 34. The PWM on-time is set by resistor R_{RT} connected from RT to GND as shown in Figure 32. The control loop maintains a constant output voltage by adjusting the PWM off-time.

Copyright © 2016–2017, Texas Instruments Incorporated

Feature Description (continued)

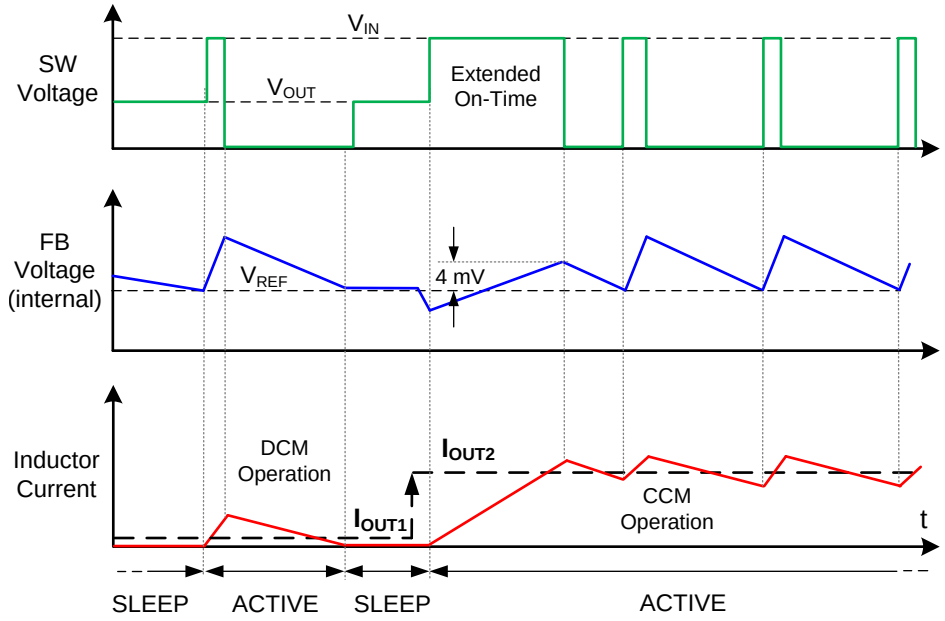


Figure 34. COT Mode SW Node Voltage, Feedback Voltage, and Inductor Current Waveforms

The required on-time adjust resistance for a particular frequency is given in Equation 2 and tabulated in Table 1. The maximum programmable on-time is 15 µs.

$$R_{RT}\left[k\Omega\right] = \frac{V_{OUT}\left[V\right]}{F_{SW}\left[kHz\right]} \cdot \frac{10^4}{1.75} \quad (2)$$

Table 1. On-Time Adjust Resistance (E96 EIA Values) for Various Switching Frequencies and Output Voltages

F_{SW} (kHz)	R_{RT} (kΩ)			
	V_{OUT} = 1.8 V	V_{OUT} = 3.3 V	V_{OUT} = 5 V	V_{OUT} = 12 V
100	102	187	287	681
200	51.1	95.3	143	240
300	34	63.4	95.3	226
400	25.5	47.5	71.5	169
500	20.5	37.4	57.6	137
600	16.9	31.6	47.5	115

The choice of control mode and switching frequency requires a compromise between conversion efficiency, quiescent current, and passive component size. Lower switching frequency implies reduced switching losses (including gate charge losses, transition losses, and so forth) and higher overall efficiency. Higher switching frequency, on the other hand, implies a smaller LC output filter and hence a more compact design. Lower inductance also helps transient response as the large-signal slew rate of inductor current increases. The ideal switching frequency in a given application is a tradeoff and thus is determined on a case-by-case basis. It relates to the input voltage, output voltage, most frequent load current level(s), external component choices, and circuit size requirement. At light loads, the PFM converter has a relatively longer sleep time interval and thus operates with lower input quiescent current and higher efficiency.

Copyright © 2016–2017, Texas Instruments Incorporated

7.3.3 COT Mode Light-Load Operation

Diode emulation mode (DEM) operation occurs when the low-side MOSFET switches off as inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and preventing negative current conduction reduces conduction loss. Power conversion efficiency is thus higher in a DEM converter than an equivalent forced-PWM CCM converter. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases.

7.3.4 Low Dropout Operation and 100% Duty Cycle Mode

If R_{DSON1} and R_{DSON2} are the high-side and low-side MOSFET on-state resistances, respectively, and R_{DCR} is the inductor DC resistance, the duty cycle in COT (CCM) or PFM mode is given by Equation 3.

$$D = \frac{V_{OUT} + \left(R_{DSON2} + R_{DCR}\right) \cdot I_{OUT}}{V_{IN} - \left(R_{DSON1} - R_{DSON2}\right) \cdot I_{OUT}} \approx \frac{V_{OUT}}{V_{IN}} \quad (3)$$

The LM5165-Q1 offers a low input voltage to output voltage dropout by engaging the high-side MOSFET at 100% duty cycle. In COT mode, a frequency foldback feature effectively extends maximum duty cycle to 100% during low dropout conditions or load-on transients. Based on the 4-mV FB comparator dropout hysteresis, the duty cycle extends as needed at low input voltage conditions, corresponding to lower switching frequency. The PWM on-time extends based on the requirement that the FB voltage exceeds the dropout hysteresis during a given on-time. 100% duty cycle operation is eventually reached as the input voltage decreases towards the output setpoint. The output voltage stays in regulation at a lower supply voltage, thus achieving an extremely low dropout voltage.

Note that PFM mode operation provides an inherently natural transition to 100% duty cycle if needed for low dropout applications.

Use Equation 4 to calculate the minimum input voltage to maintain output regulation.

$$V_{IN(min)} = V_{OUT} + I_{OUT} \cdot \left(R_{DSON1} + R_{DCR}\right) \quad (4)$$

7.3.5 Adjustable Output Voltage (FB)

Three voltage feedback options are available: the fixed 3.3-V and 5-V versions include internal feedback resistors that sense the output directly through the VOUT pin; the adjustable voltage option senses the output through an external resistor divider connected from the output to the FB pin.

The LM5165-Q1 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF1}. A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} setpoint, calculate R_{FB2} based on the selected R_{FB1} using Equation 5.

$$R_{FB2} = \frac{1.223V}{V_{OUT} - 1.223V} \cdot R_{FB1} \quad (5)$$

Selecting R_{FB1} of 100 kΩ is recommended for most applications. A larger R_{FB1} consumes less DC current, mandatory if light-load efficiency is critical. High feedback resistances generally require more careful feedback path PCB layout. It is important to route the feedback trace away from the noisy area of the PCB. For more layout recommendations, see *Layout*.

7.3.6 Adjustable Current Limit

The LM5165-Q1 manages overcurrent conditions by cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold set by the ILIM pin. Current is sensed after a leading-edge blanking time following the high-side MOSFET turnon transition. The propagation delay of current limit comparator is 100 ns.

Four programmable peak current levels are available: 60 mA, 120 mA, 180 mA and 240 mA, corresponding to resistors of 100 kΩ, 56.2 kΩ, 24.9 kΩ and 0 Ω connected at the ILIM pin, respectively. In turn, 25-mA, 50-mA, 75-mA, and 100-mA output current levels in boundary conduction mode PFM operation are possible, respectively.

Copyright © 2016–2017, Texas Instruments Incorporated

Note that in PFM mode, the inductor current ramps from zero to the chosen peak threshold every switching cycle. Consequently, the maximum output current is equal to half the peak inductor current. Meanwhile, the corresponding output current capability in COT mode is higher as the ripple current is determined by the input and output voltage and the chosen inductance.

7.3.7 Precision Enable (EN) and Hysteresis (HYS)

The precision EN input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed independently through the HYS pin for application specific power-up and power-down requirements. EN connects to a comparator-based input referenced to a 1.212-V bandgap voltage with 68-mV hysteresis. An external logic signal can be used to drive the EN input to toggle the output on and off and for system sequencing or protection. The simplest way to enable the LM5165's operation is to connect EN directly to VIN. This allows the LM5165-Q1 to start up when V_{IN} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in Figure 35 to establish a precision UVLO level. In tandem with the EN setting, use HYS to increase the voltage hysteresis as needed.

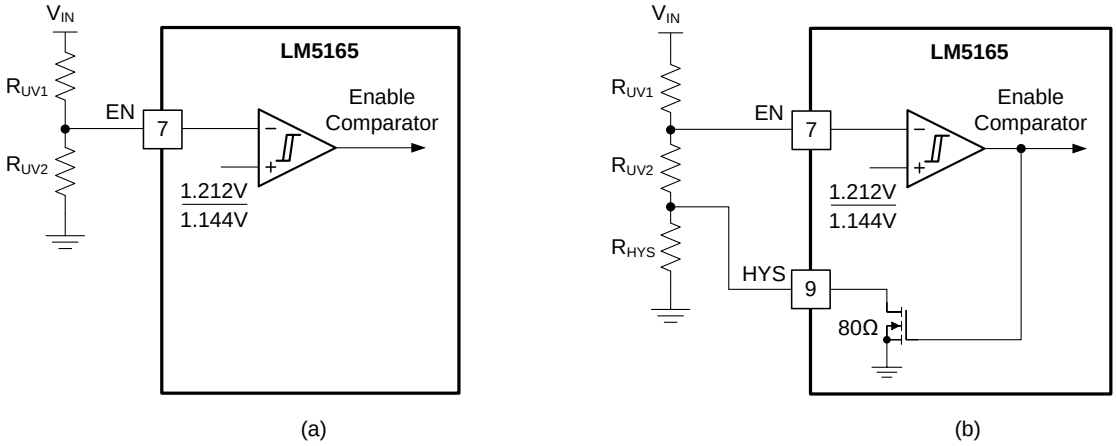


Figure 35. Programmable Input Voltage UVLO With (a) Fixed Hysteresis, (b) Adjustable Hysteresis

Use Equation 6 and Equation 7 to calculate the input UVLO voltages turnon and turnoff voltages, respectively.

$$V_{IN(on)} = 1.212V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (6)$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \quad (7)$$

There is also a low I_Q shutdown mode when EN is pulled below a base-emitter voltage drop (approximately 0.6 V at room temperature). If EN is below this hard shutdown threshold, the internal LDO regulator powers off and the internal bias supply rail collapses, shutting down the bias currents of the LM5165-Q1. The LM5165-Q1 operates in standby mode when the EN voltage is between the hard shutdown and precision enable thresholds.

7.3.8 Power Good (PGOOD)

The LM5165-Q1 provides a PGOOD flag pin to indicate when the output voltage is within the regulation level. Use the PGOOD signal for start-up sequencing of downstream converters, as shown in Figure 36, or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 12 V. Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

Copyright © 2016–2017, Texas Instruments Incorporated

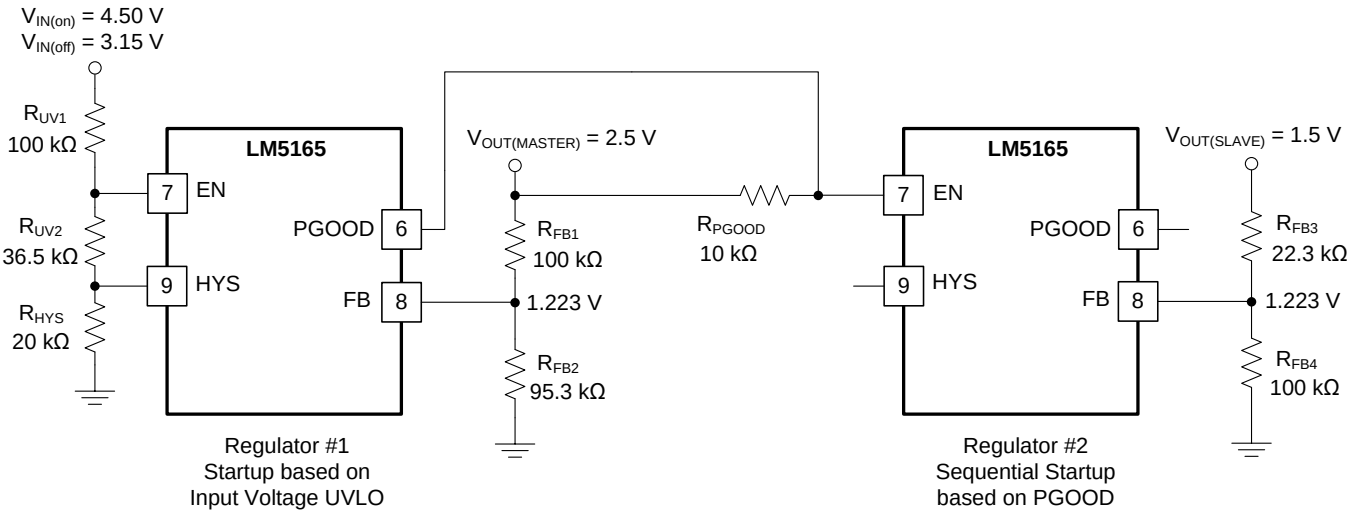


Figure 36. Master-Slave Sequencing Implementation Using PGOOD and EN

When the FB voltage exceeds 94% of the internal reference V_{REF1}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 87% of V_{REF1}, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 µs.

7.3.9 Configurable Soft Start (SS)

The LM5165-Q1 has a flexible and easy-to-use soft-start control pin, SS. The soft-start feature prevents inrush current impacting the LM5165-Q1 and the input supply when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. Selectable and adjustable start-up timing options include minimum delay (no soft-start), 900-µs internally fixed soft start, and an externally programmable soft start.

The simplest way to use the LM5165-Q1 is to leave the SS pin open. The LM5165-Q1 employs the internal soft-start control ramp and starts up to the regulated output voltage in 900 µs. In applications with a large amount of output capacitance, higher V_{OUT}, or other special requirements, extend the soft-start time by connecting an external capacitor C_{SS} from SS to GND. Longer soft-start time further reduces the supply current needed to charge the output capacitors and supply any output loading. An internal current source I_{SS} of 10 µA charges C_{SS} and generates a ramp to control the ramp rate of the output voltage. Use Equation 8 to calculate the C_{SS} capacitance for a desired soft-start time t_{SS}.

$$C_{SS}\left[nF\right] = 8.1 \cdot t_{SS}\left[ms\right] \tag{8}$$

C_{SS} is discharged by an internal FET when V_{OUT} is shutdown by EN, UVLO, or thermal shutdown.

It is desirable in some applications for the output voltage to reach its nominal setpoint in the shortest possible time. Connecting a 100-kΩ resistor from SS to GND disables the soft-start circuit, and the LM5165-Q1 operates in current limit during start-up to rapidly charge the output capacitance.

As negative inductor current is prevented, the LM5165-Q1 is capable of start-up into prebiased output conditions. With a prebiased output voltage, the LM5165-Q1 waits until the soft-start ramp allows regulation above the prebiased voltage and then follows the soft-start ramp to the regulation setpoint.

7.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the LM5165-Q1 restarts when the junction temperature falls to 160°C.

Copyright © 2016–2017, Texas Instruments Incorporated

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the LM5165-Q1. When V_{EN} is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4.6 µA at V_{IN} = 12 V. The LM5165-Q1 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal bias rail LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 0.6 V and below the precision enable threshold (1.212 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UV threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode in COT

The LM5165-Q1 is in active mode when V_{EN} is above the precision enable threshold and the internal bias rail is above its UV threshold. In COT active mode, the LM5165-Q1 is in one of three modes depending on the load current:

1. CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple;
2. Pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation. Refer to *COT Mode Light-Load Operation* for more detail;
3. Frequency foldback mode to maintain output regulation at low dropout and for improved load-on transient response. Refer to *Low Dropout Operation and 100% Duty Cycle Mode* for more detail.

7.4.4 Active Mode in PFM

Similarly, the LM5165-Q1 is in PFM active mode when V_{EN} and the internal bias rail are above the relevant thresholds, FB has fallen below the lower hysteresis level (V_{REF1}), and boundary conduction mode is recharging the output capacitor to the upper hysteresis level (V_{REF2}). There is a 4-µs wake-up delay from sleep to active states.

7.4.5 Sleep Mode in PFM

The LM5165-Q1 is in PFM sleep mode when V_{EN} and the internal bias rail are above the relevant threshold levels, V_{FB} has exceeded the upper hysteresis level (V_{REF2}), and the output capacitor is sourcing the load current. In PFM sleep mode, the LM5165-Q1 operates with very low quiescent current.

Copyright © 2016–2017, Texas Instruments Incorporated

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5165-Q1 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a LM5165-Q1-based converter, a comprehensive LM5165-Q1 Quick-start design tool is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for both COT and PFM modes using specific circuit design examples.

As mentioned previously, the LM5165-Q1 also integrates several optional features to meet system design requirements, including precision enable, UVLO, programmable soft start, programmable switching frequency in COT mode, adjustable current limit, and PGOOD indicator. Each application incorporates these features as needed for a more comprehensive design. The application circuits detailed below show LM5165-Q1 configuration options suitable for several application use cases. Refer to the *LM5165EVM-HD-C50X* and *LM5165EVM-HD-P50A* EVM user's guides for more detail.

8.2 Typical Applications

TIDesigns

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM5165-powered implementation, refer to *Field Transmitter with Bluetooth® Low Energy Connectivity Powered from 4 to 20-mA Current Loop* reference design.

8.2.1 Design 1: Wide V_{IN}, Low I_Q COT Converter Rated at 5 V, 150 mA

The schematic diagram of a 5-V, 150-mA COT converter is given in Figure 37.

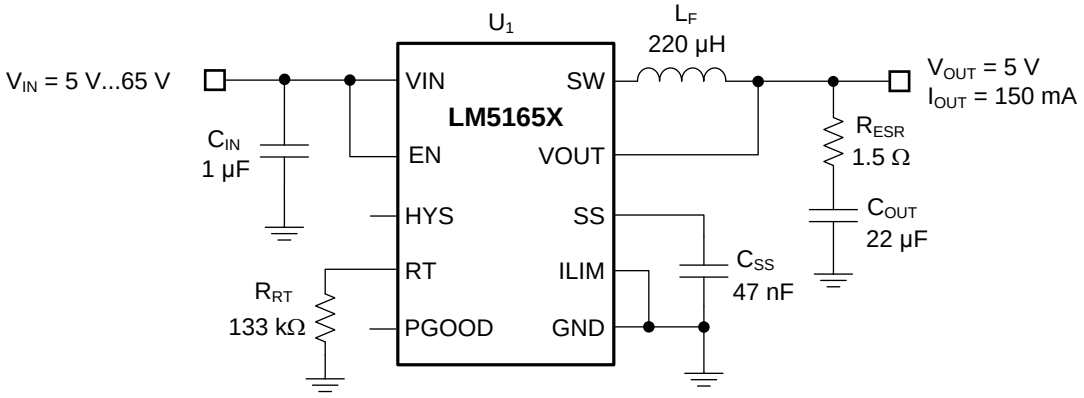


Figure 37. Schematic for Design 1 With $V_{IN(nom)}$ = 12 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 150 mA, $F_{SW(nom)}$ = 220 kHz

8.2.1.1 Design Requirements

The target full-load efficiency is 91% based on a nominal input voltage of 12 V and an output voltage of 5 V. The required input voltage range is 5 V to 65 V. The LM5165X-Q1 is chosen to deliver a fixed 5-V output voltage. The switching frequency is set by resistor R_{RT} at 220 kHz. The output voltage soft-start time is 6 ms. The required components are listed in Table 2.

Copyright © 2016–2017, Texas Instruments Incorporated

Table 2. List of Components for Design 1

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7R, 1206 ceramic	TDK	C3216X7R2A105K160AA
C_{OUT}	1	22 µF, 10 V, X7R, 1206 ceramic	Murata	GRM31CR71A226KE15L
L_F	1	220 µH ±20%, 0.29 A, 0.92 Ω typ DCR, 5.8 x 5.8 x 2.8 mm	Würth Electronik	WE-TPC 5828 744053221
		220 µH ±30%, 0.3 A, 1.25 Ω max DCR, 5.8 x 5.8 x 3.0 mm	Bourns	SRR5028-221Y
R_{ESR}	1	1.5 Ω, 5%, 0402	Std	Std
R_{RT}	1	133 kΩ, 1%, 0402	Std	Std
C_{SS}	1	47 nF, 10 V, X7R, 0402 ceramic	Std	Std
U_1	1	LM5165X-Q1 Synchronous Buck Converter, VSON-10, 5V Fixed	TI	LM5165XQDRCRQ1

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5165-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Switching Frequency – R_T

As mentioned, the switching frequency of a COT-configured LM5165-Q1 is set by the on-time programming resistor at the RT pin. As shown by Equation 2, a standard 1% resistor of 133 kΩ gives a switching frequency of 230 kHz.

Note that at very low duty cycles, the minimum controllable on-time of the high-side MOSFET, $T_{ON(min)}$, of 180 ns may affect choice of switching frequency. In CCM, $T_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. The minimum controllable duty cycle is given by Equation 9:

$$D_{MIN} = T_{ON(min)} \cdot F_{SW} \tag{9}$$

Given a fixed $T_{ON(min)}$, it follows that higher switching frequency implies a larger minimum controllable duty cycle. Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size and efficiency. The maximum supply voltage for a given $T_{ON(min)}$ before switching frequency reduction occurs is given by Equation 10.

$$V_{IN(max)} = \frac{V_{OUT}}{T_{ON(min)} \cdot F_{SW}} \tag{10}$$

8.2.1.2.3 Filter Inductor – L_F

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by Equation 11 and Equation 12.

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L_F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{11}$$

Copyright © 2016–2017, Texas Instruments Incorporated

$$I_{L(peak)} = I_{OUT(max)} + \frac{\Delta I_L}{2} \quad (12)$$

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 50% of the rated load current at nominal input voltage. Calculate the inductance using Equation 13.

$$L_F = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_{L(nom)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) \quad (13)$$

Choosing a 220-µH inductor in this design results in 55-mA peak-to-peak ripple current at nominal input voltage of 12 V, equivalent to 37% of the 150-mA rated load current. The peak inductor current at maximum input voltage of 65 V is 195 mA, sufficiently below the LM5165-Q1 peak current limit of 240 mA.

Check the inductor datasheet to ensure that the inductor's saturation current is well above the current limit setting of a particular design. Ferrite designs have low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. However, ferrite core materials exhibit a hard saturation characteristic – the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that inductor saturation current generally deceases as the core temperature increases.

8.2.1.2.4 Output Capacitors – C_{OUT}

Select the output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that arises from the triangular ripple current flowing in the capacitor. Select an output capacitance using Equation 14 to limit the voltage ripple component to 0.5% of the output voltage.

$$C_{OUT} \geq \frac{\Delta I_{L(nom)} \cdot 100}{F_{SW} \cdot V_{OUT}} \quad (14)$$

Substituting $\Delta I_{L(nom)}$ of 55 mA gives C_{OUT} greater than 5 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 22-µF, 10-V capacitor with X7R dielectric in 1206 footprint.

8.2.1.2.5 Series Ripple Resistor – R_{ESR}

Select a series resistor such that sufficient ripple in phase with the SW node voltage appears at the feedback node, FB. Use Equation 15 to calculate the required ripple resistance, designated R_{ESR}.

$$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{REF} \cdot \Delta I_{L(nom)}} \quad (15)$$

With V_{OUT} of 5 V, V_{REF} of 1.223 V, and $\Delta I_{L(nom)}$ of 55 mA at the nominal input voltage of 12 V, the required R_{ESR} is 1.5 Ω. Calculate the total output voltage ripple in CCM using Equation 16.

$$\Delta V_{OUT} = \Delta I_L \cdot \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)^2} \quad (16)$$

8.2.1.2.6 Input Capacitor – C_{IN}

An input capacitor is necessary to limit the input ripple voltage while providing switching-frequency AC current to the buck power stage. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5165-Q1. The input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by Equation 17.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \quad (17)$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 18.

Copyright © 2016–2017, Texas Instruments Incorporated

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot (\Delta V_{IN} - I_{OUT} \cdot R_{ESR})} \quad (18)$$

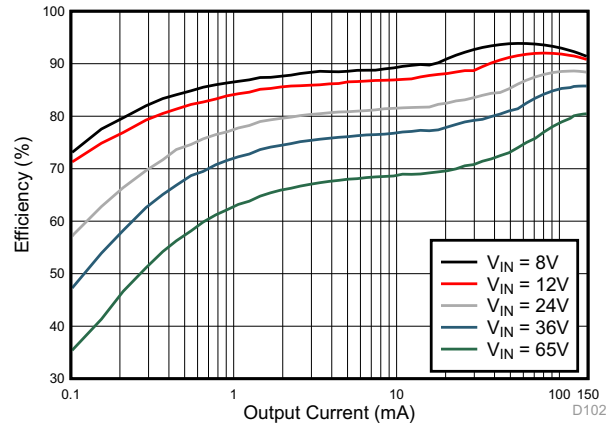
The recommended high-frequency capacitance is 1 µF or higher and should be a high-quality ceramic type X5R or X7R with sufficient voltage rating. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the LM5165-Q1 circuit is not located within approximately 5 cm from the input voltage source. This capacitor provides damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics.

8.2.1.2.7 Soft-Start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 47 nF based on Equation 8 to achieve a soft-start time of 6 ms.

8.2.1.3 Application Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.



V_{OUT} = 5 V

Figure 38. Efficiency

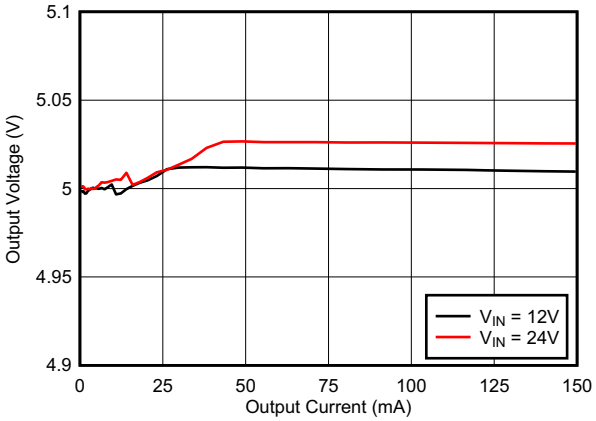
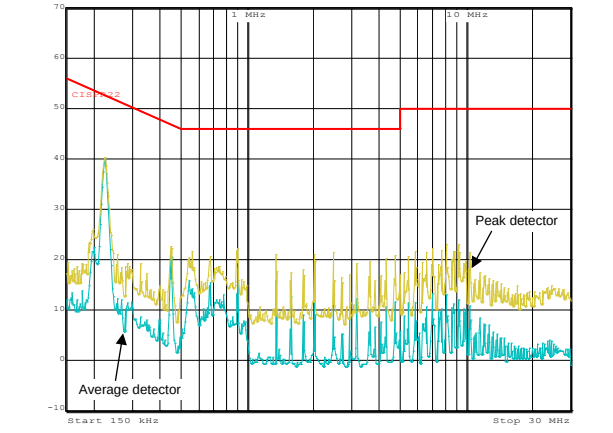
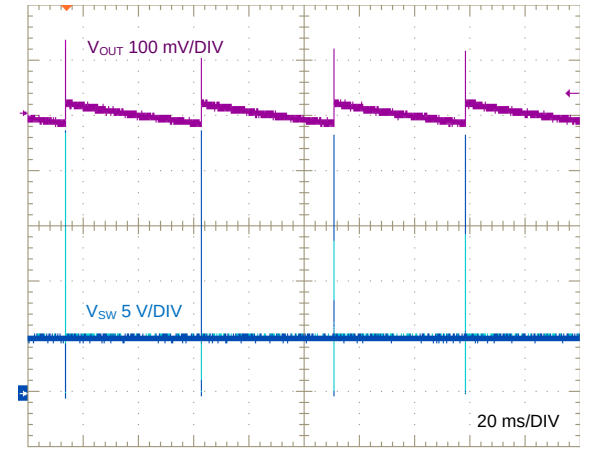


Figure 39. Load Regulation



V_{IN} = 13.5 V
I_{OUT} = 100 mA
L_{IN} = 22 µH
$C_{IN(EXT)}$ = 10 µF

Figure 40. EMI Plot – CISPR 22 Filtered Emissions



V_{IN} = 12 V
I_{OUT} = 0 mA

Figure 41. SW Node and Output Ripple Voltage, No Load

Copyright © 2016–2017, Texas Instruments Incorporated

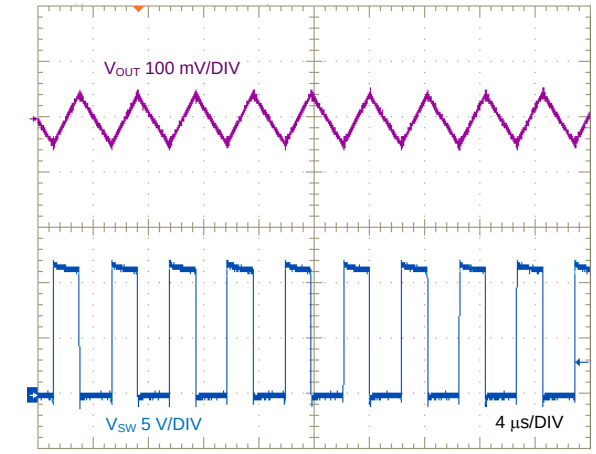


Figure 42. SW Node and Output Ripple Voltage, Full Load

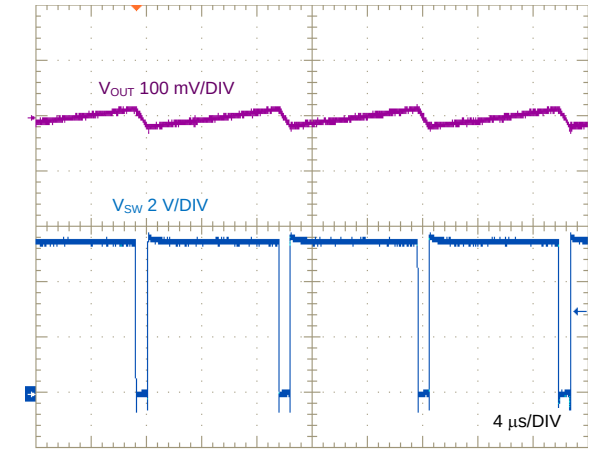


Figure 43. SW Node and Output Ripple Voltage Showing Frequency Foldback Near Dropout

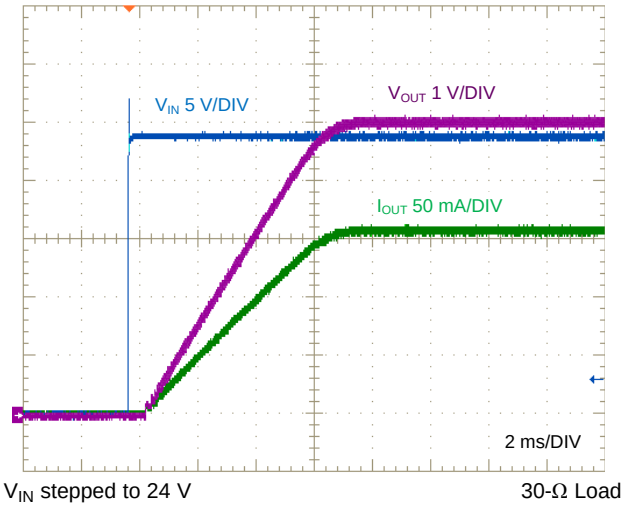


Figure 44. Startup, Full Load

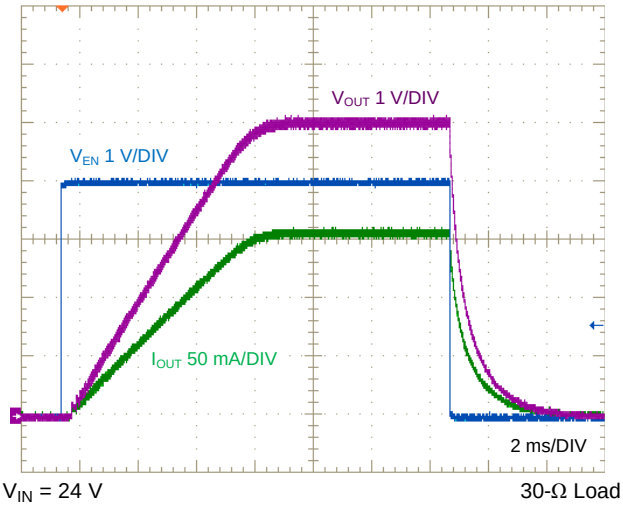


Figure 45. Enable ON and OFF

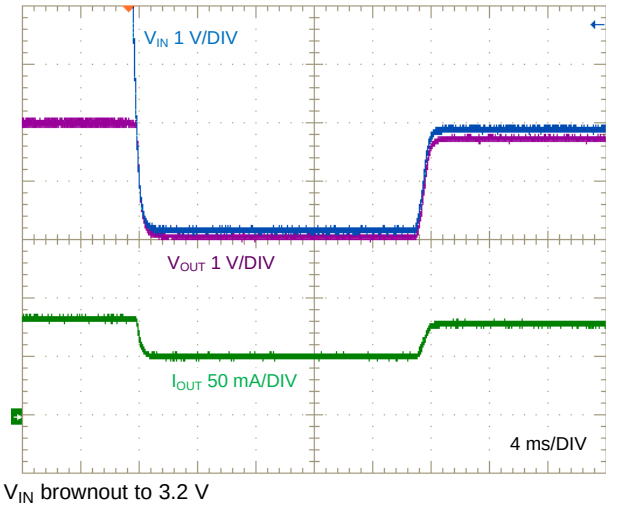


Figure 46. Dropout Performance, 75-mA Resistive Load

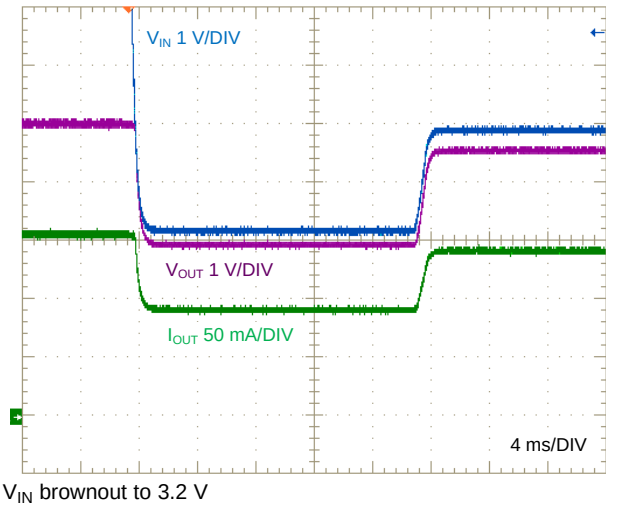


Figure 47. Dropout Performance, 150-mA Resistive Load

Copyright © 2016–2017, Texas Instruments Incorporated

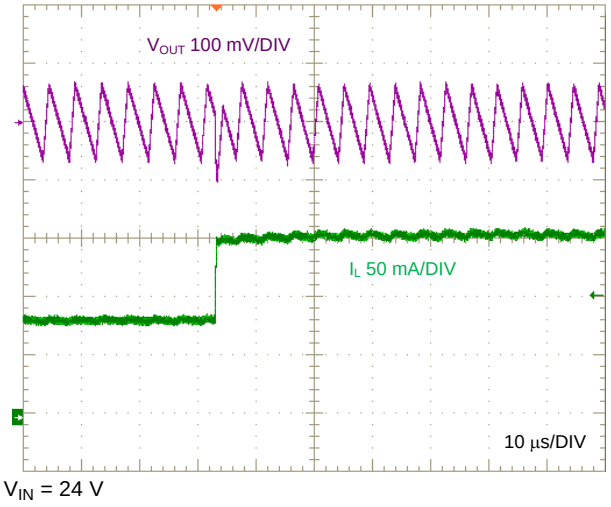


Figure 48. Load Transient, 50 mA to 150 mA, 1 A/µs

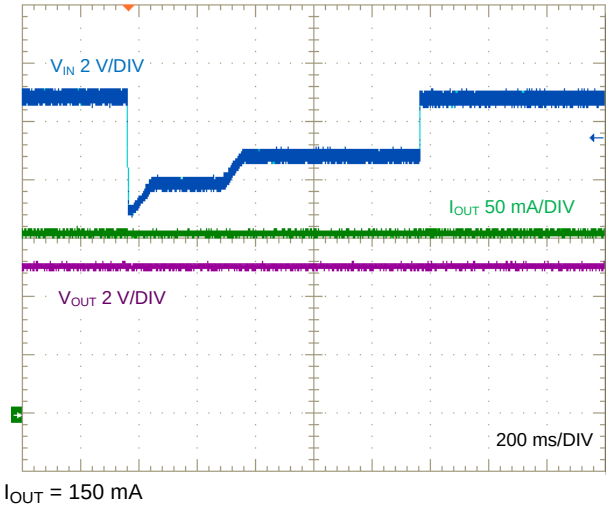


Figure 49. Input Transient (Automotive Cold Crank Profile)

8.2.2 Design 2: Small Solution Size PFM Converter Rated at 3.3 V, 50 mA

The schematic diagram of a 3.3-V, 50-mA PFM converter with minimum component count is given in Figure 50.

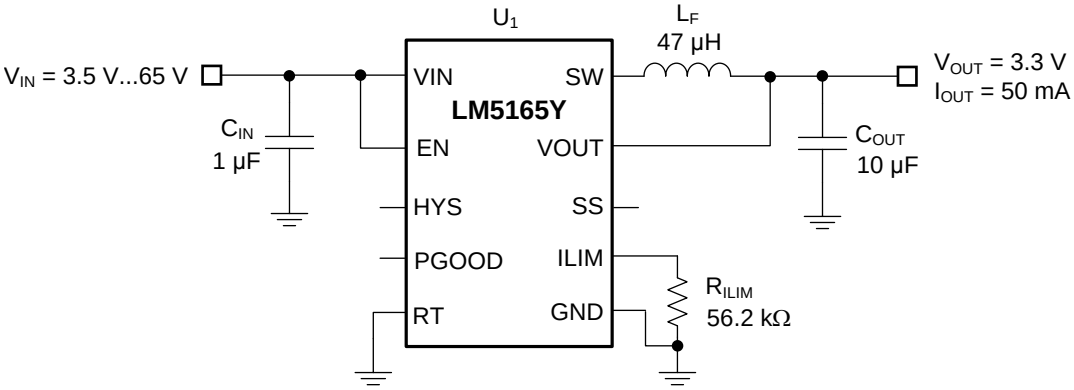


Figure 50. Schematic for Design 2 With $V_{IN(nom)}$ = 12 V, V_{OUT} = 3.3 V, $I_{OUT(max)}$ = 50 mA, $F_{SW(nom)}$ = 350 kHz

8.2.2.1 Design Requirements

The target full-load efficiency of this design is 88% based on a nominal input voltage of 12 V and an output voltage of 3.3 V. The required total input voltage range is 3.5 V to 65 V. The LM5165-Q1 has an internally-set soft-start time of 900 µs and an adjustable peak current limit threshold. The BOM is listed in Table 3.

Table 3. List of Components for Design 2

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7S, 0805 ceramic	TDK	C2012X7S2A474M125AE
C_{OUT}	1	10 µF, 6.3 V, X7R, 0805 ceramic	Taiyo Yuden	JMK212AB7106KG-T
			Murata	GRM21BR70J106KE76K
L_F	1	47 µH ±20%, 0.56 A, 650 mΩ maximum DCR, 3.9 × 3.9 × 1.7 mm	Coilcraft	LPS4018-473MRC
		47 µH ±20%, 0.7 A, 620 mΩ typical DCR, 4.0 × 4.0 × 1.8 mm	Würth	74404042470
		47 µH ±20%, 0.57 A, 650 mΩ typical DCR, 4.0 × 4.0 × 1.8 mm	Taiyo Yuden	NR4018T470M
R_{ILIM}	1	56.2 kΩ, 1%, 0402	Std	Std
U_1	1	LM5165Y-Q1 Synchronous Buck Converter, VSON-10, 3.3-V Fixed	TI	LM5165YQDRCRQ1

Copyright © 2016–2017, Texas Instruments Incorporated

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Peak Current Limit Setting – R_{ILIM}

Install a 56.2-kΩ resistor from ILIM to GND to select a 120-mA peak current limit threshold setting to meet the rated output current of 50 mA.

8.2.2.2.2 Switching Frequency – L_F

Tie RT to GND to select PFM mode of operation. The inductor, input voltage, output voltage, and peak current determine the pulse switching frequency of a PFM-configured LM5165-Q1. For a given input voltage, output voltage and peak current, the inductance of L_F sets the switching frequency when the output is in regulation. Use Equation 19 to select an inductance of 47 µH based on the target PFM converter switching frequency of 350 kHz at 12-V input.

$$L_F = \frac{V_{OUT}}{F_{SW(PFM)} \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{19}$$

$I_{PK(PFM)}$ in this example is the peak current limit setting of 120 mA plus an additional 10% margin added to include the effect of the 100-ns peak current comparator delay. An additional constraint on the inductance is the 180-ns minimum on-time of the high-side MOSFET. Therefore, to keep the inductor current well controlled, choose an inductance that is larger than $L_{F(min)}$ using Equation 20 where $V_{IN(max)}$ is the maximum input supply voltage for the application, $t_{ON(min)}$ is 180 ns, and $I_{L(max)}$ is the maximum allowed peak inductor current.

$$L_{F(min)} = \frac{V_{IN(max)} \cdot t_{ON(min)}}{I_{L(max)}} \tag{20}$$

Choose an inductor with saturation current rating above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

8.2.2.2.3 Output Capacitor – C_{OUT}

The output capacitor, C_{OUT}, filters the inductor's ripple current and stores energy to meet the load current requirement when the LM5165-Q1 is in sleep mode. The output ripple has a base component of amplitude V_{OUT}/123 related to the 10-mV typical feedback comparator hysteresis in PFM. The wakeup time from sleep to active mode adds a ripple voltage component that is a function of the output current. Approximate the total output ripple by Equation 21.

$$\Delta V_{OUT} = \frac{I_{OUT} \cdot 4\mu s}{C_{OUT}} + \frac{V_{OUT}}{123} \tag{21}$$

Also, the output capacitance must be large enough to accept the energy stored in the inductor without a large deviation in output voltage. Setting this voltage change equal to 0.5% of the output voltage results in:

$$C_{OUT} \geq 100 \cdot L_F \cdot \left(\frac{I_{PK(PFM)}}{V_{OUT}}\right)^2 \tag{22}$$

In general, select the capacitance of C_{OUT} to limit the output voltage ripple at full load current, ensuring that it is rated for worst-case RMS ripple current given by $I_{RMS} = I_{PK(PFM)}/2$. In this design example, choose a 10-µF, 6.3-V ceramic output capacitor with X7R dielectric and 0805 footprint.

8.2.2.2.4 Input Capacitor – C_{IN}

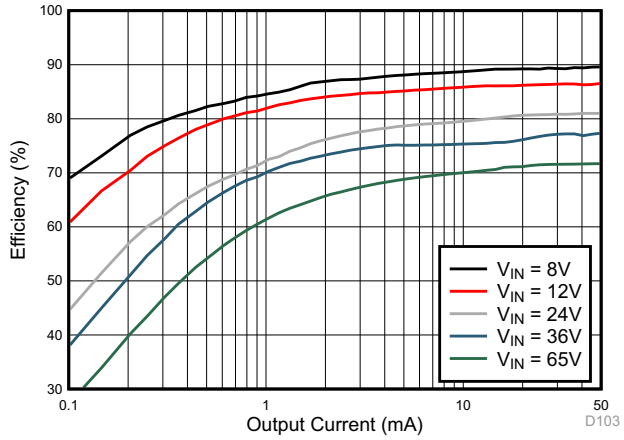
The input capacitor, C_{IN}, filters the high-side MOSFET's triangular current waveform, see Figure 72. To prevent large ripple voltage, use a low-ESR ceramic input capacitor sized for the worst-case RMS ripple current given by $I_{RMS} = I_{OUT}/2$. In this design example, choose a 1-µF, 100-V ceramic input capacitor with X7S dielectric and 0805 footprint.



For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's *Power House* blog series.

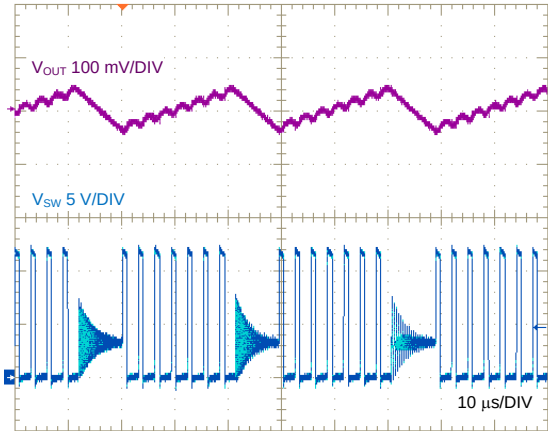
Copyright © 2016–2017, Texas Instruments Incorporated

8.2.2.3 Application Curves



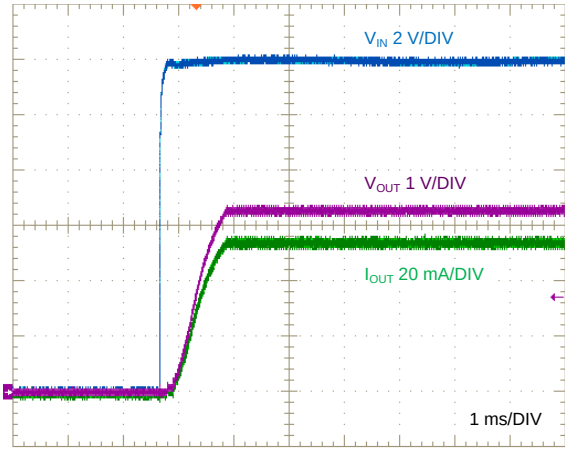
V_{OUT} = 3.3 V

Figure 51. Efficiency



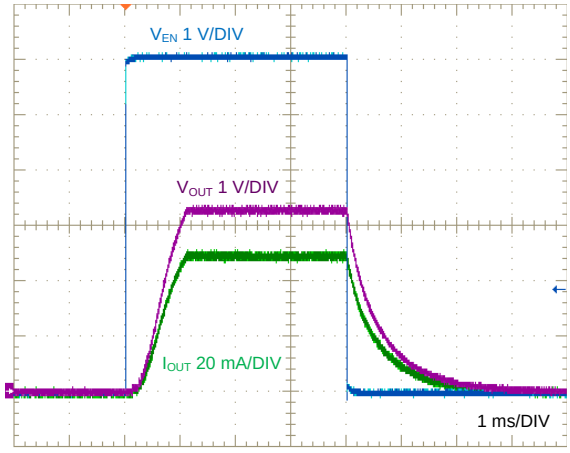
V_{IN} = 12 V I_{OUT} = 50 mA

Figure 52. SW Node and Output Ripple Voltage, Full Load



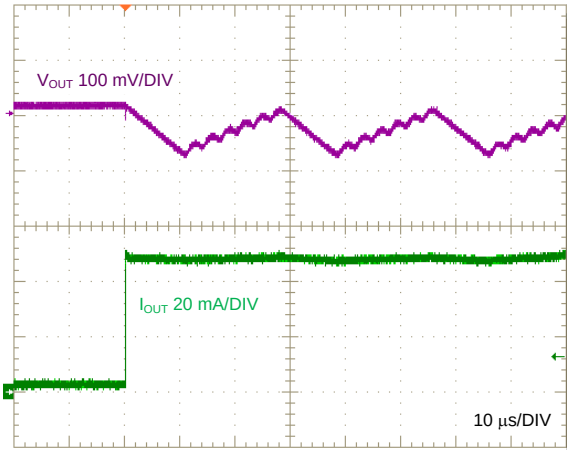
V_{IN} stepped to 12 V 66-Ω Load

Figure 53. Start-Up, Full Load



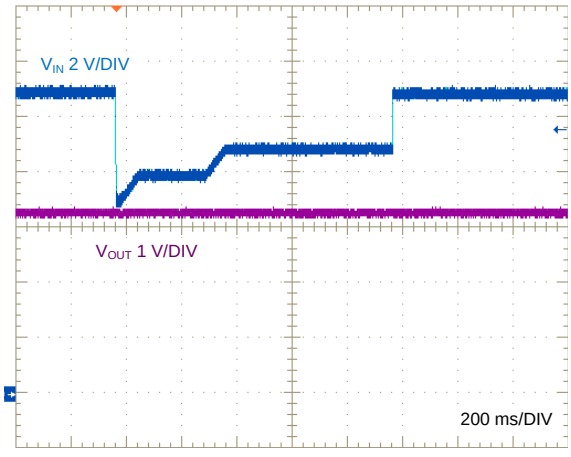
V_{IN} = 12 V 66-Ω Load

Figure 54. Enable ON and OFF



V_{IN} = 12 V

Figure 55. Load Transient, 0 mA to 50 mA, 1 A/µs



I_{OUT} = 50 mA

Figure 56. Input Voltage Transient (Automotive Cold Crank Profile)

Copyright © 2016–2017, Texas Instruments Incorporated

8.2.3 Design 3: High Density 12-V, 75-mA PFM Converter

The schematic diagram of 12-V, 75-mA PFM converter is given in Figure 57.

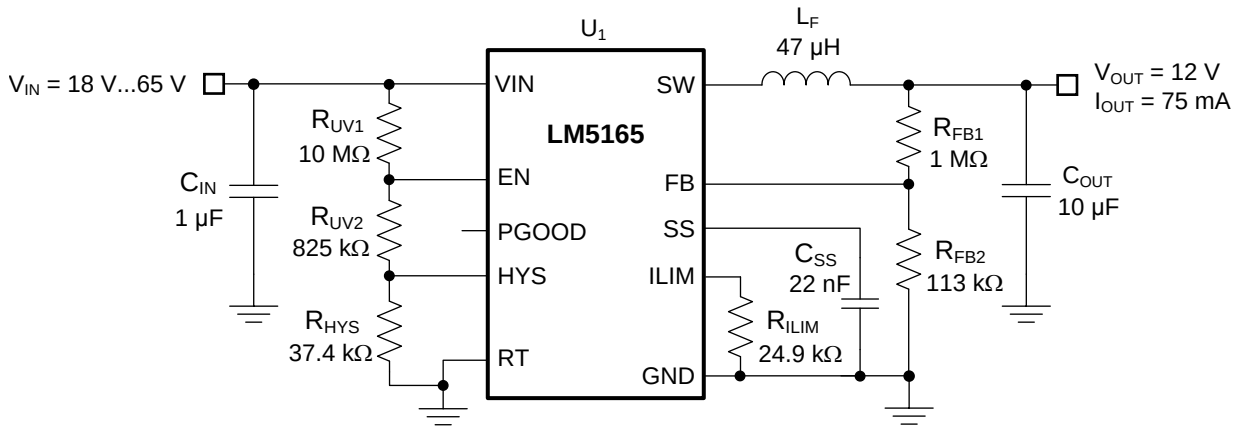


Figure 57. Schematic for Design 3 With $V_{IN(nom)}$ = 24 V, V_{OUT} = 12 V, $I_{OUT(max)}$ = 75 mA, $F_{SW(nom)}$ = 500 kHz

8.2.3.1 Design Requirements

The full-load efficiency specification is 92% based on a nominal input voltage of 24 V and an output voltage of 12 V. The total input voltage range is 18 V to 65 V, with UVLO turnon and turnoff at 16 V and 14.5 V, respectively. The output voltage setpoint is established by feedback resistors, R_{FB1} and R_{FB2}. The switching frequency is set by inductor L_F at 500 kHz at nominal input voltage. The required components are listed in Table 4.

Table 4. List of Components for Design 3

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7S, 0805 ceramic	Murata	GRJ21BC72A105KE11L
		1 µF, 100 V, X7S, 0805 ceramic, AEC-Q200	TDK	CGA4J3X7S2A105K125AE
C_{OUT}	1	10 µF, 16 V, X7R, 0805 ceramic	Taiyo Yuden	EMK212BB7106MG-T
		10 µF, 16 V, X7R, 0805 ceramic, AEC-Q200	TDK	CGA4J1X7S1C106K125AC
L_F	1	47 µH ±20%, 0.56 A, 650 mΩ maximum DCR, 3.9 × 3.9 × 1.7 mm AEC-Q200	Coilcraft	LPS4018-473MRC
R_{ILIM}	1	24.9 kΩ, 1%, 0402	Std	Std
R_{FB1}	1	1 MΩ, 1%, 0402	Std	Std
R_{FB2}	1	113 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	10 MΩ, 1%, 0603	Std	Std
R_{UV2}	1	825 kΩ, 1%, 0402	Std	Std
R_{HYS}	1	37.4 kΩ, 1%, 0402	Std	Std
C_{SS}	1	22 nF, 10 V, X7R, 0402	Std	Std
U_1	1	LM5165-Q1 Synchronous Buck Converter, VSON-10, 3 mm × 3 mm	TI	LM5165QDRCRQ1

8.2.3.2 Detailed Design Procedure

The component selection procedure for this PFM design is quite similar to that of Design 2, see Figure 50.

8.2.3.2.1 Peak Current Limit Setting – R_{ILIM}

Install a 24.9-kΩ resistor from ILIM to GND to select the 180-mA peak current limit setting for a rated output current of 75 mA.

Copyright © 2016–2017, Texas Instruments Incorporated

8.2.3.2.2 Switching Frequency – L_F

Tie RT to GND to select PFM mode of operation. Set the switching frequency by the filter inductance, L_F. Calculate an inductance of 47 µH based on the target PFM converter switching frequency of 500 kHz at 24-V input using Equation 19. Use a peak current limit setting, $I_{PK(PFM)}$, of 180 mA plus an additional 50% margin in this high-frequency design to include the effect of the 100-ns current limit comparator delay. Choose an inductor with saturation current rating well above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

8.2.3.2.3 Input and Output Capacitors – C_{IN}, C_{OUT}

Choose a 1-µF, 100-V ceramic input capacitor with 0805 footprint. Such a capacitor is typically available in X5R or X7S dielectric. Based on Equation 22, select a 10-µF, 16-V ceramic output capacitor with X7R dielectric and 0805 footprint.

8.2.3.2.4 Feedback Resistors – R_{FB1}, R_{FB2}

The output voltage of the LM5165-Q1 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor R_{FB1} and lower feedback resistor R_{FB2}. Select R_{FB1} of 1 MΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 12 V and V_{FB} = 1.223 V, calculate the resistance of R_{FB2} using Equation 5 as 113.5 kΩ. Choose the closest available standard value of 113 kΩ for R_{FB2}. Please refer to *Adjustable Output Voltage (FB)* for more detail.

8.2.3.2.5 Undervoltage Lockout Setpoint – R_{UV1}, R_{UV2}, R_{HYS}

Adjust the undervoltage lockout (UVLO) using an externally-connected resistor divider network of R_{UV1}, R_{UV2}, and R_{HYS}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. The EN rising threshold for the LM5165-Q1 is 1.212 V.

Rearranging Equation 6 and Equation 7, the expressions to calculate R_{UV2} and R_{HYS} are as follows:

$$R_{UV2} = \frac{V_{EN(on)}}{V_{IN(on)} - V_{EN(on)}} \cdot R_{UV1} \tag{23}$$

$$R_{HYS} = \frac{V_{EN(off)}}{V_{IN(off)} - V_{EN(off)}} \cdot R_{UV1} - R_{UV2} \tag{24}$$

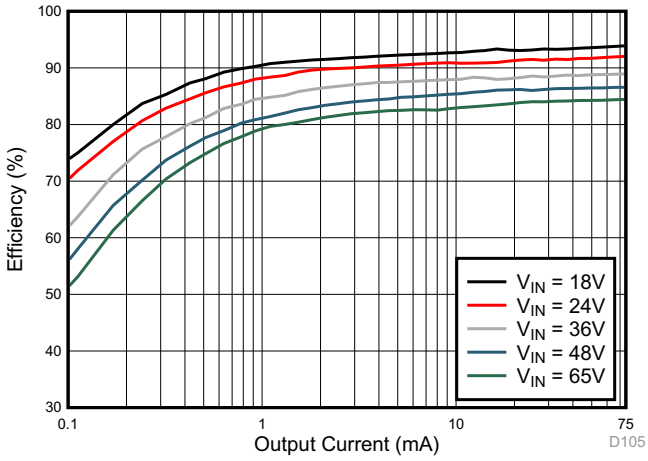
Choose R_{UV1} as 10 MΩ to minimize input quiescent current. Given the desired input voltage UVLO thresholds of 16 V and 14.5 V, calculate the resistance of R_{UV2} and R_{HYS} as 825 kΩ and 37.4 kΩ, respectively. See *Precision Enable (EN) and Hysteresis (HYS)* for more detail.

8.2.3.2.6 Soft Start – C_{SS}

Install a 22-nF capacitor from SS to GND for a soft-start time of 3 ms.

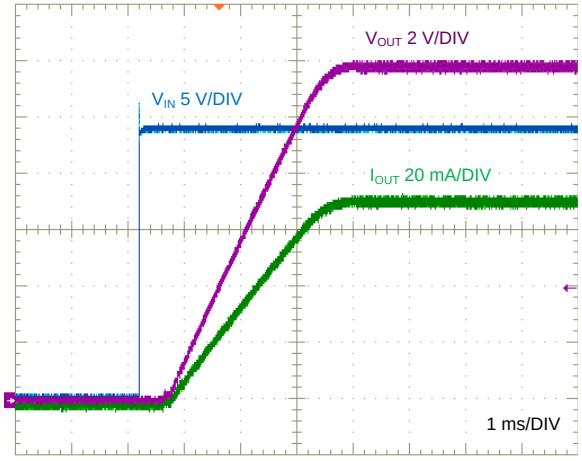
Copyright © 2016–2017, Texas Instruments Incorporated

8.2.3.3 Application Curves



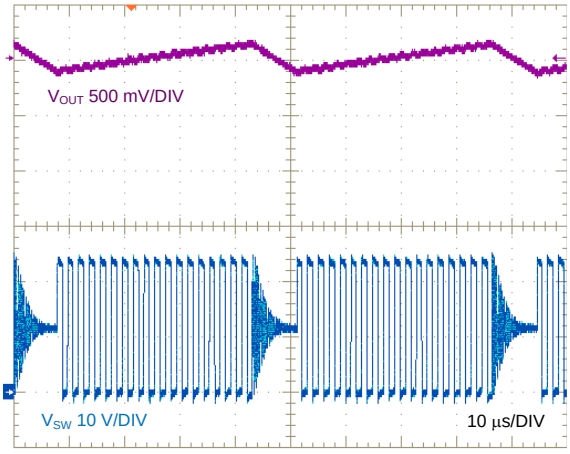
V_{OUT} = 12 V

Figure 58. Efficiency



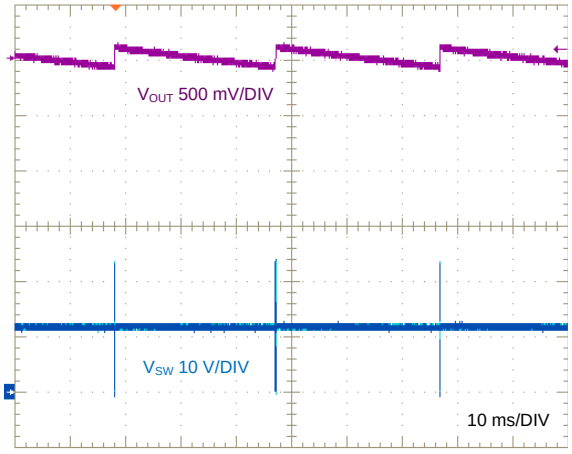
V_{IN} stepped to 24 V 160-Ω Load

Figure 59. Start-Up, Full Load



V_{IN} = 24 V I_{OUT} = 75 mA

Figure 60. SW Node and Output Ripple Voltage, Full Load



V_{IN} = 24 V I_{OUT} = 0 mA

Figure 61. SW Node and Output Ripple Voltage, No Load

Copyright © 2016–2017, Texas Instruments Incorporated

8.2.4 Design 4: 3.3-V, 150-mA COT Converter With High Efficiency

The schematic diagram of a 3.3-V, 150-mA COT converter is given in Figure 62.

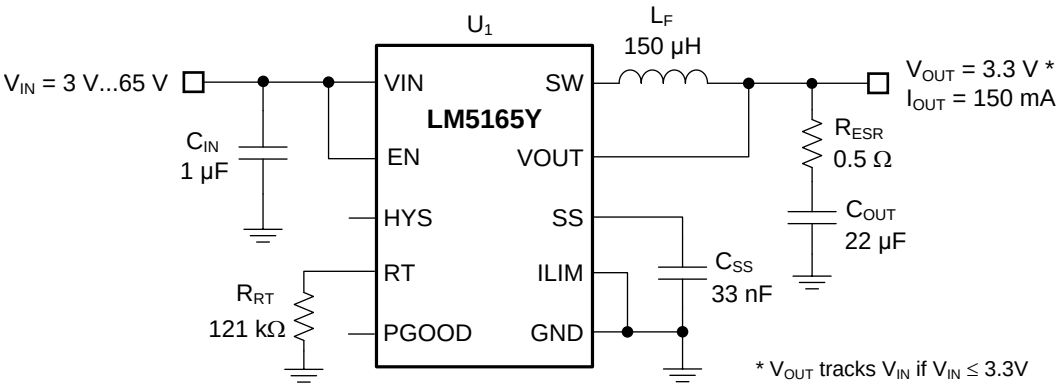


Figure 62. Schematic for Design 4 With $V_{IN(nom)}$ = 24 V, V_{OUT} = 3.3 V, $I_{OUT(max)}$ = 150 mA, $F_{SW(nom)}$ = 160 kHz

8.2.4.1 Design Requirements

The target full-load efficiency is 91% based on a nominal input voltage of 24 V and an output voltage of 3.3 V. The required input voltage range is 3 V to 65 V. The LM5165Y-Q1 is chosen to deliver a fixed 3.3-V output voltage. The switching frequency is set by resistor R_{RT} at approximately 160 kHz. The output voltage soft-start time is 4 ms. The required components are listed in Table 5. The component selection procedure for this COT design is quite similar to that of Design 1, see Figure 37.

Table 5. List of Components for Design 4

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7R, 1206 ceramic	Murata	GRM31CR72A105KA01L
C_{OUT}	1	22 µF, 6.3 V, X7S, 0805 ceramic	Murata	GRM21BR660J226ME39K
L_F	1	150 µH ±20%, 0.29 A, 0.86 Ω typical DCR, 4.8 × 4.8 × 2.9 mm	Coilcraft	LPS5030-154MLC
R_{ESR}	1	0.5 Ω, 5%, 0402	Std	Std
R_{RT}	1	121 kΩ, 1%, 0402	Std	Std
C_{SS}	1	33 nF, 10 V, X7R, 0402 ceramic	Std	Std
U_1	1	LM5165Y-Q1 Synchronous Buck Converter, VSON-10, 3.3-V Fixed	TI	LM5165YQDRCRQ1

8.2.4.2 Application Curves

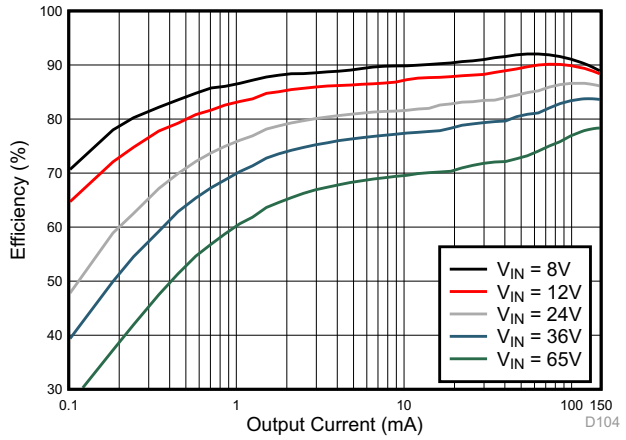


Figure 63. Efficiency

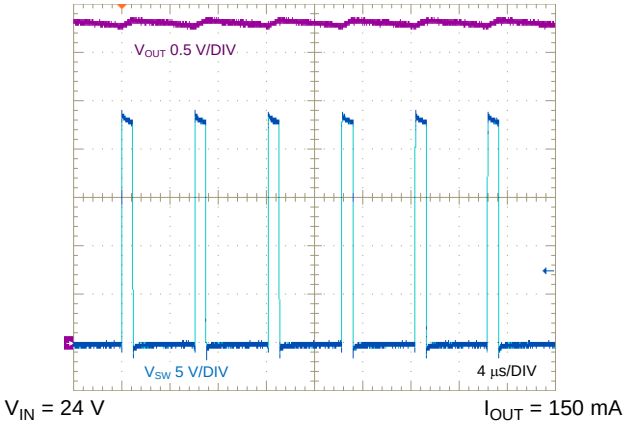


Figure 64. SW Node and Output Ripple Voltages, Full Load

Copyright © 2016–2017, Texas Instruments Incorporated

8.2.5 Design 5: 15-V, 150-mA, 600-kHz COT Converter

The schematic diagram of a 15-V, 150-mA COT converter is given in Figure 65.

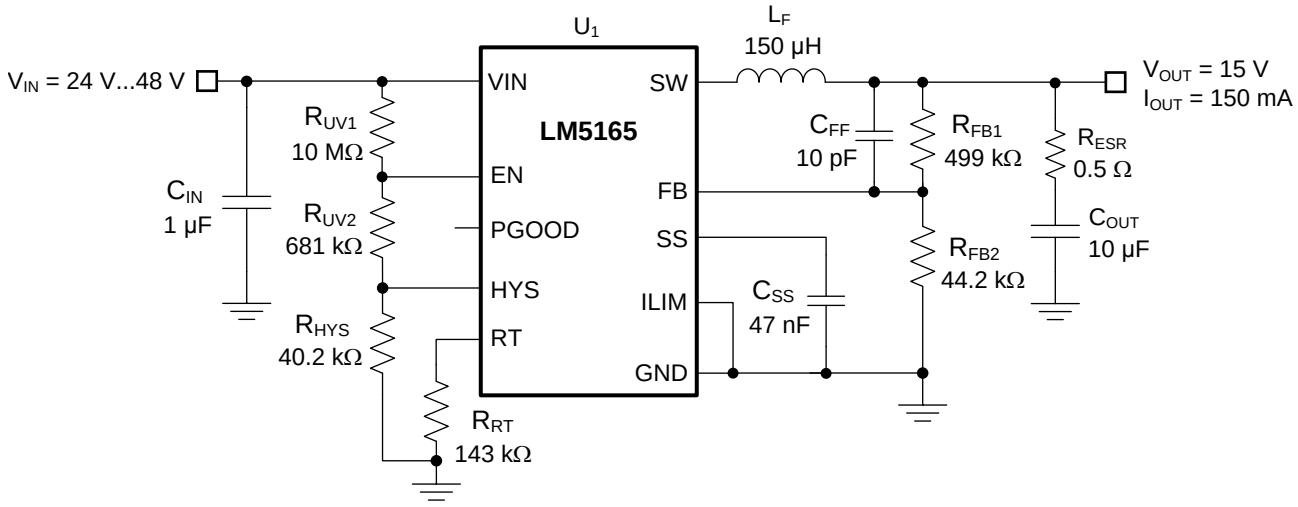


Figure 65. Schematic for Design 5 With $V_{IN(nom)}$ = 36 V, V_{OUT} = 15 V, $I_{OUT(max)}$ = 150 mA, $F_{SW(nom)}$ = 600 kHz

8.2.5.1 Design Requirements

The target full-load efficiency is 92% based on a nominal input voltage of 36 V and an output voltage of 15 V. The input voltage operating range is 24 V to 48 V, but transients as high as 65 V are possible in the application. UVLO turnon and turnoff are set at 19 V and 17 V, respectively. The LM5165-Q1 switching frequency is set at approximately 600 kHz by resistor R_{RT} of 143 kΩ. The output voltage soft-start time is 6 ms. The required components are listed in Table 6. The component selection procedure for this COT design is quite similar to that of Design 1, see Figure 37.

Table 6. List of Components for Design 5

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	1 µF, 100 V, X7R, 1206 ceramic	AVX	12061C105KAT2A
C_{OUT}	1	10 µF, 25 V, X7R, 1206 ceramic	Taiyo Yuden	TMK316B7106KL-TD
L_F	1	150 µH ±20%, 0.29 A, 0.86 Ω typical DCR, 4.8 × 4.8 × 2.9 mm	Coilcraft	LPS5030-154MLC
R_{ESR}	1	2.2 Ω, 5%, 0402	Std	Std
R_{RT}	1	143 kΩ, 1%, 0402	Std	Std
R_{FB1}	1	499 kΩ, 1%, 0402	Std	Std
R_{FB2}	1	44.2 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	10 MΩ, 1%, 0603	Std	Std
R_{UV2}	1	681 kΩ, 1%, 0402	Std	Std
R_{HYS}	1	40.2 kΩ, 1%, 0402	Std	Std
C_{FF}	1	10 pF, 10 V, X7R, 0402 ceramic	Std	Std
C_{SS}	1	47 nF, 10 V, X7R, 0402 ceramic	Std	Std
U_1	1	LM5165-Q1 Synchronous Buck Converter, VSON-10, 3 mm × 3 mm	TI	LM5165QDRCRQ1

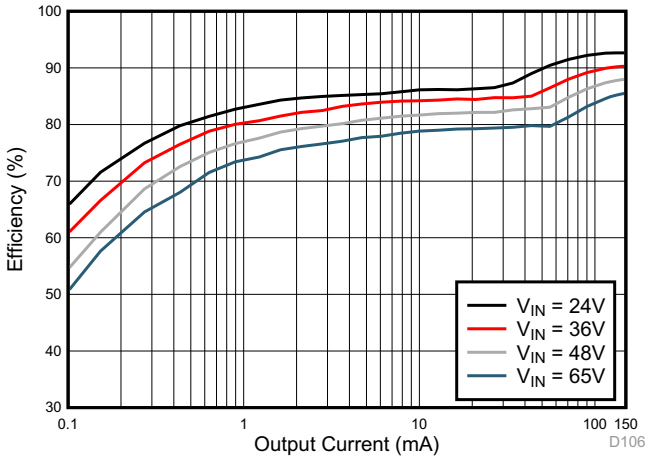
8.2.5.2 Detailed Design Procedure

8.2.5.2.1 COT Output Ripple Voltage Reduction

Depending on the required ripple resistance when operating in COT mode, the resultant output voltage ripple may be deemed too high for a given application. One option is to place a feedforward capacitor C_{FF} in parallel with the upper feedback resistor R_{FB1}. Capacitor C_{FF} increases the high-frequency gain from V_{OUT} to V_{FB} close to unity such that the output voltage ripple couples directly to the FB node.

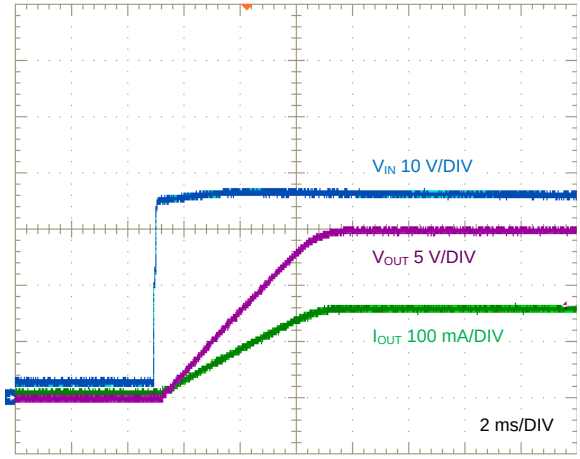
Copyright © 2016–2017, Texas Instruments Incorporated

8.2.5.3 Application Curves



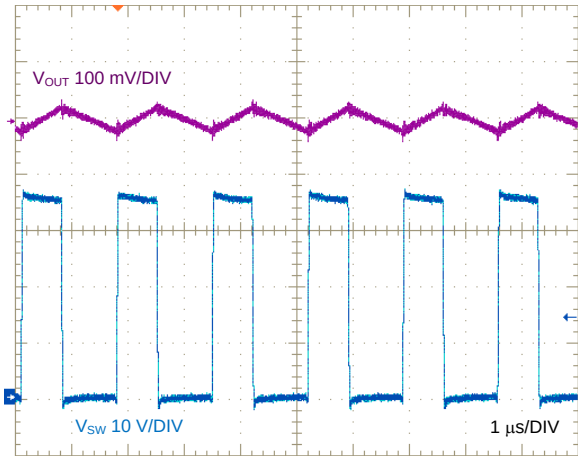
V_{OUT} = 15 V

Figure 66. Efficiency



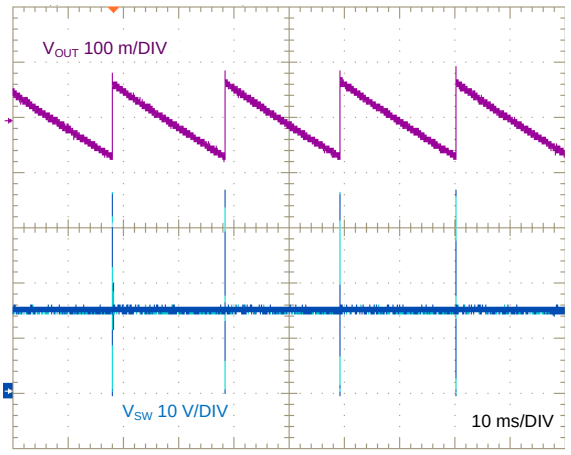
V_{IN} stepped to 36 V I_{OUT} = 150 mA

Figure 67. Start-Up, Full Load



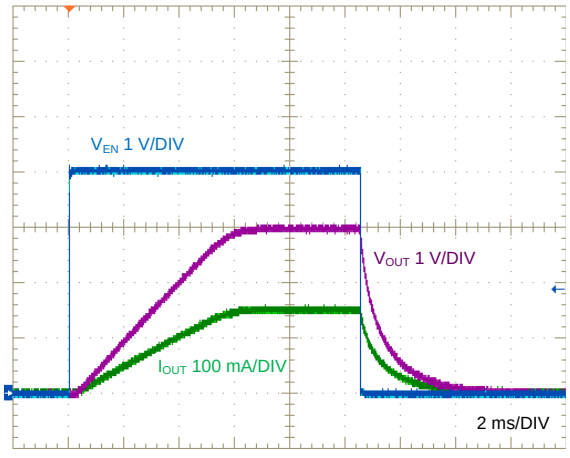
V_{IN} = 36 V I_{OUT} = 150 mA

Figure 68. SW Node and Output Ripple Voltage, Full Load



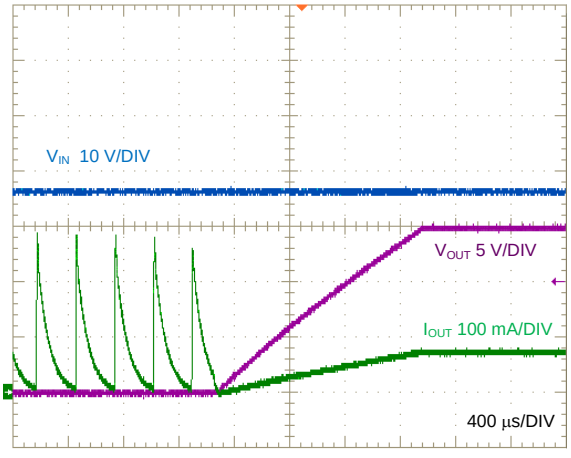
V_{IN} = 36 V I_{OUT} = 0 mA

Figure 69. SW Node and Output Ripple Voltage, No Load



V_{IN} = 36 V

Figure 70. Enable ON and OFF



V_{IN} = 36 V

Figure 71. Short Circuit Recovery

Copyright © 2016–2017, Texas Instruments Incorporated

9 Power Supply Recommendations

The LM5165-Q1 is designed to operate from an input voltage supply range between 3 V and 65 V. This input supply should be able to provide the maximum input current and maintain a voltage above 3 V. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the LM5165-Q1 supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM5165-Q1 converter, additional bulk capacitance may be required in addition to the ceramic input capacitance. A 4.7-μF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

10 Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

PCB layout is a critical for good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply's performance.

1. Bypass the VIN pin to GND with a low-ESR ceramic capacitor of X5R or X7R dielectric. Place C_{IN} as close as possible to the LM5165-Q1 VIN and GND pins. Ground return paths for both the input and output capacitors should consist of localized top-side planes that connect to the GND pin and exposed PAD.
2. Minimize the loop area formed by the input capacitor connections and the VIN and GND pins.
3. Locate the power inductor close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.
4. Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
5. Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
6. Have a single-point ground connection to the plane. Route the ground connections for the feedback, soft-start, and enable components to the ground plane. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
7. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. Minimize trace length to the FB pin. Locate both feedback resistors close to the FB pin. Place C_{FF} (if used) directly in parallel with R_{FB1}. Route the V_{OUT} sense path away from noisy nodes and preferably on a layer at the other side of a shielding layer.
9. Locate the components at RT and SS as close as possible to the device. Route with minimal trace lengths.
10. Provide adequate heatsinking for the LM5165-Q1 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed PAD to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes.

10.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of that path.

The critical switching loop of the power stage in terms of EMI is denoted in Figure 72. The topological architecture of a buck converter means that a particularly high di/dt current effective path exists in the loop comprising the input capacitor and the LM5165-Q1's integrated MOSFETs, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing the effective loop area.

Copyright © 2016–2017, Texas Instruments Incorporated

Layout Guidelines (continued)

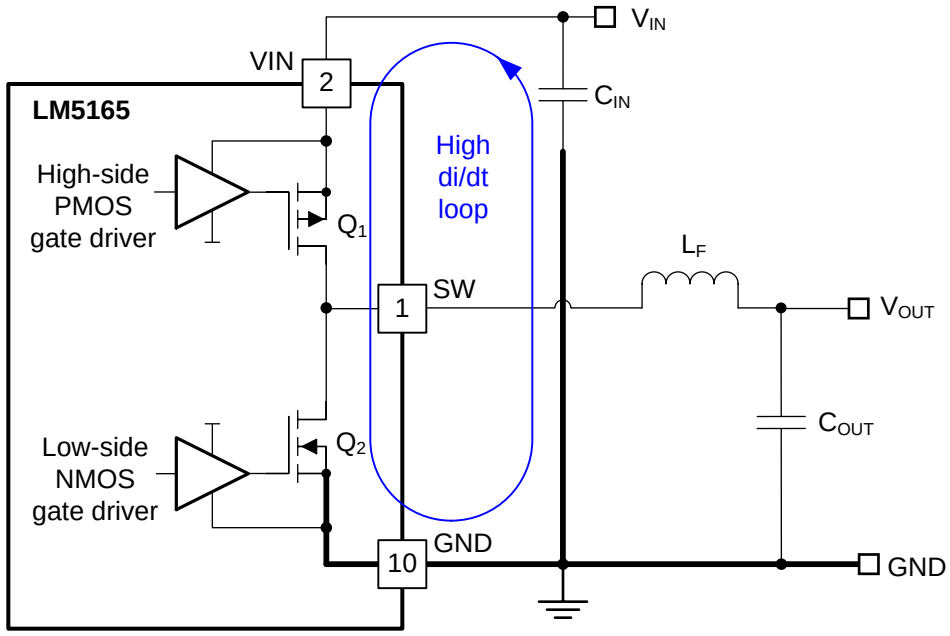


Figure 72. Synchronous Buck Converter With Power Stage Critical Switching Loop

The input capacitor provides the primary path for the high di/dt components of the high-side MOSFET's current. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the V_{OUT} side of the inductor, and connect the capacitor's return terminal to the LM5165-Q1's GND pin and exposed PAD.

10.1.2 Feedback Resistor Layout

For the adjustable output voltage version of the LM5165-Q1, reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the input to the feedback comparator and, as such, is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider away from the SW node path, the inductor and V_{IN} path to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances, greater than 100 kΩ, are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node and V_{IN} path, such that there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This provides further shielding for the voltage feedback path from switching noise sources.

Copyright © 2016–2017, Texas Instruments Incorporated

10.2 Layout Example

Figure 73 shows an example layout for the PCB top layer of a single-sided design. The bottom layer is essentially a full ground plane except for short connecting traces for SW, EN, and PGOOD.

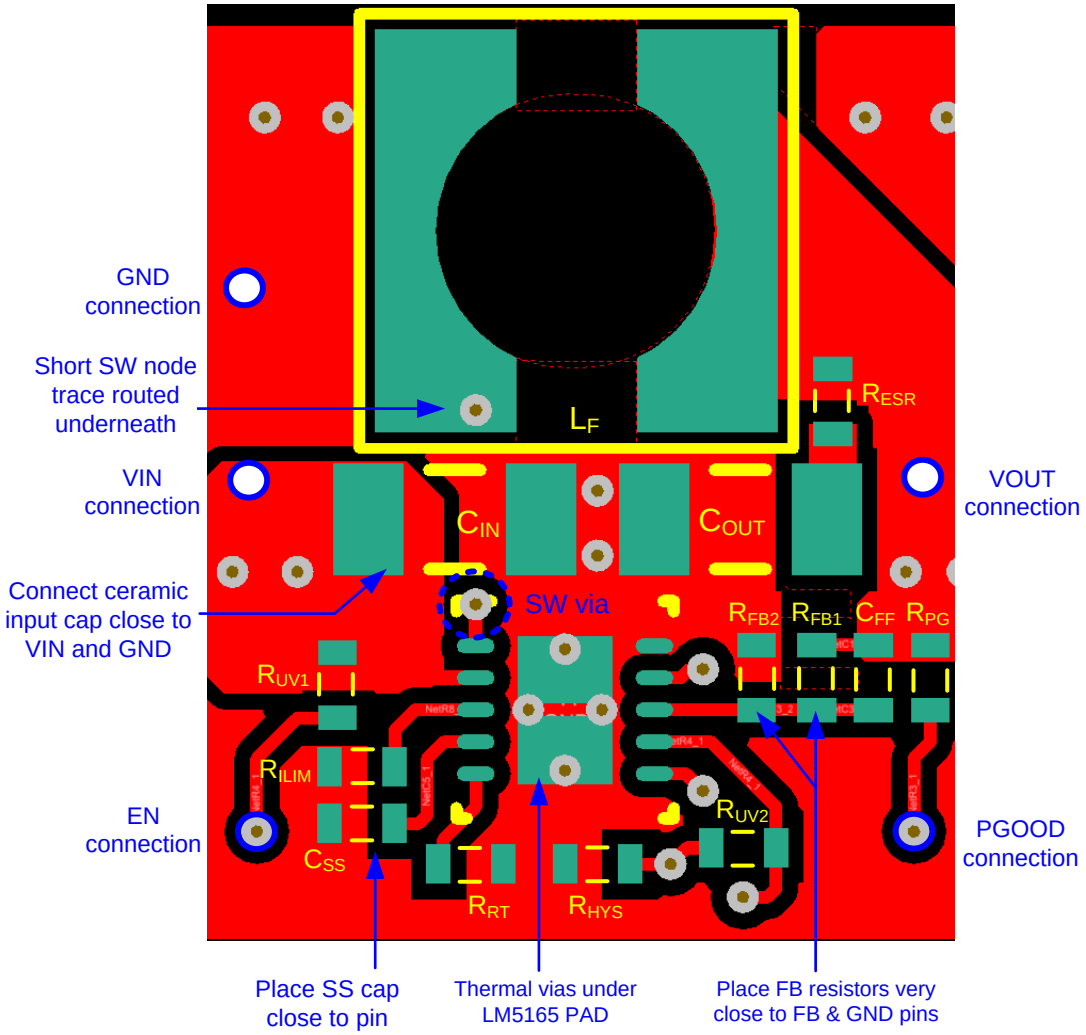


Figure 73. PCB Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 开发支持

相关开发支持，请参见以下文档：

- LM5165-Q1 *快速入门设计工具*
- LM5165-Q1 *仿真模型*
- 如需 TI 的参考设计库，请访问 TIDesigns
- 有关 TI WEBENCH 设计环境，请访问 WEBENCH® 设计中心
- 要查看该产品的相关器件，请参阅 LM5166

11.1.3 使用 WEBENCH® 工具创建定制设计

请单击此处，使用 LM5165-Q1 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *《LM5165EVM-HD-P50A EVM 用户指南》*(SNVU474)
- *《LM5165EVM-HD-C50X EVM 用户指南》*(SNVU511)
- *《LM5166EVM-C50A EVM 用户指南》*(SNVU485)
- *《低 I_Q 同步降压转换器支持智能场传感器 应用》*(SLYT671)
- *《低 EMI 降压转换器为具有 BLE 连接的多变量传感器发送器供电》*(SLYT693)
- TI 参考设计：
  - *具有低功耗 Bluetooth® 连接且由 4 至 20mA 电流回路供电的现场发送器* (TIDUC27)
  - *具有宽输入电压转换器和备用电池且适用于智能恒温器的 24V 交流电源级* (TIDUCE1)
  - *具有宽输入电压转换器和电池量表且适用于智能恒温器的 24V 交流电源级* (TIDUCW0)
- Industrial Strength 博客：
  - *为工业应用中的智能传感器发送器 供电*
  - *楼宇自动化趋势：预测性维护*
  - *楼宇自动化趋势：用于改善用户舒适度的互联传感器*

版权 © 2016–2017, Texas Instruments Incorporated

文档支持 (接下页)

- 白皮书：
  - 《评估适用于具有成本效益的严苛应用的宽 V_{IN}、低 EMI 同步降压 电路》(SLYY104)
- 《为您的 COT 降压转换器选择理想的纹波生成网络》(SNVA776)
- 《AN-2162：轻松解决直流/直流转换器的传导 EMI 问题》(SNVA489)
- 《汽车启动仿真器用户指南》(SLVU984)
- 《使用新的热指标》(SBVA025)
- 《半导体和 IC 封装热指标》(SPRA953)

11.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 7. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
LM5165-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5165QDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165Q	Samples
LM5165QDRCTQ1	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	5165Q	Samples
LM5165XQDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 0	5165XQ	Samples
LM5165XQDRCTQ1	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 0	5165XQ	Samples
LM5165YQDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	0 to 0	5165 YQ	Samples
LM5165YQDGSTQ1	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	0 to 0	5165 YQ	Samples
LM5165YQDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 0	5165YQ	Samples
LM5165YQDRCTQ1	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 0	5165YQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

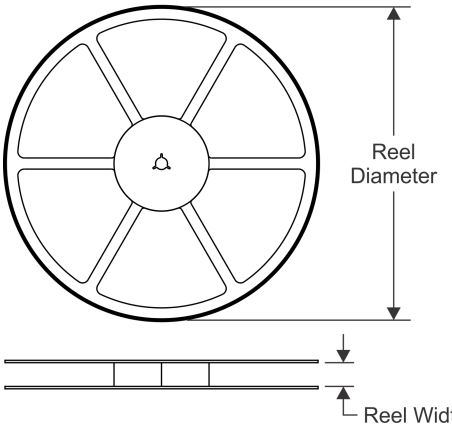
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

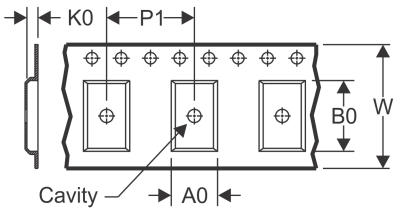
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

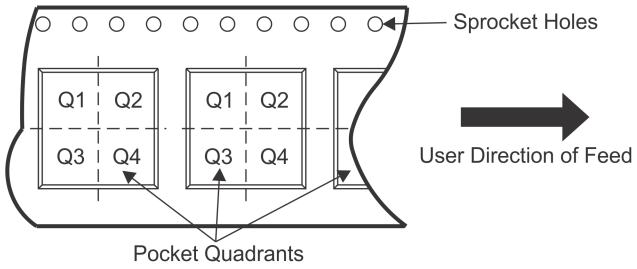


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

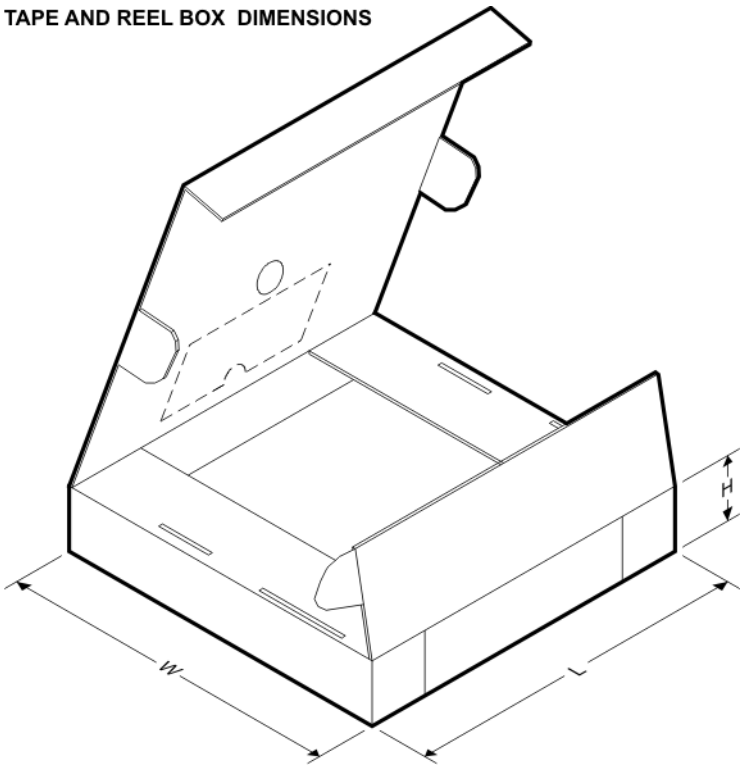
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5165QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165QDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165XQDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165XQDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165YQDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5165YQDGSTQ1	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5165YQDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LM5165YQDRCTQ1	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

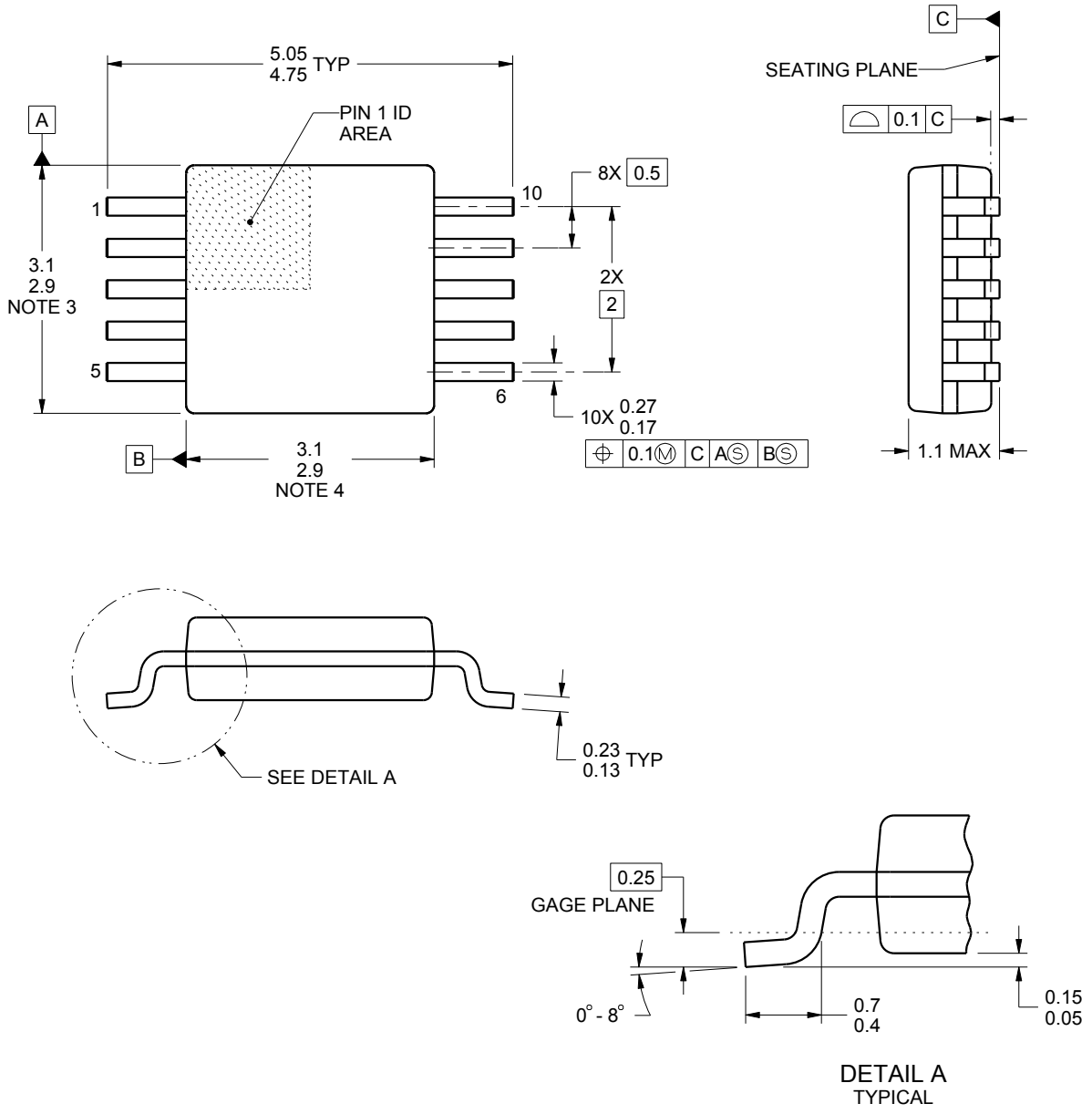
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5165QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
LM5165QDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0
LM5165XQDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
LM5165XQDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0
LM5165YQDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
LM5165YQDGSTQ1	VSSOP	DGS	10	250	366.0	364.0	50.0
LM5165YQDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
LM5165YQDRCTQ1	VSON	DRC	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

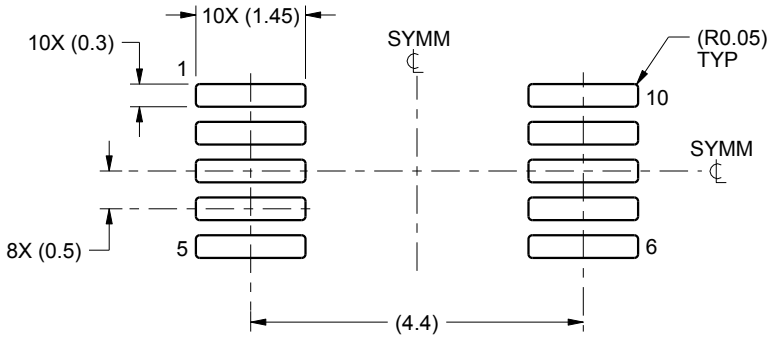
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

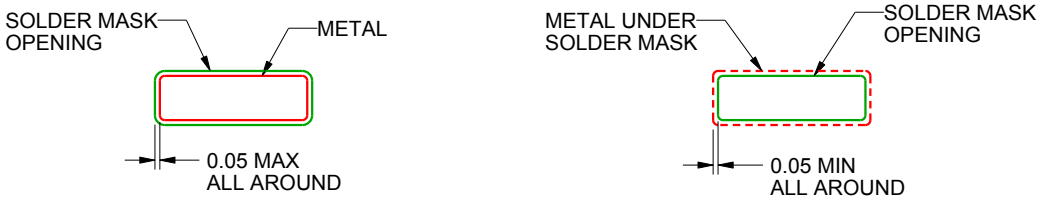


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

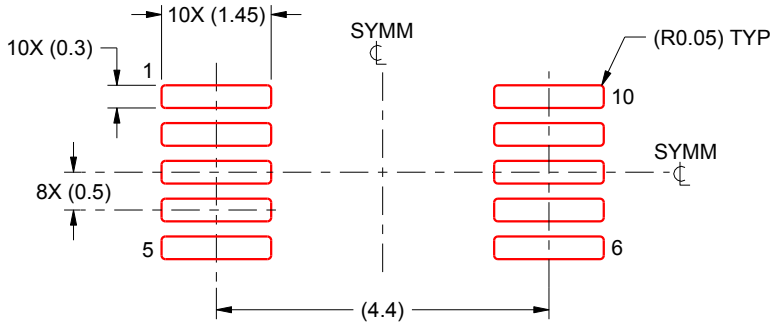


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

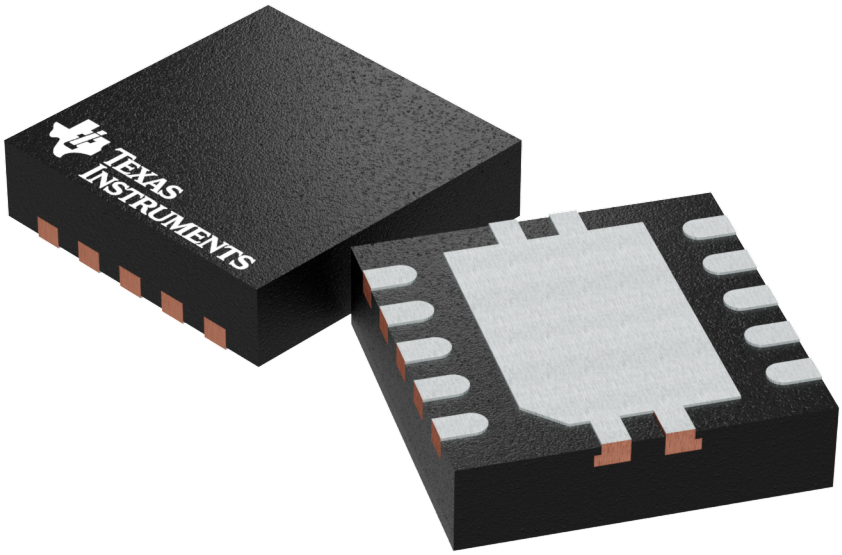
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



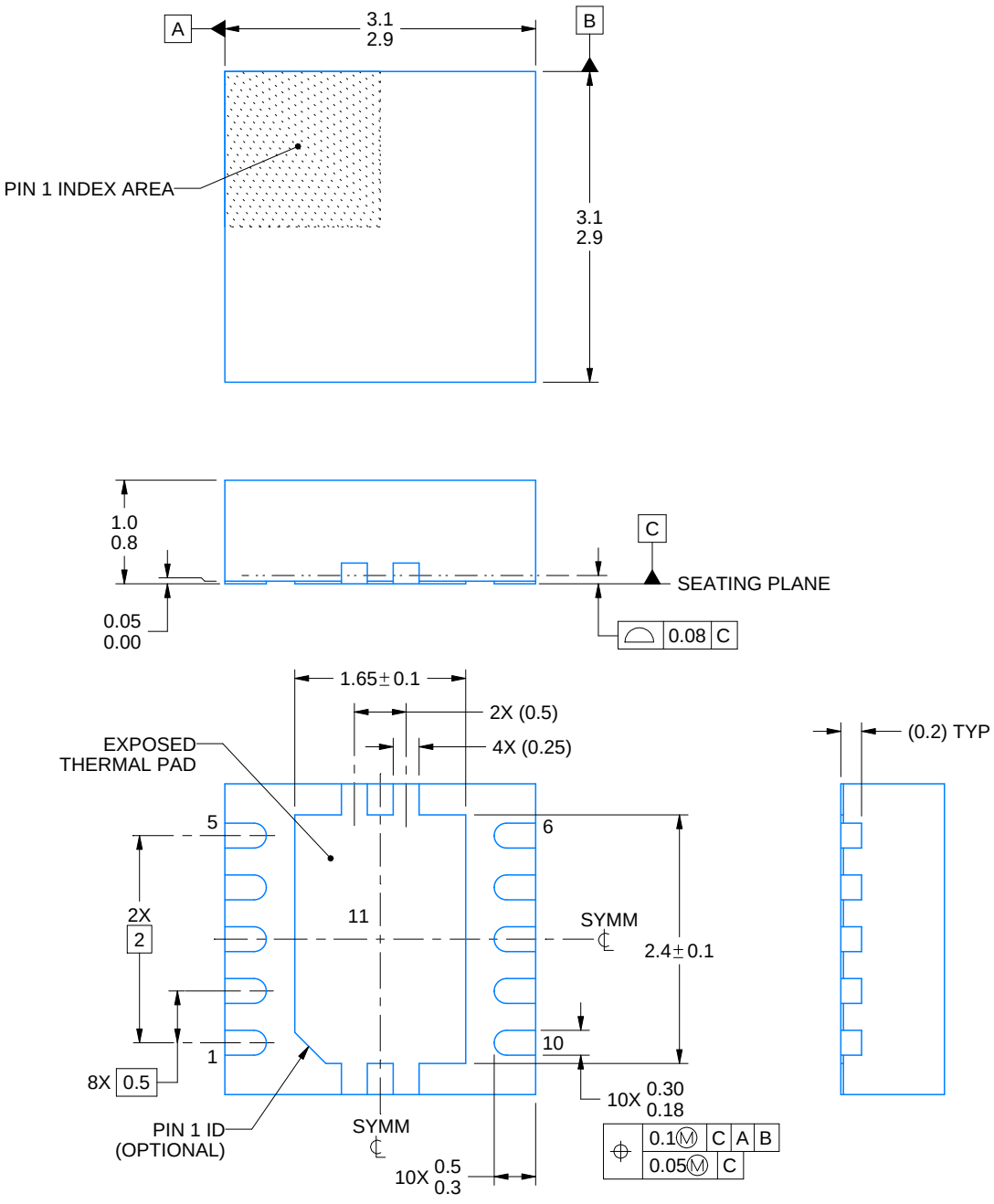
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC0010J

PACKAGE OUTLINE

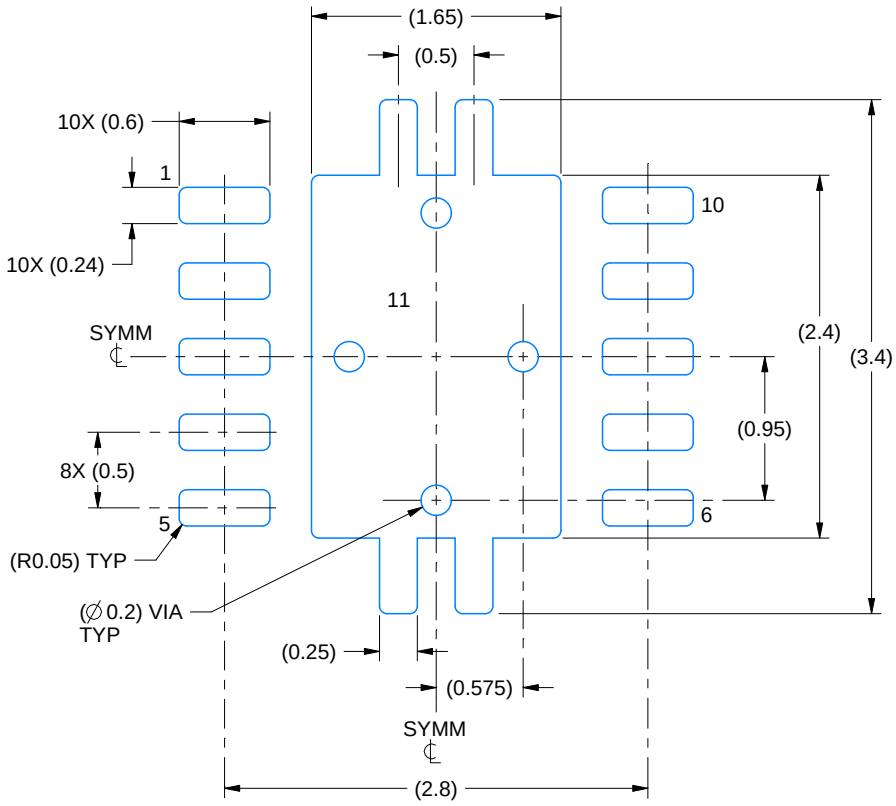
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

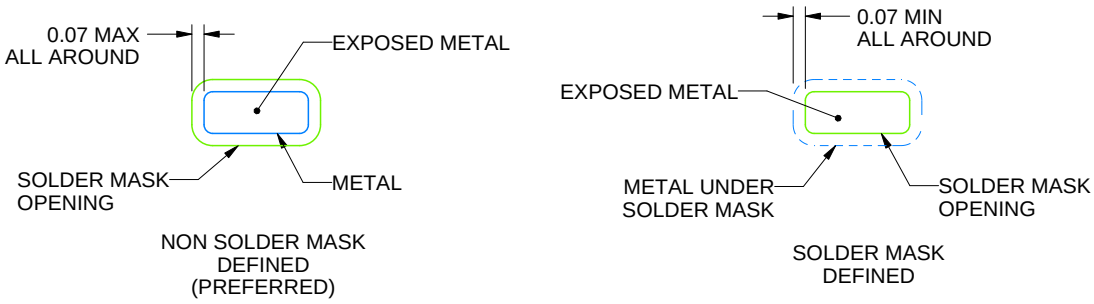


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

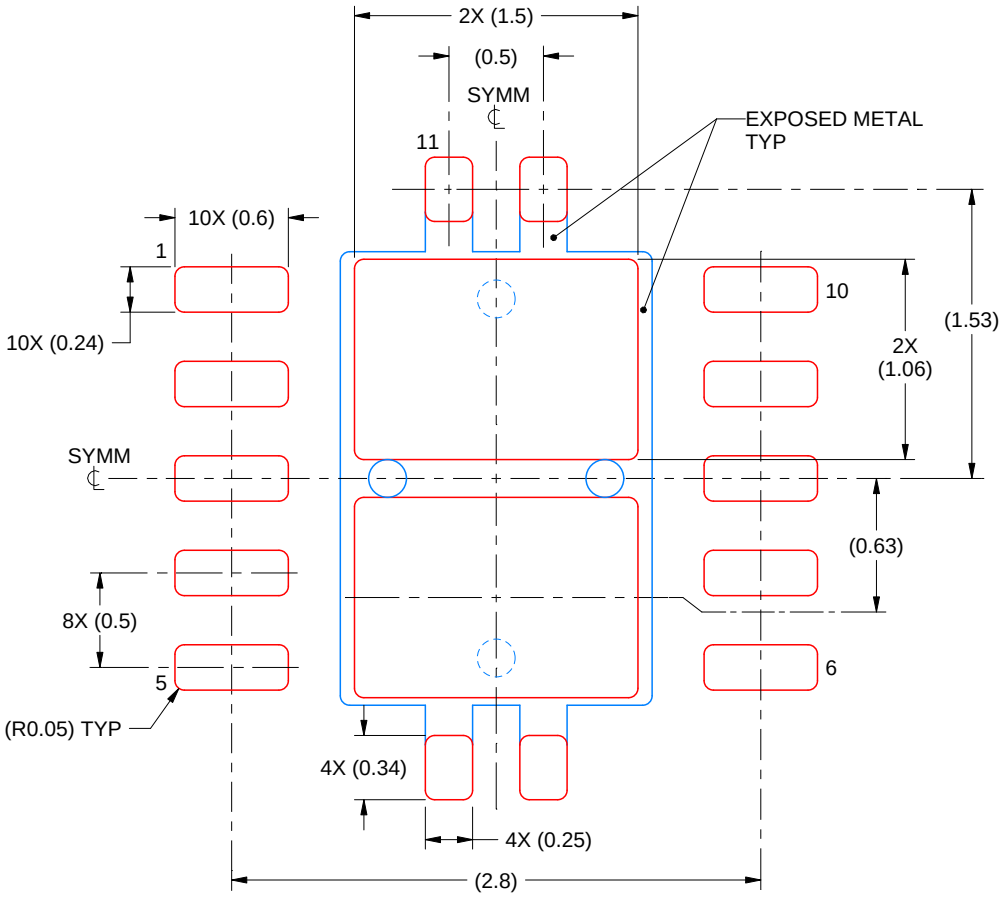
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司