LM5019 100V、100mA 恒定导通时间同步降压稳压器

1 特性

- 宽输入电压范围：7.5V 至 100V
- 集成了 100mA 高侧和低侧开关
- 无需肖特基二极管
- 恒定导通时间控制
- 无需环路补偿
- 超快瞬态响应
- 接近恒定的运行频率
- 智能峰值电流限制
- 可调节输出电压（以 1.225V 为基准电压）
- 2% 的反馈基准电压精度
- 频率可调至 1 MHz
- 可调欠压闭锁
- 远程关断
- 热关断
- 封装：
  - 8 引脚晶圆级小外形无引线 (WSON)
  - 8 引脚小外形尺寸 (SO) PowerPAD
- 使用 LM5019 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 智能电表
- 电信系统
- 汽车电子产品
- 隔离式偏置电源

3 说明

LM5019 是一款 100V、100mA 同步降压稳压器，其集成了高侧和低侧金属氧化物半导体场效应晶体管 (MOSFET)。LM5019 所采用的恒定导通时间 (COT) 控制方案无需环路补偿，可提供出色的瞬态响应，并且可实现超低降压比。导通时间与输入电压成反比，这使得整个输入电压范围内的频率几乎保持恒定。高压启动稳压器为 IC 的内部运行以及集成栅极驱动器提供了偏置电源。

峰值电流限制电路可防止出现过载情况。低压闭锁 (UVLO) 电路支持对输入低压阈值和滞后进行单独编程。其他保护 特性 包括热关断和偏置电源欠压锁定。

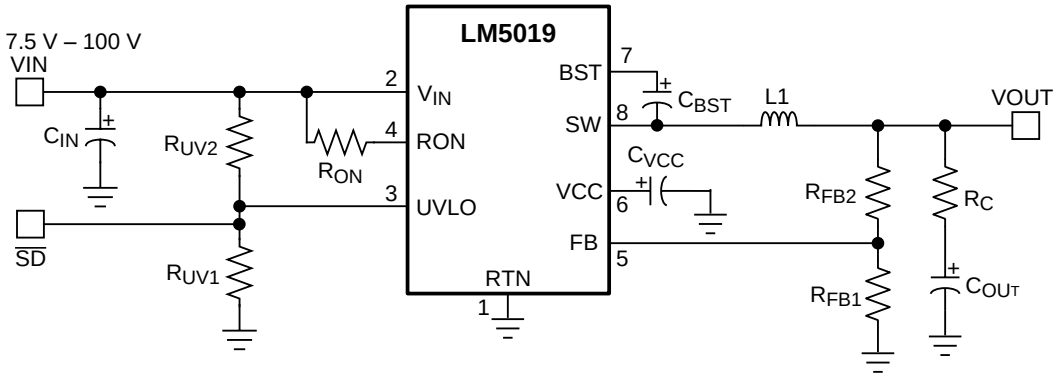
LM5019 器件采用 WSON-8 和 SO PowerPAD-8 塑料封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM5019	SO PowerPAD (8)	4.89mm × 3.90mm
	WSON (8)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 4
6 **Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics ... 7
6.7 Typical Characteristics ... 7
7 **Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 14
8 **Application and Implementation** ... 15
8.1 Application Information ... 15
8.2 Typical Applications ... 15
9 **Power Supply Recommendations** ... 24
10 **Layout** ... 24
10.1 Layout Guidelines ... 24
10.2 Layout Example ... 24
11 器件和文档支持 ... 25
11.1 器件支持 ... 25
11.2 文档支持 ... 25
11.3 接收文档更新通知 ... 25
11.4 社区资源 ... 25
11.5 商标 ... 25
11.6 静电放电警告 ... 25
11.7 Glossary ... 25
12 机械、封装和可订购信息 ... 26

4 修订历史记录

Changes from Revision F (December 2014) to Revision G **Page**

- 向数据表添加了 WEBENCH 链接 ... 1
- Deleted lead temperature from the *Absolute Maximum Ratings* table ... 5
- Changed 14 V to 13 V in V_{CC} *Regulator* section ... 11
- Changed 8 to 4 on equation in *Input Capacitor* section ... 17
- Changed 0.06 µF to 0.12 µF in *Input Capacitor* section ... 18
- 添加了*接收文档更新通知* 部分 ... 25

Changes from Revision E (December 2013) to Revision F **Page**

- 已添加 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分，以及*机械、封装和可订购信息* 部分 ... 1
- Added package designators to pin out drawings. ... 4
- Changed *Thermal Information* table. ... 5
- Added *Timing Requirements* table. ... 7
- Changed *Control Overview* section ... 10
- Changed *Soft-Start Circuit* graphic. ... 14
- Changed *Series Ripple Resistor* R_C section to *Type III Ripple Circuit* ... 17
- Changed *Isolated Fly-Buck Converter* graphic ... 19

Changes from Revision D (December 2013) to Revision E **Page**

- Added Thermal Parameters. ... 5

版权 © 2012–2017, Texas Instruments Incorporated

Changes from Revision C (September 2013) to Revision D **Page**

- 已更改 按照 TI 标准，对文档格式进行了通篇更改 1
- 已更改 将“*特性*”中的*最小工作输入电压从 9V 更改成了 7.5V* 1
- 已更改 *典型应用*中的最低工作输入电压，从 9V 更改为 7.5V..... 1
- Changed minimum operating input voltage from 9 V to 7.5 V in *Pin Descriptions* 4
- Added Maximum Junction Temperature..... 5
- Changed minimum operating input voltage from 9 V to 7.5 V in *Recommended Operating Conditions.* 5

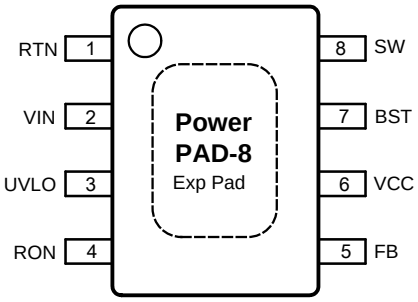
Changes from Revision B (February 2012) to Revision C **Page**

- Added SW to RTN (100 ns transient) in *Absolute Maximum Ratings.* 5

Copyright © 2012–2017, Texas Instruments Incorporated

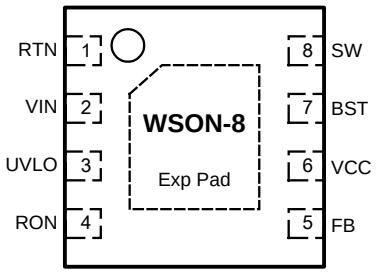
5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Connect Exposed Pad to RTN

NGU Package
8-Pin WSON
Top View



Connect Exposed Pad to RTN

Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	RTN	—	Ground	Ground connection of the integrated circuit.
2	VIN	I	Input Voltage	Operating input range is 7.5 V to 100 V.
3	UVLO	I	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225 V to provide hysteresis. When UVLO pin is pulled below 0.66 V externally, the parts goes in shutdown mode.
4	RON	I	On-Time Control	A resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. Minimum recommended on-time is 100 ns at max input voltage.
5	FB	I	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V.
6	VCC	O	Output From the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V	The internal VCC regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0-μF decoupling capacitor is recommended.
7	BST	I	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01-μF ceramic). The BST pin capacitor is charged by the VCC regulator through an internal diode when the SW pin is low.
8	SW	O	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
—	EP	—	Exposed Pad	Exposed pad must be connected to RTN pin. Connect to system ground plane on application board for reduced thermal resistance.

Copyright © 2012–2017, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
V_{IN}, UVLO to RTN	–0.3	100	V
SW to RTN	–1.5	V_{IN} + 0.3	V
SW to RTN (100-ns transient)	–5	V_{IN} + 0.3	V
BST to VCC		100	V
BST to SW		13	V
RON to RTN	–0.3	100	V
VCC to RTN	–0.3	13	V
FB to RTN	–0.3	5	V
Maximum junction temperature(2)		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For verified specifications and test conditions, see *Electrical Characteristics*. The RTN pin is the GND reference electrically connected to the substrate.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} voltage	7.5	100	V
Operating junction temperature(2)	–40	125	°C

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM5019		UNIT
		NGU (WSON)	DDA (SO PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	41.1	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.2	2.4	°C/W
Ψ_{JB}	Junction-to-board thermal characteristic parameter	19.2	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.1	30.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	34.7	37.3	°C/W
Ψ_{JT}	Junction-to-top thermal characteristic parameter	0.3	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

Copyright © 2012–2017, Texas Instruments Incorporated

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V unless stated otherwise. See(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48 V, I_{CC} = 20 mA	6.25	7.6	8.55	V
	V_{CC} Current Limit	V_{IN} = 48 V(2)	26			mA
	V_{CC} Undervoltage Lockout Voltage (V_{CC} Increasing)		4.15	4.5	4.9	V
	V_{CC} Undervoltage Hysteresis			300		mV
	V_{CC} Drop Out Voltage	V_{IN} = 9 V, I_{CC} = 20 mA		2.3		V
	I_{IN} Operating Current	Non-Switching, FB = 3 V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0 V		50	225	µA
SWITCH CHARACTERISTICS						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200 mA, BST-SW = 7 V		0.8	1.8	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200 mA		0.45	1	Ω
	Gate Drive UVLO	V_{BST} – V_{SW} Rising	2.4	3	3.6	V
	Gate Drive UVLO Hysteresis			260		mV
CURRENT LIMIT						
	Current Limit Threshold	–40°C ≤ T_J ≤ 125°C	150	240	300	mA
	Current Limit Response Time	Time to Switch Off		150		ns
	Off-Time Generator (Test 1)	FB = 0.1 V, V_{IN} = 48 V		12		µs
	Off-Time Generator (Test 2)	FB = 1 V, V_{IN} = 48 V		2.5		µs
REGULATION AND OVERVOLTAGE COMPARATORS						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	1.2	1.225	1.25	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
UNDERVOLTAGE SENSING FUNCTION						
	UV Threshold	UV Rising	1.19	1.225	1.26	V
	UV Hysteresis Input Current	UV = 2.5 V	–10	–20	–29	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	0.32	0.66		V
	Remote Shutdown Hysteresis			110		mV
THERMAL SHUTDOWN						
T_{sd}	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Copyright © 2012–2017, Texas Instruments Incorporated

6.6 Switching Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V unless stated otherwise. See(1).

		MIN	TYP	MAX	UNIT
ON-TIME GENERATOR					
T_{ON} Test 1	V_{IN} = 32 V, R_{ON} = 100 kΩ	270	350	460	ns
T_{ON} Test 2	V_{IN} = 48 V, R_{ON} = 100 kΩ	188	250	336	ns
T_{ON} Test 3	V_{IN} = 75 V, R_{ON} = 100 kΩ	250	370	500	ns
T_{ON} Test 4	V_{IN} = 10 V, R_{ON} = 250 kΩ	1880	3200	4425	ns
MINIMUM OFF-TIME					
Minimum Off-Timer	FB = 0 V		144		ns

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

6.7 Typical Characteristics

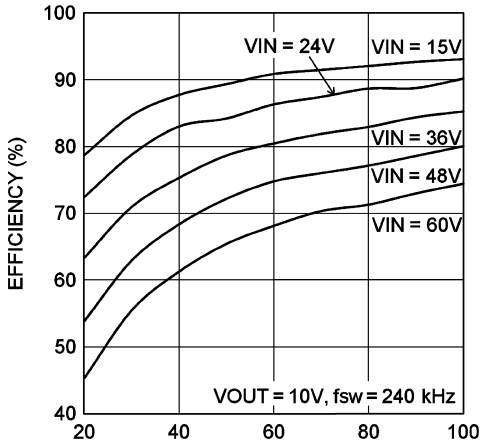


Figure 1. Efficiency at 240 kHz, 10 V

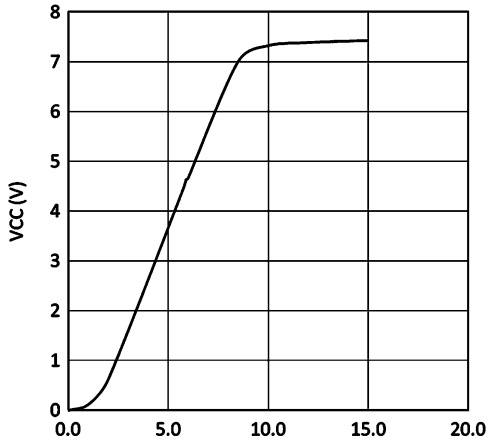


Figure 2. V_{CC} vs V_{IN}

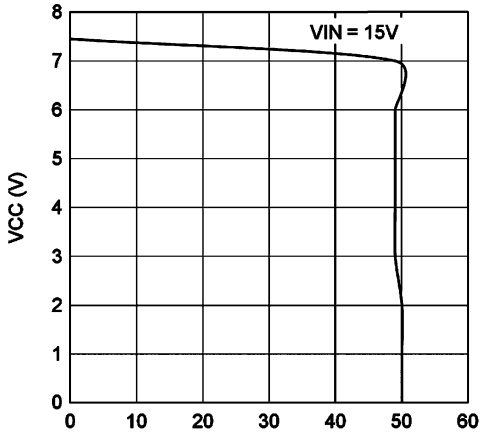


Figure 3. V_{CC} vs I_{CC}

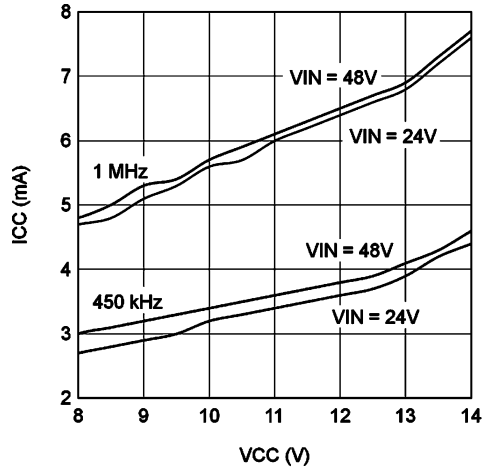


Figure 4. I_{CC} vs External V_{CC}

Copyright © 2012–2017, Texas Instruments Incorporated

Typical Characteristics (continued)

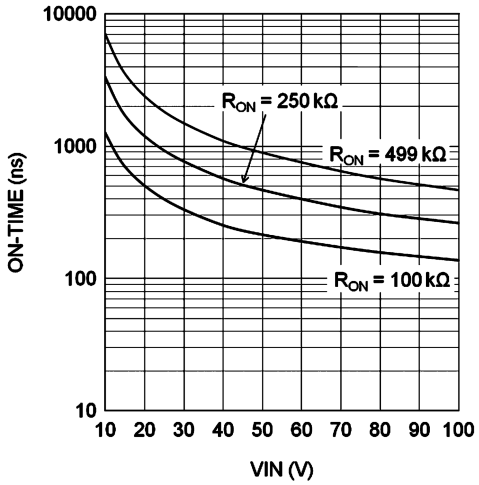


Figure 5. T_{ON} vs V_{IN} and R_{ON}

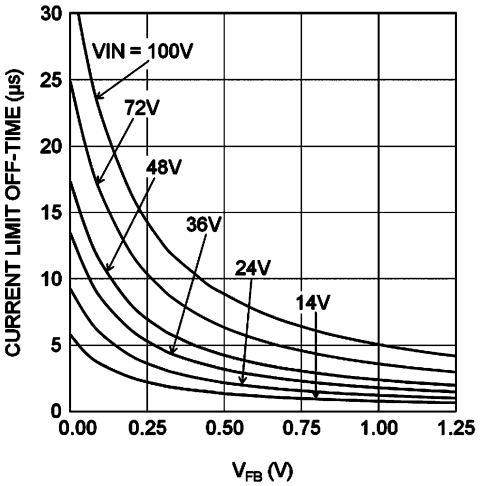


Figure 6. T_{OFF} (I_{LIM}) vs V_{FB} and V_{IN}

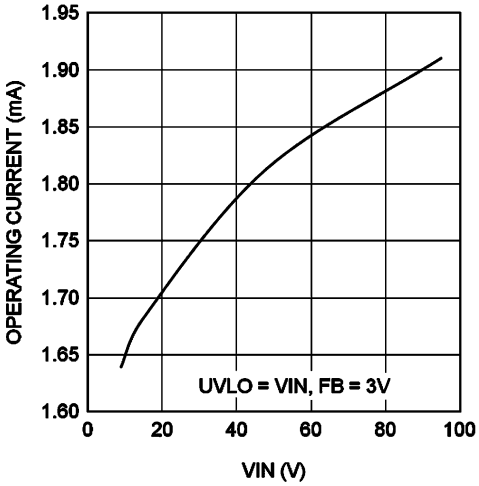


Figure 7. I_{IN} vs V_{IN} (Operating, Non-Switching)

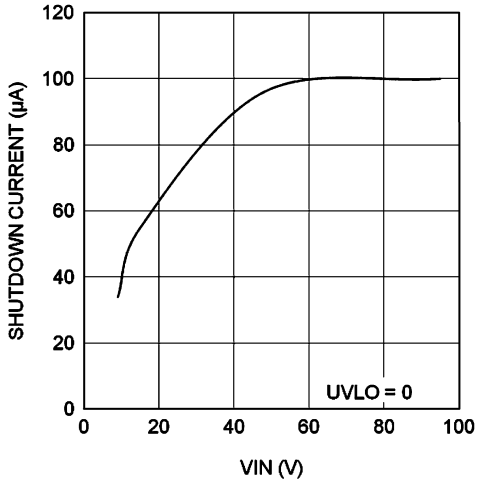


Figure 8. I_{IN} vs V_{IN} (Shutdown)

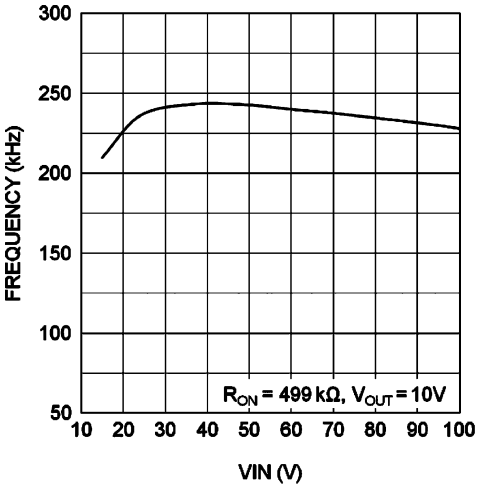


Figure 9. Switching Frequency vs V_{IN}

Copyright © 2012–2017, Texas Instruments Incorporated

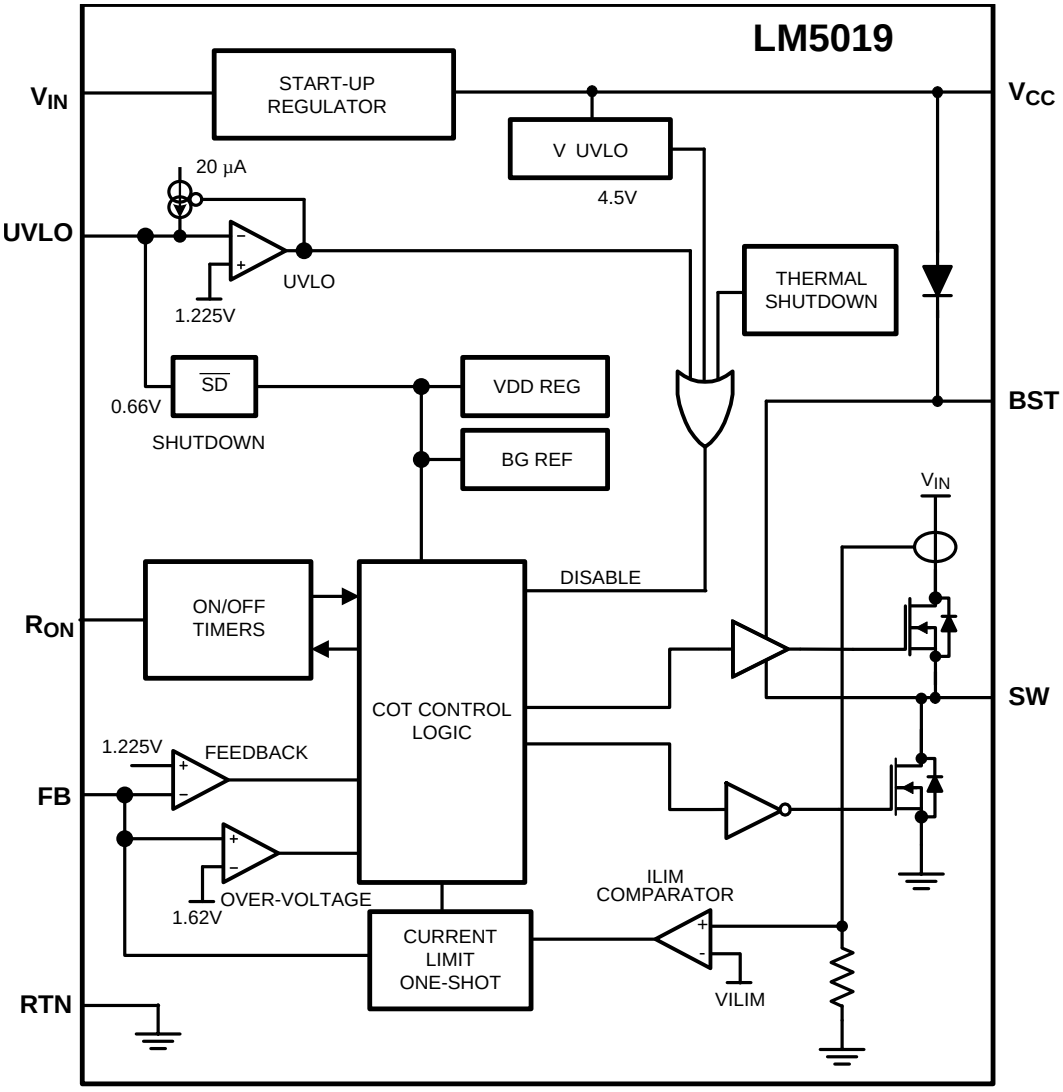
7 Detailed Description

7.1 Overview

The LM5019 step-down switching regulator features all the functions needed to implement a low cost, efficient, buck converter capable of supplying up to 100 mA to the load. This high-voltage regulator contains 100 V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback.

The LM5019 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48 V telecom and automotive power bus ranges. Protection features include: thermal shutdown, undervoltage lockout, minimum forced off-time, and an intelligent current limit.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Overview

The LM5019 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor (R_{ON}). Following the on-time the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer. When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck switch is turned on for another on-time one-shot period. This will continue until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typ).

In a synchronous buck converter, the low side (sync) FET is 'on' when the high side (buck) FET is 'off'. The inductor current ramps up when the high side switch is 'on' and ramps down when the high side switch is 'off'. There is no diode emulation feature in this IC, and therefore, the inductor current may ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as shown in Equation 1.

$$f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}} \quad (1)$$

Where $K = 9 \times 10^{-11}$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated as shown in Equation 2.

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT} - 1.225V}{1.225V} \quad (2)$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM5019. In cases where the capacitor ESR is too small, additional series resistance may be required (R_C in Figure 10).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in Figure 10. However, R_C slightly degrades the load regulation.

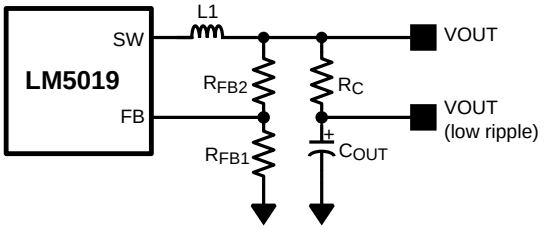


Figure 10. Low Ripple Output Configuration

7.3.2 V_{CC} Regulator

The LM5019 contains an internal high-voltage linear regulator with a nominal output of 7.6 V. The input pin (V_{IN}) can be connected directly to the line voltages up to 100 V. The V_{CC} regulator is internally current limited to 30 mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the undervoltage lockout threshold of 4.5 V, the IC is enabled.

The V_{CC} regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

Copyright © 2012–2017, Texas Instruments Incorporated

Feature Description (continued)

At high input voltages, the power dissipated in the high voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the V_{CC} regulator may supply up to 7 mA of current resulting in 48 V × 7 mA = 336 mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source, between 8.55 V and 13 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225-V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high side switch will stay on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high side switch will stay off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage will be below 1.225 V at the end of each on-time, causing the high side switch to turn on immediately after the minimum forced off-time of 144 ns. The high side switch can be turned off before the on-time is over if the peak current in the inductor reaches the current limit threshold.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62 V reference. If the voltage at FB rises above 1.62 V the on-time pulse is immediately terminated. This condition can occur if the input voltage and/or the output load changes suddenly. The high side switch will not turn on again until the voltage at FB falls below 1.225 V.

7.3.5 On-Time Generator

The on-time for the LM5019 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the LM5019 is shown in Equation 3.

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \tag{3}$$

See Figure 5. R_{ON} should be selected for a minimum on-time (at maximum V_{IN}) greater than 100 ns, for proper operation. This requirement limits the maximum switching frequency for high V_{IN}.

7.3.6 Current Limit

The LM5019 contains an intelligent current limit off-timer. If the current in the buck switch exceeds 240 mA, the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0 V and V_{IN} = 48 V, the maximum off-time is set to 16 μs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 100 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from the following equation:

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2\ V}\ \mu s \tag{4}$$

The current limit protection feature is peak limited. The maximum average output will be less than the peak.

7.3.7 N-Channel Buck Switch and Driver

The LM5019 integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01-uF ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

Copyright © 2012–2017, Texas Instruments Incorporated

Feature Description (continued)

7.3.8 Synchronous Rectifier

The LM5019 provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

7.3.9 Undervoltage Detector

The LM5019 contains a dual level Undervoltage Lockout (UVLO) circuit. When the UVLO pin voltage is below 0.66 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the controller is in standby mode. In standby mode the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage threshold and the UVLO pin voltage is greater than 1.225 V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20-μA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

If the UVLO pin is wired directly to the V_{IN} pin, the regulator will begin operation once the V_{CC} undervoltage is satisfied.

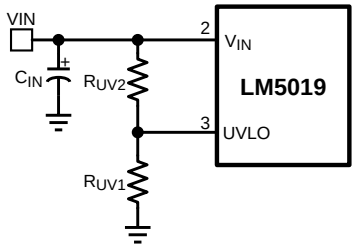


Figure 11. UVLO Resistor Setting

7.3.10 Thermal Protection

The LM5019 should be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM5019 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

7.3.11 Ripple Configuration

LM5019 uses Constant-On-Time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

Table 1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

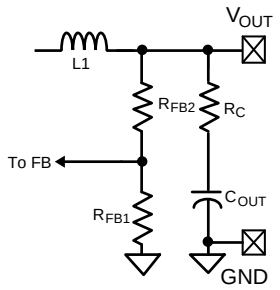
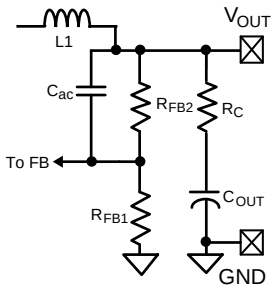
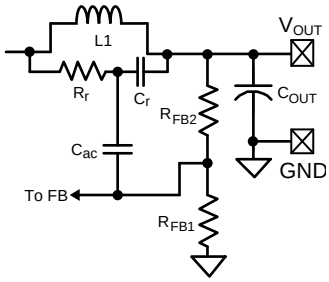
Copyright © 2012–2017, Texas Instruments Incorporated

Feature Description (continued)

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166) for more details for each ripple generation method.

Table 1. Ripple Configuration

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
		
$R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$	$C \geq \frac{5}{f_{sw}(R_{FB2} \| R_{FB1})}$ $R_C \geq \frac{25\ mV}{\Delta I_{L(MIN)}}$	$C_r = 3300\ pF$ $C_{ac} = 100\ nF$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\ mV}$

7.3.12 Soft-Start

A soft-start feature can be implemented with the LM5019 using an external circuit. As shown in Figure 12, the soft-start circuit consists of one capacitor, C_1, two resistors, R_1 and R_2, and a diode, D. During the initial start-up, the VCC voltage is established prior to the V_{OUT} voltage. Capacitor C_1 is discharged and D is thereby forward biased. The FB voltage exceeds the reference voltage (1.225 V) and switching is therefore disabled. As capacitor C_1 charges, the voltage at node B gradually decreases and switching commences. V_{OUT} will gradually rise to maintain the FB voltage at the reference voltage. Once the voltage at node B is less than a diode drop above the FB voltage, the soft-start sequence is finished and D is reverse biased.

During the initial part of the start-up, the FB voltage can be approximated as follows. Please note that the effect of R_1 has been ignored to simplify the calculation shown in Equation 5.

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \quad (5)$$

C1 is charged after the first start up. Diode D1 is optional and can be added to discharge C1 and initialize the soft-start sequence when the input voltage experiences a momentary drop.

Copyright © 2012–2017, Texas Instruments Incorporated

To achieve the desired soft-start, the following design guidance is recommended:

1. R_2 is selected so that V_{FB} is higher than 1.225 V for a V_{CC} of 4.5 V, but is lower than 5 V when V_{CC} is 8.55 V. If an external V_{CC} is used, V_{FB} should not exceed 5 V at maximum V_{CC}.
2. C_1 is selected to achieve the desired start-up time that can be determined as shown in Equation 6.

$$t_S = C_1 \times \left(R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}}\right) \quad (6)$$

3. R_1 is used to maintain the node B voltage at zero after the soft-start is finished. A value larger than the feedback resistor divider is preferred.

With component values from the applications from the schematic shown in Figure 13, selecting C_1 = 1 µF, R_2 = 1 kΩ, R_1 = 30 kΩ results in a soft-start time of about 2 ms.

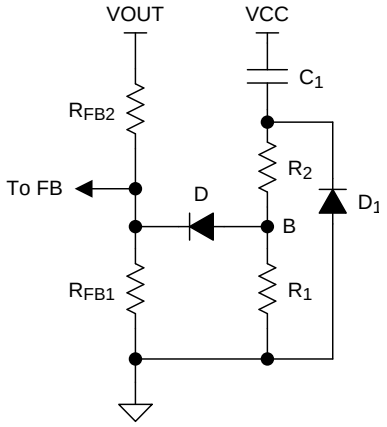


Figure 12. Soft-Start Circuit

7.4 Device Functional Modes

The UVLO pin controls the operating mode of the LM5019 device (see Table 2 for the detailed functional states).

Table 2. UVLO Mode

UVLO	V_{CC}	MODE	DESCRIPTION
< 0.66 V	Disabled	Shutdown	V_{CC} regulator disabled. Switching disabled.
0.66 V to 1.225 V	Enabled	Standby	V_{CC} regulator enabled Switching disabled.
> 1.225 V	V_{CC} < 4.5 V	Standby	V_{CC} regulator enabled. Switching disabled.
	V_{CC} > 4.5 V	Operating	V_{CC} enabled. Switching enabled.

Copyright © 2012–2017, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5019 device is step-down DC-DC converter. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 100 mA. Use the following design procedure to select component values for the LM5019 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

8.2.1 Application Circuit: 12.5 V to 95 V Input and 10 V, 100-mA Output Buck Converter

The application schematic of a buck supply is shown in Figure 13. For output voltage (V_{OUT}) more than one diode drop higher than the maximum regulation threshold of V_{CC} (8.55 V, see *Electrical Characteristics*), the V_{CC} pin can be connected to V_{OUT} through a diode (D2), to improve efficiency and reduce power dissipation in the IC.

The design example uses equations from the *Feature Description* section with component names provided in the *典型应用* schematic. Corresponding component designators from Figure 13 are also provided for each selected value.

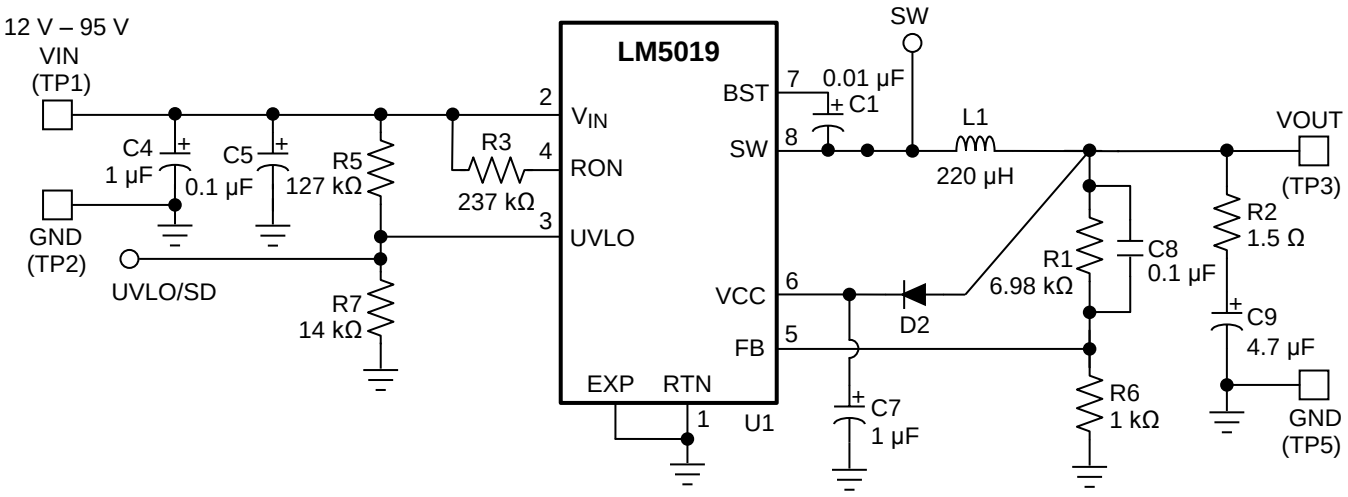


Figure 13. 12.5-V to 95-V Input and 10-V, 100-mA Output Buck Converter

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 3 lists the design parameters for this example.

Table 3. Buck Converter Design Specifications

DESIGN PARAMETERS	VALUE
Input Range	12.5 V to 95 V, transients up to 100 V
Output Voltage	10 V
Maximum Output Current	100 mA
Nominal Switching Frequency	≈ 440 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5019 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 RFB1, RFB2

$V_{OUT} = V_{FB} \times (R_{FB2} / R_{FB1} + 1)$, and since V_{FB} = 1.225 V, the ratio of R_{FB2} to R_{FB1} calculates to be 7:1. Standard values are chosen with R_{FB2} = R1 = 6.98 kΩ and R_{FB1} = R6 = 1.00 kΩ are chosen. Other values could be used as long as the 7:1 ratio is maintained.

8.2.1.2.3 Frequency Selection

At the minimum input voltage, the maximum switching frequency of LM5019 is restricted by the forced minimum off-time ($T_{OFF(MIN)}$) as given by Equation 7.

$$f_{SW(MAX)} = \frac{1 - D_{MIN}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200\ ns} = 1\ MHz \tag{7}$$

Similarly, at maximum input voltage, the maximum switching frequency of LM5019 is restricted by the minimum T_{ON} as given by Equation 8.

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/48}{100\ ns} = 2.1\,MHz \tag{8}$$

Resistor R_{ON} sets the nominal switching frequency based on Equation 9.

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}}$$

where

- $K = 9 \times 10^{-11}$ (9)

Operation at high switching frequency results in lower efficiency while providing the smallest solution. For this example 440 kHz was selected, resulting in R_{ON} = 253 kΩ. A standard value for R_{ON} = R3 = 237 kΩ is selected.

Copyright © 2012–2017, Texas Instruments Incorporated

8.2.1.2.4 Inductor Selection

The inductance selection is a compromise between solution size, output ripple, and efficiency. The peak inductor current at maximum load current should be smaller than the minimum current limit threshold of 150 mA. The maximum permissible peak to peak inductor ripple is determined by Equation 10.

$$\Delta IL = 2 \times \left(I_{LIM(min)} - I_{OUT(max)} \right) = 2 \times 50 = 100 \text{ mA} \tag{10}$$

The minimum inductance is determined by Equation 11.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{11}$$

Using maximum V_{IN} of 95 V, the calculation from Equation 11 results in L = 203 µH. A standard value of 220 µH is selected. With this value of inductance, peak-to-peak minimum and maximum inductor current ripple of 27 mA and 92 mA occur at the minimum and maximum input voltages, respectively. For robust short circuit protection, the inductor saturation current should be higher than the maximum current limit threshold of 300 mA.

8.2.1.2.5 Output Capacitor

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and is given by Equation 12.

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{ripple}}$$

where

- ΔV_{ripple} is the voltage ripple across the capacitor
- and ΔI_L is the inductor ripple current. (12)

Assuming V_{IN} = 95 V and substituting ΔV_{ripple} = 10 mV gives C_{OUT} = 2.6 µF. A 4.7-µF standard value is selected for C_{OUT} = C9. An X5R or X7R type capacitor with a voltage rating 16 V or higher should be selected.

8.2.1.2.6 Type II Ripple Circuit

Type II ripple circuit as described in *Ripple Configuration* is chosen for this example. For a constant on time converter to be stable, the injected in-phase ripple should be larger than the capacitive ripple on C_{OUT}.

Using type II ripple circuit equations with minimum FB pin ripple of 25 mV, the values of the series resistor R_C and ac coupling capacitor C_{ac} can calculated.

$$C \geq \frac{5}{f_{SW}(R_{FB2} \| R_{FB1})}$$

$$R_C \geq \frac{25 \text{ mV}}{\Delta I_{L(MIN)}} \tag{13}$$

Assuming R_{FB2} = 6.98 kΩ and R_{FB1} = 1 kΩ, the calculated minimum value of C_{ac} is 0.013 µF. A standard value of 0.1 µF is selected for C_{ac} = C8. The value of the series output resistor R_C is calculated for the minimum input voltage condition when the inductor ripple current as at a minimum. Using Equation 11 and assuming V_{IN} = 12.5 V, the minimum inductor ripple current is 27 mA. The calculated minimum value of R_C is 0.93 Ω. A standard value of 1.5 Ω is selected for R_C = R2 to provide additional ripple for stable switching at low V_{IN}.

8.2.1.2.7 V_{CC} and Bootstrap Capacitor

The V_{CC} capacitor provides charge to bootstrap capacitor as well as internal circuitry and low side gate driver. The bootstrap capacitor provides charge to high side gate driver. The recommended value for C_{VCC} = C7 is 1 µF. A good value for C_{BST} = C1 is 0.01 µF.

8.2.1.2.8 Input Capacitor

Input capacitor should be large enough to limit the input voltage ripple shown in Equation 14.

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f_{SW} \times \Delta V_{IN}} \tag{14}$$

Copyright © 2012–2017, Texas Instruments Incorporated

Choosing a ΔV_{IN} = 0.5 V gives a minimum C_{IN} = 0.12 µF. A standard value of 1.0 µF is selected for C_{IN} = C4. The input capacitor should be rated for the maximum input voltage under all conditions. A 50-V, X7R dielectric should be selected for this design.

Input capacitor should be placed directly across V_{IN} and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.1-µF capacitor should be placed near the IC to provide a bypass path for the high frequency component of the switching current. This helps limit the switching noise.

8.2.1.2.9 UVLO

The UVLO resistors R_{UV1} and R_{UV2} set the UVLO threshold and hysteresis according to Equation 15 and Equation 16.

$$V_{IN\,(HYS)} = I_{HYS} \times R_{UV2}$$

where

- I_{HYS} = 20 µA (15)

$$V_{IN}(\text{UVLO, rising}) = 1.225\ \text{V} \times \left(\frac{R_{UV2}}{R_{UV1}} + 1 \right) \quad (16)$$

For UVLO hysteresis of 2.5 V and UVLO rising threshold of 12 V, the calculated values of the UVLO resistors are RUV2 = 127 kΩ and RUV1 = 14.5 kΩ. Selecting standard values for R_{UV1} = R7 = 14 kΩ and R_{UV2} = R5 = 127 kΩ results in UVLO rising threshold of 12.5 V and hysteresis of 2.5 V.

8.2.1.3 Application Curves

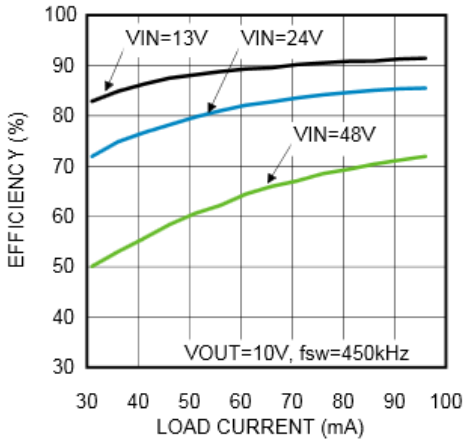


Figure 14. Efficiency vs Load Current

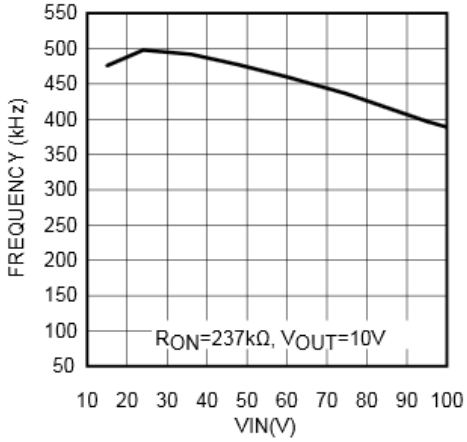


Figure 15. Frequency vs Input Voltage

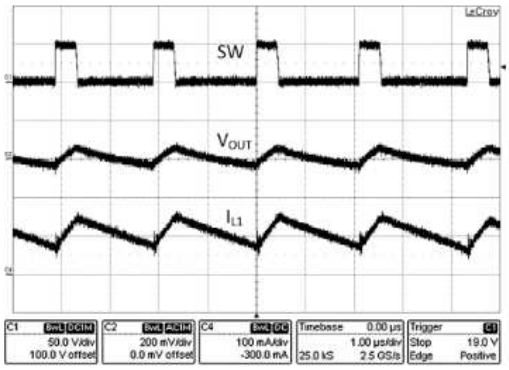


Figure 16. Typical Switching Waveform (V_{IN} = 48 V, I_{OUT} = 100 mA)

Copyright © 2012–2017, Texas Instruments Incorporated

8.2.2 Application Circuit: 20 V to 95 V Input and 10 V, 100 mA Output Isolated Fly-Buck™ Converter

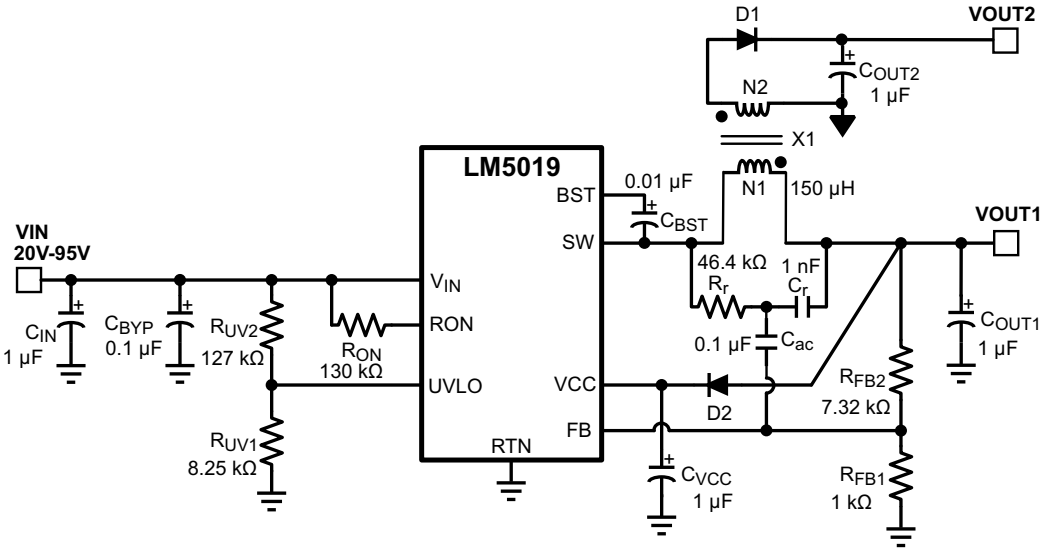


Figure 17. Isolated Fly-Buck™ Converter Using LM5019

8.2.2.1 Design Requirements

Selection of external components is illustrated through a design example. The design example specifications are shown in Table 4.

Table 4. Buck Converter Design Specifications

DESIGN PARAMETERS	VALUE
Input Voltage Range	20 V to 95 V
Primary Output Voltage	10 V
Secondary (Isolated) Output Voltage	9.5 V
Maximum Output Current (Primary + Secondary)	100 mA
Maximum Power Output	1 W
Nominal Switching Frequency	750 kHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Transformer Turns Ratio

The transformer turns ratio is selected based on the ratio of the primary output voltage to the secondary (isolated) output voltage. In this design example, the two outputs are nearly equal and a 1:1 turns ratio transformer is selected. Therefore, N2 / N1 = 1.

If the secondary (isolated) output voltage is significantly higher or lower than the primary output voltage, a turns ratio less than or greater than 1 is recommended. The primary output voltage is normally selected based on the input voltage range such that the duty cycle of the converter does not exceed 50% at the minimum input voltage. This condition is satisfied if VOUT1 < V_{IN_MIN} / 2.

8.2.2.2.2 Total IOUT

The total primary referred load current is calculated by multiplying the isolated output load(s) by the turns ratio of the transformer as shown in Equation 17.

$$I_{OUT(MAX)} = I_{OUT1} + I_{OUT2} \times \frac{N2}{N1} = 0.1\,A \quad (17)$$

8.2.2.2.3 RFB1, RFB2

The feedback resistors are selected to set the primary output voltage. The selected value for R_{FB1} is 1 kΩ. R_{FB2} can be calculated using the following equations to set V_{OUT1} to the specified value of 10 V. A standard resistor value of 7.32 kΩ is selected for R_{FB2}.

$$V_{OUT1} = 1.225V \times \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \tag{18}$$

$$\rightarrow R_{FB2} = \left(\frac{V_{OUT1}}{1.225} - 1\right) \times R_{FB1} = 7.16\ k\Omega \tag{19}$$

8.2.2.2.4 Frequency Selection

Equation 20 is used to calculate the value of R_{ON} required to achieve the desired switching frequency.

$$f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}}$$

where

- $K = 9 \times 10^{-11}$ (20)

For V_{OUT1} of 10 V and f_{SW} of 750 kHz, the calculated value of R_{ON} is 148 kΩ. A lower value of 130 kΩ is selected for this design to allow for second order effects at high switching frequency that are not included in Equation 1.

8.2.2.2.5 Transformer Selection

A coupled inductor or a flyback-type transformer is required for this topology. Energy is transferred from primary to secondary when the low-side synchronous switch of the buck converter is conducting.

The maximum inductor primary ripple current that can be tolerated without exceeding the buck switch peak current limit threshold (0.15 A minimum) is given by Equation 21.

$$\Delta I_{L1} = \left(0.15 - I_{OUT1} - I_{OUT2} \times \frac{N2}{N1}\right) \times 2 = 0.1\,A \tag{21}$$

Using the maximum peak-to-peak inductor ripple current ΔI_{L1} from Equation 21, the minimum inductor value is given by Equation 22.

$$L1 = \frac{V_{IN(MAX)} - V_{OUT}}{\Delta I_{L1} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} = 119.3\ \mu H \tag{22}$$

A higher value of 150 µH is selected to insure the high-side switch current does not exceed the minimum peak current limit threshold.

8.2.2.2.6 Primary Output Capacitor

In a conventional buck converter the output ripple voltage is calculated as shown in Equation 23.

$$\Delta V_{OUT} = \frac{\Delta I_{L1}}{8 \times f \times C_{OUT1}} \tag{23}$$

To limit the primary output ripple voltage ΔV_{OUT1} to approximately 50 mV, an output capacitor C_{OUT1} of 0.33 µF is required.

Figure 18 shows the primary winding current waveform (IL1) of a Fly-Buck converter. The reflected secondary winding current adds to the primary winding current during the buck switch off-time. Because of this increased current, the output voltage ripple is not the same as in conventional buck converter. The output capacitor value calculated in Equation 23 should be used as the starting point. Optimization of output capacitance over the entire line and load range must be done experimentally. If the majority of the load current is drawn from the secondary isolated output, a better approximation of the primary output voltage ripple is given by Equation 24.

$$\Delta V_{OUT1} = \frac{\left(I_{OUT2} \times \frac{N2}{N1}\right) \times T_{ON(MAX)}}{C_{OUT1}} \approx 67\ mV \tag{24}$$

Copyright © 2012–2017, Texas Instruments Incorporated

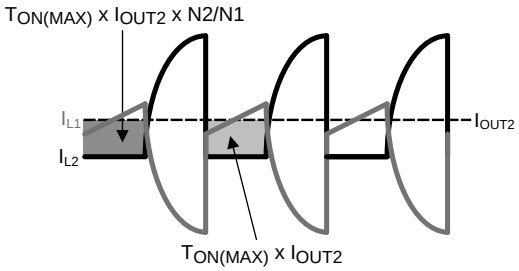


Figure 18. Current Waveforms for C_{OUT1} Ripple Calculation

A standard 1-µF, 25-V capacitor is selected for this design. If lower output voltage ripple is required, a higher value should be selected for C_{OUT1} and/or C_{OUT2}.

8.2.2.2.7 Secondary Output Capacitor

A simplified waveform for secondary output current (I_{OUT2}) is shown in Figure 19.

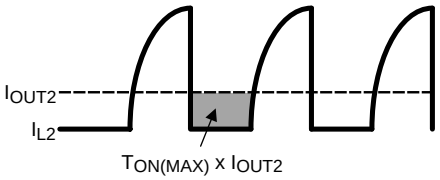


Figure 19. Secondary Current Waveforms for C_{OUT2} Ripple Calculation

The secondary output current (I_{OUT2}) is sourced by C_{OUT2} during on-time of the buck switch, T_{ON}. Ignoring the current transition times in the secondary winding, the secondary output capacitor ripple voltage can be calculated using Equation 25.

$$\Delta V_{OUT2} = \frac{I_{OUT2} \times T_{ON\,(MAX)}}{C_{OUT2}} \tag{25}$$

For a 1:1 transformer turns ratio, the primary and secondary voltage ripple equations are identical. Therefore, C_{OUT2} is chosen to be equal to C_{OUT1} (1 µF) to achieve comparable ripple voltages on primary and secondary outputs.

If lower output voltage ripple is required, a higher value should be selected for C_{OUT1} and/or C_{OUT2}.

8.2.2.2.8 Type III Feedback Ripple Circuit

Type III ripple circuit as described in *Ripple Configuration* is required for the Fly-Buck topology. Type I and Type II ripple circuits use series resistance and the triangular inductor ripple current to generate ripple at V_{OUT} and the FB pin. The primary ripple current of a Fly-Buck is the combination or primary and reflected secondary currents as illustrated in Figure 18. In the Fly-Buck topology, Type I and Type II ripple circuits suffer from large jitter as the reflected load current affects the feedback ripple.

Copyright © 2012–2017, Texas Instruments Incorporated

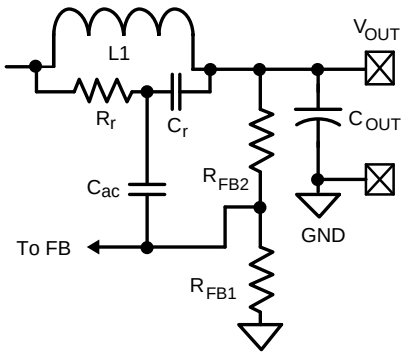


Figure 20. Type III Ripple Circuit

Selecting the Type III ripple components using the equations from *Ripple Configuration* will guarantee that the FB pin ripple is be greater than the capacitive ripple from the primary output capacitor C_{OUT1}. The feedback ripple component values are chosen as shown in Equation 26.

C_r = 1000 pF

C_{ac} = 0.1 µF

$$R_r C_r \le \frac{(V_{IN\,(MIN)} - V_{OUT}) \times T_{ON}}{50\ mV} \tag{26}$$

The calculated value for Rr is 66 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance should be selected to allow for variations in T_{ON}, C_{OUT1} and other components. For this design, Rr value of 46.4 kΩ is selected.

8.2.2.2.9 Secondary Diode

The reverse voltage across secondary-rectifier diode D1 when the high-side buck switch is off can be calculated using Equation 27.

$$V_{D1} = \frac{N2}{N1} V_{IN} \tag{27}$$

For a V_{IN_MAX} of 95 V and the 1:1 turns ratio of this design, a 100 V Schottky is selected.

8.2.2.2.10 V_{CC} and Bootstrap Capacitor

A 1-µF capacitor of 16 V or higher rating is recommended for the V_{CC} regulator bypass capacitor.

A good value for the BST pin bootstrap capacitor is 0.01-µF with a 16 V or higher rating.

8.2.2.2.11 Input Capacitor

The input capacitor is typically a combination of a smaller bypass capacitor located near the regulator IC and a larger bulk capacitor. The total input capacitance should be large enough to limit the input voltage ripple to a desired amplitude. For input ripple voltage ΔV_{IN}, C_{IN} can be calculated using Equation 28.

$$C_{IN} \ge \frac{I_{OUT(MAX)}}{4 \times f \times \Delta V_{IN}} \tag{28}$$

Choosing a ΔV_{IN} of 0.5 V gives a minimum C_{IN} of 0.067 µF. A standard value of 0.1 µF is selected for C_{BYP} in this design. A bulk capacitor of higher value reduces voltage spikes due to parasitic inductance between the power source to the converter. A standard value of 1 µF is selected for C_{IN} in this design. The voltage ratings of the two input capacitors should be greater than the maximum input voltage under all conditions.

8.2.2.2.12 UVLO Resistors

UVLO resistors R_{UV1} and R_{UV2} set the undervoltage lockout threshold and hysteresis according to Equation 29 and Equation 30.

Copyright © 2012–2017, Texas Instruments Incorporated

$$V_{IN\,(HYS)} = I_{HYS} \times R_{UV2}$$

where

- I_{HYS} = 20 µA, typical (29)

$$V_{IN}(\text{UVLO, rising}) = 1.225V \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \quad (30)$$

For a UVLO hysteresis of 2.5 V and UVLO rising threshold of 20 V, Equation 29 and Equation 30 require R_{UV1} of 8.25 kΩ and R_{UV2} of 127 kΩ and these values are selected for this design example.

8.2.2.2.13 V_{CC} Diode

Diode D2 is an optional diode connected between V_{OUT1} and the V_{CC} regulator output pin. When V_{OUT1} is more than one diode drop greater than the V_{CC} voltage, the V_{CC} bias current is supplied from V_{OUT1}. This results in reduced power losses in the internal V_{CC} regulator which improves converter efficiency. V_{OUT1} must be set to a voltage at least one diode drop higher than 8.55 V (the maximum V_{CC} voltage) if D2 is used to supply bias current.

8.2.2.3 Application Curves

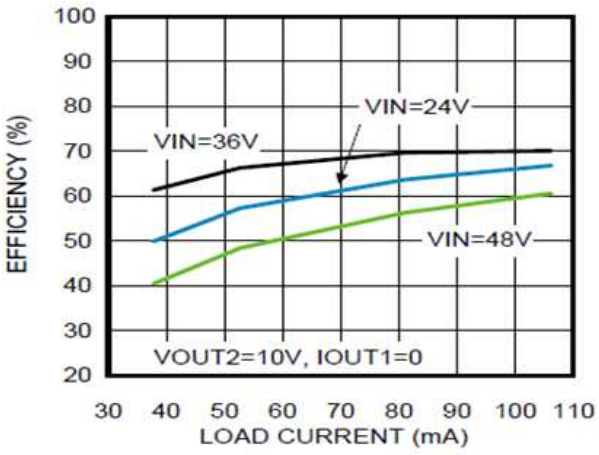
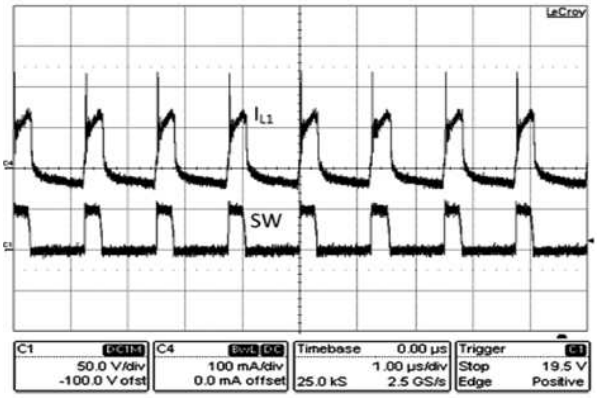


Figure 21. Efficiency at 750 kHz, VOUT1 = 10 V



VIN = 48 V IOUT1 = 0 mA IOUT2 = 100 mA

Figure 22. Steady-State Waveform

9 Power Supply Recommendations

LM5019 is a power management device. The power supply for the device is any DC voltage source within the specified input range.

10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor should be placed close to the IC, directly across V_{IN} and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-µF or 0.47-µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see Figure 23).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (see Figure 23).
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM5019. Therefore, care should be taken while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace should not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between V_{IN} and GND every cycle and is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

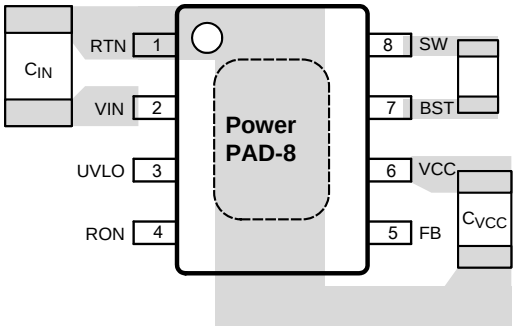


Figure 23. Placement of Bypass Capacitors

版权 © 2012–2017, Texas Instruments Incorporated

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 LM5019 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先键入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 文档支持

11.2.1 相关文档

- *AN-2240《LM5019 隔离式评估板》*(SNOU100)
- *《PowerPAD™ 布局指南》*(SLOA120)
- *AN-1481《使用恒定导通时间稳压器设计控制输出纹波并实现 ESR 独立性》*(SNVA166)
- *AN-2238《LM5019 降压评估板》*(SNVA647)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

Fly-Buck, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

版权 © 2012–2017, Texas Instruments Incorporated

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

版权 © 2012–2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5019MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L5019 MR	Samples
LM5019MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L5019 MR	Samples
LM5019SD/NOPB	ACTIVE	WSON	NGU	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5019	Samples
LM5019SDX/NOPB	ACTIVE	WSON	NGU	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5019	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

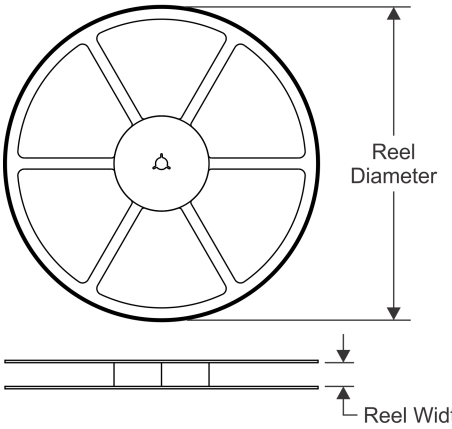
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

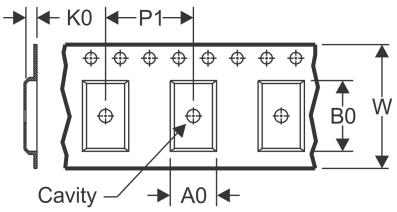
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

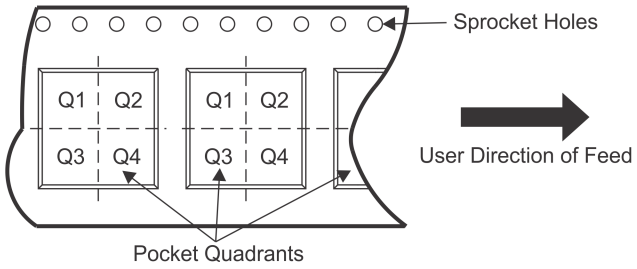


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

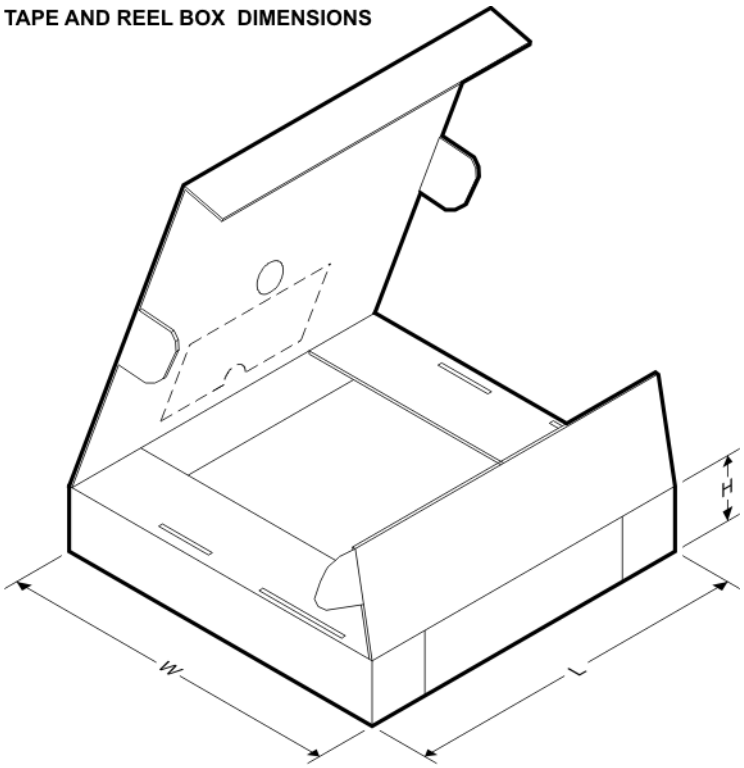
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

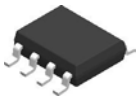
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5019MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5019SD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5019SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5019MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM5019SD/NOPB	WSON	NGU	8	1000	210.0	185.0	35.0
LM5019SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

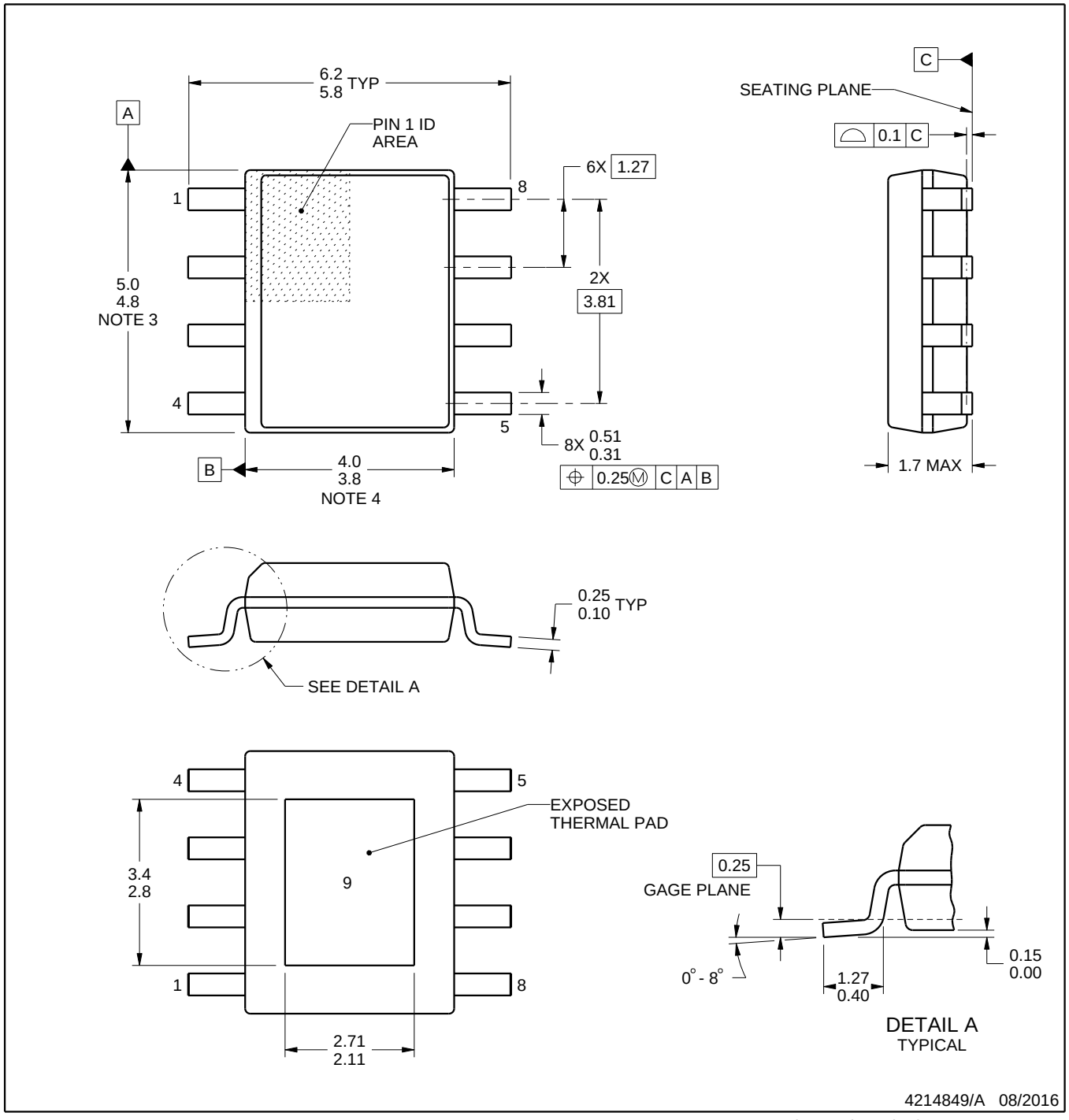


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

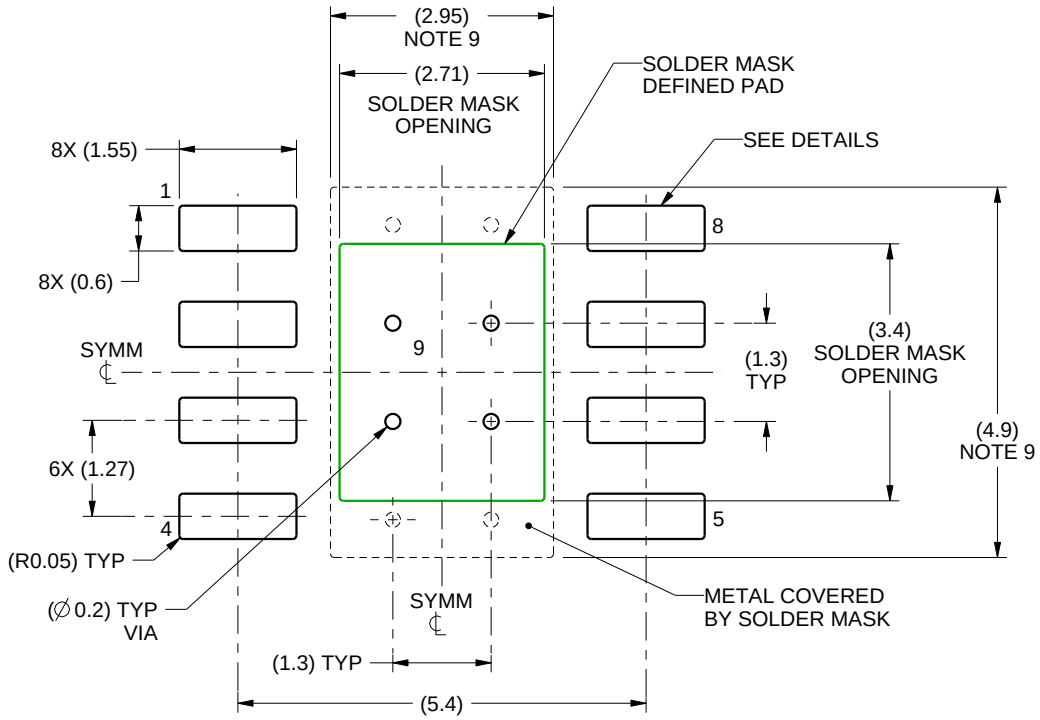
PLASTIC SMALL OUTLINE



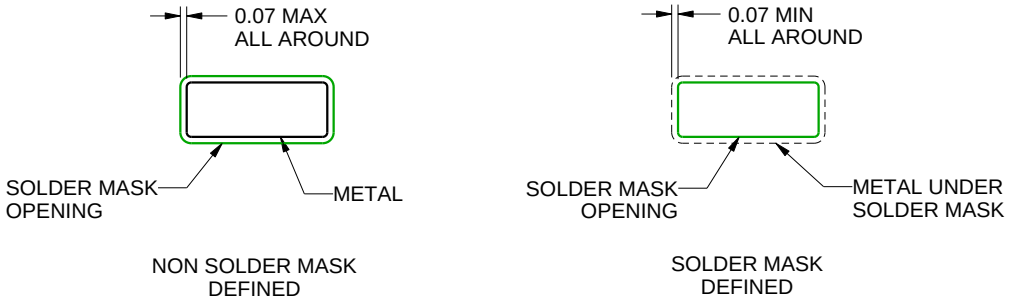
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

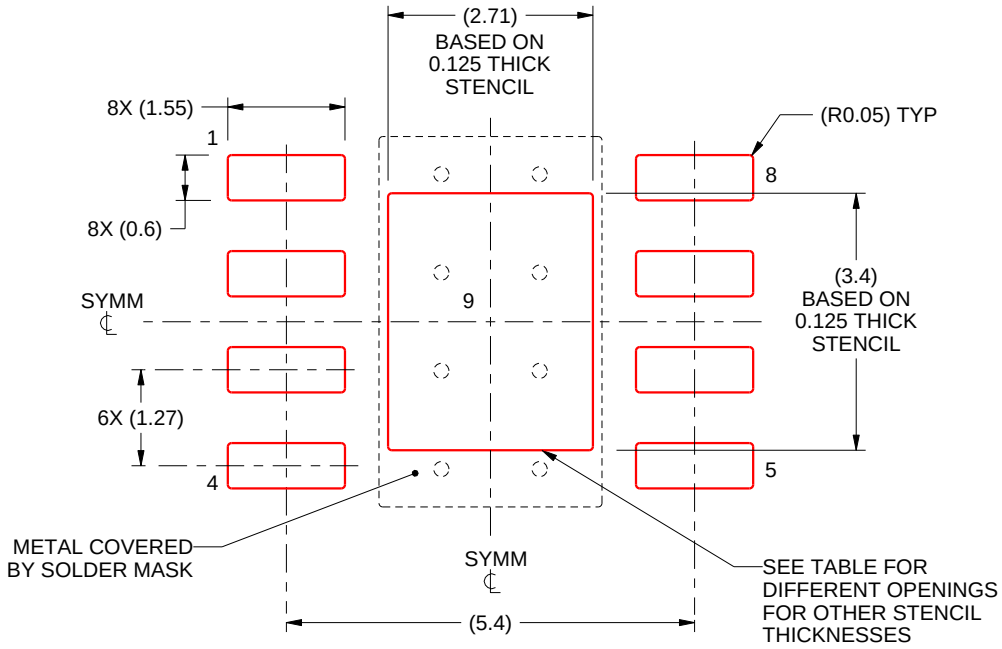
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

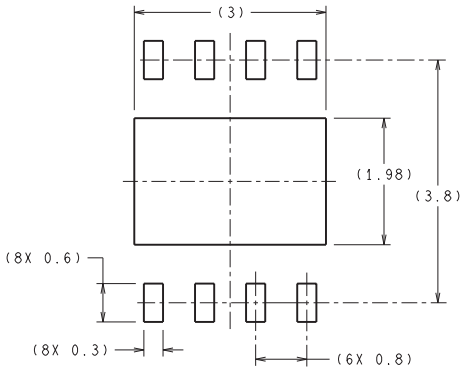
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

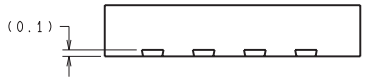
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

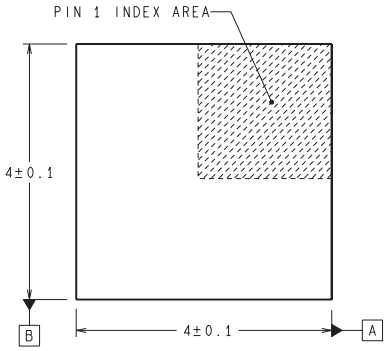
NGU0008B

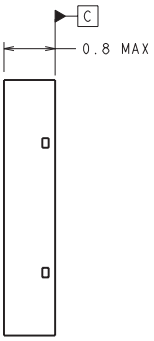


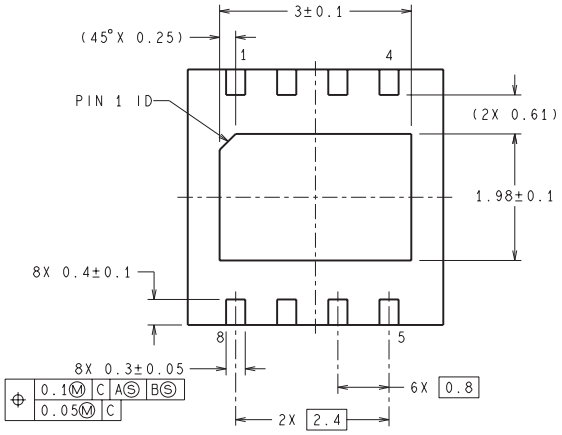
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY









SDC08B (Rev A)

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司