TPSM265R1 65-V Input, 100-mA Power Module with Ultra-Low I_Q

1 Features

- Integrated controller, MOSFETs, and inductor
- 2.8-mm x 3.7-mm x 1.9-mm package
- Wide input voltage range of 3 V to 65 V
- Three output voltage options:
  - 3.3 V, 5 V, Adjustable (1.223 V to 15 V)
- 100-mA output current
- 10.5-µA no-load quiescent current
- ±1% Internal voltage reference
- PFM mode of operation
- –40°C to 125°C ambient temperature range
- Active slew rate control for low EMI
- Meets EN55011 EMI standards
- Monotonic start-up into prebiased output
- No loop-compensation or bootstrap components
- Precision enable and input UVLO with hysteresis
- Thermal shutdown protection with hysteresis
- Create a custom regulator design using WEBENCH® Power Designer

2 Applications

- Field Transmitter and Process Sensors
- Position and Proximity Sensors
- PLC, DCS & PAC
- Servo Drive Power Supply Module
- Inverted Output Applications

3 Description

The TPSM265R1 is a compact, easy-to-use module that operates over a wide input voltage range up to a maximum continuous input voltage of 65 V. The module fully integrates a controller, MOSFETs, and an output inductor. The module is designed to quickly and easily implement a power design in a small PCB footprint. There are two fixed output voltage options, 3.3 V and 5 V, and an adjustable output voltage option that can be adjusted from 1.223 V to 15 V. Each option has a load current rating of 100 mA. The TPSM265R1 operates in Pulse Frequency Modulation (PFM) mode, providing optimal efficiency at light loads. The control scheme does not require loop compensation, providing excellent line and load transient.

Although designed for small size and simplicity, the TPSM265R1 offers many features. Precision enable, adjustable UVLO, and hysteresis allow for specific power-up and power-down requirements. Selectable/adjustable start-up timing options include minimum delay (no soft-start), internally fixed (900 µs), and externally programmable soft start via an external capacitor. An open-drain PGOOD indicator can be used for sequencing and output voltage monitoring. The very small 2.8-mm × 3.7-mm × 1.9-mm package is a good fit for space-constrained applications.

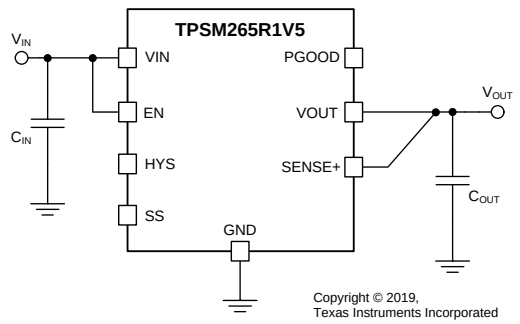
Device Information(1)

PART #	OUTPUT	PACKAGE
TPSM265R1	Adjustable	SIL-10C
TPSM265R1V3	3.3 V	SIL-10C
TPSM265R1V5	5 V	SIL-10C

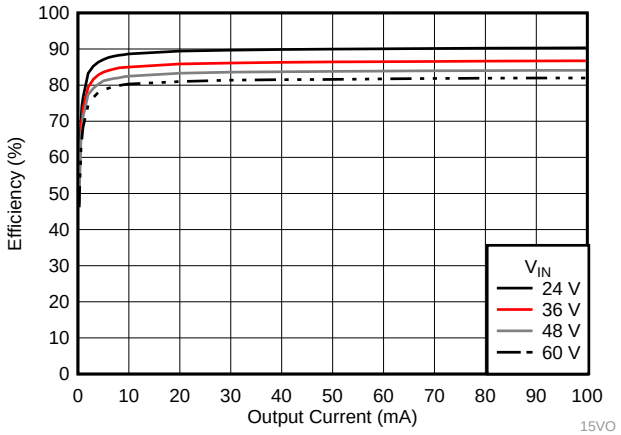
(1) For all available packages, see the orderable addendum at the end of the data sheet.

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Typical Schematic, Fixed Output



Typical Efficiency, V_{OUT} = 15 V



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

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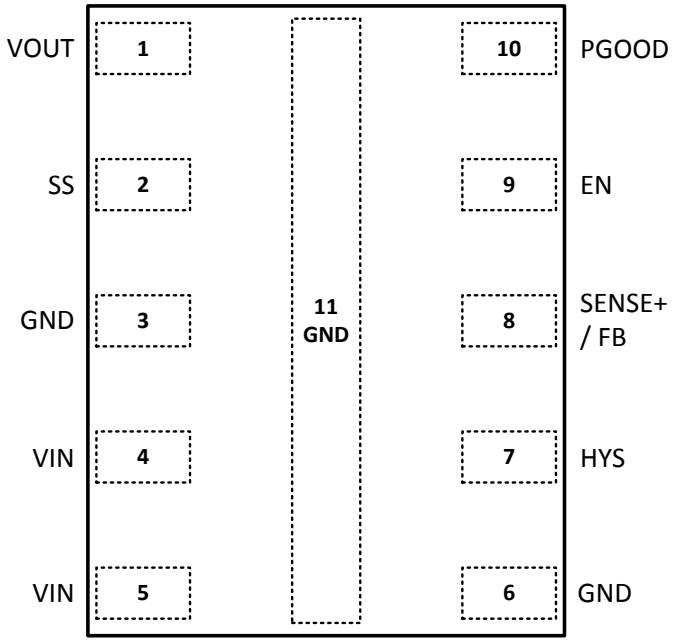
4 Revision History

DATE	REVISION	NOTES
August 2019	*	Initial Release

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5 Pin Configuration and Functions

SIL-10C Package
10-Pin Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VOUT	O	Output voltage pin. The VOUT pin is connected to the internal output inductor. Connect the VOUT pin to an external output capacitor and the output load. The output capacitor connections should be made as close as possible to the VOUT and GND pins of the module.
2	SS	I	Soft-start programming pin. If the SS pin is floating, the output voltage ramp up time is approximately 1 ms after the device is enabled by the EN pin. If a 100 k resistor is placed from the SS pin to GND, the internal soft-start is disabled and the output voltage ramps up immediately after the device is enabled with the EN pin. Other output voltage ramp up times can be obtained by connecting an appropriate capacitance from the SS pin to GND.
3, 6, 11	GND	G	Ground pins. Connect all GND pins to the system ground plane. Pin 3 is not connected to GND internal to the module. This connection must be made on the host PCB.
4, 5	VIN	I	Input supply pins. The VIN pins are connected to the internal controller and power MOSFETs. Connect the VIN pins to an external input capacitor and the input power source. The input capacitor connections must be made as close as possible to the VIN pins and GND pin 6 of the module.
7	HYS	O	Enable hysteresis pin. The open-drain HYS pin can be used along with external resistors to program the hysteresis of a user-defined UVLO using the EN pin. HYS is internally pulled to GND when EN is below its turn-on threshold and HYS goes open drain when EN is above its turn-on threshold.
8	SENSE+/FB	I	Output voltage feedback pin. For fixed output voltage options, the SENSE+ pin must be externally connected to VOUT. For the adjustable output voltage option, the FB pin must be connected to an external resistor divider that is connected between VOUT and GND.
9	EN	I	Enable pin. The module is enabled when the EN pin is pulled high and disabled when the EN pin is pulled low. An external resistor divider can be connected to the EN pin to act as an external UVLO.
10	PGOOD	O	Power Good pin. The open-drain PGOOD pin is pulled low when the SENSE+ or FB pin is below the VOUT regulation target. An external 10 k to 100 k pullup resistor can be used to pull the PGOOD pin high when VOUT meets the regulation target.

(1) G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	68	V
	SENSE+, PGOOD	–0.3	16	V
	HYS	–0.3	7	V
	FB, SS	–0.3	3.6	
Output voltage	VOUT	–0.3	16	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		tbd	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		tbd	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±tbd	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±tbd	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Input voltage	VIN		3 (1)		65	V
	PGOOD				12	V
	HYS				5	V
Output voltage	VOUT	Adjustable option	1.223		15	V
		Fixed 5V option		5		V
		Fixed 3.3V option		3.3		
Output current	Iout				100	mA
T_A	Operating ambient temperature		–40		125	°C
C_{IN}	Input capacitance		1 (2)			µF
C_{OUT}	Output capacitance		10 (3)			µF

(1) The minimum input voltage is 3.0 V or (V_{OUT} + 2 V), whichever is greater.
(2) See the Input Capacitance section of the datasheet for more information.
(3) The minimum required output capacitance is 10 µF, ceramic type. Depending on the application, additional output capacitance may be required. See the Output Capacitance section of the datasheet for more information.

6.4 Thermal Information

THERMAL METRIC (1)		TPSM265R1 SIL-10C 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*

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6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +125°C, V_{IN} = 12 V, V_{OUT} = 5 V, (unless otherwise noted); C_{IN1} = 1 µF, 100-V, 1206 ceramic, C_{IN2} = 33 µF, 100-V, electrolytic (optional), and C_{OUT} = 47 µF, 16-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VIN	Input supply voltage range	Over I_{OUT} range	3(1)		65	V
UVLO	VIN UVLO rising threshold	VIN rising	2.60	2.75	2.95	V
	VIN UVLO falling threshold	VIN falling	2.35	2.45	2.60	V
$I_{Q(VIN)}$	VIN operating non-switching supply current	V_{FB} = 1.5 V, T_A = 25°C		10.5	15	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V, T_A = 25°C		4.6	6.0	µA
ENABLE						
$V_{EN(rise)}$	EN voltage rising threshold	EN voltage rising	1.163	1.212	1.262	V
$V_{EN(fall)}$	EN voltage falling threshold	EN voltage falling	1.109	1.144	1.178	V
$V_{EN(hyst)}$	EN voltage hysteresis			68		mV
$V_{EN(sd)}$	EN shutdown threshold	EN voltage falling	0.3	0.6		V
R_{HYS}	HYS on-resistance	V_{EN} = 1 V		80	200	Ω
$I_{HYS(LKG)}$	HYS off-state leakage current	V_{EN} = 1.5 V, V_{HYS} = 5.5 V		10	100	nA
FEEDBACK (Adjustable option)						
V_{FB}	Feedback voltage(2)(3)	Lower regulation threshold	1.205	1.223	1.241	V
		Upper regulation threshold	1.220	1.233	1.246	
		Hysteresis		10		mV
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0A		0.3%		
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.3%		
	Temperature variation	-40°C ≤ T_A = T_J ≤ 125°C, I_{OUT} = 0A		0.5%		
I_{FB}	Input bias current into FB pin	V_{FB} = 1 V			100	nA
OUTPUT VOLTAGE (Fixed 5 V option)						
V_{OUT}	Output voltage set-point	SENSE+ connected to VOUT	4.9	5.0	5.1	V
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0A		0.3%		
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.3%		
	Temperature variation	-40°C ≤ T_A = T_J ≤ 125°C, I_{OUT} = 0A		0.5%		
ISENSE+	SENSE+ input current			6.7		µA
eff	Efficiency	V_{OUT} = 5.0 V, I_{OUT} = 50 mA		83.0%		
OUTPUT VOLTAGE (Fixed 3.3 V option)						
V_{OUT}	Output voltage set-point	SENSE+ connected to VOUT	3.23	3.3	3.37	V
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 0A		0.3%		
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.3%		
	Temperature variation	-40°C ≤ T_A = T_J ≤ 125°C, I_{OUT} = 0A		0.5%		
ISENSE+	SENSE+ input current			3.9		µA
eff	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 50 mA		77.2%		
CURRENT						
I_{OUT}	Output current	See SOA curves for any thermal derating	0		100	mA
I_{OCL}	Over-current limit threshold	V_{OUT} foldback		130		mA
SOFT-START						
I_{SS}	Soft-start charge current	V_{SS} = 1 V		10		µA
T_{SS}	Soft-start rise time	SS pin open		900		µs

(1) For output voltages ≤ 4 V, the recommended minimum input voltage is 3.0 V or (V_{OUT} + 1.6 V), whichever is greater. For output voltages > 4 V, the recommended minimum input voltage is (V_{OUT} + 2 V).
(2) The FB pin has both lower and upper thresholds associated with the hysteretic control scheme of the module.
(3) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.

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Electrical Characteristics (continued)

Limits apply over T_A = –40°C to +125°C, V_{IN} = 12 V, V_{OUT} = 5 V, (unless otherwise noted); C_{IN1} = 1 µF, 100-V, 1206 ceramic, C_{IN2} = 33 µF, 100-V, electrolytic (optional), and C_{OUT} = 47 µF, 16-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PGOOD	PGOOD threshold	PGOOD high, V_{OUT} rising		94%		
PGOOD	PGOOD threshold	PGOOD low, V_{OUT} falling		87%		
$I_{PGOOD(LKG)}$	PGOOD leakage current	V_{PGOOD} = 5.5 V, PGOOD high		10	100	nA
R_{PGOOD}	PGOOD ON-resistance	PGOOD low		80	200	Ω
	Min VIN for valid PGOOD output	I_{PGOOD} = 0.1 mA, V_{PGOOD} < 0.5 V		1.2	1.65	V
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (4)	Temperature rising		170		°C
T_{HYST}	Thermal shutdown hysteresis (4)			10		°C

(4) Specified by design. Not production tested.

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6.6 Typical Characteristics (VIN = 5 V)

Refer to *Typical Applications* for circuit designs.

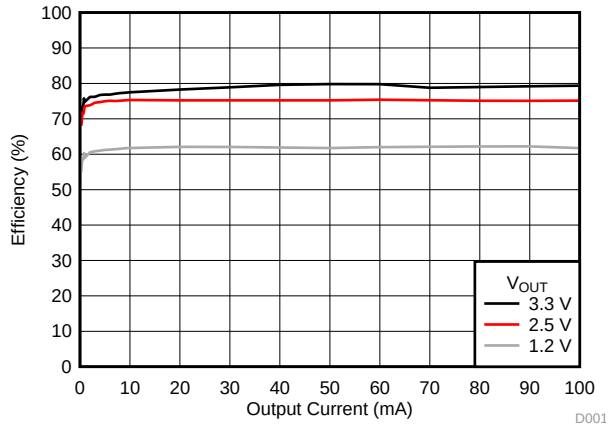


Figure 1. Efficiency

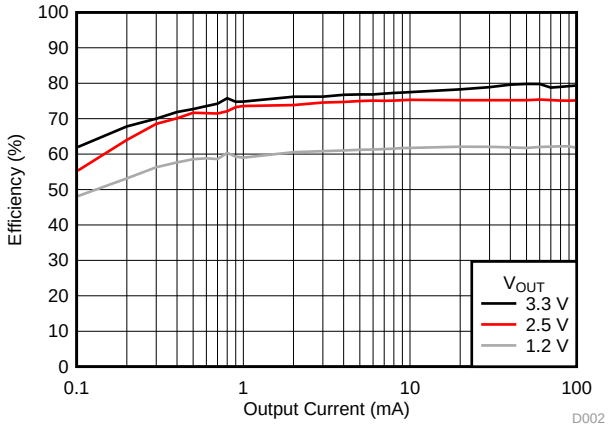


Figure 2. Efficiency Log Scale

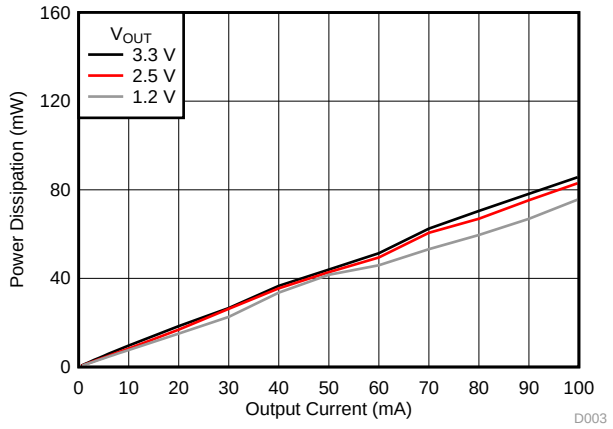
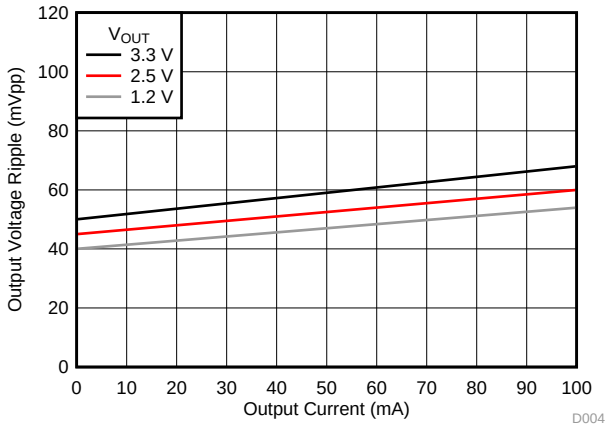
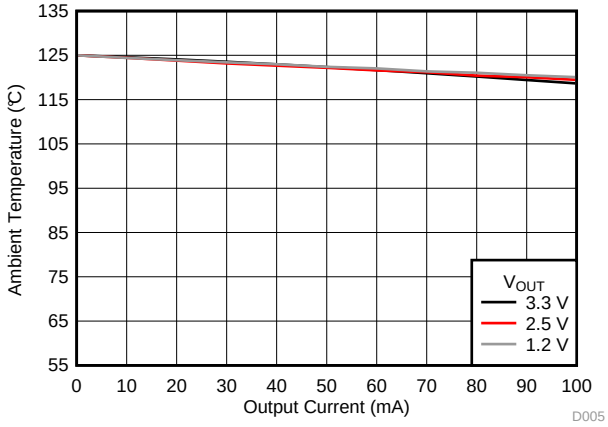


Figure 3. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

Figure 4. Output Voltage Ripple



Applies to a device soldered to a 50 mm × 75 mm, 4-layer PCB

Figure 5. Safe Operating Area

ADVANCE INFORMATION

6.7 Typical Characteristics (VIN = 12 V)

Refer to *Typical Applications* for circuit designs.

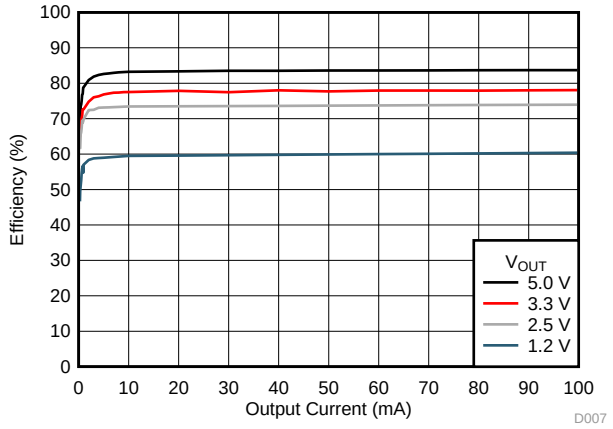


Figure 6. Efficiency

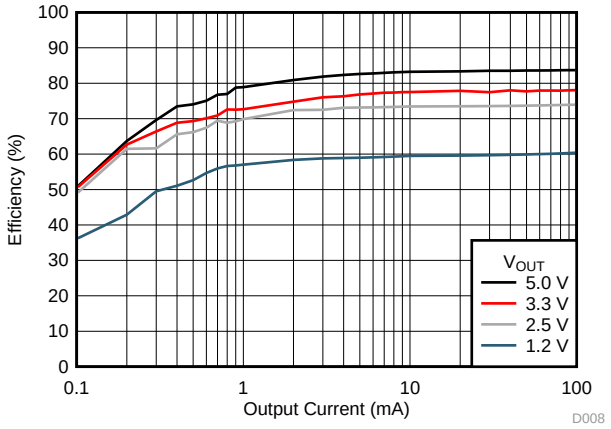


Figure 7. Efficiency Log Scale

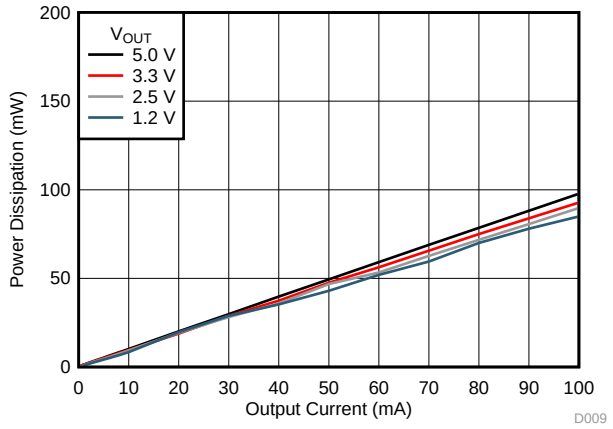
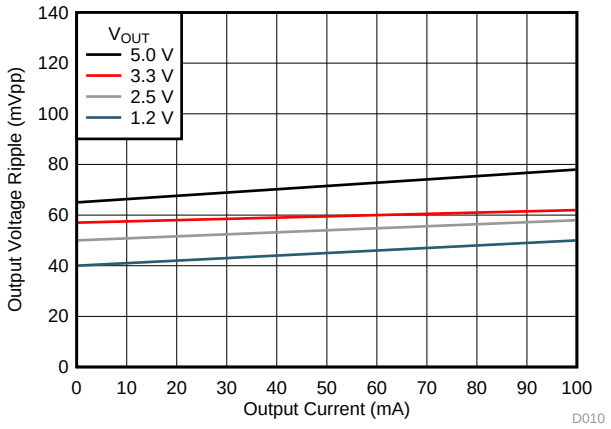
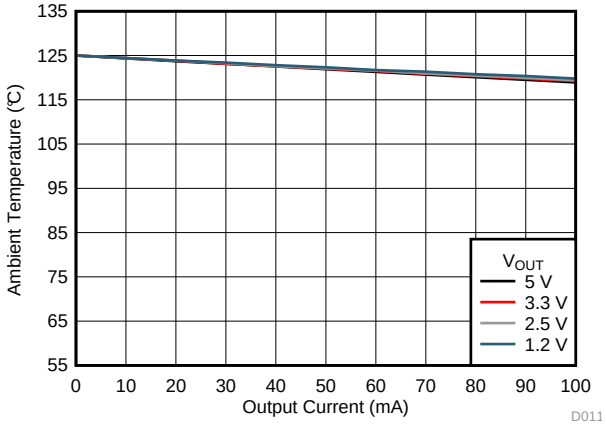


Figure 8. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

Figure 9. Output Voltage Ripple



Applies to a device soldered to a 50 mm × 75 mm, 4-layer PCB

Figure 10. Safe Operating Area

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6.8 Typical Characteristics (VIN = 24 V)

Refer to *Typical Applications* for circuit designs.

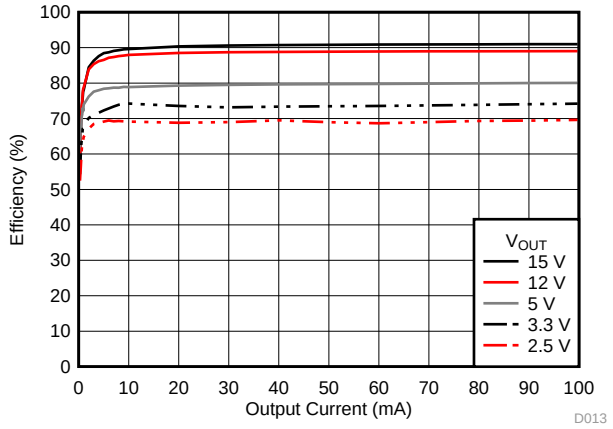


Figure 11. Efficiency

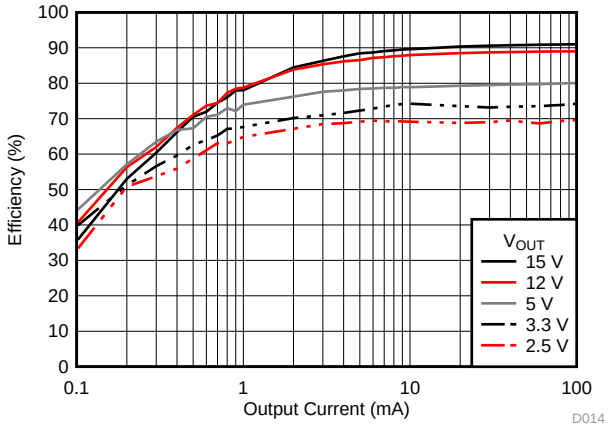


Figure 12. Efficiency Log Scale

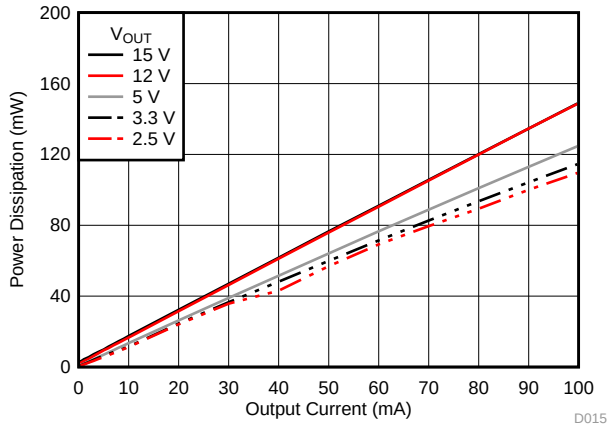
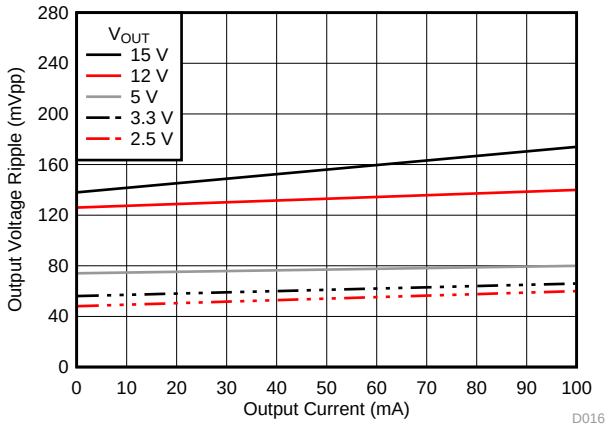
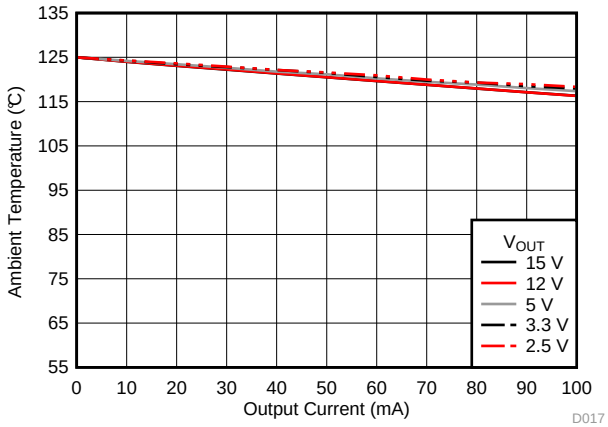


Figure 13. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

Figure 14. Output Voltage Ripple



Applies to a device soldered to a 50 mm × 75 mm, 4-layer PCB

Figure 15. Safe Operating Area

ADVANCE INFORMATION

6.9 Typical Characteristics (VIN = 48 V)

Refer to *Typical Applications* for circuit designs.

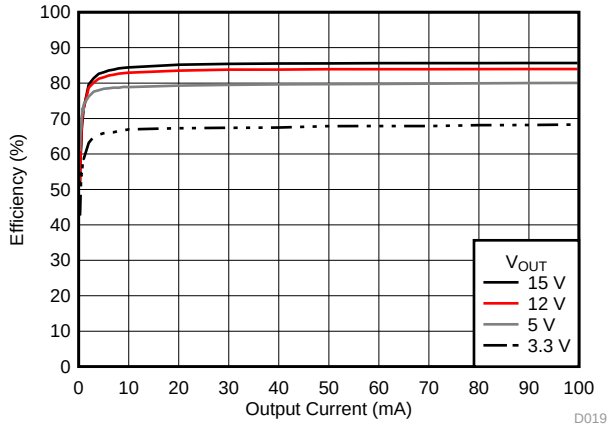


Figure 16. Efficiency

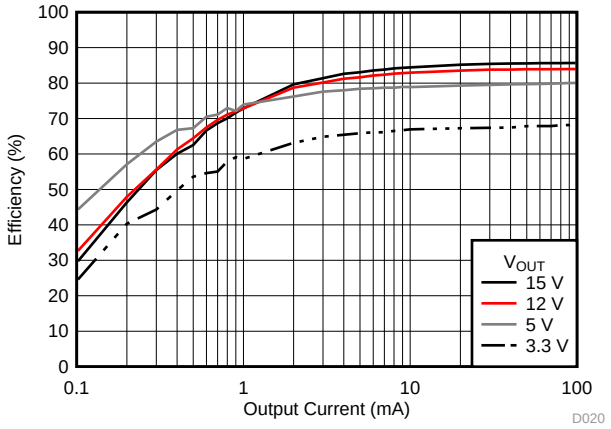


Figure 17. Efficiency Log Scale

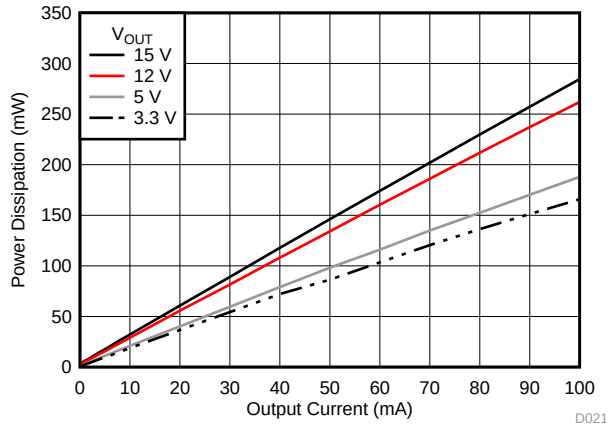
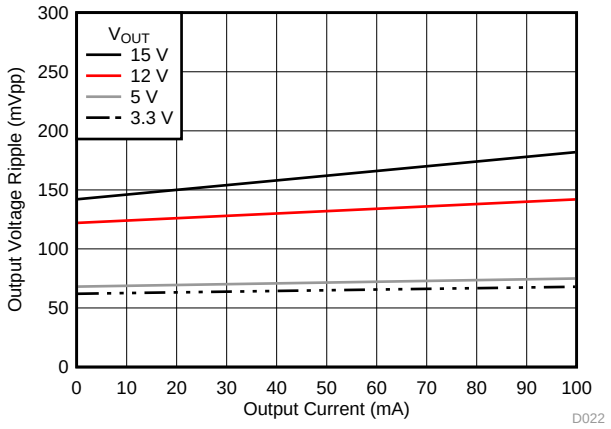
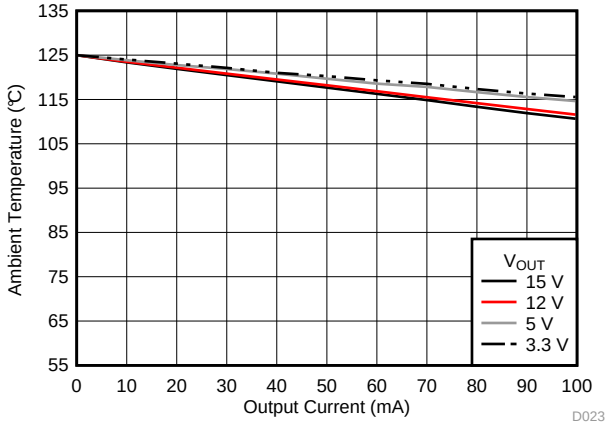


Figure 18. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

Figure 19. Output Voltage Ripple



Applies to a device soldered to a 50 mm × 75 mm, 4-layer PCB

Figure 20. Safe Operating Area

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6.10 Typical Characteristics (VIN = 65 V)

Refer to *Typical Applications* for circuit designs.

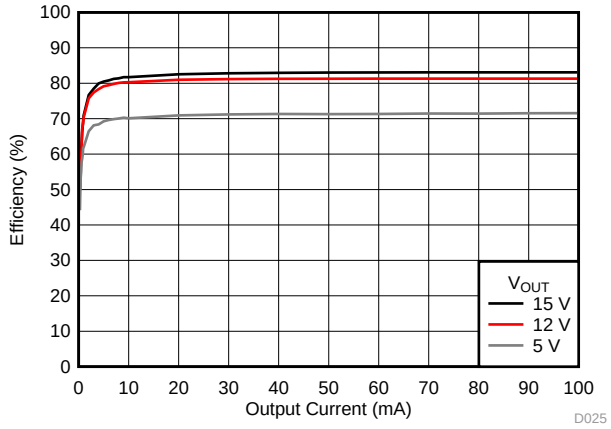


Figure 21. Efficiency

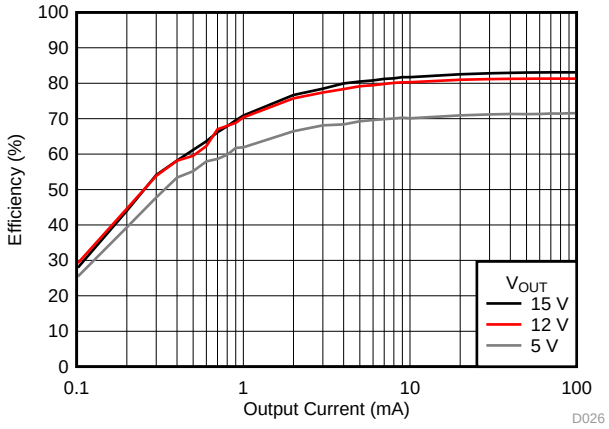


Figure 22. Efficiency Log Scale

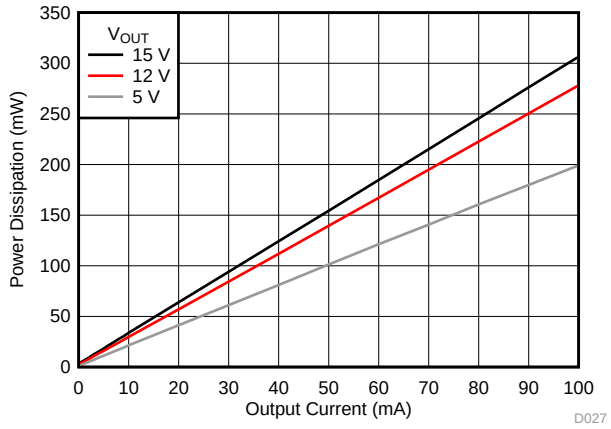
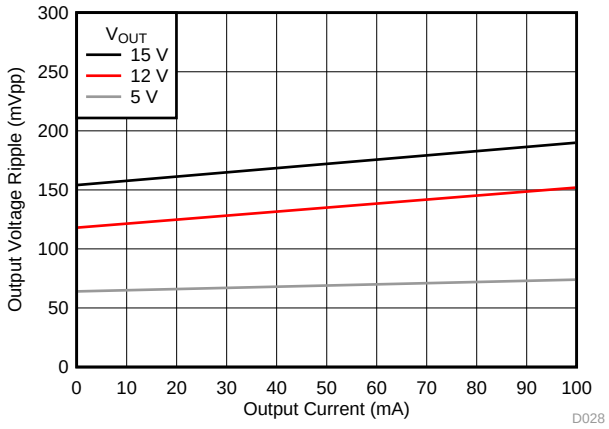
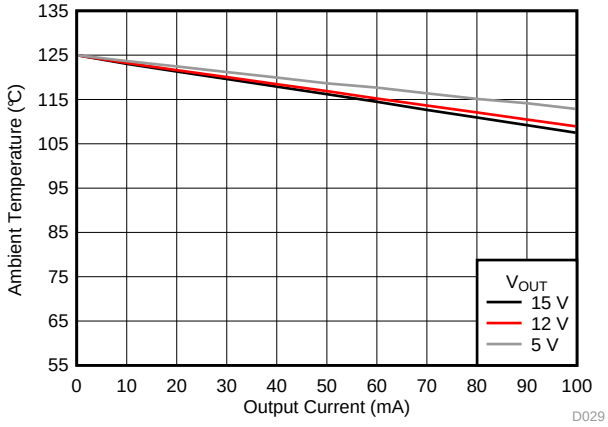


Figure 23. Power Dissipation



C_{OUT} = 47 µF, 16-V, ceramic

Figure 24. Output Voltage Ripple



Applies to a device soldered to a 50 mm × 75 mm, 4-layer PCB

Figure 25. Safe Operating Area

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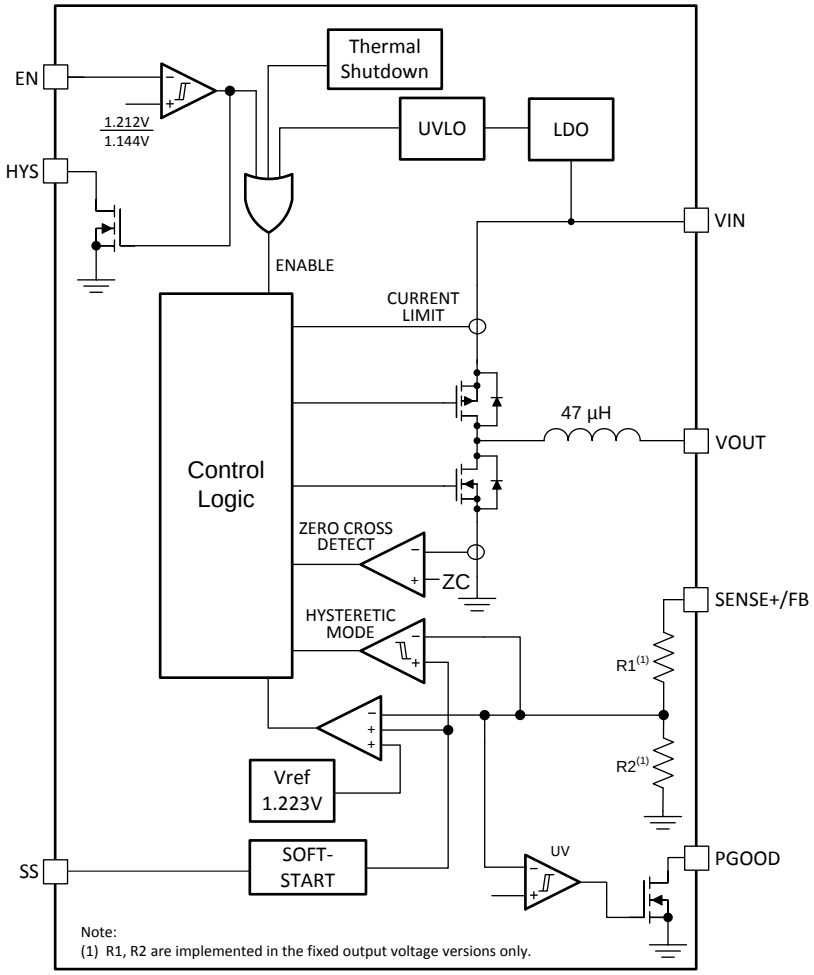
7 Detailed Description

7.1 Overview

The TPSM265R1 converter is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 3.3-V, 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated or fully-regulated supply rails. With integrated power controller, inductor, and MOSFETs, the TPSM265R1 delivers up to 100-mA DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Operation in pulse frequency modulation (PFM) mode achieves exceptional light-load efficiency performance. Control-loop compensation is not required, reducing design time and external component count.

The TPSM265R1 incorporates other features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed or externally-adjustable soft-start, monotonic start-up into prebiased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple *Layout*, requiring as few as two external components.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjustable Output Voltage (FB)

The TPSM265R1 has three voltage feedback options: fixed 3.3 V, fixed 5 V, and adjustable 1.223 V to 15 V. The fixed 3.3-V and 5-V versions include internal feedback resistors that sense the output directly through the SENSE+ pin; the adjustable voltage option senses the output through an external resistor divider connected from the output to the FB pin.

Setting the output voltage of the adjustable option requires two resistors, R_{FBT} and R_{FBB} (see Figure 26). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and GND (pin 6). A resistor divider programs the ratio from output voltage V_{OUT} to FB. The recommended value of R_{FBT} is 100 kΩ. The value for R_{FBB} can be calculated using Equation 1.

$$R_{FBB} = \frac{1.223}{V_{OUT} - 1.223} \times R_{FBT} \quad (1)$$

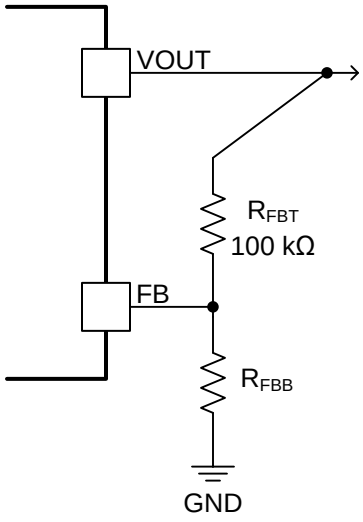


Figure 26. FB Resistor Divider

Table 1. Standard R_{FBB} Values

VOUT (V)	R_{FBB} (kΩ) (1)		VOUT (V)	R_{FBB} (kΩ) (1)
1.223	open		3.3	59.0
1.5	442		5.0	32.4
1.8	210		7.5	19.6
2.0	158		10	14.0
2.5	95.3		12	11.3
3.0	68.1		15	8.87

(1) R_{FBT} = 100 kΩ

Selecting R_{FBT} value of 100 kΩ is recommended for most applications. A larger R_{FBT} consumes less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful feedback path PCB layout. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see *Layout*.

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7.3.2 Input Capacitor Selection

The TPSM265R1 requires a minimum of 1 µF of ceramic type input capacitance. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. TI recommends adding additional capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 2 includes a preferred list of capacitors by vendor.

Table 2. Recommended Input Capacitors(1)

VENDOR	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)
Murata	X7R	GCJ21BR71H105KA01L	0805	50	1
TDK	X7R	CGA4J3X7R1H105K125AB	0805	50	1
Murata	X7S	GRJ21BC72A105KE11L	0805	100	1
TDK	X7S	CGA4J3X7S2A105K125AB	0805	100	1
Murata	X7S	GCM31CC72A225KE02L	1206	100	2.2
TDK	X7S	C3216X7S2A225K160AB	1206	100	2.2
TDK	X7R	CGA5L3X7R1H475K160AE	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values

7.3.3 Output Capacitor Selection

The minimum amount of required output capacitance for the TPSM265R1 is 10 µF of ceramic type. TI recommends adding additional capacitance for applications with transient load requirements. See Table 3 for a preferred list of output capacitors by vendor.

Table 3. Recommended Output Capacitors(1)

VENDOR	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE (µF)(2)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10
TDK	X5R	C3225X5R1C226M	1210	16	22
Murata	X5R	GRM32ER61C226K	1210	16	22
TDK	X5R	C3216X5R1E226M160AB	1206	25	22
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22
TDK	X5R	C3225X5R1A476M	1210	10	47
Murata	X5R	GRM32ER61C476K	1210	16	47

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values

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7.3.4 Precision Enable (EN), Undervoltage Lockout (UVLO), and Hysteresis (HYS)

The EN pin provides precision ON and OFF control for the TPSM265R1. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. The simplest way to enable the TPSM265R1 is to connect EN directly to VIN. This allows the TPSM265R1 to start up when V_{IN} is within its valid operating range. An external logic signal can also be used to drive the EN input to toggle the output on and off and for system sequencing or protection.

The TPSM265R1 implements internal undervoltage lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage is below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 2.95 V (max) with a typical hysteresis of 300 mV.

If an application requires a higher UVLO threshold, the EN input supports adjustable UVLO by connecting a resistor divider from VIN to the EN pin. The EN pin connects to an internal comparator referenced to a 1.212-V bandgap voltage with 68-mV hysteresis. However, applications requiring specific power-up and power-down requirements, can program the hysteresis voltage independently using the HYS pin. Figure 27 shows the resistor divider connection to establish a precision UVLO level with fixed internal hysteresis. Figure 28 shows the resistor divider connection used to set the precision UVLO level as well as the adjustable hysteresis.

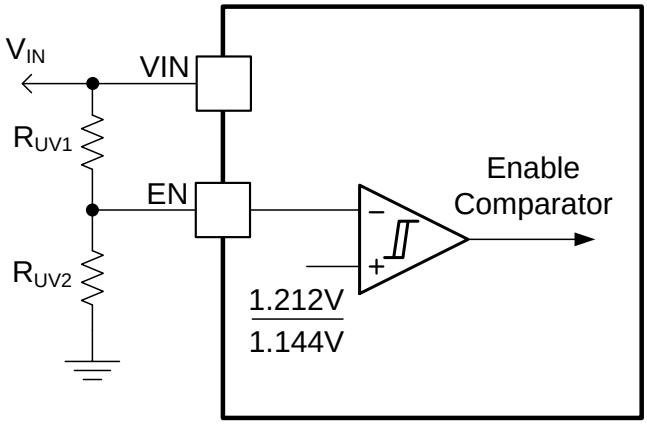


Figure 27. Programmable V_{IN} UVLO with Fixed Hysteresis

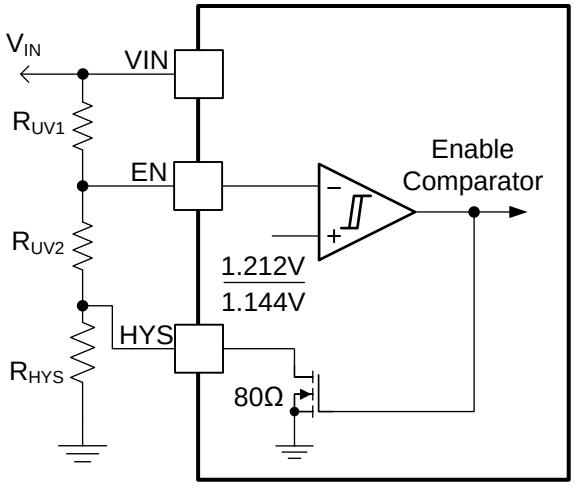


Figure 28. Programmable V_{IN} UVLO with Adjustable Hysteresis

Use Equation 2 and Equation 3 to calculate the input UVLO voltages turnon and turnoff voltages, respectively.

$$V_{IN(on)} = 1.212V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (2)$$

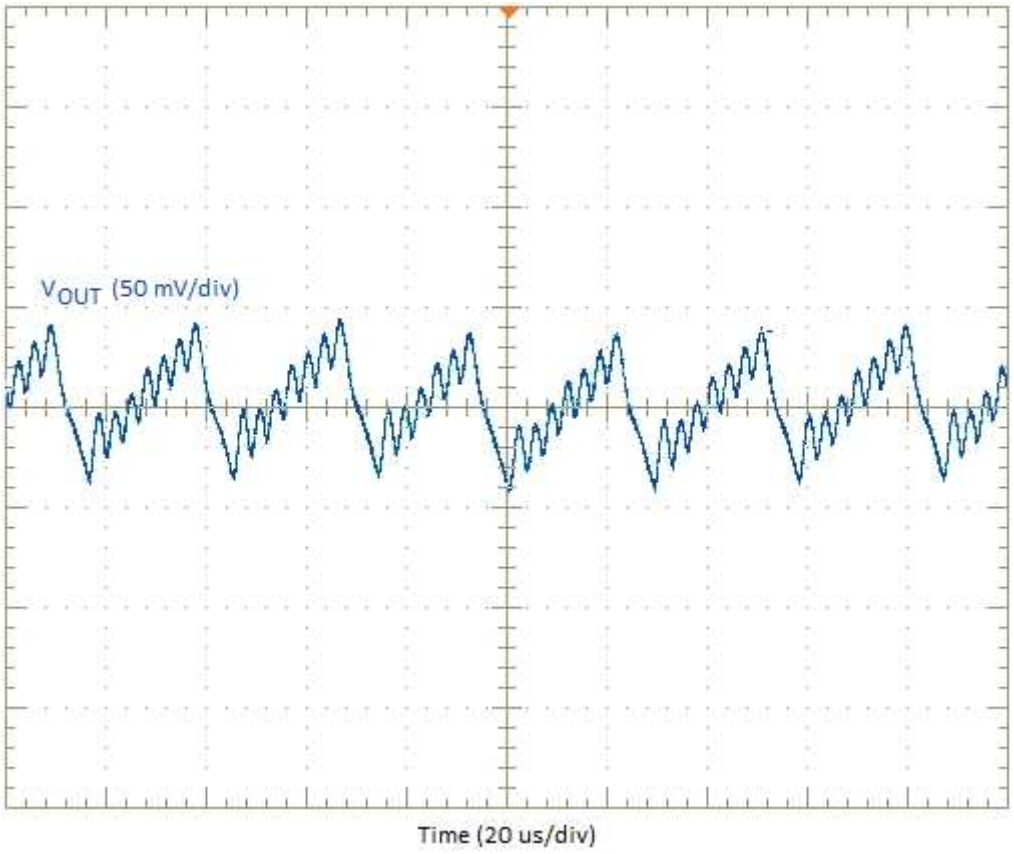
$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \quad (3)$$

There is also a low I_Q shutdown mode when EN is pulled below 0.6 V (typ). If EN is below this shutdown threshold, the internal LDO regulator powers off, shutting down the bias currents of the TPSM265R1. The TPSM265R1 operates in standby mode when the EN voltage is between the shutdown and precision enable thresholds.

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7.3.5 PFM Operation

The TPSM265R1 operates in Pulse Frequency Modulation (PFM) mode. The TPSM265R1 behaves as a hysteretic voltage regulator operating within upper and lower feedback regulation thresholds with typical 10 mV of hysteresis. Figure 29 is a representation of the relevant output voltage ripple waveform. The TPSM265R1 provides the required switching pulses to recharge the output capacitance, followed by a sleep period where most of the internal circuits are shut off. The load current is supported by the output capacitor during this time, and the TPSM265R1 current consumption approaches the sleep quiescent current of 10.5 μA (typ). The sleep period duration depends on load current and output capacitance.



V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 10 µF

R_{LOAD} = 50 Ω

Figure 29. Typical Output Voltage Ripple

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7.3.6 Power Good (PGOOD)

The TPSM265R1 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 12 V. Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

When the output voltage exceeds 94% of the setpoint, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 87% of the setpoint, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 µs.

7.3.7 Configurable Soft Start (SS)

The TPSM265R1 has a flexible and easy-to-use soft-start control pin, SS. The soft-start feature prevents inrush current when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is powered up or enabled. Selectable and adjustable start-up timing options include minimum delay (no soft-start), 900-µs internally fixed soft start, and an externally programmable soft start.

Leaving the SS pin open enables the internal soft-start control ramp with a soft-start interval of 900 µs. The soft-start time can be increased by connecting an external capacitor, C_{SS} from SS to GND. Applications with a large amount of output capacitance or higher output voltage can benefit from increasing the soft-start time. Longer soft-start time reduces the supply current needed to charge the output capacitors and supply any output loading. An internal current source, I_{SS}, of 10 µA charges C_{SS} and generates a ramp to control the ramp rate of the output voltage. Use Equation 4 to calculate the C_{SS} capacitance for a desired soft-start time, t_{SS}.

$$C_{SS}\left[nF\right] = 8.1 \cdot t_{SS}\left[ms\right] \tag{4}$$

C_{SS} is discharged by an internal FET when V_{OUT} is shut down by EN, UVLO, or thermal shutdown.

It is desirable in some applications for the output voltage to reach its nominal setpoint in the shortest possible time. Connecting a 100-kΩ resistor from SS to GND disables the soft-start circuit, and the TPSM265R1 operates in current limit during start-up to rapidly charge the output capacitance.

7.3.7.1 Prebiased Start-up

To prevent discharging of a prebiased output voltage, the TPSM265R1 is capable of start-up into prebiased output conditions. When a prebiased voltage is present at start-up, the TPSM265R1 waits until the soft-start ramp voltage is above the prebiased voltage before it begins switching and then follows the soft-start ramp to the regulation setpoint.

7.3.8 Over-current Protection (OCP)

The TPSM265R1 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

7.3.9 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C (typ) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TPSM265R1 restarts when the junction temperature falls to 160°C (typ).

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7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides ON and OFF control for the TPSM265R1. When V_{EN} is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4.6 µA at V_{IN} = 12 V. The TPSM265R1 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal bias rail LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 0.6 V and below the precision enable threshold (1.212 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UV threshold. The switching action and voltage regulation are not enabled until V_{EN} rises above the precision enable threshold.

7.4.3 Active Mode

The TPSM265R1 is in active mode when V_{EN} and the internal bias rail are above their relevant thresholds, FB has fallen below the lower hysteresis level, and boundary conduction mode is recharging the output capacitor to the upper hysteresis level. There is a 4-µs wake-up delay from sleep to active states.

7.4.4 Sleep Mode

The TPSM265R1 is in sleep mode when V_{EN} and the internal bias rail are above the relevant threshold levels, V_{FB} has exceeded the upper hysteresis level, and the output capacitor is sourcing the load current. In sleep mode, the TPSM265R1 operates with very low quiescent current.

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8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM265R1 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM265R1, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM265R1 power module.

As mentioned previously, the TPSM265R1 also integrates several optional features to meet system design requirements, including precision enable, UVLO, programmable soft-start, and PGOOD indicator. The application circuit detailed below shows TPSM265R1 configuration options suitable for several application use cases. Refer to the *TPSM265R1EVM* user's guides for more detail.

8.2 Typical Applications

8.2.1 Design: Wide V_{IN}, 5 V Output, 100 mA Output Current

Figure 30 shows the schematic diagram of a 5-V, 100-mA converter.

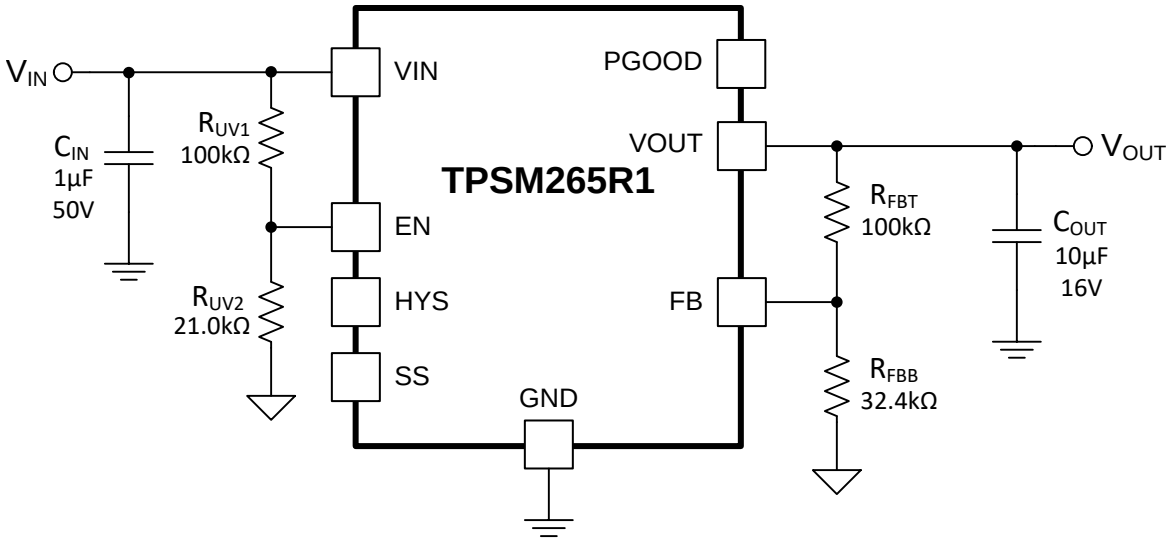


Figure 30. TPSM265R1 Typical Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters and follow the design procedures in *Detailed Design Procedure*.

Table 4. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	100 mA (50 Ω)

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM265R1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Setpoint

The output voltage of the TPSM265R1 device is externally adjustable using a resistor divider. The recommended value of R_{FBT} is 100 kΩ. The value for R_{FBB} can be selected from Table 1 or calculated using Equation 5:

$$R_{FBB} = \frac{1.223}{V_{OUT} - 1.223} \times R_{FBT} \tag{5}$$

For the desired output voltage of 5 V, the formula yields a value of 32.38 kΩ. Choose the closest available standard value of 32.4 kΩ for R_{FBB}.

8.2.1.2.3 Input Capacitors

The TPSM265R1 requires a minimum input capacitance of 1-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, a single, 1-µF, 50-V ceramic capacitor is selected.

8.2.1.2.4 Output Capacitor Selection

The TPSM265R1 requires a minimum of 10 µF of ceramic output capacitance for proper operation. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, a single 10-µF, 16-V, ceramic capacitor is used.

8.2.1.2.5 UVLO Programming

Applications requiring a higher UVLO threshold can benefit from applying a resistor divider on the EN pin. The values for the resistors can be calculated using Equation 6 and Equation 7.

$$V_{IN(on)} = 1.212V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \tag{6}$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \tag{7}$$

For this application, the UVLO was raised to 7 V. (R_{UV1} = 100 kΩ, R_{UV2} = 21.0 kΩ, and R_{HYS} = 0 (not used)).

8.2.1.2.6 Soft-Start Capacitor – C_{SS}

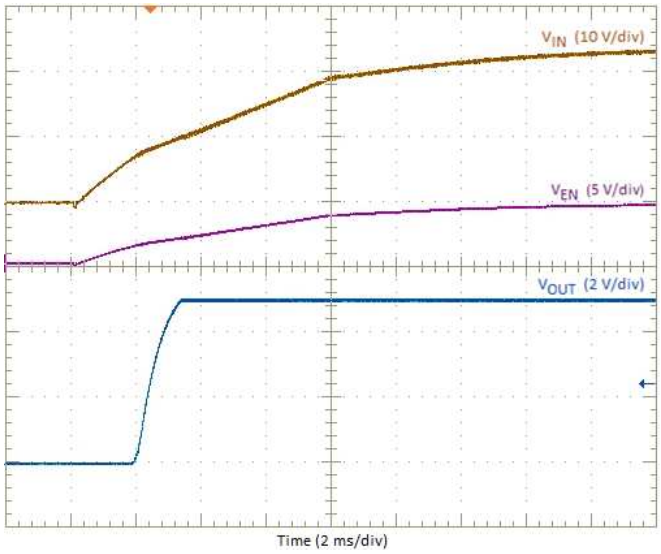
In this application, the SS pin was left open, resulting in a 900 µs soft-start rise time. Applications requiring a longer soft-start time can calculate the soft-start capacitor value using Equation 8:

$$C_{SS}[nF] = 8.1 \cdot t_{SS}[ms] \tag{8}$$

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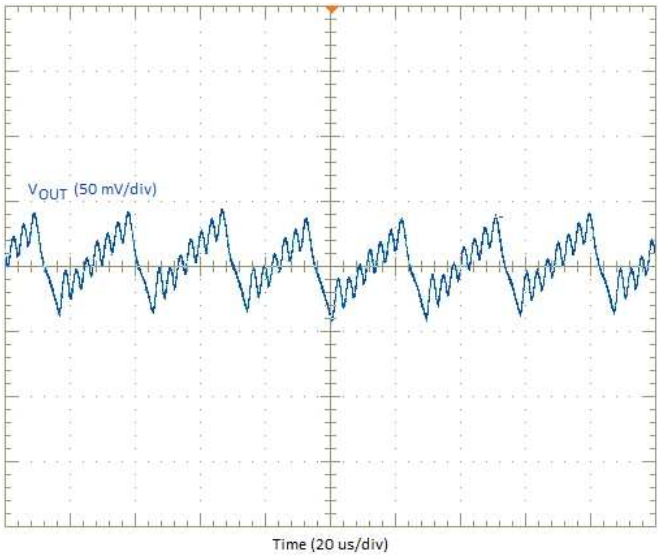
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8.2.1.3 Application Curves



V_{IN} = 24 V V_{OUT} = 5 V R_{LOAD} = 50 mΩ
R_{UV1} = 100 kΩ R_{UV2} = 21.0 kΩ

Figure 31. Start-up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 10 µF
R_{LOAD} = 50 Ω

Figure 32. Output Voltage Ripple

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9 Power Supply Recommendations

The TPSM265R1 is designed to operate from an input voltage supply range between 3 V and 65 V. This input supply must be able to provide the maximum input current and maintain a voltage above the set UVLO voltage. Ensure that the resistance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the TPSM265R1 supply rail to cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPSM265R1, additional bulk capacitance can be required in addition to the ceramic input capacitance. A 4.7-µF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 33 and Figure 34 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- **Connect all GND pins together using copper plane or thick copper traces.**
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place R_{FBT} and R_{FBB} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

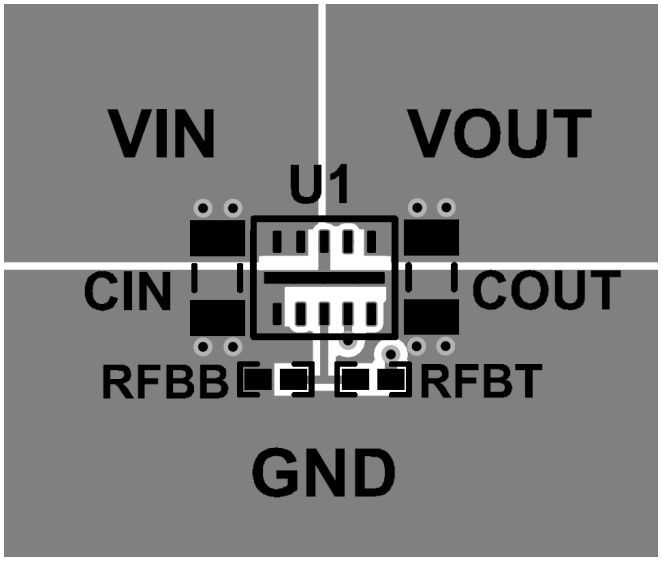


Figure 33. Typical Top-Layer Layout

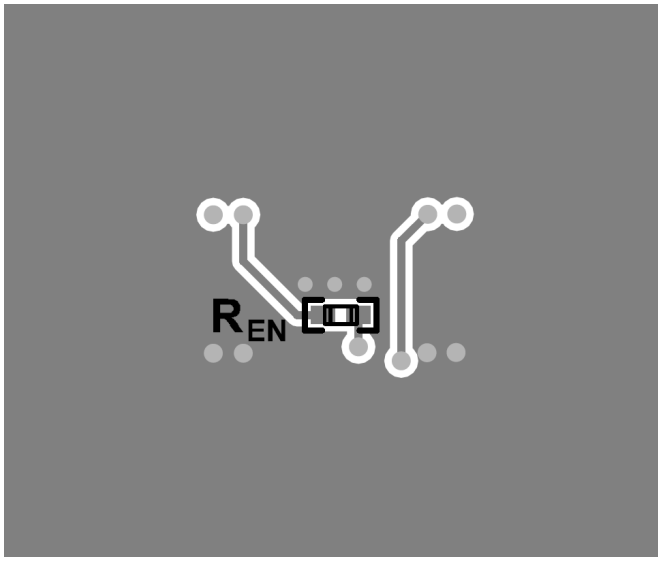


Figure 34. Typical Bottom-Layer Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

11.1.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For development support, see the following:

- For TI's reference design library, visit TIDesigns
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- To view a related device of this product, see the LM5166

11.1.3 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM265R1 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPSM265R1EVM User's Guide*
- Texas Instruments, *Using the TPSM265R1 in an Inverting Buck-Boost Topology Application Report*
- Texas Instruments, *Using New Thermal Metrics Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Community Resources (continued)

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

ADVANCE INFORMATION

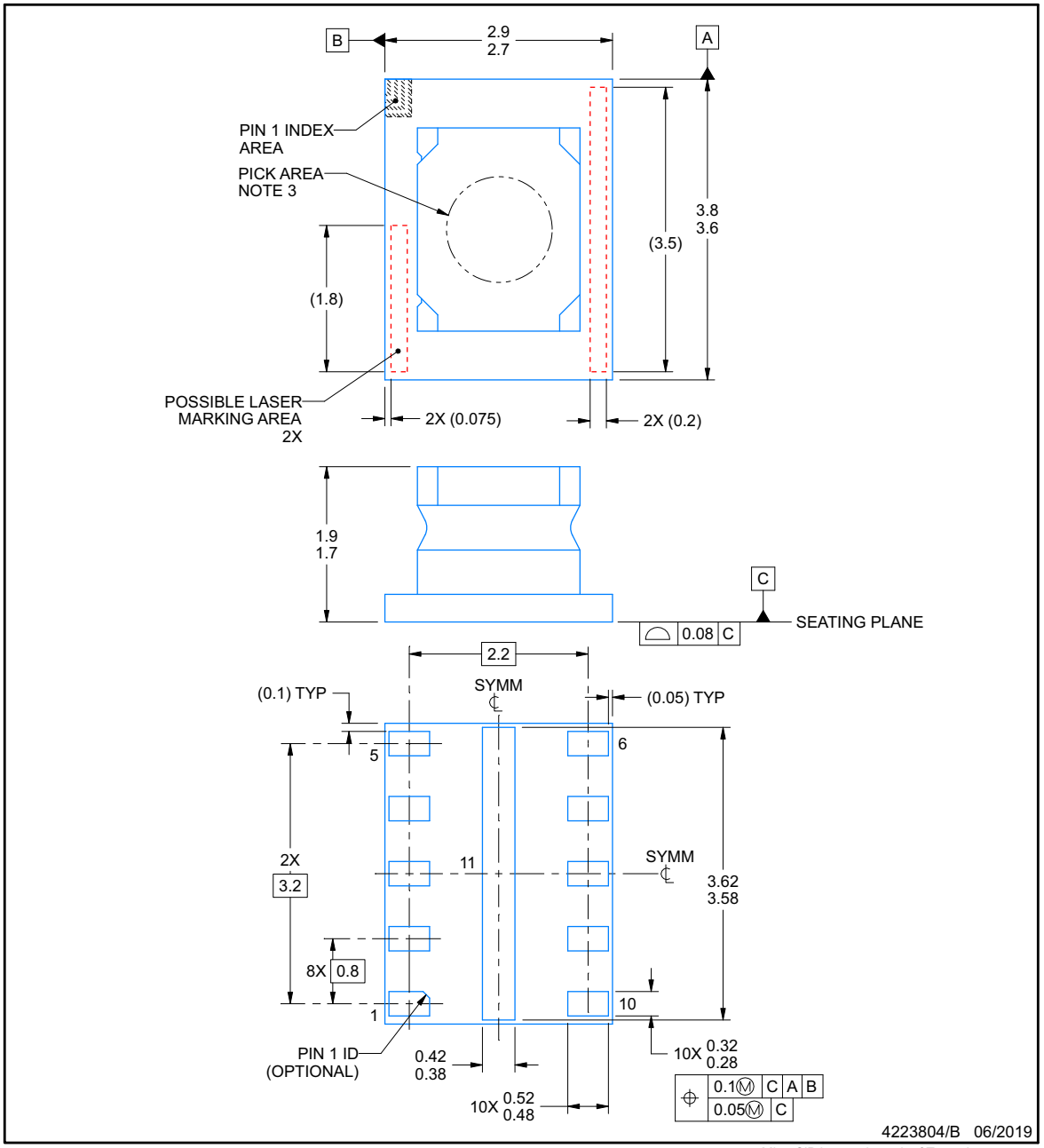
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PACKAGE OUTLINE

SIL0010C

uSIP™ - 1.9 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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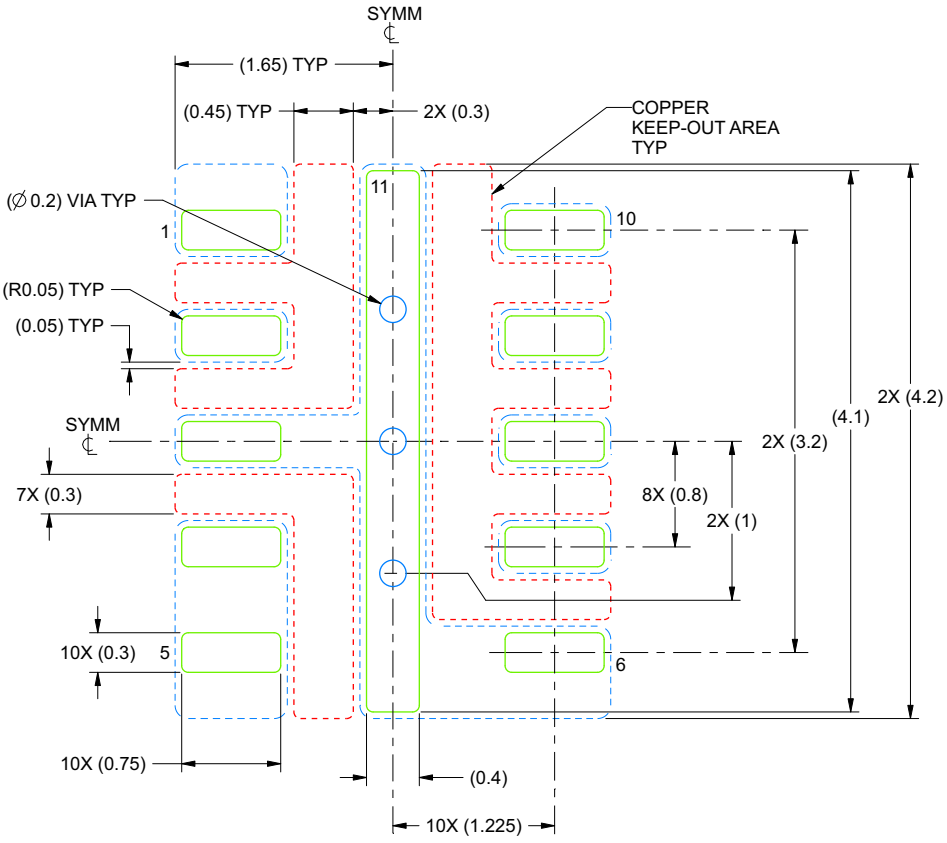
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

SIL0010C

uSIP™ - 1.9 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

5. This package is designed to be soldered to thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

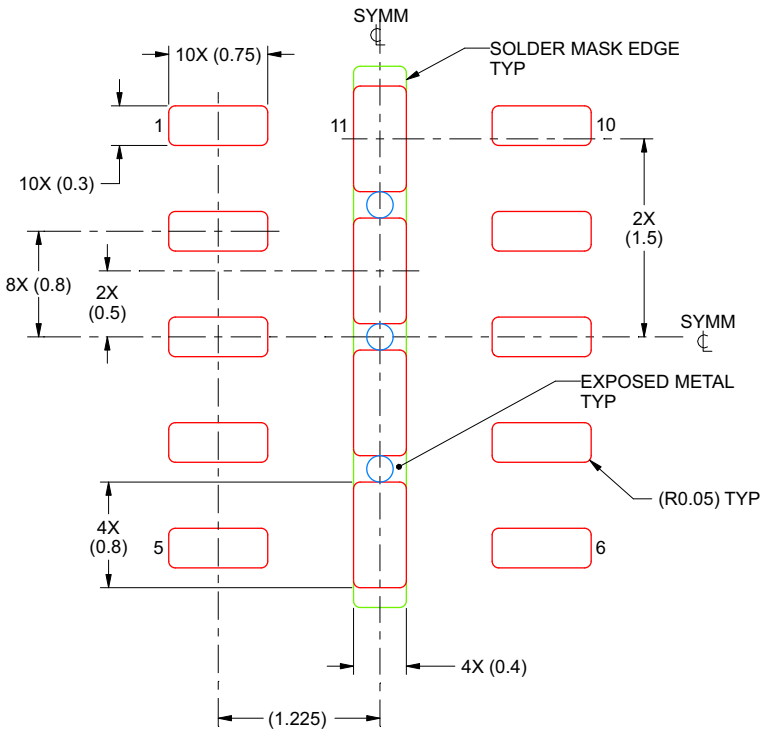
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EXAMPLE STENCIL DESIGN

SIL0010C

uSIP™ - 1.9 mm max height

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

78% SOLDER COVERAGE BY PRINTED AREA ON CENTER THERMAL PAD
SCALE:20X

4223804/B 06/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSM265R1SILR	ACTIVE	uSiP	SIL	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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