

SBVS010D – JANUARY 2000 – REVISED SEPTEMBER 2005

DMOS
500mA Low-Dropout Regulator

FEATURES

- **NEW DMOS TOPOLOGY:**
  Ultra Low Dropout Voltage:
  115mV Typ at 500mA and 3.3V Output
  Output Capacitor NOT Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE: 33μVrms**
- **HIGH ACCURACY: ±2% max**
- **HIGH EFFICIENCY:**
  I_{GND} = 1mA at I_{OUT} = 500mA
  Not Enabled: I_{GND} = 0.5μA
- **2.5V, 2.7V, 3.0V, 3.3V, 5.0V, AND ADJUSTABLE OUTPUT VERSIONS**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **OUTPUT VOLTAGE ERROR INDICATOR(1)**
- **SMALL SURFACE-MOUNT PACKAGES:**
  SOT223-5, DDPAK-5, SO-8

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

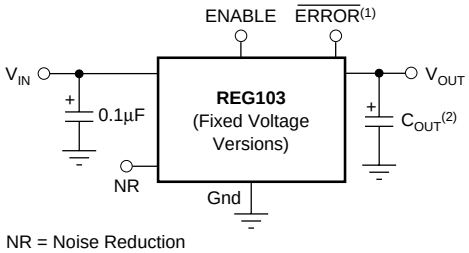
DESCRIPTION

The REG103 is a family of low-noise, low-dropout, linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 115mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1μF.

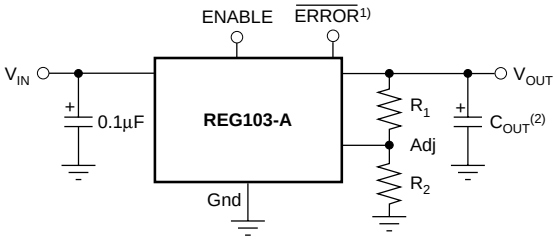
Typical ground pin current is only 1mA (at I_{OUT} = 500mA) and drops to 0.5μA in *not enabled* mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG103 has very low output noise (typically 33μVrms for V_{OUT} = 3.3V with C_{NR} = 0.01μF), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The SO-8 version of the REG103 has an $\overline{\text{ERROR}}$ pin that provides a *power good* flag, indicating the regulator is in regulation. The REG103 is well protected—internal circuitry provides a current limit that protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. In addition to the SO-8 package, the REG103 is also available in the DDPAK and the SOT223-5.



NR = Noise Reduction



NOTE: (1) SO-8 Package Only. (2) Optional.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Input Voltage, V_{IN}	–0.3V to 16V
Enable Input Voltage, V_{EN}	–0.3V to V_{IN}
Feedback Voltage, V_{FB}	–0.3V to 6.0V
NR Pin Voltage, V_{NR}	–0.3V to 6.0V
Error Flag Output	–0.3V to 6V
Error Flag Current	2mA
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (soldering, 3s, SO-8, SOT, and DDPAK)	+240°C
ESD Rating: HBM (V_{OUT} to GND)	1.5kV
HBM (All other pins)	2kV
CDM	500V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

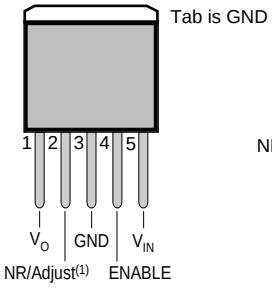
PRODUCT	V_{OUT}
REG103**xx-*yyyy/zzz***	**XX** is package designator. **YYYY** is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable). **ZZZ** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

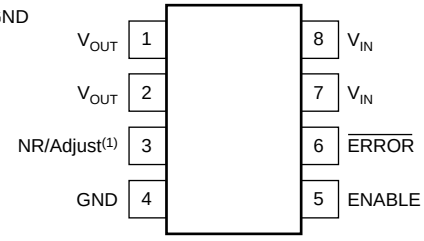
Top View

DDPAK-5



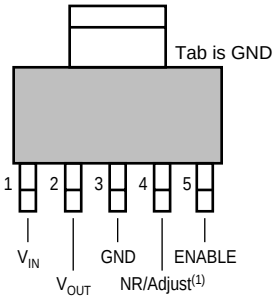
(F Package)

SO-8



(U Package)

SOT223-5



(G Package)

NOTE: (1) For REG103A-A: voltage setting resistor pin.
All other models: noise reduction capacitor pin.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_J = –40°C to +85°C.**

At T_J = +25°C, V_{IN} = V_{OUT} + 1V (V_{OUT} = 3.0V for REG103-A), V_{ENABLE} = 2V, I_{OUT} = 10mA, C_{NR} = 0.01µF, and C_{OUT} = 0.1µF(1), unless otherwise noted.

PARAMETER		CONDITION	REG103GA, UA, FA MIN	REG103GA, UA, FA TYP	REG103GA, UA, FA MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}					
REG103-2.5				2.5		V
REG103-2.7				2.7		V
REG103-3.0				3.0		V
REG103-3.3				3.3		V
REG103-5				5		V
REG103-A			V_{REF}		5.5	V
Reference Voltage	V_{REF}			1.295		V
Adjust Pin Current	I_{ADJ}			0.2	1	µA
Accuracy				±0.5	±2	%
T_J = –40°C to +85°C					**±2.8**	%
vs Temperature	**dV_{OUT}/dT**	**T_J = –40°C to +85°C**		**70**		ppm/°C
vs Line and Load		I_{OUT} = 10mA to 500mA, V_{IN} = (V_{OUT} + 0.7V) to 15V		±0.5	±2.5	%
T_J = –40°C to +85°C		**V_{IN} = (V_{OUT} + 0.9V) to 15V**			**±3.5**	**%**
DC DROPOUT VOLTAGE(2, 3)	V_{DROP}	I_{OUT} = 10mA		3	25	mV
For all models except 5V		I_{OUT} = 500mA		115	200	mV
For 5V model		I_{OUT} = 500mA		160	250	mV
For all models except 5V		**I_{OUT} = 500mA**			**230**	mV
T_J = –40°C to +85°C						
For 5V models		**I_{OUT} = 500mA**			**280**	mV
T_J = –40°C to +85°C						
VOLTAGE NOISE						
f = 10Hz to 100kHz	V_n					
Without C_{NR} (all models)		C_{NR} = 0, C_{OUT} = 0		30µVrms/V • V_{OUT}		µVrms
With C_{NR} (all fixed voltage models)		C_{NR} = 0.01µF, C_{OUT} = 10µF		10µVrms/V • V_{OUT}		µVrms
OUTPUT CURRENT						
Current Limit(4)	I_{CL}		550	700	950	mA
T_J = –40°C to +85°C			**500**		**1000**	mA
RIPPLE REJECTION						
f = 120Hz				65		dB
ENABLE CONTROL						
V_{ENABLE} HIGH (output enabled)	V_{ENABLE}		2		V_{IN}	V
V_{ENABLE} LOW (output disabled)			–0.2		0.5	V
I_{ENABLE} HIGH (output enabled)	I_{ENABLE}	V_{ENABLE} = 2V to V_{IN}, V_{IN} = 2.1V to 6.5(5)		1	100	nA
I_{ENABLE} LOW (output disabled)		V_{ENABLE} = 0V to 0.5V		2	100	nA
Output Disable Time				50		µs
Output Enable Soft Start Time				1.5		ms
$\overline{\text{ERROR}}$ FLAG(6)						
Current, Logic HIGH (open drain)—Normal Operation		V_{IN} = V_{ERROR} = V_{OUT} + 1V		0.1	10	µA
Voltage, Logic LOW—On Error		Sinking 500µA		0.2	0.4	V
THERMAL SHUTDOWN						
Junction Temperature						
Shutdown				150		°C
Reset from Shutdown				130		°C
GROUND PIN CURRENT						
Ground Pin Current	I_{GND}	I_{OUT} = 10mA		0.5	0.7	mA
		I_{OUT} = 500mA		1	1.3	mA
ENABLE Pin LOW		V_{ENABLE} ≤ 0.5V		0.5		µA
INPUT VOLTAGE	V_{IN}					
Operating Input Voltage Range(7)			2.1		15	V
Specified Input Voltage Range		V_{IN} > 2.7V	V_{OUT} + 0.7		15	V
T_J = –40°C to +85°C		**V_{IN} > 2.9V**	**V_{OUT} + 0.9**		**15**	V
TEMPERATURE RANGE						
Specified Range	T_J		–40		+85	°C
Operating Range			–55		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance						
DDPAK-5 Surface-Mount	θ_{JC}	Junction-to-Case		4		°C/W
SO-8 Surface-Mount	θ_{JA}	Junction-to-Ambient		150		°C/W
SOT223-5 Surface-Mount	θ_{JC}	Junction-to-Case		15		°C/W

NOTES: (1) The REG103 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.

(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at V_{IN} = V_{OUT} + 1V at fixed load.

(3) Not applicable for V_{OUT} less than 2.7V.

(4) Current limit is the output current that produces a 10% change in output voltage from V_{IN} = V_{OUT} + 1V and I_{OUT} = 10mA.

(5) For V_{IN} > 6.5V, see typical characteristic *V_{ENABLE} vs I_{ENABLE}*.

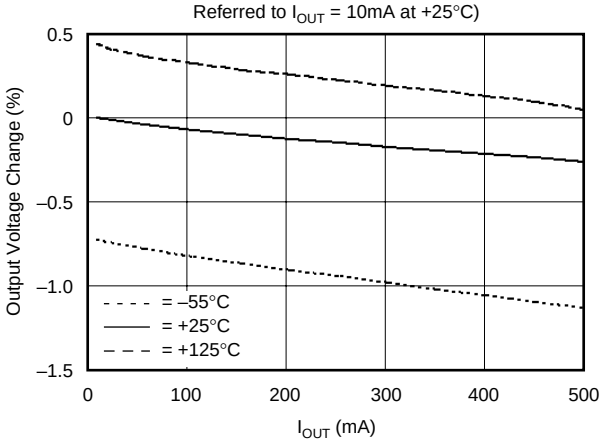
(6) Logic low indicates out-of-regulation condition by approximately 10%, or thermal shutdown.

(7) The REG103 no longer regulates when V_{IN} < V_{OUT} + $V_{DROP\ (MAX)}$. In drop-out or when the input voltage is between 2.7V and 2.1V, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at T_J = +25°C. See typical characteristic.

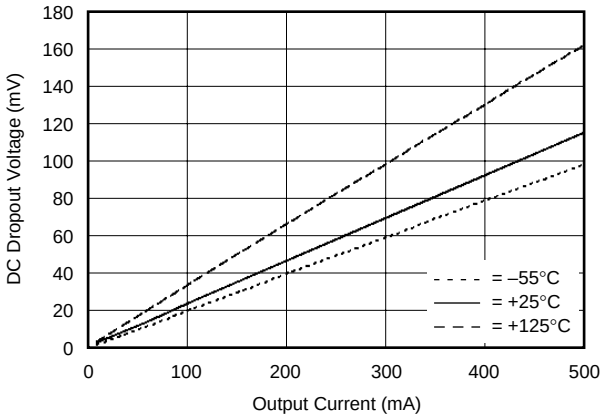
TYPICAL CHARACTERISTICS

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

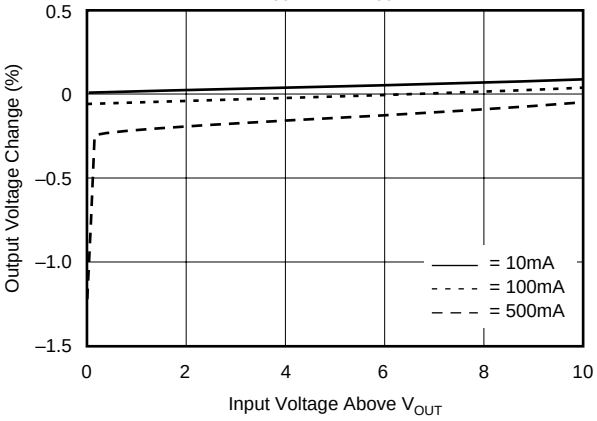
OUTPUT VOLTAGE CHANGE vs I_{OUT}
(V_{IN} = V_{OUT} + 1V, Output Voltage % Change
Referred to I_{OUT} = 10mA at +25°C)



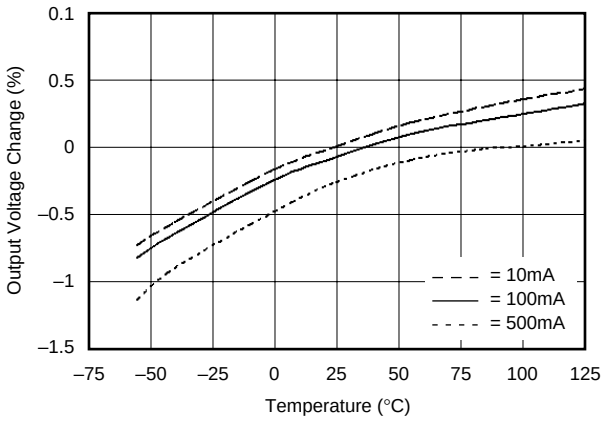
DC DROPOUT VOLTAGE vs OUTPUT CURRENT



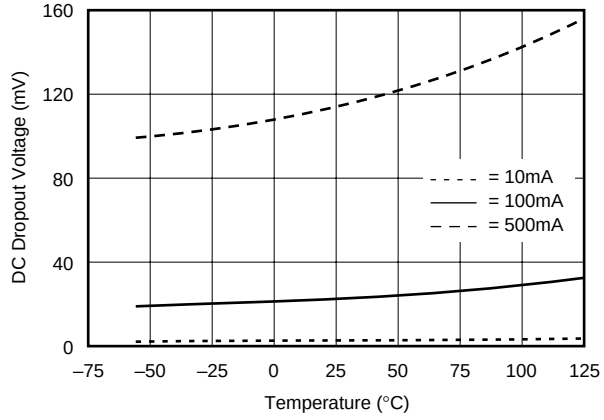
OUTPUT VOLTAGE CHANGE vs V_{IN}
(Output Voltage % Change Referred
to V_{IN} = V_{OUT} + 1V at I_{OUT} = 10mA)



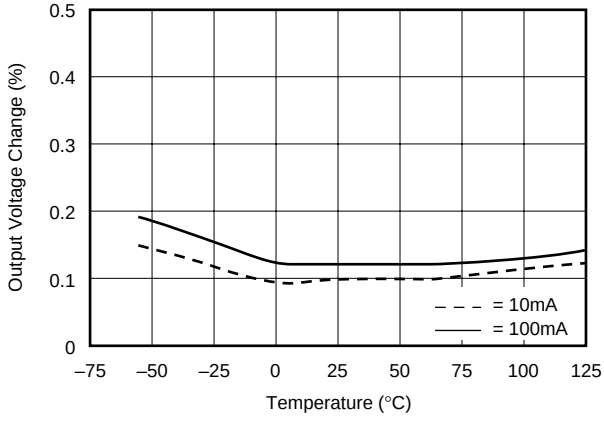
OUTPUT VOLTAGE vs TEMPERATURE
(Output Voltage % Change Referred to
I_{OUT} = 10mA at +25°C)



DC DROPOUT VOLTAGE vs TEMPERATURE



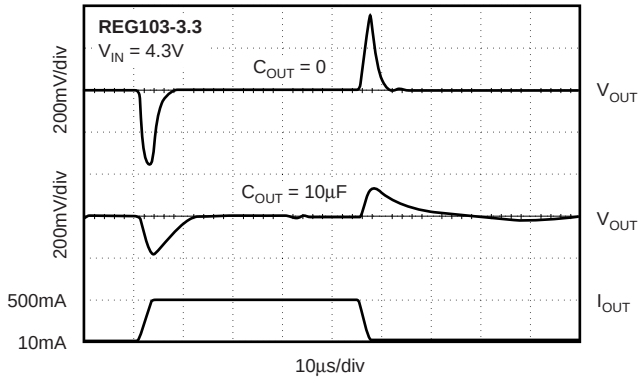
LINE REGULATION vs TEMPERATURE
(V_{IN} = V_{OUT} + 1V to V_{IN} = 15V)



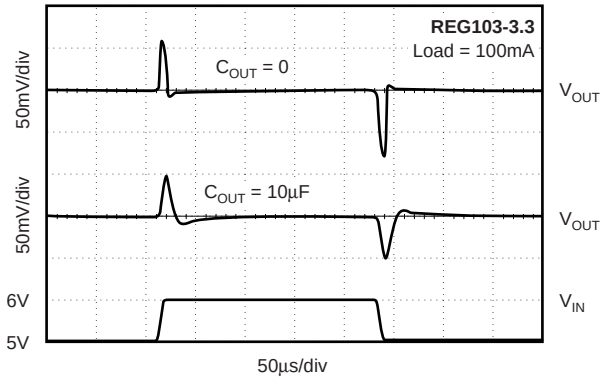
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

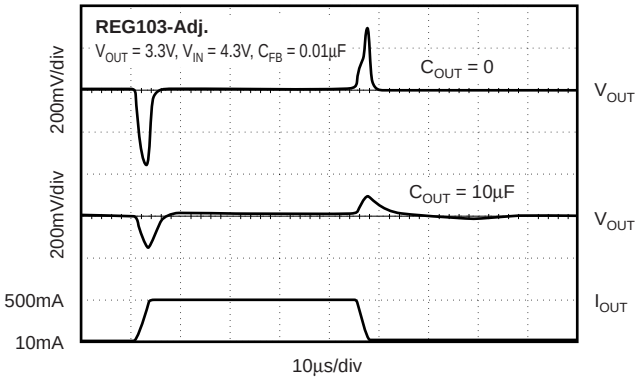
LOAD TRANSIENT RESPONSE



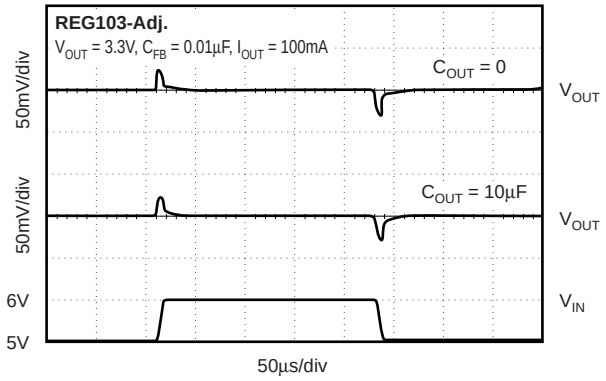
LINE TRANSIENT RESPONSE



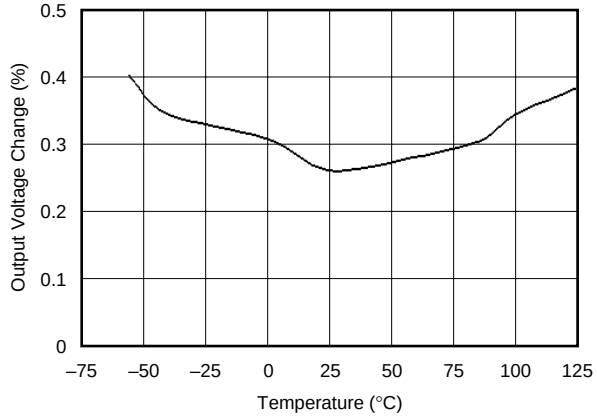
LOAD TRANSIENT RESPONSE



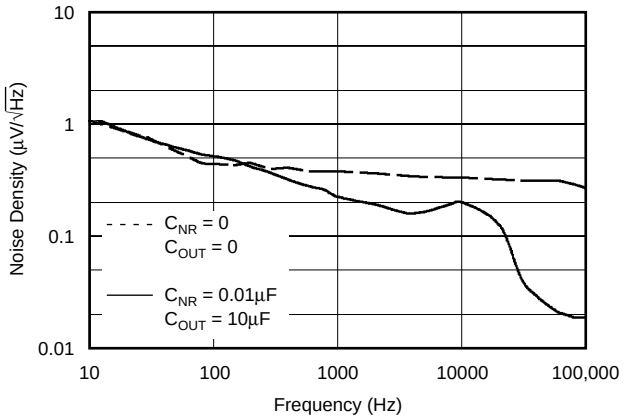
LINE TRANSIENT RESPONSE



LOAD REGULATION vs TEMPERATURE
(V_{IN} = V_{OUT} + 1V and 10mA < I_{OUT} < 500mA)



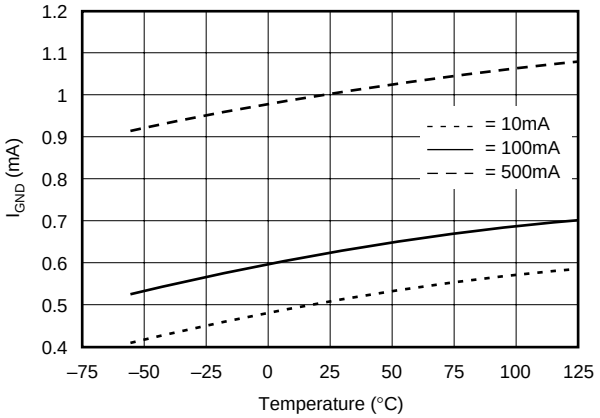
OUTPUT NOISE DENSITY



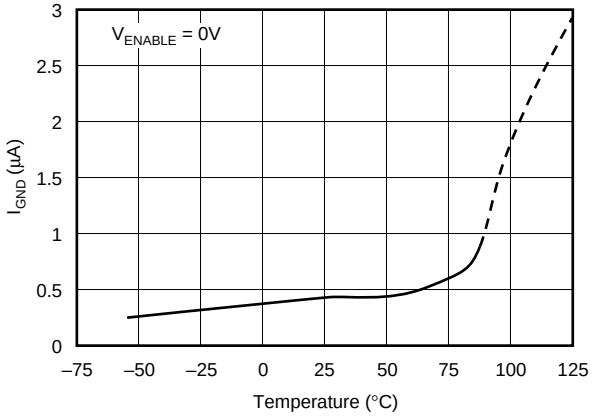
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

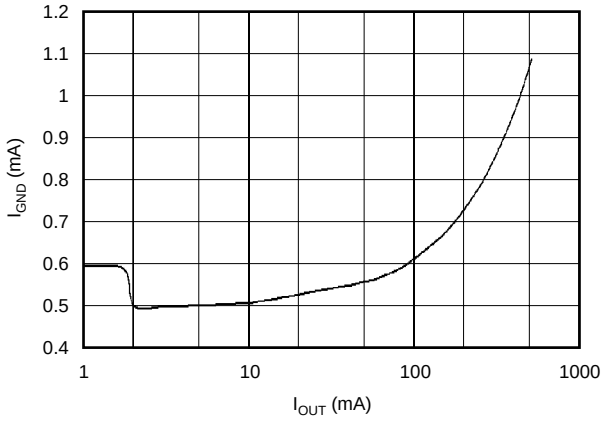
GROUND PIN CURRENT vs TEMPERATURE



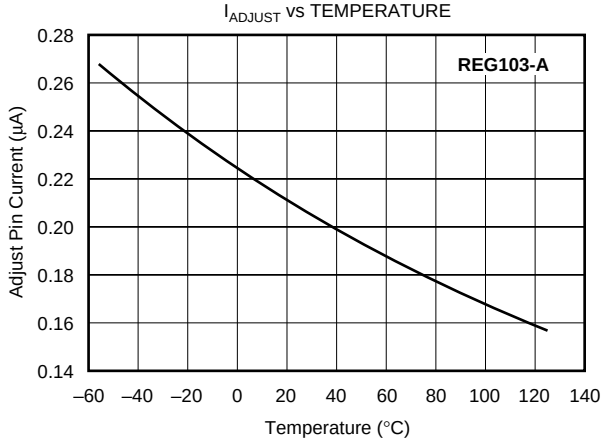
GROUND PIN CURRENT, NOT ENABLED vs TEMPERATURE



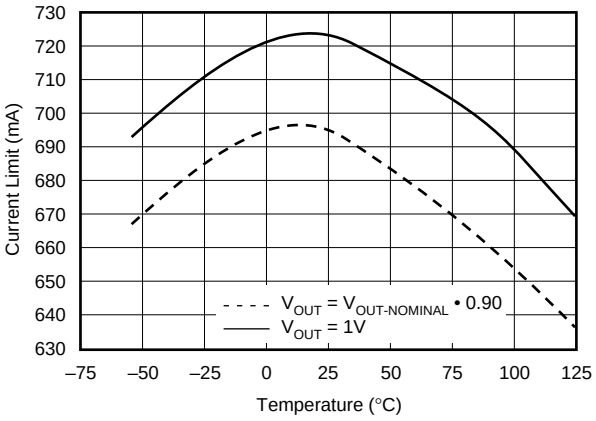
GROUND PIN CURRENT vs I_{OUT}



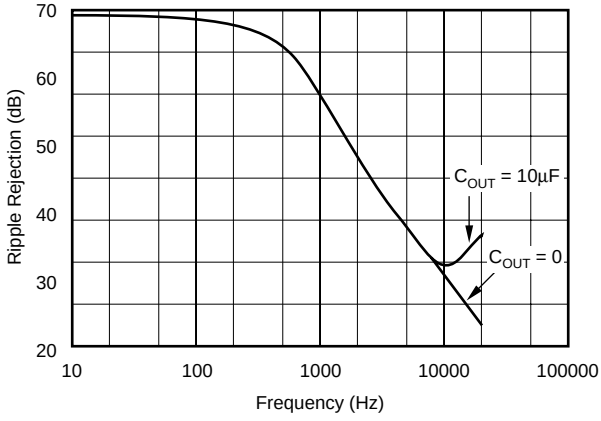
I_{ADJUST} vs TEMPERATURE



CURRENT LIMIT vs TEMPERATURE



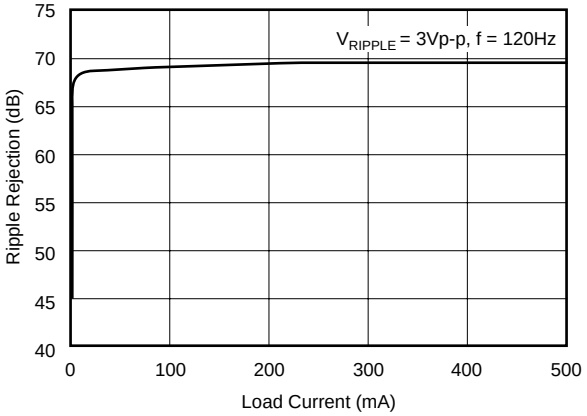
RIPPLE REJECTION vs FREQUENCY



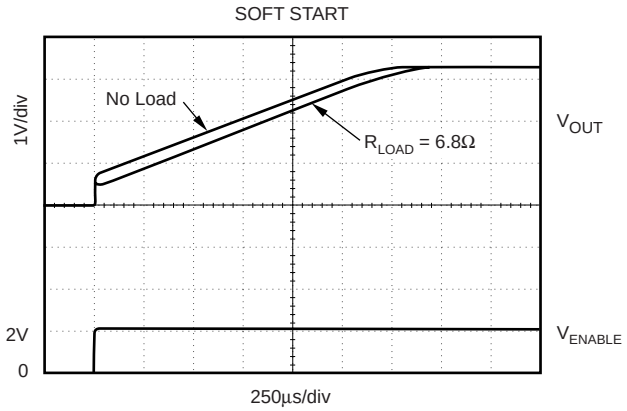
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 2V, unless otherwise noted.

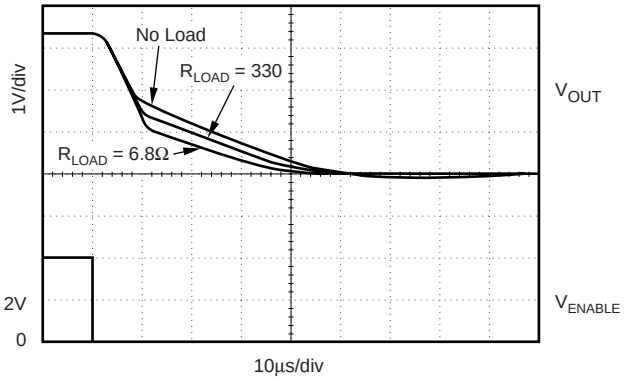
RIPPLE REJECTION vs I_{OUT}



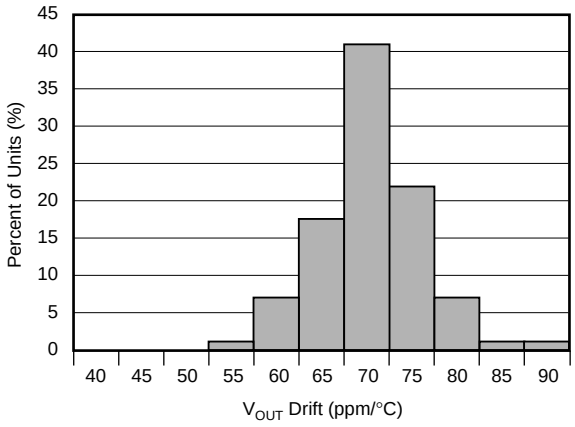
SOFT START



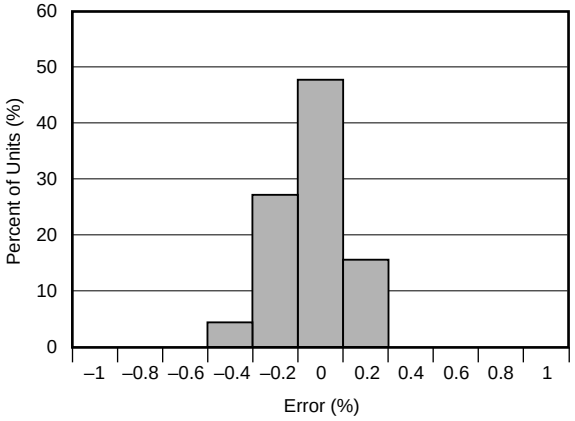
OUTPUT DISABLE TIME



OUTPUT VOLTAGE DRIFT HISTOGRAM



OUTPUT VOLTAGE ACCURACY HISTOGRAM



BASIC OPERATION

The REG103 series is a family of LDO (Low Drop-Out) linear regulators. The family includes five fixed output versions (2.5V to 5.0V) and an adjustable output version. An internal DMOS power device provides low dropout regulation with near constant ground pin current (largely independent of load and drop-out conditions) and very fast line and load transient response. All versions include internal current limit and thermal shutdown circuitry.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG103A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2. The SO-8 package provides two pins each for V_{IN} and V_{OUT}. Both sets of pins **MUST** be used and connected adjacent to the device.

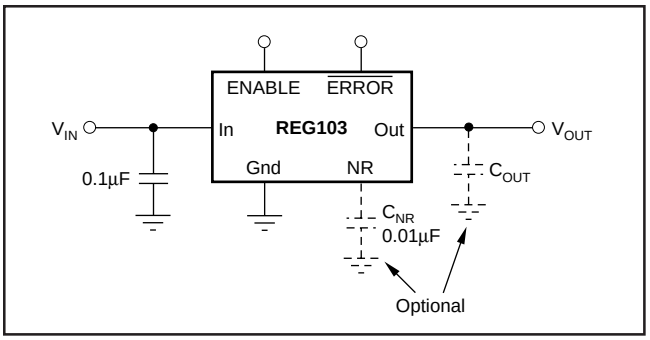


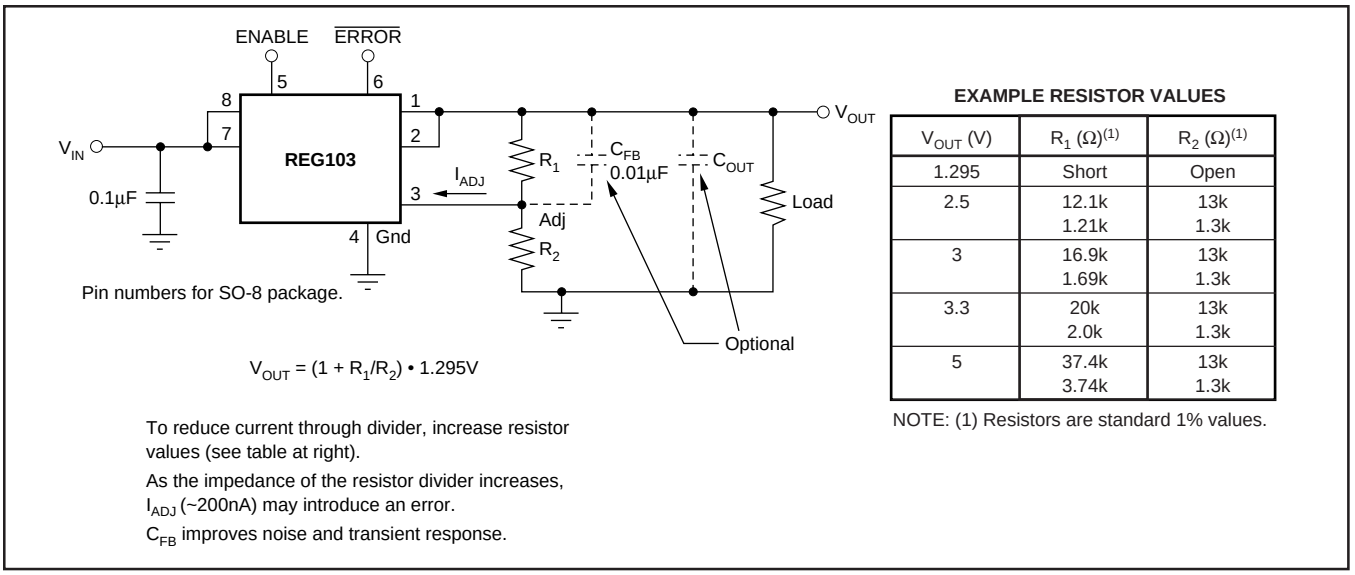
FIGURE 1. Fixed Voltage Nominal Circuit for REG103.

None of the versions require an output capacitor for regulator stability. The REG103 will accept any output capacitor type less than 1µF. For capacitance values larger than 1µF, the effective ESR should be greater than 0.1Ω. This minimum ESR value includes parasitics such as printed circuit board traces, solder joints, and sockets. A minimum 0.1µF low ESR capacitor connected to the input supply voltage is recommended.

INTERNAL CURRENT LIMIT

The REG103 internal current limit has a typical value of 700mA. A fold-back feature limits the short-circuit current to a typical short-circuit value of 40mA. This circuit will protect the regulator from damage under all load conditions. A typical characteristic of V_{OUT} versus I_{OUT} is given in Figure 3a.

Care should be taken in high current applications to avoid ground currents flowing in the circuit board traces causing voltage drops between points on the circuit. If voltage drops occur on the circuit board ground that causes the load ground voltage to be much lower than the ground voltage seen by the ground pin on the REG103, the foldback current may approach zero and the REG103 may not start up. In these types of applications, a large value resistor can be placed between V_{IN} and V_{OUT} to help "boost" up the output of the REG103 during start-up, see Figure 3b. The value for the "boost" resistor should be chosen so that the current through the "boost" resistor is less than the minimum load current: $R_{BOOST} > (V_{IN} - V_{OUT})/I_{LOAD}$. Typically, a good value for a "boost" resistor is 5kΩ.



EXAMPLE RESISTOR VALUES

V_{OUT} (V)	R_1 (Ω)(1)	R_2 (Ω)(1)
1.295	Short	Open
2.5	12.1k 1.21k	13k 1.3k
3	16.9k 1.69k	13k 1.3k
3.3	20k 2.0k	13k 1.3k
5	37.4k 3.74k	13k 1.3k

NOTE: (1) Resistors are standard 1% values.

FIGURE 2. Adjustable Voltage Circuit for REG103A.

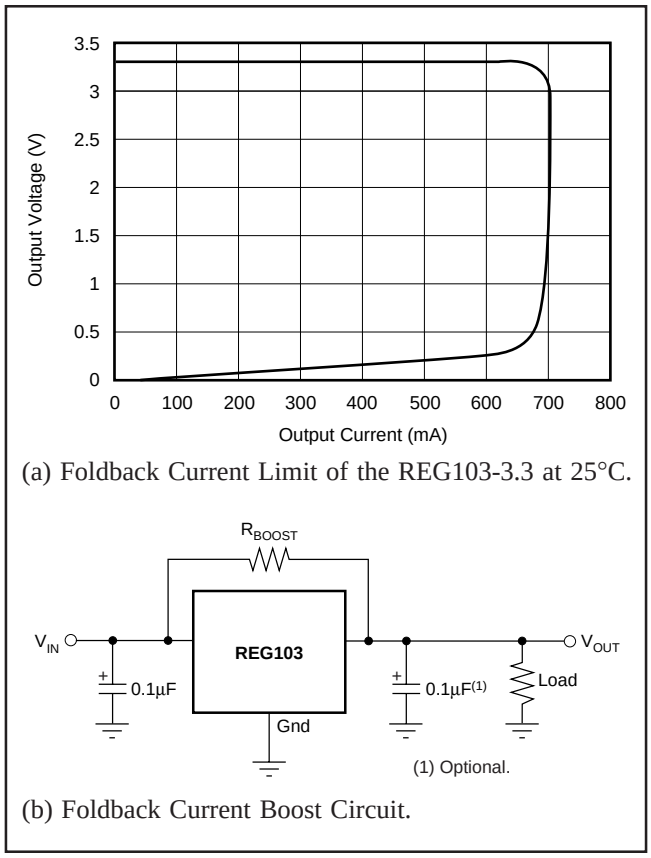


FIGURE 3. Foldback Current Limit and Boost Circuit.

ENABLE

The ENABLE pin allows the regulator to be turned on and off. This pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 0.5µA. When not used, the ENABLE pin may be connected to V_{IN}.

Internal to the part, the ENABLE pin is connected to an input resistor-zener diode circuit, as shown in Figure 4, creating a nonlinear input impedance. The ENABLE Pin Current versus Applied Voltage relationship is shown in Figure 5. When the ENABLE pin is connected to a voltage greater than 10V, a series resistor may be used to limit the current.

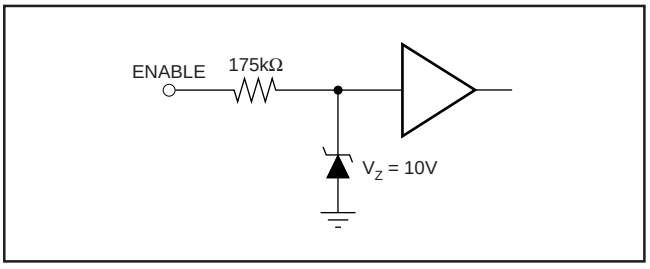


FIGURE 4. ENABLE Pin Equivalent Input Circuit.

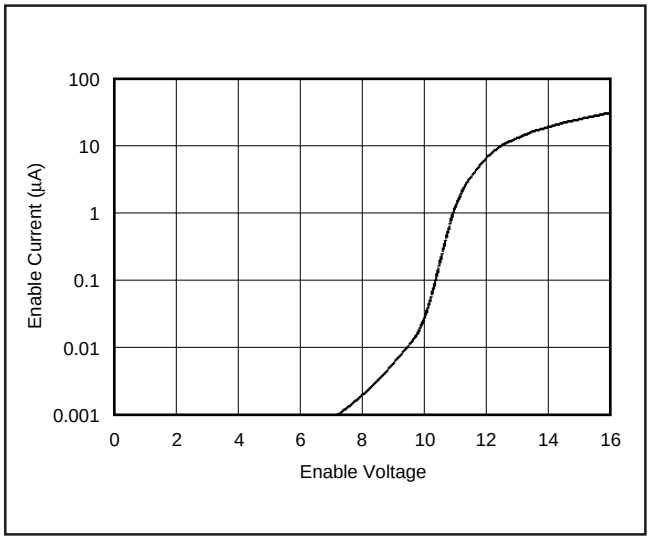


FIGURE 5. ENABLE Pin Current versus Applied Voltage.

$\overline{\text{ERROR}}$ FLAG

The error indication pin, only available on the SO-8 package version, provides a fault indication out-of-regulation condition. During a fault condition, $\overline{\text{ERROR}}$ is pulled LOW by an open drain output device. The pin voltage, in the fault state, is typically less than 0.2V at 500µA.

A fault condition is indicated when the output voltage differs (either above or below) from the specified value by approximately 10%. Figure 6 shows a typical fault-monitoring application.

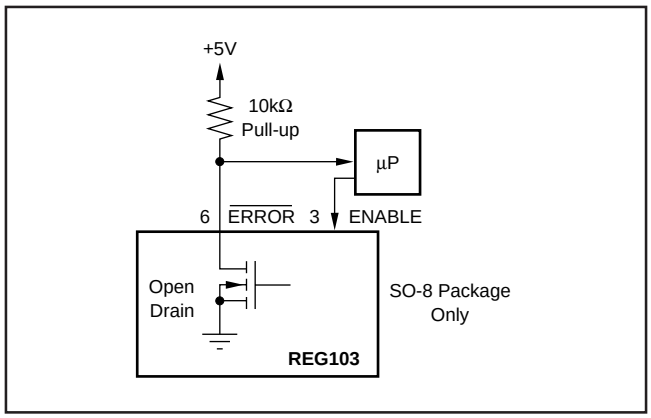


FIGURE 6. $\overline{\text{ERROR}}$ Pin Typical Fault-Monitoring Circuit.

OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage, V_{REF}, for the REG103. This reference is the dominant noise source within the REG103. It generates approximately 45µVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 45\mu Vrms \frac{R_1 + R_2}{R2} = 45\mu Vrms \bullet \frac{V_{OUT}}{V_{REF}}$$

Since the value of V_{REF} is 1.295V, this relationship reduces to:

$$V_N = 35 \frac{\mu Vrms}{V} \bullet V_{OUT}$$

Connecting a capacitor, C_{NR}, from the Noise-Reduction (NR) pin to ground, can reduce the output noise voltage. Adding C_{NR}, as shown in Figure 7, forms a low-pass filter for the voltage reference. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 3.5, as shown in Figure 8.

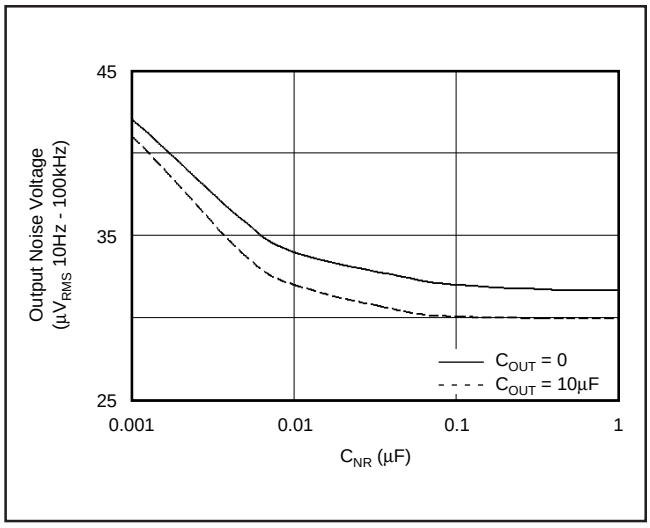


FIGURE 8. Output Noise versus Noise-Reduction Capacitor.

The REG103 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB}, connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. Figure 9 shows improved output noise performance for two capacitor combinations.

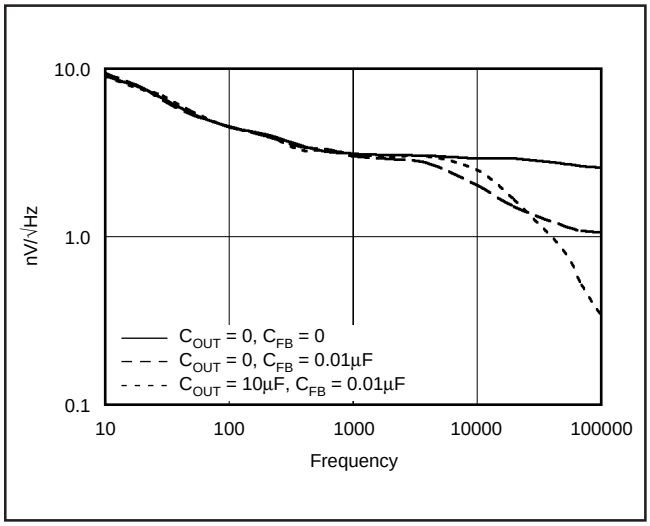


FIGURE 9. Output Noise Density on Adjustable Versions.

The REG103 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN}. The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator.

DROP-OUT VOLTAGE

The REG103 uses an N-channel DMOS as the "pass" element. When the input voltage is within a few hundred millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of V_{IN} to V_{OUT}, the regulator's input-to-output resistance is the Rds_{ON} of the DMOS pass element (typically 230mΩ). For static (DC) loads, the REG103 will typically maintain regulation down to V_{IN} to V_{OUT} voltage drop of 115mV at full-rated output current. In Figure 10, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent drop-out under DC load conditions.

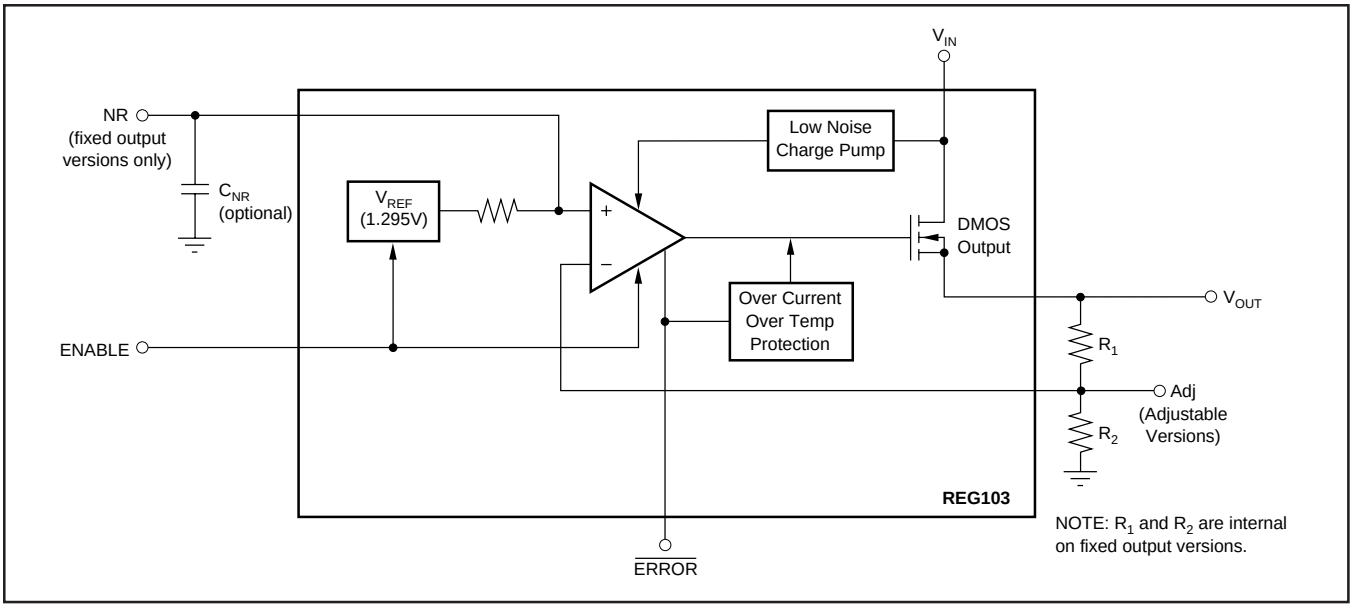


FIGURE 7. Block Diagram.

For large step changes in load current, the REG103 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this "transient drop-out" region is shown as the top line in Figure 10. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

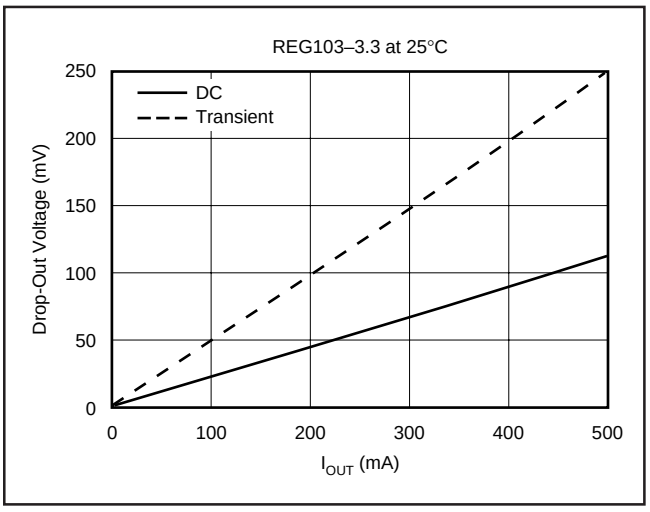


FIGURE 10. Transient and DC Dropout.

In the transient dropout region between "DC" and "Transient", transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available "headroom" V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with V_{IN} to V_{OUT} voltage drop close to DC dropout levels), the REG103 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG103 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 10nF) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

THERMAL PROTECTION

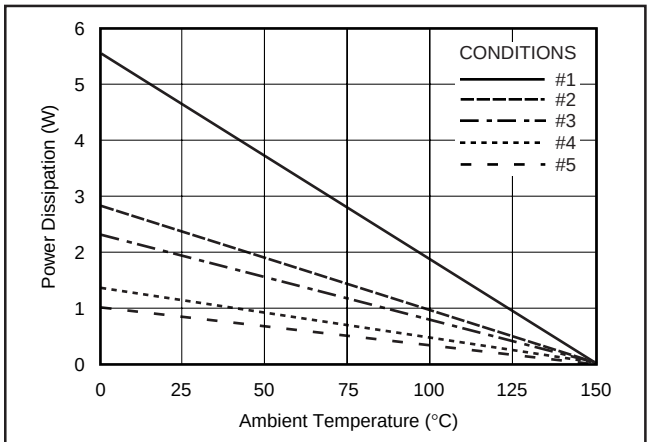
Power dissipated within the REG103 will cause the junction temperature to rise. The REG103 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 150°C, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG103 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG103 into thermal shutdown will degrade reliability.

POWER DISSIPATION

The REG103 is available in three different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 11. In all cases, the PCB copper area is bare copper, free of solder-resist mask, and not solder plated. All examples are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.



CONDITION	PACKAGE	PCB AREA	θ_{JA}
1	DDPAK	4in² Top Side Only	27°C/W
2	SOT-223	4in² Top Side Only	53°C/W
3	DDPAK	None	65°C/W
4	SOT-223	0.5in² Top Side Only	110°C/W
5	SO-8	None	150°C/W

FIGURE 11. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

REGULATOR MOUNTING

The tab of both packages is electrically connected to ground. For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation. Figure 12 shows typical thermal resistance from junction to ambient as a function of the copper area for the DDPAK.

Although the tabs of the DDPAK and the SOT-223 are electrically grounded, they are not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG103 devices are presented in the Application Bulletin "Solder Pad Recommendations for Surface-Mount Devices" (SBFA015), available from the Texas Instruments web site (www.ti.com).

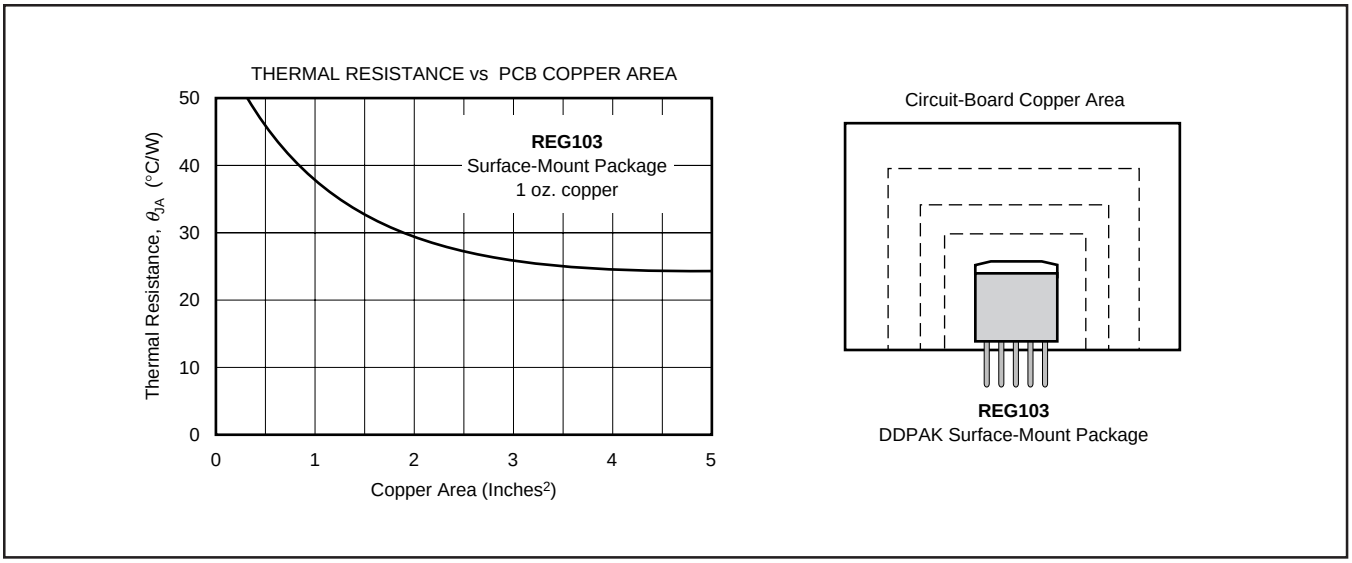


FIGURE 12. Thermal Resistance versus PCB Area for the Five-Lead DDPAK.

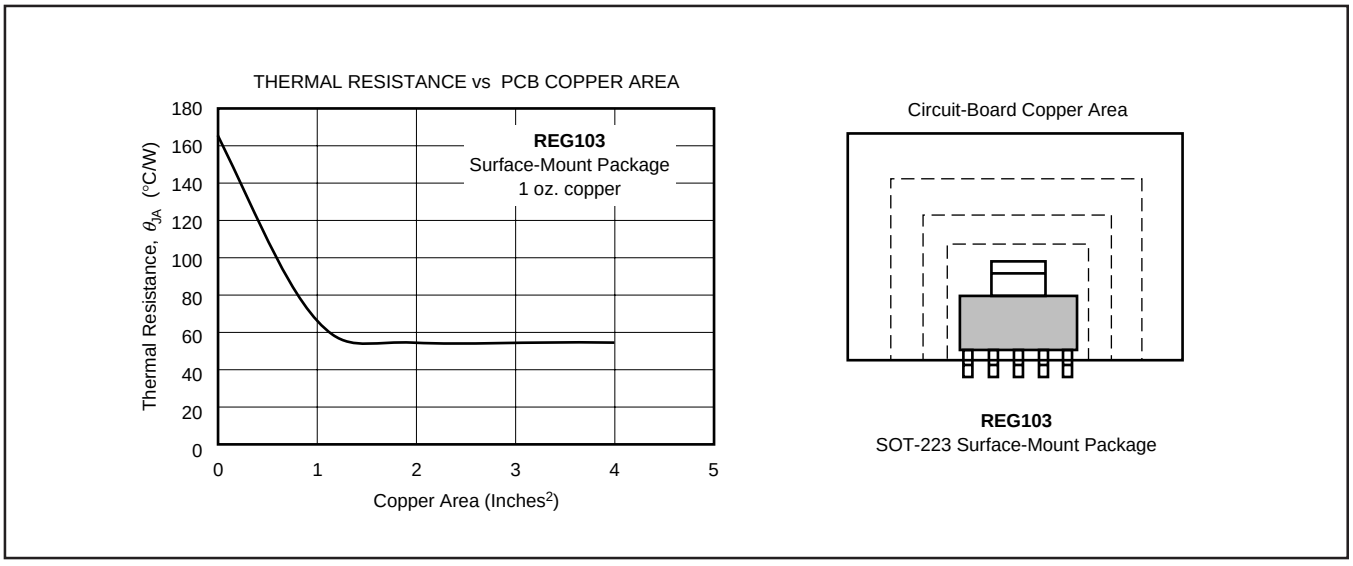


FIGURE 13. Thermal Resistance versus PCB Area for the Five-Lead SOT-223.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG103FA-2.5/500	NRND	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5	
REG103FA-2.5/500G3	NRND	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5	
REG103FA-2.5KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5	Samples
REG103FA-2.5KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-2.5	Samples
REG103FA-3.3KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-3.3	Samples
REG103FA-5KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-5	Samples
REG103FA-5KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-5	Samples
REG103FA-A/500	NRND	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A	
REG103FA-AKTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN | Call TI	Level-2-260C-1 YEAR	-40 to 85	REG 103FA-A	Samples
REG103GA-2.5	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G25	Samples
REG103GA-2.5G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G25	Samples
REG103GA-3.3	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33	Samples
REG103GA-3.3/2K5	NRND	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33	
REG103GA-3.3/2K5G4	NRND	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33	
REG103GA-3.3G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G33	Samples
REG103GA-5	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G50	Samples
REG103GA-5/2K5	NRND	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	R103G50	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG103GA-5G4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103G50	Samples
REG103GA-A	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA	Samples
REG103GA-A/2K5	NRND	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA	
REG103GA-A/2K5G4	NRND	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA	
REG103GA-AG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	R103GA	Samples
REG103UA-2.5	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25	Samples
REG103UA-2.5/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U25	Samples
REG103UA-3.3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4	Samples
REG103UA-3.3/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103UA4	
REG103UA-5	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U50	Samples
REG103UA-5/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U50	
REG103UA-A	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A	Samples
REG103UA-A/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A	
REG103UA-AG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 103U-A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

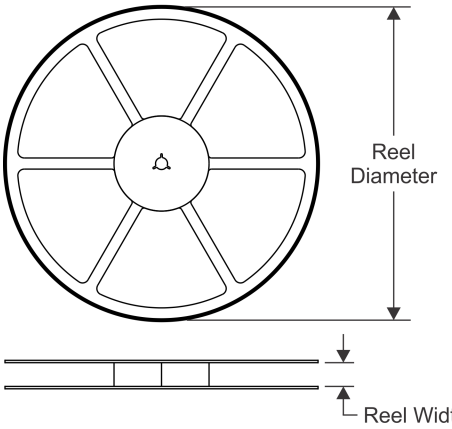
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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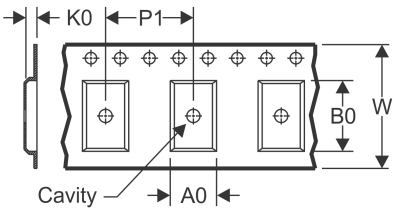
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

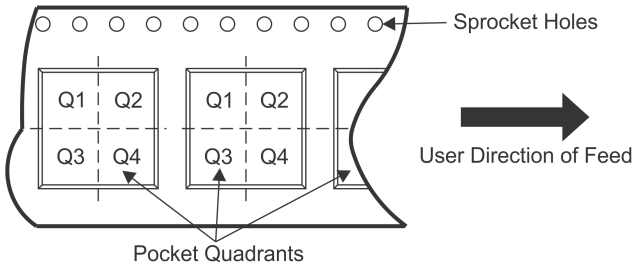


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

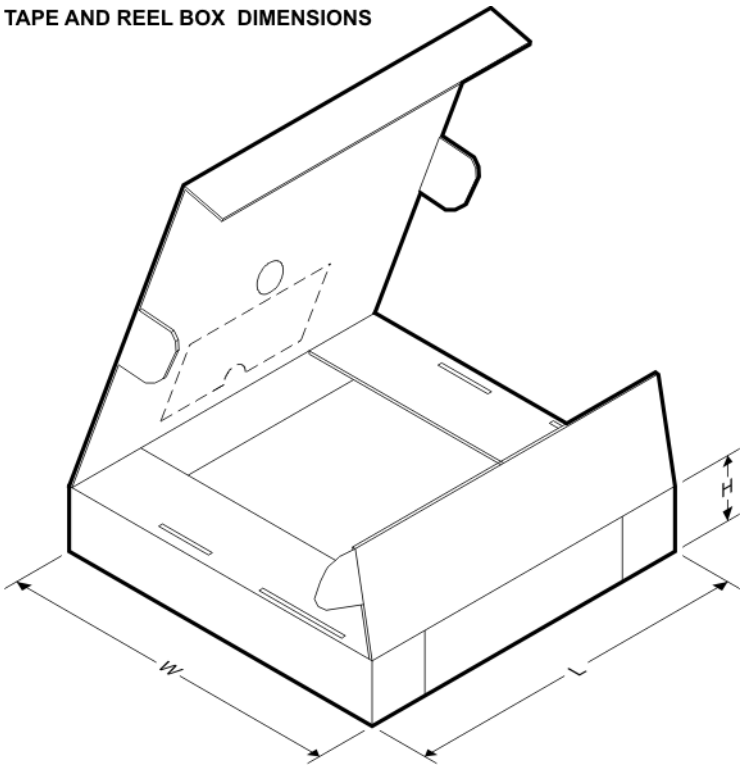
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG103FA-2.5/500	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG103FA-2.5KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG103FA-3.3KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG103FA-5KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG103FA-A/500	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG103FA-AKTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
REG103GA-3.3/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG103GA-A/2K5	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
REG103UA-2.5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG103UA-3.3/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG103UA-5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG103UA-A/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

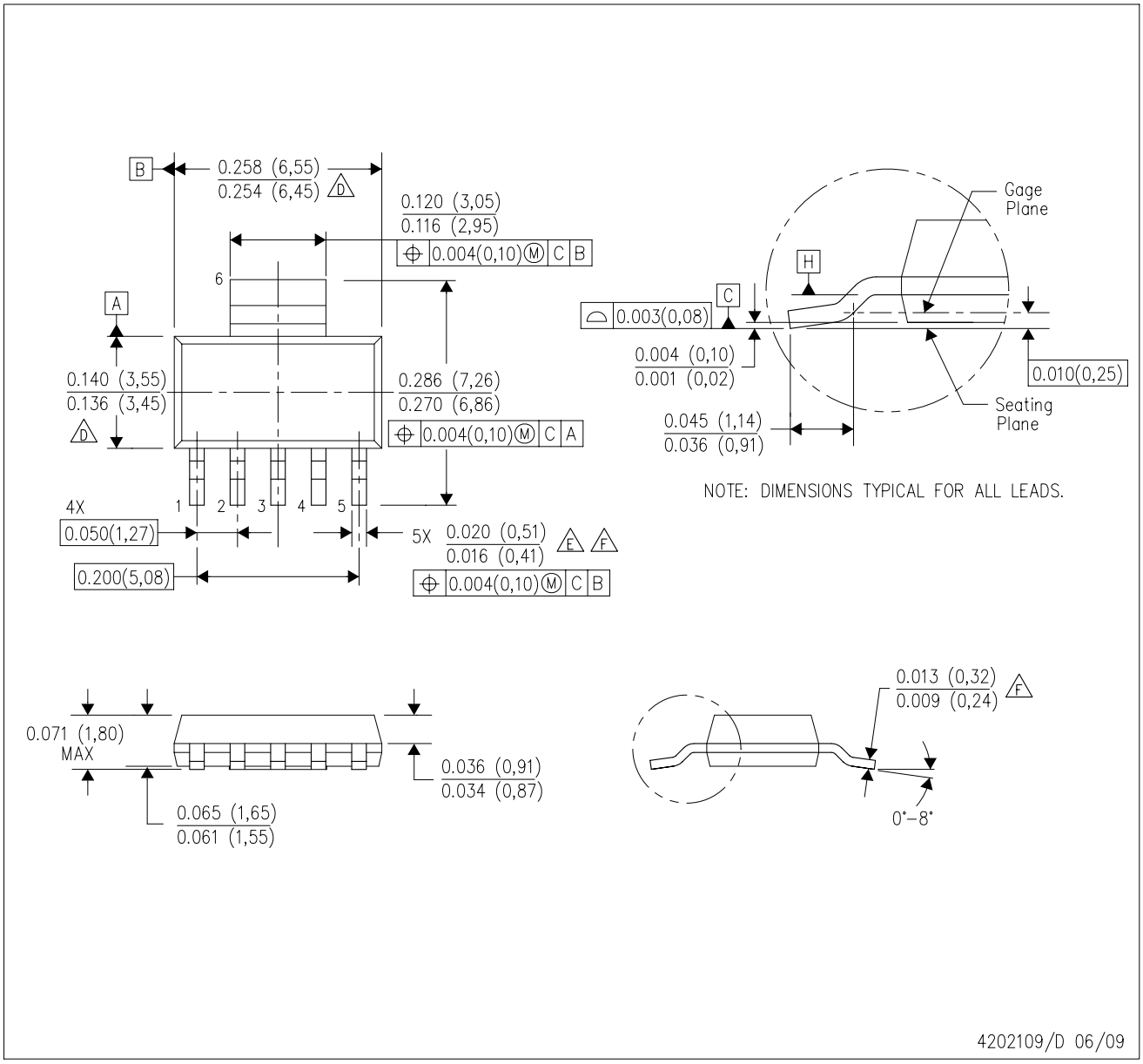
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

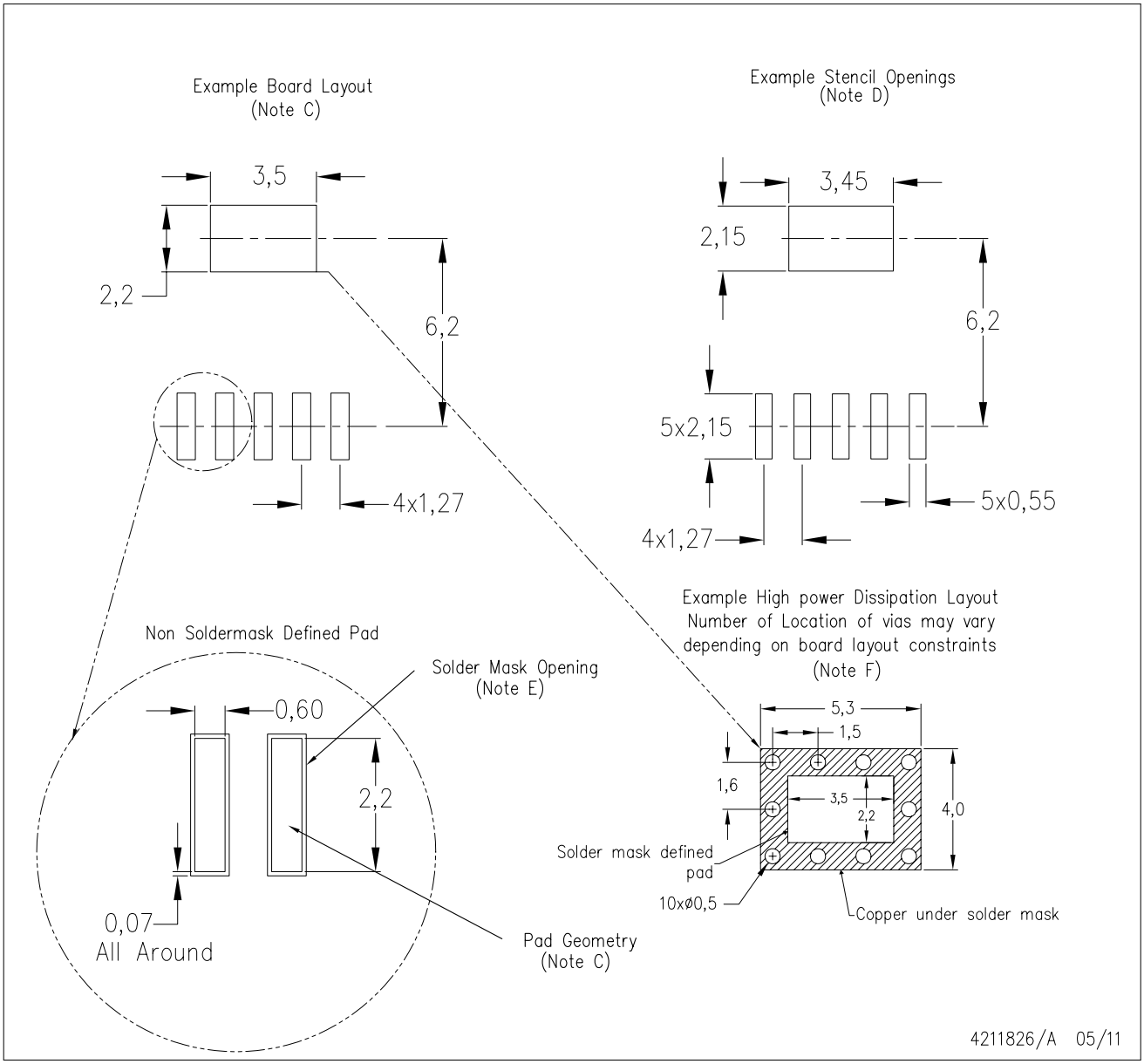
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG103FA-2.5/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
REG103FA-2.5KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG103FA-3.3KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG103FA-5KTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG103FA-A/500	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
REG103FA-AKTTT	DDPAK/TO-263	KTT	5	50	367.0	367.0	45.0
REG103GA-3.3/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG103GA-A/2K5	SOT-223	DCQ	6	2500	346.0	346.0	29.0
REG103UA-2.5/2K5	SOIC	D	8	2500	367.0	367.0	35.0
REG103UA-3.3/2K5	SOIC	D	8	2500	367.0	367.0	35.0
REG103UA-5/2K5	SOIC	D	8	2500	367.0	367.0	35.0
REG103UA-A/2K5	SOIC	D	8	2500	367.0	367.0	35.0

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



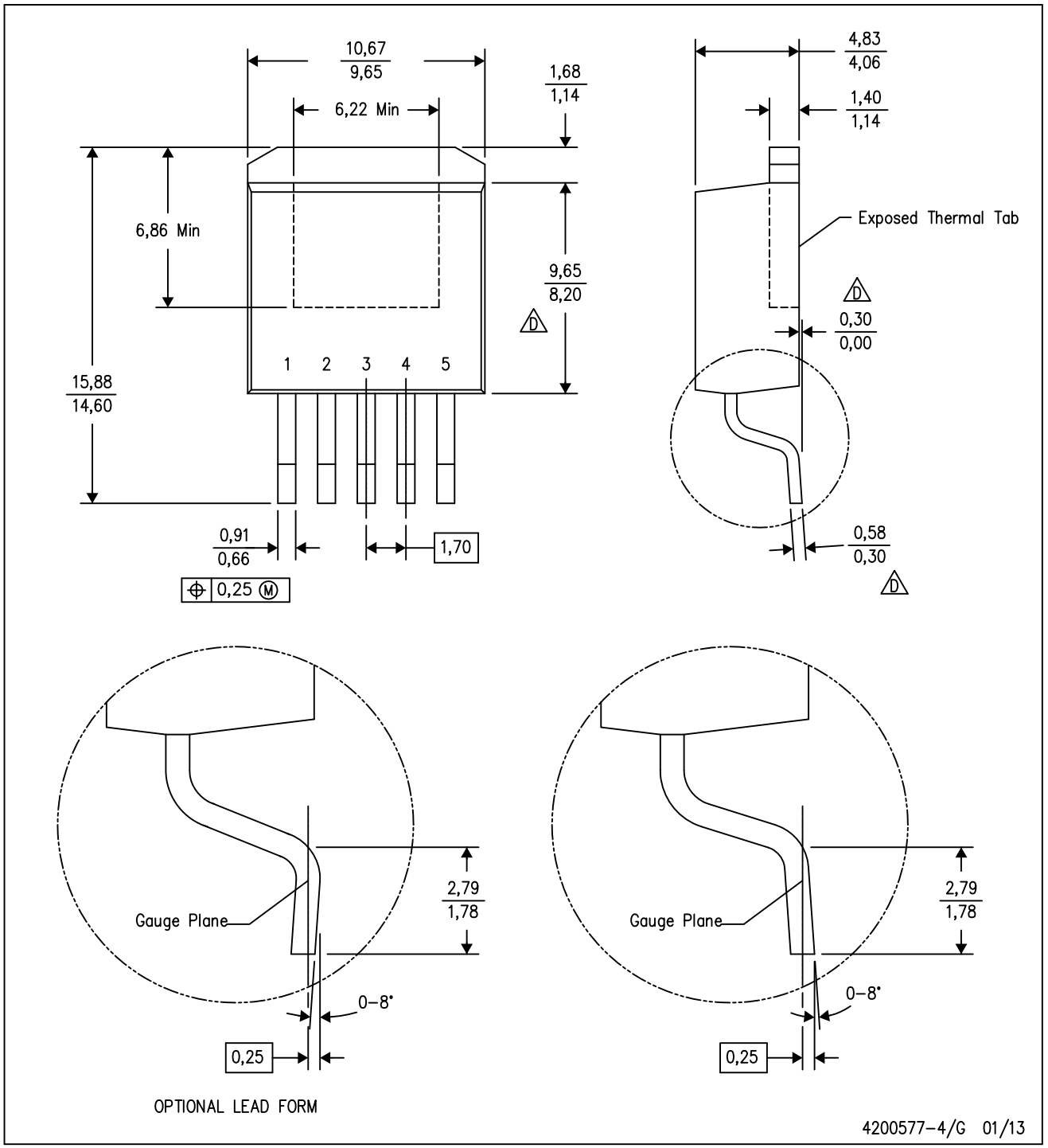
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R–PDSO–G6) PLASTIC SMALL OUTLINE



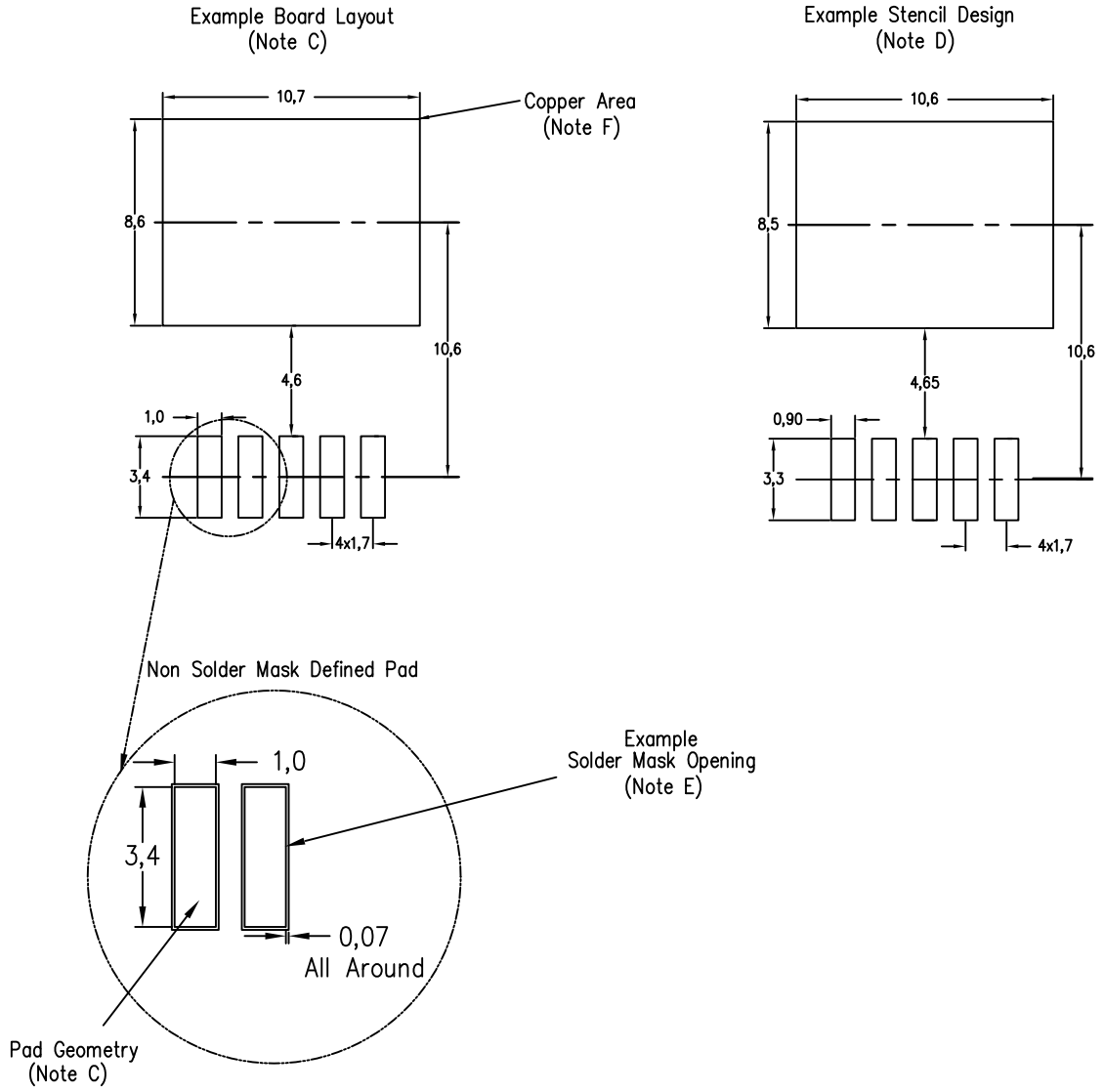
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE

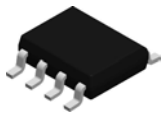


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

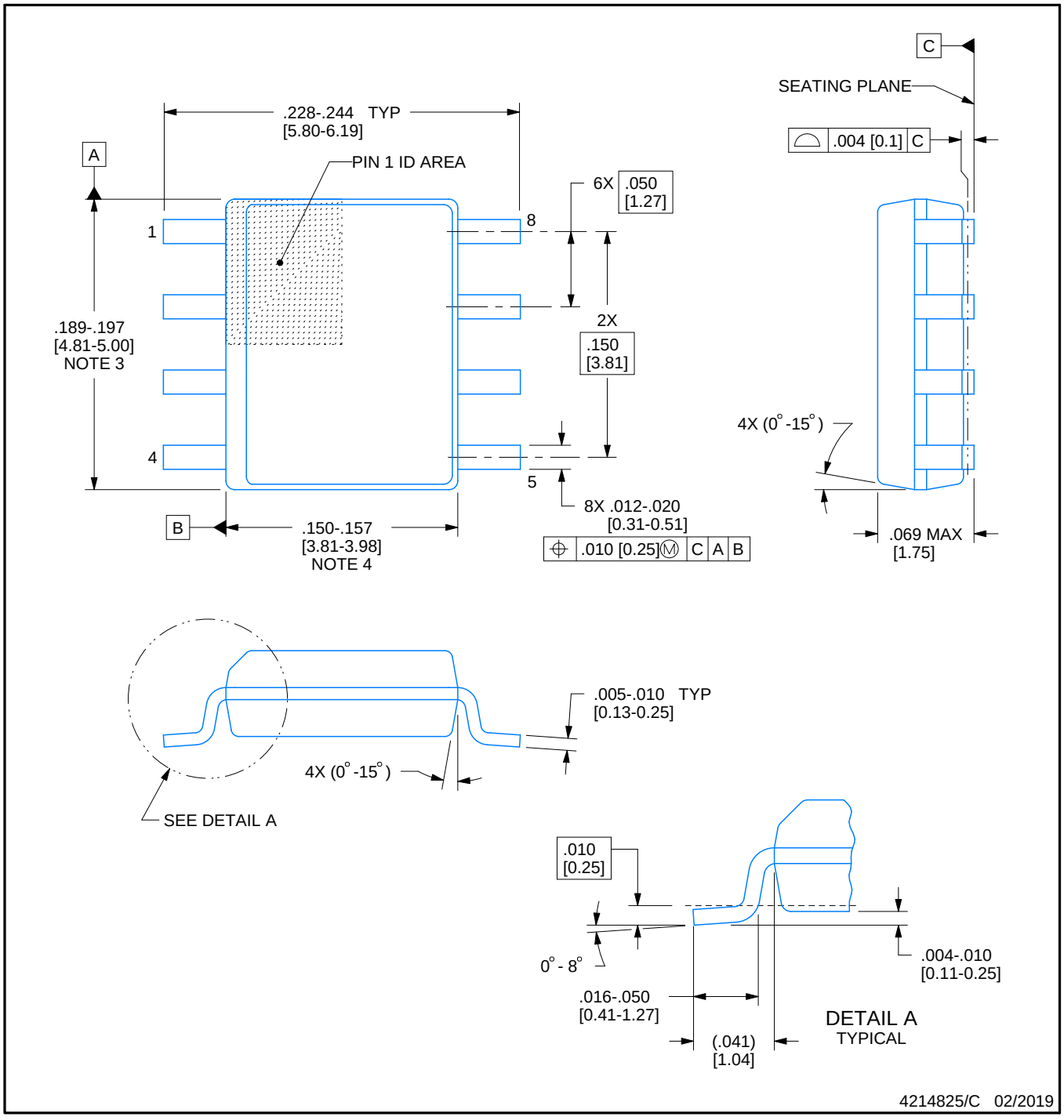


PACKAGE OUTLINE

D0008A

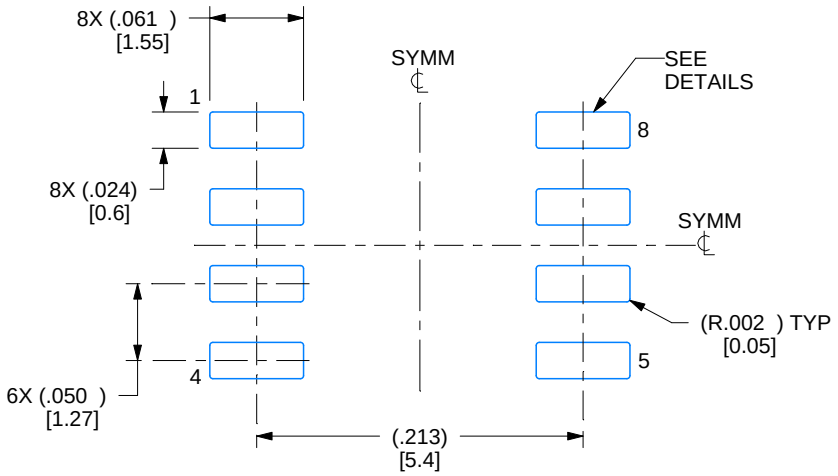
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

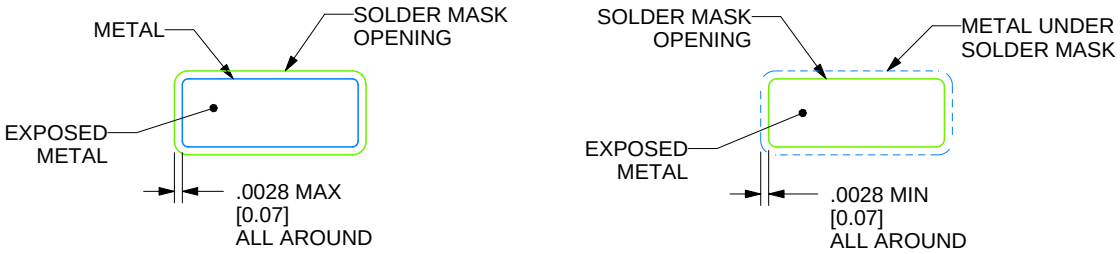


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

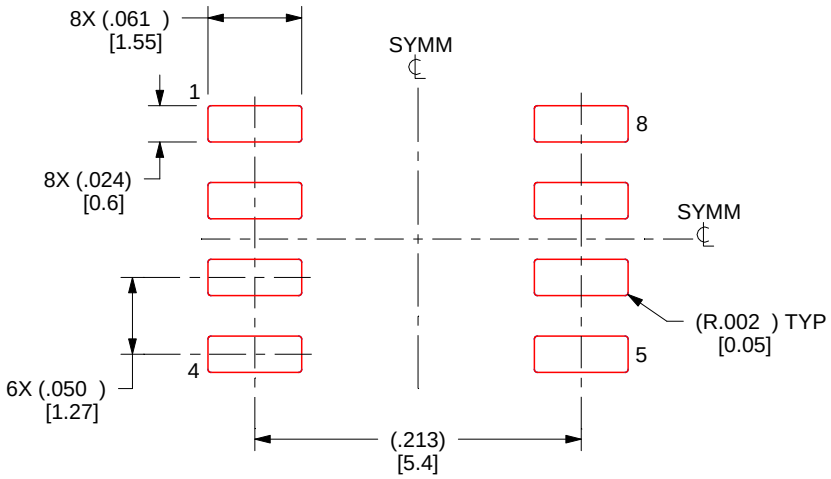
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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