LP3992 Micropower 1.5-V CMOS Voltage Regulator With Shutdown Control

1 Features

- Input Voltage: 1.9 V to 5.2 V
- Operation From a Low Input Voltage: 1.9 V
- Accurate Output Voltage: 1.5 V ± 0.09 V
- Quiescent Current in Shutdown: < 1.5 µA
- Stable With an Output Capacitor: 1 µF
- Ensured Output Current: 30 mA
- Low Output Voltage Noise: 300 μV_{RMS}
- Low Quiescent Current: 29-µA Typical
- Stable With a Ceramic Capacitor
- Logic Controlled Enable
- Fast Turnon and Turnoff
- Thermal-Overload and Short-Circuit Protection
- –40°C to +125°C Junction Temperature Range

2 Applications

- GSM Portable Phones
- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- Bluetooth Devices
- Portable Information Appliances

3 Description

The LP3992 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low noise, and low quiescent current. Battery life is prolonged by the ability of the LP3992 to provide a 1.5-V output from the low input voltage of 1.9 V. Additionally, when switched to a shutdown mode via a logic signal at the enable (EN) pin, the power consumption is reduced to virtually zero. The LP3992 also features short-circuit and thermal-shutdown protection.

The LP3992 is designed to be stable with space-saving ceramic capacitors as small as 1 µF. Performance is specified for a –40°C to +125°C temperature range.

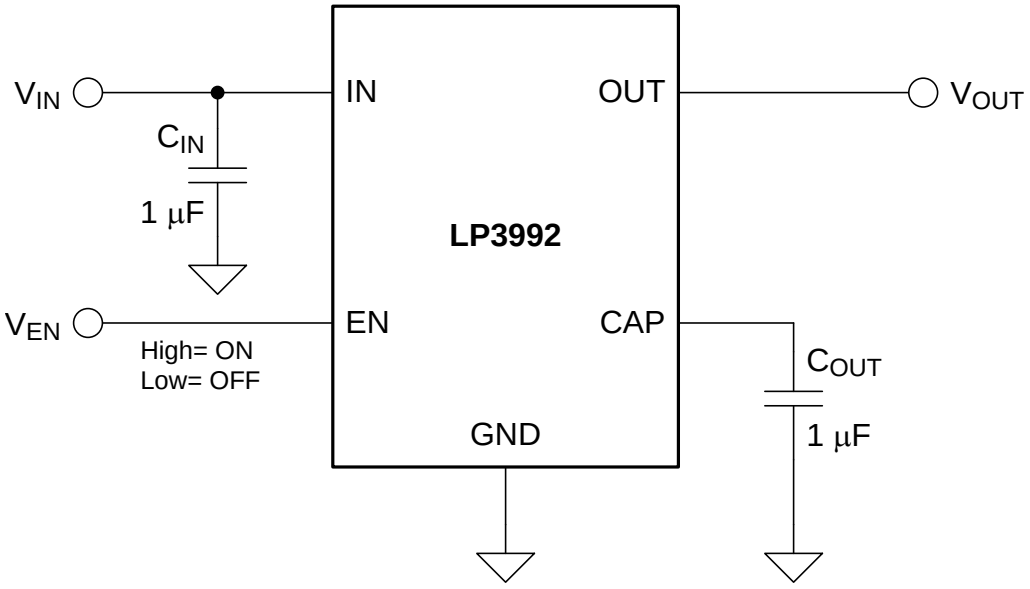
For output voltages other than 1.5 V, and for additional package options, contact TI.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3992	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 5
6.7 Typical Characteristics ... 7
7 Parameter Measurement Information ... 9
7.1 Input Test Signals ... 9
8 Detailed Description ... 10
8.1 Overview ... 10
8.2 Functional Block Diagram ... 10
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 11
9 Application And Implementation ... 12
9.1 Application Information ... 12
9.2 Typical Application ... 12
10 Power Supply Recommendations ... 15
11 Layout ... 15
11.1 Layout Guidelines ... 15
11.2 Layout Example ... 15
12 Device and Documentation Support ... 16
12.1 Documentation Support ... 16
12.2 Community Resources ... 16
12.3 Trademarks ... 16
12.4 Electrostatic Discharge Caution ... 16
12.5 Glossary ... 16
13 Mechanical, Packaging, and Orderable Information ... 16

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2013) to Revision C — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; update pin names from Vin to IN; Vout to OUT; Cout to CAP and $\overline{SD}$ to EN ... 1
- Deleted lead temperature from Abs Max table - it is in POA ... 4
- Added updated thermal information ... 4

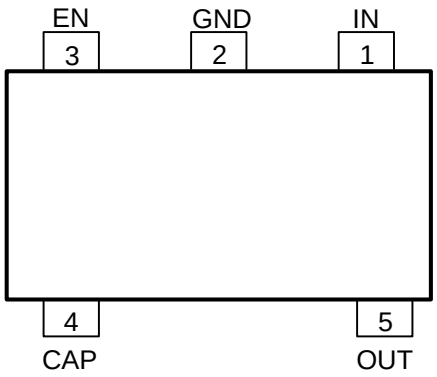
Changes from Revision A (May 2004) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 11

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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN	Input	Voltage supply input
2	GND	Ground	Common ground
3	EN	Input	Shutdown input — disables the regulator when ≤ 0.4 V, enables the regulator when ≥ 1.15 V.
4	CAP	Output	Output capacitor connection. Internally connected to V_{OUT} connection. This is the recommended device connection for the 1-µF output capacitor to ensure a stable output.
5	OUT	Output	Voltage output. Connect this output to the load circuit.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Input voltage	–0.3	6.5	V
Output voltage	–0.3 to (V_{IN} + 0.3)	6.5	V
Shutdown input voltage	–0.3	6.5	V
Maximum power dissipation		568	mW
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input voltage	1.9		5.2	V
Shutdown input voltage	0		6	V
Junction temperature	–40		125	°C
Power dissipation at 25°C			454	mW

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. For ensured performance limits and associated test conditions, see *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC(1)		LP3992 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Unless otherwise noted, V_{EN} = 1.15, V_{IN} = V_{OUT} + 1 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF; typical values and limits apply for T_J = 25°C, and minimum and maximum limits apply over the full temperature range for operation, −40°C to +125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	T_J = 25°C	1.9		5.2	mV
ΔV_{OUT}	Output voltage tolerance	Over full line and load regulation.	–90		90	mV
	Line regulation error	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.2 V, I_{OUT} = 1 mA	–0.27		0.27	%/V
	Load regulation error	I_{OUT} = 1 mA to 30 mA		100	220	µV/mA
I_{LOAD}	Load current	See(2) and (3)	0			µA
I_Q	Quiescent current	V_{EN} = 1.15 V, I_{OUT} = 0 mA		26	50	µA
		V_{EN} = 1.15 V, I_{OUT} = 30 mA		29	50	
		V_{EN} = 0.4 V		0.003	1.5	
I_{SC}	Short-circuit current limit	See(4)		90		mA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, I_{OUT} = 30 mA		40		dB
		f = 20 kHz, I_{OUT} = 30 mA		30		
E_{EN}	Output noise voltage(3)	BW = 10 Hz to 100 kHz, V_{IN} = 4.2 V		300		μV_{RMS}
$T_{SHUTDOWN}$	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
ENABLE CONTROL CHARACTERISTICS						
I_{EN}	Maximum input current at EN input	V_{EN} = 0 V and V_{IN} = 5.2 V		0.001		µA
V_{IL}	Low input threshold	V_{IN} = 1.8 V to 5.2 V			0.4	V
V_{IH}	High input threshold	V_{IN} = 1.8 V to 5.2 V	1.15			V
Transient response	Line transient response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 10 µS(3)			60	mV
	Load transient response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 1 µS, I_{OUT} = 100 µA to 5 mA(3)			60	

(1) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The device maintains the regulated output voltage without the load.
(3) This electrical specification is specified by design.
(4) Short-circuit current is measured on the input supply line at the point when the short-circuit condition reduces the output voltage to 95% of its nominal value.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON1}	Turnon time(1), 50% to 85% of $V_{OUT(NOM)}$(2)			15	µs
t_{ON2}	Turnon time(1) to 95% level(3)		40		µs
t_{OFF1}	Turnoff time(1), 85% to 50% of $V_{OUT(NOM)}$(4)				µs
t_{OFF2}	Turnoff time(1), 95% to 5% level(5)		40	15	µs

(1) This electrical specification is ensured by design.
(2) Time for V_{OUT} to rise from 50% to 85% of $V_{OUT(NOM)}$ (Figure 1).
(3) Time from V_{EN} = 1.15 V to V_{OUT} = 95% ($V_{OUT(NOM)}$) (Figure 1).
(4) Time for V_{OUT} to fall from 85% to 50% of $V_{OUT(NOM)}$ (Figure 1).
(5) Time from V_{EN} = 0.4 V to V_{OUT} = 5% ($V_{OUT(NOM)}$ (Figure 1).

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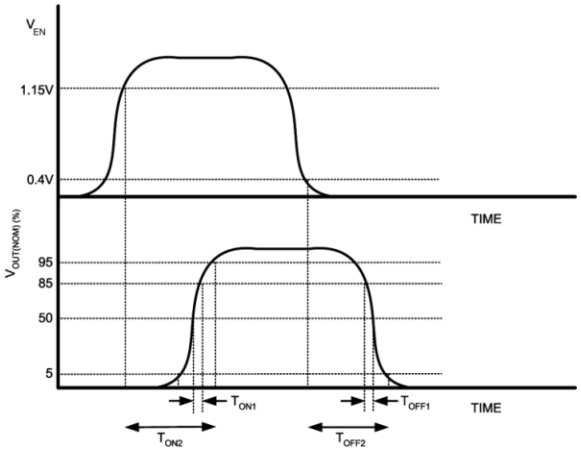


Figure 1. t_{ON} and t_{OFF} Timing Diagram

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6.7 Typical Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\text{-}\mu F$ ceramic, $V_{IN} = 2.8$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

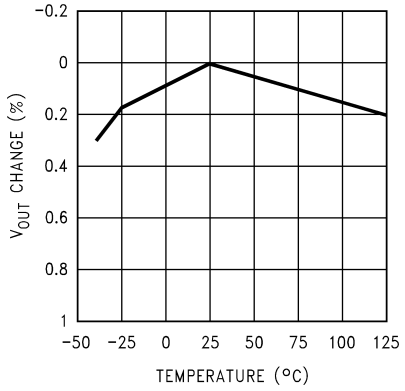


Figure 2. Output Voltage Change vs Temperature

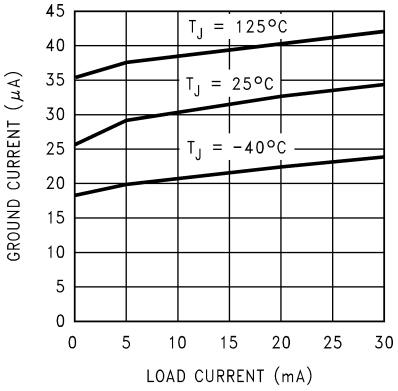


Figure 3. Ground Current vs Load Current

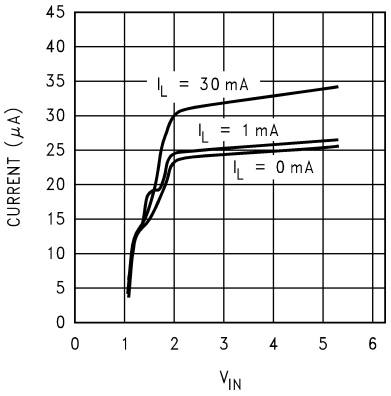


Figure 4. Ground Current vs V_{IN}

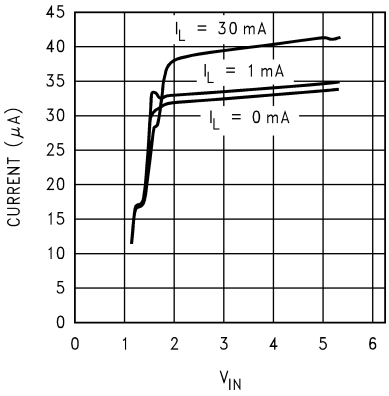


Figure 5. Ground Current vs V_{IN}

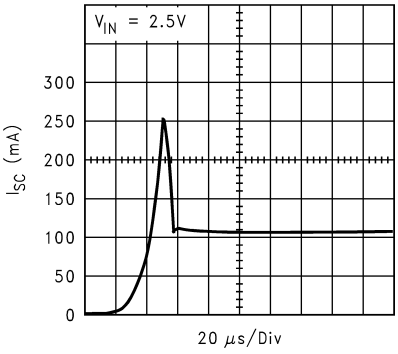


Figure 6. Short-Circuit Current

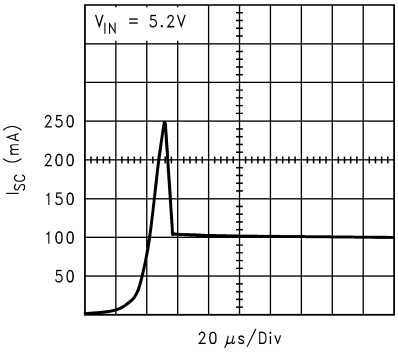


Figure 7. Short-Circuit Current

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Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT}$ = 1-µF ceramic, V_{IN} = 2.8 V, T_A = 25°C, EN pin is tied to V_{IN}.

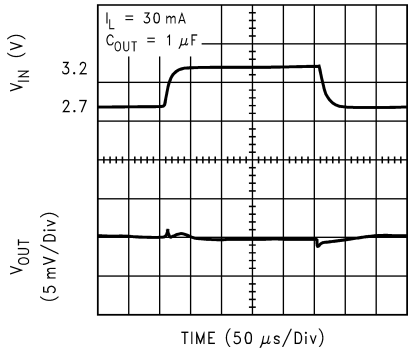


Figure 8. Line Transient Response

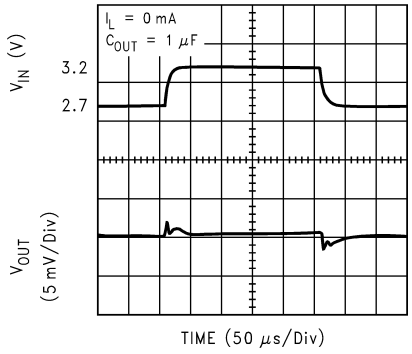


Figure 9. Line Transient Response

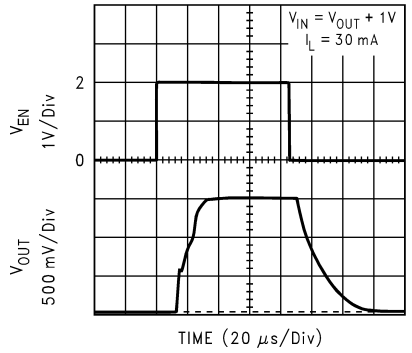


Figure 10. Turnon, Turnoff Timing

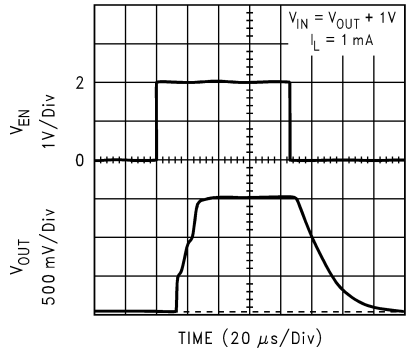


Figure 11. Turnon, Turnoff Timing

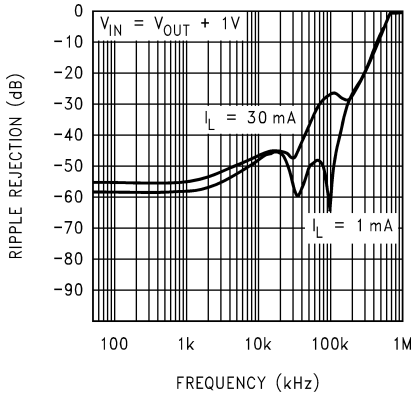


Figure 12. Ripple Rejection

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7 Parameter Measurement Information

7.1 Input Test Signals

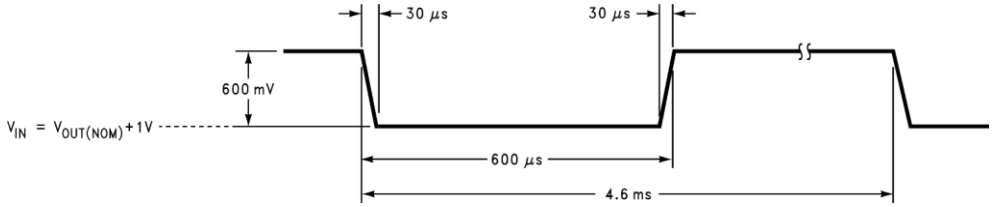


Figure 13. Line Transient Input Test Signal

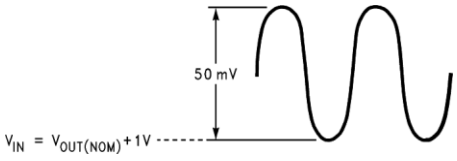


Figure 14. PSRR Input Test Signal

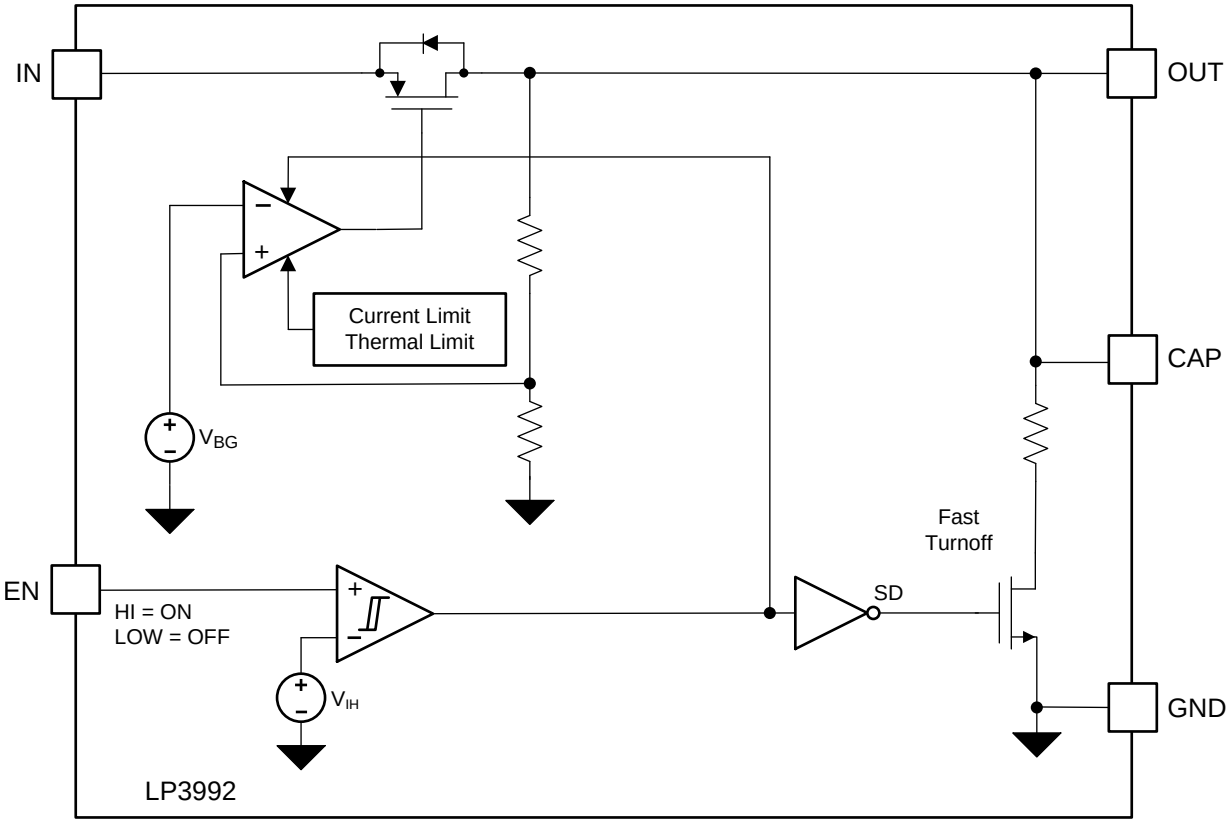
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8 Detailed Description

8.1 Overview

The LP3992 device is a CMOS voltage regulator with a low-input operating-voltage tolerance. Key protection circuits, including thermal-overload and short-circuit protection, are integrated in the device. Using the EN pin, the device may be controlled to provide a SHUTDOWN state, in which negligible supply current is drawn. The LP3992 is designed to be stable with space-saving ceramic capacitors.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Shutdown and Enable

The LP3992 may be switched ON or OFF by a logic input at the EN pin. A high voltage at the EN pin turns the device on. A low voltage on the EN pin will disable the regulator, and will activate the fast turnoff circuitry to discharge the output capacitance. When the regulator is disabled the device typically consumes 3 nA.

If the application does not require the EN feature, the EN pin must be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

8.3.2 Fast Turnon and Turnoff

The controlled shutdown feature of the device provides a fast turn off by discharging the output capacitor via an internal FET device. This discharge is current limited by the RDS_{ON} of this switch. Fast turnon is ensured by control circuitry within the reference block allowing a very fast ramp of the output voltage to reach the target voltage.

8.4 Device Functional Modes

8.4.1 Enable Operation

The LP3992 may be switched ON or OFF by a logic input at the EN pin. A high voltage at the EN pin turns the device on. A low voltage on the EN pin will disable the regulator, and will activate the fast turnoff circuitry to discharge the output capacitance. When the regulator is disabled the device typically consumes 3 nA.

If the application does not require the EN feature, the EN pin should be tied to V_{IN} to keep the regulator output permanently on.

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9 Application And Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3992 can provide 30-mA output current with 1.9-V to 5.2-V input. It is stable with 1-µF ceramic input and output capacitors. Typical output noise is 300 μV_{RMS} at frequencies from 10 Hz to 100 kHz. Typical power supply rejection is 40 dB at 1 kHz.

9.2 Typical Application

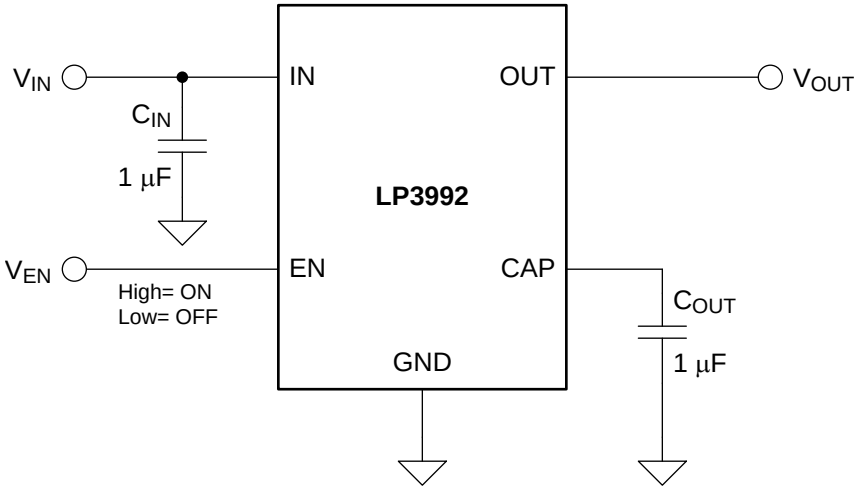


Figure 15. LP3992 Typical Application

9.2.1 Design Requirements

For typical CMOS voltage regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	1.9 V
Output voltage	1.5 ± 0.09 V
Output current	30 mA

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitors

In common with most regulators, the LP3992 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

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9.2.2.2 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP3992 IN pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good-quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1 µF over the entire operating temperature range.

9.2.2.3 Output Capacitor

The LP3992 is designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (dielectric types Z5U, Y5V or X7R) with ESR from 5 mΩ to 500 mΩ, is suitable in the LP3992 application circuit.

For this device the output capacitor should be connected between the CAP pin and ground. It is also possible to connect the output capacitor directly to the OUT pin. In this case the CAP pin must be left open-circuit or tied directly to the OUT pin.

Tantalum or film capacitors may also be used at the device output, CAP (or OUT), but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the 5-mΩ to 500-mΩ range for stability.

Table 2. Recommended Output Capacitor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitor	Capacitance(1)	0.7	1		µF
		ESR	5		500	mΩ

(1) The capacitor tolerance should be ±30% or better over the temperature range. The recommended capacitor type is X7R however, dependant on the application X5R, Y5V, and Z5U can also be used.

9.2.2.4 No-Load Stability

The LP3992 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

9.2.2.5 Capacitor Characteristics

The LP3992 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the 1-µF to 4.7-µF range, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the 20-mΩ to 40-mΩ range that easily meets the ESR requirement for stability for the LP3992.

The temperature performance of ceramic capacitors varies by type. Most large-value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

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Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. Also, the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

9.2.2.6 Power Dissipation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air (see Equation 1).

$$T_{A(MAX)} = T_{J(MAX-OP)} - (P_{D(MAX)} \times R_{\theta JA}) \quad (1)$$

The allowable power dissipation for the device in a given package can be calculated:

$$P_D = T_{J(MAX)} - T_A / R_{\theta JA} \quad (2)$$

The actual power dissipation across the device can be represented by Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Equation 2 and Equation 3 must be used to determine the optimum operating conditions for the device in the application.

This thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability of the particular PCB design and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the SOT-23 package junction-to-board thermal resistance ($R_{\theta JB}$) plus the thermal resistance contribution by the PCB copper area acting as a heatsink.

9.2.2.7 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 2
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 2.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953); for more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017). Aforementioned application notes are available at www.ti.com.

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9.2.3 Application Curves

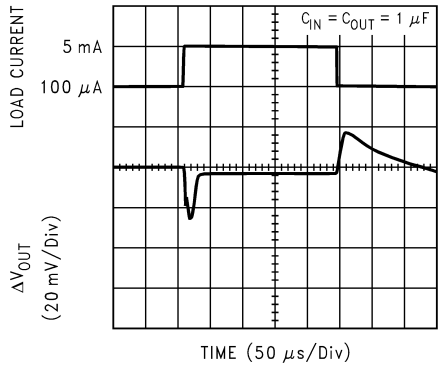


Figure 16. Load Transient Response

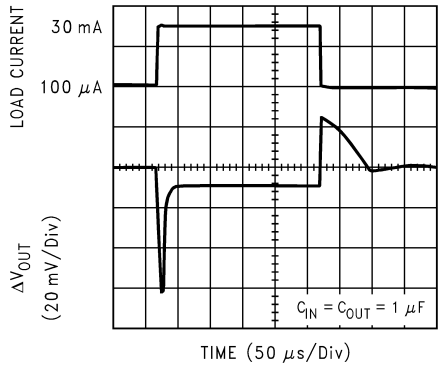


Figure 17. Load Transient Response

10 Power Supply Recommendations

The LP3992 is designed to operate from an input voltage supply range from 1.9 V to 5.2 V.

11 Layout

11.1 Layout Guidelines

The dynamic performance of the LP3992 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the device.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP3992 and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be routed back to the LP3992 GND pin using as wide and as short a copper trace as is practical.

Avoid layout connections that have any combination of long trace length, narrow trace width, or vias. These add parasitic inductances and resistance that result in inferior performance, especially during transient conditions.

11.2 Layout Example

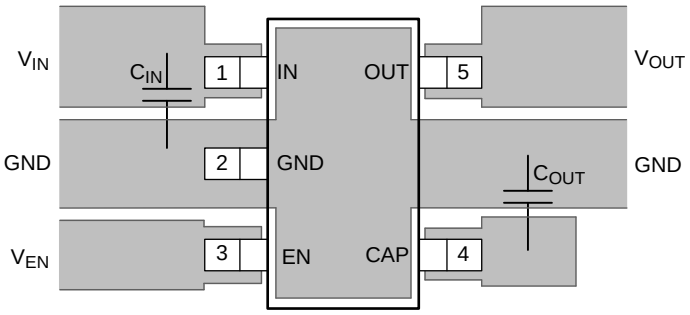


Figure 18. LP3992 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- TI Application Report *Using New Thermal Metrics* (SBVA025)
- TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3992IMFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

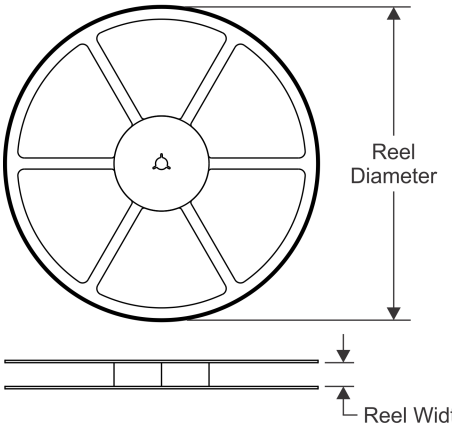
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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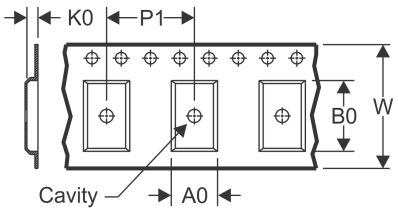
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

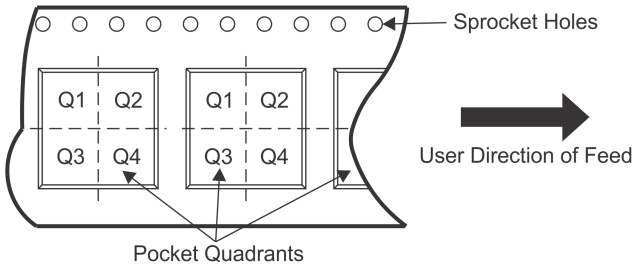


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

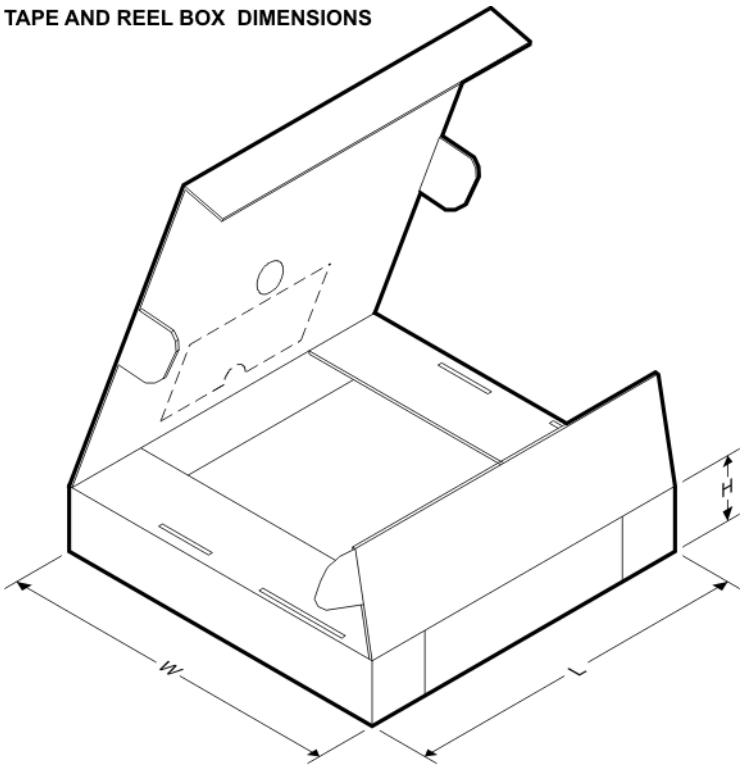
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3992IMFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

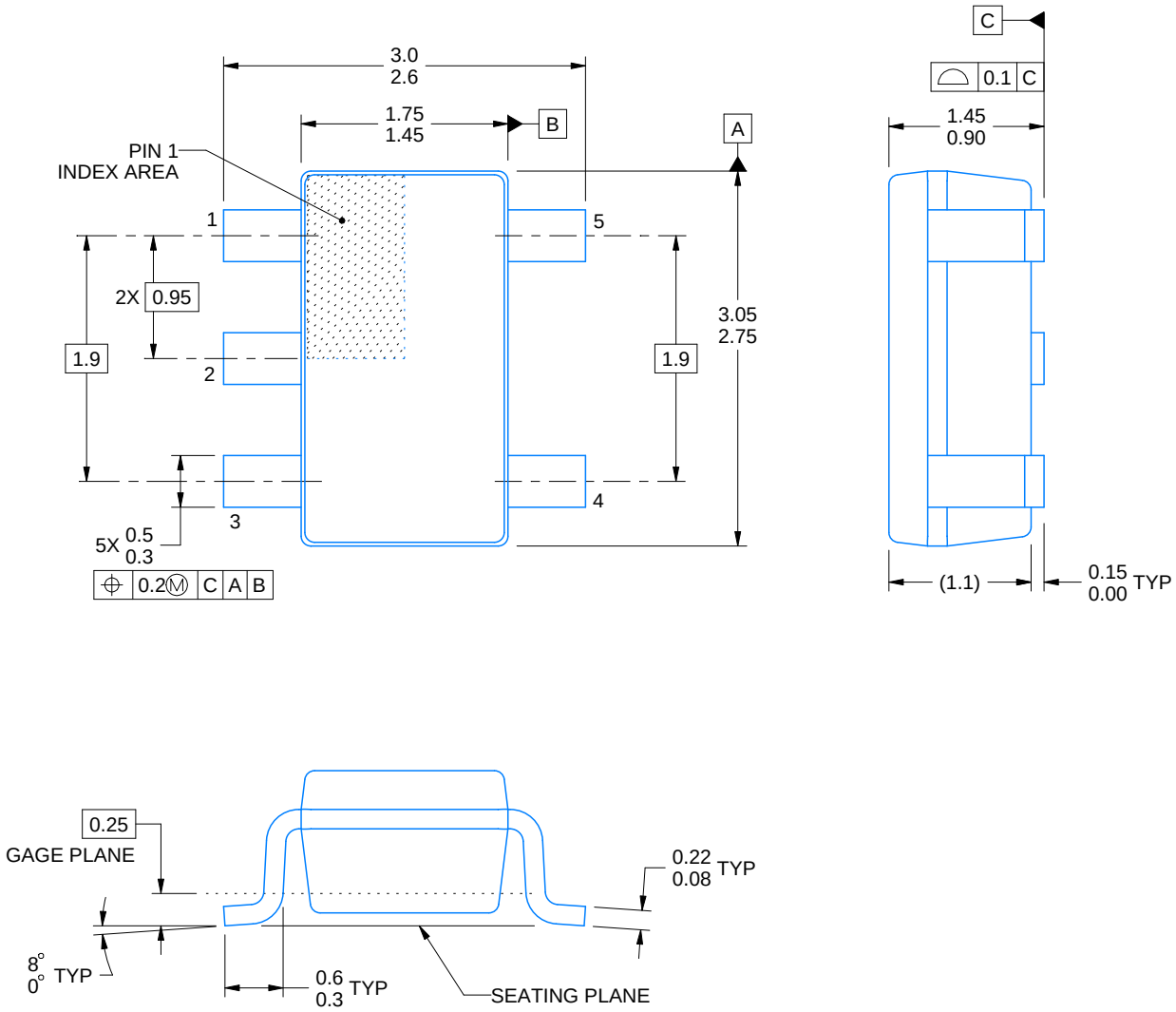
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3992IMFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

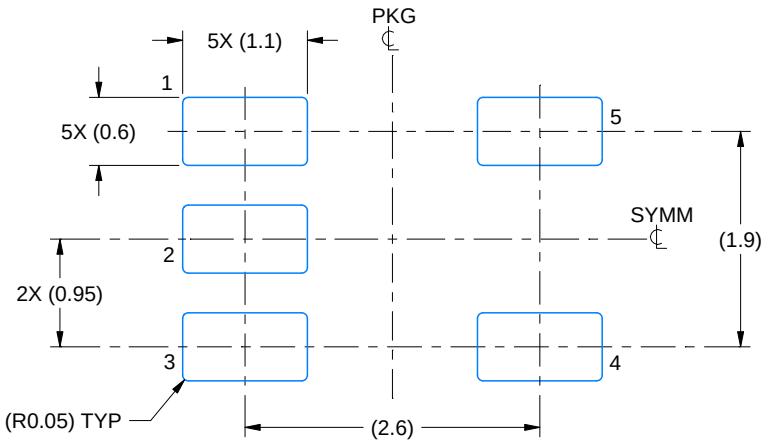
SMALL OUTLINE TRANSISTOR



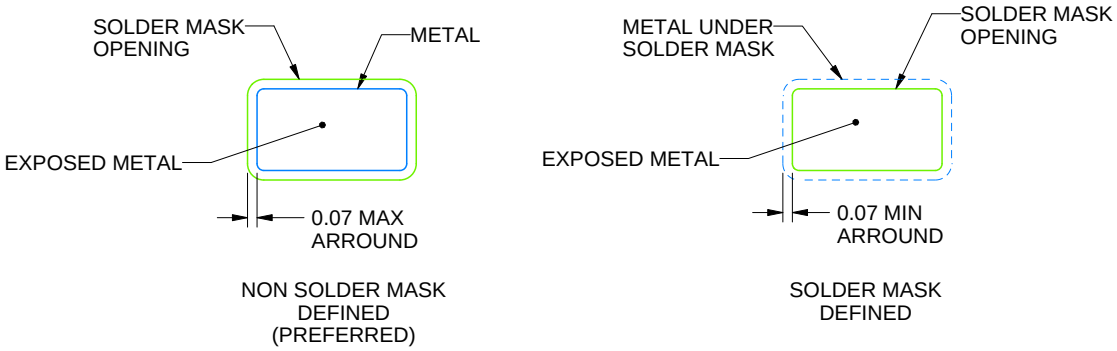
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

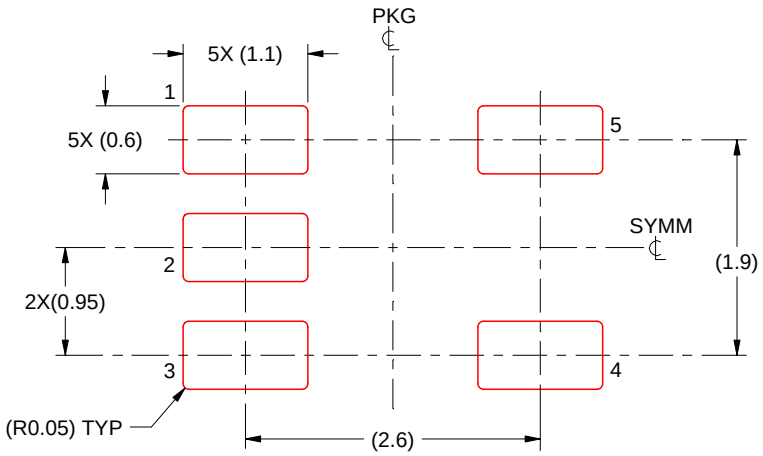


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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