LM3722/LM3723/LM3724 5-Pin Microprocessor Reset Circuits

Check for Samples: LM3722, LM3723, LM3724

FEATURES

- **Precise Monitoring of 2.5V, 3.3V, and 5V Supply Voltages**
- **Fully Specified Over Temperature**
  - **Industrial: −40°C to +85°C**
  - **Extended: −40°C to +125°C**
- **100 ms Minimum Power-On Reset pulse Width, 190 ms Typical:**
  - **Active-Low $\overline{\text{RESET}}$ Output (LM3722)**
  - **Active-High RESET Output (LM3723)**
  - **Active-Low $\overline{\text{RESET}}$ Open Drain Output (LM3724)**
- **Guaranteed $\overline{\text{RESET}}$ Output Valid for $V_{CC} \geq 1V$**
- **Low Supply Current, 6µA Typical**
- **Power Supply Transient Immunity**
- **Compatible with MAX811/812 Applications**

APPLICATIONS

- **Microprocessor Systems**
- **Computers**
- **Controllers**
- **Intelligent Instruments**
- **Portable/Battery-Powered Equipment**

DESCRIPTION

The LM3722/LM3723/LM3724 microprocessor supervisory circuits monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down, brown-out conditions, and manual reset.

The LM3722/LM3723/LM3724 asserts a reset signal whenever the supply decreases below the factory-programmed reset threshold. Reset will be asserted for at least 100ms even after V_{CC} rises above the reset threshold.

The LM3722 has an active-low $\overline{\text{RESET}}$ push-pull output. The LM3723 has an active-high RESET push-pull output. The LM3724 has an active-low open-drain $\overline{\text{RESET}}$ output.

Three standard reset voltage options are available, suitable for monitoring 5V, 3.3V, and 2.5V supply voltages. Additional reset voltages are also available; contact Texas Instruments for details.

With a low supply current of only 6µA, the LM3722/LM3723/LM3724 are ideal for use in portable equipment. The LM3722/LM3723/LM3724 are available in the 5-pin SOT-23 package.

Typical Application Circuits

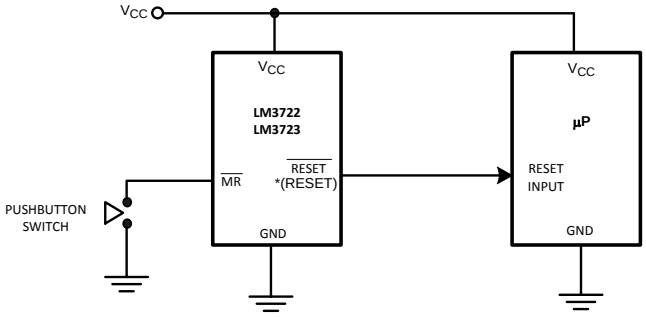


Figure 1. Typical Application Circuit

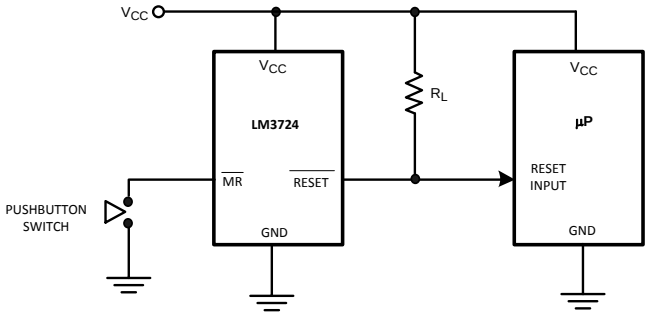


Figure 2. Typical Application Circuit with R_L Connection

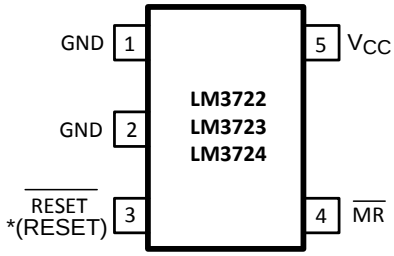
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Connection Diagram



*( ) are for LM3723

Figure 3. SOT-23-5

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	GND	Ground reference
2	GND	Ground reference, device substrate, connect to ground.
3	$\overline{\text{RESET}}$ LM3722/LM3724	Active-low output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold voltage, and for 190 ms after V_{CC} rises above the reset threshold voltage.
	RESET LM3723	Active-high output. RESET remains high while V_{CC} is below the reset threshold, and for 190 ms after V_{CC} rises above the reset threshold.
4	$\overline{\text{MR}}$	Active-low input. Reset is asserted whenever this pin is pulled low and remains asserted for 190 ms after the $\overline{\text{MR}}$ pin goes high. May be left open.
5	V_{CC}	Supply Voltage (+5V, +3.3V, or +2.5V, nominal)

Block Diagram

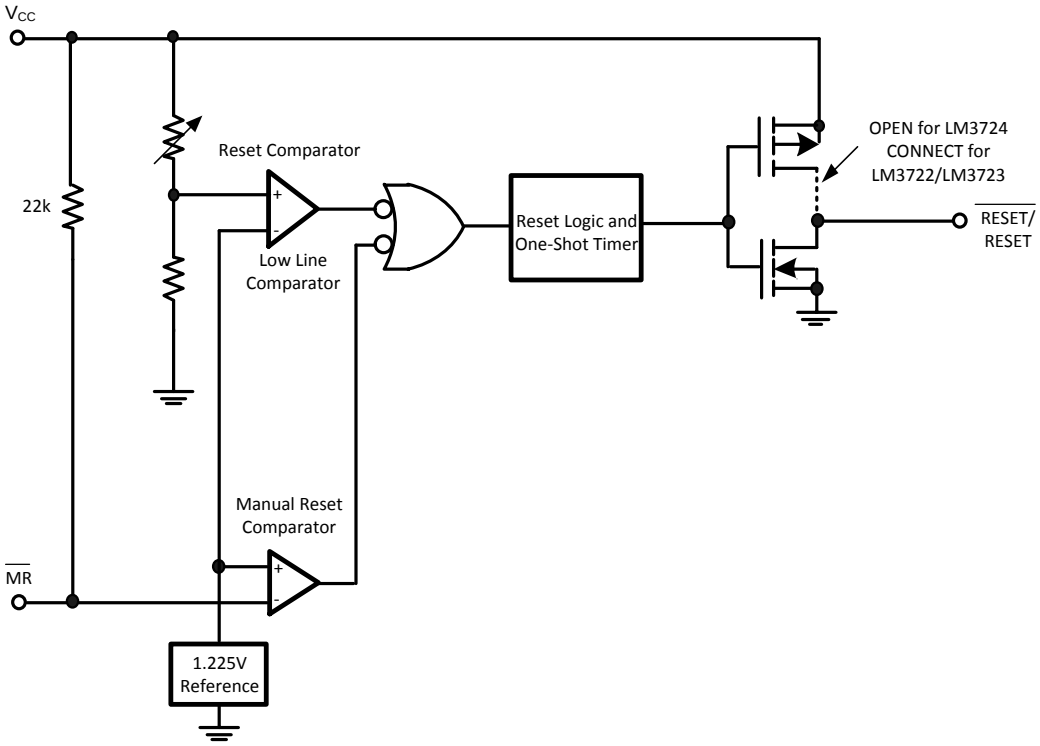


Figure 4. LM3722/LM3723/LM3724 Block Diagram

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{CC}, $\overline{MR}$	−0.3V to 6.0V
RESET, $\overline{RESET}$	−0.3V to (V_{CC}+ 0.3V)
Input Current, V_{CC} Pin	20mA
Output Current, RESET, $\overline{RESET}$ Pin	20mA
ESD Rating (3)	2kV
Continuous Power Dissipation (T_A = +70°C)	
SOT-23 (4)	320mW
Operating Temperature Range	
Industrial:	−40°C to +85°C
Extended:	−40°C to +125°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device operates correctly. Operating ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(4) At elevated temperatures, devices must be derated based on package thermal resistance. The device in the SOT-23-5 package must be derated at 4.5mW/°C at ambient temperatures above 70°C. The device has internal thermal protection.

Electrical Characteristics

Typical values are at T_A = +25°C. Limits with standard typeface are for T_A = +25°C, and limits in boldface type apply for the operating temperature range (−40°C to +85°C) for LM372_IM5X, and (−40°C to +125°C) for LM372_EM5X, unless otherwise noted. (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{CC}	V_{CC} Range			**1.0**		**5.5**	V
I_{CC}	Supply Current (I_{LOAD} = 0A)	LM372 _ -4.63	V_{CC} = 5.5V		8	**15**	µA
		LM372 _ -3.08	V_{CC} = 3.6V		7	**10**	
		LM372 _ -2.32	V_{CC} = 2.5V		6	**10**	
V_{TH}	Reset Threshold	LM372 _ -4.63		4.54 **4.50**	4.63	4.72 **4.75**	V
		LM372 _ -3.08		3.03 **3.00**	3.08	3.14 **3.15**	
		LM372 _ -2.32		2.27 **2.25**	2.32	2.37 **2.40**	
V_{TH} Tempco	Reset Threshold Temperature Coefficient				30		ppm/°C
t_{RD}	V_{CC} to Reset Delay (2)	V_{CC} = V_{TH} to (V_{TH} − 100mV)			20		µs
t_{RP}	Reset Active Timeout Period			**100**	190	**560**	ms
t_{MR}	$\overline{MR}$ Minimum Pulse Width			**10**			µs
t_{MD}	$\overline{MR}$ to Reset Propagation Delay				2		µs
	$\overline{MR}$ Glitch Immunity (3)				100		ns

(1) Production testing done at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
(2) $\overline{RESET}$ Output for LM3722 and LM3724, RESET output for LM3723.
(3) Glitches of 100 ns or less typically will not generate a reset pulse.

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Electrical Characteristics (continued)

Typical values are at T_A = +25°C. Limits with standard typeface are for T_A = +25°C, and limits in boldface type apply for the operating temperature range (−40°C to +85°C) for LM372_IM5X, and (−40°C to +125°C) for LM372_EM5X, unless otherwise noted. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	$\overline{MR}$ Input Threshold	$V_{CC} > V_{TH(MAX)}$, LM372_ -4.63	**2.3**			V
V_{IL}					**0.8**	
V_{IH}		$V_{CC} > V_{TH(MAX)}$, LM372_ -3.08, LM372_ -2.32	**0.7 V_{CC}**			
V_{IL}					**0.25 V_{CC}**	
	$\overline{MR}$ Pull-Up Resistance			22		kΩ
V_{OL}	$\overline{RESET}$ Output Voltage Low (LM3722)	$V_{CC} = V_{TH}$ min, I_{SINK} = 1.2mA, (LM3722-2.32/3.08)			**0.3**	V
		$V_{CC} = V_{TH}$ min, I_{SINK} = 3.2mA, (LM3722-4.63)			**0.4**	
		V_{CC} > 1V, I_{SINK} = 50µA			**0.3**	
V_{OH}	$\overline{RESET}$ Output Voltage High (LM3722)	$V_{CC} > V_{TH}$ max, I_{SOURCE} = 500µA, (LM3722-2.32/3.08)	**0.8V_{CC}**			V
		$V_{CC} > V_{TH}$ max, I_{SOURCE} = 800µA, (LM3722-4.63)	**V_{CC}–1.5**			
V_{OL}	RESET Output Voltage Low (LM3723)	$V_{CC} = V_{TH}$ max, I_{SINK} = 1.2mA (LM3723 -2.32/3.08)			**0.3**	V
		$V_{CC} = V_{TH}$ max, I_{SINK} = 3.2mA (LM3723 -4.63)			**0.4**	
V_{OH}	RESET Output Voltage High (LM3723)	1.8V < V_{CC} < V_{TH} min, I_{SOURCE} = 150µA	**0.8V_{CC}**			V
V_{OL}	$\overline{RESET}$ Output Voltage Low (LM3724)	$V_{CC} = V_{TH}$ min, I_{SINK} = 1.2 mA (LM3724 -2.32/3.08)			**0.3**	V
		$V_{CC} = V_{TH}$ min, I_{SINK} = 3.2 mA (LM3724 -4.63)			**0.4**	
		V_{CC} > 1V, I_{SINK} = 50µA			**0.3**	
I_{IN}	$\overline{RESET}$ Output Leakage Current (LM3724)	$V_{CC} > V_{TH}$, $\overline{RESET}$ = 5.5V			**0.5**	µA

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Typical Performance Characteristics

Supply Current vs V_{CC}

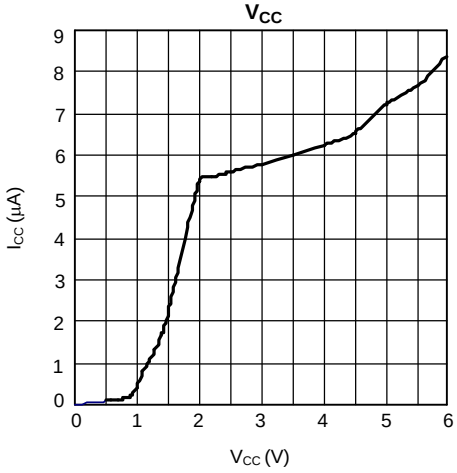


Figure 5.

Supply Current vs Temperature

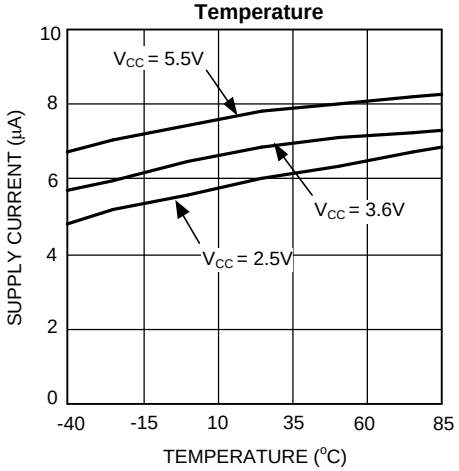


Figure 6.

Reset Timeout vs V_{CC}

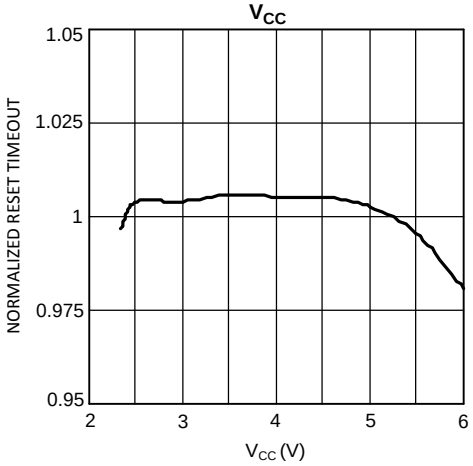


Figure 7.

Reset Timeout vs Temperature

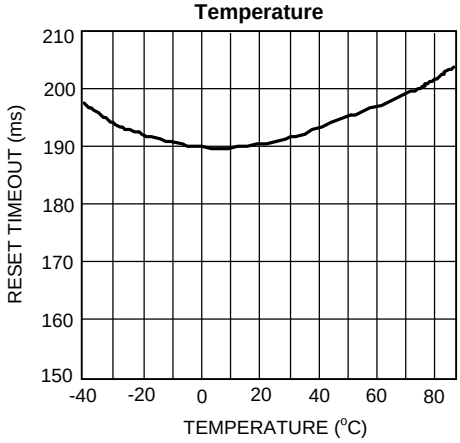


Figure 8.

Normalized V_{TH} vs Temperature

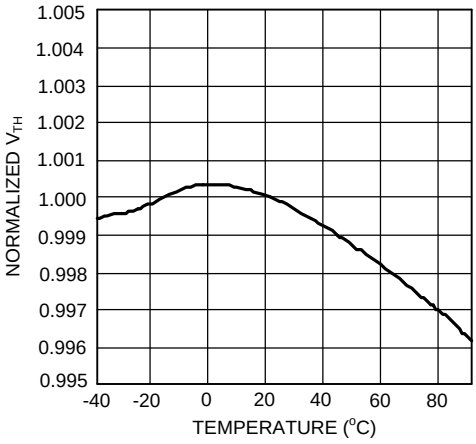


Figure 9.

LM3724 V_{OL} vs Current

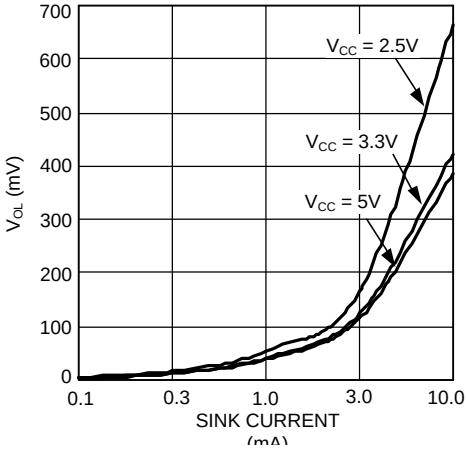


Figure 10.

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Typical Performance Characteristics (continued)

LM3724 Low V_{CC} Characteristics

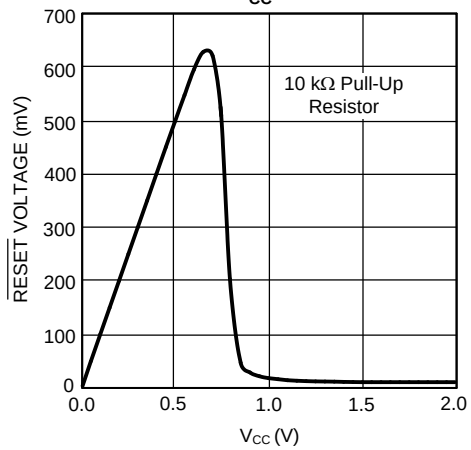


Figure 11.

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Timing Diagram

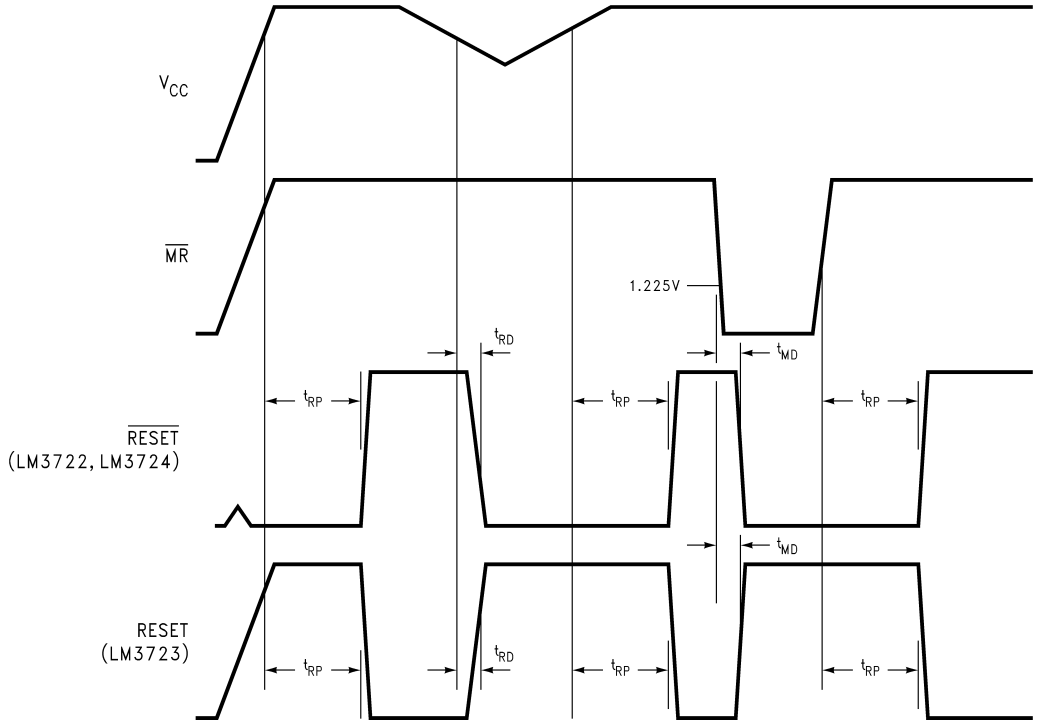


Figure 12. Timing Diagram

Circuit Information

RESET OUTPUT

The reset input of a µP initializes the device into a known state. The LM3722/LM3723/LM3724 microprocessor voltage monitoring circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{RESET}$ is guaranteed valid for $V_{CC} \geq 1V$. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high and the microprocessor initializes itself into a known state. The LM3722 and LM3724 offer an active-low $\overline{RESET}$; the LM3723 offers an active-high RESET.

As V_{CC} drops below the reset threshold (such as during a brownout), the reset activates (see the NEGATIVE-GOING V_{CC} TRANSIENTS section). When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

Additionally, the Manual Reset input ($\overline{MR}$) will initiate a forced reset. See the MANUAL RESET INPUT ($\overline{MR}$) section.

The LM3722/LM3723/LM3724 reset outputs ignore short duration glitches on V_{CC} and $\overline{MR}$. See the Applications Information section for details.

RESET THRESHOLD

The LM3722/LM3723/LM3724 are available with reset voltages of 4.63V, 3.08V, and 2.32V which are suitable for monitoring 5.0V, 3.3V, and 2.5V supplies respectively. Other reset thresholds in the 2.20V to 5.0V range, in 10 mV steps, are available; contact Texas Instruments for details.

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MANUAL RESET INPUT ($\overline{MR}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{MR}$ input is fully debounced and provides an internal 22 kΩ pull-up. When the $\overline{MR}$ input is pulled below V_{IL} ($0.25V_{CC}$) for more than 100 ns, reset is asserted after a typical delay of 2 µs. Reset remains active as long as $\overline{MR}$ is held low, and releases after $\overline{MR}$ rises above V_{IH} and the reset timeout period expires. Use $\overline{MR}$ with digital logic to assert reset or to daisy chain supervisory circuits.

APPLICATIONS INFORMATION

BENEFITS OF PRECISION RESET THRESHOLDS

A microprocessor supply supervisor must provide a reset output within a predictable range of the supply voltage. A common threshold range is between 5% and 10% below the nominal supply voltage. The 4.63V, 3.08V and 2.32V options of the LM3722/LM3723/LM3724 use highly accurate circuitry to ensure that the reset threshold occurs only within this range (for 5.0V, 3.3V and 2.5V supplies). Table 1 shows how the standard reset thresholds apply to 5.0V, 3.3V, and 2.5V nominal supply voltages.

Table 1. Monitored Tolerance Table

Reset Threshold	Supply Voltage		
	2.5V	3.3V	5.0V
4.63 ± %			90.8-94.4%
3.08 ± %		91.8-95.2%	
2.32 ± %	90.8-94.8%		

ENSURING A VALID RESET OUTPUT DOWN TO V_{CC} = 0V

When V_{CC} falls below 1V, the LM3722 $\overline{RESET}$ output is unable to sink the rated current. A high-impedance CMOS logic input connected to $\overline{RESET}$ can therefore drift to undetermined voltages. To prevent this situation, a 100kΩ resistor should be connected from the $\overline{RESET}$ output to ground, as shown in Figure 13.

A 100kΩ pull-up resistor to V_{CC} is also recommended for the LM3723, if RESET is required to remain valid for V_{CC} < 1V.

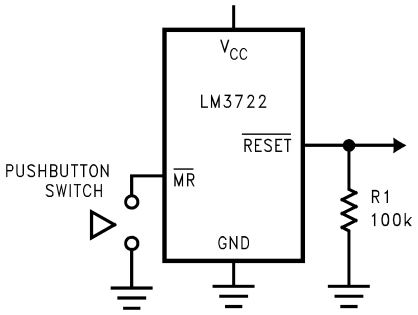


Figure 13. Circuit for $\overline{RESET}$ Valid from V_{CC} = 0V

OPEN DRAIN OUTPUT (LM3724)

An open drain output allows easy paralleling of multiple microprocessor reset circuits without requiring additional logic gates. Open drain outputs also allow interfacing devices of differing logic levels or families, since the output pull-up resistor may be connected to any supply voltage up to 5.5V, regardless of LM3724 V_{CC}.

The pull up resistor is calculated so that maximum current flow into $\overline{RESET}$ is less than 10 mA when activated. The resistor must be small enough so that the leakage current of all connected devices does not create an excessive voltage drop when the output is not activated. A resistor value of 100 kΩ will generally suffice.

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NEGATIVE-GOING V_{CC} TRANSIENTS

The LM3722/LM3723/LM3724 are relatively immune to short negative-going transients or glitches on V_{CC}. Figure 14 shows the maximum pulse width a negative-going V_{CC} transient can have without causing a reset pulse. In general, as the magnitude of the transient increases, going further below the threshold, the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 125 mV below the reset threshold and lasts 40 µs or less will not cause a reset pulse. A 0.1 µF bypass capacitor mounted as close as possible to the V_{CC} pin will provide additional transient rejection.

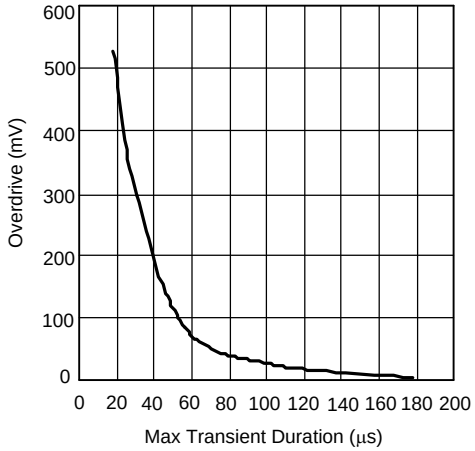


Figure 14. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

INTERFACING TO µPS WITH BIDIRECTIONAL RESET PINS

Microprocessors with bidirectional reset pins, such as the Motorola 68HC11 series, can be connected to the LM3722 $\overline{\text{RESET}}$ output. To ensure a correct output on the LM3722 even when the microprocessor reset pin is in the opposite state, connect a 4.7kΩ resistor between the LM3722 $\overline{\text{RESET}}$ output and the µP reset pin, as shown in Figure 15. Buffer the LM3722 $\overline{\text{RESET}}$ output to other system components.

Typical Application Circuits

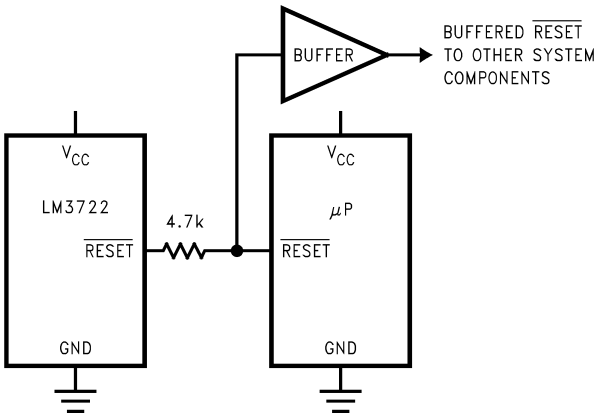


Figure 15. Interfacing to Microprocessors with Bidirectional Reset I/O

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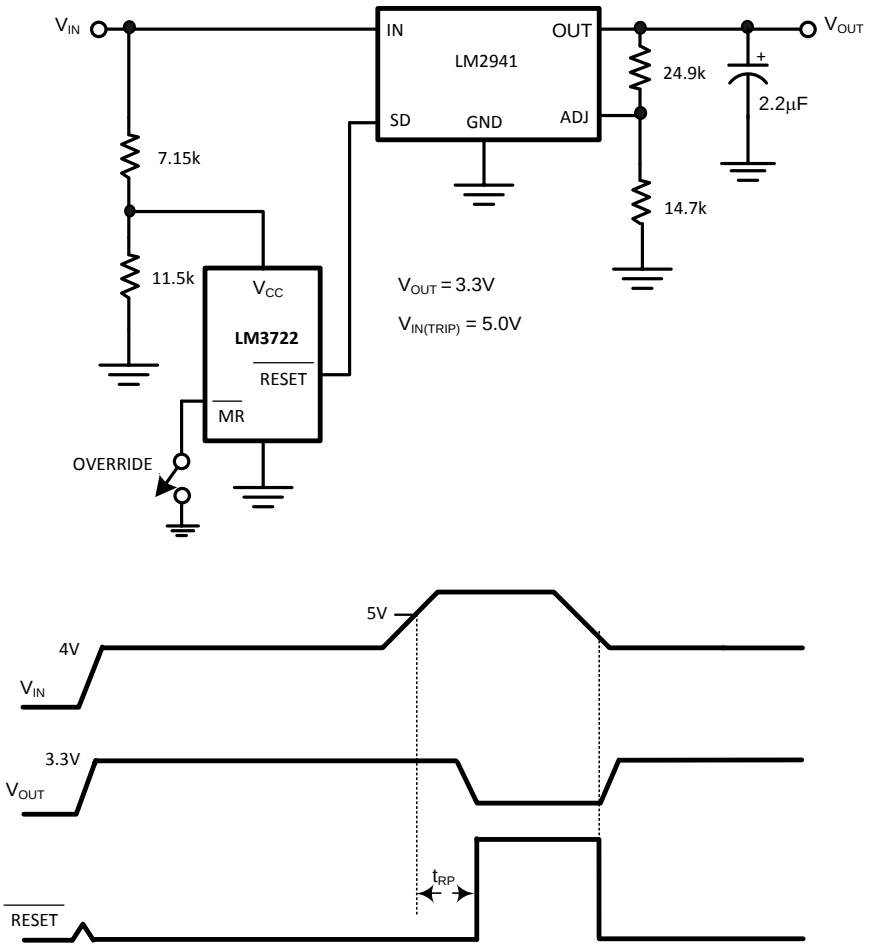


Figure 16. Regulator/Switch with Long-Term Overvoltage Lockout Prevents Overdissipation in Linear Regulator

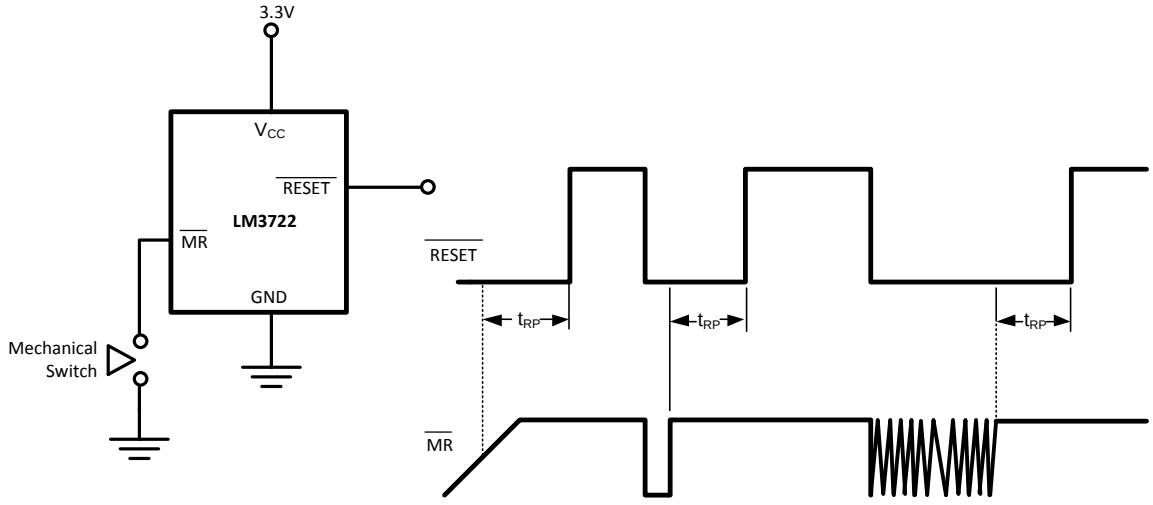


Figure 17. LM3722 Switch Debouncer

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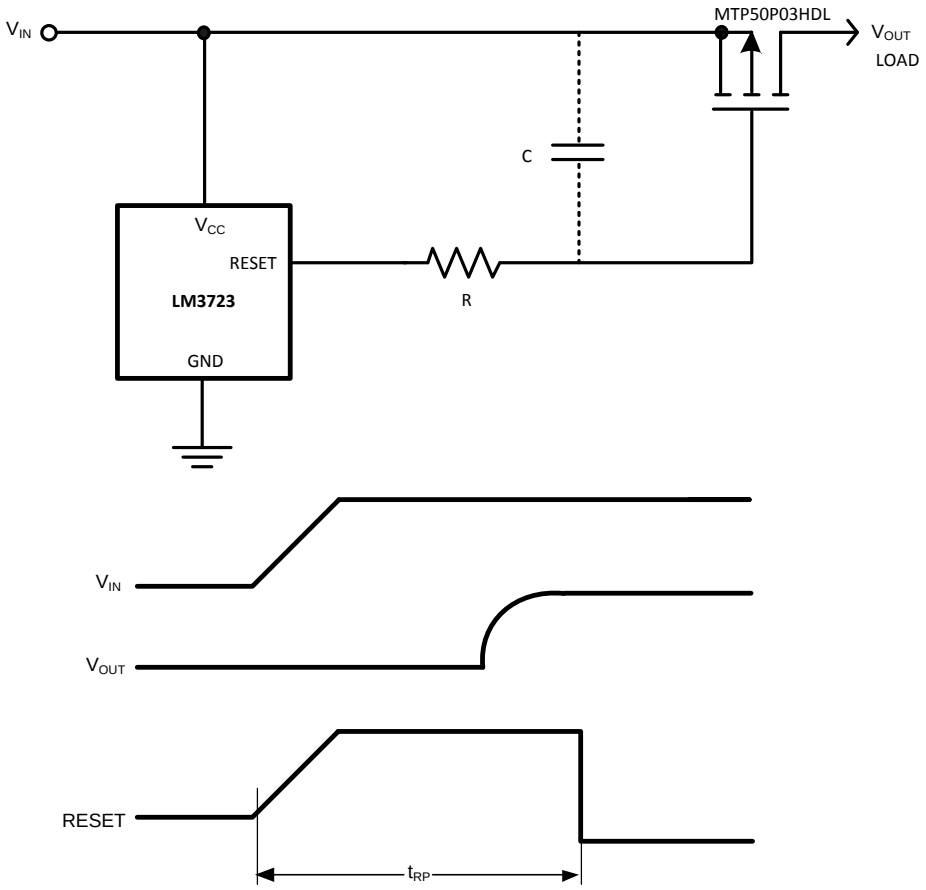


Figure 18. LM3723 Power-On Delay

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3724EM5-3.08/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	R63B	Samples
LM3724EM5-4.63/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	R62B	Samples
LM3724IM5-2.32/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R50B	Samples
LM3724IM5-3.08/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R53B	Samples
LM3724IM5-4.63/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R55B	Samples
LM3724IM5X-3.08/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R53B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

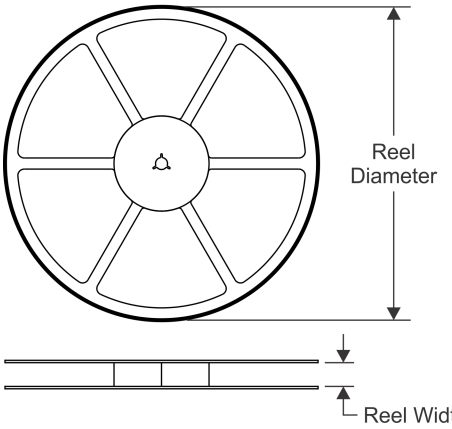
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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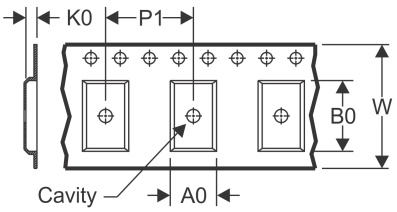
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

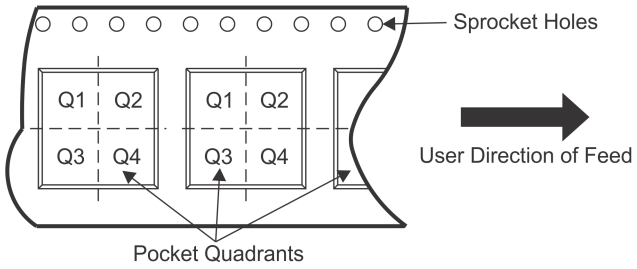


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

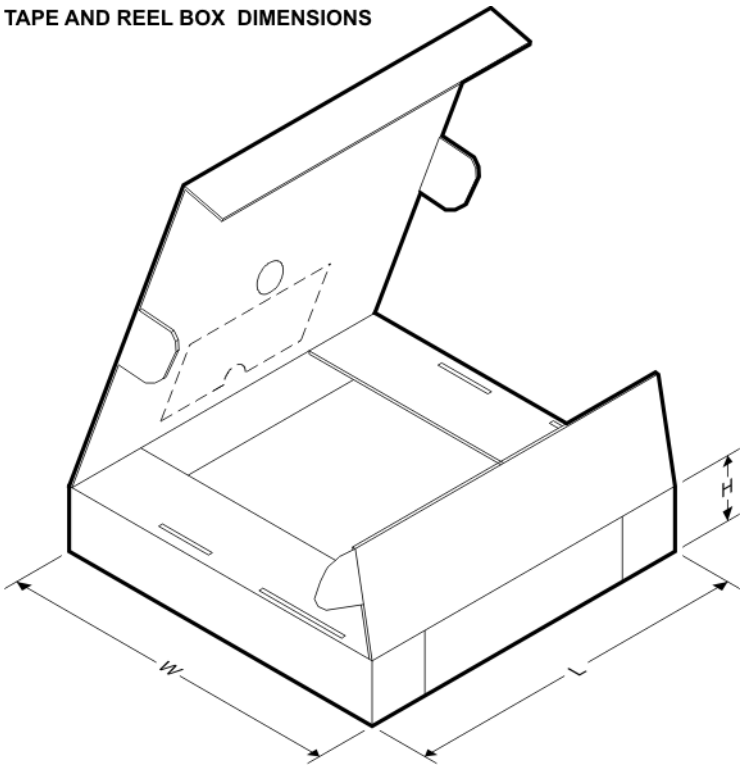
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3724EM5-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3724EM5-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3724IM5-2.32/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3724IM5-3.08/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3724IM5-4.63/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3724IM5X-3.08/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

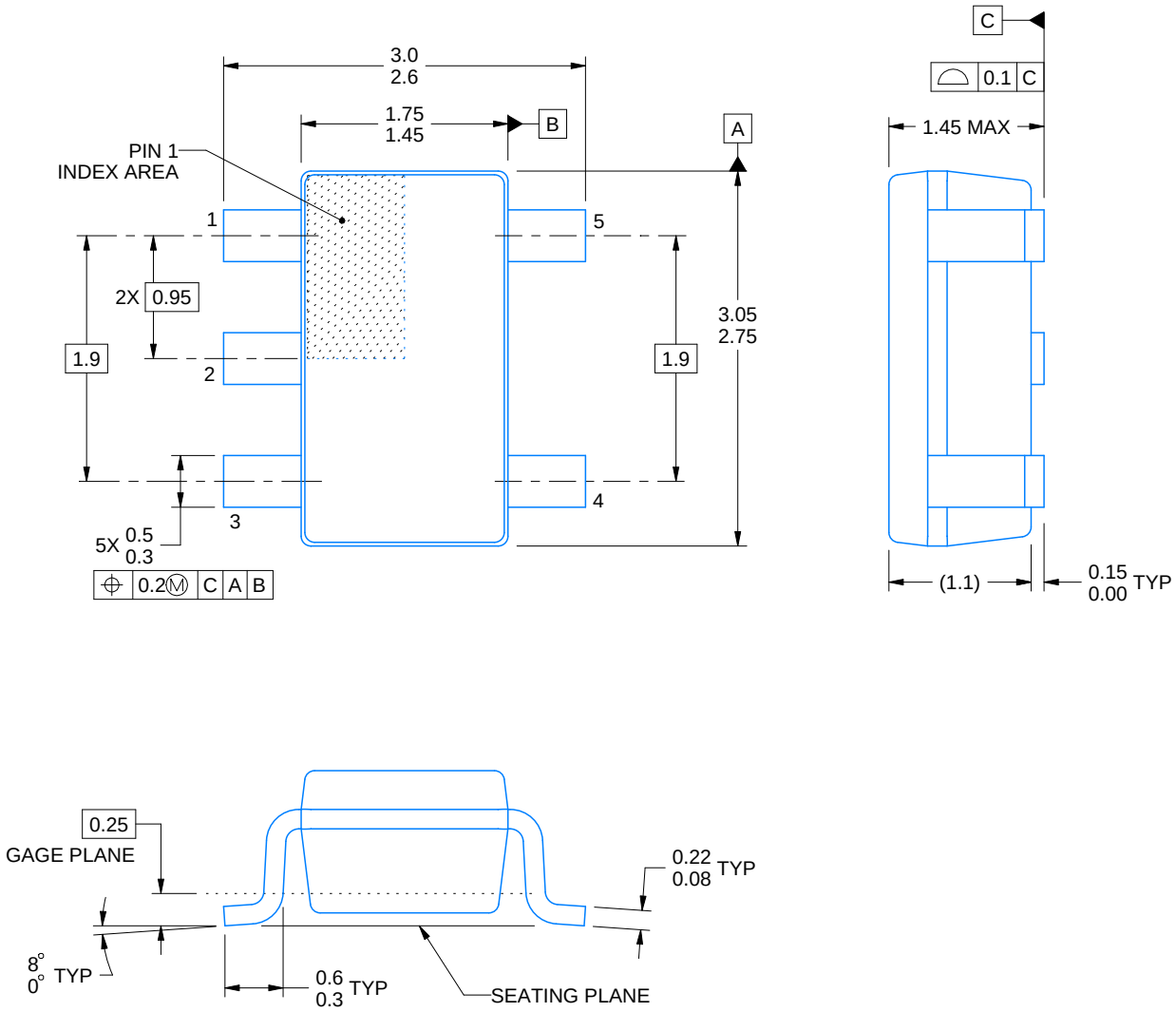
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3724EM5-3.08/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3724EM5-4.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3724IM5-2.32/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3724IM5-3.08/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3724IM5-4.63/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3724IM5X-3.08/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

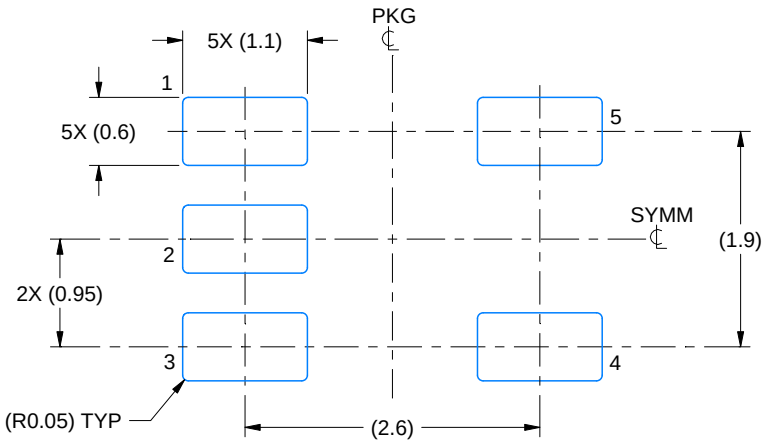
SMALL OUTLINE TRANSISTOR



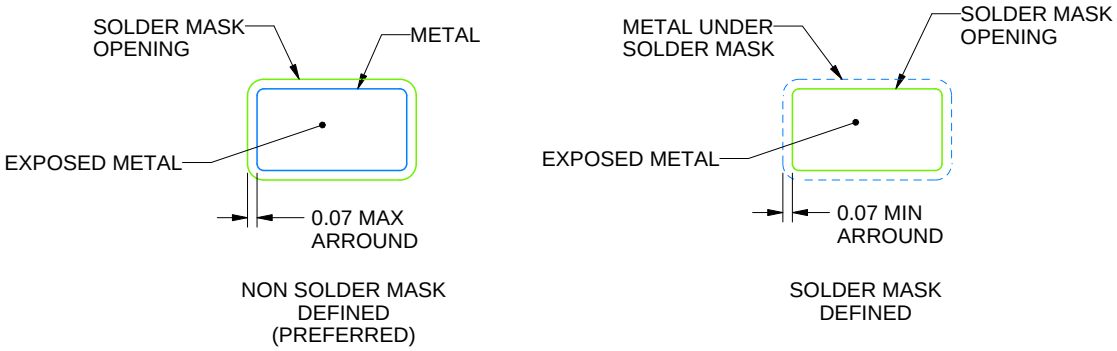
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

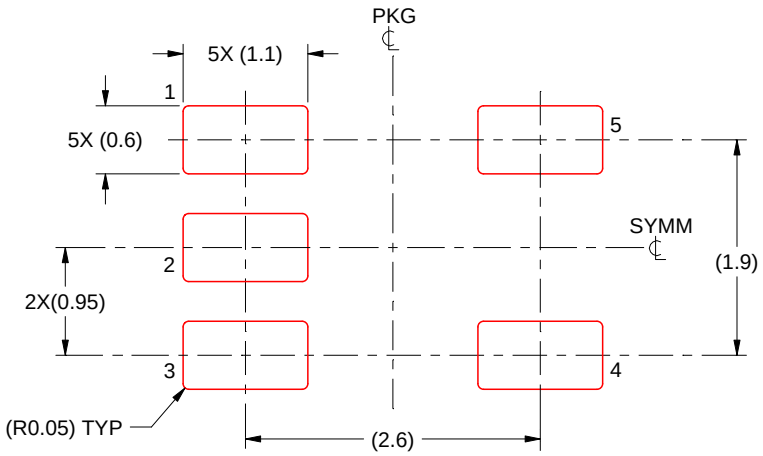


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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