

带看门狗计时器的 TPS382x 电压监视器

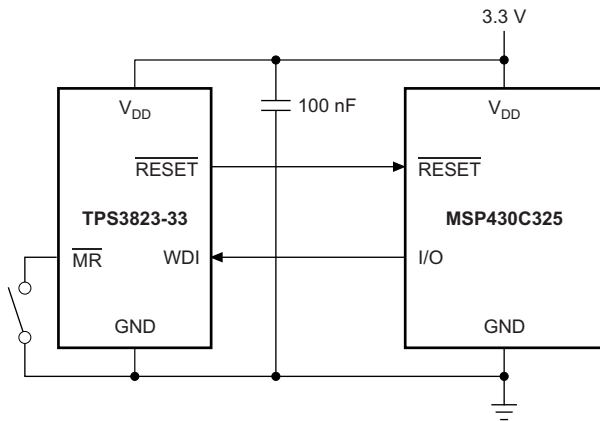
1 特性

- 具有固定延迟时间 200ms (TPS3823/4/5/8) 或 25ms (TPS3820) 的上电复位发生器
- 手动复位输入 (TPS3820/3/5/8)
- 复位输出提供低电平有效 (TPS3820/3/4/5)、高电平有效 (TPS3824/5) 和漏极开路 (TPS3828)
- 电源电压监控范围：
2.5V、3V、3.3V、5V
- 看门狗计时器 (TPS3820/3/4/8)
- 电源电流 15 μ A (典型值)
- 5 引脚 SOT-23 封装
- 温度范围：-40°C 至 85°C

2 应用

- DSP、微控制器或微处理器
- 工业设备
- 可编程控制器
- 汽车系统
- 便携式和电池供电类设备
- 智能仪表
- 无线通信系统
- 笔记本和台式计算机

典型应用原理图



3 说明

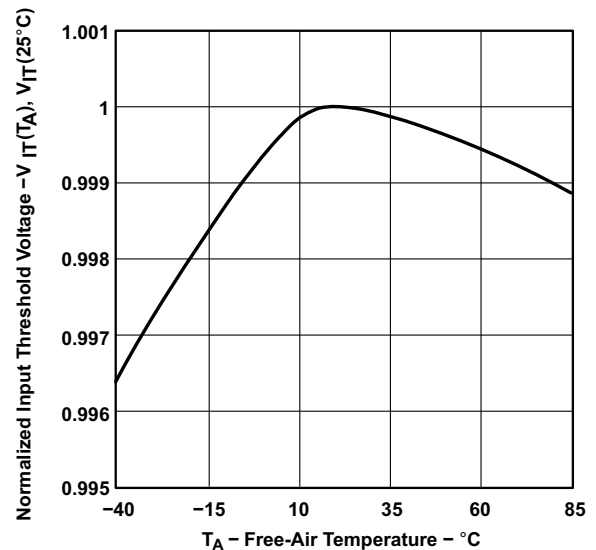
TPS382x 系列监控器主要为 DSP 和基于处理器的系统提供电路初始化和计时监测等功能。上电期间， $\overline{\text{RESET}}$ 会在电源电压 V_{DD} 超出 1.1V 时置为有效。因此只要满足以下条件，电源电压监控器就会监测 V_{DD} 并将 $\overline{\text{RESET}}$ 保持为低电平有效： V_{DD} 保持在阈值电压 $V_{\text{IT-}}$ 以下。内部计时器将会延迟输出恢复至无效状态（高电平）的时间，以确保系统正常复位。延迟时间 t_{d} 始于 V_{DD} 上升至高于阈值电压 ($V_{\text{IT-}} + V_{\text{HYS}}$)。当电源电压降到阈值电压 $V_{\text{IT-}}$ 以下时，输出再次变为有效状态（低电平）。无需外部组件。该系列中的所有器件均具有一个通过内部分压器设定的固定检测阈值电压 $V_{\text{IT-}}$ 。TPS382x 系列还提供 200ms (TPS3820) 和 1.6s (TPS3823/4/8) 的看门狗超时选项。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS382x	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

标准化输入阈值电压与大气温度间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision K (November 2015) to Revision L

Page

•	Changed the $\overline{\text{RESET}}$ columns for the TPS3824 and TPS3828 devices	4
•	Removed 'Open-drain' from the RESET column for the TPS3828 device	4
•	Changed text in the $\overline{\text{MR}}$ pin description from: RESET to: $\overline{\text{RESET}}$	4

Changes from Revision J (April 2013) to Revision K

Page

•	已添加 ESD 额定值表，特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
•	已更改 首页图	1
•	Changed <i>Pin Configuration and Functions</i> section; updated table format	4
•	Changed "free-air temperature" to "junction temperature" in <i>Absolute Maximum Ratings</i> condition statement	5
•	Deleted <i>Soldering temperature</i> specification from <i>Absolute Maximum Ratings</i> table	5
•	Changed <i>clamp current</i> to <i>current</i> specifications in <i>Absolute Maximum Ratings</i> table	5
•	Changed Removed V_I from <i>Absolute Maximum Ratings</i> table	5
•	Changed Removed V_{SENSE} from <i>Recommended Operating Conditions</i> table	5
•	Changed free-air temperature to junction temperature in <i>Electrical Characteristics</i> condition statement	6
•	Changed " T_A " to " T_J " in <i>Timing Requirements</i> condition statement	7
•	Changed " T_A " to " T_J " in <i>Switching Characteristics</i> condition statement	7
•	Added footnote (3) to <i>Functional Block Diagram</i>	10
•	Changed part number shown in Figure 9	12
•	Changed Figure 11	14

Changes from Revision I (February 2013) to Revision J
Page

• Added TPS382xA-33 to second $\overline{\text{RESET}}$ row of V_{OH} parameter in <i>Electrical Characteristics</i> table	6
• Added TPS382xA-33 to third $\overline{\text{RESET}}$ row of V_{OL} parameter in <i>Electrical Characteristics</i> table	6
• Corrected typo in V_{OL} RESET parameter test conditions	6
• Added TPS382xA-33 to third and seventh rows of V_{IT-} parameter in <i>Electrical Characteristics</i> table	6
• Added TPS382xA-33 to third row of V_{hys} parameter in <i>Electrical Characteristics</i> table	6
• Added TPS382xA-33 to third row of I_{OS} parameter in <i>Electrical Characteristics</i> table	7
• Added TPS3823A to second row of t_{out} parameter in <i>Switching Characteristics</i> table	7
• Added TPS3823A to second row of t_d parameter in <i>Switching Characteristics</i> table	7
• Added TPS3823A to first row of t_{PHL} parameter in <i>Switching Characteristics</i> table	7

Changes from Revision H (July 2012) to Revision I
Page

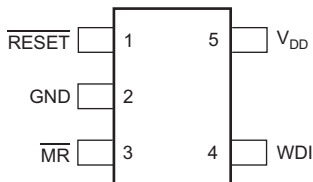
• Added last row of <i>Terminal Functions</i> table to Package Information table	4
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5 Device Comparison Table

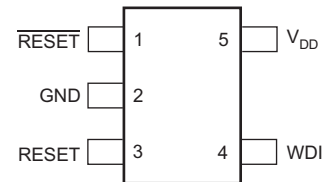
DEVICE	RESET	$\overline{\text{RESET}}$	WDI	$\overline{\text{MR}}$
TPS3820		Push-pull	X	X
TPS3823		Push-pull	X	X
TPS3823A		Push-pull	X	X
TPS3824	Push-pull	Push-pull	X	
TPS3825	Push-pull	Push-pull		X
TPS3828		Open-drain	X	X

6 Pin Configuration and Functions

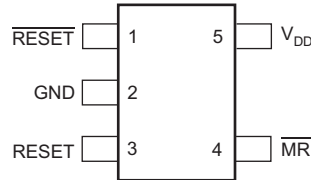
**TPS3820, TPS3823, TPS3823A, TPS3828: DBV PACKAGE
5-Pin SOT-23
Top View**



**TPS3824: DBV PACKAGE
5-Pin SOT-23
Top View**



**TPS3825: DBV PACKAGE
5-Pin SOT-23
Top View**



Pin Functions

NAME	PIN			I/O	DESCRIPTION
	TPS3820, TPS3823, TPS3823A, TPS3828	TPS3824	TPS3825		
GND	2	2	2	—	Ground connection
$\overline{\text{MR}}$	3	—	4	I	Manual-reset input. Pull low to force a reset. $\overline{\text{RESET}}$ remains low as long as $\overline{\text{MR}}$ is low and for the time-out period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V_{DD} when unused.
RESET	—	3	3	O	Active-high reset output. Either push-pull or open-drain output stage.
$\overline{\text{RESET}}$	1	1	1	O	Active-low reset output. Either push-pull or open-drain output stage.
V_{DD}	5	5	5	I	Supply voltage. Powers the device and monitors its own voltage.
WDI	4	4	—	I	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge. If unused, the WDI connection must be high impedance to prevent it from causing a reset event.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
Voltage	V _{DD}	-0.3	6	V
	RESET, $\overline{\text{RESET}}$, MR, WDI	-0.3	(V _{DD} + 0.3)	
Current	Maximum low output, I _{OL}	-5	5	mA
	Maximum high output, I _{OH}	-5	5	
	Output range (V _O < 0 or V _O > V _{DD}), I _{OK}	-10	10	
Continuous total power dissipation		See Thermal Information		
Temperature	Operating free-air, T _A	-40	85	°C
	Storage, T _{stg}	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	1.1		5.5	V
V _{IH}	High-level input voltage at $\overline{\text{MR}}$ and WDI	0.7 × V _{DD}			V
V _{IL}	Low-level input voltage			0.3 × V _{DD}	V
Δt/ΔV	Input transition rise and fall rate at $\overline{\text{MR}}$ or WDI			100	ns/V
T _A	Operating free-air temperature	-40		85	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS382x	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	209.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	72.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	36.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	35.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

7.5 Electrical Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OH}	High-level output voltage	RESET	TPS382x-25	V _{DD} = V _{IT-} + 0.2 V, I _{OH} = -20 μA	0.8 × V _{DD}	V _{DD} - 1.5 V	V	
			TPS382x-30 TPS382x-33 TPS382xA-33					V _{DD} = V _{IT-} + 0.2 V, I _{OH} = -30 μA
		TPS382x-50	V _{DD} = V _{IT-} + 0.2 V, I _{OH} = -120 μA					
		RESET	TPS3824-25 TPS3825-25	V _{DD} ≥ 1.8 V, I _{OH} = -100 μA				
	TPS3824-30 TPS3825-30	V _{DD} ≥ 1.8 V, I _{OH} = -150 μA						
	TPS3824-33 TPS3825-33							
	TPS3824-50 TPS3825-50							
V _{OL}	Low-level output voltage	RESET	TPS3824-25 TPS3825-25	V _{DD} = V _{IT-} + 0.2 V, I _{OL} = 1 mA	0.4	V		
			TPS3824-30 TPS3825-30	V _{DD} = V _{IT-} + 0.2 V, I _{OL} = 1.2 mA				
			TPS3824-33 TPS3825-33	V _{DD} = V _{IT-} + 0.2 V, I _{OL} = 3 mA				
			TPS3824-50 TPS3825-50	V _{DD} = V _{IT-} + 0.2 V, I _{OL} = 3 mA				
		RESET	TPS382x-25	V _{DD} = V _{IT-} - 0.2 V, I _{OL} = 1 mA	0.4			
			TPS382x-30	V _{DD} = V _{IT-} - 0.2 V, I _{OL} = 1.2 mA				
			TPS382x-33 TPS382xA-33					
			TPS382x-50	V _{DD} = V _{IT-} - 0.2 V, I _{OL} = 3 mA				
Power-up reset voltage ⁽¹⁾			V _{DD} ≥ 1.1 V, I _{OL} = 20 μA			0.4	V	
V _{IT-}	Negative-going input threshold voltage ⁽²⁾	RESET	TPS382x-25	T _A = 0°C to 85°C	2.21	2.25	2.30	V
			TPS382x-30		2.59	2.63	2.69	
			TPS382x-33 TPS382xA-33		2.88	2.93	3	
			TPS382x-50		4.49	4.55	4.64	
		RESET	TPS382x-25	T _A = -40°C to 85°C	2.20	2.25	2.30	
			TPS382x-30		2.57	2.63	2.69	
			TPS382x-33 TPS382xA-33		2.86	2.93	3	
			TPS382x-50		4.46	4.55	4.64	
V _{hys}	Hysteresis at V _{DD} input	TPS382x-25		30	mV			
		TPS382x-30						
		TPS382x-33 TPS382xA-33						
		TPS382x-50				50		
I _{IH(AV)}	Average high-level input current	WDI	WDI = V _{DD} , time average (DC = 88%)	120	μA			
I _{IL(AV)}	Average low-level input current		WDI = 0.3 V, V _{DD} = 5.5 V time average (DC = 12%)	-15				
I _{IH}	High-level input current	WDI	WDI = V _{DD}	140	190	μA		
		MR	MR = V _{DD} × 0.7, V _{DD} = 5.5 V	-40	-60			
I _{IL}	Low-level input current	WDI	WDI = 0.3 V, V _{DD} = 5.5 V	140	190	μA		
		MR	MR = 0.3 V, V _{DD} = 5.5 V	-110	-160			

 (1) The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) must be placed near the supply terminals.

Electrical Characteristics (continued)

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_{OS}	Output short-circuit current ⁽³⁾	\overline{RESET} $V_{DD} = V_{IT-, max} + 0.2 V, V_O = 0 V$			-400	μA	
							TPS382x-25
							TPS382x-30
							TPS382x-33 TPS382xA-33
	TPS382x-50				-800		
I_{DD}	Supply current	WDI, \overline{MR} , and outputs unconnected		15	25	μA	
	Internal pullup resistor at \overline{MR}			52		k Ω	
C_i	Input capacitance at \overline{MR} , WDI	$V_i = 0 V$ to 5.5 V		5		pF	

(3) The \overline{RESET} short-circuit current is the maximum pullup current when \overline{RESET} is driven low by a microprocessor bidirectional reset pin.

7.6 Timing Requirements

At $R_L = 1 M\Omega$, $C_L = 50 pF$, and $T_J = 25^\circ C$, unless otherwise noted.

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD} $V_{DD} = V_{IT-} + 0.2 V, V_{DD} = V_{IT-} - 0.2 V$	6			μs
		at \overline{MR} $V_{DD} \geq V_{IT-} + 0.2 V, V_{IL} = 0.3 \times V_{DD}, V_{IH} = 0.7 \times V_{DD}$	1			μs
		at WDI $V_{DD} \geq V_{IT-} + 0.2 V, V_{IL} = 0.3 \times V_{DD}, V_{IH} = 0.7 \times V_{DD}$	100			ns

7.7 Switching Characteristics

At $R_L = 1 M\Omega$, $C_L = 50 pF$, and $T_J = 25^\circ C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{out}	Watchdog time out	TPS3820 $V_{DD} \geq V_{IT-} + 0.2 V$	112	200	300	ms
		TPS3823/4/8, TPS3823A See Figure 1	0.9	1.6	2.5	s
t_d	Delay time	TPS3820 $V_{DD} \geq V_{IT-} + 0.2 V$	15	25	37	ms
		TPS3823/4/5/8, TPS3823A See Figure 1	120	200	300	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	\overline{MR} to \overline{RESET} delay (TPS3820/3/5/8, TPS3823A) $V_{DD} \geq V_{IT-} + 0.2 V, V_{IL} = 0.3 \times V_{DD}, V_{IH} = 0.7 \times V_{DD}$			0.1	μs
		V_{DD} to \overline{RESET} delay $V_{IL} = V_{IT-} - 0.2 V, V_{IH} = V_{IT-} + 0.2 V$			25	
t_{PLH}	Propagation (delay) time, low-to-high-level output	\overline{MR} to \overline{RESET} delay (TPS3824/5) $V_{DD} \geq V_{IT-} + 0.2 V, V_{IL} = 0.3 \times V_{DD}, V_{IH} = 0.7 \times V_{DD}$			0.1	μs
		V_{DD} to \overline{RESET} delay (TPS3824/5) $V_{IL} = V_{IT-} - 0.2 V, V_{IH} = V_{IT-} + 0.2 V$			25	

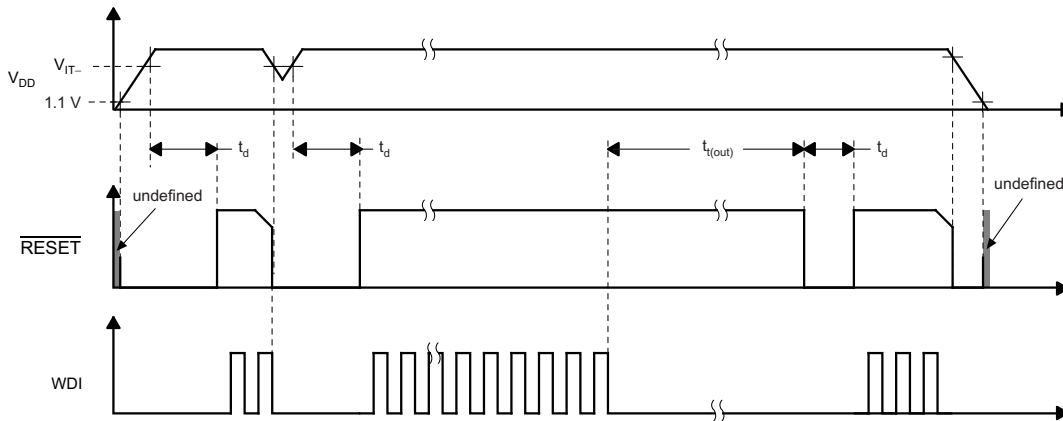


Figure 1. Timing Diagram

7.8 Typical Characteristics

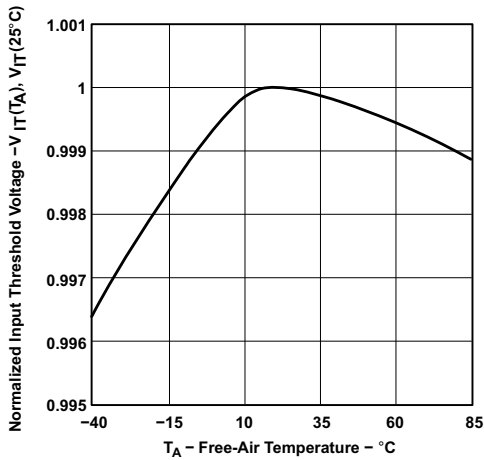


Figure 2. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

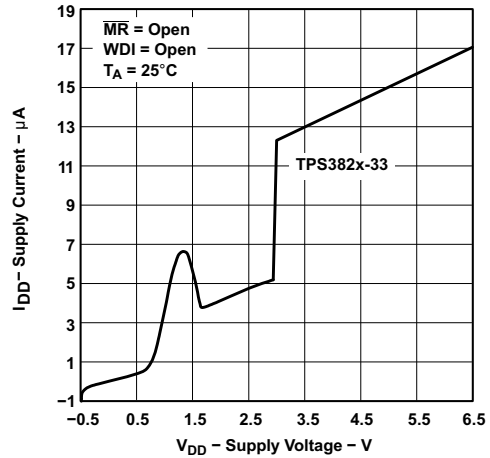


Figure 3. Supply Current vs Supply Voltage

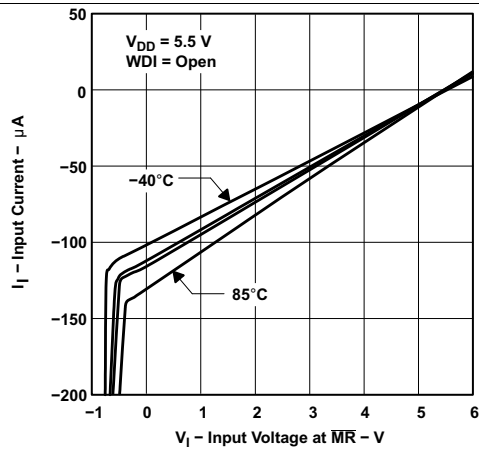


Figure 4. Input Current vs Input Voltage at \overline{MR}

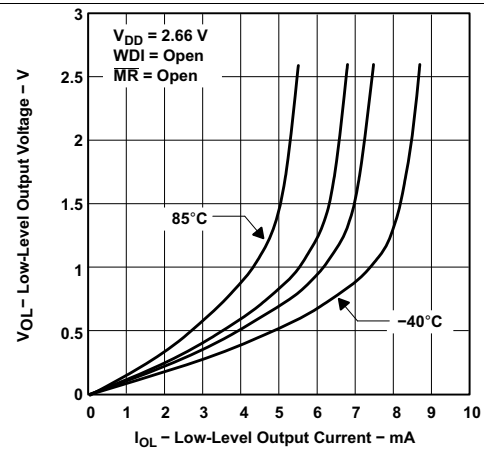


Figure 5. Low-Level Output Voltage vs Low-Level Output Current

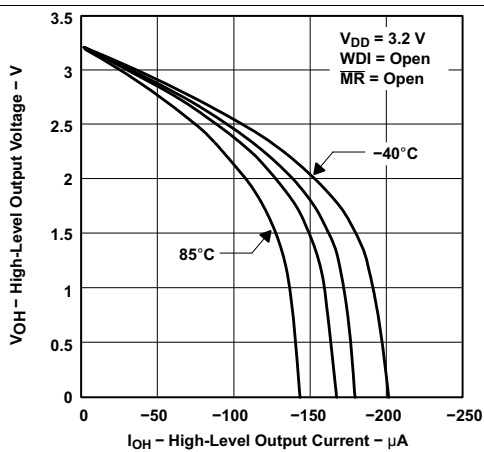


Figure 6. High-Level Output Voltage vs High-Level Output Current

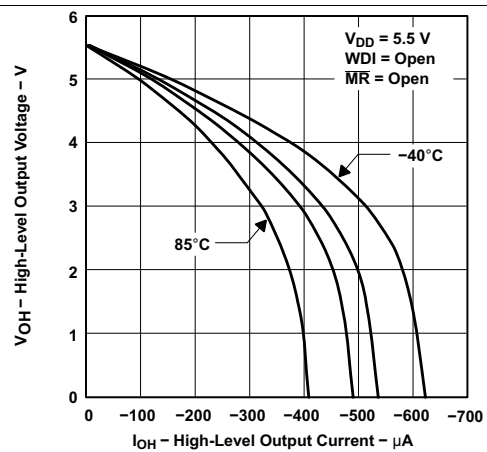
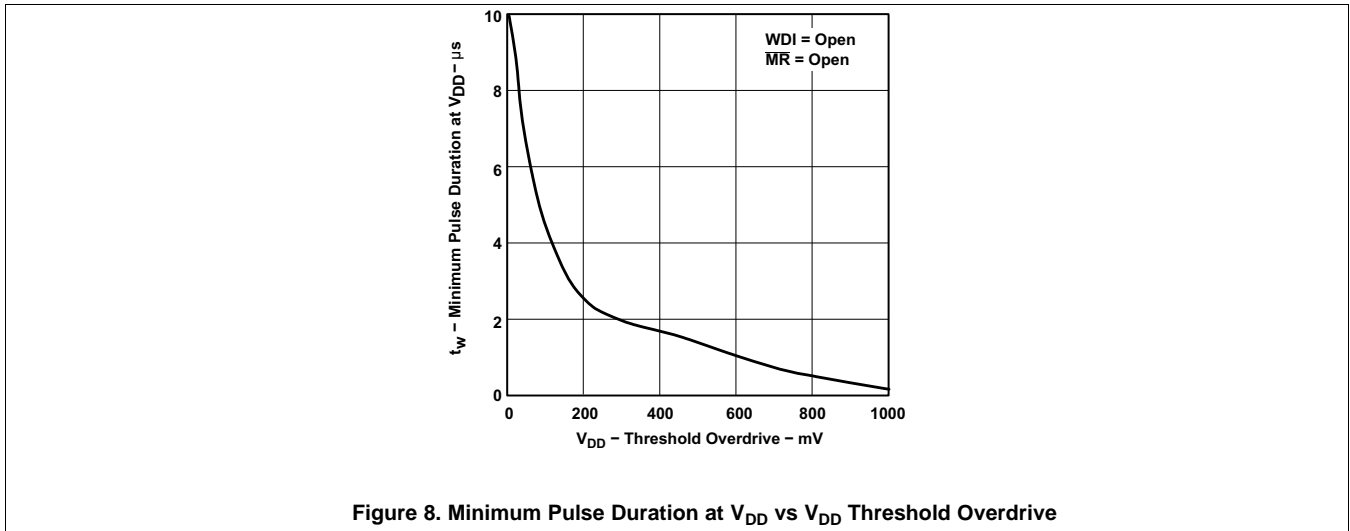


Figure 7. High-Level Output Voltage vs High-Level Output Current

Typical Characteristics (continued)



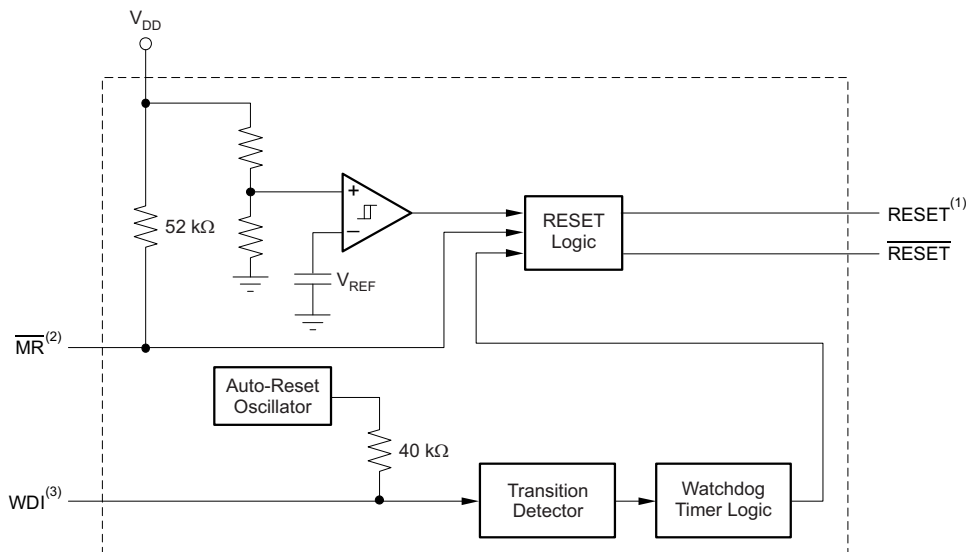
8 Detailed Description

8.1 Overview

The TPS382x family of supervisors provide circuit initialization and timing supervision. Optional configurations include devices with active-high and active-low output signals (TPS3824/5), devices with a watchdog timer (TPS3820/3/4/8), and devices with manual reset ($\overline{\text{MR}}$) pins (TPS3820/3/5/8). $\overline{\text{RESET}}$ asserts when the supply voltage, V_{DD} , rises above 1.1 V. For devices with active-low output logic, the device monitors V_{DD} and keeps $\overline{\text{RESET}}$ low as long as V_{DD} remains below the negative threshold voltage, $V_{\text{IT-}}$. For devices with active-high output logic, $\overline{\text{RESET}}$ remains high as long as V_{DD} remains below $V_{\text{IT-}}$. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d , starts after V_{DD} rises above the positive threshold voltage ($V_{\text{IT-}} + V_{\text{HYS}}$). When the supply voltage drops below $V_{\text{IT-}}$, the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage, $V_{\text{IT-}}$, set by an internal voltage divider, so no external components are required.

The TPS382x family is designed to monitor supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The devices are available in a 5-pin SOT-23 package and are characterized for operation over a temperature range of -40°C to 85°C .

8.2 Functional Block Diagram



(1) TPS3824/5

(2) TPS3820/3/5/8

(3) TPS3820/3/4/8

8.3 Feature Description

8.3.1 Manual Reset ($\overline{\text{MR}}$)

The $\overline{\text{MR}}$ input allows an external logic signal from processors, logic circuits, and/or discrete sensors to force a reset signal regardless of V_{DD} with respect to $V_{\text{IT-}}$ or the state of the watchdog timer. A low level at $\overline{\text{MR}}$ causes the reset signals to become active.

8.3.2 Active-High or Active-Low Output

All TPS382x devices have an active-low logic output ($\overline{\text{RESET}}$), while the TPS3824/5 devices also include an active-high logic output (RESET).

8.3.3 Push-Pull or Open-Drain Output

All TPS382x devices, except for TPS3828, have push-pull outputs. TPS3828 devices have an open-drain output.

Feature Description (continued)

8.3.4 Watchdog Timer (WDI)

The TPS3820, TPS3823, TPS3824, and TPS3828 devices have a watchdog timer that must be periodically triggered by either a positive or negative transition at WDI to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{out} , RESET becomes active for the time period t_q . This event also reinitializes the watchdog timer.

The watchdog timer can be disabled by disconnecting the WDI pin from the system. If the WDI pin detects that it is in a high-impedance state, the TPS3820, TPS3823, TPS3824, or TPS3828 will generate its own WDI pulse to ensure that $\overline{\text{RESET}}$ does not assert. If this behavior is not desired, place a 1-k Ω resistor from WDI to ground. This resistor will help ensure that the TPS3820, TPS3823, TPS3824, or TPS3828 detects that WDI is not in a high-impedance state.

In applications where the input to the WDI pin is active (transitioning high and low) and the TPS3820, TPS3823, TPS3824, or TPS3828 is asserting $\overline{\text{RESET}}$, $\overline{\text{RESET}}$ is stuck at a logic low after the input voltage returns above V_{IT} . If the application requires that input to WDI be active when the reset signal is asserted, then either the **A** version of the device or a FET should be used to decouple the WDI signal. The **A** version does not latch the reset signal to the asserted state if a WDI pulse is received while RESET is asserted. An external FET decouples the WDI signal by disconnecting the WDI input when $\overline{\text{RESET}}$ is asserted. For more details on this, see [Decoupling WDI During Reset Event](#). The **A** version of the device does not require this FET, but it does operate in circuits that have it. Therefore, the **A** version is backwards-compatible with the non-**A** versions.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TPS382x devices.

Table 1. Function Table

INPUTS		OUTPUTS	
$\overline{\text{MR}}$ ⁽¹⁾	$V_{\text{DD}} > V_{\text{IT}}$	$\overline{\text{RESET}}$	RESET ⁽²⁾
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

(1) TPS3820/3/5/8

(2) TPS3824/5

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS382x family of devices are very small supervisory circuits that monitor fixed supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The TPS382x family operates from 1.1 V to 5.5 V. Orderable options include versions with either push-pull or open-drain outputs, versions that use active-high or active-low logic for output signals, versions with a manual reset pin, and versions with a watchdog timer. See the [Device Comparison Table](#) for an overview of device options.

9.2 Typical Applications

9.2.1 Supply Rail Monitoring With Watchdog Time-Out and 200-ms Delay

The TPS3823A can be used to monitor the supply rail for devices such as microcontrollers. The downstream device is enabled by the TPS3823A once the voltage on the supply pin (V_{DD}) is above the internal threshold voltage ($V_{IT+} + V_{HYS}$). The downstream device is disabled by the TPS3823A when V_{DD} falls below the threshold voltage minus the hysteresis voltage (V_{IT-}). The TPS3823A also issues a reset signal if the WDI input is not periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{out} , \overline{RESET} becomes active for the time period t_d .

Some applications require a shorter reset signal than the 200 ms that most of the TPS382x family provide. In these cases, the TPS3820 is a good choice because it has a delay time of only 25 ms. If an open-drain output is required, replace the TPS3823A with the TPS3828 (if the WDI input must be active while \overline{RESET} is low, see [Decoupling WDI During Reset Event](#)). [Figure 9](#) shows the TPS3823A in a typical application.

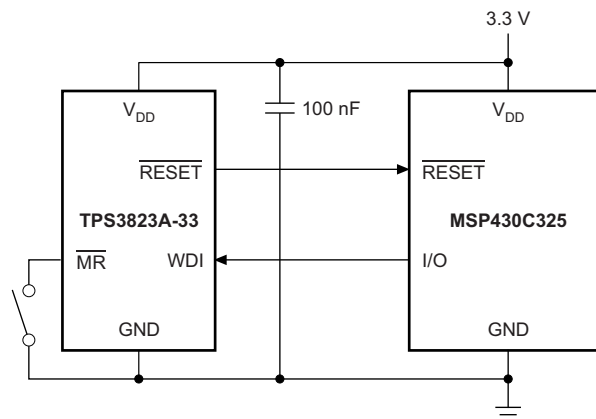


Figure 9. Supply Rail Monitoring With Watchdog Time-Out

9.2.1.1 Design Requirements

The TPS3823A must drive the enable pin of a MSP430C325 using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device and monitor the I/O pin to determine if the microcontroller is operating correctly.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Determine which version of the TPS382x family best suits the functional performance required.

If the input supply is noisy, include an input capacitor to help avoid unwanted changes to the reset signal.

9.2.1.3 Application Curve

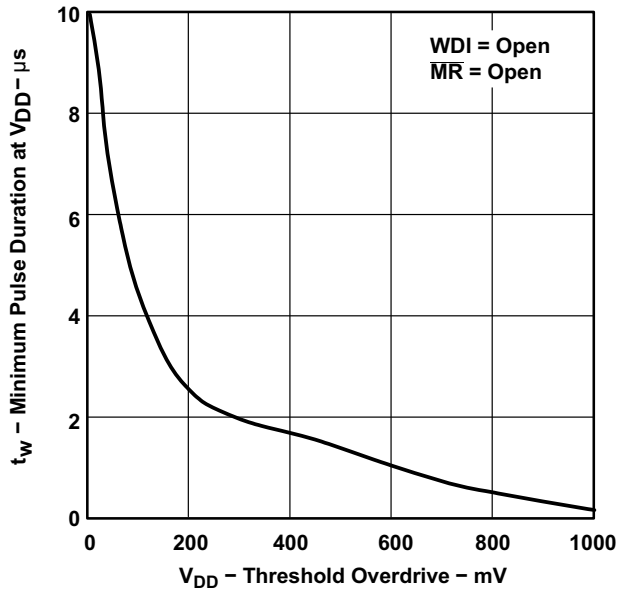


Figure 10. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

Typical Applications (continued)

9.2.2 Decoupling WDI During Reset Event

If the application requires that the input to WDI is active when the reset signal is asserted and the **A** version of the device cannot be used, [Figure 11](#) shows how to decouple WDI from the active signal using an N-channel FET. The N-channel FET is placed in series with the WDI pin, with the gate of the FET connected to the RESET output.

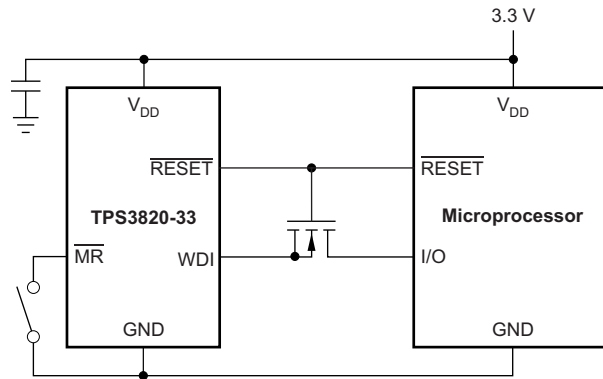


Figure 11. WDI Example

9.2.2.1 Design Requirements

The TPS3820 must drive the enable pin of a microprocessor using a logic-high signal to signify that the supply voltage is above the minimum operating voltage of the device and monitor the I/O pin to determine if the microcontroller is operating correctly. The reset signal delay time should be greater than 10 ms but less than 50 ms to achieve the desired behavior.

9.2.2.2 Detailed Design Procedure

Determine which version of the TPS3820 is best suited for monitoring the supply voltage.

If the input supply is noisy, include an input capacitor to help avoid unwanted changes to the reset signal.

9.2.2.3 Application Curve

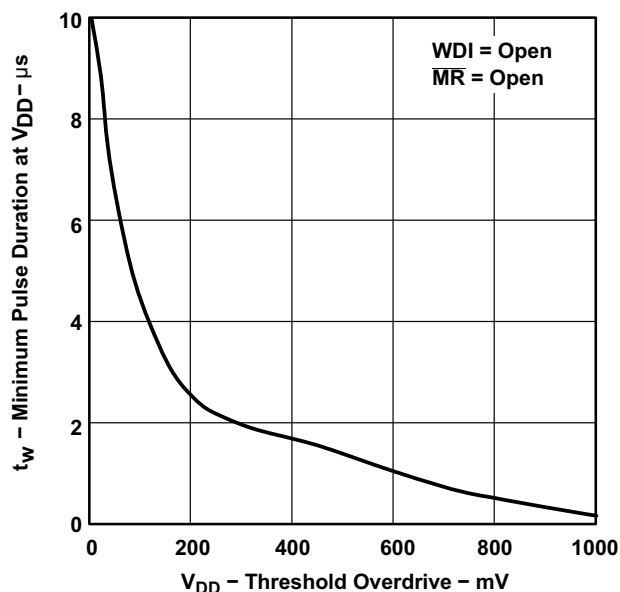


Figure 12. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 1.1 V to 5.5 V. Though not required, it is good analog design practice to place a 0.1- μ F ceramic capacitor close to the V_{DD} pin if the input supply is noisy.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit board (PCB) that is used for the TPS382x family of devices.

- Place the V_{DD} decoupling capacitor (C_{VDD}) close to the device.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{DD} voltage.

11.2 Layout Example

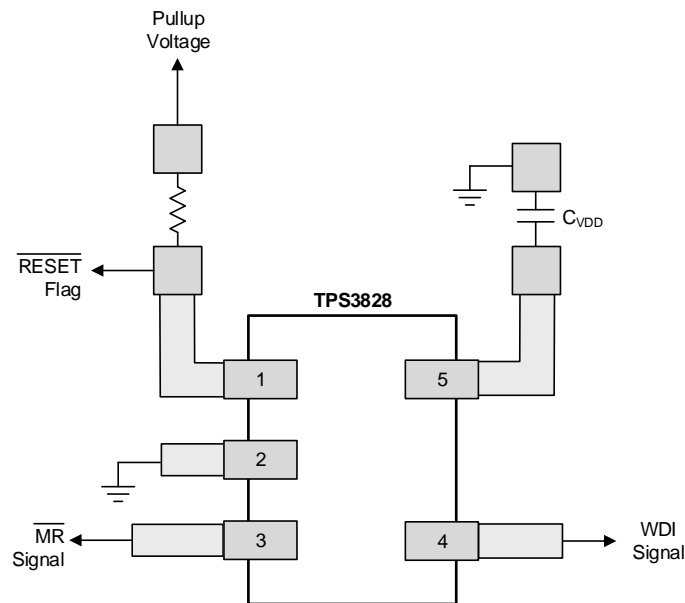


Figure 13. Example Layout (DBV Package)

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从产品文件夹中的工具与软件下获取 TPS382x 的 SPICE 模型。

12.1.2 器件命名规则

表 2. 订购信息⁽¹⁾

可订购器件名称 ⁽²⁾⁽³⁾		阈值电压 ⁽⁴⁾	标记
TPS3820-33DBVT	TPS3820-33DBVR	2.93V	PDEI
TPS3820-50DBVT	TPS3820-50DBVR	4.55V	PDDI
TPS3823-25DBVT	TPS3823-25DBVR	2.25V	PAPI
TPS3823-30DBVT	TPS3823-30DBVR	2.63V	PAQI
TPS3823-33DBVT	TPS3823-33DBVR	2.93V	PARI
TPS3823-50DBVT	TPS3823-50DBVR	4.55V	PASI
TPS3824-25DBVT	TPS3824-25DBVR	2.25V	PATI
TPS3824-30DBVT	TPS3824-30DBVR	2.63V	PAUI
TPS3824-33DBVT	TPS3824-33DBVR	2.93V	PAVI
TPS3824-50DBVT	TPS3824-50DBVR	4.55V	PAWI
TPS3825-33DBVT	TPS3825-33DBVR	2.93V	PDGI
TPS3825-50DBVT	TPS3825-50DBVR	4.55V	PDFI
TPS3828-33DBVT	TPS3828-33DBVR	2.93V	PDII
TPS3828-50DBVT	TPS3828-50DBVR	4.55V	PDHI
TPS3823A-33DBVT	TPS3823A-33DBVR	2.93V	PYPI

(1) 要获得最新的封装和订购信息，请见本文档末尾的封装选项附录，或者访问 TI 网站 www.ti.com。

(2) DBVT 封装表示卷带数量为 250 件。

(3) DBVR 封装表示卷带数量为 3000 件。

(4) 如需其他阈值电压版本，请与当地 TI 销售办事处联系。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

《禁用 TI 系列监控器的看门狗计时器》(SLVA145)

12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPS3820	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3823	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3824	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3825	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS3828	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3820-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDEI	Samples
TPS3820-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDEI	Samples
TPS3820-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDEI	Samples
TPS3820-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDEI	Samples
TPS3820-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDDI	Samples
TPS3820-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDDI	Samples
TPS3823-25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAPI	Samples
TPS3823-25DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAPI	Samples
TPS3823-25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAPI	Samples
TPS3823-25DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAPI	Samples
TPS3823-30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAQI	Samples
TPS3823-30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAQI	Samples
TPS3823-30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAQI	Samples
TPS3823-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PARI	Samples
TPS3823-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PARI	Samples
TPS3823-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PARI	Samples
TPS3823-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PARI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3823-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PASI	Samples
TPS3823-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PASI	Samples
TPS3823-50DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PASI	Samples
TPS3823A-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PYPI	Samples
TPS3823A-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PYPI	Samples
TPS3824-25DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PATI	Samples
TPS3824-25DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PATI	Samples
TPS3824-30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAUI	Samples
TPS3824-30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAUI	Samples
TPS3824-30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAUI	Samples
TPS3824-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAVI	Samples
TPS3824-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAVI	Samples
TPS3824-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAVI	Samples
TPS3824-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAVI	Samples
TPS3824-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PAWI	Samples
TPS3824-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAWI	Samples
TPS3824-50DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PAWI	Samples
TPS3825-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDGI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3825-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDGI	Samples
TPS3825-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDGI	Samples
TPS3825-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDGI	Samples
TPS3825-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDFI	Samples
TPS3825-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDFI	Samples
TPS3825-50DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDFI	Samples
TPS3828-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDII	Samples
TPS3828-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDII	Samples
TPS3828-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDII	Samples
TPS3828-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDII	Samples
TPS3828-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDHI	Samples
TPS3828-50DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDHI	Samples
TPS3828-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDHI	Samples
TPS3828-50DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDHI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3820-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3820-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3820-50DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3820-50DBVT	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3820-50DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3820-50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-25DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3823-25DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3823-25DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3823-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823-50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3823A-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3823A-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3824-25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-25DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-25DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-25DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-30DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-30DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3824-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3824-50DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3824-50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3825-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3825-33DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS3825-50DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3825-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3825-50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3828-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3828-33DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3828-50DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3828-50DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3820-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3820-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3820-50DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3820-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3820-50DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3820-50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3823-25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-25DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3823-25DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3823-25DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3823-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3823-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3823-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823-50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3823A-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3823A-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3824-25DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3824-25DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3824-25DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3824-25DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3824-30DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3824-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-30DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3824-30DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3824-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3824-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3824-50DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TPS3824-50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3825-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3825-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3825-50DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS3825-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3825-50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3828-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3828-33DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS3828-50DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS3828-50DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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