

具有可选输入时钟驱动器的低压 1:10 低电压正射极耦合逻辑 (LVPECL)

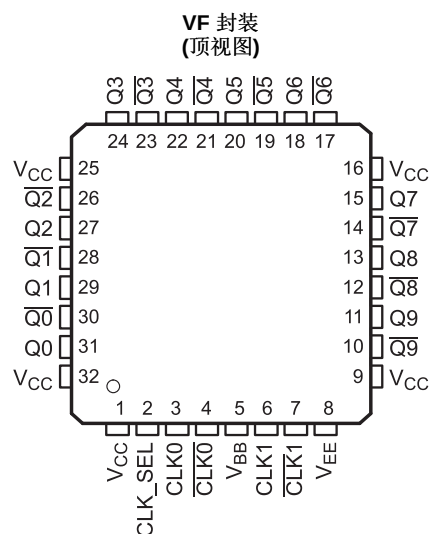
查询样品: **CDCLVP111-EP**

特性

- 将一个差分时钟输入对 **LVPECL** 分配至 **10** 个差分 **LVPECL**
- 与低压发射器耦合逻辑 (**LVECL**) 和 **LVPECL** 完全兼容
- 支持 **2.375V** 至 **3.8V** 的宽电源电压范围
- 通过 **CLK_SEL** 可选择时钟输入
- 针对时分应用的低输出偏斜 (典型值 **15ps**)
 - 额外抖动少于 **1ps**
 - 传播延迟少于 **355ps**
 - 开输入缺省状态
 - 低压差分信令 (**LVDS**), 电流模式逻辑 (**CML**), 短截线串联端接逻辑 (**SSTL**) 输入兼容
- 针对单端计时的 **V_{BB}** 基准电压输出
- 采用 **32** 引脚薄型方形扁平 (**LQFP**) 封装
- 频率范围介于 **DC** 至 **3.5GHz** 之间
- 与 **MC100** 系列 **EP111**, **ES6111**, **LVEP111**, **PTN1111** 引脚到引脚兼容

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用 (**-55°C** 至 **125°C**) 温度范围 ⁽¹⁾
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性



(1) 可定制工作温度范围

应用范围

- 设计用于驱动 **50Ω** 传输线路
- 高性能时分

说明

CDCLVP111 时钟驱动器使用最小的时分偏斜将 **LVPECL** 输入的一个差分时钟对 (**CLK0**, **CLK1**) 分频为差分 **LVPECL** 时钟 (**Q0**, **Q9**) 输出的十个对。CDCLVP111 可接受两个时钟源进入同一个输入复用器。CDCLVP111 专门设计用于驱动器 **50Ω** 传输线路。当一个输出引脚不被使用时, 建议将其保持在开状态以减少功耗。如果只使用差分对中的输出引脚中的一个, 那么其它输出引脚必须被同样地端接至 **50Ω**。

如果要求单端输入运行, **V_{BB}** 基准电压输出被使用。在这种情况下, **V_{BB}** 引脚应该被连接至 **CLK0** 并由一个 **10nF** 电容器旁通至接地 (**GND**)。

然而, 要实现高达 **3.5GHz** 的高速性能, 强烈建议使用差分模式。

CDCLVP111 额定工作温度范围是 **-55°C** 至 **125°C**。



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: **SCAS933**

CDCLVP111-EP

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www.ti.com.cn**Table 1. FUNCTION TABLE**

CLK_SEL	ACTIVE CLOCK INPUT
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

Table 2. ORDERING INFORMATION⁽¹⁾

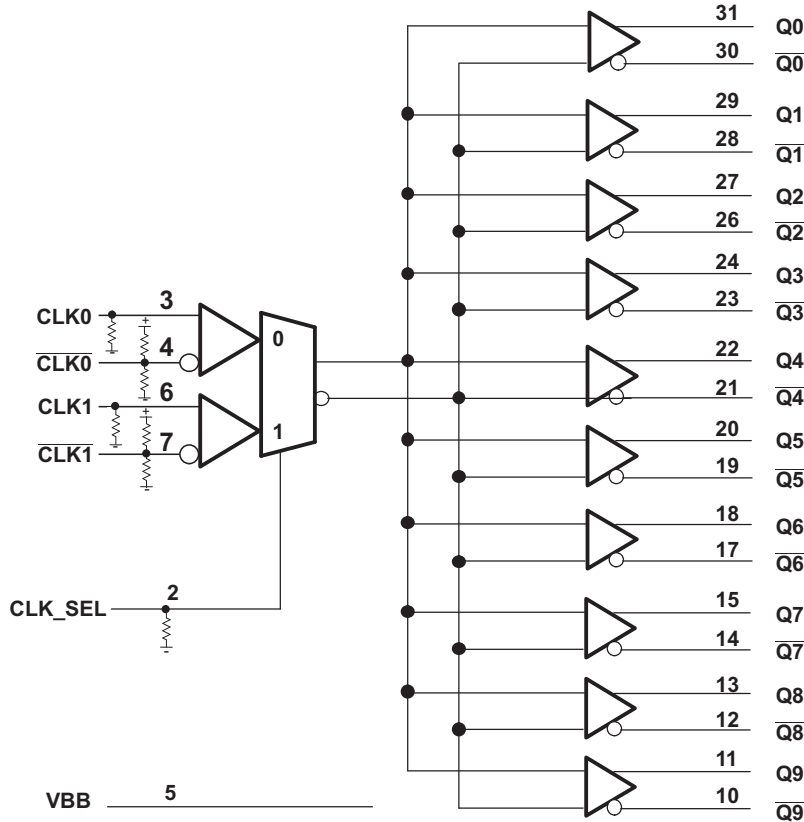
T _J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	LQFP - VF	CDCLVP111MVFREP	LVP111MEP	V62/12624-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION



PIN FUNCTIONS⁽¹⁾

PIN		DESCRIPTION
NAME	NO.	
CLK_SEL	2	Clock select. Used to select between CLK0 and CLK1 input pairs. LVTTTL/LVCMOS functionality compatible.
CLK0, $\overline{\text{CLK0}}$	3, 4	Differential LVECL/LVPECL input pair
CLK1, $\overline{\text{CLK1}}$	6, 7	
Q [9:0]	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	LVECL/LVPECL clock outputs, these outputs provide low-skew copies of CLK _n .
$\overline{\text{Q}}[9:0]$	10, 12, 14, 17, 19, 21, 23, 26, 28, 30	LVECL/LVPECL complementary clock outputs, these outputs provide copies of $\overline{\text{CLKn}}$.
V _{BB}	5	Reference voltage output for single-ended input operation
V _{CC}	1, 9, 16, 25, 32	Supply voltage
V _{EE}	8	Device ground or negative supply voltage in ECL mode

(1) CLK_n, CLK_SEL pull down resistor = 75 kΩ; $\overline{\text{CLKn}}$ pull up resistor = 37.5 kΩ; $\overline{\text{CLKn}}$ pull down resistor = 50 kΩ.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V_{CC}	Supply voltage (Relative to V_{EE})	–0.3 to 4.6	V
V_I	Input voltage	–0.3 to $V_{CC} + 0.5$	V
V_O	Output voltage	–0.3 to $V_{CC} + 0.5$	V
I_{IN}	Input current	±20	mA
V_{EE}	Negative supply voltage (Relative to V_{CC})	–4.6 to 0.3	V
I_{BB}	Sink/source current	–1 to 1	mA
I_O	DC output current	–50	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Maximum operating junction temperature	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

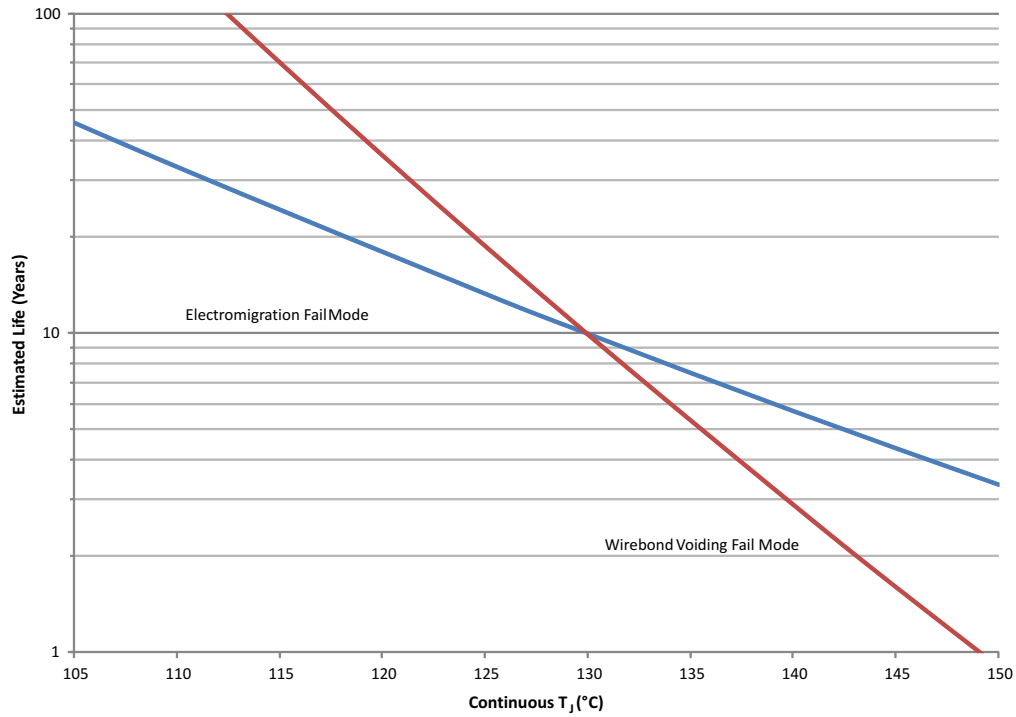
RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (relative to V_{EE})	2.375	2.5/3.3	3.8	V
T_J	Operating junction temperature	–55		125	°C

PACKAGE THERMAL IMPEDANCE, VF (LQFP)

		TEST CONDITION	VALUE	UNIT
θ_{JA}	Thermal resistance junction to ambient ⁽¹⁾	0 LFM	74	°C/W
		150 LFM	66	°C/W
		250 LFM	64	°C/W
		500 LFM	61	°C/W
θ_{JC}	Thermal resistance junction to case		39	°C/W

- (1) According to JESD 51-7 standard.



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. CDCLVP111 in 32/VF Package Operating Life Derating Chart

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LVECL DC ELECTRICAL CHARACTERISTICS

 Vsupply: $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V}$ to -3.8 V over operating temperature range $T_j = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{EE}	Supply internal current	Absolute value of current	-55°C , 25°C , 125°C	35		85	mA
I_{CC}	Output and internal supply current	All outputs terminated $50\ \Omega$ to $V_{CC} - 2\text{ V}$	-55°C , 25°C			385	mA
			125°C			405	
I_{IN}	Input current	Includes pullup/pulldown resistors, $V_{IH} = V_{CC}$, $V_{IL} = V_{CC} - 2\text{ V}$	-55°C , 25°C , 125°C	-150		150	μA
V_{BB}	Internally generated bias voltage	For $V_{EE} = -3$ to -3.8 V , $I_{BB} = -0.2\text{ mA}$	-55°C , 25°C , 125°C	-1.45	-1.3	-1.125	V
		$V_{EE} = -2.375$ to -2.75 V , $I_{BB} = -0.2\text{ mA}$	-55°C , 25°C , 125°C	-1.4	-1.25	-1.1	
V_{IH}	High-level input voltage (CLK_SEL)		-55°C , 25°C , 125°C	-1.165		-0.88	V
V_{IL}	Low-level input voltage (CLK_SEL)		-55°C , 25°C , 125°C	-1.81		-1.475	V
V_{ID}	Input amplitude (CLKn, CLKn)	Difference of input, See ⁽¹⁾ $ V_{IH} - V_{IL} $	-55°C , 25°C , 125°C	0.5		1.3	V
V_{CM}	Common-mode voltage (CLKn, CLKn)	DC offset relative to V_{EE}	-55°C , 25°C , 125°C	$V_{EE} + 1$		-0.3	V
V_{OH}	High-level output voltage	$I_{OH} = -21\text{ mA}$	-55°C	-1.26		-0.85	V
			25°C	-1.2		-0.85	
			125°C	-1.15		-0.8	
V_{OL}	Low-level output voltage	$I_{OL} = -5\text{ mA}$	25°C	-1.85		-1.425	V
			-55°C , 125°C	-1.85		-1.25	
V_{OD}	Differential output voltage swing	Terminated with $50\ \Omega$ to $V_{CC} - 2\text{ V}$, See Figure 4	-55°C , 25°C , 125°C	400			mV

 (1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

LVPECL DC ELECTRICAL CHARACTERISTICS

Vsupply: $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}$, $V_{EE} = 0 \text{ V}$ over operating temperature range $T_j = -55^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EE} Supply internal current	Absolute value of current	-55°C, 25°C, 125°C	35	85	mA
I_{CC} Output and internal supply current	All outputs terminated 50 Ω to $V_{CC} - 2 \text{ V}$	-55°C, 25°C		385	mA
		125°C		405	
I_{IN} Input current	Includes pullup/pulldown resistors $V_{IH} = V_{CC}$, $V_{IL} = V_{CC} - 2 \text{ V}$	-55°C, 25°C, 125°C	-150	150	μA
V_{BB} Internally generated bias voltage	$V_{CC} = 3 \text{ to } 3.8 \text{ V}$, $I_{BB} = -0.2 \text{ mA}$	-55°C, 25°C, 125°C	$V_{CC} - 1.45$	$V_{CC} - 1.3$	V
	$V_{CC} = 2.375 \text{ to } 2.75 \text{ V}$, $I_{BB} = -0.2 \text{ mA}$	-55°C, 25°C, 125°C	$V_{CC} - 1.4$	$V_{CC} - 1.25$	
V_{IH} High-level input voltage (CLK_SEL)		-55°C, 25°C, 125°C	$V_{CC} - 1.165$	$V_{CC} - 0.88$	V
V_{IL} Low-level input voltage (CLK_SEL)		-55°C, 25°C, 125°C	$V_{CC} - 1.81$	$V_{CC} - 1.475$	V
V_{ID} Input amplitude (CLKn, CLKn)	Difference of input, see (1), $ V_{IH} - V_{IL} $	-55°C, 25°C, 125°C	0.5	1.3	V
V_{CM} Common-mode voltage (CLKn, CLKn)	DC offset relative to V_{EE}	-55°C, 25°C, 125°C	1	$V_{CC} - 0.3$	V
V_{OH} High-level output voltage	$I_{OH} = -21 \text{ mA}$	-55°C	$V_{CC} - 1.26$	$V_{CC} - 0.85$	V
		25°C	$V_{CC} - 1.2$	$V_{CC} - 0.85$	
		125°C	$V_{CC} - 1.15$	$V_{CC} - 0.8$	
V_{OL} Low-level output voltage	$I_{OL} = -5 \text{ mA}$	25°C	$V_{CC} - 1.85$	$V_{CC} - 1.425$	V
		-55°C, 125°C	$V_{CC} - 1.85$	$V_{CC} - 1.25$	
V_{OD} Differential output voltage swing	Terminated with 50 Ω to $V_{CC} - 2 \text{ V}$, See Figure 4	-55°C, 25°C, 125°C	400		mV

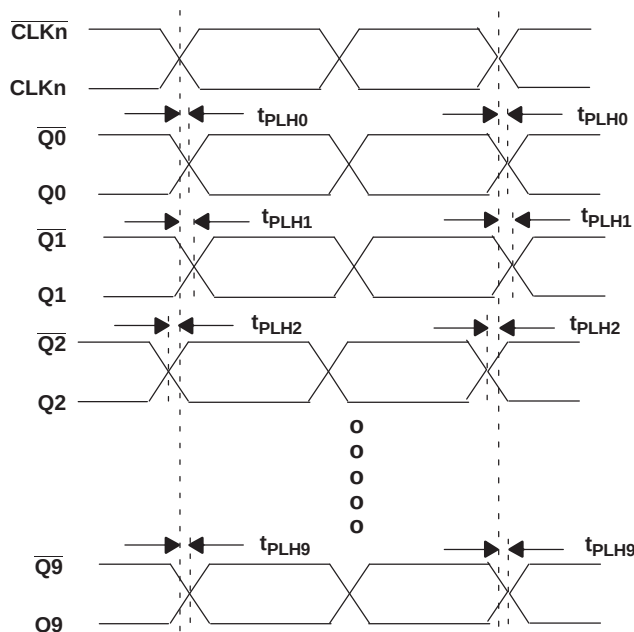
(1) V_{ID} minimum and maximum is required to maintain ac specifications, actual device function tolerates a minimum V_{ID} of 100 mV.

AC ELECTRICAL CHARACTERISTICS

Vsupply: $V_{CC} = 2.375 \text{ V to } 3.8 \text{ V}$, $V_{EE} = 0 \text{ V}$ or LVECL/LVPECL input $V_{CC} = 0 \text{ V}$, $V_{EE} = -2.375 \text{ V to } -3.8 \text{ V}$ over operating temperature range $T_j = -55^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd} Differential propagation delay CLKn, CLKn to all Q0, Q0... Q9, Q9	See Note D in Figure 2	200		355	ps
$t_{sk(o)}$ Output-to-output skew	See Notes A and D in Figure 2		15	50	ps
$t_{sk(pp)}$ Part-to-part skew	See Notes B and D in Figure 2		70		ps
t_{aj} Additive phase jitter ⁽¹⁾	Integration bandwidth of 20 kHz to 20 MHz, $f_{out} = 200 \text{ MHz}$ at 25°C		0.125	0.8	ps
$f_{(max)}$ Maximum frequency ⁽¹⁾	Functional up to 3.5 GHz, see Figure 4			3500	MHz
t_r/t_f Output rise and fall time (20%, 80%)	See Note D in Figure 2			240	ps

(1) Specification is guaranteed by bench characterization and is not tested in production.



- A. Output skew is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, \dots, 9$) or the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, \dots, 9$).
- B. Part-to-part skew, is calculated as the greater of: The difference between the fastest and the slowest t_{PLHn} ($n = 0, 1, \dots, 9$) across multiple devices or the difference between the fastest and the slowest t_{PHLn} ($n = 0, 1, \dots, 9$) across multiple devices.
- C. Typical value measured at ambient when clock input is 155.52 MHz for an integration bandwidth of 20 kHz to 5 MHz.
- D. Input conditions: $V_{CM} = 1$ V, $V_{ID} = 0.5$ V and $F_{IN} = 1$ GHz.

Figure 2. Waveform for Calculating Both Output and Part-to-Part Skew

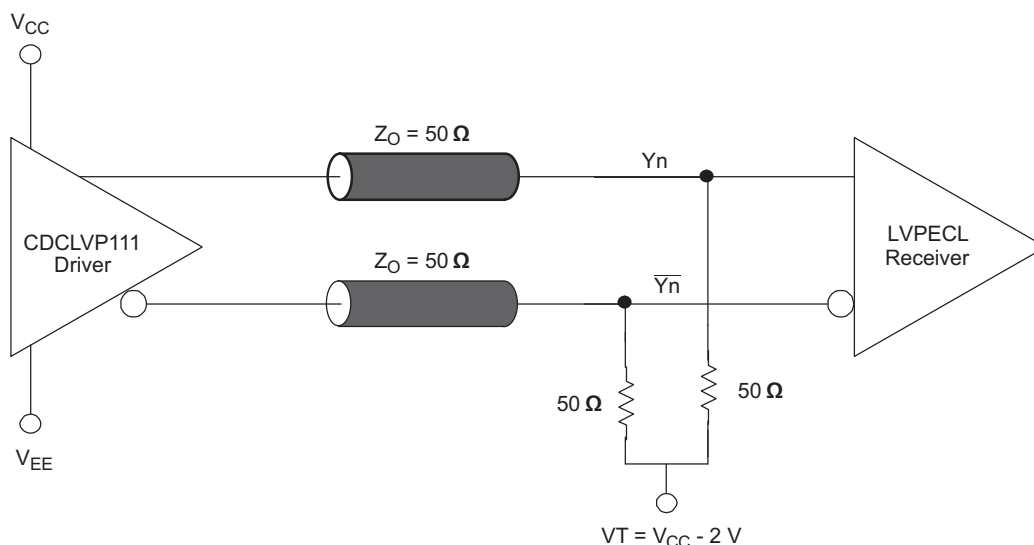


Figure 3. Typical Termination for Output Driver (See the Interfacing Between LVPECL, LVDS, and CML Application Note, Literature Number [SCAA056](#))

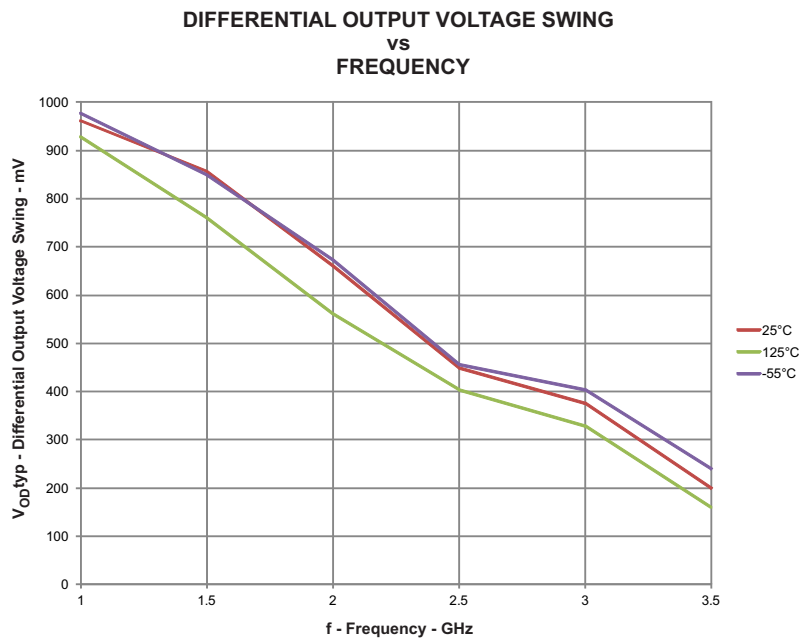


Figure 4. LVPECL Input Using CLK0 Pair, $V_{CC} = 2.375$ V, $V_{CM} = 1$ V, $V_{ID} = 0.5$ V

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVP111MVFREP	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	LVP111MEP	Samples
V62/12624-01XE	ACTIVE	LQFP	VF	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	LVP111MEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CDCLVP111-EP :

- Catalog: [CDCLVP111](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

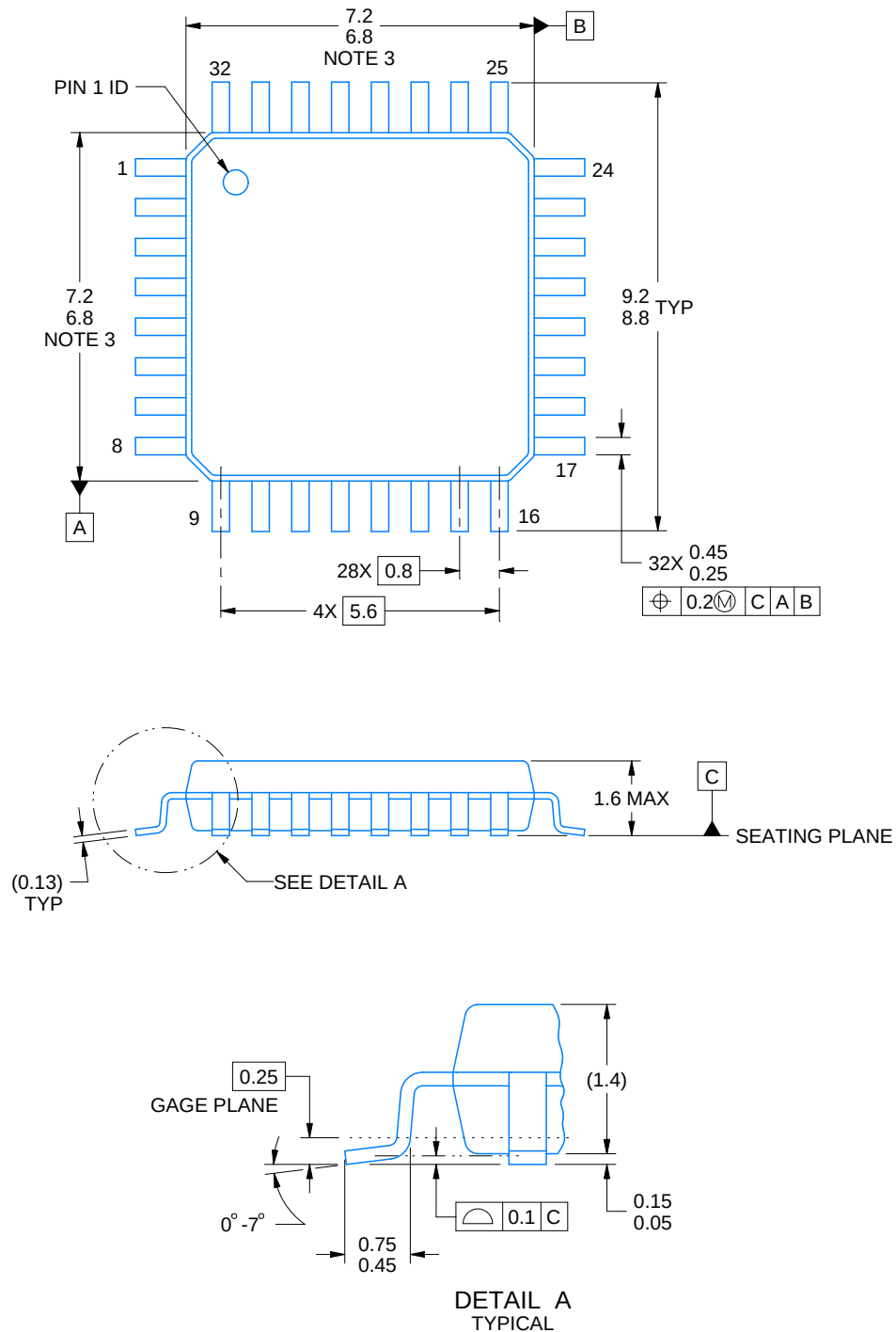
VF0032A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

PowerPAD is a trademark of Texas Instruments.

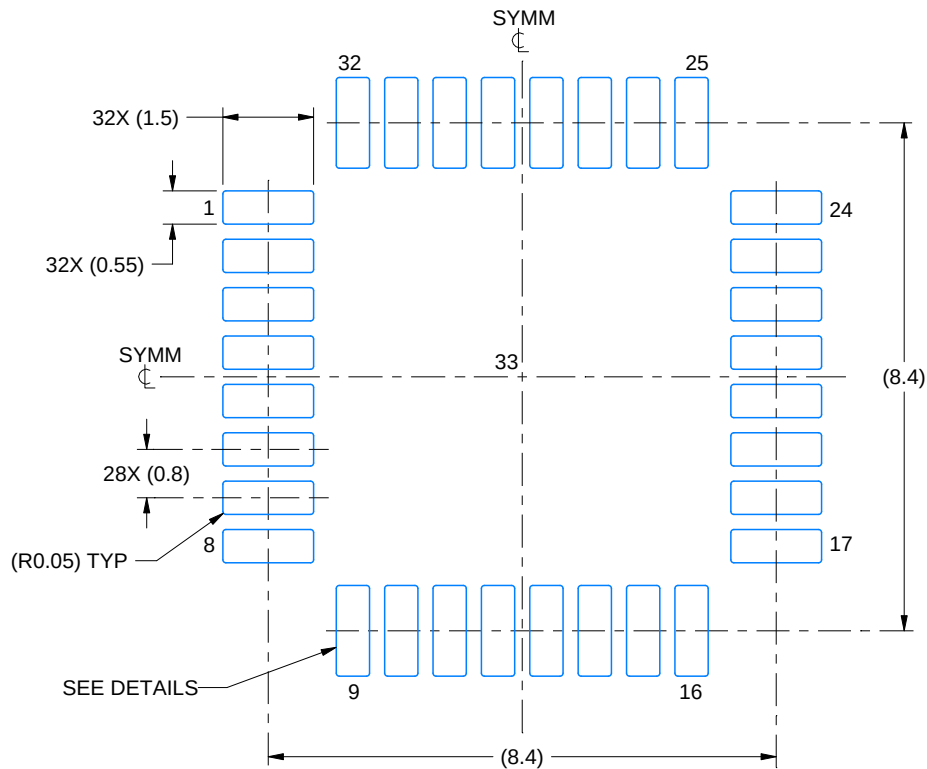
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

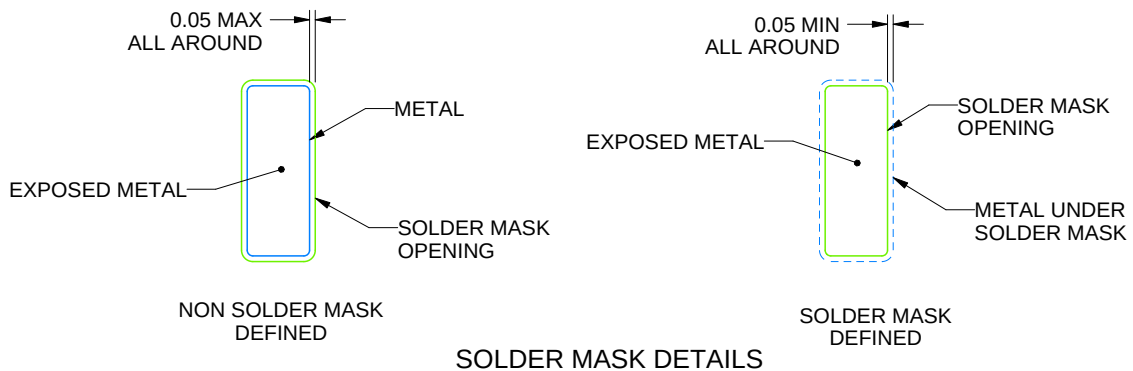
VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



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NOTES: (continued)

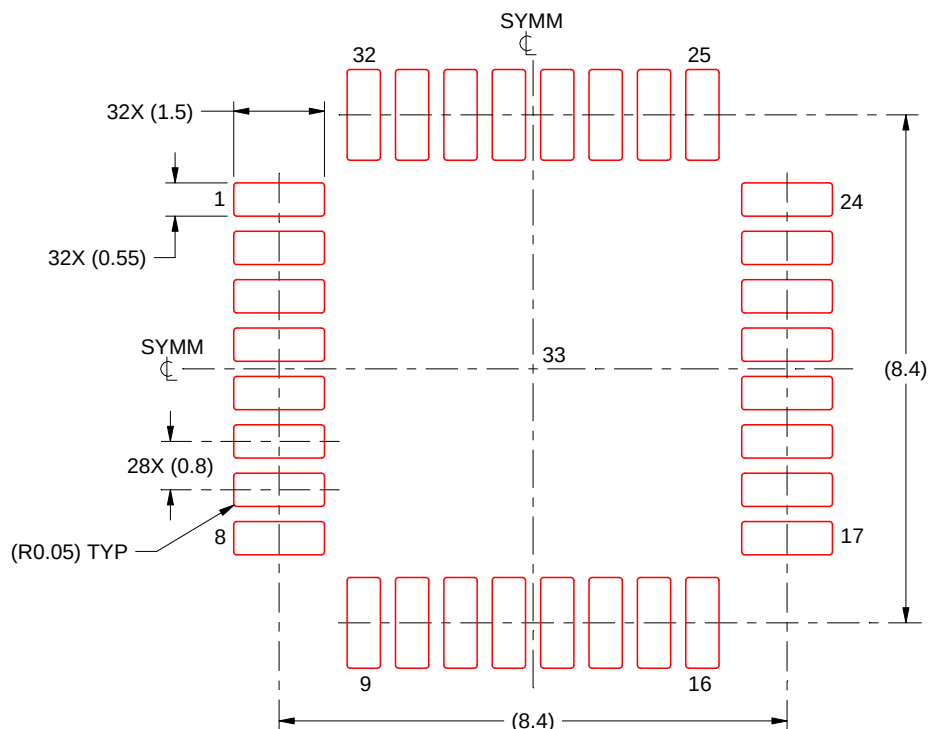
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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