

## 带有可选展频时钟 (SSC) 的时钟缓冲器/时钟倍乘器

 查询样品: [CDCS503-Q1](#)

### 特性

- 符合汽车应用要求
- 具有下列结果的 **AEC-Q100** 测试指南:
  - 器件温度 **2** 级
  - **-40°C 至 105°C** 环境温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 **H2**
  - 器件充电器件模型 (CDM) ESD 分类等级 **C3B**
- 带有可选展频时钟 (SSC) 的易于使用的时钟生成器产品的一部分
- 带有可选输出频率和可选 **SSC** 的时钟倍乘器
- 通过两个外部引脚可控制 **SSC**
  - $\pm 0\%$ ,  $\pm 0.5\%$ ,  $\pm 1\%$ ,  $\pm 2\%$  中心展频
- 可使用一个外部控制引脚来选择 **x1** 或者 **x4** 的频率倍乘
- 通过控制引脚进行输出禁用

- 单一 **3.3V** 器件电源
- 宽温度范围 **-40°C 至 105°C**
- 节省空间的 **8** 引脚薄型小外形尺寸 (TSSOP) 封装

### 应用范围

- 要求通过 **SSC** 和/或者时钟倍乘来减少电磁干扰 (EMI) 的车载应用

IN	1	8	VDD
SSC_SEL 0	2	7	OE
SSC_SEL 1	3	6	OUT
GND	4	5	FS

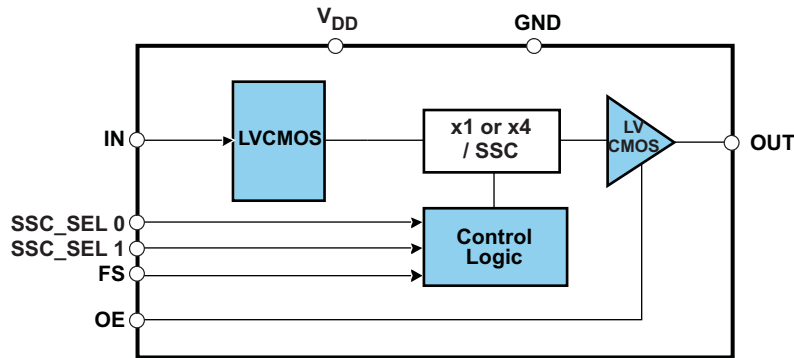


图 1. 方框图



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## 说明

CDCS503-Q1 是一款带有可选频率倍乘的可展频、LVCMOS 输入时钟缓冲器。

它与 CDCS502 共用主要的功能性，但是它使用一个 LVCMOS 输入级而不是 CDCS502 所使用的晶振输入级，并且 CDCS503-Q1 有一个输出使能引脚。

此器件在输入上接受一个 3.3V LVCMOS 信号。

这个输入信号由一个锁相环路 (PLL) 处理，此环路的输出频率或者与输入频率相等或者被乘以因子 4。

PLL 还可通过三角调制将时钟信号以输出时钟频率为中心扩展  $\pm 0\%$ ， $\pm 0.5\%$ ， $\pm 1\%$  或者  $\pm 2\%$ 。

这样，此器件可生成介于 8MHz 和 108MHz 之间带有或者不带有 SSC 的输出频率。

一个独立的控制引脚可被用于启用或者禁用输出。CDCS503-Q1 运行在一个 3.3V 环境中。

器件额定运行温度介于  $-40^{\circ}\text{C}$  至  $105^{\circ}\text{C}$  之间，并采用 8 引脚 TSSOP 封装。

表 1. 功能表

OE	FS	SSC_SEL 0	SSC_SEL 1	SSC 数量	$f_{\text{OUT}}/f_{\text{IN}}$	$f_{\text{in}}=27\text{MHz}$ 时的 $f_{\text{OUT}}$
0	x	x	x	x	x	三态
1	0	0	0	$\pm 0.00\%$	1	27MHz
1	0	0	1	$\pm 0.50\%$	1	27MHz
1	0	1	0	$\pm 1.00\%$	1	27MHz
1	0	1	1	$\pm 2.00\%$	1	27MHz
1	1	0	0	$\pm 0.00\%$	4	108MHz
1	1	0	1	$\pm 0.50\%$	4	108MHz
1	1	1	0	$\pm 1.00\%$	4	108MHz
1	1	1	1	$\pm 2.00\%$	4	108MHz



这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## DEVICE INFORMATION

### PACKAGE

IN	1	<b>CDCS503-Q1</b>	8	VDD
SSC_SEL 0	2		7	OE
SSC_SEL 1	3		6	OUT
GND	4		5	FS

### PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
IN	1	I	LVC MOS clock input
OUT	6	O	LVC MOS clock output
SSC_SEL 0, 1	2, 3	I	Spread selection pins, internal pullup
OE	7	I	Output enable, internal pullup
FS	5	I	Frequency multiplication selection, internal pullup
VDD	8	Power	3.3-V power supply
GND	4	Ground	Ground

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	TSSOP 2000	CDCS503TPWRQ1	CS503Q

### PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PW 8-PIN TSSOP		THERMAL AIRFLOW (CFM)				UNIT
		0	150	250	500	
R <sub>θJA</sub>	High K	149	142	138	132	°C/W
	Low K	230	185	170	150	
R <sub>θJC</sub>	High K	65				°C/W
	Low K	69				

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		CDCS503TPWRQ1	UNIT
		PW (8 PINS)	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	179.9	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	64.9	
θ <sub>JB</sub>	Junction-to-board thermal resistance	108.7	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	107	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	n/a	

(1) 有关传统和全新热度的更多信息，请参阅 IC 封装热量应用报告（文献号：SPRA953）。

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
$V_{DD}$	Supply voltage range	–0.5 to 4.6	V
$V_{IN}$	Input voltage range	–0.5 to 4.6	V
$V_{out}$	Output voltage range	–0.5 to 4.6	V
$I_{IN}$	Input current ( $V_I < 0$ , $V_I > V_{DD}$ )	20	mA
$I_{out}$	Continuous output current	50	mA
$T_{ST}$	Storage temperature range	–65 to 150	°C
$T_J$	Maximum junction temperature	125	°C
ESD Rating	Human-body model (HBM) AEC-Q100 classification level H2	1.5	kV
	Charged-device model (CDM) AEC-Q100 classification level C3B	750	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

			MIN	NOM	MAX	UNIT
$V_{DD}$	Supply voltage		3		3.6	V
$f_{IN}$	Input frequency	FS = 0	8		32	MHz
		FS = 1	8		27	
$V_{IL}$	Low-level input voltage LVCMOS				$0.3 V_{DD}$	V
$V_{IH}$	High-level input voltage LVCMOS		$0.7 V_{DD}$			V
$V_I$	Input voltage threshold LVCMOS			$0.5 V_{DD}$		V
$C_L$	Output load test LVCMOS				15	pF
$I_{OH}/I_{OL}$	Output current				$\pm 12$	mA
$T_A$	Operating free-air temperature		-40		105	°C

**DEVICE CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{DD}$	Device supply current	$f_{out} = 20$ MHz; FS = 0, no SSC		19	mA	
		$f_{out} = 70$ MHz; FS = 1, SSC = 2%		22		
$f_{OUT}$	Output frequency	FS = 0		8	32	MHz
		FS = 1		32	108	
$I_{IH}$	LVCMOS input current	$V_I = V_{DD}$ ; $V_{DD} = 3.6$ V			10	$\mu$ A
$I_{IL}$	LVCMOS input current	$V_I = 0$ V; $V_{DD} = 3.6$ V			-10	$\mu$ A
$V_{OH}$	LVCMOS high-level output voltage	$I_{OH} = -0.1$ mA		2.9	V	
		$I_{OH} = -8$ mA		2.4		
		$I_{OH} = -12$ mA		2.2		
$V_{OL}$	LVCMOS low-level output voltage	$I_{OL} = 0.1$ mA			0.1	V
		$I_{OL} = 8$ mA			0.5	
		$I_{OL} = 12$ mA			0.8	
$I_{OZ}$	High-impedance-state output current	OE = Low		-2	2	$\mu$ A
$t_{JIT(C-C)}$	Cycle to cycle jitter <sup>(1)</sup>	$f_{out} = 108$ MHz; FS = 1, SSC = 1%, 10000 Cycles			110	ps
$t_r/t_f$	Rise and fall time <sup>(1)</sup>	20%–80%			0.75	ns
$O_{dc}$	Output duty cycle <sup>(2)</sup>		45%		55%	
$f_{MOD}$	Modulation frequency		30			kHz

 (1) Measured with Test Load, see [Figure 3](#).

(2) Not production tested.

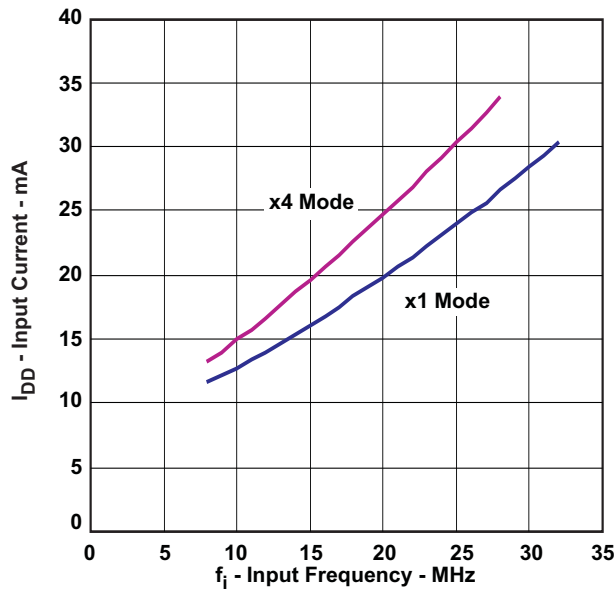


Figure 2. I<sub>DD</sub> vs Input Frequency, V<sub>CC</sub> = 3.3 V, SSC = 2%, Output Loaded With Test Load

### APPLICATION INFORMATION

#### SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS503-Q1 device uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

$$FS = 0: f_{mod} = f_{IN} / 708$$

$$FS = 1: f_{mod} = f_{IN} / 620$$

### PARAMETER MEASUREMENT INFORMATION

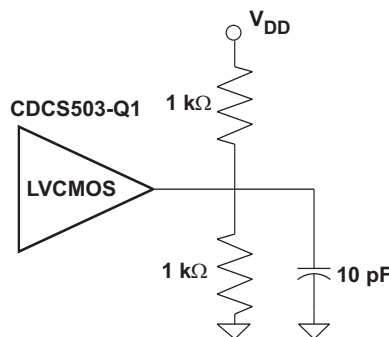
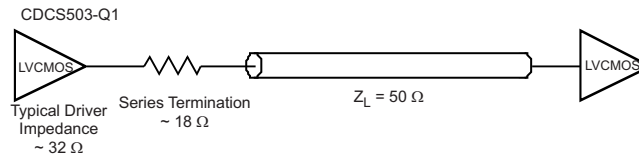


Figure 3. Test Load

**PARAMETER MEASUREMENT INFORMATION (continued)**



**Figure 4. Load for 50-Ω Board Environment**

## REVISION HISTORY

Changes from Revision A (June 2012) to Revision B	Page
• 在 FAD 中将符合 AEC Q100 标准改为了 AEC Q100 测试指南 .....	1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCS503TPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	CS503Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF CDCS503-Q1 :**

- Catalog: [CDCS503](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS503TPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS503TPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0

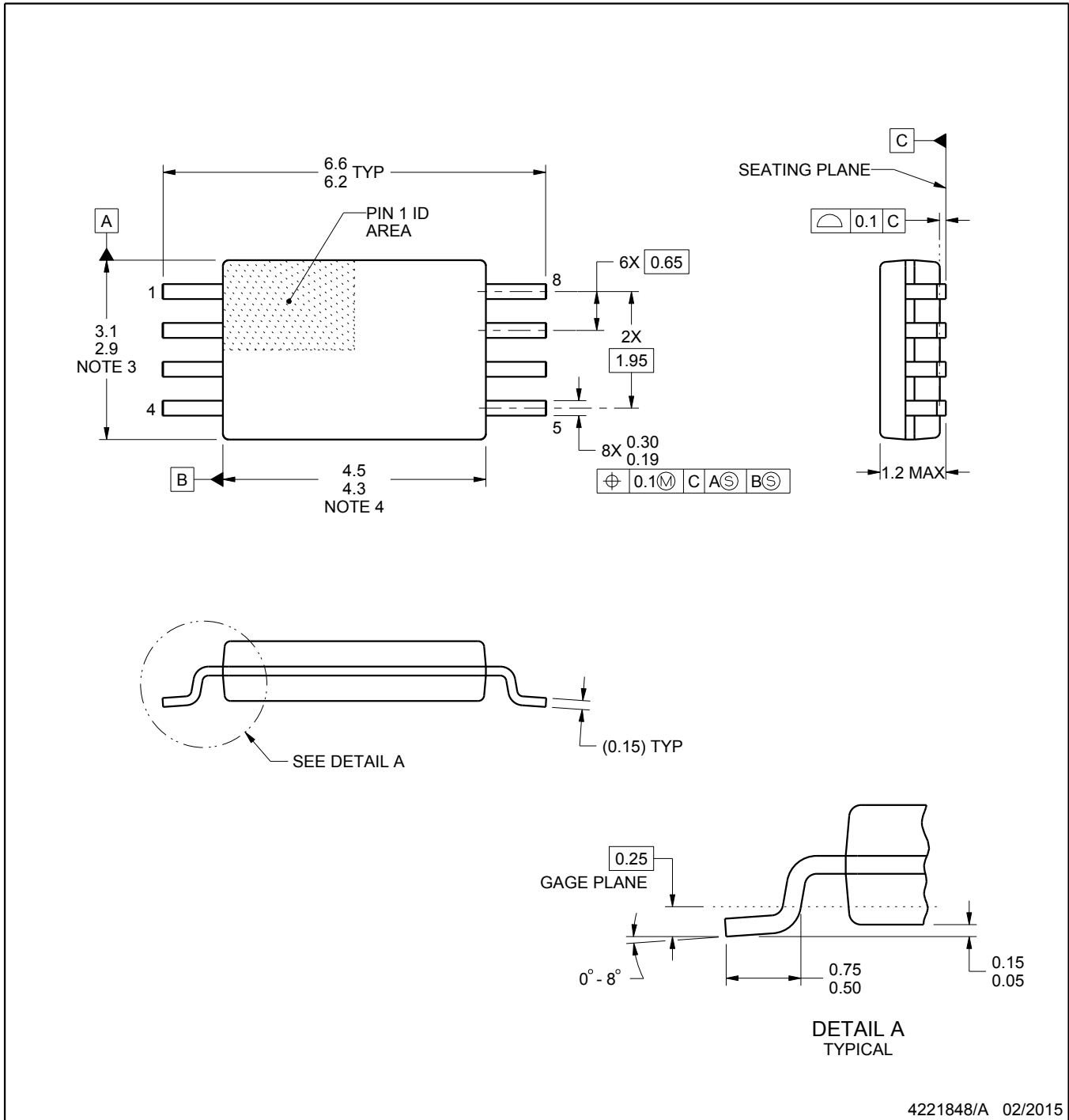
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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### NOTES:

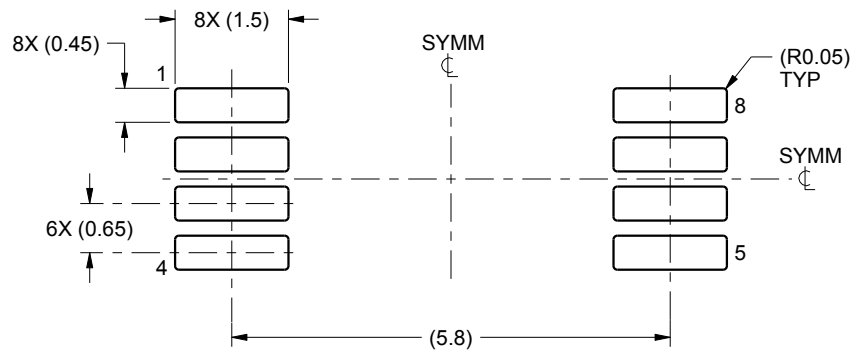
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

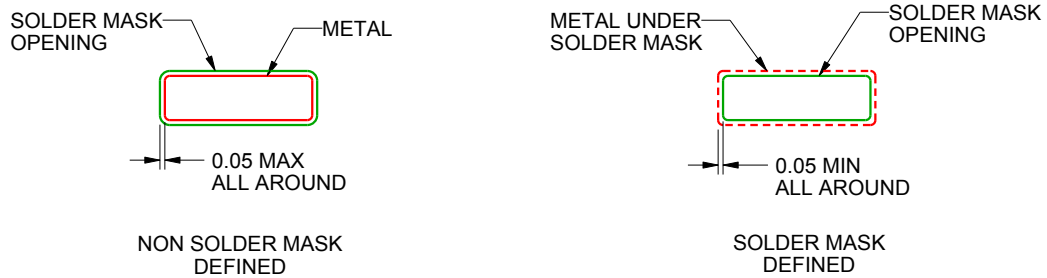
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

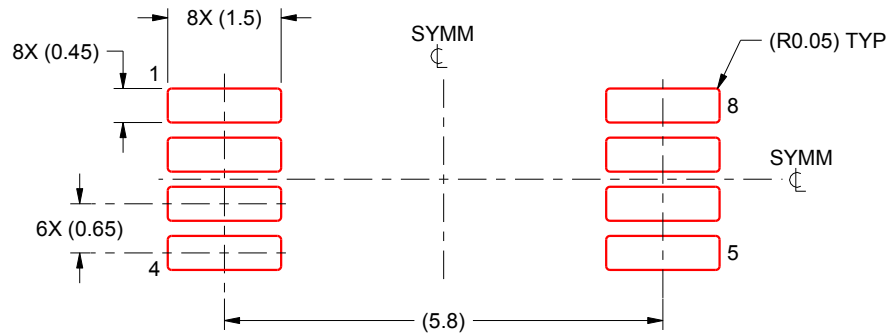
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com.cn/omap">www.ti.com.cn/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>