CDCE6214-Q1 Ultra-Low Power Clock Generator With One PLL, Four Differential Outputs, Two Inputs, and Internal EEPROM

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 2: –40°C to +105°C
- Configurable high performance, low-power, frac-N PLL with RMS jitter with spurs (12 kHz – 20 MHz, F_{out} > 100 MHz) as:
  - Integer mode:
    - Differential output: 350fs typical, 600fs maximum
    - LVCMOS output: 1.05ps typical, 1.5ps maximum
  - Fractional mode:
    - Differential output: 1.7ps typical, 2.1ps maximum
    - LVCMOS output: 2.0ps typical, 4.0ps maximum
  - Supports PCIe Gen1/2/3 with SSC and Gen 1/2/3/4 without SSC
  - 2.35-GHz to 2.6-GHz internal VCO
- Typical power consumption: 120 mW at 1.8 V
- Universal clock input, two reference inputs for redundancy
  - Differential AC-coupled or LVCMOS: 10 MHz to 200 MHz
  - Crystal: 10 MHz to 50 MHz
- Flexible output clock distribution
  - 4 channel dividers: Up to 5 unique output frequencies from 24 kHz to 350 MHz
  - Combination of LVDS-like, LP-HCSL or LVCMOS outputs on OUT0 – 4 pins
  - Glitch-less output divider switching and output channel synchronization
  - Individual output enable through GPIO and register
- Frequency margining options
  - DCO mode: frequency increment/decrement with 10ppb or less step-size
- Fully integrated, configurable loop bandwidth: 100 kHz to 1.6 MHz
- Single or mixed supply for level translation: 1.8/2.5/3.3 V
- Configurable GPIOs and flexible configuration options
  - I^2C-compatible interface: up to 400 kHz
  - Integrated EEPROM with two pages and external select pin
- Supports 100-Ω systems
- Small footprint: 24-pin WQFN (4 mm × 4 mm)

2 Applications

- Data Center & Enterprise Computing, PC & Notebook
- Advanced driver assistance systems (ADAS) - Sensor Fusion
- Infotainment & Cluster - Automotive Head Unit - eAVB
- Enterprise Machine - Multi-Function Printer

3 Description

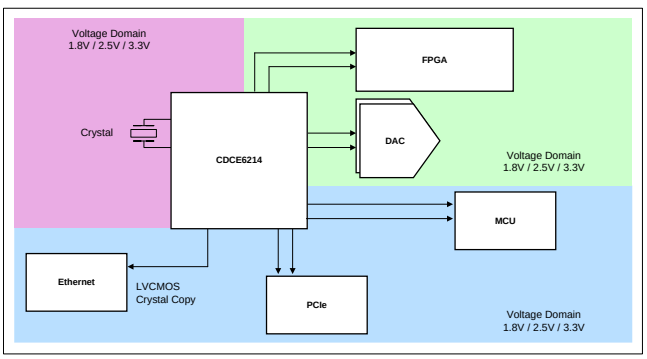
The CDCE6214-Q1 is a four-channel, ultra-low power, medium grade jitter, clock generator for automotive applications that can generate five independent clock outputs selectable between various modes of drivers. The input source could be a single-ended or differential input clock source, or a low-frequency crystal. The CDCE6214-Q1 features a frac-N PLL to synthesize unrelated base frequency from any input frequency. The CDCE6214-Q1 can be configured through the I2C interface. In the absence of the serial interface, the GPIO pins can be used in Pin Mode to configure the product into distinctive configurations. On-chip EEPROM (Non-volatile Memory) can be used to change the configuration, which is pre-selectable through the pins.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCE6214-Q1	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Example CDCE6214-Q1



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2019	*	Initial release.

5 Description (cont.)

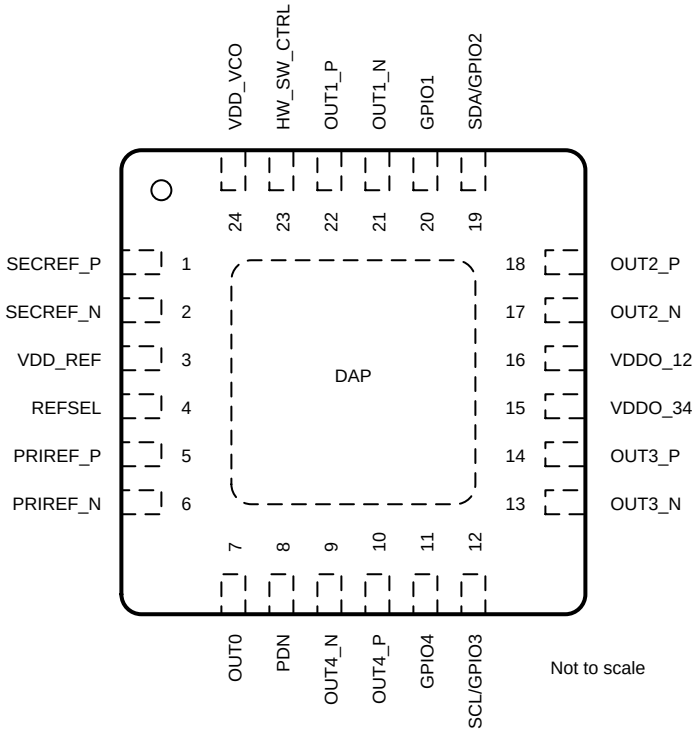
The device provides frequency margining options with glitch-free operation to support system design verification tests (DVT) and Ethernet Audio-Video Bridging (eAVB). Fine frequency margining is available on any output channel by steering the fractional feedback divider in DCO mode.

Internal power conditioning provides excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The analog and digital core blocks operate from either a 1.8-V, 2.5-V, or 3.3-V ±5% supply, and output blocks operate from a 1.8-V, 2.5-V, or 3.3-V ±5% supply.

The CDCE6214-Q1 enables high-performance clock trees from a single reference at ultra-low power with a small footprint. The factory- and user-programmable EEPROM features make the CDCE6214-Q1 an easy-to-use, instant-on clocking device with a low power consumption.

6 Pin Configuration and Functions

CDCE6214-Q1 RTW Package
24-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
DAP	—	G	Die Attach Pad. The DAP is an electrical connection and provides a thermal dissipation path. For proper electrical and thermal performance of the device, the DAP must be connected to PCB ground plane.
VDD_REF	3	P	1.8/2.5/3.3-V Power Supply for Reference Input and Digital.
VDD_VCO	24	P	1.8/2.5/3.3-V Power Supply for PLL/VCO.
VDDO_12	16	P	1.8/2.5/3.3-V Power Supply for OUT1 and OUT2 channels
VDDO_34	15	P	1.8/2.5/3.3-V Power Supply for OUT0, OUT3, and OUT4 channels
INPUT BLOCK			
HW_SW_CTRL	23	I, R_{PUPD}	Manual selection pin for EEPROM pages (3-state). Weak Pullup/Pulldown. R_{PU} = 75 kΩ. R_{PD} = 75 kΩ.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PRIREF_P	5	I	Primary reference clock. Accepts a differential or single-ended input. Input pins have AC-coupling capacitors and biasing internally in differential mode. For LVCMOS, input should be provided on PRIREF_P and the non-driven input pin should be pulled down to ground.
PRIREF_N	6	I	
REFSEL	4	I, R_{PUPD}	Manual selection pin of reference input (3-state). Weak Pullup/Pulldown. R_{PU} = 75 kΩ. R_{PD} = 75 kΩ.
SECREF_P	1	I	Secondary reference clock. Accepts a differential or single-ended input or XTAL. Input pins have AC-coupling capacitors and biasing internally in differential mode. For XTAL input, drive SECREF_P and SECREF_N with the XTAL. SECREF_P is XOUT, SECREF_N is XIN. For LVCMOS input, input should be provided on SECREF_P, and the non-driven input pin should be pulled down to ground.
SECREF_N	2	I	
OUTPUT BLOCK			
OUT0	7	O	LVCMOS Output 0. Reference Input can be bypassed into this output.
OUT1_P	22	O	LVDS-like/LP-HCSL/LVCMOS Output Pair 1. Programmable driver with LVDS-like/LP-HCSL or 2x LVCMOS outputs.
OUT1_N	21	O	
OUT2_P	18	O	LVDS-like/LP-HCSL Output Pair 2. Programmable driver with LVDS-like/LP-HCSL outputs.
OUT2_N	17	O	
OUT3_P	14	O	LVDS-like/LP-HCSL Output Pair 3. Programmable driver with LVDS-like/LP-HCSL outputs.
OUT3_N	13	O	
OUT4_P	10	O	LVDS-like/LP-HCSL/LVCMOS Output Pair 4. Programmable driver with LVDS-like/LP-HCSL or 2x LVCMOS outputs.
OUT4_N	9	O	
DIGITAL CONTROL / INTERFACES			
GPIO1	20	I/O, R_{PU}	STATUS output or GPIO1 input. Weak pullup resistor when configured as Input. R_{PU} = 75 kΩ.
GPIO4	11	I/O, R_{PU}	STATUS output or GPIO4 input. Weak pullup resistor when configured as Input. R_{PU} = 75k Ω.
PDN	8	I, R_{PU}	Device Power-down/RESET (active low) or SYNCN. Weak pullup resistor. R_{PU} = 75 kΩ.
SDA/GPIO2	19	I/O	I2C Serial Data (bidirectional, open-drain) or GPIO2 input. Requires an external pullup resistor to VDD_REF in I2C mode. I2C slave address is initialized from on-chip EEPROM. Fail-safe Input.
SCL/GPIO3	12	I	I2C Serial Clock or GPIO3 input. Requires an external pullup resistor to VDD_REF in I2C mode. Fail-safe Input.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD_REF, VDD_VCO, VDDO_12, VDDO_34	Supply Voltage	-0.3	3.63	V
PRIREF_P, PRIREF_N, SECREF_P, SECREF_N	Input Voltage	-0.3	VDD_REF + 0.3	V
GPIO1, SDA/GPIO2, SCL/GPIO3, GPIO4, REFSEL, HW_SW_CTRL, PDN	Input Voltage	-0.3	VDD_REF + 0.3	V
OUT0, OUT1_P, OUT1_N, OUT2_P, OUT2_N, OUT3_P, OUT3_N, OUT4_P, OUT4_N(2)	Output Voltage	-0.3	VDDO_X + 0.3	V
GPIO1, SDA/GPIO2	Output Voltage	-0.3	VDD_REF + 0.3	V
T_J	Junction Temperature		125	ºC
T_{stg}	Storage temperature	-65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VDDO_X refers to the output supply for a specific output channel, where X denotes the channel index.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD_VCO	Core supply voltage	1.71	1.8, 2.5, 3.3	3.465	V
VDDO_12, VDDO_34	Output supply voltage	1.71	1.8, 2.5, 3.3	3.465	V
VDD_REF	Reference supply voltage	1.71	1.8, 2.5, 3.3	3.465	V
T_A	Ambient temperature	-40		105	ºC
T_J	Junction temperature	-40		125	ºC
T_{LOCK}	Continuous lock over temperature (without VCO calibration)			145	ºC
t_{RAMP}	Maximum supply voltage ramp time (1)	0.1		30	ms

(1) VDD pin should monotonically reach 95% of its final value within supply ramp time. Parameter specified by characterization. All VDD pins were tied together for this evaluation. For non-monotonic or slower power supply ramp, it is recommended to pull-down PDN pin until VDD pins have reached 95% of its final value. PDN pin has a 50 kΩ pull-up resistor. When PDN pin cannot be actively controlled, it is recommended to add a capacitor to GND on PDN pin to delay the release of reset.

7.4 Thermal Information

THERMAL METRIC (1)		CDCE6214 RTW QFN-24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 EEPROM Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
n_{EEcyc}	EEPROM programming cycles	each word	10			cycles
t_{EEret}	EEPROM data retention		10			years

7.6 Reference Input, Single Ended Characteristics (PRIREF, SECREF)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN_Ref}	Reference frequency		10		200	MHz
V_{IH}	Input high voltage	LVCMOS Input Buffer	0.8 × VDD_REF			V
V_{IL}	Input low voltage	LVCMOS Input Buffer			0.2 × VDD_REF	V
dV_{IN}/dT	Input slew rate	20% - 80%	1			V/ns
IDC	Input duty cycle		40		60	%
$I_{IN\_LEAKAGE}$	Input leakage current		-100		100	uA
C_{IN_REF}	Input capacitance	at 25°C			5	pF

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7.7 Reference Input, Differential Characteristics (PRIREF, SECREF)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN_Ref}	Reference frequency		10		200	MHz
V_{IN_DIFF}	Differential input voltage swing, peak-to-peak	VDD_REF = 2.5/3.3 V	0.4		1.6	V
V_{IN_DIFF}	Differential input voltage swing, peak-to-peak	VDD_REF = 1.8V	0.4		1.0	V
dV_{IN}/dT	Input slew rate	20% - 80%	1			V/ns
IDC	Input duty cycle		40		60	%
$I_{IN\_LEAKAGE}$	Input leakage current		-100		100	uA
C_{IN_REF}	Input capacitance	at 25°C		5		pF

7.8 Reference Input, Crystal Mode Characteristics (SECREF)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN_Xtal}	Crystal frequency	Fundamental mode	10		50	MHz
Z_{ESR}	Crystal equivalent series resistance	f_{XTAL} = 10MHz to 16MHz			60	Ω
Z_{ESR}	Crystal equivalent series resistance	f_{XTAL} = 16MHz to 30MHz(2)			50	Ω
Z_{ESR}	Crystal equivalent series resistance	f_{XTAL} = 30MHz to 50MHz(3)			30	Ω
C_L	Crystal load capacitance	Using on-chip load capacitance. A supported Crystal is within	5		12.8	pF
P_{XTAL}	Crystal tolerated drive power	A supported crystal tolerates up to			200	uW
C_{XIN_LOAD}	On-Chip load capacitance	Programmable in typ. 200fF steps	3		9.1	pF

(1) Parameter specified by characterization. Not tested at production.
(2) Tested using NX3225SA (25MHz XTAL), C_L=8pF, C_0=1.42pF. Measured max. series resistor=600 Ω at 1.8V/2.5V/3.3V supply (12 x Z_{ESR}).
(3) Tested using NX3225SA (50MHz XTAL), C_L=8pF, C_0=1.42pF. Measured max. series resistor=60 Ω at 1.8V supply (2 x Z_{ESR}) and 120 Ω at 2.5V/3.3V supply (4 x Z_{ESR})

7.9 General Purpose Input Characteristics (GPIO[4:1], REFSEL, PDN)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		0.8 × VDD_REF			V
V_{IL}	Input low voltage				0.2 × VDD_REF	V
I_{IH}	Input high level current	VIH = VDD_REF, GPIO[1:4], PDN	-5		5	µA
I_{IL}	Input low level current	VIL = GND, GPIO[2:3]	-5		5	µA
I_{IL}	Input low level current	VIL = GND, GPIO[1], GPIO[4], PDN	-100		100	µA
dV_{IN}/dT	Input slew rate	20% - 80%	0.5			V/ns
T_{PULSE_WIDTH}	Pulse width for correct operation		10			ns
R_{PU}	Pull-up Resistance	Pins PDN, GPIO[1], GPIO[4]		77		kΩ
C_{IN}	Pin Capacitance				10	pF

7.10 Triple Level Input Characteristics (HW_SW_CTRL)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		0.8 × VDD_REF			V
V_{IM}	Input mid voltage	Float pin	0.41 × VDD_REF	0.5 × VDD_REF	0.58 × VDD_REF	V
V_{IL}	Input low voltage				0.2 × VDD_REF	V
I_{IH}	Input high level current	VIH = VDD_REF		40		µA

Triple Level Input Characteristics (HW_SW_CTRL) (continued)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input low level current	VIL = GND		-40		µA

7.11 Logic Output Characteristics (GPIO1, GPIO2)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH	Output high voltage		0.8*VDD_REF			V
VOL	Output low voltage				0.2*VDD_REF	V

7.12 Phase Locked Loop Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PFD}	Phase Detector Frequency	Integer and Fractional PLL mode	1		100	MHz
f_{VCO}	Voltage Controlled Oscillator Frequency		2350		2600	MHz
f_{BW}	Configurable closed-loop PLL Bandwidth	REF = 25 MHz	100		1600	kHz
K_{VCO}	Voltage Controlled Oscillator Gain	f_{VCO} = 2.4 GHz		155		MHz/V
K_{VCO}	Voltage Controlled Oscillator Gain	f_{VCO} = 2.5 GHz		200		MHz/V
$\lvert\Delta T_{CL}\rvert$	Allowable Temperature Drift for Continuous Lock(1)	dT/dt ≤ tbd K			145	°C
$f_{MAX\text{-}ERROR}$	Maximum frequency error with frac-N PLL				0.1	ppm

(1) The maximum allowable temperature drift for continuous lock is: how far the temperature can drift in either direction from the value it was at the time, when the On-Chip VCO was calibrated while the PLL stays in lock throughout the temperature drift. The internal VCO calibration takes place: at device start-up, when the device is reset using the RESET pin and when REGISTER bit is changed. This implies the device will work over the entire frequency range, but if the temperature drifts more than the 'maximum allowable temperature drift for continuous lock', then it is necessary to re-calibrate the VCO, using the appropriate REGISTER bit, to ensure the PLL stays in lock. Regardless of what temperature the part was initially calibrated at, the temperature can never drift outside the ambient temperature range of -40 °C to 105 °C.

7.13 Closed Loop Output Jitter Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RJ_CL}	RMS Phase Jitter(1)	RMS jitter with spurs from 12 kHz to 20 MHz , Input Crystal = 25 MHz, Differential OUTx > 100MHz, int-PLL		350	600	fs
t_{RJ_CL}	RMS Phase Jitter(2)	RMS jitter with spurs from 12 kHz to 20 MHz, Input Crystal = 25 MHz, Differential OUTx > 100 MHz, frac-PLL		1600	2100	fs
$t_{RJ\_CL,\ PCIE}$	RMS Phase Jitter(1)	PCIe Gen 3 Filter applied, XIN = Crystal 25 MHz, OUTx = 100 MHz, frac-N PLL with and without SSC, LP-HCSL or LVDS output		475	1000	fs

(1) Parameters specified by characterization. Not tested at production.
(2) Parameters defined by characterization. Not tested at production. F_{IN} = 25MHz, F_{OUT}= 161.1328MHz, F_{PFD} = 25MHz, RMS Noise = 1.83ps. F_{IN} = 25MHz, F_{OUT}= 161.1328MHz, F_{PFD} = 50MHz, RMS Noise = 1.33ps. F_{IN} = 25MHz, F_{OUT}= 148.5MHz, F_{PFD} = 25MHz, RMS Noise = 1.74ps. F_{IN} = 25MHz, F_{OUT}= 148.5MHz, F_{PFD} = 50MHz, RMS Noise = 1.43ps. F_{IN} = 25MHz, F_{OUT}= 148.3516MHz, F_{PFD} = 25MHz, RMS Noise = 1.6ps. F_{IN} = 25MHz, F_{OUT}= 148.3516MHz, F_{PFD} = 50MHz, RMS Noise = 1.5ps. F_{IN} = 25MHz, F_{OUT}= 106.5MHz, F_{PFD} = 25MHz, RMS Noise = 0.8ps. F_{IN} = 25MHz, F_{OUT}= 106.5MHz, F_{PFD} = 50MHz, RMS Noise = 1.3ps.

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7.14 Input and Output Isolation

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{ISOLATION}$	Reference input isolation(1)	Crosstalk between reference inputs, PRIREF = 27MHz LVCMOS, SECREF = 25MHz XTAL		tbd		dB
$P_{ISOLATION}$	Reference input isolation(1)	Crosstalk between reference inputs, PRIREF = 100MHz HCSL, SECREF = 25MHz LVDS		tbd		dB
$P_{ISOLATION}$	Clock output isolation(1)	Crosstalk between clock outputs, OUT1 = 100MHz LP-HCSL, OUT2 = 156.25MHz LVDS, PFD = 25MHz, int-PLL		tbd		dB
$P_{ISOLATION}$	Clock output isolation(1)	Crosstalk between clock outputs, OUT1 = 156.25MHz LVDS, OUT0 = 25MHz LVCMOS		tbd		dB

(1) Parameters specified by characterization. Not tested at production.

7.15 Buffer Mode Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RJ_ADD}	Additive RMS Phase Jitter, System Level	int. Range from 10 kHz to 20 MHz , REF = HCSL 100 MHz with 0.5V/ns, OUTx = 100 MHz LP-HCSL			TBD	fs
$t_{PROP, LVCMOS}$	Input-to-output propagation delay	REF = LVCMOS 25 MHz, OUTx = 25 MHz LVCMOS		1		ns
$t_{PROP, Differential}$	Input-to-output propagation delay(2)	REF = HCSL 100 MHz, OUTx = 100 MHz LP-HCSL or LVDS		tbd		ps
$t_{PROP-VARIATION}$	Input-to-output delay variation in ZDB mode(1)	ZDB mode, differential input = differential output = 100 MHz, PLL BW = 300kHz to 900kHz across temperature	-200		200	ps

(1) Parameters specified by characterization. Not tested at production
(2) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched. OUT2/OUT3 is matched. There is an additional skew 150ps- 250ps between OUT1/OUT4 and OUT2/OUT3. Parameters specified by characterization. Not tested at production.

7.16 PCIe Spread Spectrum Generator

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SSC-RATE}$	SSC modulation rate	OUTx = 100 MHz	30	31.5	33	kHz
$P_{AMPL-RED}$	SSC amplitude reduction	OUTx = 100 MHz		tbd		dB
$f_{SSC-STEP}$	Down and Center spread SSC step size	OUTx = 100 MHz		0.25		%
$t_{SSC\_FREQ\_DEVIATION}$	Down spread min/max deviation	OUTx = 100 MHz. F_{PFD} = 25M, 50M, 100M	-0.5		0	%
$t_{SSC\_FREQ\_DEVIATION}$	Center spread min/max deviation	OUTx = 100 MHz. F_{PFD} = 25M, 50M, 100M	-0.5		0.5	%

7.17 LVCMOS Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{O_LVCMOS}	Output frequency	2pF to GND, normal mode	0.024		200	MHz
V_{OH_LVCMOS}	Output high voltage	I_{OH} = 1 mA, VDDO_x is corresponding supply voltage.	0.8*VDDO_x			V
V_{OL_LVCMOS}	Output low voltage	I_{OL} = 1 mA, VDDO_x is corresponding supply voltage.			0.2*VDDO_x	V
I_{OH}	Output high current	Vout = 0.8 × VDDO_x, VDDO_x = 1.8V		-7.2		mA
I_{OH}	Output high current	Vout = 0.8 × VDDO_x, VDDO_x = 2.5V		-10		mA
I_{OH}	Output high current	Vout = 0.8 × VDDO_x, VDDO_x = 3.3V		-13.2		mA
I_{OL}	Output low current	Vout = 0.2 × VDDO_x, VDDO_x = 1.8V		7.2		mA
I_{OL}	Output low current	Vout = 0.2 × VDDO_x, VDDO_x = 2.5V		10		mA

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LVCMOS Output Characteristics (continued)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Output low current	Vout = 0.2 × VDDO_x, VDDO_x = 3.3V		13.2		mA
$T_{RISE-FALL}$	Output rise & fall time(1)	20/80%, C_L= 5pF, normal mode	300	500	700	ps
$T_{RISE-FALL}$	Output rise & fall time(1)	20/80%, C_L= 5pF, slow mode		1000		ps
T_{SKEW}	Output-to-output skew(2)	LVCMOS-to-LVCMOS outputs, same divide value		100		ps
T_{SKEW}	Output-to-output skew(2)	LVCMOS-to-Differential outputs, same divide value		400		ps
ODC	Output duty cycle(1)	Not in PLL bypass mode	45		55	%
R_{ON_LVCMOS}	Output impedance	Normal mode		50		Ω
R_{ON_LVCMOS}	Output impedance	Slow mode		65		Ω

(1) Parameters specified by characterization. Not tested at production.
(2) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched within $T_{OUT-SKEW}$. OUT2/OUT3 is matched within $T_{OUT-SKEW}$. Parameters specified by characterization. Not tested at production.

7.18 LP-HCSL Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{O_HCSL}	Output frequency		0.024		350	MHz
V_{OH}	Output high voltage		660		850	mV
V_{OL}	Output low voltage		-150		150	mV
V_{CROSS}	Absolute crossing point	12in, 100 Ω ±10% diff. trace with 2 pF±5%/pin in FR4.	250		550	mV
ΔV_{CROSS}	Relative crossing point variation	w.r.t to average crossing point			140	mV
dV/dt	Slew rate for rising and falling edge	differential, at V_{CROSS} +/-150 mV, f_{O_HCSL}=100 MHz (1)	1		4	V/ns
ΔdV/dt	Slew rate matching	single ended, at V_{CROSS} +/-75 mV, f_{O_HCSL}=100 MHz (1)			20	%
Vrb	Output ringback voltage	Measured on differential output at 100MHz and specifies min voltage from zero crossing	-100		100	mV
Tstable	Time elapsed until ringback	Min time until ringback is allowed	500			ps
ODC	Output duty cycle	Not in PLL bypass mode	45		55	%
$T_{OUT-SKEW}$	Output skew(2)	Same divide value, LP-HCSL to LP-HCSL		100		ps

(1) PCIe test load slew rate
(2) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched within $T_{OUT-SKEW}$. OUT2/OUT3 is matched within $T_{OUT-SKEW}$. There is an additional skew 150ps- 250ps between OUT1/OUT4 and OUT2/OUT3. Parameters specified by characterization. Not tested at production.

7.19 LVDS Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{O\_PRG\_AC}$	Output frequency		0.024		350	MHz
V_{CM}	Output common mode	VDDO_X = 2.5V, 3.3V	1.125	1.2	1.375	V
V_{CM}	Output common mode	VDDO_X = 1.8V	0.9	1.0	1.1	V
V_{OD}	Differential output voltage	VDDO_X = 1.8V (F_{out} < 200MHz), 2.5V, 3.3V.	0.25	0.30	0.45	V
V_{OD}	Differential output voltage	VDDO_X = 1.8V & F_{out} > 200MHz	0.22	0.30	0.45	V
t_{RF}	Output rise/fall times	LVDS (20% to 80%)	450	650	900	ps
ODC	Output duty cycle	Not in PLL bypass mode	45		55	%

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LVDS Output Characteristics (continued)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{OUT-SKEW}$	Output skew(1)	Same divide value, LVDS to LVDS output		100		ps

(1) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched within $T_{OUT-SKEW}$. OUT2/OUT3 is matched within $T_{OUT-SKEW}$. There is an additional skew 150ps- 250ps between OUT1/OUT4 and OUT2/OUT3. Parameters specified by characterization. Not tested at production.

7.20 Output Synchronization Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU_SYNC}	Setup time SYNC pulse(1)	with respect to PLL reference rising edge at 100 MHz with R=1	3			ns
t_{H_SYNC}	Hold time SYNC pulse(1)	with respect to PLL reference rising edge at 100 MHz with R=1			3	ns
t_{PWH_SYNC}	High pulse width for SYNC(1)	With R = 1, at least 2 PFD periods + 24 feedback pre-scaler periods	60			ns
t_{PWL_SYNC}	Low pulse width for SYNC(1)	With R = 1, at least 1 PFD period	6			ns
t_{EN}	Individual output enable time(2)	tri-state to first valid rising edge			4	nCK
t_{DIS}	Individual output disable time(2)	last valid falling edge to tri-state			4	nCK

(1) Designed by characterization. Not tested at production.
(2) Output clock cycles of respective output channel. Global output enable handled by digital logic, additional propagation will be added.

7.21 Power-On Reset Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{THRESHOLD}$	POR threshold voltage(1)	Min-max voltage at which POR is triggered	0.875		1.275	V
$t_{STARTUP}$	Start up time	Startup time after VDD reaches 95% to the time outputs are toggling with correct frequency (input = crystal or external clock)		9		ms
t_{VDD}	Power supply ramp time(2)	timing requirement for any VDD pin while PDN=LOW	0.1		30	ms

(1) POR threshold voltage is the power supply voltage at which the internal reset is de-asserted. It is qualified with PDN. Parameters specified by characterization. Not tested at production.
(2) VDD pin should monotonically reach 95% of its final value within supply ramp time. Parameters specified by characterization. All VDD pins were tied together for this evaluation. For non-monotonic or slower power supply ramp, it is recommended to pull-down PDN pin until VDD pins have reached 95% of its final value. PDN pin has a 50 kΩ pull-up resistor. When PDN pin cannot be actively controlled, it is recommended to add a capacitor to GND on PDN pin to delay the release of reset.

7.22 I^2C-Compatible Serial Interface Characteristics (SDA/GPIO2, SCL/GPIO3)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input Voltage, Logic High		0.7 × VDD_REF			V
V_{IL}	Input Voltage, Logic Low				0.3 × VDD_REF	V
I_{IH}	Input Leakage Current	VDD_REF ± 10%	-10		10	µA
V_{OL}	Low Level Output Voltage	at 3mA sink current			0.4	V
I_{OL}	Low Level Output Current	V_{OL}=0.4V	3			mA
C_{IN}	Input Capacitance(2)				10	pF
C_{OUT}	Output Capacitance (2)	max bus capacitance per pin			400	pF

(1) All I^2C compatible parameters not tested at production.
(2) Guaranteed by Design. Not tested at production.

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7.23 Timing Requirements, I²C-Compatible Serial Interface (SDA/GPIO2, SCL/GPIO3)

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PW_G}	Pulse Width of Suppressed Glitches				50	ns
f_{SCL}	SCL Clock Frequency	Standard		100		kHz
f_{SCL}	SCL Clock Frequency	Fast-mode		400		kHz
t_{SU_STA}	Setup Time Start Condition	SCL=V_{IH} before SDA=V_{IL}		0.6		µs
t_{H_STA}	Hold Time Start Condition	SCL=V_{IL} after SCL=V_{IL} After this time, the first clock edge is generated.		0.6		µs
t_{SU_SDA}	Setup Time Data	SDA valid after SCL=V_{IL}, f_{SCL}=100kHz	250			ns
t_{SU_SDA}	Setup Time Data	SDA valid after SCL=V_{IL}, f_{SCL}=400kHz	100			ns
t_{H_SDA}	Hold Time Data(2)	SDA valid before SCL=V_{IH}	0(3)			(4)µs
t_{VD_SDA}	Valid Data or Acknowledge Time	f_{SCL}=100kHz(4)			3.45	µs
t_{VD_SDA}	Valid Data or Acknowledge Time	f_{SCL}=400kHz(3)			0.9	µs
t_{PWH_SCL}	Pulse Width High, SCL	f_{SCL}=100kHz	4.0			µs
t_{PWH_SCL}	Pulse Width High, SCL	f_{SCL}=400kHz	0.6			µs
t_{PWL_SCL}	Pulse Width Low, SCL	f_{SCL}=100kHz	4.7			µs
t_{PWL_SCL}	Pulse Width Low, SCL	f_{SCL}=400kHz	1.3			µs
t_{IR}	Input Rise Time				300	ns
t_{IF}	Input Fall Time				300	ns
t_{OF}	Output Fall Time	C_{OUT}=10..400pF			250	ns
t_{SU_STOP}	Setup Time Stop Condition			0.6		µs
t_{BUS}	Bus Free Time	Time between a Stop and a Start condition		1.3		µs

(1) All I²C-compatible parameters not tested at production.
(2) t_{H_SDA} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum t_{H_SDA} could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_SDA} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{PWL_SCL}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

7.24 Power Supply Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8V ± 5%, 2.5V ± 5%, 3.3V ± 5% and T_A = -40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD_REF}	VDD_REF supply current	25MHz XTAL, DBL ON		11		mA
I_{DD_VCO}	VCO and PLL current	f_{VCO}=2400MHz, PSA=PSB=4 and N-divider=48		14		mA
I_{DD_OUT}	Output Channel Current	IOD=6, LP-HCSL, 100MHz on OUT3 & OUT4, 25MHz on OUT0		22		mA
I_{DD_OUT}	Output Channel Current	IOD=6, LP-HCSL, 100MHz on OUT1 & OUT2		18.5		mA
I_{DD_PDN}	Power down current	using reset pin / bits		3	10	mA
I_{DD_TYP}	Typical current	4x 100MHz LVDS case using crystal input and doubler, SSC off		55		mA
I_{DD_TYP}	Typical current	4x 100MHz LP-HCSL case using crystal input and doubler, SSC off		65		mA
L_{PSNR}	Power supply noise rejection	OUTx=100MHz differential, on one of VDDx injected sine wave at f_{INJ}=100kHz		tbd		dB
L_{PSNR}	Power supply noise rejection	OUTx=100MHz differential, on one of VDDx injected sine wave at f_{INJ}=1MHz		tbd		dB

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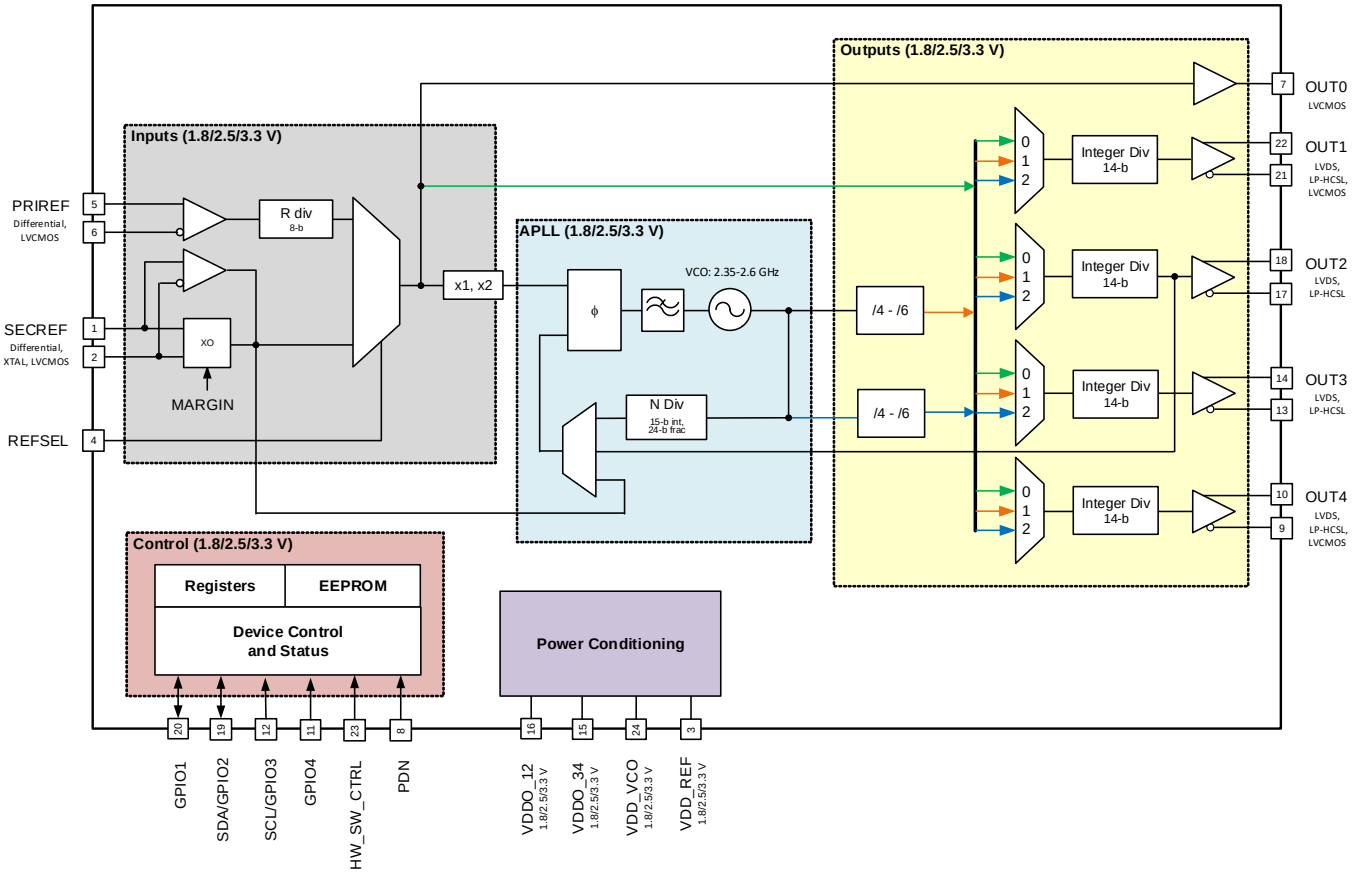
8 Detailed Description

8.1 Overview

CDCE6214-Q1 automotive clock generator is a Phase-Locked Loop (PLL) with integrated loop filter and selectable input reference. The output of the integrated voltage-controlled oscillator (VCO) is connected to the clock distribution network, which includes multiple frequency dividers and multiplexers. The output of these network is connected to four output channels with configurable differential and single ended buffers. CDCE6214-Q1 can be configured using I2C serial interface or built-in EEPROM at power up.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CDCE6214-Q1 Blocks

The following sections describe the individual blocks of the CDCE6214-Q1.

8.3.1.1 Reference Block

A reference clock to the PLL is fed to pins 1 (SECREF_P) and 2 (SECREF_N) or to pins 5 (PRIREF_P) and 6 (PRIREF_N). There are multiple input stages to accommodate various clock references. Pins 1 and 2 can be used to connect a XTAL across it or provide an external single-ended LVCMOS clock or a differential clock. These modes are selectable through register programming. When differential mode is selected, the inputs are automatically AC-coupled and biased appropriately for proper functioning of the input stage. When XTAL or LVCMOS mode is selected, internal AC-coupling capacitor and biasing circuitry is disengaged. Pins 5 and 6 can be used to provide an external single-ended LVCMOS clock or a differential clock.

Feature Description (continued)

The reference MUX selects the reference clock for the PLL. Pin 4 (REFSEL) can be used to select PRIREF or SECREF Input path. Alternatively, this can be configured through the register settings.

A reference divider or a clock doubler can be engaged to further multiply (2x) or divide the reference clock to the PLL.

The output clock from the reference block can be bypassed to the OUT0 and other output channels. The bypassed clock is selectable between the Input clock or PFD clock.

8.3.1.2 XTAL Oscillator

The SECREF_P and SECREF_N pins provide a crystal oscillator stage to drive a fundamental mode crystal in the range of 10 MHz to 50 MHz. The crystal input stage integrates a tunable load capacitor array up to 9 pF. The drive capability of the oscillator is adjusted using register programming.

8.3.1.3 LVCMOS

The LVCMOS input buffer threshold voltage follows VDD_REF. This allows the engineer to use the device as a level shifter because the outputs all have separate supplies.

8.3.1.4 Differential AC-Coupled

The differential input stage has an internal bias generator and internal AC-coupling capacitor. It should only be used as an AC-coupled reference input.

8.3.1.5 Reference MUX

Either PRIREF or SECREF can be selected as clock to the PLL and clock distribution path. The reference MUX is controlled either through pin 4 (REFSEL) or through the register settings.

8.3.1.6 Reference Divider

A reference divider can be used to divide higher input frequencies to the permitted PFD range. It supports division values of 1 to 255.

8.3.1.7 Reference Doubler

The reference path contains a doubler circuit. It is used to double the input frequency and can be used to achieve the highest PFD update frequency of 100 MHz using a 50-MHz crystal or PFD update frequency of 50 MHz using a 25-MHz crystal.

8.3.1.8 Clock Bypass

The input reference clock or the PFD clock can be bypassed to OUT0 (LVCMOS output). It can also be bypassed to the OUT1–OUT4 pins, which are selectable among other clock distribution networks.

8.3.2 Phase-Locked Loop (PLL)

The CDCE6214-Q1 has a fully integrated Phase-Locked Loop (PLL) circuit. The error between a reference phase and an internal feedback phase is compared at the phase-frequency-detector. The comparison result is fed to a charge pump that is connected to an integrated loop filter. The control voltage resulting from the loop filter tunes an internal voltage-controlled oscillator (VCO). The frequency of the VCO is fed through a feedback divider (N-counter) back to the PFD.

- Integer and Fractional-N PLL mode of operation.
- 24-bit Numerator and Denominator can be used to generate fractional frequencies with frequency accuracy better than 0.1ppm.
- PFD operates between 1 MHz and 100 MHz.
- Live Lock Detector provides PLL Lock status (not in SSC mode). Additionally, sticky bit lock detect detects if there was any temporary loss of lock.
- Integrated selectable loop filter components.
- For a 25-MHz PFD frequency, PFD bandwidth between 100 kHz and 1.6 MHz can be achieved to optimize

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Feature Description (continued)

PLL to input reference.

- Voltage-controlled oscillator (VCO) ranges from 2350 MHz to 2600 MHz.
- Supports 0.25% and 0.5% centre and down-spread Spread Spectrum Clocking (SSC) generation. Further, VCO also supports up to 0.5% SSC references at 100 MHz.

8.3.2.1 Spread Spectrum Clocking

This device support triangular-mode, spread-spectrum clocking. SSC clock is generated through the fractional dividers in the PLL through fractional-N operation. When SSC is enabled, SSC clock is available on all clock sourced from the PLL. Reference clock or PFD clock is available on the OUT1–OUT4 pins.

Down-spread and centre-spread is supported. The following modes are supported.

- PFD frequencies: Either 25 MHz or 50 MHz or 100 MHz.
- Down-spread: –0.25% and ±0.5%
- Centre-spread: ±0.25% and ±0.5%

Pre-configured settings are available to select any of these combinations.

Using these pre-configured settings, fmod of 31.5 kHz is synthesized for 100-MHz output clock.

8.3.3 Clock Distribution

The VCO connects to two individually configurable pre-scaler dividers sourcing the on-chip clock distribution – PSA and PSB.

The clock distribution consists of four output channels. Each output channel contains an integer divider (IOD) with glitch-less switching and synchronization capabilities.

IOD can be sourced from either the PSA, the PSB, or the Reference Clock. IOD can be bypassed to provide a Reference clock at the output.

There are five output channels – OUT0, OUT1, OUT2, OUT3, and OUT4.

The OUT0 is a slew-rate controllable LVCMOS output. Either the reference clock or PFD clock can be routed to this output through the clock distribution network.

The OUT1 and OUT4 are identical output channels. The output buffers in this channel are compatible with various signalling standards – LVCMOS, LP-HCSL, and LVDS-like.

The OUT2 and OUT3 are identical output channels. The output buffers in this channel are compatible with various signalling standards – LP-HCSL and LVDS-like.

- The LP-HCSL output buffer can be directly connected to the receiver without any termination resistor to GND. The output impedance of LP-HCSL is trimmed to 50 Ω. A series resistor can be used to adapt to the trace impedance.
- The LVDS-like requires a differential termination connected between the positive and negative polarity output pins. The termination can be connected directly or through an AC-coupling capacitor. For a 50-Ω system, a 100-Ω differential termination is appropriate.
- LVCMOS outputs are designed for capacitive loads only. The polarity of the positive and negative output pins can be configured individually.

The differential buffers support wide range of output frequencies up to 350 MHz. LVCMOS supports up to 200 MHz.

8.3.3.1 Glitch-Less Operation

The bit fields ch{x}_glitchless_en can be used to enable glitch-less output divider update. This feature ensures that the high pulse of a clock period is not cut off by the output divider update process. It ensures that setup and hold time of a receiver is not violated. The low pulse in the transition from earlier period to the new period is extended accordingly.

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Feature Description (continued)

8.3.3.2 Divider Synchronization

The output dividers can be reset in a deterministic way. This can be achieved using the sync bit or PDN pin. The level of the pin is qualified internally using the reference frequency at the PFD. A low level will mute the outputs. A high level will synchronously release all output dividers to operation, so that all outputs share a common rising edge. The first rising edge can be individually delayed in steps of the respective pre-scaler period, up to 32 cycles using ch{x}_sync_delay. This allows the user to compensate external delays like routing mismatch, cables, or inherent delays introduced by logic gates in an FPGA design. Each channel can be included or excluded from the SYNC process.

For a deterministic behaviour over power-cycles seen from input to output the reference divider must be set to 1. It should not divide the reference clock nor should the reference doubler be used.

8.3.4 Control Pins

The ultra-low power clock generator is controlled by multiple LVCMOS input pins.

The HW_SW_CTRL acts as EEPROM page select. The CDCE6214-Q1 clock generator contains two pages of configuration settings. The level of this pin is sampled after device power-up. A low level selects Page 0. A high level selects page one. The EEPROMSEL pin is a tri-level input pin. This third voltage level is automatically applied by an internal voltage divider. The mid-level is used to select an internal default where the serial interface is enabled.

PDN (pin 8) resets the internal circuitry and is used in the initial power-up sequence. The pin can be reconfigured to act as synchronization input. The differential outputs are kept in mute while SYNC is low. When SYNC is high, outputs are active. Moreover status signals can be observed on this pin.

The SCL (pin 12) can act as general-purpose input or Clock pin for I2C Interface.

The SDA (pin 19) can act as general-purpose input or Data pin for I2C Interface.

The REFSEL is used to select between the input references to the PLL. A low level selects the SECREF input pins. A high level selects the PRIREF input pins.

8.3.4.1 Global and Individual Output Enable

The output enable functionality allows the user to enable or disable all or a specific output buffer. The bypass copy on OUT0 is excluded from the global output enable signal. When an output is disabled, it drives a configurable mute-state. When the serial interface is deactivated one can use all individual output enable signals at the same time. The individual output enable signal controls the respective output channel integer divider to gate the clock. Therefore each integer divider needs to be active.

The individual output enable signal enables and disables the respective output in a deterministic way. Therefore the high and low level of the signal is qualified by counting four cycles of the respective output clock.

1. The OE falling edge disables the output. The output is enabled for 4 cycles after asserting the Output Enable of a channel. This will enable any further operation in the system after OE is asserted.
2. The OE rising edge enables the output. Outputs starts toggling after 4 internal clock cycles.

8.3.5 EEPROM - Cyclic Redundancy Check

The device contains a cyclic redundancy check (CRC) function for reads from the EEPROM to the device registers. At start-up the EEPROM will be read internally and a CRC value calculated. One of the EEPROM words contains an earlier stored CRC value. The stored and the actual CRC value are compared and the result transferred to register. The CRC calculation can be triggered again by writing a 1 to the update_crc bit. A mismatch between stored and calculated CRC value is informational only and non-blocking to the device operation. Just reading back the CRC status bit and the live CRC value can speed up in-system EEPROM programming and avoid reading back each word of the EEPROM for known configurations.

The polynomial used is CCITT-CRC16: $x^{16} + x^{12} + x^5 + 1$.

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8.4 Device Functional Modes

8.4.1 Zero Delay Mode

There are two types of Zero Delay mode supported in this device: Internal Zero Delay and External Zero Delay. For zero delay mode operation, TI recommends to use the external zero delay mode. In this mode, the PRIREF clock is used as input to the PFD. The output of one of the channels can be routed back to the SECREF pin as an external clock. In case of internal zero delay mode, the output of OUT2 is internally looped back.

8.4.2 Digitally-Controlled Oscillator (DCO) or Frequency Increment/Decrement Mode.

Digitally-Controlled Oscillator (DCO) mode can be used to increment/decrement the output frequency in smaller step size as low as 10ppb. There are two ways to control the frequency increment/decrement functionality:

1. Through a I2C register write. Writing into FREQ_INC register would increment one-step size. Writing into FREQ_DEC register would decrement one-step size.
2. Through the GPIO pins configured as Frequency Increment/Decrement. Every rising edge on the FREQ_INC signal increases the output frequency, thus decreases the division value. Every rising edge on the FREQ_DEC signal decreases the output frequency, thus increases the division value.

The step-size of such change is defined in the registers through the I^2C or EEPROM.

8.5 Programming

8.5.1 Modes of Operation

There are various modes of operation of the device.

1. Fall-back mode: Setting HW_SW_CTRL pin = M (Float) and REFSEL = M (float) would bypass loading contents of EEPROM at power-up. Also, the PLL would not be auto-calibrated, and the I2C interface would be active. This mode would allow the user to fully configure the device before re-locking the PLL.
2. Page 0: Setting HW_SW_CTRL pin = L and REFSEL = L or H would allow loading the contents of EEPROM Page 0 at power up. The PLL would automatically recalibrate and output is enabled after PLL_LOCK.
3. Page 1: Setting HW_SW_CTRL pin = H and REFSEL = L or H would allow loading the contents of EEPROM Page 1 at power up. The PLL would automatically recalibrate and output is enabled after PLL_LOCK.

8.5.1.1 I2C Serial Interface

The CDCE6214-Q1 ultra-low power clock generator provides an I2C-compatible serial interface for register and EEPROM access. The device is compatible to standard-mode I2C at 100 kHz and the fast-mode I2C at 400-kHz clock frequency.

1. In Fall-back Mode, I2C slave address = 67h.
2. In other modes, I2C slave address = 68h (Default).
3. The LSB bit of the device can be programmed in the EEPROM. For example, if I2C_A0 is programmed H in Page 0 of EEPROM, setting HW_SW_CTRL=0 would set I2C address as 69h.
4. Two devices with EEPROM + 1 device in fall-back mode can be used on the same I2C bus with addresses 67h, 68h and 69h.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application using I2C interface and 25-MHz crystal input is shown in Figure 1. The two ends of 25-MHz XTAL are connected to pin 1 and 2. The REFSEL pin is pulled down to select a secondary input. The HW_SW_CTRL can be pulled either low or high if EEPROM is used, or kept floating if EEPROM is unused. 1.8 V, 2.5 V, or 3.3 V can be supplied to the VDD_REF and VDD_VCO pins, as well as VDDO_12 and VDDO_34 pins with filtering. Data and clock lines of I2C must be pulled to VDD_REF using pullup resistors. The PDN can be connected to the MCU if a hardware reset is required, otherwise it can be left floating. The GPIO1 and 4 pins can be connected to the MCU if needed, otherwise they can be left floating. Unused outputs can be left floating.

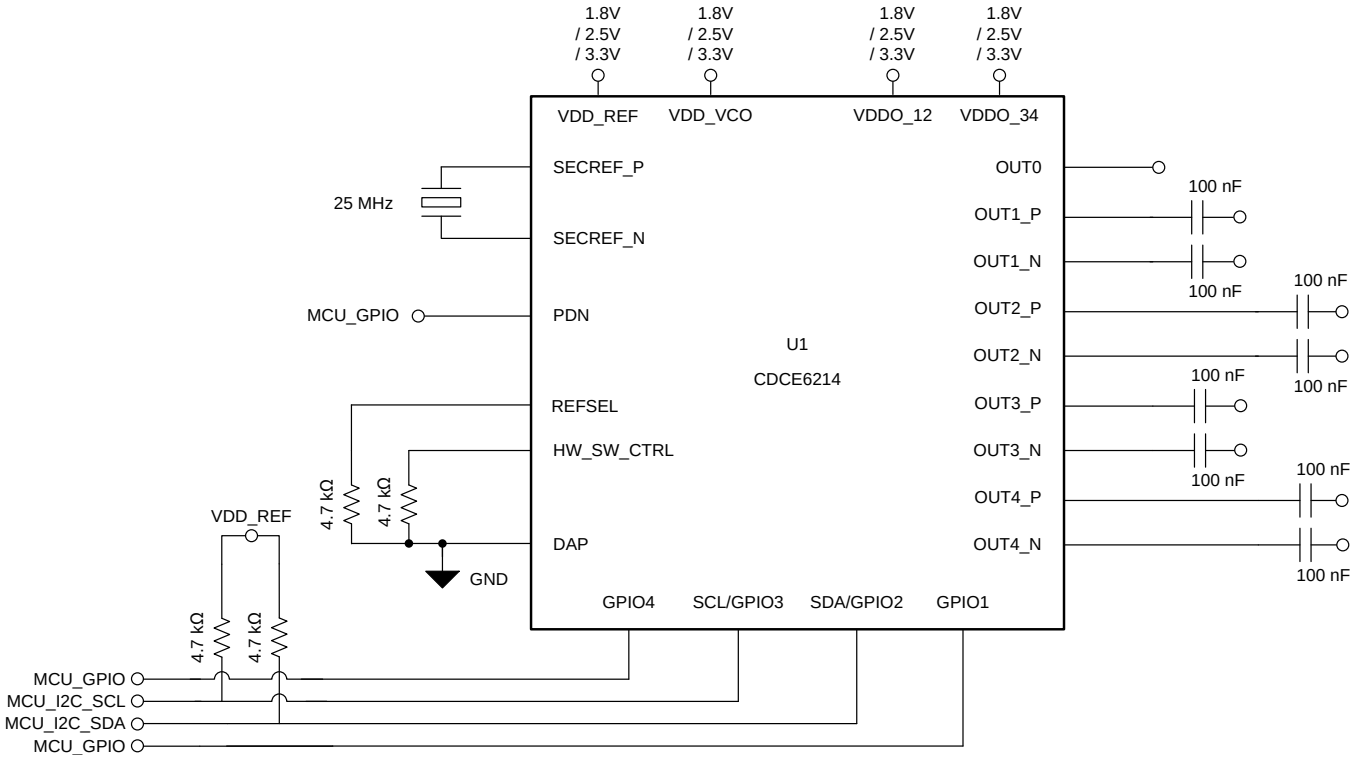


Figure 1. Typical Application Schematic With I2C Interface

ADVANCE INFORMATION

9.2 Typical Application

Figure 2 shows typical block diagram for eAVB system using CDCE6214-Q1.

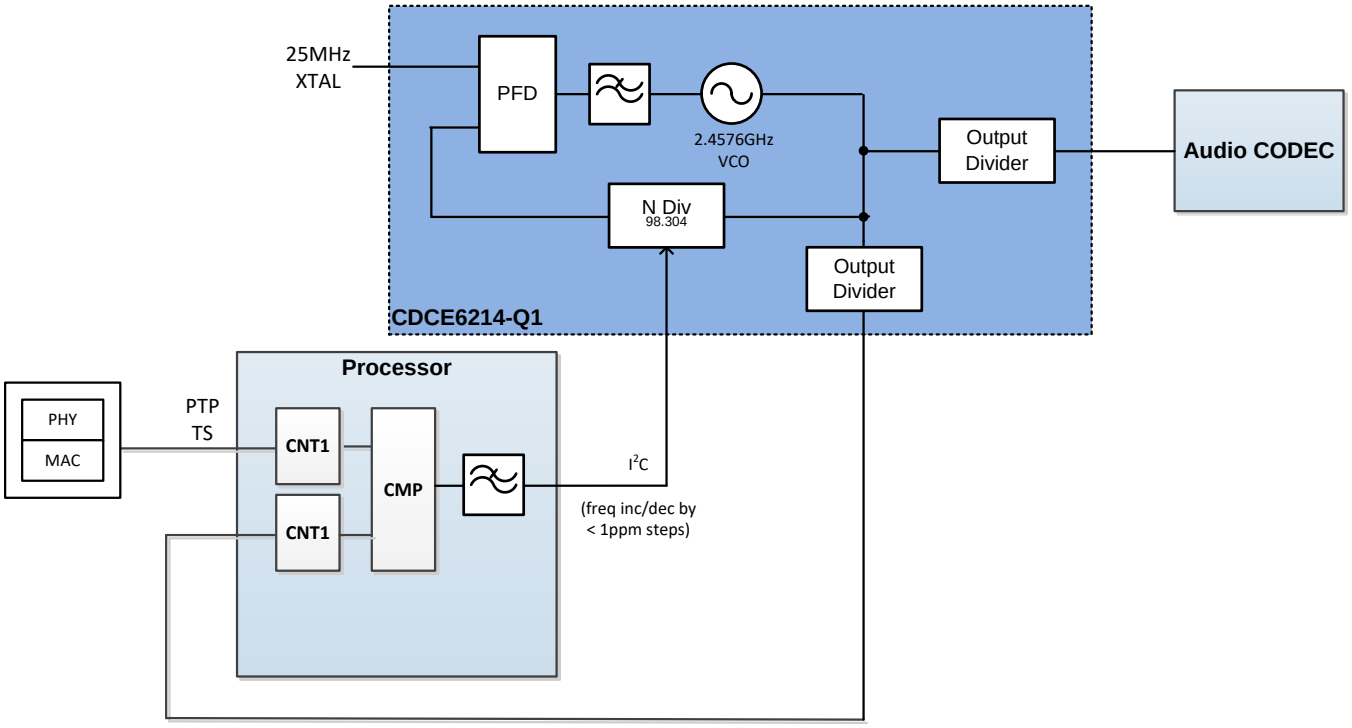


Figure 2. eAVB System Block Diagram Using CDCE6214-Q1

9.2.1 Design Requirements

For designs with the CDCE6214-Q1, the designer must select:

- a primary or secondary input
- an input type
- an input frequency
- a device communication mode (I2C and/or EEPROM)
- the required device operation modes to configure the connections of GPIO pins
- a supply voltage (1.8 V, 2.5 V, or 3.3V)
- a digital reference (1.8 V, 2.5 V, or 3.3 V)
- an output reference (1.8 V, 2.5 V, or 3.3 V)
- an output format

9.2.2 Detailed Design Procedure

The CDCE6214-Q1 is designed for ease-of-use. To power up the device:

1. Either tie the power supply pin (VDD_REF, VDD_VCO, VDDO_12 and VDDO_34) together or independently connect them to the 1.8-V, 2.5-V, or 3.3-V power supply.
2. Solder the GND Pin (DAP) to the PCB Plane.
3. Ensure that the REFSEL, HW_SW_CTRL, and PDN configuration pins are appropriately connected.
    1. Internally connect the PDN pin to VDD_REF through a pullup resistor. When floating, the PDN pin would automatically release device from PDN.
    2. If PDN pin is low, the device will not respond to I2C commands.
    3. REFSEL and HW_SW_CTRL are tri-level pins. If left floating, the device will start in fall-back mode.

ADVANCE INFORMATION

Typical Application (continued)

The device is factory-configured to provide:

- 100-MHz LVDS with 25-MHz XTAL when HW_SW_CTRL=L. The 25-MHz output on OUT0 is enabled.
- 100-MHz LP-HCSL with 25-MHz XTAL and HW_SW_CTRL = H. The 25-MHz output on OUT0 is enabled.

10 Power Supply Recommendations

The CDCE6214-Q1 provides multiple power supply pins. Each power supply supports 1.8 V, 2.5 V, or 3.3 V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with its individual supply voltage. The VDD_REF pin supplies the control pins and the serial interface. Therefore, any pullup resistors shall be connected to the same domain as VDD_REF. VDD_VCO powers all PLL blocks. VDDO_12 powers outputs OUT1 and OUT2. VDDO_34 powers OUT0, OUT3, and OUT4.

Using different VDD_REF and VDDO_34 can be used for level translation operation on OUT0.

10.1 Power-Up Sequence

There are no restrictions from the device for applying power to the supply pins. From an application perspective, TI recommends to either apply all the VDDs at the same time or apply the VDDREF first. The digital core is connected to VDDREF and thus the settings of the EEPROM are applied automatically.

10.2 Decoupling

TI recommends isolating all power supplies using a ferrite bead and provide decoupling for each of the supplies. TI also recommends optimizing the decoupling for the respective layout, and consider the power supply impedance to optimize for the individual frequency plan.

An example for a decoupling per supply pin: 1x 4.7 µF, 1x 470 nF, and 1x 100 nF.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

For this example, follow these guidelines:

- Isolate inputs and outputs using a GND shield. routes all inputs and outputs as differential pairs.
- Isolate outputs to adjacent outputs when generating multiple frequencies.
- Isolate the crystal area, connect the GND pads of the crystal package and flood the adjacent area. Figure 4 shows a foot print which supports multiple crystal sizes.
- Try to avoid impedance jumps in the fan-in and fan-out areas when possible.
- Use five VIAs to connect the thermal pad to a solid GND plane. Full-through VIAs are preferred.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Try to place them very close on the same layer or directly on the backside layer. Larger values can be placed more far away. Figure 4 shows three decoupling capacitors close to the device. Ferrite beads are recommended to isolate the different frequency domains and the VDD_VCO domain.
- Preferably use multiple VIAs to connect wide supply traces to the respective power planes.

11.2 Layout Examples

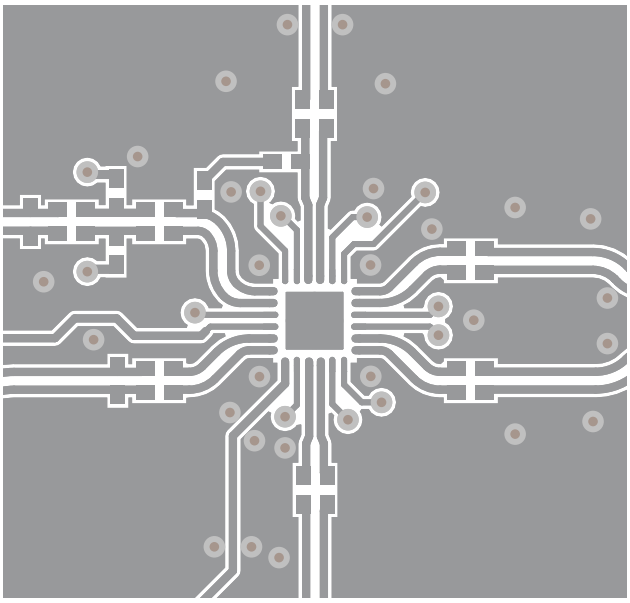


Figure 3. Layout Example, Top Layer

Layout Examples (continued)

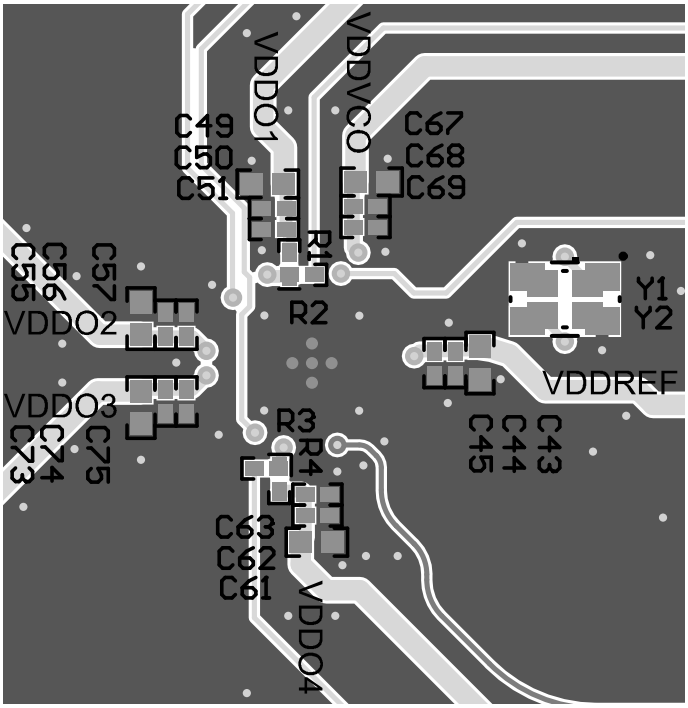


Figure 4. Layout Example, Bottom Layer

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Contact your TI representative for more information.

12.1.2 Device Nomenclature

CDCE6214-Q1 - 62= clock generator 1= 1x PLL 4=4x outputs E = EEPROM, integer and fractional output dividers

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

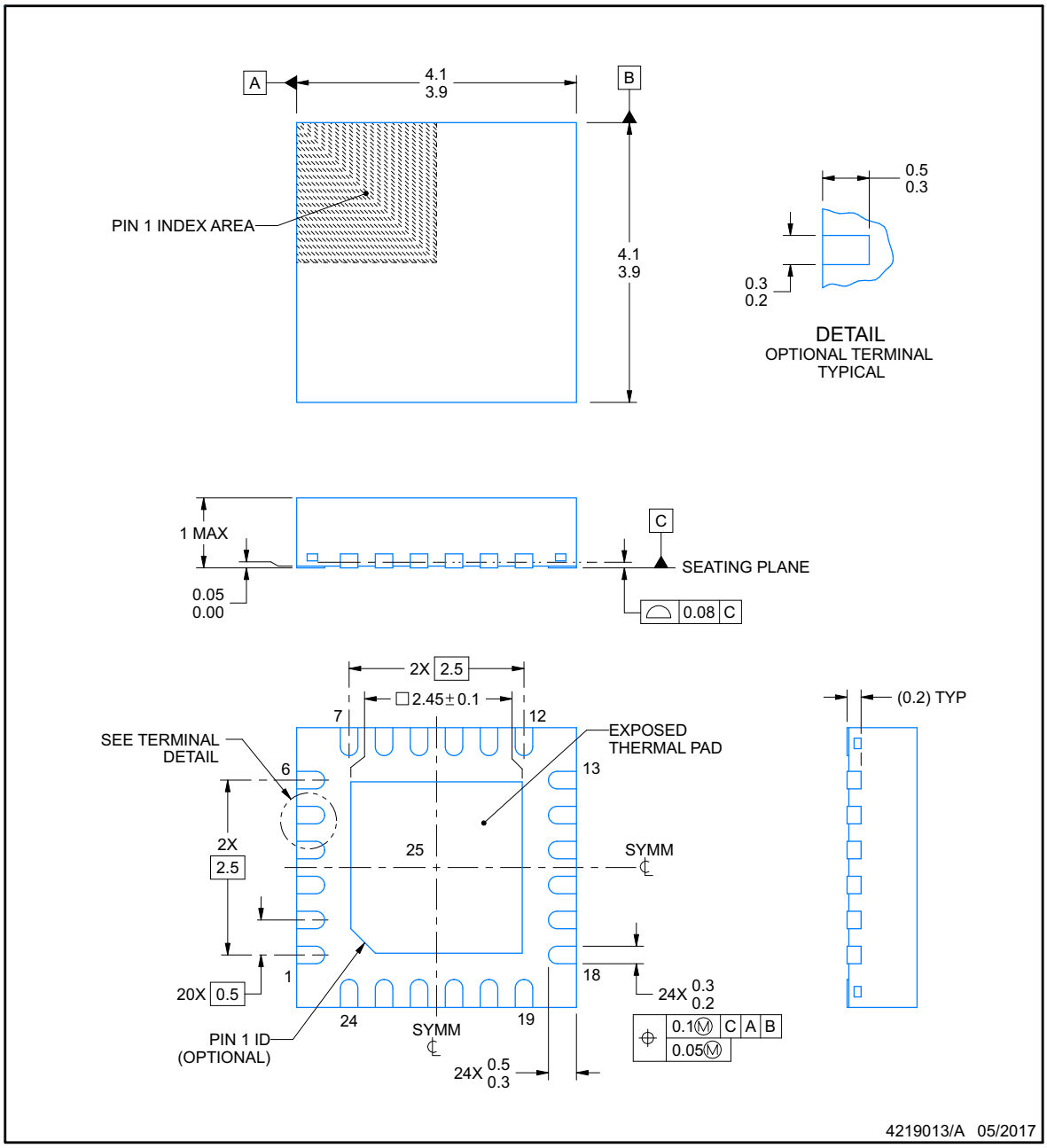
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

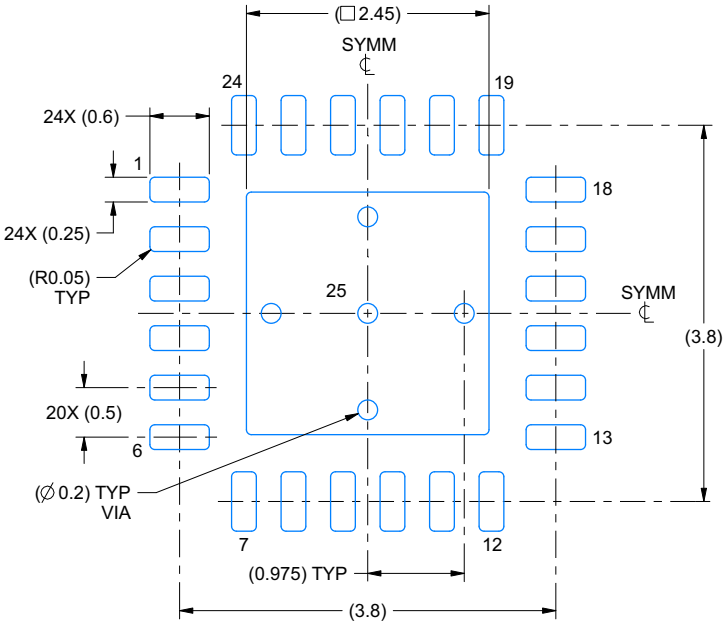
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

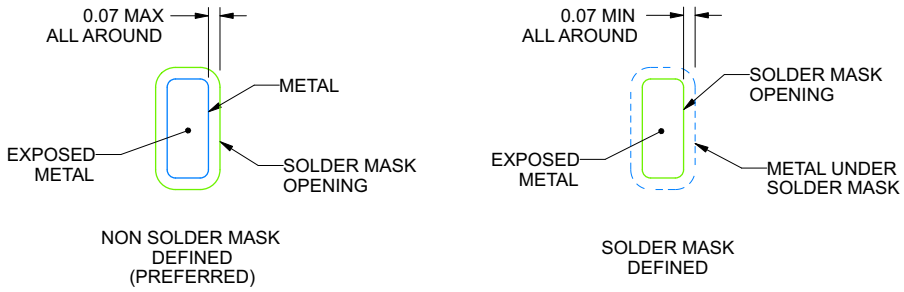
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

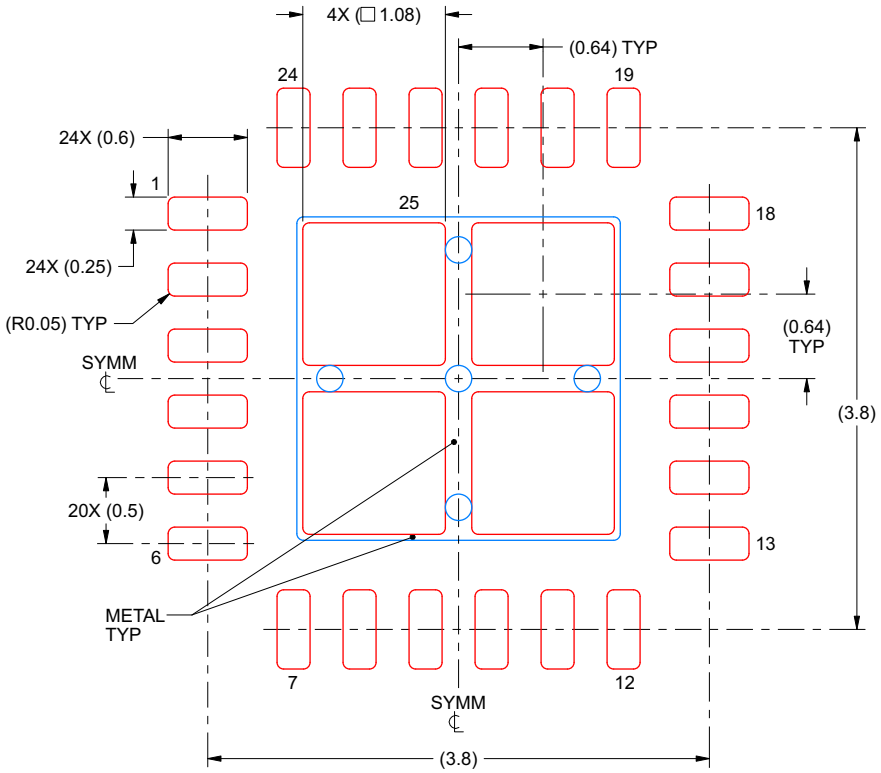
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE6214TWRGERQ1	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI			
CDCE6214TWRGETQ1	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI			
PCDCE6214TWRGETQ1	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

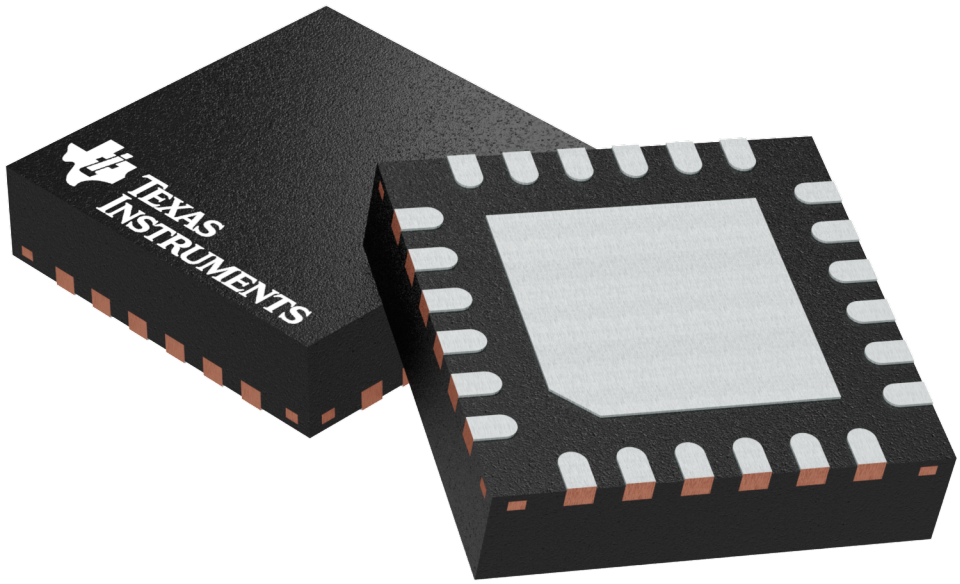
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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