CC3220MODx 和 CC3220MODAx SimpleLink™ Wi-Fi® CERTIFIED™ 无线 MCU 模块

1 模块概述

1.1 特性

- CC3220MODx 是一个无线 MCU 模块系列，包含 SimpleLink ™ Wi-Fi®单芯片无线 MCU，其中 CC3220MODS 和 CC3220MODAS 模块包含 CC3220SM2ARGK 无线 MCU，CC3220MODSF 和 CC3220MODASF 模块包含 CC3220SF12ARGK 无线 MCU。完全集成的工业温度级绿色模块，包括所有必需的时钟、SPI 闪存和无源器件
- CC3220MODAx 模块包含一体化天线，可轻松集成到主机系统中
- CC3220MODx 和 CC3220MODAx SimpleLink™ Wi-Fi® 无线 MCU 片上系统 (SoC) 包含支持两种独立执行环境的单芯片：
  - 用户应用专用 Arm® Cortex®-M4 MCU
  - 用以运行所有 Wi-Fi 和互联网逻辑层的网络处理器 MCU
- 经过 FCC、IC、CE、MIC 和 SRRC 认证
- Wi-Fi Alliance 成员可申请转让 Wi-Fi CERTIFIED™ 模块
- 1.27mm 间距 QFM 封装便于实现轻松组装和低成本 PCB 设计
- 应用 MCU 子系统
  - Arm® Cortex®-M4 内核，运行频率 80MHz
  - 嵌入式存储器
    - CC3220MODS 和 CC3220MODAx 型号包含 256KB RAM
    - CC3220MODSF 和 CC3220MODASF 是基于闪存的 MCU，具有集成的 1MB 闪存和 256KB RAM
    - 采用 ROM 的外设驱动器
  - McASP 支持两个 I2S 通道
  - SD
  - SPI
  - I^2C
  - UART
  - 8 位同步图像接口
  - 4 个具有 16 位 PWM 模式的通用计时器 (GPT)
  - 1 个看门狗计时器模块
  - 4 通道、12 位模数转换器 (ADC)
  - 调试接口：JTAG、cJTAG 和 SWD
- Wi-Fi 网络处理器子系统
  - Wi-Fi® Internet-on-a-chip™专用 Arm® MCU 可充分减轻应用 MCU 承担的 Wi-Fi 和互联网协议压力
  - Wi-Fi® 模式
    - 802.11b/g/n 基站
    - 802.11b/g/n 接入点支持多达 4 个基站
    - Wi-Fi Direct®客户端和组所有者
    - WPA2™个人和企业安全性：WEP、 WPA ™、WPA2 PSK 和 WPA2 企业版 (802.1x)
    - IPv4 和 IPv6 TCP 与 IP 堆栈
    - 业界标准的 BSD 套接字应用编程接口 (API)
      - 16 个同步 TCP 或 UDP 套接字
      - 6 个同步 TLS 和 SSL 套接字
    - IP 寻址：具有重复地址检测 (DAD) 的 StaticIP、LLA、DHCPv4、DHCPv6
    - SimpleLink 技术连接管理器，可实现自主快速的 Wi-Fi 连接
    - 借助以下特性，实现灵活的 Wi-Fi 配置：SmartConfig™技术、AP 模式和 WPS2 选项
    - RESTful API 支持（使用内部 HTTP 服务器）
    - 嵌入式网络 应用 在专用网络处理器上运行
    - 广泛的安全 特性的 xHCI 控制器：
      - 硬件 特性的 xHCI 控制器：
        - 独立执行环境
        - 器件标识
        - 可实现高级快速安全性的硬件加密引擎（包括 AES、DES、3DES、SHA2、MD5、CRC 和校验和）
      - 初始安全编程
        - 调试安全性
        - JTAG 和调试端口处于锁定状态
      - 个人和企业 Wi-Fi 安全性
      - 安全套接字（SSLv3、TLS1.0、TLS1.1、TLS1.2）

  - 网络安全性
    - HTTPS 服务器
    - 受信任的根证书目录
    - TI 信任根公钥
  - SW IP 保护
    - 安全密钥存储
    - 文件系统安全
    - 软件篡改检测
    - 克隆保护
    - 安全启动：启动期间验证运行时二进制的完整性和真实性
  - 嵌入式网络 应用 在专用网络处理器上运行
    - 具有动态用户回调的 HTTP 和 HTTPS 网络服务器
    - mDNS、DNS-SD 和 DHCP 服务器
    - Ping
  - 恢复机制：可恢复到出厂默认设置或恢复到完整出厂映像
- Wi-Fi TX 功率
  - 1 DSSS 时为 17.0dBm
  - 54 OFDM 时为 13.5dBm
- Wi-Fi RX 灵敏度
  - 1 DSSS 时为 –95.0dBm
  - 54 OFDM 时为 –73.5dBm
- 应用数据吞吐量
  - UDP：16Mbps
  - TCP：13Mbps
- 电源管理子系统
  - 具有宽电源电压的集成式直流/直流转换器
    - V_{BAT}：2.3V - 3.6V
  - 高级低功耗模式:
    - 关断：1µA
    - 休眠：5µA
    - 低功耗深度睡眠 (LPDS)：135µA（测试对象为具有 256KB RAM 保持的 CC3220MODS 和 CC3220MODSF）
    - RX 流量（MCU 处于活跃状态）：54 OFDM 时为 59mA（测试对象为 CC3220MODS；CC3220MODSF 和 CC3220MODASF 会额外消耗 15mA）
    - TX 流量（MCU 处于活跃状态）：在 54 OFDM、最大功耗时为 223mA（测试对象为 CC3220MODS；CC3220MODSF 和 CC3220MODASF 会额外消耗 15mA）
    - 空闲连接（MCU 处于 LPDS 状态）：DTIM = 1 时为 710µA（测试对象为具有 256KB RAM 保持的 CC3220MODS 和 CC3220MODSF）
- 其他集成组件
  - 40.0MHz 晶体
  - 32.768kHz 晶体 (RTC)
  - 32 兆位串行闪存
  - 射频滤波器和无源组件
- 尺寸兼容的 QFM 封装
  - CC3220MODx：1.27mm 间距、63 引脚、20.5mm × 17.5mm
  - CC3220MODAx：1.27mm 间距、63 引脚、20.5mm × 25.0mm
- 工作温度
  - 环境温度范围：–40°C 至 +85°C
- 模块支持 SimpleLink 开发人员生态系统

1.2 应用

物联网 (IoT) 应用，包括：

- 家庭和楼宇自动化
- 低功耗摄像头
- 温度调节装置
- 访问控制和电子锁 (E-Lock)
- 资产跟踪和实时定位系统 (RTLS) 标签
- 云连接
- 互联网网关
- 设备
- 安防系统
- 智能能源
- 工业控制
- 智能插座和仪表计量
- 无线音频
- IP 网络传感器节点
- 医疗设备

1.3 说明

使用此完全可编程的无线微控制器 (MCU) 模块开始您的设计，它经过 FCC、IC、CE、MIC 和 SRRC 认证，且具有内置 Wi-Fi 连接。德州仪器 (TI) 的 SimpleLink™ CC3220MODx 和 CC3220MODAx 模块系列专为 IoT 而设计， 是一款™集成了两个物理独立片上 MCU 的无线模块。

- 应用处理器 Arm® Cortex®-M4 MCU 具有用户专用的 256KB RAM（CC3220SF 型号上具有 1MB XIP 闪存）。
- 一个网络处理器 MCU，可运行所有 Wi-Fi® 和互联网逻辑层。此基于 ROM 的子系统包含 802.11b/g/n 无线电、基带和具有强大加密引擎的 MAC，采用 256 位加密，可实现快速安全的互联网连接。

CC3220MODx 和 CC3220MODAx 无线 MCU 系列属于 TI 第二代 Internet-on-a chip™ 系列解决方案。此代产品引入了新的 特性 和功能，可进一步简化物联网连接。新功能包括：

- IPv6
- 增强的 Wi-Fi 配置
- 优化的低功耗管理
- 增强的文件系统安全
- Wi-Fi AP 可连接多达 4 个基站
- 可同时打开更多的 BSD 套接字—多达 16 个 BSD 套接字（其中 6 个支持安全型 HTTPS）
- 支持 HTTPS
- 支持 RESTful API
- 非对称密钥加密库

CC3220MODx 和 CC3220MODAx 无线 MCU 系列支持以下模式：基站、AP 和 Wi-Fi Direct®。CC3220MODx 和 CC3220MODAx 模块还支持 WPA2 个人和企业安全版。该子系统包含嵌入式 TCP/IP 和 TLS/SSL 堆栈、HTTP 服务器和多个互联网协议。该模块支持多种 Wi-Fi 配置方法，包括基于 AP 模式的 HTTP、SmartConfig™ 技术和 WPS2.0。

电源管理子系统包括支持宽电源电压范围的集成式直流/直流转换器。此子系统支持低功耗深度睡眠、RTC 休眠（仅消耗 5µA）和关断模式（仅消耗
1µA）等低功耗模式，有助于延长电池寿命。

该模块包含多种外设，如快速并行摄像头接口、I2S、SD、UART、SPI、I^2C 和 4 通道 ADC。

SimpleLink CC3220MODx 和 CC3220MODAx 模块系列有 4 个不同的模块型号：CC3220MODS、CC3220MODSF、CC3220MODA 和 CC3220MODASF。

- CC3220MODS 和 CC3220MODAS 模块包含用于处理代码和数据的应用专用型嵌入式 RAM (256KB)。此外，CC3220MODAS 还包含一体式天线。
- CC3220MODSF 和 CC3220MODASF 模块包含用于处理代码和数据的应用专用型串行闪存 (1MB) 和 RAM (256KB)。此外，CC3220MODASF 还包含一体式天线。

这 4 个模块集成有 40MHz 晶体、32.768kHz RTC 时钟、32Mb SPI 串行闪存、射频滤波器和无源组件。这些模块还具有其他安全 特性，例如已经过加密和身份验证的文件系统、用户 IP 加密和身份验证、安全引导（闪存引导时对应用映像进行身份验证和完整性验证）等。

CC3220MODx 和 CC3220MODAx 器件是 SimpleLink™ MCU 平台的一部分，包含 Wi-Fi、 低功耗 *Bluetooth*®、低于 1GHz 器件和主机 MCU。它们都共用配有单核软件开发套件 (SDK) 和丰富工具集的通用、易用型开发环境。一次性集成 SimpleLink 平台后，用户可以将产品组合中器件的任何组合添加至您的设计中。SimpleLink 平台的最终目标是确保设计要求变更时，完全重复使用代码。

CC3220MODx 和 CC3220MODAx 模块系列是一个完整的平台解决方案，其中包含软件、示例 应用、工具、用户和编程指南、参考设计和 E2E™在线社区。该模块系列还是 SimpleLink™ MCU 产品系列的一部分，并且支持 SimpleLink™ 开发人员生态系统。更多详细信息，请访问 www.ti.com/simplelink。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
CC3220MODSM2MOBR	QFM (63)	20.50mm × 17.50mm
CC3220MODSF12MOBR	QFM (63)	20.50mm × 17.50mm
CC3220MODASM2MONR	QFM (63)	25.50mm × 20.50mm
CC3220MODASF12MONR	QFM (63)	25.50mm × 20.50mm

(1) 有关详细信息，请参阅 节 10。

1.4 功能方框图

图 1-1 显示了 CC3220MODx 模块的功能方框图。

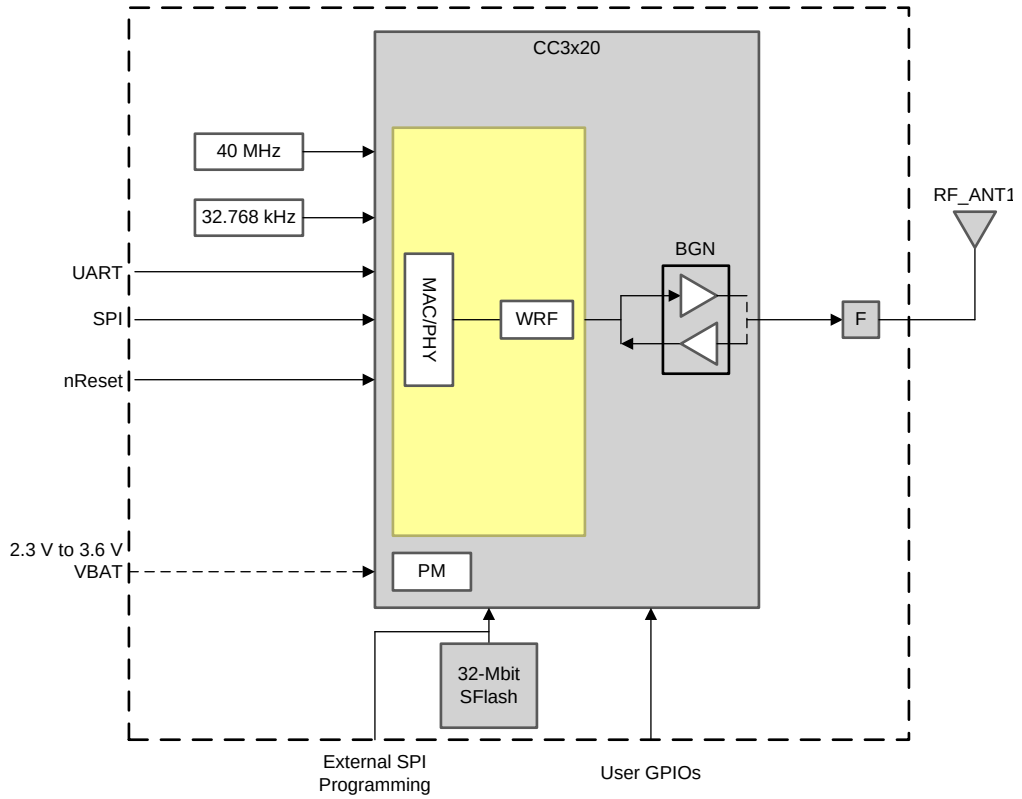


图 **1-1. CC3220MODx** 功能方框图

图 1-2 显示了 CC3220MODAx 模块的功能方框图。

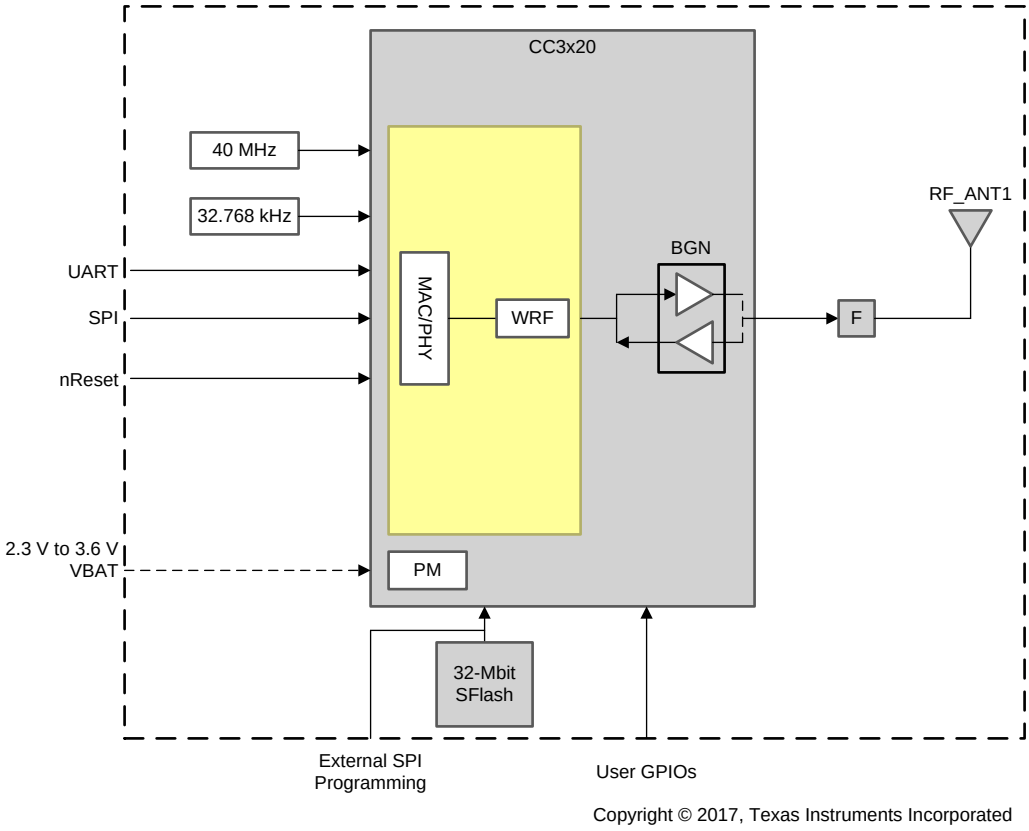


图 1-2. CC3220MODAx 功能方框图

图 1-3 显示了 CC3220x 硬件概述。

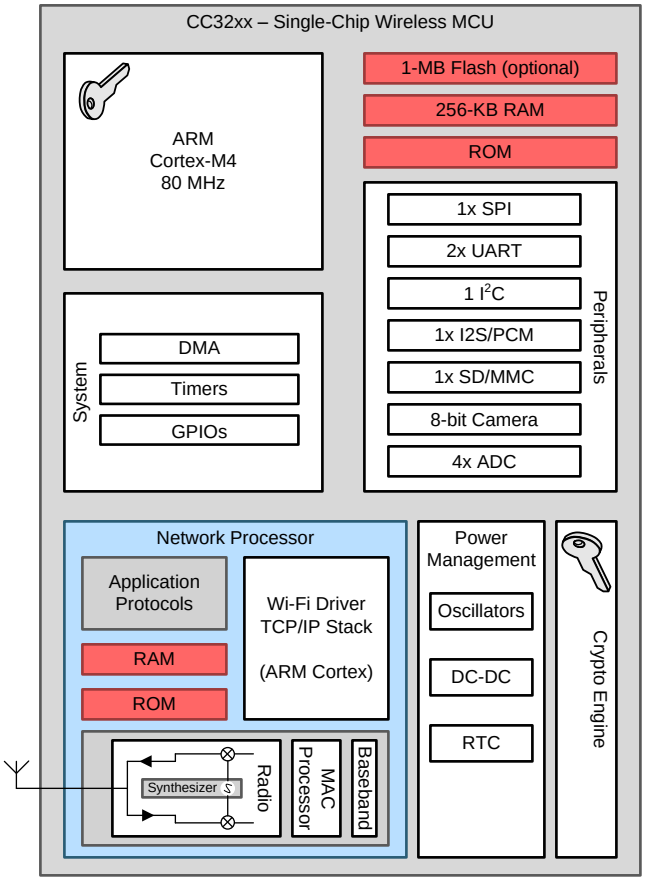


图 1-3. CC3220x 硬件概述

图 1-4 显示了 CC3220x 嵌入式软件的概述。

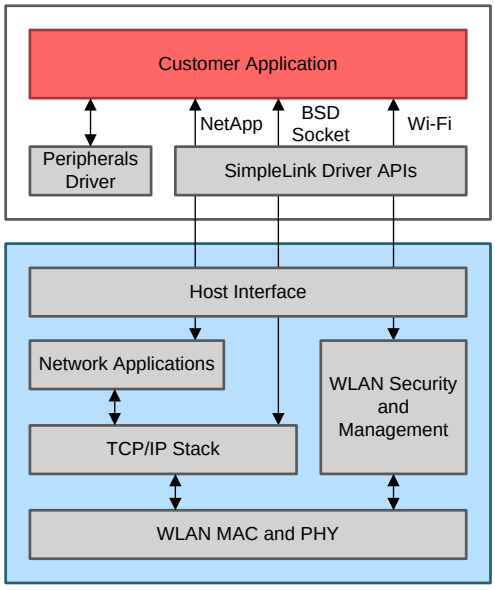


图 **1-4. CC3220x** 嵌入式软件概述

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from August 2, 2017 to December 7, 2018	Page
• Changed ID for MIC (Japan) in Table 6-6	67
• Changed figures in Section 6.11	70
• Changed MARKING for MIC ID: modular MIC grant ID in Table 6-7	71

3 Device Comparison

Table 3-1 shows the features supported across different CC3x20 modules.

Table 3-1. Device Features Comparison

FEATURE	DEVICE				
	CC3120MOD	**CC3220MODS**	**CC3220MODSF**	**CC3220MODAS**	**CC3220MODASF**
On-board chip	CC3120	CC3220S	CC3220SF	CC3220S	CC3220SF
On-board ANT	No	No	No	Yes	Yes
sFlash	32-Mbit	32-Mbit	32-Mbit	32-Mbit	32-Mbit
Regulatory certifications	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC
Wi-Fi Alliance® Certification	Yes	Yes	Yes	Yes	Yes
Input voltage	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V
Package	17.5 mm × 20.5 mm QFM	17.5 mm × 20.5 mm QFM	17.5 mm × 20.5 mm QFM	25.0 mm × 20.5 mm QFM	25.0 mm × 20.5 mm QFM
Operating temperature range	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C
Classification	Wi-Fi Network Processor	Wireless Microcontroller	Wireless Microcontroller	Wireless Microcontroller	Wireless Microcontroller
Standard	802.11 b/g/n	802.11 b/g/n	802.11 b/g/n	802.11 b/g/n	802.11 b/g/n
Frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
TCP/IP Stack	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6
Sockets	16	16	16	16	16
Integrated MCU	–	Arm® Cortex®-M4 at 80 MHz	Arm® Cortex®-M4 at 80 MHz	Arm® Cortex®-M4 at 80 MHz	Arm® Cortex®-M4 at 80 MHz
ON-CHIP APPLICATION MEMORY					
RAM	–	256KB	256KB	256KB	256KB
Flash	–	–	1MB	–	1MB
PERIPHERALS AND INTERFACES					
Universal Asynchronous Receiver/Transmitter (UART)	1	2	2	2	2
Serial Port Interface (SPI)	1	1	1	1	1
Multichannel Audio Serial Port (McASP)- I2S or PCM	–	2-ch	2-ch	2-ch	2-ch
Inter-Integrated Circuit (I^2C)	–	1	1	1	1
Analog-to-digital converter (ADC)	–	4-ch, 12-bit	4-ch, 12-bit	4-ch, 12-bit	4-ch, 12-bit
Parallel interface (8-bit PI)	–	1	1	1	1
General-purpose timers	–	4	4	4	4
Multimedia card (MMC / SD)	–	1	1	1	1

Table 3-1. Device Features Comparison (continued)

FEATURE	DEVICE				
	CC3120MOD	CC3220MODS	CC3220MODSF	CC3220MODAS	CC3220MODASF
SECURITY FEATURES					
Wi-Fi level of security	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)
Secure sockets (SSL v3 or TLS 1.0 /1.1/ 1.2)	6	6	6	6	6
Additional networking security	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key
Hardware acceleration	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines
Secure boot	–	Yes	Yes	Yes	Yes
Enhanced Application Level Security	–	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming

3.1 Related Products

For information about other devices in this family of products or related products see the links below.

The SimpleLink™ MCU Portfolio offers a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi®, Bluetooth® low energy, Sub-1GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications.

Companion Products Review products that are frequently purchased or used in conjunction with this product.

SimpleLink™ Wi-Fi® Family The SimpleLink Wi-Fi Family offers several Internet-on-a chip solutions, which address the need of battery operated, security enabled products. Texas instruments offers a single chip wireless microcontroller and a wireless network processor which can be paired with any MCU, to allow developers to design new wi-fi products, or upgrade existing products with wi-fi capabilities.

BoosterPack™ Plug-In Modules BoosterPack™ Plug-In Modules extend the functionality of TI LaunchPad Kit. Application specific BoosterPack Plug in modules allow you to explore a broad range of applications, including capacitive touch, wireless sensing, LED Lighting control, and more. Stack multiple BoosterPack modules onto a single LaunchPad kit to further enhance the functionality of your design.

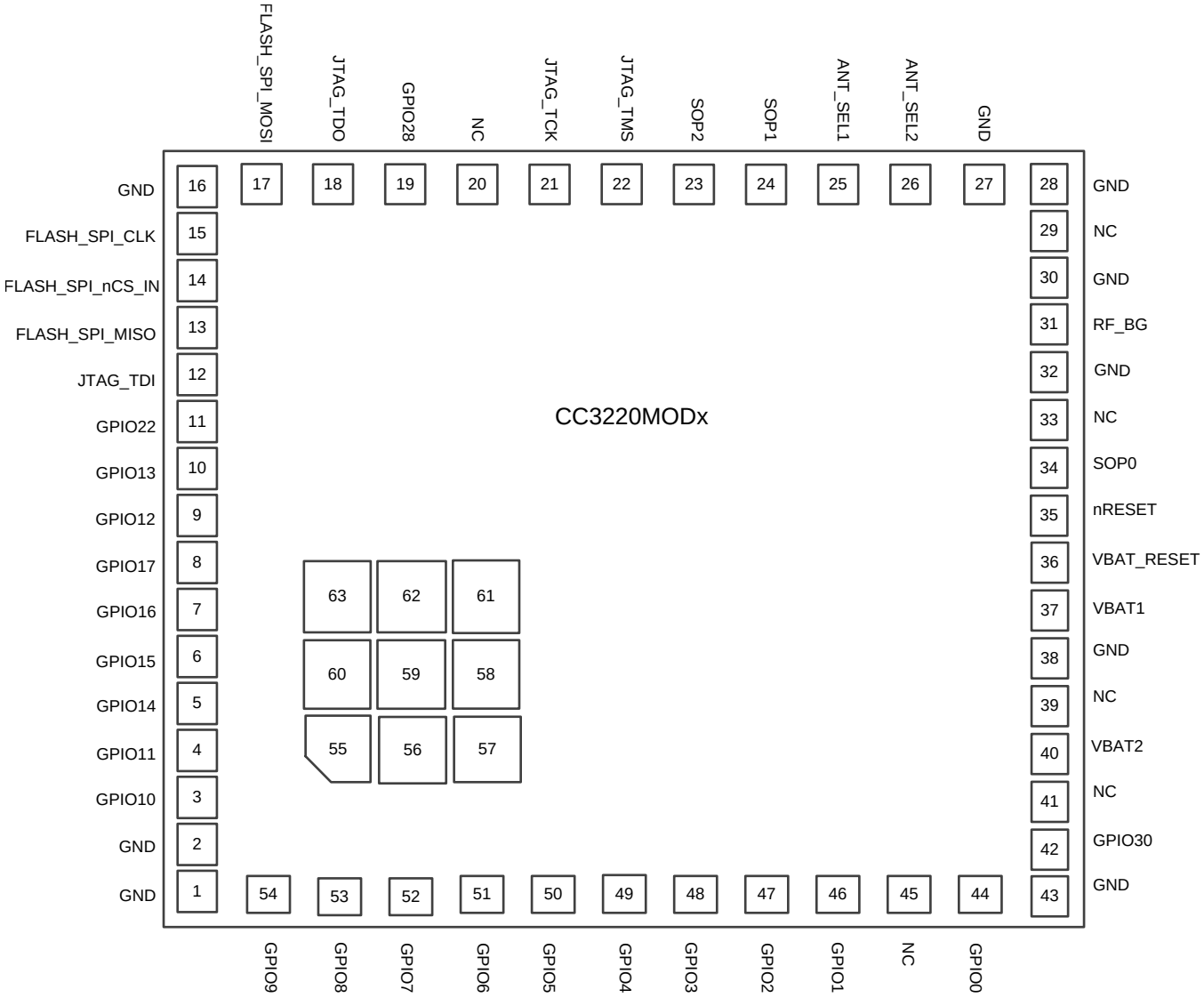
Reference Designs for CC3200 and CC3220 Modules TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

SimpleLink™ Wi-Fi® CC3220 SDK The SimpleLink Wi-Fi CC3220 SDK contains drivers for the CC3220 programmable MCU, sample applications, and documentation required to start development with CC3220 solutions.

4 Terminal Configuration and Functions

4.1 CC3220MODx and CC3220MODAx Pin Diagram

Figure 4-1 shows the pin diagram for the CC3220MODx module.



NOTE: Figure 4-1 shows the approximate location of pins on the module. For the actual mechanical diagram, see 节 10.

Figure 4-1. CC3220MODx Pin Diagram Bottom View

Figure 4-2 shows the pin diagram for the CC3220MODAx module.

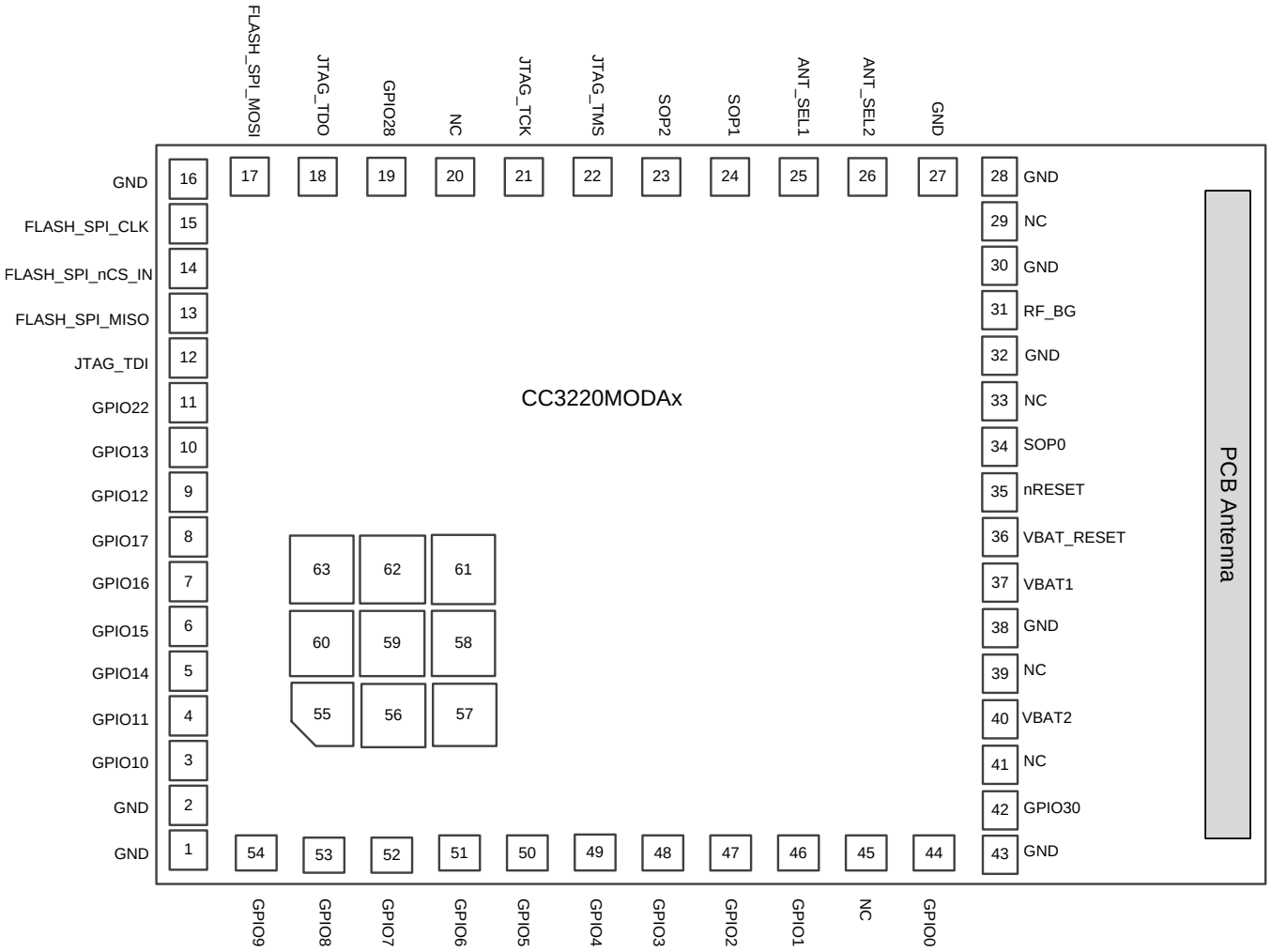


Figure 4-2. CC3220MODAx Pin Diagram Bottom View

4.2 Pin Attributes

Table 4-1 lists the pin descriptions of the CC3220MODx and CC3220MODAx module.

Table 4-1. Module Pin Attributes

MODULE PIN		TYPE[1]	CC3220 DEVICE PIN NO.	MODULE PIN DESCRIPTION
NO.	NAME			
1	GND	–	–	Ground
2	GND	–	–	Ground
3	GPIO10	I/O	1	GPIO[2]
4	GPIO11	I/O	2	GPIO[2]
5	GPIO14	I/O	5	GPIO[2]
6	GPIO15	I/O	6	GPIO[2]
7	GPIO16	I/O	7	GPIO[2]
8	GPIO17	I/O	8	GPIO[2]
9	GPIO12	I/O	3	GPIO[2]
10	GPIO13	I/O	4	GPIO[2]
11	GPIO22	I/O	15	GPIO[2]
12	JTAG_TDI	I/O	16	JTAG TDI input. Leave unconnected if not used on product[2]
13	FLASH_SPI_MISO	I	–	External Serial Flash Programming: SPI data in
14	FLASH_SPI_nCS_IN	I	–	External Serial Flash Programming: SPI chip select (active low)
15	FLASH_SPI_CLK	I	–	External Serial Flash Programming: SPI clock
16	GND	–	–	Ground
17	FLASH_SPI_MOSI	O	–	External Serial Flash Programming: SPI data out
18	JTAG_TDO	I/O	17	JTAG TDO output. Leave unconnected if not used on product[1]
19	GPIO28	I/O	18	GPIO[2]
21	JTAG_TCK	I/O	19	JTAG TCK input. Leave unconnected if not used on product.[2]
22	JTAG_TMS	I/O	20	JTAG TMS input. Leave unconnected if not used on product.[2]
23	SOP2	–	21	See Section 6.9.1 for SOP[2:0] configuration modes.
24	SOP1	–	34	See Section 6.9.1 for SOP[2:0] configuration modes.
25	ANT_SEL1	I/O	29	Antenna selection control[2]
26	ANT_SEL2	I/O	30	Antenna selection control[2]
27	GND	–	–	Ground
28	GND	–	–	Ground
30	GND	–	–	Ground
31	RF_BG	I/O	31	2.4-GHz RF input/output
32	GND	–	–	Ground
34	SOP0	–	35	See Section 6.9.1 for SOP[2:0] configuration modes.
35	nRESET	I	32	There is an internal, 100 kΩ, pull-up resistor option from the nRESET pin to VBAT_RESET. Note: VBAT_RESET is not connected to VBAT1 or VBAT2 within the module. The following connection schemes are recommended: • Connect nRESET to a switch, external controller, or host, only if nRESET will be in a defined state under all operating conditions. Leave VBAT_RESET unconnected to save power. • If nRESET cannot be in a defined state under all operating conditions, connect VBAT_RESET to the main module power supply (VBAT1 and VBAT2). Due to the internal pull-up resistor a leakage current of 3.3 V / 100 kΩ is expected.
36	VBAT_RESET	–	37	
37	VBAT1	Power	39	Power supply for the module, must be connected to battery (2.3 V to 3.6 V)
38	GND	–	–	Ground

Table 4-1. Module Pin Attributes (continued)

MODULE PIN		TYPE(1)	CC3220 DEVICE PIN NO.	MODULE PIN DESCRIPTION
NO.	NAME			
40	VBAT2	Power	10, 44, 54	Power supply for the module, must be connected to battery (2.3 V to 3.6 V)
42	GPIO30	I/O	53	GPIO(2)
43	GND	–	–	Ground
44	GPIO0	I/O	50	GPIO(2)
46	GPIO1	I/O	55	GPIO(2)
47	GPIO2	I/O	57	GPIO(2)
48	GPIO3	I/O	58	GPIO(2)
49	GPIO4	I/O	59	GPIO(2)
50	GPIO5	I/O	60	GPIO(2)
51	GPIO6	I/O	61	GPIO(2)
52	GPIO7	I/O	62	GPIO(2)
53	GPIO8	I/O	63	GPIO(2)
54	GPIO9	I/O	64	GPIO(2)
55	GND	–	–	Thermal ground
56	GND	–	–	Thermal ground
57	GND	–	–	Thermal ground
58	GND	–	–	Thermal ground
59	GND	–	–	Thermal ground
60	GND	–	–	Thermal ground
61	GND	–	–	Thermal ground
62	GND	–	–	Thermal ground
63	GND	–	–	Thermal ground

(1) I = input; O = output; I/O = bidirectional

(2) For pin multiplexing details, see Table 4-4.

4.3 Connections for Unused Pins

All unused pins must be left as no connect (NC) pins. Table 4-2 and Table 4-3 list the NC pins on the CC3220MODx and CC3220MODAx modules, respectively.

Table 4-2. Connections for Unused Pins

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE	DESCRIPTION
20	NC	WLAN analog	–	Reserved. Do not connect.
29	NC	WLAN analog	–	Reserved. Do not connect.
33	NC	WLAN analog	–	Reserved. Do not connect.
39	NC	WLAN analog	–	Reserved. Do not connect.
41	NC	WLAN analog	–	Reserved. Do not connect.
45	NC	WLAN analog	–	Reserved. Do not connect.

Table 4-3. CC3220MODAx Connections for Unused Pins

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE	DESCRIPTION
20	NC	WLAN analog	–	Reserved. Do not connect.
29	NC	WLAN analog	–	Reserved. Do not connect.
31	NC	WLAN analog	–	Reserved. Do not connect.
33	NC	WLAN analog	–	Reserved. Do not connect.
39	NC	WLAN analog	–	Reserved. Do not connect.
41	NC	WLAN analog	–	Reserved. Do not connect.
45	NC	WLAN analog	–	Reserved. Do not connect.

4.4 Pin Attributes and Pin Multiplexing

The module makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at module reset) and register control.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used. Table 4-4 describes the general pin attributes and presents an overview of pin multiplexing. All pin multiplexing options are configurable using the pin MUX registers. The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. Drive strength is individually configurable for each pin.
- All I/Os support 10-μA pullup and pulldown resistors.
- By default, all I/Os float in the Hibernate state. However, the default state can be changed by SW.
- All digital I/Os are non fail-safe.

NOTE

If an external device drives a positive voltage to the signal pads and the CC3220MODx or CC3220MODAx modules are not powered, DC is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3220MODx or CC3220MODAx modules can occur. To prevent current draw, TI recommends any one of the following conditions:

- All devices interfaced to CC3220MODx and CC3220MODAx modules must be powered from the same power rail as the chip.
- Use level shifters between the device and any external devices fed from other independent rails.
- The nRESET pin of the CC3220MODx and CC3220MODAx modules must be held low until the VBAT supply to the module is driven and stable.
- All GPIO pins default to high impedance unless programmed by the MCU. The bootloader sets the TDI, TDO, TCK, TMS, and Flash_SPI pins to mode 1. All the other pins are left in the Hi-Z state.

Table 4-4. Pin Attributes and Pin Multiplexing

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
1	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
2	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
3	GPIO10	I/O	No	No	No	GPIO_PAD_CONFIG_10 (0x4402 E0C8)	0	GPIO10	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							1	I2C_SCL	I^2C clock	I/O (open drain)	Hi-Z, Pull, Drive		
							3	GT_PWM06	Pulse-width modulated O/P	O	Hi-Z, Pull, Drive		
							7	UART1_TX	UART TX data	O	1		
							6	SDCARD_CLK	SD card clock	O	0		
							12	GT_CCP01	Timer capture port	I	Hi-Z, Pull, Drive		

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
4	GPIO11	I/O	Yes	No	No	GPIO_PAD_CONFIG_11 (0x4402 E0CC)	0	GPIO11	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							1	I2C_SDA	I^2C data	I/O (open drain)	Hi-Z, Pull, Drive		
							3	GT_PWM07	Pulse-width modulated O/P	O	Hi-Z, Pull, Drive		
							4	pXCLK (XVCLK)	Free clock to parallel camera	O	0		
							6	SDCARD_CMD	SD card command line	I/O (open drain)	Hi-Z, Pull, Drive		
							7	UART1_RX	UART RX data	I	Hi-Z, Pull, Drive		
							12	GT_CCP02	Timer capture port	I	Hi-Z, Pull, Drive		
							13	MCAFSX	I2S audio port frame sync	O	Hi-Z, Pull, Drive		
5	GPIO14	I/O	No	No	No	GPIO_PAD_CONFIG_14 (0x4402 E0D8)	0	GPIO14	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							5	I2C_SCL	I^2C clock	I/O (open drain)			
							7	GSPI_CLK	General SPI clock	I/O			
							4	pDATA8 (CAM_D4)	Parallel camera data bit 4	I			
							12	GT_CCP05	Timer capture port	I			

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
6	GPIO15	I/O	No	No	No	GPIO_PAD_CONFIG_15 (0x4402 E0DC)	0	GPIO15	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							5	I2C_SDA	I^2C data	I/O (open drain)			
							7	GSPI_MISO	General SPI MISO	I/O			
							4	pDATA9 (CAM_D5)	Parallel camera data bit 5	I			
							13	GT_CCP06	Timer capture port	I			
							8	SDCARD_DATA0	SD card data	I/O			
7	GPIO16	I/O	No	No	No	GPIO_PAD_CONFIG_16 (0x4402 E0E0)	0	GPIO16	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
											Hi-Z, Pull, Drive		
											Hi-Z, Pull, Drive		
							7	GSPI_MOSI	General SPI MOSI	I/O	Hi-Z, Pull, Drive		
							4	pDATA10 (CAM_D6)	Parallel camera data bit 6	I	Hi-Z, Pull, Drive		
							5	UART1_TX	UART1 TX data	O	1		
							13	GT_CCP07	Timer capture port	I	Hi-Z, Pull, Drive		
							8	SDCARD_CLK	SD card clock	O	Zero		

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
8	GPIO17	I/O	Yes	No	No	GPIO_PAD_CONFIG_17 (0x4402 E0E4)	0	GPIO17	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							5	UART1_RX	UART1 RX data	I			
							7	GSPI_CS	General SPI chip select	I/O			
							4	pDATA11 (CAM_D7)	Parallel camera data bit 7	I			
							8	SDCARD_CMD	SD card command line	I/O			
9	GPIO12	I/O	No	No	No	GPIO_PAD_CONFIG_12 (0x4402 E0D0)	0	GPIO12	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							3	McACLK	I2S audio port clock output	O	Hi-Z, Pull, Drive		
							4	pVS (VSYNC)	Parallel camera vertical sync	I	Hi-Z, Pull, Drive		
							5	I2C_SCL	I^2C clock	I/O (open drain)	Hi-Z, Pull, Drive		
							7	UART0_TX	UART0 TX data	O	1		
							12	GT_CCP03	Timer capture port	I	Hi-Z, Pull, Drive		
10	GPIO13	I/O	Yes	No	No	GPIO_PAD_CONFIG_13 (0x4402 E0D4)	0	GPIO13	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							5	I2C_SDA	I^2C data	I/O (open drain)			
							4	pHS (HSYNC)	Parallel camera horizontal sync	I			
							7	UART0_RX	UART0 RX data	I			
							12	GT_CCP04	Timer capture port	I			

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
11	GPIO22	I/O	No	No	No	GPIO_PAD_CONFIG_22 (0x4402 E0F8)	0	GPIO22	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							7	McAFSX	I2S audio port frame sync	O			
							5	GT_CCP04	Timer capture port	I			
12	JTAG_TDI	I/O	No	No	Muxed with JTAG TDI	GPIO_PAD_CONFIG_23 (0x4402 E0FC)	1	TDI	JTAG TDI. Reset default pinout.	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							0	GPIO23	GPIO	I/O			
							2	UART1_TX	UART1 TX data	O	1		
							9	I2C_SCL	I2C clock	I/O (open drain)	Hi-Z, Pull, Drive		
13	FLASH_SPI_MISO	N/A	N/A	N/A	N/A	N/A	N/A	FLASH_SPI_MISO	Data from SPI serial Flash (fixed default)	N/A	Hi-Z	Hi-Z	Hi-Z
14	FLASH_SPI_nCS_IN	N/A	N/A	N/A	N/A	N/A	N/A	FLASH_SPI_nCS_IN	Chip select to SPI serial Flash (fixed default)	N/A	1	Hi-Z, Pull, Drive	Hi-Z
15	FLASH_SPI_CLK	N/A	N/A	N/A	N/A	N/A	N/A	FLASH_SPI_CLK	Clock to SPI serial Flash (fixed default)	N/A	Hi-Z, Pull, Drive [3]	Hi-Z, Pull, Drive	Hi-Z
16	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
17	FLASH_SPI_MOSI	N/A	N/A	N/A	N/A	N/A	N/A	FLASH_SPI_MOSI	Data to SPI serial Flash (fixed default)	N/A	Hi-Z, Pull, Drive [3]	Hi-Z, Pull, Drive	Hi-Z

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
18	JTAG_TDO	I/O	Yes	No	Muxed with JTAG TDO	GPIO_PAD_CONFIG_24 (0x4402 E100)	1	TDO	JTAG TDO. Reset default pinout.	O	Hi-Z, Pull, Drive	Driven high in SWD; driven low in 4-wire JTAG	Hi-Z
							0	GPIO24	GPIO	I/O			
							5	PWM0	Pulse-width modulated O/P	O			
							2	UART1_RX	UART1 RX data	I			
							9	I2C_SDA	I^2C data	I/O (open drain)			
							4	GT_CCP06	Timer capture port	I			
							6	McAFSX	I2S audio port frame sync	O			
19	GPIO28	I/O	No	No	No	GPIO_PAD_CONFIG_40 (0x4402 E140)	0	GPIO28	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
20	NC	WLAN analog	N/A	N/A	N/A	N/A	N/A	NC	Reserved	N/A	N/A	N/A	N/A
21	JTAG_TCK	I/O	No	No	Muxed with JTAG/ SWD-TCK	GPIO_PAD_CONFIG_28 (0x4402 E110)	1	TCK	JTAG/SWD TCK. Reset default pinout.	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							8	GT_PWM03	Pulse-width modulated O/P	O			
22	JTAG_TMS	I/O	No	No	Muxed with JTAG/ SWD-TMSC	GPIO_PAD_CONFIG_29 (0x4402 E114)	1	TMS	JTAG/SWD TMS. Reset default pinout.	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							0	GPIO29	GPIO				

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
23[4]	SOP2	O only	No	No	No	GPIO_PAD_CONFIG_25 (0x4402 E104)	0	GPIO25	GPIO	O	Hi-Z, Pull, Drive	Driven Low	Hi-Z
							9	GT_PWM02	Pulse-width modulated O/P	O	Hi-Z, Pull, Drive		
							2	McAFSX	I2S audio port frame sync	O	Hi-Z, Pull, Drive		
							See [5]	TCXO_EN	Enable to optional external 40-MHz TCXO	O	0		
							See [6]	SOP2	Sense-on-power 2	I	Hi-Z, Pull, Drive		
24	SOP1	Config sense	N/A	N/A	N/A	N/A	N/A	SOP1	Sense-on-power 1	N/A	N/A	N/A	N/A
25[7]	ANT_SEL1	O only	No	User config not required [8]	No	GPIO_PAD_CONFIG_26 (0x4402 E108)	0	ANTSEL1[3]	Antenna selection control	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
26[7]	ANT_SEL2	O only	No	User config not required [8]	No	GPIO_PAD_CONFIG_27 (0x4402 E10C)	0	ANTSEL2[3]	Antenna selection control	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
27	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
28	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
29	NC	WLAN analog	N/A	N/A	N/A	N/A	N/A	NC	Reserved	N/A	N/A	N/A	N/A
30	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
31	RF_BG	WLAN analog	N/A	N/A	N/A	N/A	N/A	CC3220MODx: RF BG band CC3220MODAx: NC	N/A	N/A	N/A	N/A	N/A
32	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
33	NC	WLAN analog	N/A	N/A	N/A	N/A		NC	Reserved				
34	SOP0	Config sense	N/A	N/A	N/A	N/A	N/A	SOP0	Sense-on-power 0	N/A	N/A	N/A	N/A
35	nRESET	Global reset	N/A	N/A	N/A	N/A	N/A	nRESET	Master chip reset. Active low.	N/A	N/A	N/A	N/A
36	VBAT_ RESET	Global reset	N/A	N/A	N/A	N/A	N/A	VBAT_RESET	VBAT to nRESET pullup resistor	N/A	N/A	N/A	N/A
37	VBAT1	Supply input	N/A	N/A	N/A	N/A	N/A	VBAT1	Analog DC/DC input (connected to chip input supply [VBAT])	N/A	N/A	N/A	N/A
38	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
39	NC	WLAN analog	N/A	N/A	N/A	N/A	N/A	NC	Reserved	N/A	N/A	N/A	N/A
40	VBAT2	Supply input	N/A	N/A	N/A	N/A	N/A	VBAT2	Analog input supply VBAT	N/A	N/A	N/A	N/A
41	NC	WLAN analog	N/A	N/A	N/A	N/A	N/A	NC	Reserved	N/A	N/A	N/A	N/A
42	GPIO30	I/O	No	User config not required [8]	No	GPIO_PAD_ CONFIG_30 (0x4402 E118)	0	GPIO30	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							9	UART0_TX	UART0 TX data	O	1		
							2	McACLK	I2S audio port clock	O	Hi-Z, Pull, Drive		
							3	McAFSX	I2S audio port frame sync	O	Hi-Z, Pull, Drive		
							4	GT_CCP05	Timer capture port	I	Hi-Z, Pull, Drive		
							7	GSPI_MISO	General SPI MISO	I/O	Hi-Z, Pull, Drive		

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
43	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
44	GPIO0	I/O	No	User config not required [8]	No	GPIO_PAD_CONFIG_0 (0x4402 E0A0)	0	GPIO0	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							12	UART0_CTS	UART0 Clear-to-Send input (active low)	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							6	McAXR1	I2S audio port data 1 (RX/TX)	I/O	Hi-Z, Pull, Drive		
							7	GT_CCP00	Timer capture port	I	Hi-Z, Pull, Drive		
							9	GSPI_CS	General SPI chip select	I/O	Hi-Z, Pull, Drive		
							10	UART1_RTS	UART1 Request-to-Send (active low)	O	1		
							3	UART0_RTS	UART0 Request-to-Send (active low)	O	1		
							4	McAXR0	I2S audio port data 0 (RX/TX)	I/O	Hi-Z, Pull, Drive		
45	NC	WLAN analog	N/A	N/A	N/A	N/A	N/A	NC	Reserved	N/A	N/A	N/A	N/A

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
46	GPIO1	I/O	No	No	No	GPIO_PAD_CONFIG_1 (0x4402 E0A4)	0	GPIO1	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							3	UART0_TX	UART0 TX data	O	1		
							4	pCLK (PIXCLK)	Pixel clock from parallel camera sensor	I	Hi-Z, Pull, Drive		
							6	UART1_TX	UART1 TX data	O	1		
							7	GT_CCP01	Timer capture port	I	Hi-Z, Pull, Drive		
47[10]	GPIO2	Analog input (up to 1.8 V)/ digital I/O	Yes	See [9]	No	GPIO_PAD_CONFIG_2 (0x4402 E0A8)	See [5]	ADC_CH0	ADC channel 0 input (1.5-V max)	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							0	GPIO2	GPIO	I/O	Hi-Z, Pull, Drive		
							3	UART0_RX	UART0 RX data	I	Hi-Z, Pull, Drive		
							6	UART1_RX	UART1 RX data	I	Hi-Z, Pull, Drive		
							7	GT_CCP02	Timer capture port	I	Hi-Z, Pull, Drive		
48[10]	GPIO3	Analog input (up to 1.8 V)/ digital I/O	No	See [9]	No	GPIO_PAD_CONFIG_3 (0x4402 E0AC)	See [5]	ADC_CH1	ADC channel 1 input (1.5-V max)	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							0	GPIO3	GPIO	I/O	Hi-Z, Pull, Drive		
							6	UART1_TX	UART1 TX data	O	1		
							4	pDATA7 (CAM_D3)	Parallel camera data bit 3	I	Hi-Z, Pull, Drive		

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
49[10]	GPIO4	Analog input (up to 1.8 V)/ digital I/O	Yes	See [9]	Yes	GPIO_PAD_CONFIG_4 (0x4402 E0B0)	See[5]	ADC_CH2	ADC channel 2 input (1.5-V max)	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							0	GPIO4	GPIO	I/O	Hi-Z, Pull, Drive		
							6	UART1_RX	UART1 RX data	I	Hi-Z, Pull, Drive		
							4	pDATA6 (CAM_D2)	Parallel camera data bit 2	I	Hi-Z, Pull, Drive		
50[10]	GPIO5	Analog input up to 1.5 V	No	See[9]	No	GPIO_PAD_CONFIG_5 (0x4402 E0B4)	See[5]	ADC_CH3	ADC channel 3 input (1.5 V max)	I	i-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							0	GPIO5	GPIO	I/O	Hi-Z, Pull, Drive		
							4	pDATA5 (CAM_D1)	Parallel camera data bit 1	I	Hi-Z, Pull, Drive		
							6	McAXR1	I2S audio port data 1 (RX, TX)	I/O	Hi-Z, Pull, Drive		
							7	GT_CCP05	Timer capture port	I	Hi-Z, Pull, Drive		

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[1]	Hib[2]	nRESET = 0
51	GPIO6	I/O	No	No	No	GPIO_PAD_CONFIG_6 (0x4402 E0B8)	0	GPIO6	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							5	UART0_RTS	UART0 Request-to-Send (active low)	O	1		
							4	pDATA4 (CAM_D0)	Parallel camera data bit 0	I	Hi-Z, Pull, Drive		
							3	UART1_CTS	UART1 Clear to send (active low)	I	Hi-Z, Pull, Drive		
							6	UART0_CTS	UART0 Clear to send (active low)	I	Hi-Z, Pull, Drive		
							7	GT_CCP06	Timer capture port	I	Hi-Z, Pull, Drive		
52	GPIO7	I/O	No	No	No	GPIO_PAD_CONFIG_7 (0x4402 E0BC)	0	GPIO7	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							13	McACLK	I2S audio port clock	O	Hi-Z, Pull, Drive		
							3	UART1_RTS	UART1 Request to send (active low)	O	1		
							10	UART0_RTS	UART0 Request to send (active low)	O	1		
							11	UART0_TX	UART0 TX data	O	1		
53	GPIO8	I/O	No	No	No	GPIO_PAD_CONFIG_8 (0x4402 E0C0)	0	GPIO8	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							6	SDCARD_IRQ	Interrupt from SD card (future support)	I			
							7	McAFSX	I2S audio port frame sync	O			
							12	GT_CCP06	Timer capture port	I			

Table 4-4. Pin Attributes and Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES						FUNCTION					PAD STATES		
Pkg. Pin	Pin Alias	Use	Select as Wakeup Source	Config. Addl. Analog Mux	Muxed With JTAG	Dig. Pin Mux Config. Reg.	Dig. Pin Mux Config. Mode Value	Signal Name	Signal Description	Signal Direction	LPDS(1)	Hib(2)	nRESET = 0
54	GPIO9	I/O	No	No	No	GPIO_PAD_CONFIG_9 (0x4402 E0C4)	0	GPIO9	GPIO	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
							3	GT_PWM05	Pulse-width modulated O/P	O			
							6	SDCARD_DATA0	SD card data	I/O			
							7	McAXR0	I2S audio port data (RX, TX)	I/O			
							12	GT_CCP00	Timer capture port	I			
55	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
56	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
57	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
58	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
59	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
60	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
61	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
62	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A
63	GND	GND	N/A	N/A	N/A	N/A	N/A	GND	GND	N/A	N/A	N/A	N/A

(1) LPDS state: The state of unused I/Os is Hi-Z. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

(2) Hibernate mode: The state of the I/Os is Hi-Z. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

(3) To minimize leakage in some serial Flash vendors during LPDS, TI recommends that the user application always enables internal weak pulldowns on FLASH_SPI_DIN, FLASH_SPI_DOUT, and FLASH_SPI_CLK pins.

(4) Pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

(5) For details on proper use, see *Drive Strength and Reset States for Analog-Digital Multiplexed Pins*.

(6) Pin is one of three that must have a passive pullup or pulldown resistor onboard to configure the chip hardware power-up mode. For this reason, the pin must be output only when used for digital functions.

(7) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3220MODx module between two antennas. These pins must not be used for other functionalities.

(8) Device firmware automatically enables the digital path during ROM boot.

(9) Requires user configuration to enable the analog switch of the ADC channel. (Switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

(10) Pin is shared by the ADC inputs and digital I/O pad cells.

NOTE

The ADC inputs are tolerant up to 1.8 V (see Section 5.14.5.6 for further details on the useable range of the ADC). The digital pads can tolerate up to 3.6 V. Hence, take care to prevent accidental damage to the ADC inputs. TI recommends first disabling the output buffers of the digital I/Os corresponding to the desired ADC channel (that is, converted to Hi-Z state), and thereafter disabling the respective pass switches (S7 [Pin 47], S8 [Pin 48], S9 [Pin 49], and S10 [Pin 50]). For more information, see Section 4.5.

4.5 Drive Strength and Reset States for Analog-Digital Multiplexed Pins

Table 4-5 describes the use, drive strength, and default state of analog- and digital-multiplexed pins at first-time power up and reset (nRESET pulled low).

Table 4-5. Drive Strength and Reset States for Analog-Digital Multiplexed Pins

PIN	BOARD LEVEL CONFIGURATION AND USE	DEFAULT STATE AT FIRST POWER UP OR FORCED RESET	STATE AFTER CONFIGURATION OF ANALOG SWITCHES (ACTIVE, LPDS, and HIB POWER MODES)	MAXIMUM EFFECTIVE DRIVE STRENGTH (mA)
25	Connected to the enable pin of the RF switch (ANT_SEL1). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
26	Connected to the enable pin of the RF switch (ANT_SEL2). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
44	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
42	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
47	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
48	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
49	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
50	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4

4.6 Pad State After Application of Power to Chip, but Before Reset Release

When a stable power is applied to the CC3220MODx or CC3220MODAx module for the first time or when supply voltage is restored to the proper value following a prior period with supply voltage below 1.5 V, the level of the digital pads are undefined in the period starting from the release of nRESET and until the DIG_DCDC of the CC3220x chip powers up. This period is less than approximately 10 ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins are required to have a definite value during this pre-reset period, an appropriate pullup or pulldown must be used at the board level. The recommended value of these external pullup or pulldown resistors is 2.7 kΩ.

5 Specifications

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{BAT}	–0.5	3.8	V
Digital I/O	–0.5	V_{BAT} + 0.5	V
RF pin	–0.5	2.1	V
Analog pins	–0.5	2.1	V
Operating temperature (T_A)	–40	85	°C
Storage temperature (T_{stg})	–40	85	°C
Junction temperature (T_j)(3)		120	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Junction temperature is for the CC3220x device that is contained within the module.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	±2000	V
		Charged device model (CDM), per JESD22-C101(2) — All pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	TYP	MAX	UNIT
V_{BAT}	2.3	3.3	3.6	V
Operating temperature	–40	25	85	°C
Ambient thermal slew	–20		20	°C/minute

(1) To ensure WLAN performance, the ripple on the power supply must be less than ±300 mV. The ripple should not cause the supply to fall below the brownout voltage.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(3) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.

5.4 Current Consumption (CC3220MODS and CC3220MODAS)

T_A = 25 °C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		272		mA
				TX power level = 4		190		
			6 OFDM	TX power level = 0		248		
				TX power level = 4		182		
			54 OFDM	TX power level = 0		223		
				TX power level = 4		160		
		RX(3)	1 DSSS			59		
			54 OFDM			59		
	NWP idle connected(4)					15.3		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		269		mA
				TX power level = 4		187		
			6 OFDM	TX power level = 0		245		
				TX power level = 4		179		
			54 OFDM	TX power level = 0		220		
				TX power level = 4		157		
		RX(3)	1 DSSS			56		
			54 OFDM			56		
	NWP idle connected(4)					12.2		
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX(3)	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS(5)					135		µA
	NWP idle connected(4)					710		µA
MCU hibernate	NWP hibernate					5		µA
MCU shutdown	NWP shutdown					1		
Peak calibration current (6)		V_{BAT} = 3.6 V				420		mA
		V_{BAT} = 3.3 V				450		
		V_{BAT}= 2.3 V				620		

(1) TX power level = 0 implies maximum power (see Figure 5-1, Figure 5-2, and Figure 5-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) CC3220MODx and CC3220MODAx are constant, power-source systems. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) The RX current is measured with a 1-Mbps throughput rate.
(4) DTIM = 1
(5) The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3220MODx and CC3220MODAx modules can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.
(6) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC3x20 SimpleLink™ Wi-Fi® and Internet of Things Network Processor Programmer's Guide*.

5.5 Current Consumption (CC3220MODSF and CC3220MODASF)

T_A = 25 °C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		286		mA
				TX power level = 4		202		
			6 OFDM	TX power level = 0		255		
				TX power level = 4		192		
			54 OFDM	TX power level = 0		232		
				TX power level = 4		174		
		RX(3)	1 DSSS			74		
			54 OFDM			74		
	NWP idle connected(4)					25.2		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		282		mA
				TX power level = 4		198		
			6 OFDM	TX power level = 0		251		
				TX power level = 4		188		
			54 OFDM	TX power level = 0		228		
				TX power level = 4		170		
		RX(3)	1 DSSS			70		
			54 OFDM			70		
	NWP idle connected(4)					21.2		
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX(3)	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS(5)					135		µA
	NWP idle connected(4)					710		µA
MCU hibernate	NWP hibernate					5		µA
MCU shutdown	NWP shutdown					1		
Peak calibration current (6)		V_{BAT}= 3.6 V				420		mA
		V_{BAT}= 3.3 V				450		
		V_{BAT}= 2.3 V				620		

(1) TX power level = 0 implies maximum power (see Figure 5-1, Figure 5-2, and Figure 5-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) CC3220MODx and CC3220MODAx are constant, power-source systems. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) The RX current is measured with a 1-Mbps throughput rate.
(4) DTIM = 1
(5) The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3220MODx and CC3220MODAx modules can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.
(6) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC3x20 SimpleLink™ Wi-Fi® and Internet of Things Network Processor Programmer's Guide*.

5.6 TX Power and IBAT Versus TX Power Level Settings

Figure 5-1, Figure 5-2, and Figure 5-3 show TX Power and IBAT versus TX power level settings for the CC3220MODS module at modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively. For the CC3220MODSF module, the IBAT current has an increase of approximately 10 mA to 15 mA depending on the transmitted rate. The TX power level will remain the same.

In Figure 5-1, the area enclosed in the circle represents a significant reduction in current during transition from TX power level 3 to level 4. In the case of lower range requirements (14-dBm output power), TI recommends using TX power level 4 to reduce the current.

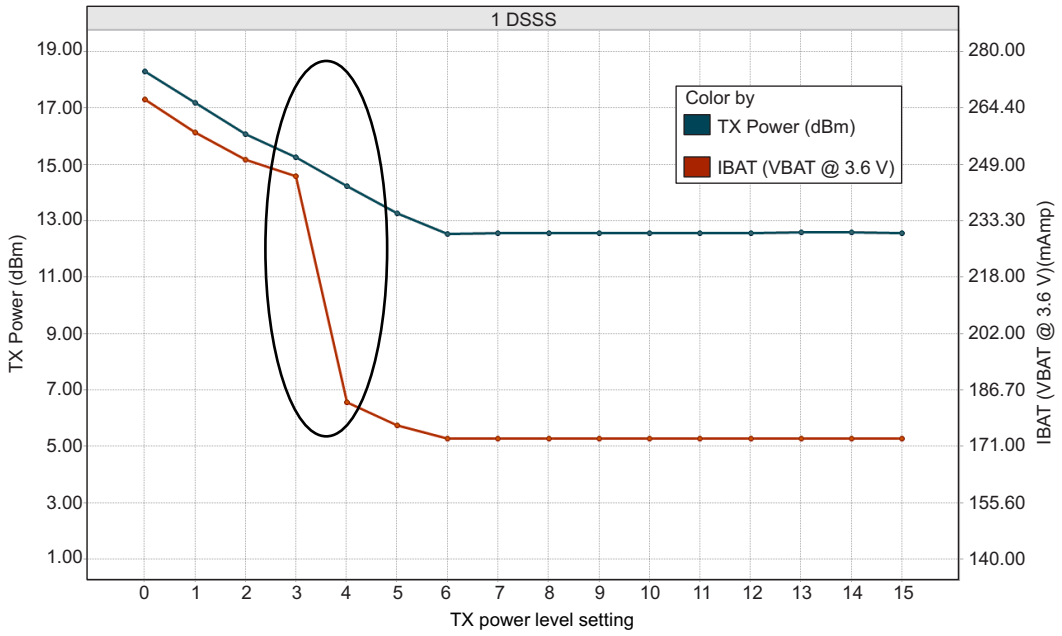


Figure 5-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

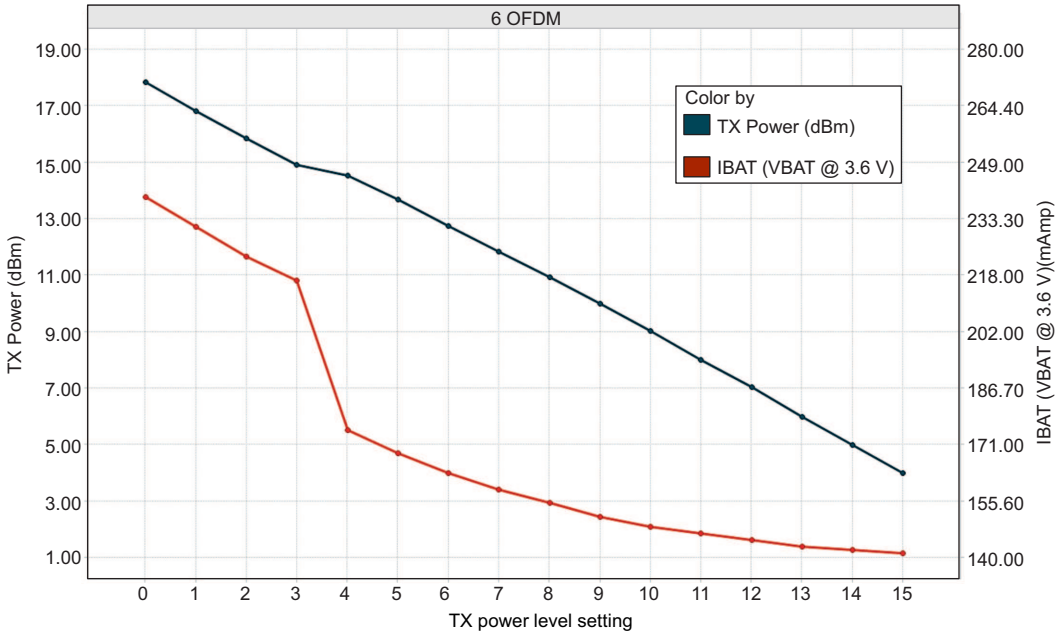


Figure 5-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

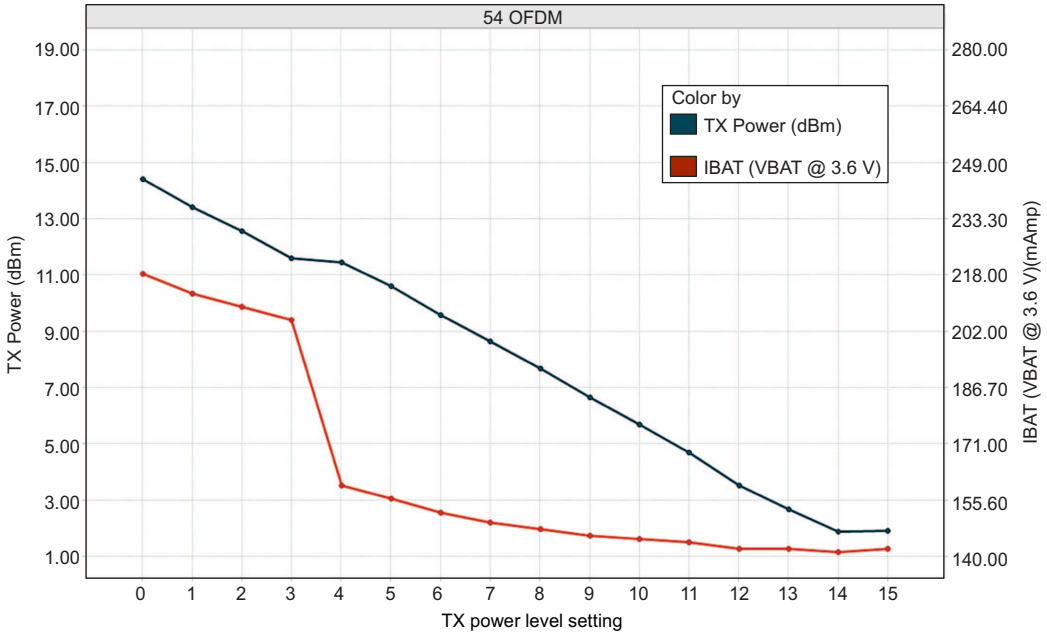


Figure 5-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

5.7 Brownout and Blackout Conditions

The module enters a brownout condition whenever the input voltage dips below $V_{BROWNOUT}$ (see Figure 5-4 and Figure 5-5). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (four contacts for a 2× AA battery), and the wiring and PCB routing resistance.

NOTE

When the module is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

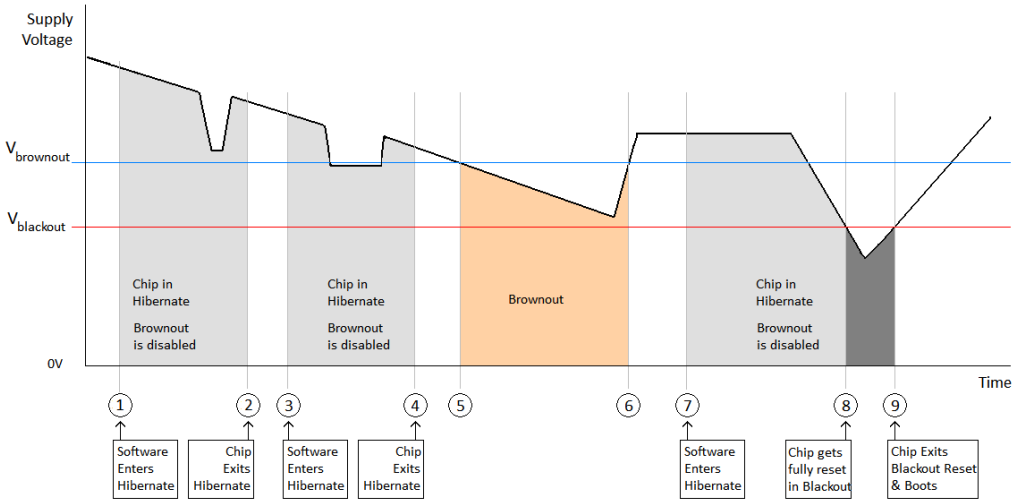


Figure 5-4. Brownout and Blackout Levels (1 of 2)

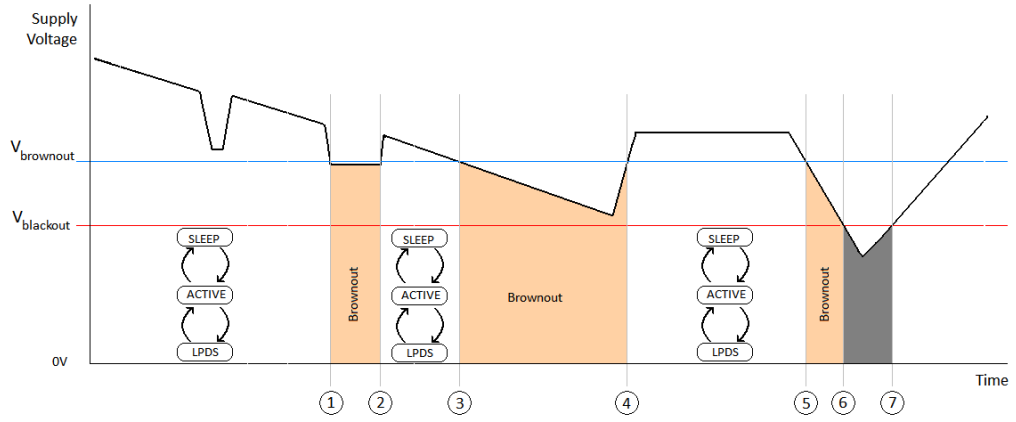


Figure 5-5. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the device shut down within the module except for the Hibernate block (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the module are lost. $V_{brownout}$ = 2.1 V and $V_{blackout}$ = 1.67 V

Table 5-1 lists the brownout and blackout voltage levels.

Table 5-1. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

5.8 Electrical Characteristics

T_A = 25°C, V_{BAT} = 3.3 V

PARAMETER			TEST CONDITIONS(1)	MIN	NOM	MAX	UNIT
GPIO Pins Except 25, 26, 42, and 44 (25°C)							
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
I_{OH}	High-level source current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			
I_{OL}	Low-level sink current	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			
GPIO Pins 25, 26, 42, and 44 (25°C)							
C_{IN}	Pin capacitance				7		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

Electrical Characteristics *(continued)*

T_A = 25°C, V_{BAT} = 3.3 V

PARAMETER			TEST CONDITIONS(1)	MIN	NOM	MAX	UNIT
I_{IH}	High-level input current				50		nA
I_{IL}	Low-level input current				50		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.3 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
I_{OH}	High-level source current, V_{OH} = 2.4	2-mA drive		1.5			mA
		4-mA drive		2.5			
		6-mA drive		3.5			
I_{OL}	Low-level sink current	2-mA drive		1.5			mA
		4-mA drive		2.5			
		6-mA drive		3.5			
V_{IL}	nRESET(2)				0.6		V
Pin Internal Pullup and Pulldown (25°C)							
I_{OH}	Pullup current (V_{DD} = 3.0 V)			5		10	µA
I_{OL}	Pulldown current (V_{DD} = 3.0 V)			5			µA

(2) The nRESET pin must be held below 0.6 V for the device to register a reset.

5.9 CC3220MODAx Antenna Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Polarization			Linear		
Peak Gain	2450 MHz			2.5	dBi
Efficiency	2450 MHz		70%		

5.10 WLAN Receiver Characteristics

T_A = 25°C, V_{BAT} = 2.3 V to 3.6 V. Parameters measured at module pin on channel 6 (2437 MHz).

PARAMETER	RATE	MIN	TYP	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g or 11n rates) (10% PER)(1)	1 DSSS		–95.0		dBm
	2 DSSS		–93.0		
	11 CCK		–87.0		
	6 OFDM		–89.5		
	9 OFDM		–89.0		
	18 OFDM		–85.5		
	36 OFDM		–79.5		
	54 OFDM		–73.5		
	MCS7 (mixed mode)		–69.5		
Maximum input level (10% PER)	802.11b		–3.0		dBm
	802.11g		–9.0		

(1) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

5.11 WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.3 V to 3.6 V. Parameters measured at module pin on channel 6 (2437 MHz)(1)(2).

PARAMETER	RATE	MIN	TYP	MAX	UNIT
Max RMS Output Power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		17.0		dBm
	2 DSSS		17.0		
	11 CCK		17.3		
	6 OFDM		16.3		
	9 OFDM		16.3		
	18 OFDM		16		
	36 OFDM		15		
	54 OFDM		13.5		
	MCS7 (mixed mode)		12		
Transmit center frequency accuracy		–20		20	ppm

(1) The edge channels (2412 MHz and 2462 MHz) have reduced TX power to meet FCC emission limits.
(2) Power of 802.11b rates is reduced to meet ETSI requirements.

5.12 Reset Requirement

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	Operation mode level		0.65 × V_{BAT}		V
V_{IL}	Shutdown mode level(1)	0	0.6		V
	Minimum time for nReset low for resetting the module	5			ms
T_r and T_f	Rise and fall times		20		µs

(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

5.13 Thermal Resistance Characteristics for MOB and MON Packages

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\Theta_{JC}$	Junction-to-case	11.4	0.00
$R\Theta_{JB}$	Junction-to-board	8.0	0.00
$R\Theta_{JA}$	Junction-to-free air	18.7	0.00
Psi_{JT}	Junction-to-package top	5.3	0.00
Psi_{JB}	Junction-to-board	7.7	0.00

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.
(3) m/s = meters per second.

5.14 Timing and Switching Characteristics

5.14.1 Power-Up Sequencing

For proper start-up of the CC3220MODx and CC3220MODAx modules, perform the recommended power-up sequencing as follows:

1. Tie V_{BAT1} (pin 37) and V_{BAT2} (pin 40) together on the board.
2. Hold the nRESET pin low while the supplies are ramping up.

Figure 5-6 shows the reset timing diagram for the first-time power-up and reset removal.

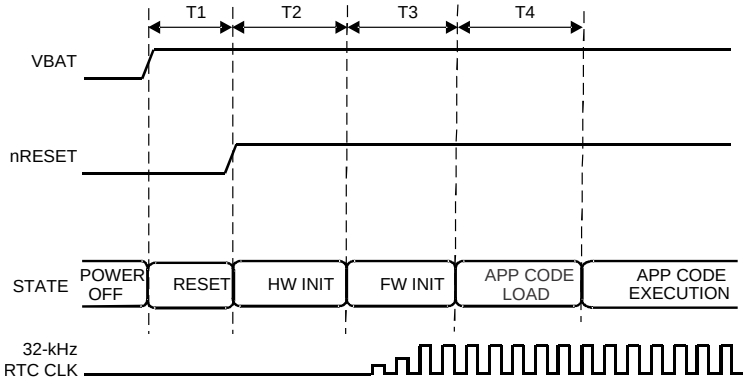


Figure 5-6. First-Time Power-Up and Reset Removal Timing Diagram

Table 5-2 lists the timing requirements for the first-time power-up and reset removal.

Table 5-2. First-Time Power-Up and Reset Removal Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	Internal 32-kHz crystal settling plus firmware initialization time plus radio calibration		1.35		s
T4	App code load time for CC3220MODS and CC3220MODAS	CC3220MODS and CC3220MODAS		Image size (KB) × 1.7 ms		
	App code load time for CC3220MODSF and CC3220MODASF	CC3220MODSF and CC3220MODASF		Image size (KB) × 0.06 ms		

5.14.2 Power-Down Sequencing

For proper power down of the CC3220MODx and CC3220MODAx module, ensure that the nRESET (pin 35) and nHIB (pin 4) pins have remained in a known state for a minimum of 200 ms before removing power from the module.

5.14.3 Device Reset

When a device restart is required, the user may issue a negative pulse to the nRESET pin. The user must ensure the reset is properly applied: A negative reset pulse (on pin 35) of at least 200-mS duration.

5.14.4 Wake Up From Hibernate Timing

Table 5-3 lists the software hibernate timing requirements.

NOTE

The internal 32.768-kHz crystal is kept enabled by default when the module goes to hibernate.

Table 5-3. Software Hibernate Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{HIB_MIN}	Minimum hibernate time		10			ms
$T_{wake\_from\_hib}$ (1)	Hardware wakeup time plus firmware initialization time			50 (2)		ms
T_APP_CODE_LOAD	App code load time for CC3220MODS and CC3220MODAS	CC3220MODS and CC3220MODAS		Image size (KB) × 1.7 ms		
	App code load time for CC3220MODSF and CC3220MODASF	CC3220MODSF and CC3220MODASF		Image size (KB) × 0.06 ms		

(1) $T_{wake\_from\_hib}$ can be 200 ms on rare occasions when calibration is performed. Calibration is performed sparingly, typically when exiting Hibernate and only if temperature has changed by more than 20°C or more than 24 hours have elapsed since a prior calibration.
(2) Wake-up time can extend to 75 ms if a patch is downloaded from the serial Flash.

Figure 5-7 shows the timing diagram for wake up from the hibernate state.

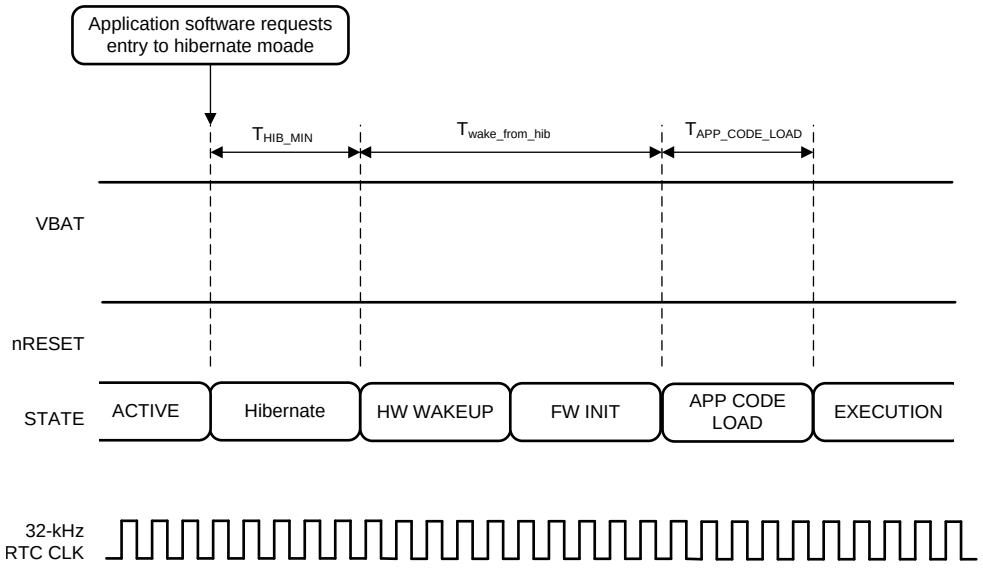


Figure 5-7. Wake Up From Hibernate Timing Diagram

5.14.5 Peripherals Timing

This section describes the peripherals that are supported by the CC3220MODx and CC3220MODAx modules, as follows:

- SPI
- I2S
- GPIOs
- I^2C
- IEEE 1149.1 JTAG
- ADC
- Camera parallel port
- External Flash
- UART
- SD Host
- Timers

5.14.5.1 SPI

5.14.5.1.1 SPI Master

The CC3220MODx and CC3220MODAx microcontroller includes one SPI module, which can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase; a programmable timing control between chip select and external clock generation; and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 5-8 shows the timing diagram for the SPI master.

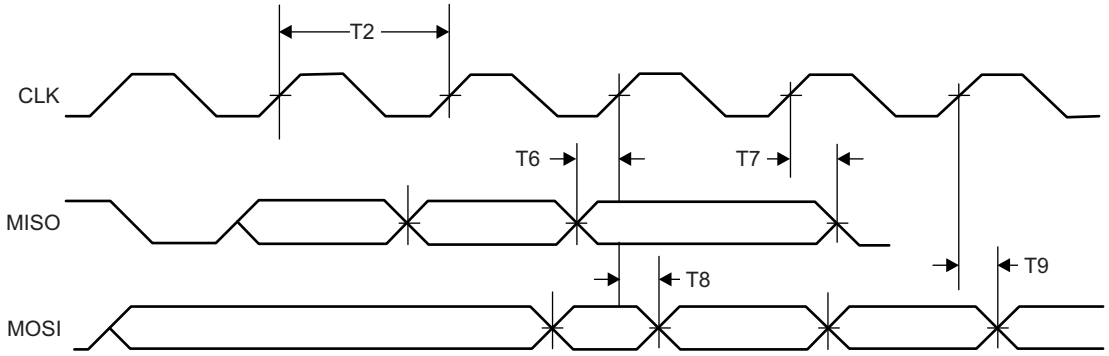


Figure 5-8. SPI Master Timing Diagram

Table 5-4 lists the timing parameters for the SPI master.

Table 5-4. SPI Master Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
	$F^{(1)}$	Clock frequency		20	MHz
T2	$T_{clk}^{(1)}$	Clock period	50		ns
	$D^{(1)}$	Duty cycle	45%	55%	
T6	$t_{IS}^{(1)}$	RX data setup time	1		ns
T7	$t_{IH}^{(1)}$	RX data hold time	2		ns
T8	$t_{OD}^{(1)}$	TX data output delay		8.5	ns
T9	$t_{OH}^{(1)}$	TX data hold time		8	ns

(1) Timing parameter assumes a maximum load of 20 pF.

5.14.5.1.2 SPI Slave

Figure 5-9 shows the timing diagram for the SPI slave.

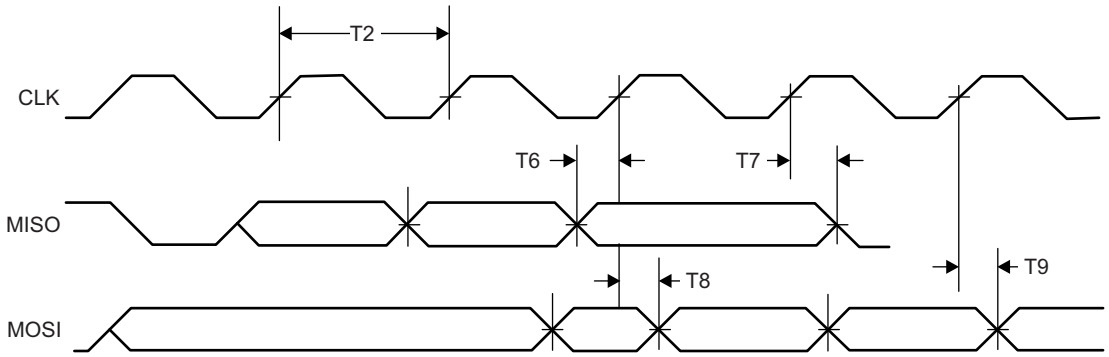


Figure 5-9. SPI Slave Timing Diagram

Table 5-5 lists the timing parameters for the SPI slave.

Table 5-5. SPI Slave Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
	$F^{(1)}$	Clock frequency @ VBAT = 3.3 V		20	MHz
		Clock frequency @ VBAT ≤ 2.3 V		12	
T2	$T_{clk}^{(1)}$	Clock period	50		ns
	$D^{(1)}$	Duty cycle	45%	55%	
T6	$t_{IS}^{(1)}$	RX data setup time	4		ns
T7	$t_{IH}^{(1)}$	RX data hold time	4		ns
T8	$t_{OD}^{(1)}$	TX data output delay		20	ns
T9	$t_{OH}^{(1)}$	TX data hold time		24	ns

(1) Timing parameter assumes a maximum load of 20 pF at 3.3 V.

5.14.5.2 I2S

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

5.14.5.2.1 I2S Transmit Mode

Figure 5-10 shows the timing diagram for the I2S transmit mode.

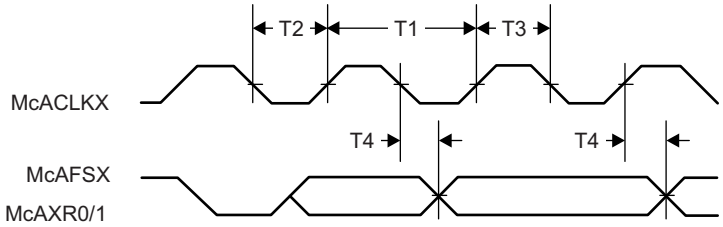


Figure 5-10. I2S Transmit Mode Timing Diagram

Table 5-6 lists the timing parameters for the I2S transmit mode.

Table 5-6. I2S Transmit Mode Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t^{LP} (1)	Clock low period		1/2 fclk	ns
T3	t_{HT} (1)	Clock high period		1/2 fclk	ns
T4	t_{OH} (1)	TX data hold time		22	ns

(1) Timing parameter assumes a maximum load of 20 pF.

5.14.5.2.2 I2S Receive Mode

Figure 5-11 shows the timing diagram for the I2S receive mode.

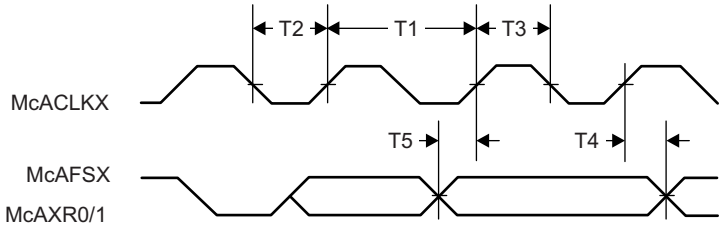


Figure 5-11. I2S Receive Mode Timing Diagram

Table 5-7 lists the timing parameters for the I2S receive mode.

Table 5-7. I2S Receive Mode Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t^{LP} (1)	Clock low period		1/2 f_{clk}	ns
T3	t_{HT} (1)	Clock high period		1/2 f_{clk}	ns
T4	t_{OH} (1)	RX data hold time		0	ns
T5	t_{OS} (1)	RX data setup time		15	ns

(1) Timing parameter assumes a maximum load of 20 pF.

5.14.5.3 GPIOs

All digital pins of the module can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 µA), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Figure 5-12 shows the GPIO timing diagram.

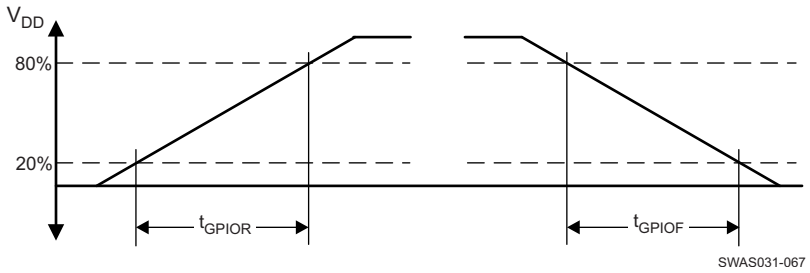


Figure 5-12. GPIO Timing Diagram

Table 5-8 lists the GPIO output transition times for V_{BAT} = 2.3 V.

Table 5-8. GPIO Output Transition Times (V_{BAT} = 2.3 V)(1)(2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r			T_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2	2MA_EN=1 4MA_EN=0	11.7	13.9	16.3	11.5	13.9	16.7	ns
4	2MA_EN=0 4MA_EN=1	13.7	15.6	18.0	9.9	11.6	13.6	ns
6	2MA_EN=1 4MA_EN=1	5.5	6.4	7.4	3.8	4.7	5.8	ns

(1) V_{BAT} = 2.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins other than the multiplexed analog-digital pins 25, 26, 42, and 44.

Table 5-9 lists the GPIO output transition times for V_{BAT} = 3.3 V.

Table 5-9. GPIO Output Transition Times (V_{BAT} = 3.3 V)(1)(2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r			T_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2	2MA_EN=1 4MA_EN=0	8.0	9.3	10.7	8.2	9.5	11.0	ns
4	2MA_EN=0 4MA_EN=1	6.6	7.1	7.6	4.7	5.2	5.8	ns
6	2MA_EN=1 4MA_EN=1	3.2	3.5	3.7	2.3	2.6	2.9	ns

(1) V_{BAT} = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins except the multiplexed analog-digital pins 29, 30, 45, 50, 52 and 53.

5.14.5.3.1 GPIO Input Transition Time Parameters

Table 5-10 lists the input transition time parameters.

Table 5-10. GPIO Input Transition Time Parameters

		MIN	MAX	UNIT
t_r	Input transition time (t_r, t_f), 10% to 90%	1	3	ns
t_f		1	3	ns

5.14.5.4 I²C

The CC3220MODx and CC3220MODAx MCUs include one I2C module operating with standard (100 kbps) or fast (400 kbps) transmission speeds.

Figure 5-13 shows the I²C timing diagram.

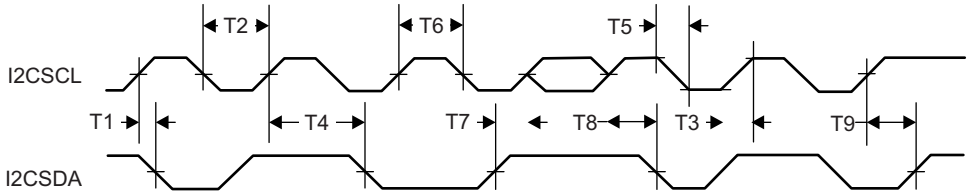


Figure 5-13. I²C Timing Diagram

Table 5-11 lists the I²C timing parameters.

Table 5-11. I²C Timing Parameters(1)

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T2	t_{LP}	Clock low period	See (2)		System clock
T3	t_{SRT}	SCL/SDA rise time		See (3)	ns
T4	t_{DH}	Data hold time	NA		
T5	t_{SFT}	SCL/SDA fall time	3		ns
T6	t_{HT}	Clock high time	See (2)		System clock
T7	t_{DS}	Data setup time	tLP/2		System clock
T8	t_{SCSR}	Start condition setup time	36		System clock
T9	t_{SCS}	Stop condition setup time	24		System clock

(1) All timing is with 6-mA drive and 20-pF load.
(2) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
(3) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of external pullup. Rise time depends on the value of the external signal capacitance and external pullup register.

5.14.5.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1,*Test Access Port and Boundary-Scan Architecture*.

Figure 5-14 shows the JTAG timing diagram.

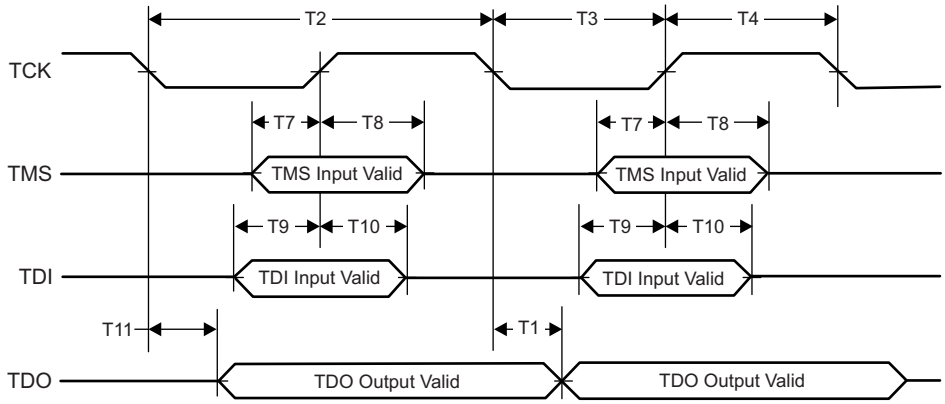


Figure 5-14. JTAG Timing Diagram

Table 5-12 lists the JTAG timing parameters.

Table 5-12. JTAG Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
T1	f_{TCK}	Clock frequency		15	MHz
T2	t_{TCK}	Clock period		$1 / f_{TCK}$	ns
T3	t_{CL}	Clock low period		$t_{TCK} / 2$	ns
T4	t_{CH}	Clock high period		$t_{TCK} / 2$	ns
T7	t_{TMS_SU}	TMS setup time	1		ns
T8	t_{TMS_HO}	TMS hold time	16		ns
T9	t_{TDI_SU}	TDI setup time	1		ns
T10	t_{TDI_HO}	TDI hold time	16		ns
T11	t_{TDO_HO}	TDO hold time		15	ns

5.14.5.6 ADC

Table 5-13 lists the ADC electrical specifications. See *CC32xx ADC Appnote* for further information on using the ADC and for application-specific examples.

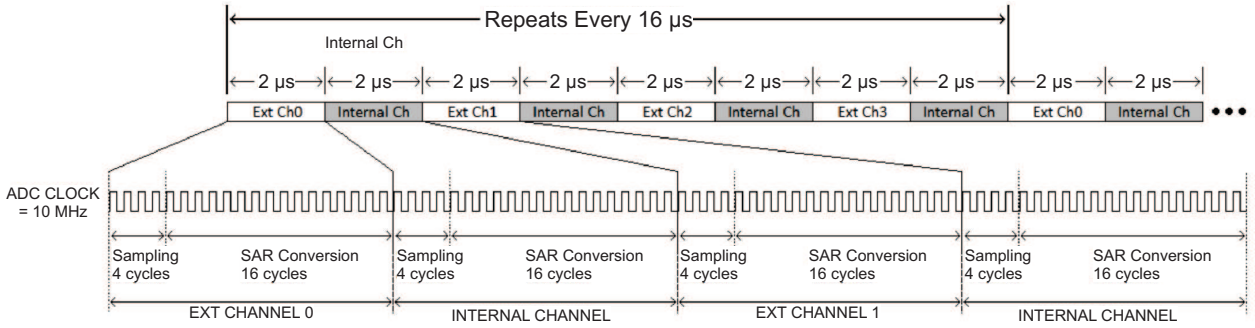


Figure 5-15. ADC Clock Timing Diagram

Figure 5-15 shows the ADC clock timing diagram.

Table 5-13. ADC Electrical Specifications

PARAMETER	DESCRIPTION	TEST CONDITIONS / ASSUMPTIONS	MIN	TYP	MAX	UNIT
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Worst-case deviation from histogram method over full scale (not including first and last three LSB levels)	–2.5		2.5	LSB
DNL	Differential nonlinearity	Worst-case deviation of any step from ideal	–1		4	LSB
Input range			0		1.4	V
Driving source impedance					100	Ω
FCLK	Clock rate	Successive approximation input clock rate		10		MHz
Input capacitance				12		pF
Input impedance		ADC Pin 57		2.15		kΩ
		ADC Pin 58		0.7		
		ADC Pin 59		2.12		
		ADC Pin 60		1.17		
Number of channels				4		
F_{sample}	Sampling rate of each pin			62.5		KSPS
F_input_max	Maximum input signal frequency				31	kHz
SINAD	Signal-to-noise and distortion	Input frequency DC to 300 Hz and 1.4 V_{pp} sine wave input	55	60		dB
I_active	Active supply current	Average for analog-to-digital during conversion without reference current		1.5		mA
I_PD	Power-down supply current for core supply	Total for analog-to-digital when not active (this must be the SoC level test)		1		µA
Absolute offset error		FCLK = 10 MHz		±2		mV
Gain error				±2%		
V_{ref}	ADC reference voltage			1.467		V

5.14.5.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 5-16 shows the timing diagram for the camera parallel port.

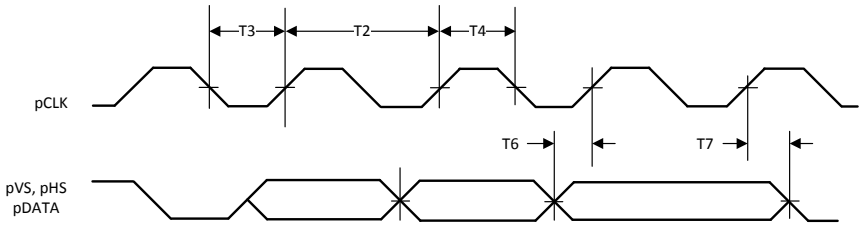


Figure 5-16. Camera Parallel Port Timing Diagram

Table 5-14 lists the timing parameters for the camera parallel port.

Table 5-14. Camera Parallel Port Timing Parameters

ITEM	NAME	DESCRIPTION	MIN	MAX	UNIT
	pCLK	Clock frequency		2	MHz
T2	T_{clk}	Clock period		1/pCLK	ns
T3	t_{LP}	Clock low period		$T_{clk}/2$	ns
T4	t_{HT}	Clock high period		$T_{clk}/2$	ns
T6	t_{IS}	RX data setup time		2	ns
T7	t_{IH}	RX data hold time		2	ns

5.14.5.8 UART

The CC3220MODx and CC3220MODAx modules include two UARTs with the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16-bit × 8-bit TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Generation and detection of line-breaks
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Generation and detection of even, odd, stick, or no-parity bits
  - Generation of 1 or 2 stop-bits
- RTS and CTS hardware flow support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using µDMA:
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

5.14.5.9 External Flash Interface

The CC3220MODx and CC3220MODAx modules include the Macronix™ 32-Mbit serial Flash. The serial Flash can be programmed directly using the external Flash interface (pins 13, 14, 15, and 17). Note that during normal operation, the external Flash interface should remain unconnected.

For timing details of the 32-Mbit Macronix serial Flash, see the MX25R3235F data sheet.

5.14.5.10 SD Host

The CC3220MODx and CC3220MODAx modules provide an interface between a local host (LH), such as an MCU and an SD memory card, and handles SD transactions with minimal LH intervention.

The SD host does the following:

- Provides SD card access in 1-bit mode
- Deals with SD protocol at the transmission level
- Handles data packing
- Adds cyclic redundancy checks (CRC)
- Start and end bit
- Checks for syntactical correctness

The application interface sends every SD command and either polls for the status of the adapter or waits for an interrupt request. The result is then sent back to the application interface in case of exceptions or to warn of end-of-operation. The controller can be configured to generate DMA requests and work with minimum CPU intervention. Given the nature of integration of this peripheral on the CC3220x platform, TI recommends that developers use peripheral library APIs to control and operate the block. This section emphasizes understanding the SD host APIs provided in the peripheral library of the CC3220x Software Development Kit (SDK).

The SD Host features are as follows:

- Full compliance with SD command and response sets, as defined in the SD memory card
  - Specifications, v2.0
  - Includes high-capacity (size >2 GB) cards HC SD
- Flexible architecture, allowing support for new command structure.
- 1-bit transfer mode specifications for SD cards
- Built-in 1024-byte buffer for read or write
  - 512-byte buffer for both transmit and receive
  - Each buffer is 32-bits wide by 128-words deep
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Integrates an internal transceiver that allows a direct connection to the SD card without external transceiver
- Supports configurable busy and response timeout
- Support for a wide range of card clock frequency with odd and even clock ratio
- Maximum frequency supported is 24 MHz

5.14.5.11 Timers

Programmable timers can be used to count or time external events that drive the timer input pins. The general-purpose timer module (GPTM) of the CC3220MODx and CC3220MODAx contains 16- or 32-bit GPTM blocks. Each 16- or 32-bit GPTM block provides two 16-bit timers or counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or they can be concatenated to operate as one 32-bit timer. Timers can also be used to trigger µDMA transfers.

The GPTM contains four 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Counts up or counts down
- Sixteen 16- or 32-bit capture compare pins (CCP)
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using micro direct memory access controller (µDMA):
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt
- Runs from system clock (80 MHz)

6 Detailed Description

6.1 Overview

The CC3220MODx and CC3220MODAx are Wi-Fi® internet-on-a chip modules that consists of an Arm® Cortex®-M4 processor with a rich set of peripherals for diverse application requirements, a Wi-Fi network processor, and power-management subsystems.

6.2 Arm® Cortex®-M4 Processor Core Subsystem

The high-performance Arm® Cortex®-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Cortex®-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm® Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

6.3 Wi-Fi® Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated Arm® MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3220MODx and CC3220MODAx modules support station, AP, and Wi-Fi Direct® modes. The module also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv6, IPv4 TCP/IP stack.

6.3.1 WLAN

The WLAN features are as follows:

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct® client and group owner with CCK and OFDM rates in the 2.4-GHz ISM band, channels 1 to 13.

NOTE

802.11n is supported only in Wi-Fi station, Wi-Fi Direct, and P2P client modes.

- Autocalibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial-Flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x).
- Smart provisioning options deeply integrated within the module providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point using HTTPS
  - SmartConfig Technology: a 1-step, 1-time process to connect a CC3220MODx or CC3220MODAx-enabled module to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.

6.3.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

NOTE

Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, or RAW sockets
- Support of 6 simultaneous SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet

- Built-in network application and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial Flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3220MODx and CC3220MODAx modules provide critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

Table 6-1 describes the NWP features.

Table 6-1. NWP Features

Feature	Description
Wi-Fi standards	802.11b/g/n station 802.11b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi channels	1 to 13
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x)
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 with DAD
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key Secure key storage File system security Software tamper detection Cloning protection Secure boot Validate the integrity and authenticity of the run-time binary during boot Initial secure programming Debug security JTAG and debug
Power management	Enhanced power policy management uses 802.11 power save and deep-sleep power modes
Other	Transceiver Programmable RX filters with event-trigger mechanism

6.4 Security

The SimpleLink™ Wi-Fi® CC3220MODx and CC3220MODAx internet-on-a chip modules enhance the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0/1
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TLS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2

- Secure sockets
  - Protocol versions: SSL v3, TLS 1.0, TLS 1.1, TLS 1.2
  - Powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256
  - Server authentication
  - Client authentication
  - Domain name verification
  - Runtime socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- Trusted root-certificate catalog – Verifies that the CA used by the application is trusted and known secure content delivery
- TI root-of-trust public key – Hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery – Allows encrypted file transfer to the system using asymmetric keys created by the device

Code and Data Security:

- Network passwords and certificates are encrypted and signed.
- Cloning protection – Application and data files are encrypted by a unique key per device.
- Access control – Access to application and data files only by using a token provided in file creation time. If an unauthorized access is detected, a tamper protection lockdown mechanism takes effect.
- Encrypted and Authenticated file system
- Secured boot – Authentication of the application image on every boot
- Code and data encryption – User application and data files are encrypted in sFlash.
- Code and data authentication – User Application and data files are authenticated with a public key certificate.
- Offloaded crypto library for asymmetric keys, including the ability to create key-pair, sign and verify data buffer
- Recovery mechanism

Device Security:

- Separate execution environments – Application processor and network processor run on separate Arm® cores
- Initial secure programming – Allows for keeping the content confidential on the production line
- Debug security
  - JTAG lock
  - Debug ports lock
- True random number generator

Figure 6-1 shows the high-level structure of the CC3220S and CC3220SF devices that are contained within the CC3220MODS and CC3220MODSF modules, respectively. The application image, user data, and network information files (passwords, certificates) are encrypted using a device-specific key.

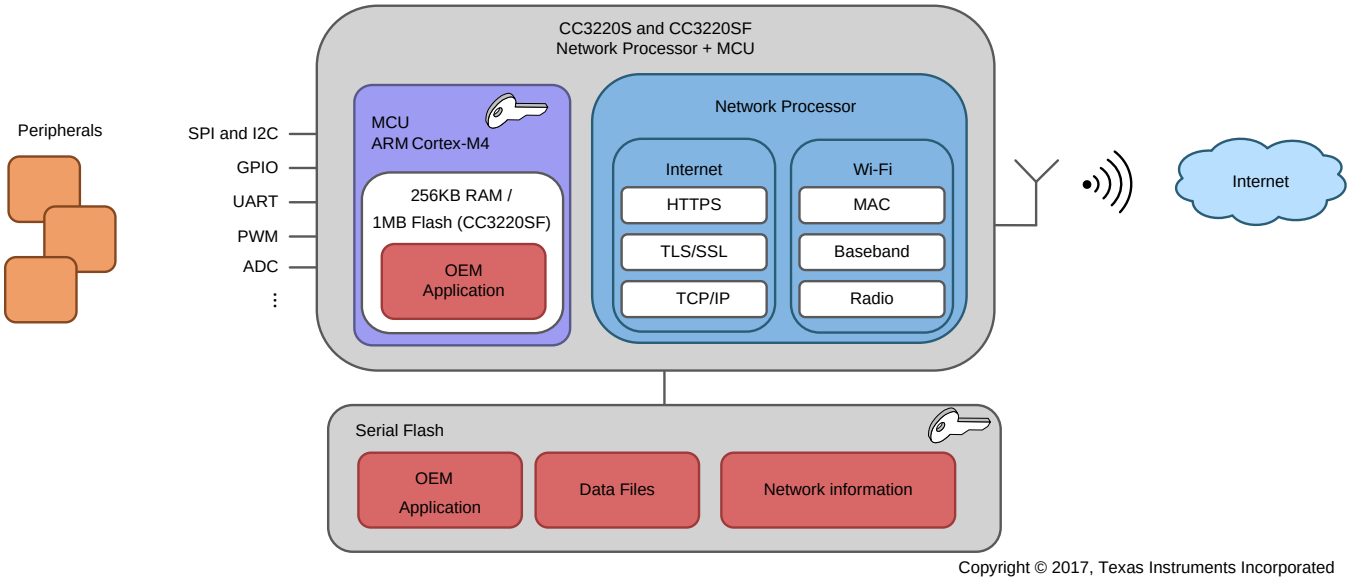


Figure 6-1. CC3220S and CC3220SF High-Level Structure

6.5 Power-Management Subsystem

The CC3220MODx and CC3220MODAx power-management subsystems contain DC/DC converters to accommodate the differing voltage or current requirements of the system.

The CC3220MODx and CC3220MODAx are fully integrated module-based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

6.5.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the module can be directly connected to two AA alkaline batteries. All other voltages required to operate the module are generated internally by the DC/DC converters. This scheme is the most common mode for the module because it supports wide-voltage operation from 2.3 to 3.6 V.

6.6 Low-Power Operating Mode

From a power-management perspective, the CC3220MODx and CC3220MODAx module comprise the following two independent subsystems:

- Arm® Cortex®-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Arm® Cortex®-M4 application processor runs the user application loaded from an external serial Flash, or internal Flash (in CC3220MODSF). The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 6-2.

Table 6-2. User Program Modes

APPLICATION PROCESSOR (MCU) MODE(1)	DESCRIPTION
MCU active mode	MCU executing code at 80-MHz state rate
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3 ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source.
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial Flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO .
MCU shutdown mode	The lowest power mode system-wise. All device logics are off, including the RTC. The wake-up time in this mode is longer than hibernate at about 1.1 s. To enter or exit the shutdown mode, the state of the nRESET line is changed (low to shut down, high to turn on).

(1) Modes are listed in order of power consumption, with highest power modes listed first.

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see Table 6-3).

Table 6-3. Networking Subsystem Modes

NETWORK PROCESSOR MODE	DESCRIPTION
Network active mode (processing layer 3, 2, and 1)	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing not required.
Network active listen mode	Special power optimized active mode for receiving beacon frames (no other frames supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power save operation. The CC3220MODx and CC3220MODAx NWPs automatically goes into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats.
Network LPDS mode	Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake up.
Network disabled	The network is disabled

The operation of the application and network processor ensures that the module remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

6.7 Memory

6.7.1 Internal Memory

The CC3220x device within the CC3220MODx and CC3220MODAx modules includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. The micro direct memory access (μDMA) controller can transfer data to and from SRAM and various peripherals. The CC3220x device ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3220x API list.

6.7.1.1 SRAM

The CC3220MODx and CC3220MODAx family provides 256KB of on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is at offset 0x2000 0000 of the device memory map.

Use the μDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

6.7.1.2 ROM

The internal zero-wait-state ROM of the CC3220MODx and CC3220MODAx module is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial Flash memory is empty). The DriverLib software library of the CC3220MODx and CC3220MODAx controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce Flash memory requirements and free the Flash memory to be used for other purposes.

6.7.1.3 Flash Memory

The CC3220SF device within the CC3220MODSF and CC3220MODASF modules comes with an on-chip Flash memory of 1MB that allows application code to execute in place while freeing SRAM exclusively for read-write data. The Flash memory is used for code and constant data sections and is directly attached to the ICODE/DCODE bus of the Arm® Cortex®-M4 core. A 128-bit-wide instruction prefetch buffer allows maintenance of maximum performance for linear code or loops that fit inside the buffer.

The Flash memory is organized as 2-KB sectors that can be independently erased. Reads and writes can be performed at word (32-bit) level.

6.7.1.4 Memory Map

Table 6-4 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 6-4. Memory Map

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x0000 0000	0x0007 FFFF	On-chip ROM (bootloader + DriverLib)	
0x0100 0000	0x010F FFFF	On-chip Flash (for user application code)	CC3220SF device only
0x2000 0000	0x2003 FFFF	Bit-banded on-chip SRAM	
0x2200 0000	0x23FF FFFF	Bit-band alias of 0x2000 0000 to 0x200F FFFF	
0x4000 0000	0x4000 0FFF	Watchdog timer A0	
0x4000 4000	0x4000 4FFF	GPIO port A0	
0x4000 5000	0x4000 5FFF	GPIO port A1	
0x4000 6000	0x4000 6FFF	GPIO port A2	
0x4000 7000	0x4000 7FFF	GPIO port A3	
0x4000 C000	0x4000 CFFF	UART A0	
0x4000 D000	0x4000 DFFF	UART A1	
0x4002 0000	0x4000 07FF	I^2C A0 (master)	
0x4002 4000	0x4002 4FFF	GPIO group 4	
0x4002 0800	0x4002 0FFF	I^2C A0 (slave)	
0x4003 0000	0x4003 0FFF	General-purpose timer A0	
0x4003 1000	0x4003 1FFF	General-purpose timer A1	
0x4003 2000	0x4003 2FFF	General-purpose timer A2	
0x4003 3000	0x4003 3FFF	General-purpose timer A3	
0x400F7000	0x400F 7FFF	Configuration registers	
0x400F E000	0x400F EFFF	System control	
0x400F F000	0x400F FFFF	µDMA	
0x4200 0000	0x43FF FFFF	Bit band alias of 0x4000 0000 to 0x400F FFFF	
0x4401 0000	0x4401 0FFF	SDIO master	
0x4401 8000	0x4401 8FFF	Camera Interface	
0x4401 C000	0x4401 DFFF	McASP	
0x4402 0000	0x4402 0FFF	SSPI	Used for external serial Flash
0x4402 1000	0x4402 1FFF	GSPI	Used by application processor
0x4402 5000	0x4402 5FFF	MCU reset clock manager	
0x4402 6000	0x4402 6FFF	MCU configuration space	
0x4402 D000	0x4402 DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402 E000	0x4402 EFFF	MCU shared configuration	
0x4402 F000	0x4402 FFFF	Hibernate configuration	
0x4403 0000	0x4403 FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)	
0x4403 0000	0x4403 0FFF	DTHE registers and TCP checksum	
0x4403 5000	0x4403 5FFF	MD5/SHA	
0x4403 7000	0x4403 7FFF	AES	
0x4403 9000	0x4403 9FFF	DES	
0xE000 0000	0xE000 0FFF	Instrumentation trace Macrocell™	
0xE000 1000	0xE000 1FFF	Data watchpoint and trace (DWT)	
0xE000 2000	0xE000 2FFF	Flash patch and breakpoint (FPB)	
0xE000 E000	0xE000 EFFF	NVIC	
0xE004 0000	0xE004 0FFF	Trace port interface unit (TPIU)	
0xE004 1000	0xE004 1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004 2000	0xE00F FFFF	Reserved	

6.8 Restoring Factory Default Configuration

The module has an internal recovery mechanism that rolls back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the sFLASH in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by calling software APIs, or by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial Flash vendor.

6.9 Boot Modes

6.9.1 Boot Mode List

The CC3220MODx and CC3220MODAx module implements a sense-on-power (SoP) scheme to determine the device operation mode.

SoP values are sensed from the module pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and used to determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0). Table 6-5 lists the pull configurations.

All CC3220MODx and CC3220MODAx modules contain internal pull down resistors on the SOP[2:0] lines. The application can use SOP2 for other functions after chip has powered up. However, to avoid spurious SOP values from being sensed at power up, TI strongly recommends using the SOP2 pin only for output signals. The SOP0 and SOP1 pins are multiplexed with the WLAN analog test pins and are not available for other functions.

Table 6-5. CC3220MODx and CC3220MODAx Functional Configurations

NAME	SOP[2]	SOP[1]	SOP[0]	SoP MODE	COMMENT
UARTLOAD	Pullup	Pulldown	Pulldown	LDfrUART	Factory, lab Flash, and SRAM loads through the UART. The device waits indefinitely for the UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.
FUNCTIONAL_2WJ	Pulldown	Pulldown	Pullup	Fn2WJ	Functional development mode. In this mode, 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection.
FUNCTIONAL_4WJ	Pulldown	Pulldown	Pulldown	Fn4WJ	Functional development mode. In this mode, 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection. The default configuration for CC3220MODx and CC3220MODAx modules.
UARTLOAD_FUNCTIONAL_4WJ	Pulldown	Pullup	Pulldown	LDfrUART_FnWJ	Supports Flash and SRAM load through UART and functional mode. The MCU bootloader tries to detect a UART break on UART receive line. If the break signal is present, the device enters the UARTLOAD mode, otherwise, the device enters the functional mode. TDI, TMS, TCK, and TDO are available for debugger connection.
RET_FACTORY_IMAGE	Pulldown	Pullup	Pullup	RetFactDef	When module reset is toggled, the MCU bootloader kickstarts the procedure to restore factory default images.

6.10 Device Certification and Qualification

The CC3220MODx and CC3220MODAx modules from TI are certified for FCC, IC, ETSI/CE, Japan MIC, and SRRC. Moreover, the module is also Wi-Fi CERTIFIED™ with the ability to request a certificate transfer for Wi-Fi alliance members. TI customers that build products based on the CC3220MODx or CC3220MODAx from TI can save in testing cost and time per product family.

Table 6-6. CC3220MODx and CC3200MODAx List of Certifications

Regulatory Body	Specification	ID (IF APPLICABLE)
FCC (USA)	Part 15C + MPE FCC RF Exposure	Z64-CC3220MOD
IC (Canada)	RSS-102 (MPE) and RSS-247 (Wi-Fi)	451I-CC3220MOD
ETSI/CE (Europe)	EN300328 v2.1.1 (2.4GHz Wi-Fi)	—
	EN62311:2008 (MPE)	—
	EN301489-1 v2.1.1 (General EMC)	—
	EN301489-17 v3.1.1 (EMC)	—
	EN60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013	—
MIC (Japan)	Article 49-20 of ORRE	201-170386
SRRC (China)	EN300328 v1.7.1	CC3220MODSM2MOB: 2017DJ2948(M) CC3220MODSF12MOB: 2017DJ2944(M) CC3220MODASM2MON: 2017DJ3095 CC3220MODASF12MON: 2017DJ3121

6.10.1 FCC Certification and Statement

CAUTION

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be co-located or operating with any other antenna or transmitter.

The CC3220MODx and CC3220MODAx modules from TI are certified for the FCC as a single-modular transmitter. The modules are FCC-certified radio modules that carries a modular grant.

You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation of the device.

6.10.2 Industry Canada (IC) Certification and Statement

CAUTION

IC RF Radiation Exposure Statement:

To comply with IC RF exposure requirements, this device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas étre co-localisés ou fonctionnant en conjonction avec une autre antenne ou transmetteur.

The CC3220MODx and CC3220MODAx modules from TI are certified for IC as a single-modular transmitter. The CC3220MODx and CC3220MODAx modules from TI meet IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

This device complies with Industry Canada licence-exempt RSS standards.

Operation is subject to the following two conditions:

- This device may not cause interference.
- This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

- L'appareil ne doit pas produire de brouillage
- L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

6.10.3 ETSI/CE Certification

The CC3220MODx and CC3220MODAx modules from TI are CE certified with certifications to the appropriate EU radio and EMC directives summarized in the Declaration of Conformity and evidenced by the CE mark. The modules are tested against the new Radio Equipment Directive (RE-D). See the full text of the EU Declaration of Conformity for the CC3220MODSM2MOB, CC3220MODSF12MOB, CC3220MODASM2MON, and CC3220MODASF12MON devices.

6.10.4 MIC Certification

The CC3220MODx and CC3220MODAx modules from TI are MIC certified against article 49-20 and the relevant articles of the Ordinance Regulating Radio Equipment.

Operation is subject to the following condition:

- The host system does not contain a wireless wide area network (WWAN) device.

6.10.5 SRRC Certification and Statement

The CC3220MODx modules from TI comply with the rules and regulations of the SRRC for a limited modular approval (LMA).

Operation is subject to the following condition:

- The host system does not contain a WWAN device.

In addition, the host system using an approved LMA radio requires the following:

- New CMIIT ID
- Required radiated related testing only
- The host system's new SRRC certificate contains the CMIIT ID information of the LMA.
- The host system must be affixed with the new MIIT ID (not the CMIIT ID of the LMA) following the SRRC labeling requirements.

NOTE

When an LMA radio is embedded into a host system, it does not mean the host system complies with SRRC rules and regulations. The manufacturer of the host system is responsible for ensuring that the combined system complies with SRRC rules and regulations.

The CC3220MODAx modules from TI comply with the rules and regulations of the SRRC for a full modular approval (FMA).

Operation is subject to the following condition:

- The host system does not contain a WWAN device.

In addition, the host system using an approved FMA radio requires the following:

- The host system does not require a new SRRC certificate for the combined system.
- The host system must be affixed with the MIIT ID of the FMA following the SRRC labeling requirements.

6.11 Module Markings

Figure 6-2 and Figure 6-3 show the markings for the SimpleLink™ CC3220MODx modules.

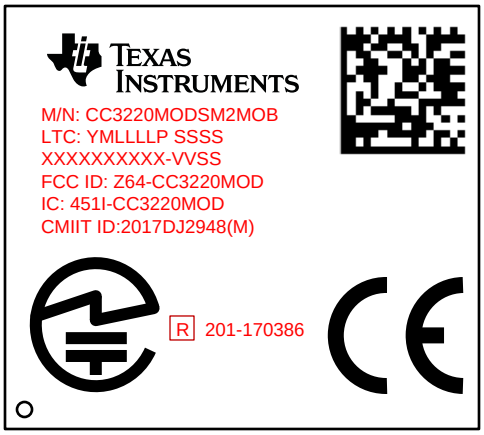


Figure 6-2. CC3220MODS Module Marking

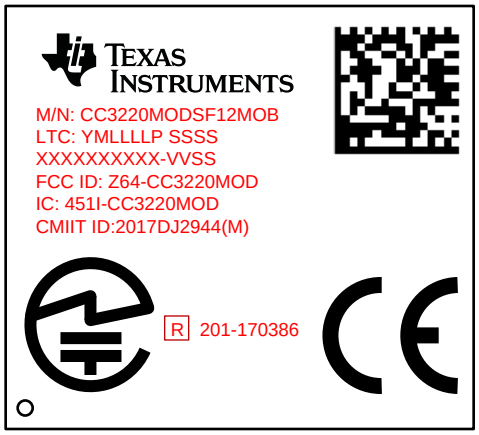


Figure 6-3. CC3220MODSF Module Marking

Figure 6-4 and Figure 6-5 show the markings for the SimpleLink™ CC3220MODAx modules.

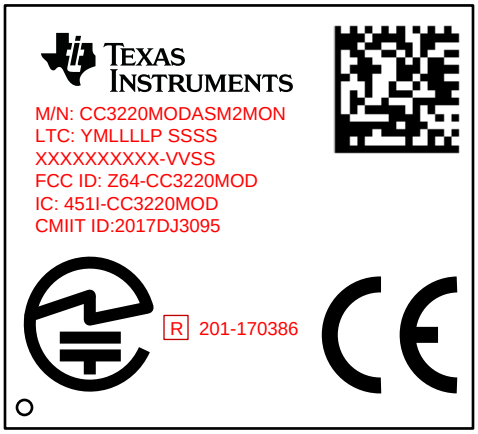


Figure 6-4. CC3220MODAS Module Marking

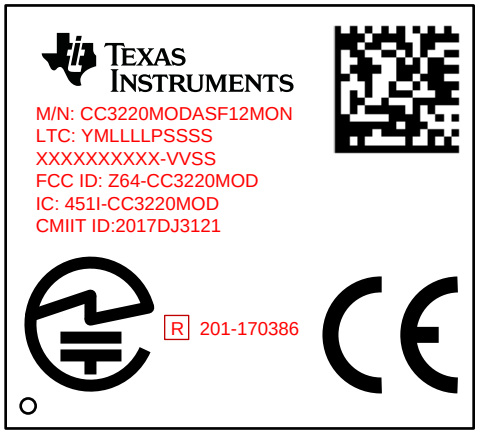


Figure 6-5. CC3220MODASF Module Marking

Table 6-7 lists the CC3220MODx and CC3220MODAx module markings.

Table 6-7. Module Descriptions

MARKING	DESCRIPTION
CC3220MODSM2MOB	Model
CC3220MODSF12MOB	
CC3220MODASM2MON	
CC3220MODASF12MON	
YMLLLLP SSSS	LTC (lot trace code): • Y = Year • M = Month • LLLL = Assembly lot code • P = Reserved for internal use • SSSS = Serial number
XXXXXXXXXX-VVSS	TI internal use only
Z64-CC3220MOD	FCC ID: single modular FCC grant ID
451I-CC3220MOD	IC: single modular IC grant ID
2017DJ2946(M)	CMIIT: limited modular SRRC grant ID
2017DJ2944(M)	CMIIT: limited modular SRRC grant ID
2017DJ3095	CMIIT: full modular SRRC grant ID
2017DJ3121	CMIIT: full modular SRRC grant ID
	MIC compliance mark
R 201-170386	MIC ID: modular MIC grant ID
CE	CE compliance mark

6.12 End Product Labeling

These modules are designed to comply with the FCC single modular FCC grant, FCC ID: Z64-CC3220MOD. The host system using this module must display a visible label indicating the following text:

Contains FCC ID: Z64-CC3220MOD

These modules are designed to comply with the IC single modular FCC grant, IC: 451I-CC3220MOD. The host system using this module must display a visible label indicating the following text:

Contains IC: 451I-CC3220MOD

This module is designed to comply with the JP statement, 201-170386. The host system using this module must display a visible label indicating the following text:

Contains transmitter module with certificate number: 201-170386

6.13 Manual Information to the End User

The OEM integrator must be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual must include all required regulatory information and warnings as shown in this manual.

7 Applications, Implementation, and Layout

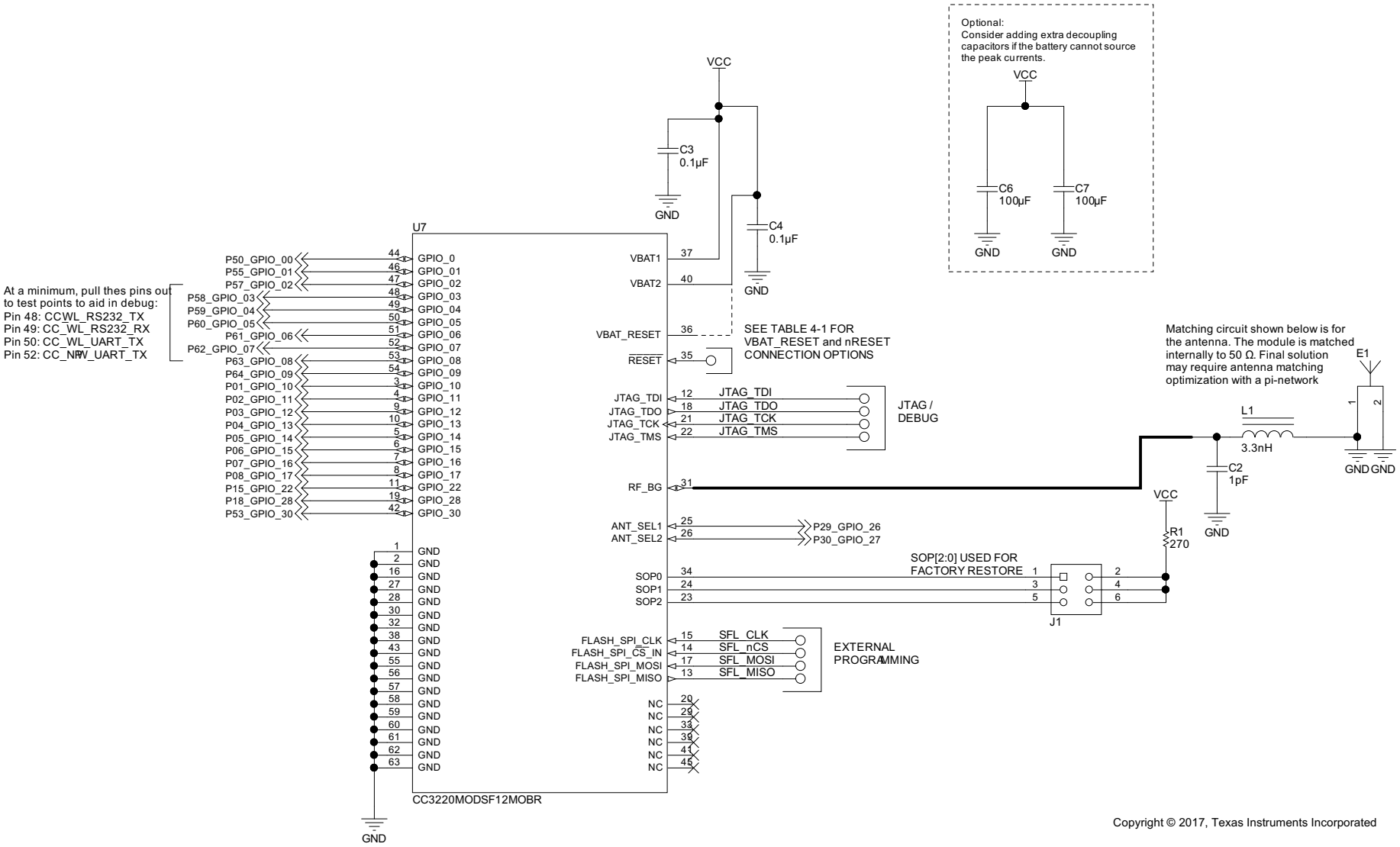
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Typical Application

Figure 7-1 shows the typical application schematic using the CC3220MODx module.

Note that the CC3220MODx and CC3220MODAx modules share the same reference schematic. The difference between the two references is the antenna and its matching circuitry. Pin 31 is not accessible to the designer in the CC3220MODAx module, because it contains an integral antenna. See the full reference schematics for CC3220MODx and CC3220MODAx.



Note: For the board files and BOM, see the LAUNCHXL-CC3220MODSF.

Figure 7-1. CC3220MODx Typical Application Schematic

Table 7-1 provides the bill of materials for a typical application using the CC3220MODx module in Figure 7-1.

Note that the CC3220MODx and CC3220MODAx modules share the same reference BOM. The difference between the two references is the antenna and its matching circuitry. Pin 31 is not accessible to the designer in the CC3220MODAx module, because it contains an integral antenna. See the full reference schematics for CC3220MODx and CC3220MODAx.

Table 7-1. Bill of Materials

QTY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C2 (1)	1 pF	Murata	GRM1555C1H1R0BA01D	Capacitor, ceramic, 1 pF, 50 V, ±10%, C0G/NP0, 0402
3	C3, C4, C5	0.1 µF	Murata	GRM155R61A104KA01D	Capacitor, ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
2	C6, C7	100 µF	Murata	LMK325ABJ107MMHT	Capacitor, ceramic, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
1	E1 (1)	2.45-GHz Ant	Taiyo Yuden	AH316M245001-T	Antenna Bluetooth WLAN ZigBee® WIMAX
1	L1 (1)	3.3 nH	Murata	LQG15HS3N3S02D	Inductor, multilayer, air core, 3.3 nH, 0.3 A, 0.17 Ω, SMD
1	R1	270	Vishay-Dale	CRCW0402270RJNED	RES, 270, 5%, 0.063 W, 0402
1	U1	CC3220MODSF	Texas Instruments	CC3220MODSF12MOBR	SimpleLink™ Wi-Fi® and Internet-of-Things Module Solution, a Single-Chip Wireless MCU, MOB0063A (SIP MODULE-63)

(1) For CC3220MODAx: C2, L1, and E1 are not present.

7.2 Device Connection and Layout Fundamentals

7.2.1 Power Supply Decoupling and Bulk Capacitors

Depending upon routing resistors and battery type, TI recommends adding two 100-µF ceramic capacitors to help provide the peak current drawn by the CC3220MODx and CC3220MODAx modules.

NOTE

The module enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Figure 5-4 and Figure 5-5). This condition must be considered during design of the power supply routing specifically if operating from a battery. For more details on brown-out consideration, see Section 5.7.

7.2.2 Reset

The module features an internal RC circuit to reset the device during power ON. The nRESET pin must be held below 0.6 V for at least 5 ms for the device to successfully reset.

7.2.3 Unused Pins

All unused pins can be left unconnected without any concern to leakage current.

7.3 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3220MODx and CC3220MODAx modules. The integrator of the CC3220MODx and CC3220MODAx modules must comply with the PCB layout recommendations described in the following subsections to minimize the risk with regulatory certifications for the FCC, IC, CE, MIC, and SRRC. Moreover, TI recommends customers follow the guidelines described in this section to achieve similar performance to that obtained with the TI reference design.

7.3.1 General Layout Recommendations

Ensure that the following general layout recommendations are followed:

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.

7.3.2 CC3220MODx RF Layout Recommendations

The RF section of this wireless module gets top priority in terms of layout. It is very important for the RF section to be laid out correctly to ensure optimum performance from the module. A poor layout can cause low-output power, EVM degradation, sensitivity degradation, and mask violations.

Figure 7-2 shows the RF placement and routing of the CC3220MODx module with external antenna.

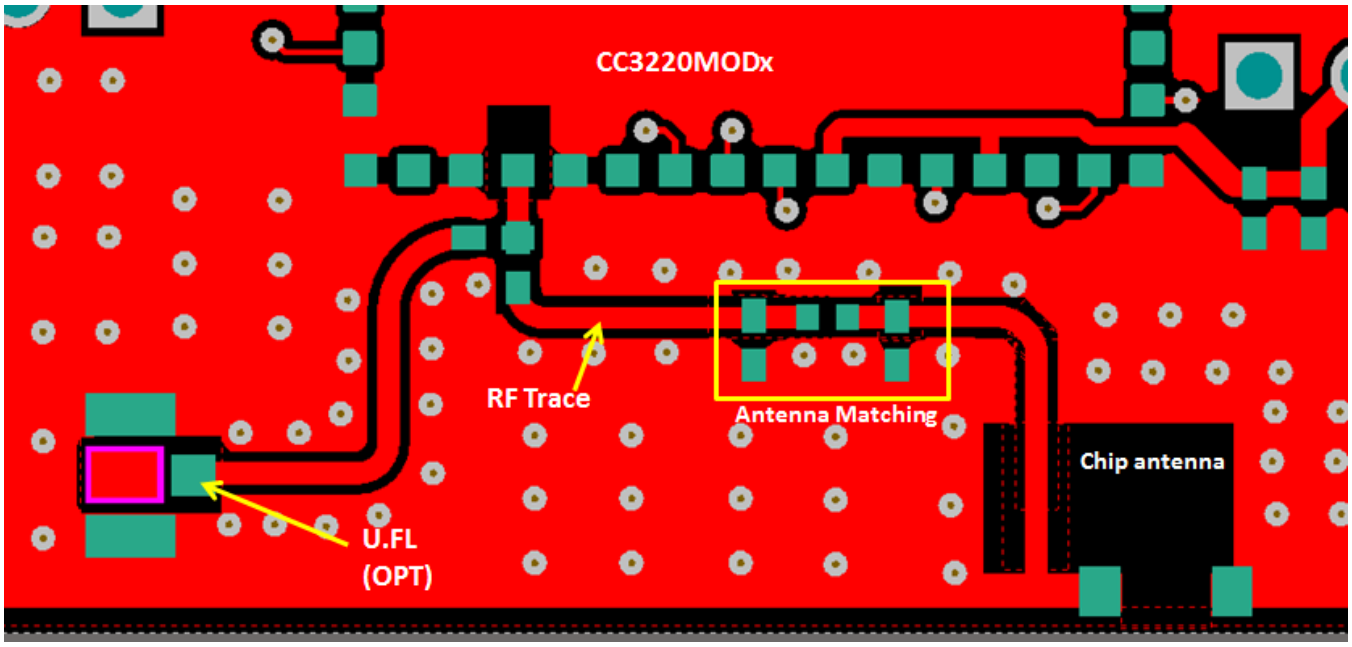


Figure 7-2. RF Section Layout

Follow these RF layout recommendations for the CC320MODx device:

- RF traces must have 50-Ω impedance.
- RF trace bends must be made with gradual curves, and 90° bends must be avoided.
- RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

For optimal RF performance, ensure the copper cut out on the top layer under the RF-BG pin (pin 31) is as shown in Figure 7-3.

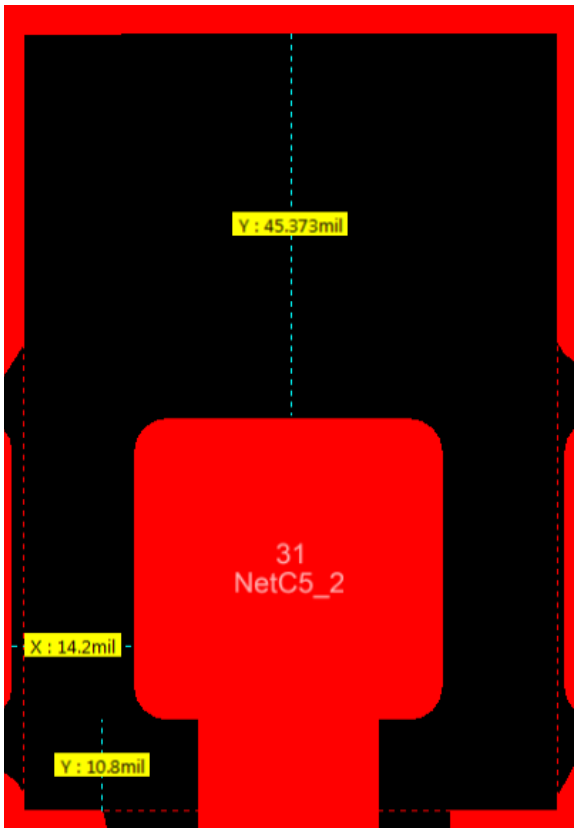


Figure 7-3. Top Layer Copper Pullback on RF Pads

7.3.2.1 Antenna Placement and Routing

The antenna is the element used to convert the guided waves on the PCB traces to the free space electromagnetic radiation. The placement and layout of the antenna are the keys to increased range and data rates. Table 7-2 provides a summary of the recommended antennas to use with the CC3220MODx module.

Table 7-2. Antenna Guidelines

SR NO.	GUIDELINES
1	Place the antenna on an edge or corner of the PCB.
2	Ensure that no signals are routed across the antenna elements on all the layers of the PCB.
3	Most antennas, including the chip antenna used on the LaunchPad™, require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4	Ensure that there is provision to place matching components for the antenna. These must be tuned for best return loss when the complete board is assembled. Any plastics or casing must also be mounted while tuning the antenna because this can impact the impedance.
5	Ensure that the antenna impedance is 50 Ω because the module is rated to work only with a 50-Ω system.
6	In case of printed antenna, ensure that the simulation is performed with the solder mask in consideration.
7	Ensure that the antenna has a near omnidirectional pattern.
8	The feed point of the antenna is required to be grounded. This is only for the antenna type used on the CC3220MODx Launchpad. See the specific antenna data sheets for the recommendations.
9	To use the FCC certification of the module, refer to the CC3120 and CC3220 Radio Certifications wiki page on CC3220MODx Radio certification

Table 7-3 lists the recommended antennas to use with the CC3220MODx module. Other antennas may be available for use with the CC3220MODx modules. See the CC3120 and CC3220 Radio Certifications wiki page.

Table 7-3. Recommended Components

CHOICE	PART NUMBER	MANUFACTURER	NOTES
1	AH316M245001-T	Taiyo Yuden	Can be placed on edge of the PCB and uses much less PCB space

7.3.2.2 Transmission Line Considerations

The RF signal from the module is routed to the antenna using a Coplanar Waveguide with ground (CPW-G) structure. CPW-G structure offers the maximum amount of isolation and the best possible shielding to the RF lines. In addition to the ground on the L1 layer, placing GND vias along the line also provides additional shielding.

Figure 7-4 shows a cross section of the coplanar waveguide with the critical dimensions.

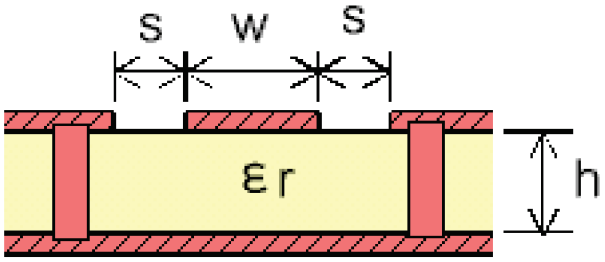


Figure 7-4. Coplanar Waveguide (Cross Section)

Figure 7-5 shows the top view of the coplanar waveguide with GND and via stitching.

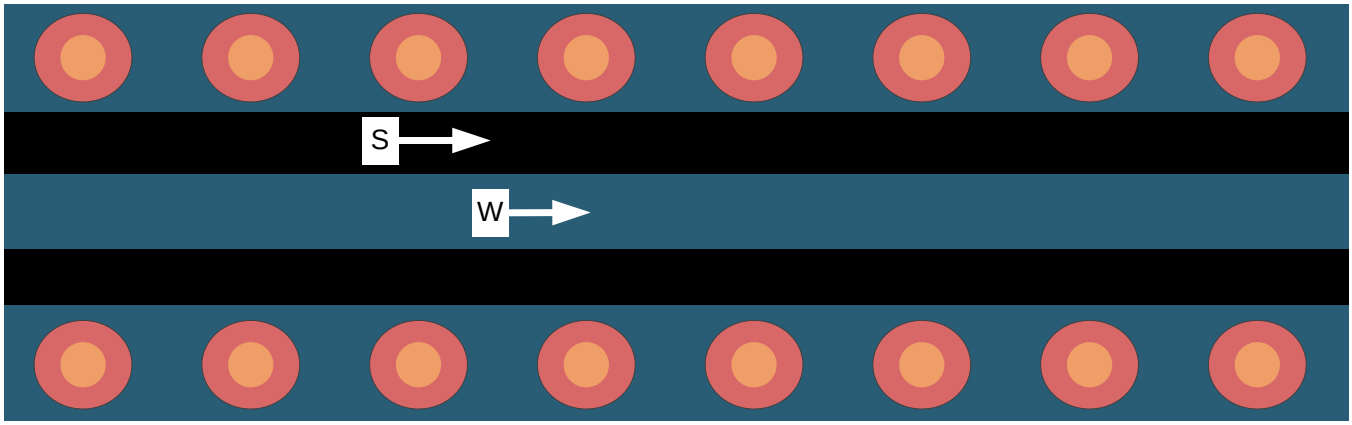


Figure 7-5. CPW With GND and Via Stitching (Top View)

The recommended values for the PCB are provided for 2-layer boards in Table 7-4 and 4-layer boards in Table 7-5.

Table 7-4. Recommended PCB Values for 2-Layer Board (L1 to L2 = 42.1 mils)

PARAMETER	VALUE	UNIT
W	24.5	mils
S	6.5	mils
H	42.1	mils
Er (FR-4 substrate)	4.8	

Table 7-5. Recommended PCB Values for 4-Layer Board (L1 to L2 = 16 mils)

PARAMETER	VALUE	UNITS
W	21	mils
S	10	mils
H	16	mils
Er (FR-4 substrate)	4.5	

7.3.3 CC3220MODAx RF Layout Recommendations

Use the following guidelines to lay out the CC3220MODAx module with integral antenna, as shown in Figure 7-6.

- The module must have an overhang of 1 mm from the PCB edge.
- The module must have a 6-mm clearance on all layers (no copper) to the left and right of the module placement.
- There must be at least one ground-reference plane under the module on the main PCB.
- For additional Layout recommendations, see the *CC3220MODASx SimpleLink™ Wi-Fi® and IoT Solution With MCU LaunchPad™ Hardware User's Guide*.

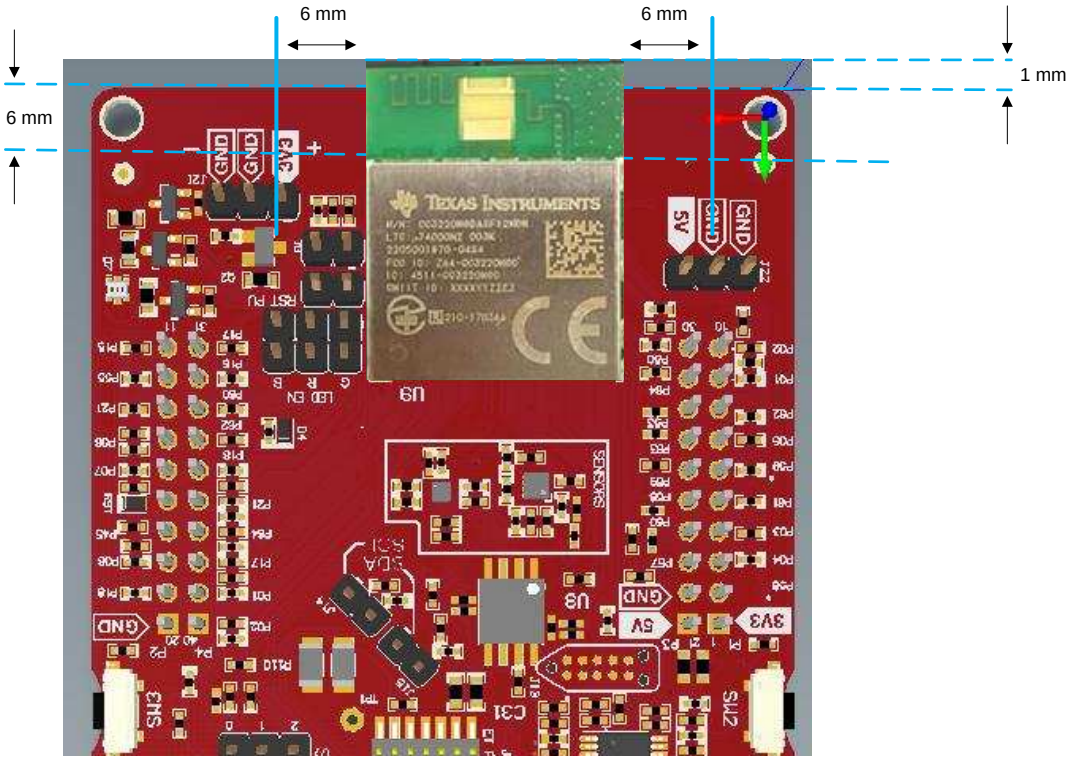


Figure 7-6. CC3220MODAx Layout Guidelines

8 Environmental Requirements and Specifications

8.1 PCB Bending

The PCB bending specification will maintain planeness at a thickness of less than 0.1 mm.

8.2 Handling Environment

8.2.1 Terminals

The product is mounted with motherboard through land-grid array (LGA). To prevent poor soldering, do not make skin contact with the LGA portion.

8.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product to malfunction.

8.3 Storage Condition

8.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product will be 12 months from the date the bag is sealed.

8.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

8.4 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12 to 24 hours

Baking times: 1 time

8.5 Soldering and Reflow Condition

- Heating method: Conventional convection or IR convection
- Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method
- Solder paste composition: Sn/3.0 Ag/0.5 Cu
- Allowable reflow soldering times: 2 times based on the reflow soldering profile (see Figure 8-1)
- Temperature profile: Reflow soldering will be done according to the temperature profile (see Figure 8-1)
- Peak temperature: 245°C

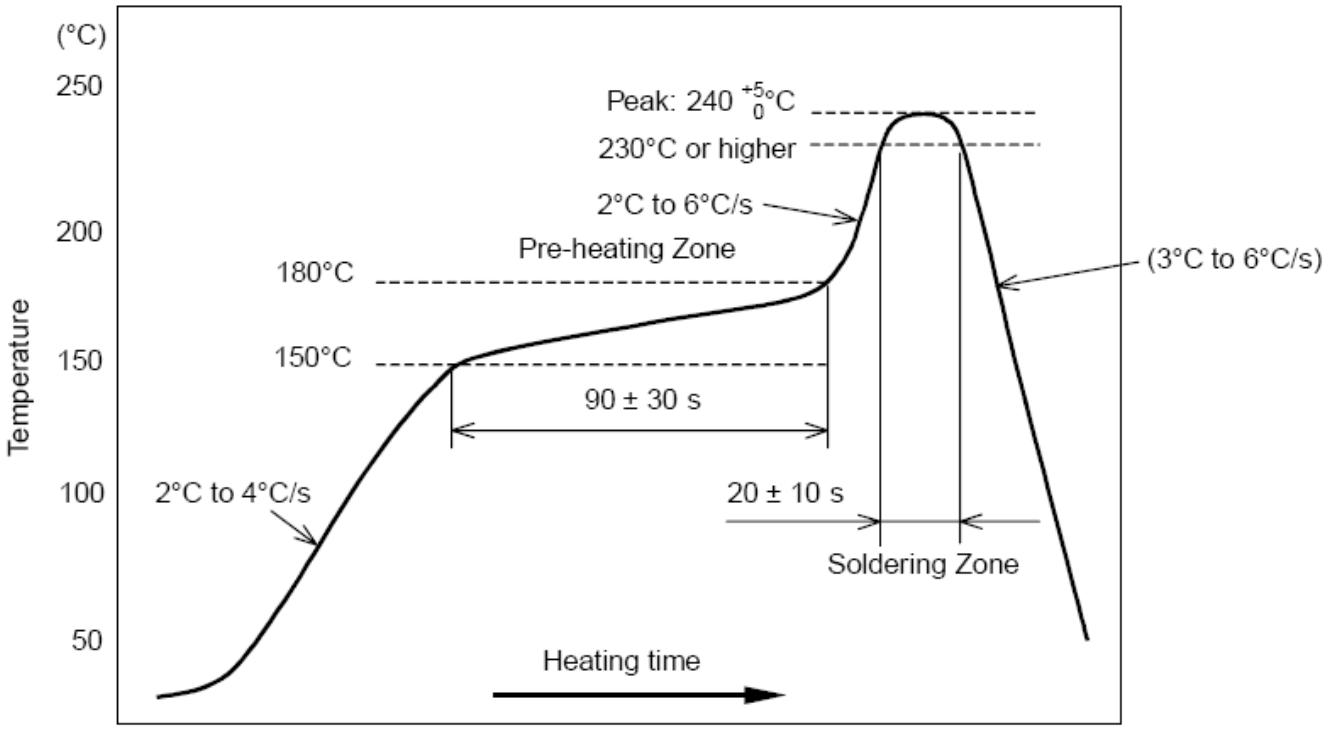


Figure 8-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)

NOTE

TI does not recommend the use of conformal coating or similar material on the SimpleLink™ module. This coating can lead to localized stress on the solder connections inside the module and impact the module reliability. Use caution during the module assembly process to the final PCB to avoid the presence of foreign material inside the module.

器件和文档支持中的

9 器件和文档支持

TI 提供大量的开发工具。此部分列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

9.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.2 开发工具和软件

有关开发工具和软件的最新列表，请访问 CC3220MOD 工具和软件页面。或者，单击页面右上角的“通知我”按钮，随时获取有关 CC3220MOD 的更新消息。

SimpleLink™ Wi-Fi® Starter Pro SimpleLink™ Wi-Fi® Starter Pro 移动应用是一款用于配置 SimpleLink 的新型移动应用。它遵从嵌入式配置库以及在设备端运行的示例。如需使用 SimpleLink Wi-Fi 产品进行 Wi-Fi 配置，TI 建议使用新配置版本。它可以协同反馈和备用选项实现高级 AP 模式配置，确保成功完成处理。客户可以使用嵌入式库和移动库来集成其最终产品。

SimpleLink™ CC3220 Wi-Fi® 软件开发套件 (SDK) SimpleLink™ Wi-Fi® CC3220 SDK 包含适用于 CC3220 可编程 MCU 的驱动程序、30 多个示例 应用，以及使用该解决方案所需的文档。该 SDK 还包含闪存编程器、系统文件和用户文件（证书、网页等）。闪存编程器是一种命令行工具，用于闪存软件、配置网络和软件参数（SSID、接入点通道、网络配置文件等）。此 SDK 可与 TI 的 SimpleLink Wi-Fi CC3220 LaunchPad 配合使用。

SimpleLink™ Wi-Fi® 无线电测试工具 SimpleLink™ Wi-Fi® 无线电测试工具是一款基于 Windows 系统的软件工具，用于在开发和认证过程中对 SimpleLink Wi-Fi CC3120 和 CC3220 设计进行射频评估和测试。通过手动将无线电设置为传输或接收模式，该工具可提供低级无线电测试功能。使用此工具需要熟悉并了解无线电电路理论和无线电测试方法的知识。

适用于 TI 微控制器 (MCU)、Sitara 处理器和 SimpleLink™ 器件的 Uniflash 独立闪存工具 CCS Uniflash 是一个独立工具，用于编程 TI MCU 的片上闪存内存和 Sitara 处理器的板载闪存内存。Uniflash 具有 GUI、命令行和脚本界面。CCS UniFlash 免费提供。

9.3 固件更新

即使未发布 相关计划， TI 也会不时更新此模块相应服务包中的功能。由于更改不断发生，TI 建议用户在其用于生产的模块中使用最新服务包。

若要随时获取更新消息，请使用产品页面右上角的 SDK“通知我”按钮，或者访问 http://www.ti.com.cn/tool/cn/simplelink-cc3220-sdk。

9.4 器件命名规则

为了指出产品开发周期所处的阶段，TI 为 CC3220MODx 和 CC3220MODAx 以及支持工具的部件号分配了前缀（请参阅 图 9-1）。

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的部件号分配了前缀。每个器件具有以下其中一个前缀：X、P 或空（无前缀）（例如 *CC3220MODx 和 CC3220MODAx*）。德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。这些前缀代表了产品开发的发展阶段，即从工程原型 (TMDX) 直到完全合格的生产器件和工具 (TMDS)。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

支持工具开发进化流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品.

TMDS 完全合格的开发支持产品。

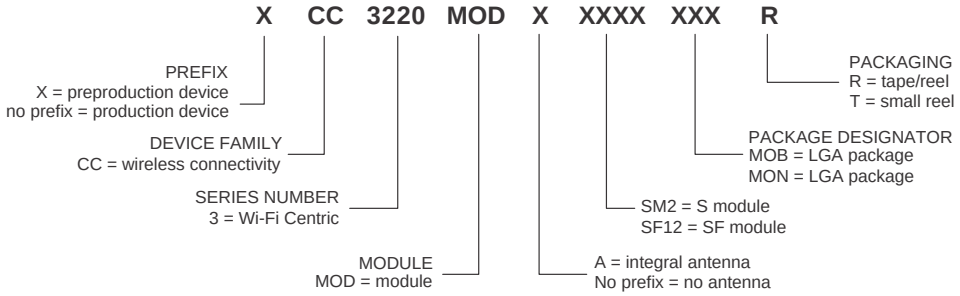


图 **9-1. CC3220MODx 和 CC3220MODAx 模块命名规则**

有关采用 QFM 封装类型的 CC3220MODx 和 CC3220MODAx 器件的可购部件号，请参阅 节 10.2，访问 ti.com.cn，或者联系您的 TI 销售代表。

9.5 文档支持

要接收文档更新通知（包括器件勘误表），请转至 ti.com.cn 上的 CC3220MOD 产品文件夹。单击右上角的 *"通知我"*可每周接收产品信息更改摘要。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

下面列出了介绍处理器、相关外设以及其他配套技术资料的最新文档。

应用报告

将 **TI 的 Wi-Fi® Alliance 认证转移到基于 SimpleLink™ 的产品** 此文档说明了如何使用 Wi-Fi Alliance® (WFA) 衍生认证转移策略将德州仪器 (TI) 已获得的 WFA 认证转移到您开发的系统中。

SimpleLink™ CC3x20 Wi-Fi® Internet-on-a chip™ 解决方案内置安全性 特性 德州仪器 (TI) 的 SimpleLink Wi-Fi CC3120 和 CC3220 Internet-on-a chip™系列器件提供范围广泛的内置安全功能，以便帮助开发人员解决各种安全需求，且不会对主微控制器 (MCU) 造成任何处理负担。本文档介绍这些安全相关的特性，并提供有关在实际系统实现环境中利用每个特性的建议。

在 SimpleLink™ CC3x20 Wi-Fi® 和物联网设备上使用串行闪存 本应用手册分为两个部分。第一部分提供重要指南，以及在选择和嵌入与 CC3120 和 CC3220 (CC3x20) 器件配对的串行闪存时应考虑的最佳实践设计技巧。第二部分介绍文件系统，同时为使用 CC3x20 器件的系统设计人员提供相关指南及注意事项。

SimpleLink™ CC3x20 Wi-Fi® 和物联网无线更新 此文档介绍了适用于德州仪器 (TI) SimpleLink™ Wi-Fi® CC3x20 系列器件的 OTA 库，并说明了如何准备新的云就绪更新供 OTA 库下载。

SimpleLink™ CC3x20 Wi-Fi® Internet-on-a chip™ 解决方案器件配置 本指南介绍了为 SimpleLink Wi-Fi 器件提供连接无线网络所需信息（网络名称、密码等）的配置过程。

SimpleLink™ CC3x20 Wi-Fi® Internet-on-a chip™ 网络子系统电源管理 该应用报告介绍了进行电源管理和延长电池寿命的最佳做法，适用于嵌入式低功耗 Wi-Fi 器件，例如德州仪器 (TI) 提供的 SimpleLink Wi-Fi Internet-on-a chip™ 解决方案。

更多文献

RemoTI 清单
CC3220MODx SimpleLink™ Wi-Fi® 和物联网硬件设计文件
CC3220MODAx SimpleLink™ Wi-Fi® 和物联网硬件设计文件
CC3120、CC3220 SimpleLink™ Wi-Fi® 和物联网设计检查清单

用户指南

Simplelink™ CC3x20 Wi-Fi® 嵌入式编程 此应用手册详细介绍了一些其他选项，这些选项 利用 UniFlash 所提供的全部功能，但没有必要连通电脑。此选项称为嵌入式编程。为实现嵌入式编程，下面将详细介绍通过 UART 实现的引导加载程序协议。

UniFlash SimpleLink™ CC3x20 Wi-Fi® 和 IoC™ 解决方案 ImageCreator 和 Pro 本文档介绍如何安装、操作和使用作为 UniFlash 一部分的 SimpleLink ImageCreator 工具。

SimpleLink™ CC3x20 Wi-Fi® 和物联网网络处理器 本文档为软件 (SW) 程序员提供了使用 SimpleLink Wi-Fi 器件网络子系统所需的全部知识。本指南提供了编写强大、优化型网络主机应用 的基本指南，并介绍了网络子系统的功能。本指南包含一些示例代码屏幕截图，以便使用户明白如何使用主机驱动程序。可在正式的软件开发套件 (SDK) 中找到更全面的代码示例。本指南未提供有关 主机驱动程序 API 的详细说明。

SimpleLink™ CC3220 Wi-Fi® 开箱即用应用 此应用展示了德州仪器 (TI) 的 CC3220 LaunchPad™ 开发套件所提供的开箱即用 (OOB) 体验。

适用于移动应用的 SimpleLink™ CC3x20 Wi-Fi® 配置 本指南介绍了 TI 的 SimpleLink™ Wi-Fi® 配置解决方案，适用于移动 解决方案，具体说明了如何使用用于实现 UI 要求的 Android®™ 和 iOS®构建块、网络和构建移动应用所需的配置 API。

SimpleLink™ CC3220 Wi-Fi® 开箱即用快速入门指南 本快速入门指南详细介绍了德州仪器 (TI) 的 CC3220 LaunchPad™ 开发套件的开箱即用体验。

SimpleLink™ CC3220 Wi-Fi® 和物联网 TRM 本手册介绍了 SimpleLink CC32xx 无线 MCU 的模块和外设。每个 说明 均从一般意义上介绍模块或外设。可能并未对所有器件上的 所有 模块或外设的所有特性和功能都作出介绍。引脚功能、内部信号连接和操作参数都因器件不同而各异。有关这些细节，用户应查阅具体器件的产品说明书。

SimpleLink™ CC3x20 Wi-Fi® 和 Internet-on-a chip™ 解决方案无线电工具 这款无线电工具作为直接接入无线电的控制面板，可用于射频 (RF) 评估及获取认证。本指南介绍如何使该工具在德州仪器 (TI) ™ 评估平台（例如 CC3120 器件的 BoosterPack™ 和 FTDI 仿真板或 CC3220 器件的 LaunchPad™）上无缝运行。

SimpleLink™ CC3220 Wi-Fi® 和物联网解决方案（单芯片无线 MCU） 此指南旨在帮助用户完成运行首个 CC3220、CC3220S、CC3220SF、CC3220MODx 和 CC3220MODAx SimpleLink™ Wi-Fi® 以及物联网解决方案（来自 Texas Instruments™ 的单芯片无线 MCU）示例应用的初始设置和演示。此指南介绍了如何安装软件开发套件 (SDK) 以及开始创建首个应用所需的各种其他工具。

SimpleLink™ CC3220MOD Wi-Fi® LaunchPad™ 开发套件硬件 CC3220MOD SimpleLink LaunchPad™ 开发套件 (LAUNCHCC3220MODASF) 是一个适合基于 Arm®Cortex®-M4 的 MCU 的低成本评估平台。LaunchPad 设计着重强调 CC3220MOD Internet-on-a chip™ 解决方案和 Wi-Fi 功能。CC3220MOD LaunchPad 还 具有 温度和加速计传感器、可编程用户按钮、用于自定义应用的三个 LED 和用于调试的板载仿真。CC3220MOD LaunchPad XL 接口采用可堆栈接头，使其在与众多现有 BoosterPack™ 插件模块附加板上的其他外设对接时可轻松扩展 LaunchPad 的功能，例如图形显示、音频编解码、天线选择、环境传感等。

SimpleLink™ CC3220 Wi-Fi® 和物联网 本文档为用户介绍了 CC3220x 器件的环境设置以及软件开发套件 (SDK) 的一些参考示例。本文档介绍了可用于支持进一步应用开发的平台和框架。

9.5.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

9.6 商标

SimpleLink, Internet-on-a-chip, SmartConfig, 是一款, E2E, BoosterPack, LaunchPad, Internet-on-a chip

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Arm, Cortex, Thumb are registered trademarks of Arm Limited.
低功耗 *Bluetooth* is a registered trademark of Bluetooth SIG, Inc.
Android is a registered trademark of Google, Inc.
Macrocell is a trademark of Kappa Global Inc.
Macronix is a trademark of Macronix International Co..
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Wi-Fi, Wi-Fi Direct are registered trademarks of Wi-Fi Alliance.
ZigBee is a registered trademark of ZigBee Alliance.
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9.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

9.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。

10.1 机械、焊盘和焊锡膏制图

注

说明添加了注释
模块总高度为 2.45mm。

CC3220MODx 模块的重量为 0.00175kg ±3%。

CC3220MODAx 模块的重量为 0.00206kg ±3%

注

1. 所有尺寸的单位皆为 mm。
2. 阻焊层应与焊盘大小相同或比焊盘大 5%
3. 焊锡膏必须采用与所有外设焊盘相同的引脚。对于接地引脚，焊锡膏量应比焊盘少 20%。

10.2 Package Option Addendum

The CC3220MOD is only offered in a 1000-unit reel.

10.2.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL, Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
CC3220MODSM2MOBR	ACTIVE	QFM	MOB	63	1000	Green (RoHS and no Sb/Br)	Ni, AU	3, 250°C	–40 to 85	CC3220MODSM2MOB
CC3220MODSF12MOBR	ACTIVE	QFM	MOB	63	1000	Green (RoHS and no Sb/Br)	Ni, AU	3, 250°C	–40 to 85	CC3220MODSF12MOB
CC3220MODASM2MONR	ACTIVE	QFM	MON	63	800	Green (RoHS and no Sb/Br)	Ni, AU	3, 250°C	–40 to 85	CC3220MODASM2MON
CC3220MODASF12MONR	ACTIVE	QFM	MON	63	800	Green (RoHS and no Sb/Br)	Ni, AU	3, 250°C	–40 to 85	CC3220MODASF12MON

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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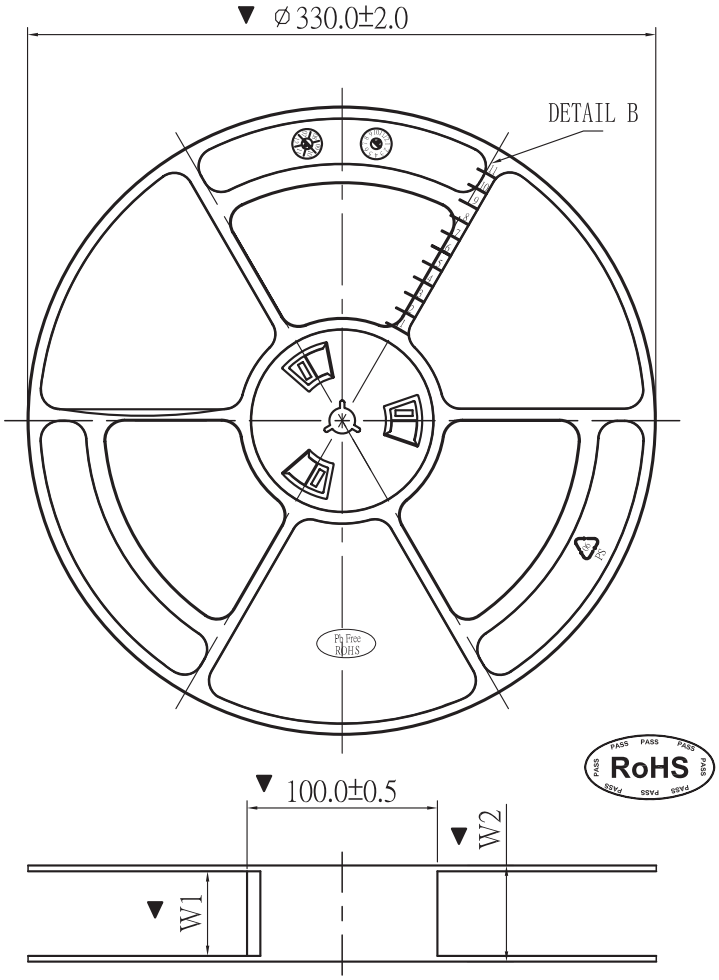
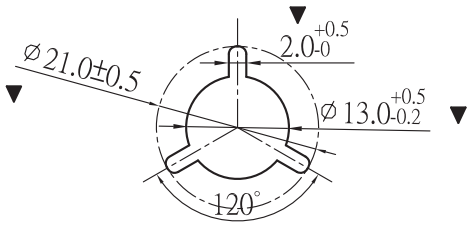
10.2.2 Tape and Reel Information

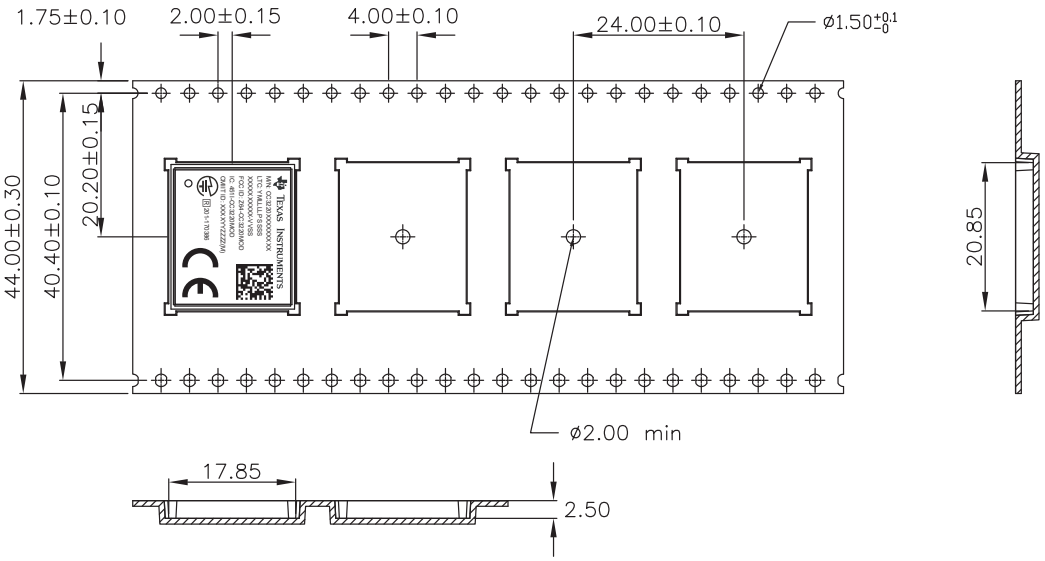




Surface resistance 10^{7}~$10^{11}\Omega/\square$

Spec	Vendor No.	W1	W2(max)
13" 100*12mm	RUR-22-3-X*	$12.4^{+2.0}_{-0}$	18.4
13" 100*16mm	RUR-23-3-X*	$16.4^{+2.0}_{-0}$	22.4
13" 100*24mm	RUR-24-3-X*	$24.4^{+2.0}_{-0}$	30.4
13" 100*32mm	RUR-25-3-X*	$32.4^{+2.0}_{-0}$	38.4
13" 100*44mm	RUR-26-3-X*	$44.4^{+2.0}_{-0}$	50.4
13" 100*56mm	RUR-27-3-X*	$56.4^{+2.0}_{-0}$	62.4
13" 100*72mm	RUR-28-3-X*	$72.4^{+2.0}_{-0}$	79.5
13" 100*88mm	RUR-29-3-X*	$88.4^{+2.0}_{-0}$	96
13" 100*104mm	RUR-2A-3-X*	$104.4^{+2.0}_{-0}$	112

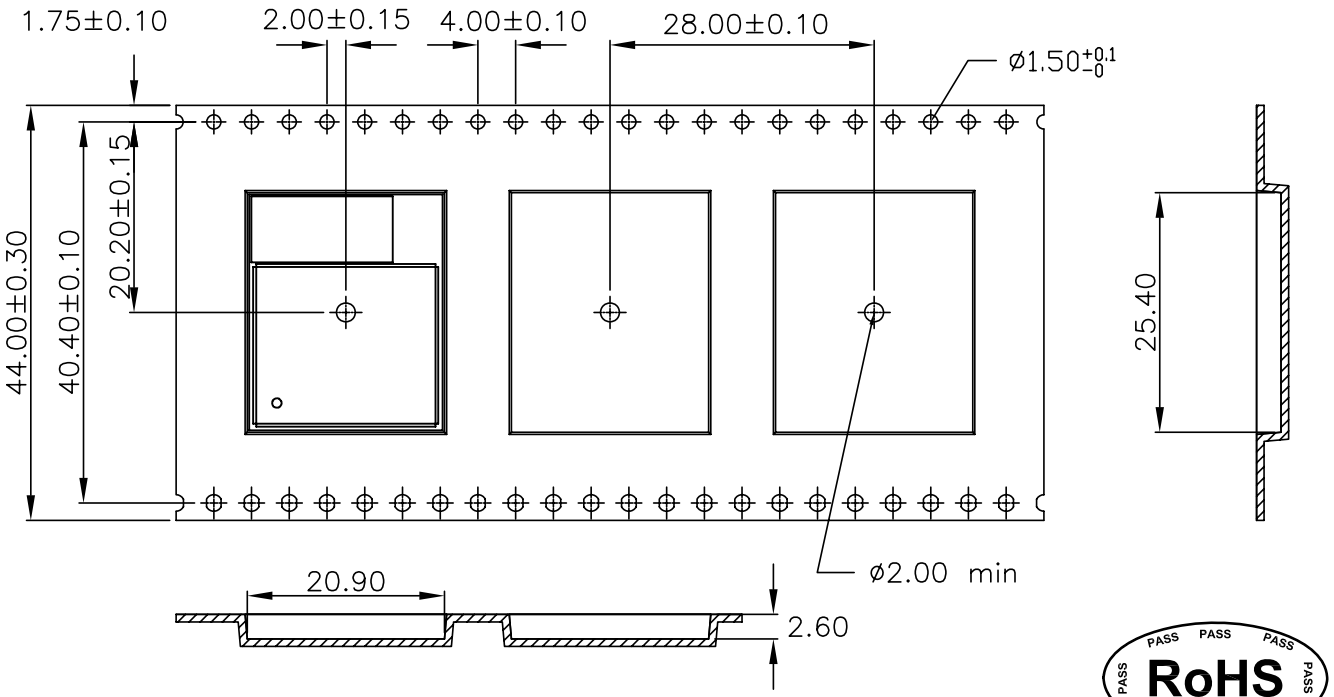
10.2.2.1 CC3220MODx Tape Specifications



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-C requirements.
5. Thickness : 0.40±0.05mm.
6. Packing length per13" reel : 25 Meters.
7. Component load per 7" reel : 1000pcs

W	44.00±0.30
A0	17.85±0.10
B0	20.85±0.10
K0	2.50±0.10

10.2.2.2 CC3220MODAx Tape Specifications



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.40±0.05mm.
6. Packing length per 13" reel : 23.5 Meters.(樣品盤)
7. Component load per 13" reel : 800 pcs.

W	44.00±0.30
A0	20.90±0.10
B0	25.40±0.10
K0	2.60±0.10

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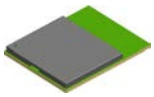
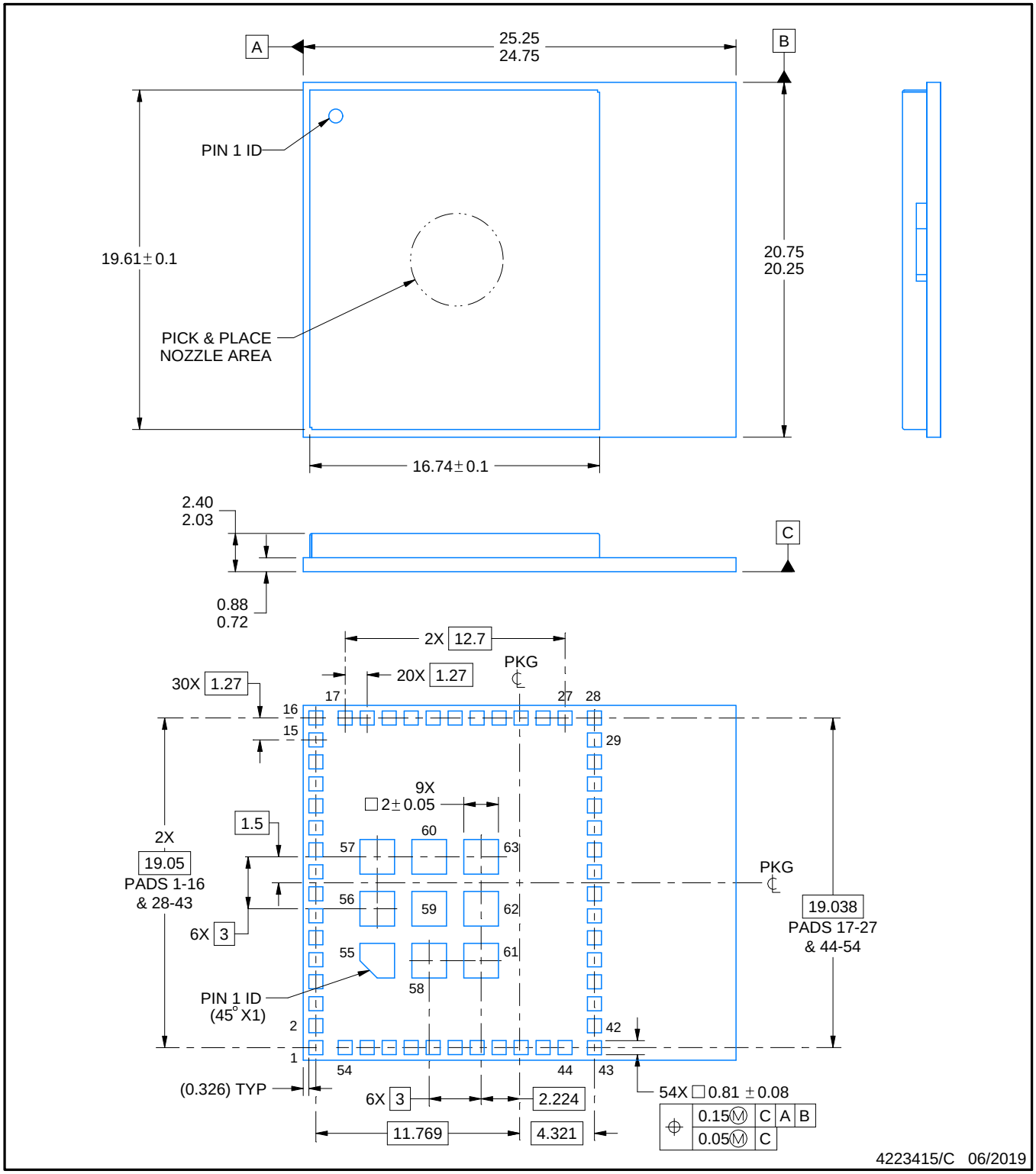
MON0063A



PACKAGE OUTLINE

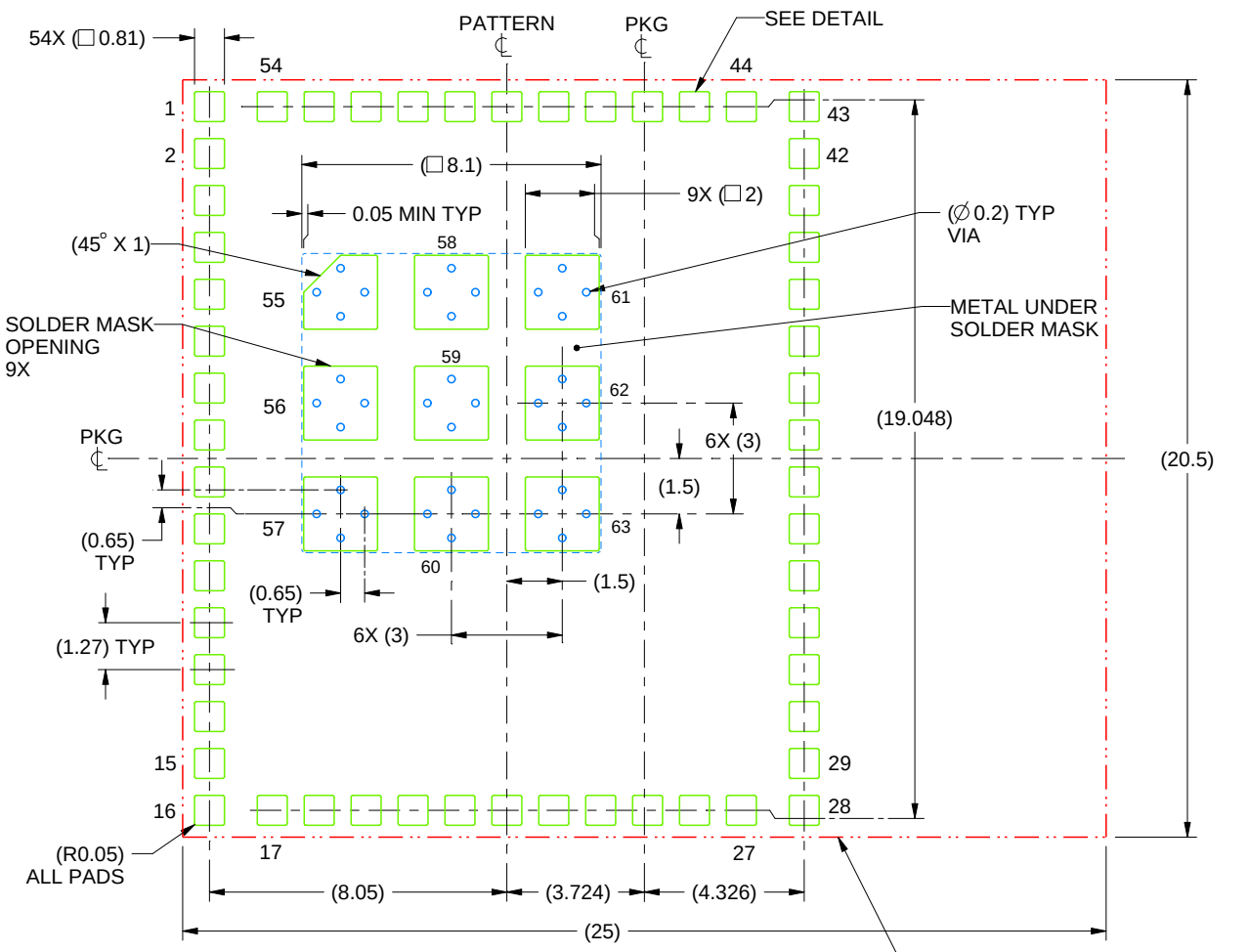
QFM - 2.4 mm max height

QUAD FLAT MODULE

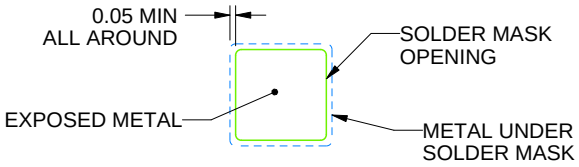


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:5X

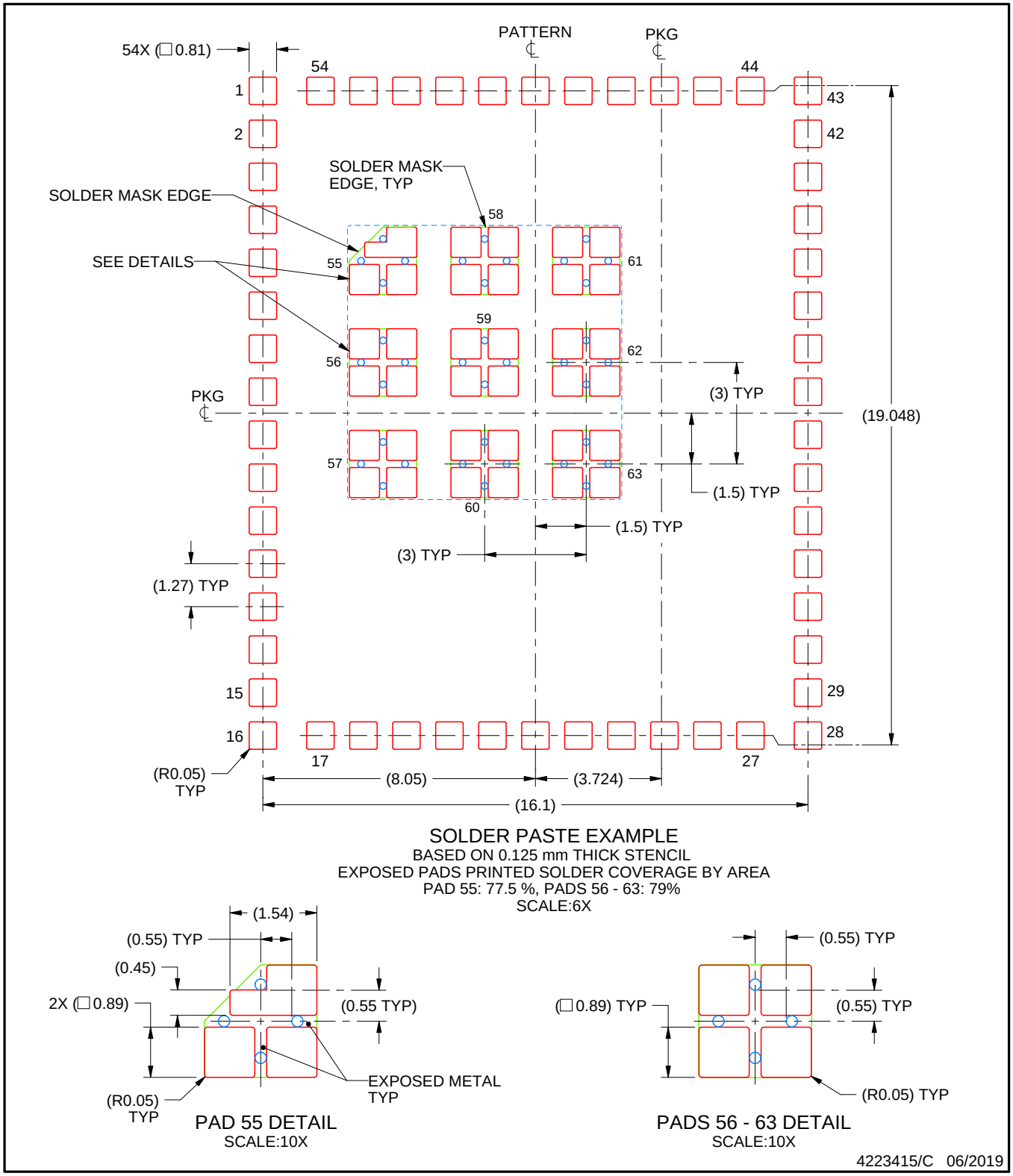


SIGNAL PADS DETAIL

4223415/C 06/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

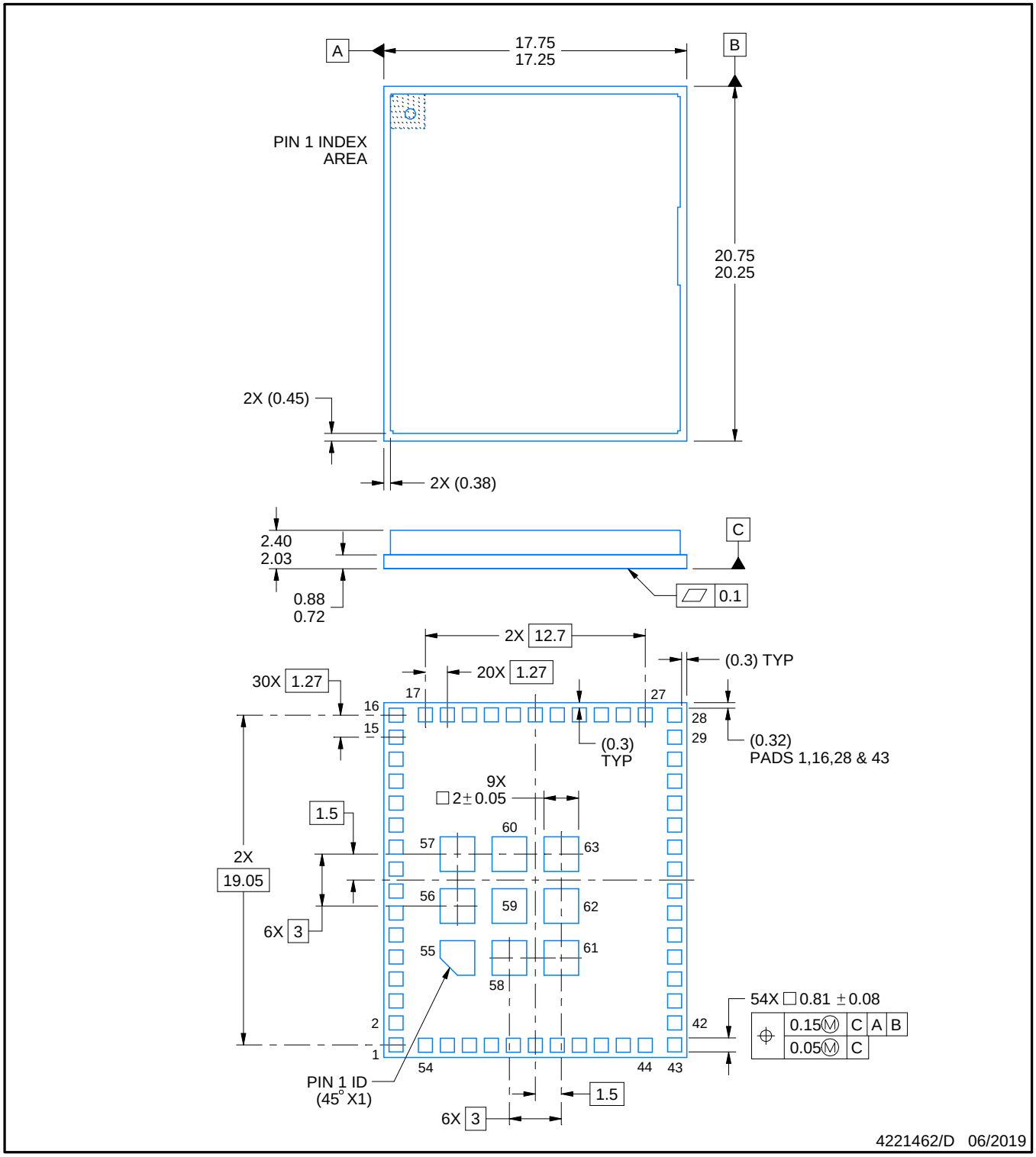
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

MOB0063A

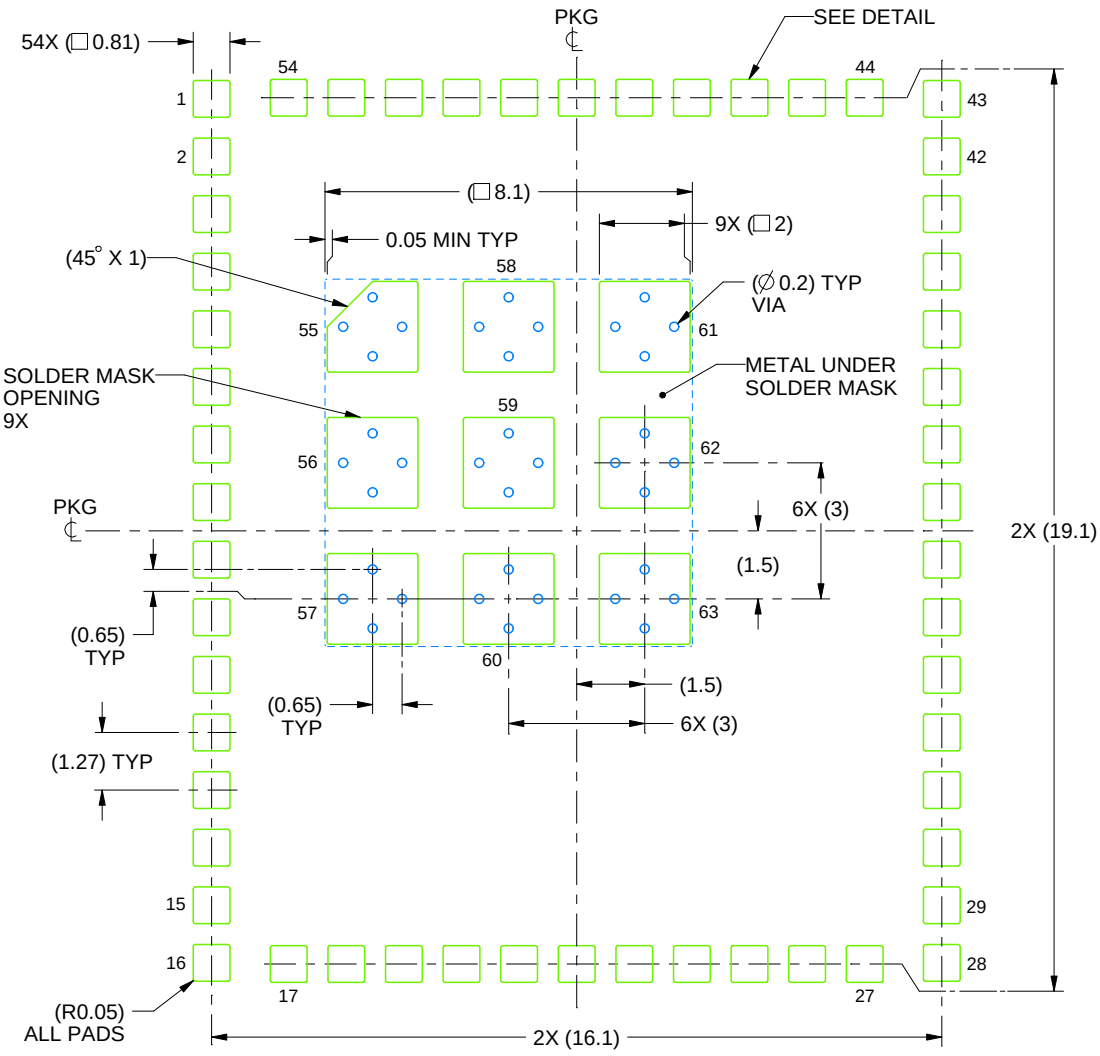
QFM - 2.4 mm max height

QUAD FLAT MODULE

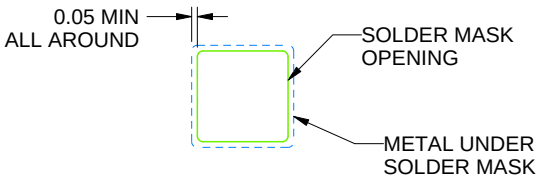


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:6X

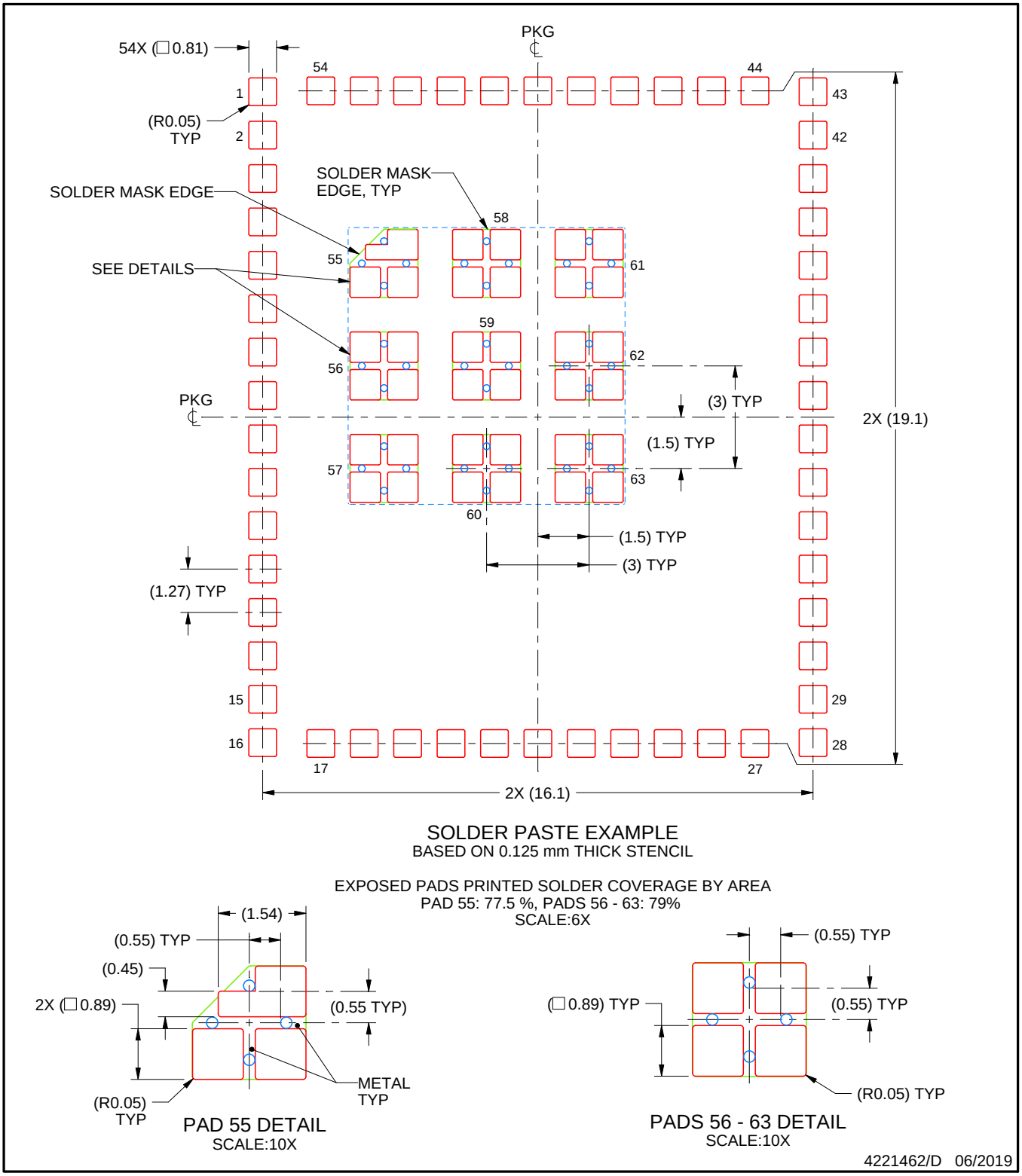


SIGNAL PADS DETAIL

4221462/D 06/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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