

LMX2581E 具有集成 VCO 的宽带频率合成器

1 特性

- 输出频率：50MHz 至 3800MHz
- 输入时钟频率高达 900MHz
- 相位检测器速率高达 200MHz
- 支持分数和整数两种模式
- 标准化锁相环 (PLL) 相位噪声为 -229dBc/Hz
- 标准化 PLL $1/f$ 噪声为 -120.8dBc/Hz
- 对于 2.5GHz 载波, 1MHz 偏移时的压控振荡器 (VCO) 相位噪声为 -137dBc/Hz
- 整数模式下的抖动为 100fs (均方根 (RMS))
- 可编程的分数调制器阶数
- 可编程的分数分母
- 高达 12dBm 的可编程输出功率
- 可编程的 32 级电荷泵电流
- 提供相应的可编程选项以使用外部 VCO
- 数字锁定检测
- 3 线串行接口和读回功能
- 单电源电压范围：3.15V 至 3.45V
- 支持最低至 1.6V 的逻辑电平

2 应用

- 无线基础设施 (通用移动通信系统 (UMTS)、长期演进技术 (LTE)、全球微波互联接入 (WiMax)、多标准基站)
- 无线宽带
- 测试和测量
- 时钟发生

4 简化电路原理图

3 说明

LMX2581E 是一款低噪声宽带频率合成器, 其集成有 $\Delta\Sigma$ 分数 N 锁相环 (PLL)、多核 VCO、可编程输出分频器以及两个差动输出缓冲器。VCO 的频率范围为 1880MHz 至 3800MHz, 既可以直接发送至输出缓冲器, 也可以进行 2 至 38 范围内的分频。每个缓冲器在 2700MHz 频率下都能够提供 -3dBm 至 $+12\text{dBm}$ 范围内的输出功率。该器件集成有低噪声、低压降稳压器 (LDO), 用于实现出色的抗扰度和稳定性能。

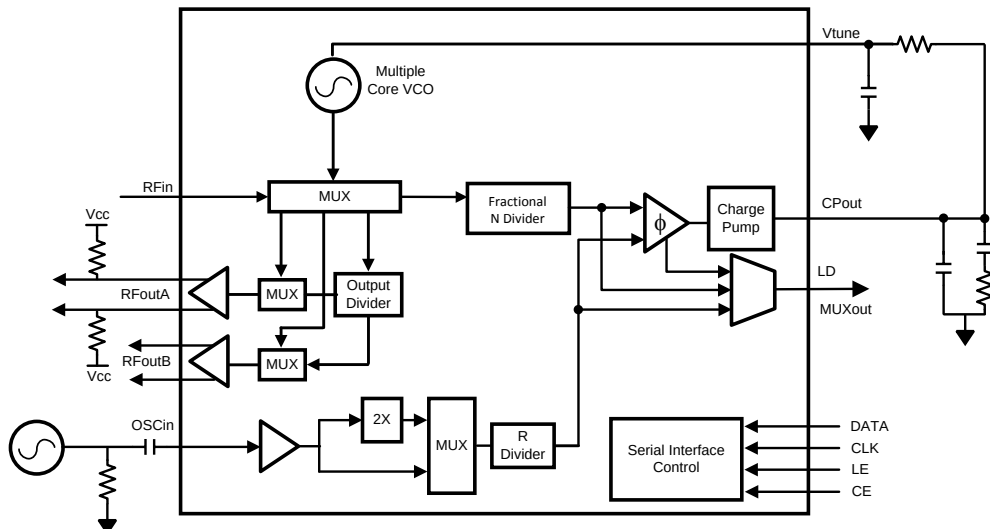
该合成器是一款高度可编程的器件, 用户可通过编程来优化其性能。在分数模式下, 分母和调制器阶数均可编程, 并且还可以配置抖动。用户还能够直接指定 VCO 内核或者完全旁路掉内部 VCO。最后, 该器件还包含许多便捷功能, 例如断电、快速锁定、自动静音以及锁定检测。所有寄存器均可通过简单的 3 线接口进行编程, 并且还提供读回功能。

LMX2581E 通过 3.3V 单电源供电运行, 并且采用 32 引脚 $5.0\text{mm} \times 5.0\text{mm}$ 超薄型四方扁平无引线 (WQFN) 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
LMX2581E	WQFN (32) DAP	5.00mm x 5.00mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。



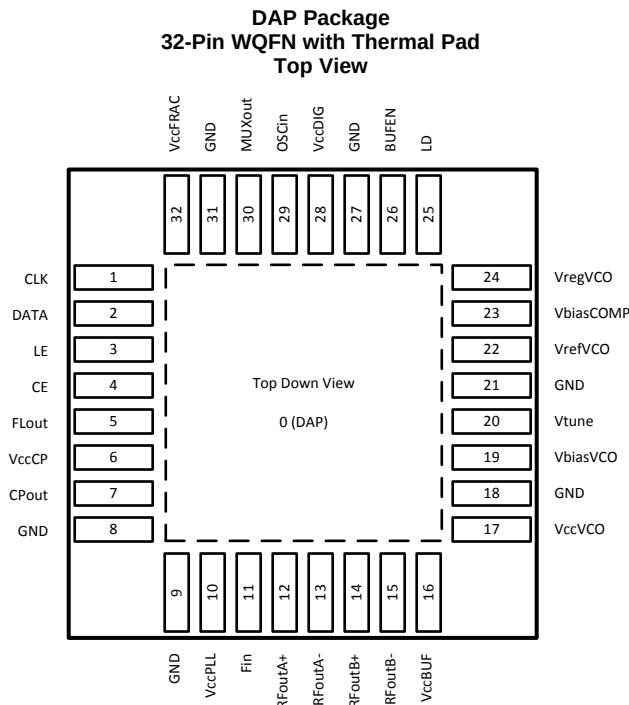
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5 修订历史记录

日期	修订版本	注释
2015 年 7 月	*	首次发布。

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
0	DAP	GND	The DAP should be grounded.
1	CLK	Input	MICROWIRE Clock Input. High Impedance CMOS input.
2	DATA	Input	MICROWIRE Data. High Impedance CMOS input.
3	LE	Input	MICROWIRE Latch Enable. High Impedance CMOS input.
4	CE	Input	Chip Enable Pin.
5	FLout	Output	Fastlock Output. This can switch in an external resistor to the loop filter during locking to improve lock time.
6	VccCP	Supply	Charge Pump Supply.
7	CPout	Output	Charge Pump Output.
8	GND	GND	Ground for the Charge Pump.
9	GND	GND	Ground for the N and R divider.
10	VccPLL	Supply	Supply for the PLL.
11	Fin	Input	High frequency input pin for an external VCO. Leave Open or Ground if not used.
12	RFoutA+	Output	Differential divided output. For single-ended operation, terminate the complimentary side with a load equivalent to the load at this pin.
13	RFoutA-	Output	Differential divided output. For single-ended operation, terminate the complimentary side with a load equivalent to the load at this pin.
14	RFoutB+	Output	Differential divided output. For single-ended operation, terminate the complimentary side with a load equivalent to the load at this pin.
15	RFoutB-	Output	Differential divided output. For single-ended operation, terminate the complimentary side with a load equivalent to the load at this pin.
16	VccBUF	Supply	Supply for the Output Buffer.
17	VccVCO	Supply	Supply for the VCO.
18	GND	GND	Ground Pin for the VCO. This can be attached to the regular ground. Ensure a solid trace connects this pin to the bypass capacitors on pins 19, 23, and 24.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
19	VbiasVCO	Output	Bias circuitry for the VCO. Place a 2.2 μ F capacitor to GND (Preferably close to Pin 18).
20	Vtune	Input	VCO tuning voltage input. See the functional description regarding the minimum capacitance to put at this pin.
21	GND	GND	VCO ground.
22	VrefVCO	Output	VCO capacitance. Place a capacitor to GND (Preferably close to Pin 18). This value should be between 5% and 10% of the capacitance at pin 24. Recommended value is 1 μ F.
23	VbiasCOMP	Output	VCO bias voltage temperature compensation circuit. Place a minimum 10 μ F capacitor to GND (Preferably close to Pin 18). If it is possible, use more capacitance to slightly improve VCO phase noise.
24	VregVCO	Output	VCO regulator output. Place a minimum 10 μ F capacitor to GND (Preferably close to Pin 18). If it is possible, use more capacitance to slightly improve VCO phase noise.
25	LD	Output	Multiplexed output that can perform lock detect, PLL N and R counter outputs, Readback, and other diagnostic functions.
26	BUFEN	Input	Enable pin for the RF output buffer. If not used, this can be overwritten in software.
27	GND	GND	Digital Ground.
28	VccDIG	Supply	Digital Supply.
29	OSCin	Input	Reference input clock.
30	MUXout	Output	Multiplexed output that can perform lock detect, PLL N and R counter outputs, Readback, and other diagnostic functions..
31	GND	GND	Ground for the fractional circuitry.
32	VccFRAC	Supply	Supply for the fractional circuitry.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Power supply voltage	−0.3	3.6	V
V _{IN}	Input voltage to pins other than V _{CC} pins	−0.3	(V _{CC} + 0.3)	V
T _L	Lead temperature (solder 4 sec.)		260	°C
T _J	Junction temperature		150	°C
V _{OSCIN}	Voltage on OSCIN (Pin29)	≤1.8 with V _{CC} Applied ≤1 with V _{CC} = 0		V _{pp}
Storage Temperature, T _{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{CC}	Power Supply Voltage	3.15	3.3	3.45	V
T _J	Junction Temperature			125	°C
T _A	Ambient Temperature	−40		85	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMX2581E	UNIT
		DAP (WQFN)	
		32 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	30	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance		
R _{θJB}	Junction-to-board thermal resistance		
Ψ _{JT}	Junction-to-top characterization parameter		
Ψ _{JB}	Junction-to-board characterization parameter		
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40°C ≤ T_A ≤ 85°C; except as specified. Typical values are at V_{CC} = 3.3 V, 25°C.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION							
I _{CC}	Entire chip supply current	One Output Enabled OUT _x _PWR = 15		178			mA
I _{CC} Core	Supply current except for output buffers	Output Buffers and VCO Divider Disabled.		134			mA
I _{CC} RFout	Additive current for each output buffer	OUT _x _PWR = 15		44			mA
I _{CC} VCO_DIV	Additive VCO divider current	VCO Divider Enabled		20			mA
I _{CC} PD	Power down current	Device Powered Down (CE Pin = LOW)		7			mA
OSCin REFERENCE INPUT							
f _{OSCin}	OSCin frequency range	Doubler Enabled		5	250		MHz
		Doubler Disabled		5	900		
V _{OSCin}	OSCin input voltage	AC Coupled		0.4	1.7		V _{pp}
Spur _{Foscin}	Oscin spur	Foscin = 100 MHz, Offset = 100 MHz		-81			dBc
PLL							
f _{PD}	Phase detector frequency			200			MHz
K _{PD}	Charge-pump gain	Gain = 1X		110			μA
		Gain = 2X		220			
		...		...			
		Gain = 31X		3410			
PN _{PLL_1/f_Norm}	Normalized PLL 1/f noise ⁽¹⁾	Gain =31X Normalized to 1 GHz carrier and 10 kHz Offset		-120.8			dBc/Hz
PN _{PLL_FOM}	PLL figure of merit (Normalized Noise Floor) ⁽¹⁾	Gain =31X. Normalized to PLL1 and f _{PD} =1Hz		-229			dBc/Hz
f _{RFin}	External VCO input pin frequency	Internal VCOs Bypassed (OUTA_PD=OUTB_PD=1)		0.5	2.2		GHz
p _{RFin}	External VCO input pin power	Internal VCOs Bypassed (OUTA_PD=OUTB_PD=1)		0	+8		dBm
Spur _{Fpd}	Phase detector spurs ⁽²⁾	Fpd = 25 MHz		-85			dBc
		Fpd = 100 MHz		-81			
OUTPUTS							
p _{RFoutA+/-} p _{RFoutB+/-}	Output power level ⁽³⁾ (3)	Inductor Pullup F _{OUT} = 2.7 GHz	OUT _x _PWR=15	7.3			dBm
			OUT _x _PWR=45	12			
H2 _{RFoutX+/-}	Second harmonic ⁽⁴⁾	F _{OUT} = 2.7 GHz	OUT _x _PWR=15	-25			dBc

- (1) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into 1/f and flat components. PLL_Flat = PLL_FOM + 20*log(Fvco/Fpd)+10*log(Fpd / 1Hz). PLL_1/f = PLL_1/f_Norm + 20*log(Fvco / 1GHz) - 10*log(Offset/10kHz). Once these two components are found, the total PLL noise can be calculated as PLL_Noise = 10*log(10^{PLL_Flat/10} + 10^{PLL_1/f / 10})
- (2) The spurs at the offset of the phase detector frequency are dependent on many factors, such as the phase detector frequency.
- (3) The output power is dependent of the setup and is also programmable. Consult [Application and Implementation](#) for more information.
- (4) The harmonics vary as a function of frequency, output termination, board layout, and output power setting.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40°C ≤ T_A ≤ 85°C; except as specified. Typical values are at V_{CC} = 3.3 V, 25°C.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO							
f _{VCO}		Before the VCO Divider	All VCO Cores Combined	1880		3800	MHz
K _{VCO}	VCO gain	V _{tune} = 1.3 Volts	Core 1	12 to 24			MHz/V
			Core 2	15 to 30			
			Core 3	20 to 37			
			Core 4	21 to 37			
ΔT _{CL}	Allowable temperature drift (5)	VCO not being re-calibrated	Fvco ≥2.5 GHz	−125		+125	°C
			Fvco < 2.5 GHz	−100		+125	
t _{VCOcal}	VCO calibration time (6)	f _{OSCin} = 100 MHz f _{PD} = 100 MHz Full Band Change 1880 — 3800 MHz	No Pre-programming	140			μs
			With Pre-programming	10			
PN _{VCO}	VCO phase noise (OUTx_PWR =15)	f _{VCO} = 1.9 GHz Core 1	10 kHz Offset	−85.4			dBc/Hz
			100 kHz Offset	−114.5			
			1 MHz Offset	−137.0			
			10 MHz Offset	−154.2			
			40 MHz Offset	−156.7			
		f _{VCO} = 2.2 GHz Core 2	10 kHz Offset	−84.6			dBc/Hz
			100 kHz Offset	−114.1			
			1 MHz Offset	−137.5			
			10 MHz Offset	−154.5			
			40 MHz Offset	−156.1			
		f _{VCO} = 2.7 GHz Core 3	10 kHz Offset	−81.7			dBc/Hz
			100 kHz Offset	−112.2			
			1 MHz Offset	−136.0			
			10 MHz Offset	−153.1			
			40 MHz Offset	−155.0			
		f _{VCO} = 3.3 GHz Core 4	10 kHz Offset	−79.0			dBc/Hz
			100 kHz Offset	−108.6			
			1 MHz Offset	−132.6			
			10 MHz Offset	−152.0			
			40 MHz Offset	−155.0			

- (5) Continuous tuning range over temperature refers to programming the device at an initial temperature and allowing this temperature to drift WITHOUT reprogramming the device. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.
- (6) VCO digital calibration time is the amount of time it takes for the VCO to find the correct frequency band when switching to a new frequency. After the correct frequency band is found, the remaining error is typically less than 1 MHz and then the PLL settles the rest of the error in an analog manner. Pre-programming refers to specifying a band that is close to the final (< 20 MHz), which greatly improves the VCO calibration time.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40°C ≤ T_A ≤ 85°C; except as specified. Typical values are at V_{CC} = 3.3 V, 25°C.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INTERFACE (DATA, CLK, LE, CE, MUXout, BUFEN, LD)					
V _{IH}	High-level input voltage	1.4		V _{CC}	V
V _{IL}	Low level input voltage			0.4	V
I _{IH}	High-level input current	V _{IH} = 1.75 V		5	μA
I _{IL}	Low-level input current	V _{IL} = 0 V		5	μA
V _{OH}	High-level output voltage	I _{OH} = -500 μA			V
V _{OL}	Low-Level output voltage	I _{OL} = -500 μA			V
			0	0.4	V

7.6 Timing Requirements, MICROWIRE Timing

See Figure 1		MIN	NOM	MAX	UNIT
t _{ES}	Clock-to-enable low time	35			ns
t _{CS}	Data-to-clock set up time	10			ns
t _{CH}	Data-to-clock hold time	10			ns
t _{CWH}	Clock pulse width high	25			ns
t _{CWL}	Clock pulse width low	25			ns
t _{CES}	Enable-to-clock setup time	10			ns
t _{EWL}	Enable pulse width high	10			ns

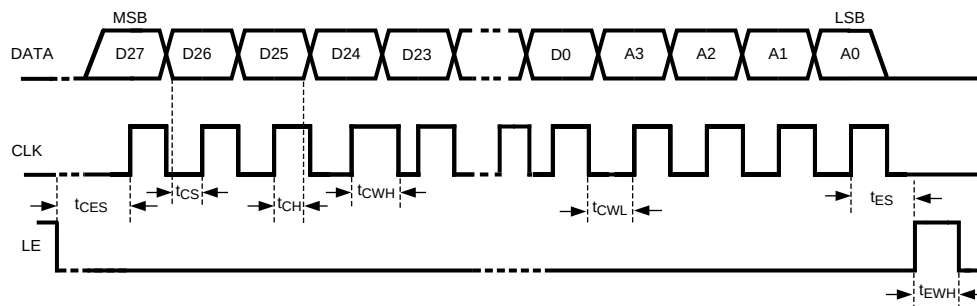


Figure 1. Serial Data Input Timing

7.7 Typical Characteristics

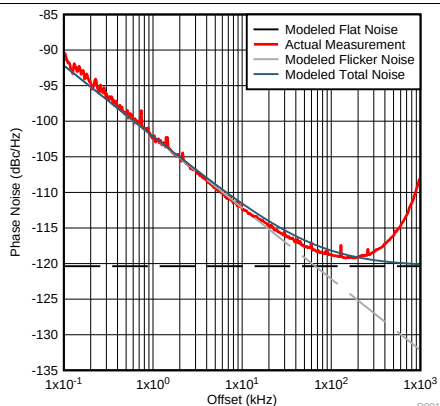


Figure 2. Measurement of PLL Figure of Merit and Normalized 1/f Noise

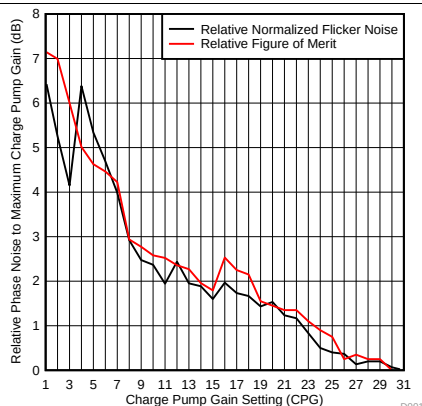


Figure 3. K_{PD} Impact on PLL Noise Metrics

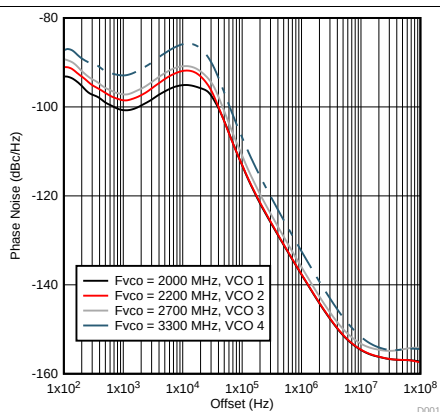


Figure 4. Closed Loop Noise for Narrower Bandwidth Filter

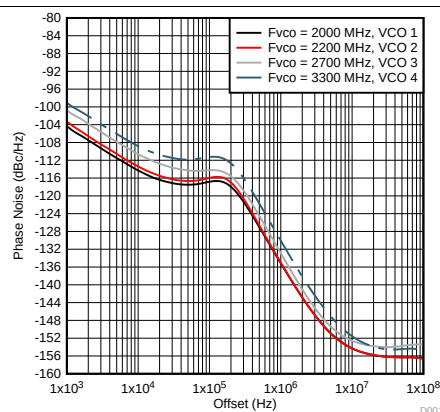


Figure 5. Closed Loop Noise for Wider Bandwidth

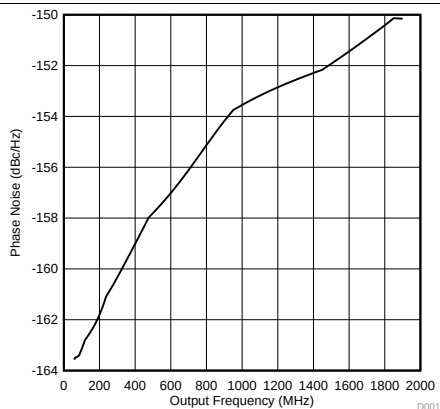


Figure 6. VCO Output Divider Noise Floor vs. Frequency

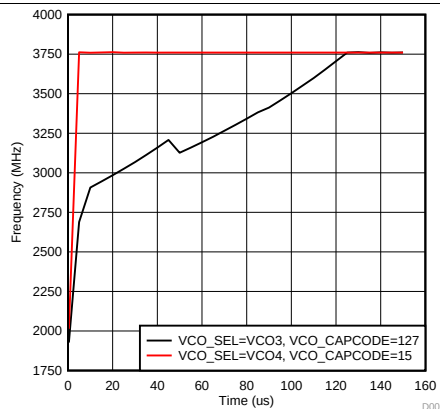


Figure 7. VCO Digital Calibration Time

Typical Characteristics (continued)

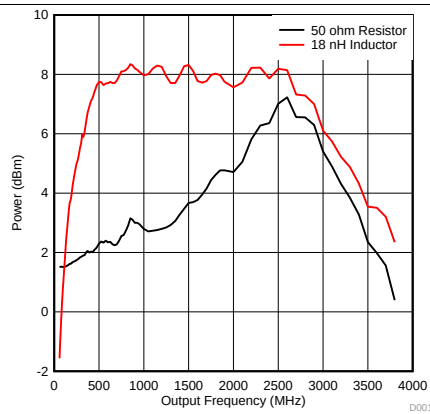


Figure 8. Single-Ended Output Power vs. Frequency

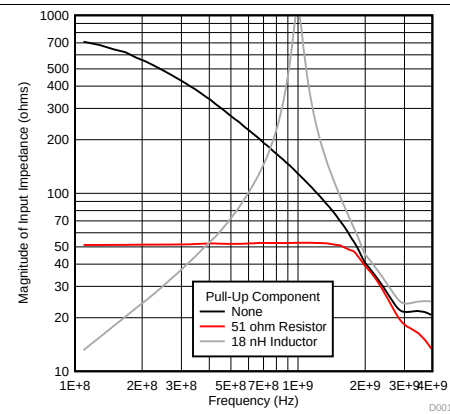


Figure 9. Impedance of RFoutX Pins

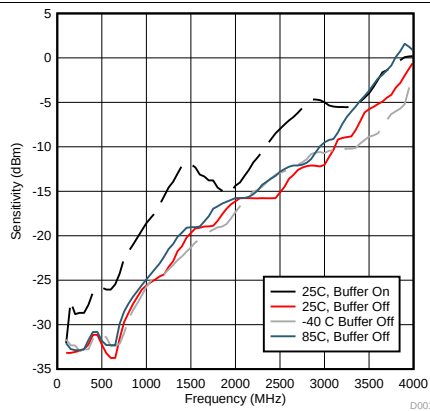


Figure 10. Sensitivity for External VCO Input (Fin) Pin

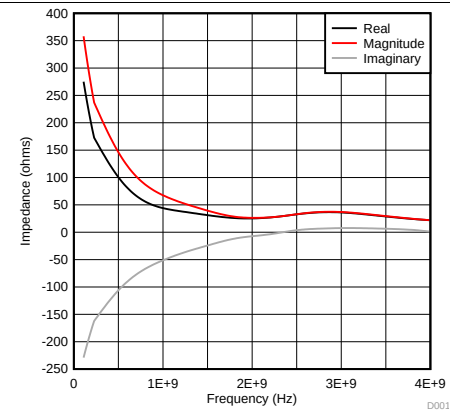


Figure 11. Impedance of External VCO Input (Fin) Pin

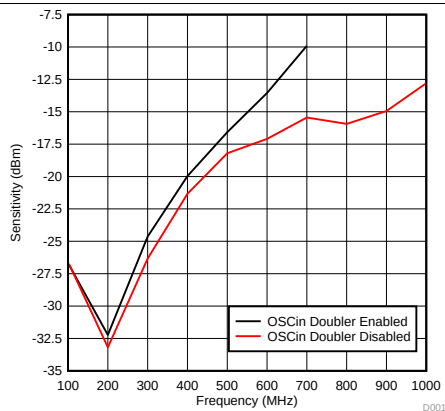


Figure 12. OSCin Input Sensitivity

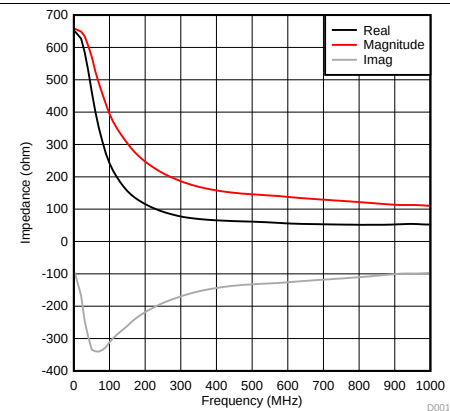


Figure 13. OSCin Input Impedance

8 Detailed Description

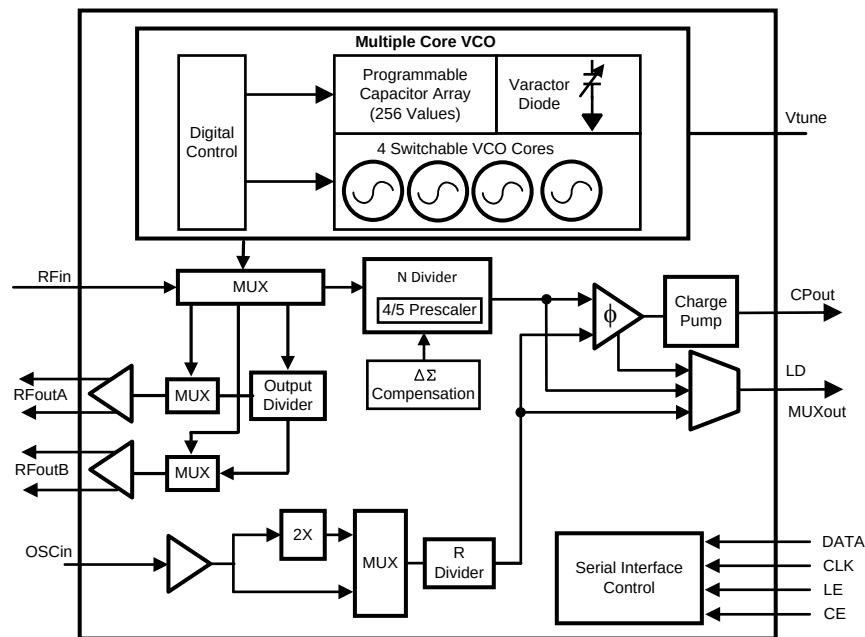
8.1 Overview

The LMX2581E is a synthesizer, consisting of a reference input and R divider, phase detector and charge pump, VCO and high frequency fractional (N) divider, and two programmable output buffers. The device requires external components for the loop filter and output buffers, which are application dependent.

Based on the oscillator input frequency (f_{OSC}), PLL R divider value (PLL_R), PLL N Divider Value (PLL_N), Fractional Numerator (PLL_NUM), Fractional Denominator (PLL_DEN), and VCO divider value (VCO_DIV), the output frequency of the LMX2581E (f_{OUT}) can be determined as follows:

$$f_{OUT} = f_{OSC} \times OSC_2X / PLL_R \times (PLL_N + PLL_NUM / PLL_DEN) / VCO_DIV \quad (1)$$

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Typical Performance Characteristics

8.3.1.1 Phase Noise Typical Performance Plot Explanations

Figure 2 shows 2700 MHz output and a 100 MHz phase detector frequency. The modeled noises (Flat, Flicker, and Total) are calculated from the normalized -229 dBc/Hz figure of merit and the -120.8 dBc/Hz normalized $1/f$ noise from the electrical table. After 200 kHz, the loop filter dynamics cause the noise to increase sharply.

Figure 3 shows the relative changes with the normalized PLL noise and figure of merit as a function of charge pump gain. The PLL phase noise changes as a function of the charge pump gain.

Figure 4 shows the phase noise for a filter optimized for spurs with a 20 MHz phase detector and running in fractional mode with strong dithering. Due to the narrower loop bandwidth, the impact of the VCO phase noise inside the loop bandwidth is in the 1 to 10 kHz region.

In Figure 5, the loop filter was optimized for RMS jitter. This was in fractional mode with a phase detector of 200 MHz and uses the First Order Modulator.

In Figure 6, the output divider noise floor only applies when the output divider is not bypassed and depends mainly on output frequency, not the actual divide value.

8.3.1.2 Other Typical Performance Plot Characteristics Explanations

Figure 7 shows a frequency change of 1880 MHz to 3760 MHz with $F_{osc} = F_{pd} = 100$ MHz. If the VCO3 is selected as the starting VCO with VCO_CAPCODE=127, digital calibration time is closer to 115 μ s. If VCO4 is selected as the starting VCO with VCO_CAPCODE=15, the calibration time is greatly shortened to something of the order of 5 μ s.

Figure 8 was measured with a board with very short traces. Only one of the differential outputs is routed.

In Figure 9, the output impedance is mainly determined by the pullup component used at lower frequencies. For the resistor, it is 51 Ω up to about 2 GHz, where the impedance of the device starts to dominate. For the inductor it increases with frequency and then reaches a resonance frequency before coming down. These behaviors are specific to the pullup component. These impedance plots match the conditions that were used to measure output power.

In Figure 12, the OSCin input sensitivity for a sine wave. The voltage has no impact and the temperature only has a slight impact. Enabling the doubler limits the performance

In Figure 13, For lower frequencies, the magnitude of the OSCin input impedance can be considered high relative to 50 Ω . At higher frequencies, it is not as high and a resistive pad may be better than a simple shunt 50 Ω resistor for matching.

Feature Description (continued)

8.3.2 Impact of Temperature on VCO Phase Noise

The phase noise specifications for the VCO in [Electrical Characteristics](#) are for a narrow loop bandwidth at room temperature. If the temperature is changed, [Table 1](#) gives an approximation on how the VCO phase noise is impacted. For instance, if one was to lock the PLL at -40°C and then measure the phase noise at 1 MHz offset, the phase noise would typically be of the order of 2 dB better than if it was locked and measured at 25°C. If the PLL is locked at -40°C and then the temperature was to drift to 85°C, then the phase noise at 1 MHz offset would typically be about 2 dB worse than it would be if it was locked and measured at 25°C. These numbers are only approximations and may change between devices and over VCO cores slightly.

Table 1. Approximate Change in VCO Phase Noise vs. Temperature and Temperature Drift in dB

STARTING TEMPERATURE	FINAL TEMPERATURE	OFFSET				
		10 kHz	100 kHz	1 MHz	10 MHz	40 MHz
-40°C	-40°C	-2	-1	-2	-2	0
	25°C	-1	0	0	-1	0
	85°C	-3	2	2	-0	0
25°C	-40°C	-1	-1	0	-1	0
	25°C	These are all zero because all measurements are relative to this row.				
	85°C	-3	2	2	0	0
85°C	-40°C	-4	-2	-2	0	0
	25°C	-1	0	0	-2	0
	85°C	-2	2	2	0	0

8.3.3 OSCin INPUT and OSCin Doubler

The OSCin pin is driven with a single-ended signal which is used as a frequency reference. Before the OSCin frequency reaches the phase detector, it may be doubled with the OSCin doubler and/or divided with the PLL R divider.

Because the OSCin signal is used as a clock for the VCO calibration, the OSC_FREQ word needs to be programmed correctly and a proper signal needs to be applied at the OSCin pin at the time of programming the R0 register in order for the VCO calibration to properly work. Higher slew rates tend to yield the best fractional spurs and phase noise, so a square wave signal is best for OSCin. If using a sine wave, higher frequencies tend to yield better phase noise and fractional spurs due to their higher slew rates. The OSCin pin has high impedance, so for optimal performance, it is recommended to use either a shunt resistor or resistive pad to make sure that the impedances looking towards and away from the device input are both close to 50 Ω.

8.3.4 R Divider

The R divider divides the OSCin frequency down to the phase detector frequency. With this device, it is possible to use both the doubler and the R divider at the same time.

8.3.5 PLL N Divider And Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator (PLL_DEN) from 1 to 4,194,303. The integer portion, PLL_N, is the whole part of the N divider value and the fractional portion, PLL_NUM / PLL_DEN, is the remaining fraction. PLL_N, PLL_NUM, and PLL_DEN are software programmable. So in general, the total N divider value, N, is determined by: $N = PLL_N + PLL_NUM / PLL_DEN$. The order of the delta sigma modulator is programmable from integer mode to third order. There are also several dithering modes that are also programmable. In order to make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

8.3.5.1 Programmable Dithering Levels

If used appropriately, dithering may be used to reduce sub-fractional spurs, but if used inappropriately, it can actually create spurs and increase phase noise. [Table 2](#) provides guidelines for the use of dithering based on the fractional denominator, after the fraction is reduced to lowest terms.

Table 2. Dithering Recommendations

FRACTION	DITHERING RECOMMENDATION	COMMENTS
Fractional Numerator = 0	Disable Dithering	This is often the worst case for spurs, which can actually be turned into the best case by simply disabling dithering. This will have performance that is similar to integer mode.
Equivalent Denominator < 20	Disable Dithering	These fractions are not well randomized and dithering will likely create phase noise and spurs.
Equivalent Denominator is not divisible by 2 or 3	Disable Dithering	There will be no sub-fractional spurs, so dithering is likely not to be very effective
Equivalent Denominator > 200 and is divisible by 2 or 3	Consider Dithering	Dithering may help reduce the sub-fractional spurs, but understand it may degrade the PLL phase noise.

In general, dithering is likely to cause more harm than good for poorly randomized fractions like 1/2. There are situations when dithering does make sense and when it is used, it is recommended to adjust the PFD_DLY word accordingly to compensate for this.

8.3.5.2 Programmable Delta Sigma Modulator Order

The fractional modulator order is programmable, which gives the opportunity to better optimize phase noise and spurs. Theoretically, higher order modulators push out phase noise to farther offsets, as described in [Table 3](#).

Table 3. Choosing the Fractional Modulator Order

MODULATOR ORDER	APPLICATIONS
Integer Mode (Order = 0)	If the fractional numerator is zero, it is best to run the device in integer mode to minimize phase noise and spurs.
First Order Modulator	When the equivalent fractional denominator is 6 or less, the first order modulator theoretically has lower phase noise and spurs, so it always makes sense in these situations. When the fractional denominator is between 6 and about 20, consider using the first order modulator because the spurs might be far enough outside the loop bandwidth that they will be filtered. The first order modulator also does not create any sub-fractional spurs or phase noise.
2nd and 3rd Order Modulators	The choice between 2nd and 3rd order modulator tends to be a little more application specific. If the fractional denominator is not divisible by 3, then the 2nd and 3rd order modulators will have spurs in the same offsets, so the 3rd is generally better for spurs. However, if stronger levels of dithering is used, the 3rd order modulator will create more close-in phase noise than the 2nd order modulator

[Figure 14](#) and [Figure 15](#) give an idea of the theoretical impact of the delta sigma modulator order on the shaping of the phase noise and spurs. In terms of phase noise, this is what one would theoretically expect if strong dithering was used for a well-randomized fraction. Dithering can be set to different levels or even shut off and the noise can be eliminated. In terms of spurs, they can change based on fraction, but they will theoretically be pushed out to higher phase detector frequencies. However, one must be aware that these are just THEORETICAL graphs and for offsets that are on the order of less than 5% of the phase detector frequency, other factors can impact the noise and spurs. In [Figure 14](#), the curves all cross at 1/6th of the phase detector frequency and that this transfer function peaks at half of the phase detector frequency, which is assumed to be well outside the loop bandwidth. [Figure 15](#) shows the impact of the phase detector frequency on the modulator noise.

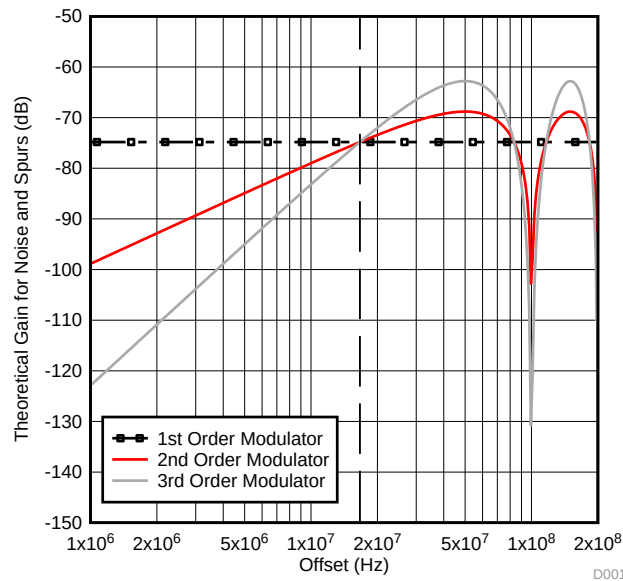


Figure 14. Theoretical Delta Sigma Noise Shaping for a 100 MHz Phase Detector Frequency

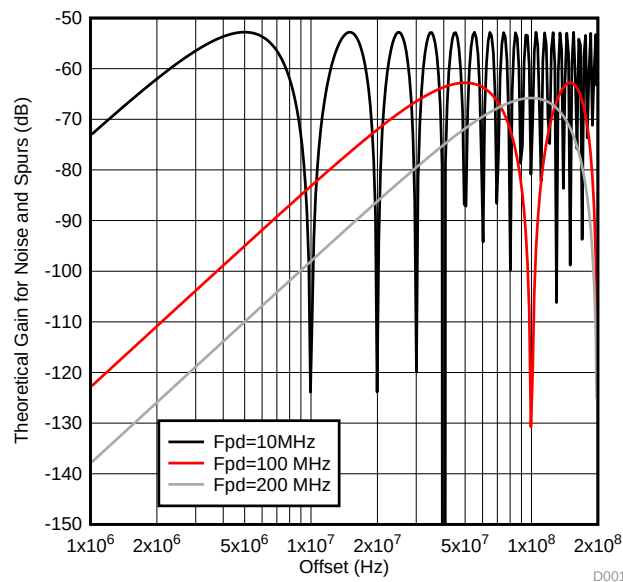


Figure 15. Theoretical Delta Sigma Noise Shaping for 3rd Order Modulator

For lower offsets, the actual noise added by the delta sigma modulator may be higher than the theoretical values shown due to nonlinearity of the phase detector. This noise floor can vary with the modulator order, phase detector frequency, and PFD_DLY word setting as shown in the following table, which shows the phase noise at 10 kHz offset for a frequency close to 2801 MHz with a well randomized fraction and strong dithering. The phase noise in integer mode is also shown for comparison purposes.

Table 4. Impact of PFD_DLY, Modulator Order, and Phase Detector Frequency on Modulator Noise Floor

PFD_DLY	INTEGER				2nd ORDER MODULATOR				3rd ORDER MODULATOR			
	Fpd= 25 MHz	Fpd= 50MHz	Fpd= 100 MHz	Fpd= 200 MHz	Fpd= 25 MHz	Fpd= 50MHz	Fpd= 100 MHz	Fpd= 200 MHz	Fpd= 25 MHz	Fpd= 50MHz	Fpd= 100 MHz	Fpd= 200 MHz
0	-106.7	-109.5	-111.4	-111.0	-106.3	-108.8	-110.6	-111.0	-84.4	-87.5	-90.1	-93.8
1	-106.2	-108.8	-110.6	-110.9	-106.5	-108.4	-110.1	-110.0	-88.3	-91.3	-93.6	-98.5
2	-106.0	-108.3	-109.7	-110.1	-105.6	-108.3	-109.2	-110.1	-92.9	-96.1	-98.1	-102.8
3	-106.0	-108.2	-109.4	-109.9	-105.3	-107.9	-109.2	-109.8	-99.2	-101.8	-102.6	-105.4
4	-105.6	-107.7	-109.4	-110.0	-105.1	-107.5	-108.7	-109.3	-103.0	-105.4	-105.8	-106.2
5	-105.5	-107.6	-108.8	-110.1	-105.6	-107.4	-108.6	-109.0	-101.4	-104.0	-103.7	-105.5
6	-105.1	-107.3	-108.5	-109.3	-104.6	-107.0	-107.8	-109.1	-98.4	-101.6	-102.7	-102.9
7	-104.8	-106.8	-108.2	-105.9	-104.6	-106.2	-107.4	-108.7	-97.1	-100.6	-102.1	-100.2

8.3.6 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the R and N dividers and generates a correction current corresponding to the phase error. This charge pump current is software programmable to many different levels. The phase detector frequency, f_{PD} , can be calculated as follows:

$$f_{PD} = f_{OSCin} \times OSC_2X / R \quad (2)$$

The charge pump outputs a correction current into the loop filter, which is implemented with external components. The gain of the charge pump is programmable to 32 different levels with the CPG word and the PFD_DLY word can adjust the minimum on time that the charge pump comes on for.

8.3.7 External Loop Filter

The LMX2581E requires an external loop filter which is application-specific and can be configured by consulting [LMX2581E Tools and Software](#). For the LMX2581E, it matters what impedance is seen from the Vtune pin looking outwards. This impedance is dominated by the component C3_LF for a third order filter or C1_LF for a second order filter ($R3_LF = C3_LF = 0$). If there is at least 3.3 nF for the capacitance that is shunt with this pin, the VCO phase noise will be close to the best it can be. If there is less, the VCO phase noise in the 100 k to 1MHz region. In cases where 3.3 nF might restrict the loop bandwidth to be too narrow, it might make sense to violate this restriction a little and sacrifice some VCO phase noise in order to get a wider loop bandwidth.

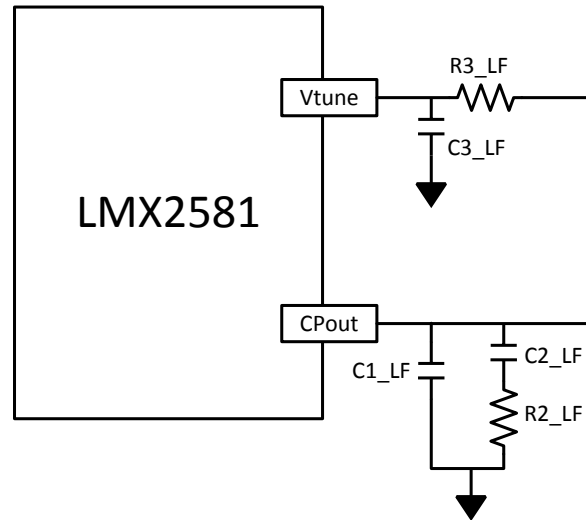


Figure 16. Typical Loop Filter

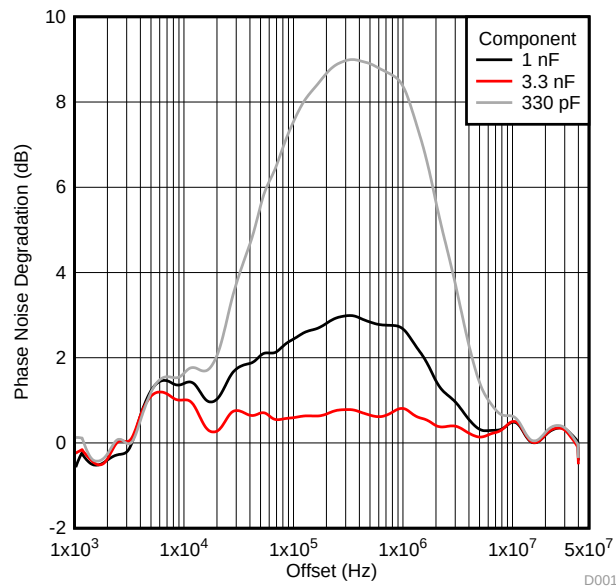


Figure 17. Vtune Capacitor Impact on VCO Phase Noise

8.3.8 Low Noise, Fully Integrated VCO

The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies and divider values as follows: $f_{VCO} = f_{PD} \times N = f_{OSCin} \times OSC_2X \times N / R$. The VCO is fully integrated, including the tank circuitry.

In order to reduce the VCO tuning gain and therefore improve the VCO phase noise performance, the internal VCO is actually made of VCO cores working as one. These cores starting from lowest frequency to highest frequency are VCO 1, VCO 2, VCO 3, and VCO 4. Each VCO core has 256 different frequency bands. Band 255 is the lowest frequency and Band 0 is the highest. This creates the need for frequency calibration in order to determine the correct VCO core and correct frequency band in that VCO core. The frequency calibration routine is activated any time that the R0 register is programmed with the NO_FCAL bit equal to zero. In order for this frequency calibration to work properly, the OSC_FREQ word needs to be set to the correct setting. The VCO_SEL word allows the user to suggest a particular VCO core for the device to choose, which is useful for optimizing fractional spurs and minimizing lock time.

Table 5. Approximate (NOT Ensured) VCO Core Frequency Ranges

VCO CORE	APPROXIMATE FREQUENCY RANGE
VCO 1	1800 to 2270 MHz
VCO 2	2135 to 2720 MHz
VCO 3	2610 to 3220 MHz
VCO 4	3075 to 3880 MHz

8.3.8.1 VCO Digital Calibration

When the frequency is changed, the digital VCO goes through the following VCO calibration:

1. Depending on the status of the VCO_SEL word, the starting VCO core is selected.
2. The algorithm starts counting at the default band in this core as determined by the VCO_CAPCODE value.
3. The VCO increments or decrements the CAPCODE based on the what the actual VCO output is compared to the target VCO output.
4. Repeat step 3 until either the VCO is locked or the VCO is at VCO_CAPCODE = 0 or 255
5. If not locked, then choose the next appropriate VCO if possible and return to step 3. If not possible, the calibration is terminated.

A good starting point is to set VCO_SEL = 2 for VCO 3 and set VCO_SEL_MODE = 1 to start at the selected core. If there is the potential of switching the VCO from a frequency above 3 GHz directly to a frequency below 2.2 GHz, VCO_SEL_MODE can not be set to 0. In this case, VCO_SEL_MODE can still be set to 1 to select a starting core, but the starting core specified by VCO_SEL can not be VCO 4.

The digital calibration time can be improved dramatically by giving the VCO guidance regarding which VCO core and which VCO_CAPCODE to start using. Even if the wrong VCO core is chosen, which could happen near the boundary of two cores, the calibration time is improved. For situations where the frequency change is small, the device can be programmed to automatically start at the last VCO core used. For applications where the frequency change is relatively small, the best VCO calibration time can often be achieved by setting the VCO_SEL_MODE to choose the last VCO core that was used.

8.3.9 Programmable VCO Divider

The VCO divider can be programmed to even values from 2 to 38 as well as bypassed by either one or both of the RFout outputs. When the zero delay mode is not enabled, the VCO divider is not in the feedback path between the VCO and the PLL and therefore has no impact on the PLL loop dynamics. After this programmable divider is changed, it may be beneficial to reprogram the R0 register to re-calibrate the VCO. The frequency at the RFout pin is related to the VCO frequency and divider value, VCO_DIV, as follows:

$$f_{RFout} = f_{VCO} / VCO_DIV \quad (3)$$

When this divider is enabled, there will be some far-out phase noise contribution to the VCO noise.

When changing to a VCO_DIV value of 4, either from a state of VCO_DIV=2 or OUTx_MUX = 0, it is necessary to program VCO_DIV first to a value of 6, then to a value of 4. This holds for no other VCO_DIV value and is not necessary if the VCO frequency (but not VCO_DIV) is changing.

8.3.10 0-Delay Mode

When the VCO divider is used, an ambiguous phase relationship is created between the OSCin and RFout pins. 0-Delay mode can be enabled to eliminate this ambiguity.

When this mode is used, special care needs to be taken because it does interfere with the VCO calibration if not done correctly. The correct way to use 0-Delay mode is as follows:

1. If N is not divisible by VCO_DIV, reduce the phase detector frequency to make it so.
2. Program as normal and lock the PLL.
3. Program the NO_FCAL =1.
4. Program 0_DLY = 1. This will cause the PLL to lose lock.
5. Program the PLL_N value with PLL_N^* / VCO_DIV , where PLL_N^* is the original value.
6. The PLL should now be locked in zero delay mode.

8.3.11 Programmable RF Output Buffers

The output states of the RFoutA and RFoutB pins are controlled by the BUFEN pin as well as the BUFEN_DIS programming bit. If the pin is powered up, then output power can be programmed to various levels with the OUTx_PWR words.

Table 6. Output States of the RFoutA and RFoutB Pins

OUTA_PD OUTB_PD	BUFEN_DIS	BUFEN PIN	OUTPUT STATE
1	X	X	Powered Down
0	0	X	Powered Up
	1	Low	Powered Down
		High	Powered Up

8.3.11.1 Choosing the Proper Pullup Component

The first decision is to whether to use a resistor or inductor for a pullup.

- The resistor pullup involves placing a 50 Ω resistor to the power supply on each side, which makes the output impedance easy to match and close to 50 Ω . However, it is a higher current for the same output power, and the maximum possible output power is more limited. For this method, the OUTx_PWR setting should be kept about 30 or less (for a 3.3-V supply) to avoid saturation. The resistive pullup is also sometimes more desirable when the output frequency is lower.
- The inductor pullup involves placing an inductor to the power supply. This inductor should look like high impedance at the frequency of interest. This method offers higher output power for the same current and higher maximum output power. The output power is about 3 dB higher for the same OUTx_PWR setting than the resistor pullup. Since the output impedance will be very high and poorly matched, it is recommended to either keep traces short or to AC couple this into a pad for better impedance matching.

If an output is partially used or unused:

- If the output is unused, then power it down in software. No external components are necessary.
- If only one side of the differential output is used, include the pullup component and terminate the unused side, such that the impedance as seen by this pin looks similar to the impedance as seen by the used side.

8.3.11.2 Choosing the Best Setting for the RFoutA_PWR and RFoutB_PWR Words

Table 7 shows the impact of the RFoutX_PWR word on the output power and current RELATIVE to a setting of RFoutX_PWR = 15. The choice of pullup component has an impact on the output power, but not much impact on the output current. The relative noise floor measurements are made without the VCO divider engaged.

Table 7. Impact of the RFoutX_PWR Word on the Output Power and Current

OUTx_PWR	RELATIVE CURRENT (mA)	RESISTIVE PULLUP		INDUCTOR PULLUP	
		RELATIVE OUTPUT POWER (dB)	RELATIVE NOISE FLOOR (dB)	RELATIVE OUTPUT POWER (dB)	RELATIVE NOISE FLOOR (dB)
0	-16	- 9.0	+ 4.0	- 9.0	+ 2.5
5	- 11	- 4.6	+ 0.7	- 4.6	+ 0.5
10	- 5	-2.0	+ 0.9	-2.0	- 0.1
15	0	0	0	0	0
20	+ 5	+ 1.4	+ 0.7	+ 1.5	- 0.6
25	+10	+ 2.1	+ 1.6	+ 2.8	- 1.1
30	+15	+ 2.4	+ 1.6	+ 3.9	- 1.0
35	+20	+ 2.2	+ 1.6	+ 4.8	- 0.9
40	+25	+ 1.9	+ 3.2	+ 5.4	+ 0.2
45	+30	+ 1.4	+ 5.6	+6.0	+ 2.0

For a resistive pullup, a setting of 15 is optimal for noise floor and a setting if 30 is optimal for output power. Settings above 30 are generally not recommended for a resistive pullup. For an inductor pullup, a setting of 30 is optimal for noise floor and a setting of 45 is optimal for output power. These settings may vary a little based on output frequency, supply voltage, and loading of the output, but the above table gives a fairly close indication of what performance to expect.

8.3.12 Fastlock

The LMX2581E includes the Fastlock feature that can be used to improve the lock times. When the frequency is changed, a timeout counter is used to engage the Fastlock for a programmable amount of time. During the time the device is in Fastlock, the FLout pin changes from high impedance to low, thus switching in the external resistor R2pLF in parallel with R2_LF.

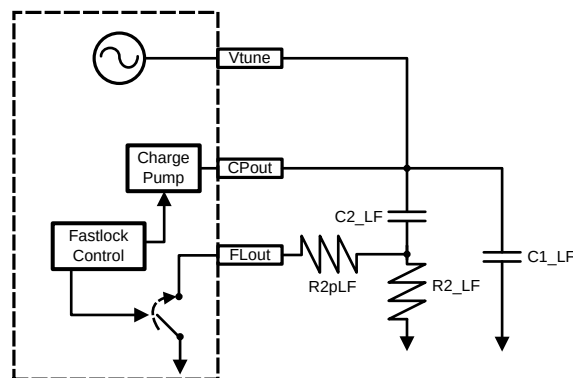


Table 8. Normal Operation vs. Fastlock

PARAMETER	NORMAL OPERATION	FASTLOCK
Charge Pump Gain	CPG	FL_CPG
FLout Pin	High Impedance	Grounded

Once the loop filter values and charge pump gain are known for normal operation, they can be determined for Fastlock operation as well. In normal operation, one can not use the highest charge pump gain and still use Fastlock because there will be no larger current to switch in. The resistor and the charge pump current are changed simultaneously so that the phase margin remains the same while the loop bandwidth is multiplied by a factor of K as shown in Table 9:

Table 9. Fastlock Configuration

PARAMETER	SYMBOL	CALCULATION
Charge Pump Gain in Fastlock	FL_CPG	Typically use the highest value.
Loop Bandwidth Multiplier	K	$K = \sqrt{FL_CPG / CPG}$
External Resistor	R2pLF	$R2 / (K - 1)$

8.3.13 Lock Detect

The LMX2581E offers two circuits to detect lock, Vtune and Digital Lock Detect, which may be used separately or in conjunction. Digital Lock Detect gives a reliable indication of lock/unlock if programmed correctly with the one exception, which occurs when the PLL is locked to a valid OSCin signal and then the OSCin signal is abruptly removed. In this case, digital lock detect can sometimes still indicate a locked state, but Vtune Lock detect will correctly indicate an unlocked state. Therefore, for the most reliable lock detect, it is recommended to use these in conjunction, because each technique's drawback is covered by the other one. Note that because the powerdown mode powers down the lock detect circuitry, it is possible to get a high lock detect indication when the device is powered down. The details of the two respective methods are described below in the [Vtune Lock Detect](#) and [Digital Lock Detect \(DLD\)](#) sections.

8.3.13.1 Vtune Lock Detect

This style of lock detect only works with the internal VCO. Whenever the tuning voltage goes below the threshold of about 0.5 V, or above the threshold of about 2.2 V, the internal VCO will become unlocked and the Vtune lock detect will indicate that the device is unlocked. For this reason, when the Vtune lock detect says the PLL is unlocked, one can be certain that it is unlocked.

8.3.13.2 Digital Lock Detect (DLD)

This lock detect works by comparing the phase error as presented to the phase detector. If the phase error plus the delay as specified by the PFD_DLY word outside the tolerance as specified by DLD_TOL, then this comparison would be considered to be an error, otherwise passing. At higher phase detector frequencies, it may be necessary to adjust the DLD_ERR_CNT and DLD_PASS_CNT. The DLD_ERR_CNT specifies how many errors are necessary to cause the circuit to consider the PLL to be unlocked. The DLD_PASS_CNT multiplied by 8 specifies how many passing comparisons are necessary to cause the PLL to be considered to be locked and also resets the count for the errors. The DLD_ERR_CNT and DLD_PASS_CNT values may be decreased to make the circuit more sensitive, but if lock detect is made too sensitive, chattering can occur and these values should be increased.

8.3.14 Part ID and Register Readback

8.3.14.1 Uses of Readback

The LMX2581E allows any of its registers to be read back, which could be useful for the following applications below.

- Register Readback
 - By reading back the register values, it can be confirmed that the correct information was written. In addition to this, Register R6 has special diagnostic information that could potentially be useful for debugging problems.
- Part ID Readback
 - By reading back the part ID, this information may be used by whatever device is programming the LMX2581E to identify this device and know what programming information to send. In addition to this, the BUFEN and CE pins may be used to create 4 unique part ID values. Although these pins can impact the device, they may be overridden in software. It is not necessary to have the device programmed in order to do part ID Readback.

The procedure for doing this Readback is in [Serial Timing for Readback](#). Depending on the settings for the ID(R0[31]) and RDADDR (R6[8:5]), information a different bit stream will be returned as shown in [Table 10](#).

Table 10. Uses of Readback

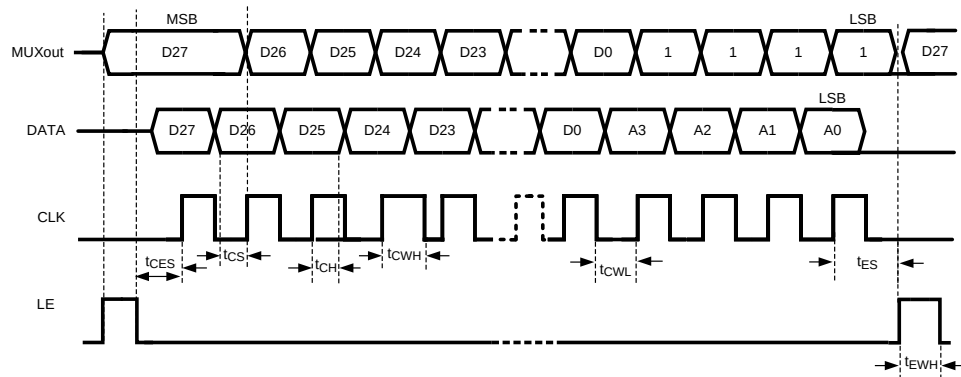
ID	BUFEN PIN	CE PIN	READBACK CODE
0	X	X	Readback register defined by RDADDR.
1	0	0	0x 00000500
	0	1	0x 00000510
	1	0	0x 00000520
	1	1	0x 00000530

8.3.14.2 Serial Timing for Readback

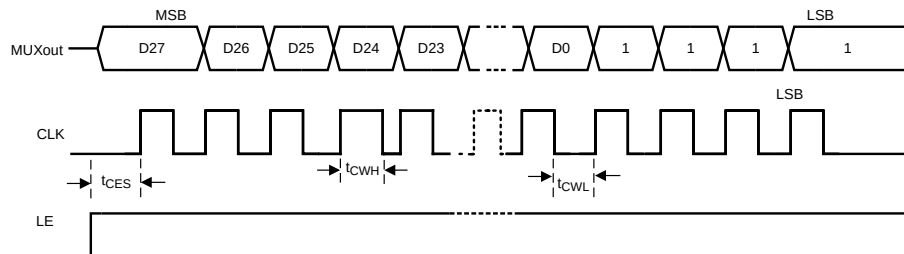
Readback is done through the the MUXout (or LD) pin with the same clock that is used to clock in the data.

- Choose either the MUXout (or LD) pin for reading back data and program the MUXOUT_SELECT (or LD_SELECT) to readback mode.
- Bring the LE pin from low to high to start the readback at the MSB.
- After the signal to the CLK pin goes high, the data will be ready at the readback pin 10 ns afterwards. It is recommended to read back the data on the falling edge of the clock. Technically, the first bit actually becomes ready after the rising edge of LE, but it still needs to be clocked out.
- The address being clocked out will all be 1's.

Because the CLK pin is both used to clock in data and clock out data, special care needs to be taken to ensure that erroneous data is not being clocked in during readback. There are two approaches to deal with this. The first approach is to actually send valid data during readback. For this approach, R6 is a recommended register and the approach is shown in [Figure 18](#):


Figure 18. Timing for Readback

A second approach is to hold LE high during readback so that the clock pulses do not clock data into the part, but still function for readback purposes. [Figure 19](#) demonstrates this method:


Figure 19. Timing for Readback, Holding LE High

8.3.15 Optimization of Spurs

The LMX2581E offers several programmable features for optimizing fractional spurs. In order to get the best out of these features, it makes sense to understand the different kinds of spurs as well as their behaviors, causes, and remedies. Although optimizing spurs may involve some trial and error, there are ways to make this process more systematic. Texas Instruments offers tools for information and tools for fractional spurs such as Application Note AN-1879 (

[AN-1879 Fractional N Frequency Synthesis](#)), [The Clock Design Tool](#), and this datasheet.

8.3.15.1 Phase Detector Spur

The phase detector spur occurs at an offset from the carrier equal to the phase detector frequency, f_{PD} . To minimize this spur, considering using a smaller value for PFD_DLY, smaller value for CPG_BLEED, and a lower phase detector frequency. In some cases where the loop bandwidth is very wide relative to the phase detector frequency, some benefit might be gained from using a narrower loop bandwidth or adding poles to the loop filter, but otherwise the loop filter has minimal impact. Bypassing at the supply pins and board layout can also have an impact on this spur, especially at higher phase detector frequencies.

8.3.15.2 Fractional Spur - Integer Boundary Spur

This spur occurs at an offset equal to the difference between the VCO frequency and the closest integer channel for the VCO. For instance, if the phase detector frequency is 100 MHz and the VCO frequency was 2703 MHz, then the integer boundary spur would be at 3 MHz offset. This spur can be either PLL or VCO dominated. If it is PLL dominated, then the following table shows that decreasing the loop bandwidth and some of the programmable fractional words may impact this spur. If the spur is VCO dominated, then reducing the loop filter will not help, but rather reducing the phase detector and having a good slew rate and signal integrity at the OSCin pin will help. Regardless of whether it is PLL or VCO dominated, the VCO core does impact this spur.

Table 11. Typical Integer Boundary Spur Levels

VCO CORE	FRACTIONAL INTEGER BOUNDARY SPURS			
	PLL DOMINATED		VCO DOMINATED	
	InBandSpur Metric	FORMULA	VCOXtalkSpur METRIC	FORMULA
VCO 1	-33	$\text{InBandSpur} + \text{PLL_Transfer_Function}(\text{Offset}) - 20 \times \log(\text{VCO_DIV})$	-89	$\text{VCOXtalkSpur} + \text{VCO_Transfer_Function}(\text{Offset}) + 20 \times \log(f_{PD}) - 20 \times \log(\text{Offset} / 1\text{MHz})$
VCO 2	-25		-83	
VCO 3	-37		-99	
VCO 4	-34		-87	

It is common practice to benchmark a fractional PLL spurs by choosing a worst case VCO frequency and use this as a metric. However, one should be cautious that this is only a metric for the integer boundary spur. For instance, suppose that one was to compare two devices by using an 100 MHz phase detector frequency, tune the VCO to 2000.001 MHz, and measure the integer boundary spur at 1 kHz. If one part was to have better spurs at this frequency, this does not necessarily mean that the spurs would be better at a channel farther from an integer boundary, like 2025.001 MHz.

8.3.15.3 Fractional Spur - Primary Fractional Spurs

These spurs occur at multiples of $f_{PD} / \text{PLL_DEN}$ and are not the integer boundary spur. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, the primary fractional spurs would be at 1,2,4,5,6,...MHz. These are impacted by the loop filter bandwidth and modulator order. If a small frequency error is acceptable, then a larger equivalent fraction may improve these spurs. For instance, if the fraction is 53/200, expressing this as 530,000 / 2,000, 001. This larger un-equivalent fraction pushes the fractional spur energy to much lower frequencies that hopefully is not so critical.

8.3.15.4 Fractional Spur - Sub-Fractional Spurs

These spurs appear at a fraction of f_{PD} / PLL_DEN and depend on modulator order. With the first order modulator, there are no sub-fractional spurs. The second order modulator can produce 1/2 sub-fractional spurs if the denominator is even. A third order modulator can produce sub-fractional spurs at 1/2, 1/3, or 1/6 of the offset, depending if it is divisible by 2 or 3. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, no sub-fractional spurs for a first order modulator or sub-fractional spurs at multiples of 1.5 MHz for a 2nd or 3rd order modulator would be expected.

Aside from strategically choosing the fractional denominator and using a lower order modulator, another tactic to eliminate these spurs is to use dithering and express the fraction in larger equivalent terms (that is, 1000000/4000000 instead of 1/4). If a small frequency error is acceptable, also consider a larger un-equivalent fraction like (1000000,4000000). However, dithering can also add phase noise, so if dithering is used, this needs to be managed with the various levels it has and the PFD_DLY word to get the best possible performance.

8.3.15.5 Summary of Spurs and Mitigation Techniques

Table 12 gives a summary of the spurs discussed so far and techniques to mitigate them.

Table 12. Spurs and Mitigation Techniques

SPUR TYPE	OFFSET	WAYS to REDUCE	TRADE-OFF
Phase Detector	f_{PD}	1. Reduce Phase Detector Frequency 2. Decrease PFD_DLY 3. Decrease CPG_BLEED	Although reducing the phase detector frequency does improve this spur, it also degrades phase noise.
Integer Boundary	$f_{VCO} \bmod f_{PD}$	Methods for PLL Dominated Spurs 1. Avoid the worst case VCO frequencies if possible. 2. Strategically choose which VCO core to use if possible. 3. Ensure good slew rate and signal integrity at the OSCin pin 4. Reduce the loop bandwidth or add more filter poles for out of band spurs 5. Experiment with modulator order, PFD_DLY, and CPG_BLEED	Reducing the loop bandwidth may degrade the total integrated noise if the bandwidth is too narrow.
		Methods for VCO Dominated Spurs 1. Avoid the worst case VCO frequencies if possible. 2. Strategically choose which VCO core to use if possible. 3. Reduce Phase Detector Frequency 4. Ensure good slew rate and signal integrity at the OSCin pin 5. Make the impedance looking outwards from the OSCin pin close to 50 Ω.	Reducing the phase detector may degrade the phase noise and also reduce the capacitance at the Vtune pin.
Primary Fractional	f_{PD} / PLL_DEN	1. Decrease Loop Bandwidth 2. Change Modulator Order 3. Use Larger Un-equivalent Fractions	Decreasing the loop bandwidth too much may degrade in-band phase noise. Also, larger un-equivalent fractions only sometimes work
Sub-Fractional	$f_{PD} / PLL_DEN / k$ k=2,3, or 6	1. Use Dithering 2. Use Larger Equivalent Fractions 3. Use Larger Un-equivalent Fractions 4. Reduce Modulator Order 5. Eliminate factors of 2 or 3 in denominator (see AN-1879, SNAA062)	Dithering and larger fractions may increase phase noise.

8.4 Device Functional Modes

8.4.1 Full Synthesizer Mode

In this mode, the internal VCO is enabled. When combined with an external reference and loop filter, this mode provides a complete signal source.

8.4.2 External VCO Mode

The LMX2581E allows the user to use an external VCO by using the Fin pin and selecting the external VCO mode for the MODE word. Because this is software selectable, the user may have a setup that switches between the external and internal VCO. Because the Fin pin is close to the RFoutA and RFoutB pins, some care needs to be taken to minimize board crosstalk when both an external VCO and an output buffer is used. If only one output buffer is required, it is recommended to use the RFoutB output because it is physically farther from the Fin pin and therefore will have less board related crosstalk. When using external VCO with a different characteristic, it may be necessary to change the phase detector polarity (CPP).

8.4.3 Powerdown Modes

The LMX2581E can be powered down either fully or partially with the PWDN_MODE word or the CE pin. The two types of powerdown are in the following table.

Table 13. LMX2581E Powerdown Modes

POWERDOWN STATE	DESCRIPTION
Partial Powerdown	VCO, PLL, and Output buffers are powered down, but the LDOs are kept powered up to reduce the time it takes to power the device back up.
Full Powerdown	VCO, PLL, Output Buffers, and LDOs are all powered down.

When coming out of a full powerdown state, it is necessary to do the initial power-on programming sequence described in later sections. If coming out of a partial powerdown state, it is necessary to do the sequence for switching frequencies after initialization, that is described in later sections.

8.5 Programming

The LMX2581E is programmed using several 32-bit registers. A 32-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last LSB bits, ADDR[3:0], form the address field, which is used to decode the internal register address. The remaining 28 bits form the data field DATA[27:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank.

8.5.1 Serial Data Input Timing

There are several programming considerations (see [Figure 20](#)):

- A slew rate of at least 30 V/us is recommended for the CLK, DATA, and LE signals
- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter.
- The LE pin may be held high after programming and this will cause the LMX2581E to ignore clock pulses.
- The CLK signal should not be high when LE transitions to low.
- When CLK and DATA lines are shared between devices, it is recommended to divide down the voltage to the CLK, DATA, and LE pins closer to the minimum voltage. This provides better noise immunity.
- If the CLK and DATA lines are toggled while the in VCO is in lock. As is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

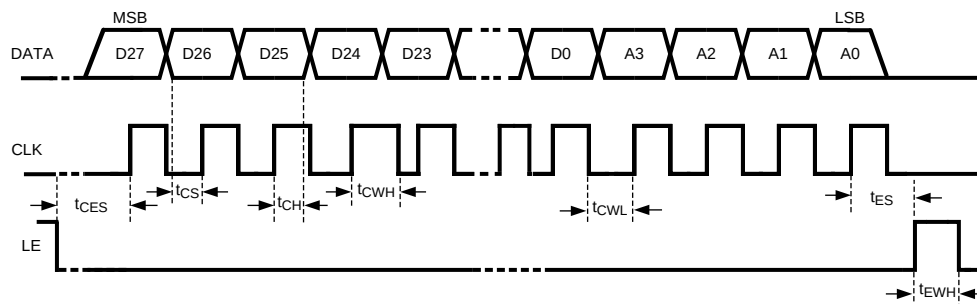


Figure 20. Serial Data Input Timing

8.5.2 Recommended Initial Power on Programming Sequence

When the device is first powered up, the device needs to be initialized and the ordering of this programming is very important. After the following sequence is complete, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure the Vcc pins are at the proper levels.
2. Ensure that a valid reference is applied to the OSCin pin
3. Program register R5 with RESET (R5[4]) =1
4. Program registers R15,R13,R10,R9,R8,R7,R6,R5,R4,R3,R2,R1, and R0
5. Wait 20 ms
6. Program the R0 register again OR do the recommended sequence for changing frequencies.

8.5.3 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. (optional) If the OUTx_MUX State is changing, program Register R5
2. (optional) If the VCO_DIV state is changing, program Register R3. See [VCO_DIV\[4:0\] — VCO Divider Value](#) if programming a to a value of 4.
3. (optional) If the MSB of the fractional numerator or charge pump gain is changing, program register R1
4. (Required) Program register R0

Although not necessary, it is also acceptable to program the R0 register a second time after this programming sequence. It is not necessary to program the initial power on sequence to change frequencies.

Programming (continued)

8.5.4 Triggering Registers

The action of programming certain registers may trigger special actions as shown in [Table 14](#).

Table 14. Triggering Registers

REGISTER	CONDITIONS	ACTIONS TRIGGERED	WHY THIS IS DONE
R5	RESET = 1	All Registers are reset to power on default values. This takes less than 1 us. The reset bit is self-clearing.	The registers are reset by the power on reset circuitry when power is initially applied. The RESET bit allows the user the option to perform the same functionality of the power-on reset through software.
R0	NO_FCAL = 0	—Starts the Frequency Calibration —Engages Fastlock (If FL_TOC>0)	This activates the frequency calibration, which chooses the correct VCO core and also the correct frequency band within that core. This is necessary whenever the frequency is changed. If it is desired that the R0 register be programmed without activating this calibration, then the NO_FCAL bit can be set to zero. If the fastlock timeout counter is programmed to a nonzero value, then this action also engages fastlock.
R0	NO_FCAL = 1	—Engages Fastlock (If FL_TOC>0)	This engages fastlock, which may be used to decrease the lock time in some circumstances.

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8.6 Register Maps
Table 15. Register Map

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[27:0]																												ADDRESS[3:0]			
R15	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	VCO CAP MAN	VCO_CAPCODE[7:0]								1	1	1	1
R13	DLD_ERR_CNT[3:0]				DLD_PASS_CNT[9:0]										DLD_TOL [2:0]		1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1
R10	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	0	0	1	0	1
R9	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1
R8	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0
R7	0	FL_SELECT [4:0]					FL_PINMODE [2:0]			FL_INV	MUXOUT_SELECT [4:0]				MUX_INV	MUXOUT_PINMODE [2:0]		LD_SELECT [4:0]				LD_INV	LD_PINMODE[2:0]			0	1	1	1			
R6	0	RD_DIAGNOSTICS[19:0]																				1	0	RDADDR[3:0]			uWIRE_LOC_K	0	1	1	0	
R5	0	0	0	0	0	0	0	OUT_LD_EN	OSC_FREQ[2:0]			BUF_EN_DIS	0	0	0	VCO_SEL_MODE [1:0]	OUTB_MUX [1:0]	OUTA_MUX [1:0]	0_DLY	MODE [1:0]	PWDN_MODE [2:0]		RESET	0	1	0	1					
R4	PFD_DLY [2:0]			FL_FRC_E	FL_TOC[11:0]										FL_CPG[4:0]				0	CPG_BLEED[5:0]					0	1	0	0				
R3	0	0	1	0	0	0	0	0	0	VCO_DIV[4:0]					OUTB_PWR[5:0]				OUTA_PWR[5:0]					OUTB_PD	OUTA_PD	0	0	1	1			
R2	0	0	OSC_2X	0	CPP	1	PLL_DEN[21:0]																					0	0	1	0	
R1	CPG[4:0]					VCO_SEL [1:0]		PLL_NUM[21:12]								FRAC_ORDER [2:0]			PLL_R[7:0]							0	0	0	1			
R0	ID	FRAC_DITHER [1:0]		NO_FCAL	PLL_N[11:0]										PLL_NUM[11:0]													0	0	0	0	

8.6.1 Programming Word Descriptions

8.6.1.1 Register R15

The programming of register R15 is only necessary when one wants to change the default value of VCO_CAPCODE for improving the VCO calibration time or use the VCO_CAP_MAN bit for diagnostic purposes.

8.6.1.1.1 VCO_CAP_MAN — Manual VCO Band Select

This bit determines if the value of VCO_CAPCODE is just used as a starting point for the initial frequency calibration or if the VCO is forced to this value. If this is forced, it is only for diagnostic purposes.

VCO_CAP_MAN	IMPACT of VCO_CAPCODE
0	VCO_CAPCODE value is initial starting point for VCO digital calibration.
1	VCO_CAPCODE value is forced all the time. For diagnostic purposes only.

8.6.1.1.2 VCO_CAPCODE[7:0] — Capacitor Value for VCO Band Selection

This word selects the VCO tank capacitor value that is initially used when VCO calibration is run or that is forced when VCO_CAP_MAN is set to one. The lower values correspond to less capacitance, which corresponds to a higher VCO frequency for a given VCO Core. If this word is not programmed, it is defaulted to 128.

VCO_CAPCODE	VCO TANK CAPACITANCE	VCO FREQUENCY
0	Minimum	Highest
...	...	...
255	Maximum	Lowest

8.6.1.2 Register R13

Register R13 gives access to words that are used for the digital lock detect circuitry.

8.6.1.2.1 DLD_ERR_CNT[3:0] - Digital Lock Detect Error Count

This is the amount of phase detector comparisons that may exceed the tolerance as specified in DLD_TOL before digital lock indicates an unlocked state. The recommended default is 4 for phase detector frequencies of 80 MHz or below; higher frequencies may require the user to experiment to optimize this value.

8.6.1.2.2 DLD_PASS_CNT[9:0] - Digital Lock Detect Success Count

This value multiplied by 8 is the amount of phase detector comparison within the tolerance specified by DLD_TOL and adjusted by DLD_ERR_CNT that are necessary to cause the digital lock to indicate a locked state. The recommended value is 32 for phase detector frequencies of 80 MHz or below; higher frequencies may require the user to experiment and optimize this value based on application.

8.6.1.2.3 DLD_TOL[2:0] — Digital Lock Detect

This is the tolerance that is used to compare with each phase error to decide if it is a success or a fail. Larger settings are generally recommended, but they are limited by several factors such as PFD_DLY, modulator order, and especially the phase detector frequency.

DLD_TOL	PHASE ERROR TOLERANCE (ns)	TYPICAL PHASE DETECTOR FREQUENCY
0	1	Fpd > 130 MHz
1	1.7	80 MHz < Fpd ≤ 130 MHz
2	3	60 MHz < Fpd ≤ 80 MHz
3	6	45 MHz < Fpd ≤ 60 MHz
4	10	30 MHz < Fpd ≤ 45 MHz
5	18	Fpd ≤ 30 MHz
6–7	Reserved	n/a

8.6.1.3 Registers R10, R9, and R8

These registers control functions that are not disclosed to the user and the power on default values are not optimal. Therefore these registers need to be programmed to the values specified in the register map for proper operation.

8.6.1.4 Register R7

This register has words that control status pins, which would be LD, MUXout, and FLout

8.6.1.4.1 FL_PINMODE[2:0], MUXOUT_PINMODE[2:0], and LD_PINMODE[2:0] — Output Format for Status Pins

These words control the state of the output pin.

FL_PINMODE MUXOUT_PINMODE LD_PINMODE	OUTPUT TYPE
0	TRI-STATE (Default for LD_PINMODE)
1	Push-Pull (Default for MUXOUT_PINMODE)
2	Open Drain
3	High Drive Push-Pull (Can drive 5 mA for an LED)
4	High Drive Open Drain
5	High Drive Open Source
6,7	Reserved

8.6.1.4.2 FL_INV, MUX_INV, LD_INV - Inversion for Status Pins

The logic for the LD and MUXOUT pins can be inverted with these bits.

FL_INV MUX_INV LD_INV	PIN STATUS
0	Normal Operation
1	Inverted

8.6.1.4.3 FL_SELECT[4:0], MUXOUT_SELECT[4:0], LD_SELECT[4:0] — State for Status Pins

This word controls the output state of the MUXout, LD, and FLout pins. Note that during fastlock, the FL_SELECT word is ignored.

FL_SELECT MUXOUT_SELECT LD_SELECT	OUTPUT
0	GND
1	Digital Lock Detect (Based on Phase Measurement)
2	Vtune Lock Detect (Based on tuning voltage)
3	Lock Detect (Based on Phase Measurement AND tuning voltage)
4	Readback (Default for MUXOUT_SELECT)
5	PLL_N divided by 2
6	PLL_N divided by 4
7	PLL_R divided by 2
8	PLL_R divided by 4
9	Analog Lock Detect
10	OSCin Detect
11	Fin Detect
12	Calibration Running
13	Tuning Voltage out of Range
14	VCO calibration fails in the low frequency direction.
15	VCO Calibration fails in the high frequency direction.
16-31	Reserved

8.6.1.5 Register R6

8.6.1.5.1 RD_DIAGNOSTICS[19:0] — Readback Diagnostics

This word contains several pieces of information that may be read back for debug and diagnostic purposes.

RD_DIAGNOISTICS[19:8]								
19	18	17	16	15	[14:11]	10	9	8
VCO_SELECT	FIN_DETECT	OSCIN_DETECT	VCO_DETECT	Reserved		CAL_RUNNING	VCO_RAIL_HIGH	VCO_RAIL_LOW

RD_DIAGNOISTICS[7:0]							
7	6	5	4	3	2	1	0
Reserved	VCO_TUNE_HIGH	VCO_TUNE_VALID	FLOUT_ON	DLD	LD_PIN STATE	CE_PIN STATE	BUFEN_PIN STATE

WORD NAME	MEANING if VALUE is ONE
VCO_SELECT	This is the VCO that the device chose to use. 0 = VCO 1, 1 = VCO 2, 2 = VCO 3, 3 = VCO 4
FIN_DETECT	Indicates transitions at the Fin pin have been detected. This could either be the VCO signal or self-oscillation of the Fin pin in the event that no signal is present. This bit needs to be manually reset by programming register R5 with R5[30] = 1, and then again with bit R5[30]=0
OSCIN_DETECT	Indicates transitions at the OSCin pin have been detected. This could either be a signal at the OSCin pin or self-oscillation at the OSCin pin in the event no signal is present. This bit needs to be manually reset by programming R5 with R5[29] = 1 and then again with R5[29] = 0.
CAL_RUNNING	Indicates that some calibration in the part is currently running.
VCO_RAIL_HIGH	Indicates that the VCO frequency calibration failed because the VCO would need to be a higher frequency than it could achieve.
VCO_RAIL_LOW	Indicates that the VCO frequency calibration failed because the VCO would need to be a lower frequency than it could achieve.
VCO_TUNE_HIGH	Indicates that the VCO tuning voltage is higher than 2.4 volts and outside the allowable range.
VCO_TUNE_VALID	Indicates that the VCO tuning voltage is inside then allowable range.
FLOUT_ON	Indicates that the FLOut pin is low.
DLD	Indicates that the digital lock detect phase measurement indicates a locked state. This does not include any consideration of the VCO tuning voltage.
LD_PINSTATE	This is the state of the LD Pin.
CE_PINSTATE	This is the state of the CE pin.
BUFEN_PINSTATE	This is the state of the BUFEN pin.

8.6.1.5.2 RDADDR[3:0] — Readback Address

When the ID bit is set to zero, this word designates which register is read back from. When the ID bit is set to one, the unique part ID identifying the device as the LMX2581E is read back.

ID	RDADDR	INFORMATION READ BACK
1	Don't Care	Part ID
0	0	Register R0
	1	Register R1
	...	...
	15 (default)	Register R15

8.6.1.5.3 uWIRE_LOCK - Microwire lock

uWIRE_LOCK	MICROWIRE
0	Normal Operation
1	Locked out – All Programming except to the uWIRE_LOCK bit is ignored

8.6.1.6 Register R5

8.6.1.6.1 OUT_LDEN — Mute Outputs Based on Lock Detect

When this bit is enabled, the RFoutA and RFoutB pins are disabled if the PLL digital lock detect circuitry indicates that the PLL is in the unlocked state.

OUT_LDEN	PLL DIGITAL LOCK DETECT STATUS	RFoutA / RFoutB PINS
0	Don't Care	Normal Operation
1	Locked	Normal Operation
1	Unlocked	Powered Down

8.6.1.6.2 OSC_FREQ[2:0] — OSCin Frequency for VCO Calibration

This word should be set to in accordance to the OSCin frequency BEFORE the doubler. It is critical for running internal calibrations for this device.

OSC_FREQ	OSCin FREQUENCY
0	$f_{\text{OSCin}} < 64 \text{ MHz}$
1	$64 \leq f_{\text{OSCin}} < 128 \text{ MHz}$
2	$128 \leq f_{\text{OSCin}} < 256 \text{ MHz}$
3	$256 \leq f_{\text{OSCin}} < 512 \text{ MHz}$
4	$512 \leq f_{\text{OSCin}}$
≥ 5	Reserved

8.6.1.6.3 BUFEN_DIS - Disable for the BUFEN Pin

This pin allows the BUFEN pin to be disabled. This is useful if one does not want to pull this pin high or use it for the readback ID.

BUFEN_DIS	BUFEN PIN
0	Impacts Output buffers
1	Ignored.

8.6.1.6.4 VCO_SEL_MODE — Method of Selecting Internal VCO Core

This word allows the user to choose how the VCO selected by the VCO_SEL word is treated. Note setting 0 should not be used if switching from a frequency above 3 GHz to a frequency below 2.2 GHz.

VCO_SEL_MODE	VCO SELECTION
0	VCO core is automatically selected based on the last one that was used. If none was used before, it chooses the lowest frequency VCO core.
1	VCO selection starts at the value as specified by the VCO_SEL word. However, if this is invalid, it will choose another VCO.
2	VCO is forced to the selection as defined by the VCO_SEL word, regardless of whether it is valid or not. Note that this mode is not ensured and is only included for diagnostic purposes.
3	Reserved

8.6.1.6.5 OUTB_MUX — Mux for RFoutB

This word determines whether RFoutB is the VCO frequency, the VCO frequency divided by VCO_DIV, or the fin frequency.

OUTB_MUX	RFoutB FREQUENCY
0	f_{VCO}
1	$f_{\text{VCO}} / \text{VCO_DIV}$
2	f_{Fin}
3	Reserved

8.6.1.6.6 OUTA_MUX — Mux for RFoutA

This word determines whether RFoutA is the VCO frequency, the VCO frequency divided by VCO_DIV, or the fin frequency.

OUTA_MUX	RFoutA FREQUENCY
0	f_{VCO}
1	f_{VCO} / VCO_DIV
2	f_{Fin}
3	Reserved

8.6.1.6.7 0_DLY - Zero Delay Mode

When this mode is enabled, the VCO divider is put in the feedback path of the PLL so that the delay from input to output of the device will be deterministic.

0_DLY	PHASE DETECTOR INPUT
0	Direct VCO or Fin signal.
1	Channel Divider output.

8.6.1.6.8 MODE[1:0] — Operating Mode

This word determines in what mode the device is run.

MODE	OPERATIONAL MODE	PLL	VCO	FIN PIN
0	Full Chip Mode	Powered Up	Powered Up	Powered Down
1	PLL Only Mode	Powered Up	Powered Down	Powered Down
2,3	Reserved	Reserved	Reserved	Reserved

8.6.1.6.9 PWDN_MODE - Powerdown Mode

This word powers the device up and down. Aside from the traditional power up and power down, there is the partial powerdown that powers down the PLL and VCO, but keeps the LDOs powered up to allow the device to power up faster.

PWDN_MODE	CE Pin	DEVICE STATUS
0	X	Powered Up
1	X	Full Powerdown
2	X	Reserved
3	X	Partial Powerdown
4	Low	Full Powerdown
	High	Powered Up
5	X	Reserved
6	Low	Partial Powerdown
	High	Powered Up
7	Low	Full Powerdown
	High	Partial Powerdown

8.6.1.6.10 RESET - Register Reset

When this bit is enabled, the action of programming register R5 resets all registers to their default power on reset status, otherwise the words in register 5 may be programmed without resetting all the registers.

RESET	ACTION of PROGRAMMING REGISTER R5
0	Registers and state machines are operational.
1	Registers and state machines are reset, then this reset is automatically released.

8.6.1.7 Register R4

8.6.1.7.1 PFD_DLY[2:0] — Phase Detector Delay

This word controls the minimum on time for the charge pump. The minimum setting often yields the best phase detector spurs and integer mode PLL phase noise. Higher settings may be useful in reducing the delta sigma noise of the modulator when dithering is enabled. These settings are not generally recommended if the phase detector frequency exceeds 130 MHz. If unsure, program this word to zero.

PFD_DLY	PULSE WIDTH	WHEN RECOMMENDED
0	370 ps	Default Use with a 2nd order modulator , when dithering is disabled, or when the phase detector frequency is >130 MHz.
1	760 ps	Consider these settings for a 3rd order modulator when dithering is used.
2	1130 ps	
3	1460 ps	
4	1770 ps	
5	2070 ps	
6	2350 ps	
7	2600 ps	

8.6.1.7.2 FL_FRCE — Force Fastlock Conditions

This bit forces the fastlock conditions on, provided that the FL_TOC word is greater than zero.

FL_FRCE	FASTLOCK TIMEOUT COUNTER	FASTLOCK
0	0	Disabled
	> 0	Fastlock engaged as long as timeout counter is counting down
1	0	Invalid State
	> 0	Always Engaged

8.6.1.7.3 FL_TOC[11:0] — Fastlock Timeout Counter

This word controls the timeout counter used for fastlock.

FL_TOC	FASTLOCK TIMEOUT COUNTER	COMMENTS
0	Disabled	Fastlock Disabled
1	2 x Reference Cycles	Fastlock engaged as long as timeout counter is counting down
2	2 x 2 x Reference cycles	
...		
4095	2 x 4095 x Reference cycles	

8.6.1.7.4 FL_CPG[4:0] — Fastlock Charge Pump Gain

This word determines the charge pump current that is active during fastlock.

FL_CPG	FASTLOCK CURRENT STATE
0	TRI-STATE
1	1X
2	2X
..	...
31	31X

8.6.1.7.5 CPG_BLEED[5:0]

The CPG bleed word is for advanced users who want to get the lowest possible integer boundary spur. The impact of this word is on the order of 2 dB. For users who do not care about this, the recommendation is to default this word to zero.

USER TYPE	FRAC_ORDER	CPG	CPG BLEED RECOMMENDATION
Basic User	X	X	0
Advanced User	< 2	X	0
	X	< 4X	0
	>1	$4X \leq \text{CPG} < 12X$	2
		$12X \leq \text{CPG}$	4

8.6.1.8 Register R3

8.6.1.8.1 VCO_DIV[4:0] — VCO Divider Value

This word determines the value of the VCO divider. Note that the this divider may be bypassed with the OUTA_MUX and OUTB_MUX words.

VCO_DIV	VCO DIVIDER VALUE
0	2
1	4
2	6
3	8
4	10
...	...
18	38
20 - 31	Invalid State

8.6.1.8.2 OUTB_PWR[5:0] — RFoutB Output Power

This word controls the output power for the RFoutB output.

OUTB_PWR	RFoutB POWER
0	Minimum
...	...
47	Maximum
48 – 63	Reserved

8.6.1.8.3 OUTA_PWR[5:0] — RFoutA Output Power

This word controls the output power for the RFoutA output.

OUTA_PWR	RFout POWER
0	Minimum
...	...
47	Maximum
48 – 63	Reserved.

8.6.1.8.4 OUTB_PD — RFoutB Powerdown

This bit powers down the RFoutB output.

OUTB_PD	RFoutB
0	Normal Operation
1	Powered Down

8.6.1.8.5 OUTA_PD — RFoutA Powerdown

This bit powers down the RFoutA output.

OUTA_PD	RFoutA
0	Normal Operation
1	Powered Down

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8.6.1.9 Register R2
8.6.1.9.1 OSC_2X — OSCin Doubler

This bit controls the doubler for the OSCin frequency.

OSC_2X	OSCin DOUBLER
0	Disabled
1	Enabled

8.6.1.9.2 CPP - Charge Pump Polarity

This bit sets the charge pump polarity. Note that the internal VCO has a negative tuning gain, so it should be set to negative gain with the internal VCO enabled.

CPP	CHARGE PUMP POLARITY
0	Positive
1	Negative (Default)

8.6.1.9.3 PLL_DEN[21:0] — PLL Fractional Denominator

These words control the denominator for the PLL fraction. Note that 0 is only permissible in integer mode.

PLL _DEN	PLL_DEN[21:0]																				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194 303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.6.1.10 Register R1

8.6.1.10.1 CPG[4:0] — PLL Charge Pump Gain

This word determines the charge pump current that used during steady state operation.

CPG	CHARGE PUMP CURRENT STATE
0	TRI-STATE
1	1X
2	2X
..	...
31	31X

Note that if the CPG setting is 400 μ A or lower, then the CPG_BLEED word needs to be set to 0.

8.6.1.10.2 VCO_SEL[1:0] - VCO Selection

These words allow the user to specify which VCO the frequency calibration starts at. If uncertain, program this word to 0 to start at the lowest frequency VCO core. A programming setting of 3 (VCO 4) should not be used if switching to a frequency below 2.2 GHz.

VCO_SEL	VCO SELECTION
0	VCO 1 (Lowest Frequency)
1	VCO 2
2	VCO 3
3	VCO 4 (Highest Frequency)

8.6.1.10.3 FRAC_ORDER[2:0] — PLL Delta Sigma Modulator Order

This word sets the order for the fractional engine.

FRAC_ORDER	MODULATOR ORDER
0	Integer Mode
1	1st Order Modulator
2	2nd Order Modulator
3	3rd Order Modulator
4-7	Reserved

8.6.1.10.4 PLL_R[7:0] — PLL R divider

This word sets the value that divides the OSCin frequency.

PLL_R	PLL_R DIVIDER VALUE
0	256
1	1 (bypass)
...	...
255	255

8.6.1.11 Register R0

Register R0 controls the frequency of the device. Also, unless disabled by setting NO_FCAL = 1, the action of writing to the R0 register triggers a frequency calibration for the internal VCO.

8.6.1.11.1 ID - Part ID Readback

When this bit is set, the part ID indicating the device is an LMX2581E is read back from the device. Consult the Feature Description for more details.

ID	READBACK MODE
0	Register
1	Part ID

8.6.1.11.2 FRAC_DITHER[1:0] — PLL Fractional Dithering

This word sets the dithering mode. When the fractional numerator is zero, it is recommended, although not required, to set the FRAC_DITHER mode to disabled for the best possible spurs. Doing this shuts down the fractional circuitry and eliminates fractional spurs for these frequencies. This is the reason why the FRAC_DITHER word is in the R0 register, so that it can be set correctly for every frequency if this setting changes.

FRAC_DITHER	DITHERING MODE
0	Weak
1	Medium
2	Strong
3	Disabled

8.6.1.11.3 NO_FCAL — Disable Frequency Calibration

Normally, when the R0 register is written to, a frequency calibration for the internal VCO is triggered. However, this feature may be disabled. If the frequency is changed, then this frequency calibration is necessary for the internal VCO.

NO_FCAL	VCO FREQUENCY CALIBRATION
0	Done upon write to R0 Register
1	Not done on write to R0 Register

8.6.1.11.4 PLL_N - PLL Feedback Divider Value

This is the feedback divider value for the PLL. There are some restrictions on this depending on the modulator order.

PLL_N	PLL_N[11:0]											
<7	Invalid state											
7	Possible only in integer mode or with a 1st order modulator											
8-9	Possible in integer mode, 1st order modulator, or 2nd order modulator											
10-13	Possible only in integer mode, 1st order modulator, 2nd order modulator, or 3rd order modulator											
14	0	0	0	0	0	0	0	0	1	1	1	0
...	...	...	...	...	...	...	...	...	...	...	...	...
4095	1	1	1	1	1	1	1	1	1	1	1	1

8.6.1.11.5 PLL_NUM[21:12] and PLL_NUM[11:0] — PLL Fractional Numerator

These words control the numerator for the PLL fraction.

PLL NUM	PLL_NUM[21:12]										PLL_NUM[11:0]											
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	
4095	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	
4194 303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMX2581E can be used in a broad class of applications. In general, they tend to fall in the categories where the output frequency is a nicely related input frequency and those that require fractional mode. The following schematic generally applies to most applications.

9.2 Typical Applications

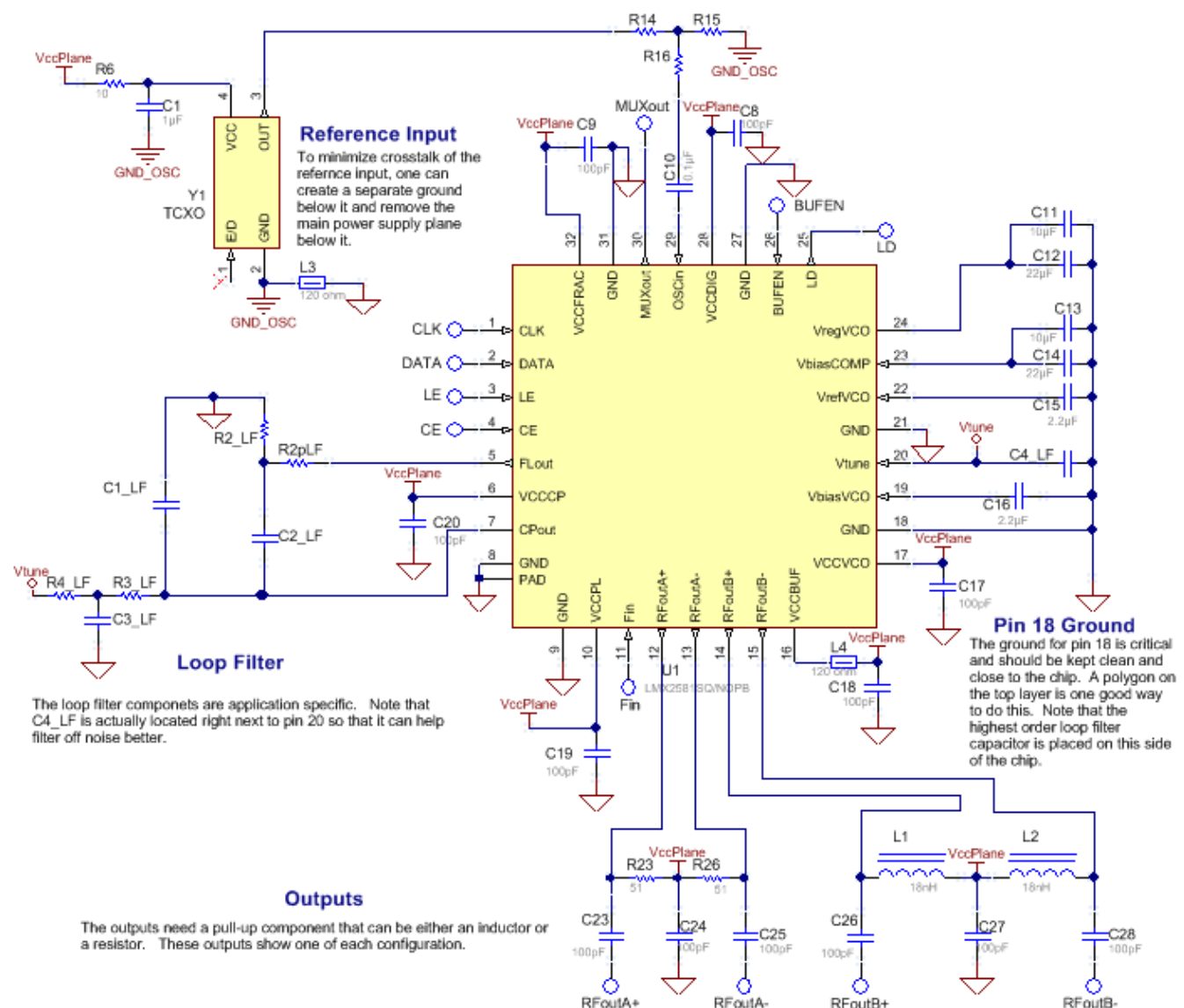


Figure 21. Typical Schematic

Typical Applications (continued)

9.2.1 Clocking Application

When the output and input frequencies are nicely related, the LMX2581E can often achieve this in integer mode. In integer mode, fractional spurs and noise are much less of a concern, so higher phase detector frequency and wider loop bandwidth are typically used for optimal phase noise performance.

9.2.1.1 Design Requirements

For this example, consider a design for a fixed 1500 MHz output clock to be generated from a 100 MHz input clock. Good close in phase noise and maximizing the output power are desired in this particular example

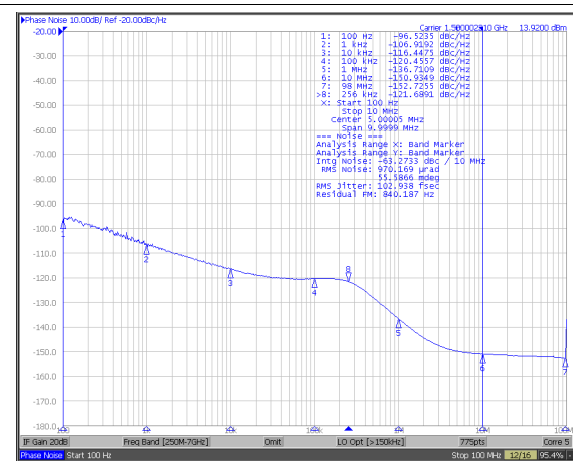
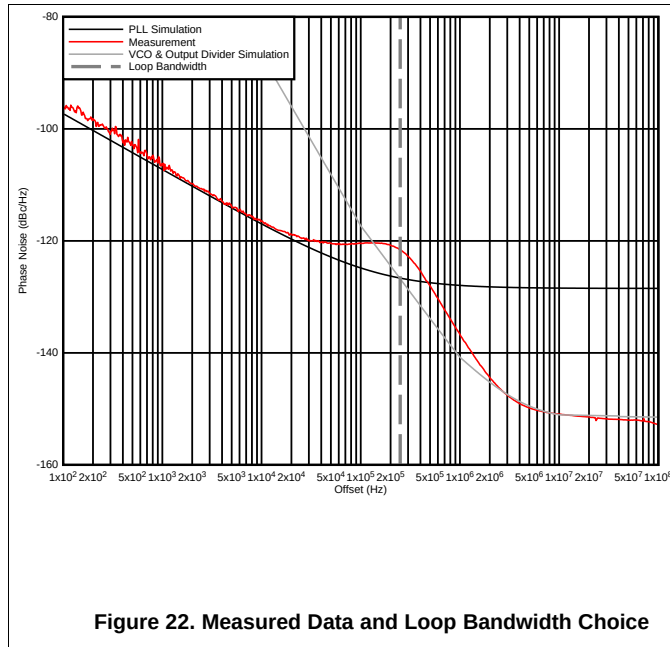
9.2.1.2 Detailed Design Procedure

For this kind of application, the design goal is typically to minimize the jitter.

PARAMETER	VALUE	REASON for CHOOSING
Fout	1500 MHz	This parameter was given.
Fosc	100 MHz	This parameter was given.
Fpd	200 MHz	Choose a highest possible phase detector frequency. There are no fractional spurs and this increases the value of C1
Fvco	3000 MHz	The VCO needs to be a multiple of 1500 MHz, which restricts it to be 3000 MHz.
Kpd	31x	This maximizes the C1 capacitor and also the phase noise
Loop Bandwidth	256 kHz	Theoretically, optimal jitter is obtained by choosing the loop bandwidth to the frequency where the open loop PLL and closed loop VCO noise are equal, which would be about 250 kHz. The phase margin is typically chosen around 70 degrees, but is chosen to be 50 degrees to increase the value of the C1 capacitor to be at least 1 nF to reduce VCO phase noise degradation.
Phase Margin	50 deg	
OUT_A_PWR	45	This yields the maximum output power.
C1	1 nF	Calculated with TI clock design software
C2	6.8 nF	
R2	270 Ω	
Pullup Component	18 nH Inductor	This gives maximum output power.

9.2.1.3 Application Curves

Figure 22 is an example of the performance that one might see for an application like this. The achieved results show an output power of about 14 dBm (single-ended) and a jitter from 100 Hz to 10 MHz of 100 fs. Note that the output power is higher than +12 dBm as claimed in the electrical specifications because this is at a lower frequency than 2.7 GHz.



9.2.2 Fractional PLL Application

For applications where the output frequency is not always related nicely to the input frequency, lowering the loop bandwidth and reducing the phase detector frequency can often improve spurs at the cost of in-band phase noise.

9.2.2.1 Design Requirements

Consider generating 1880 to 3800 MHz from a 100 MHz input frequency with a channel spacing of 200 kHz. This is the situation similar that was used for the EVM board.

9.2.2.2 Detailed Design Procedure

PARAMETER	VALUE	REASON for CHOOSING
Fout	1880 - 3800 MHz	This parameter was given.
Fosc	100 MHz	This parameter was given.
Fpd	25 MHz	By trial and error and experimenting with the clock design tool, we see that this gives a good trade-off between the integer boundary spur and phase noise.
Loop Bandwidth	28.7 KHz	This is around where the PLL and VCO noise meet. The VCO is at 2700 MHz
Kpd	31x	Choose the highest charge pump gain to maximize the capacitor next to the VCO.
C1_LF	1.8 nF	The loop filter can be calculated with the clock design tool. Note that we need to keep the loop bandwidth not too wide so that the capacitor next to the VCO is larger. Also, it is put in C4_LF spot, not C3_LF spot. Both are electrically equivalent, but layoutwise, C4_LF makes more sense. See the board layout in sections to come.
C2_LF	56 nF	
C3_LF	Open	
C4_LF	3.3 nF	
R2_LF	390 Ω	
R3_LF	270 Ω	
R4_LF	0 Ω	
OUT_A_PWR	30	This combination of pullup component and output power settings yields optimal noise floor.
Pullup Component	18 nH Inductor	

9.2.2.3 Application Curves

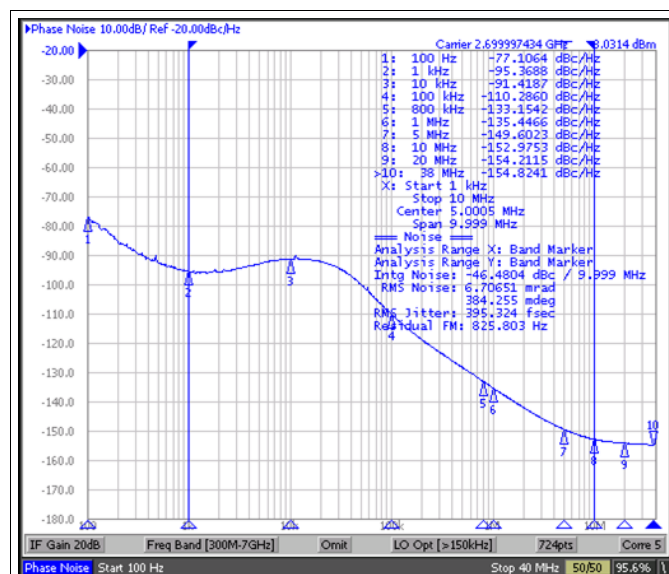


Figure 24. Integer Channel

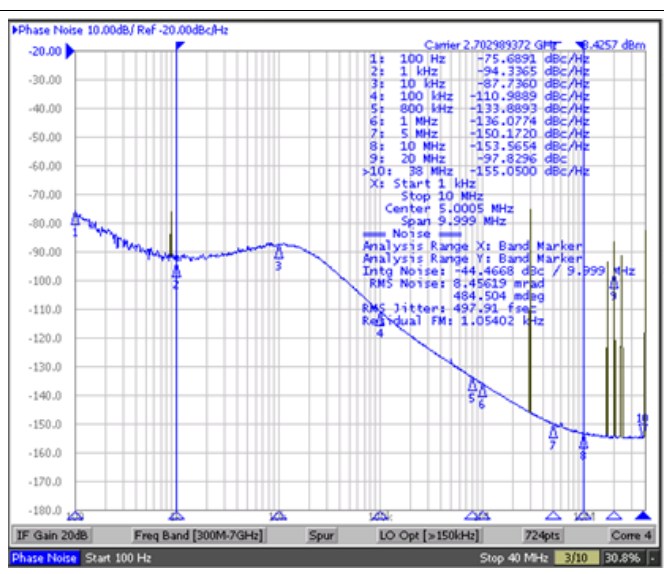


Figure 25. Fractional Channel 2703 MHz

9.3 Do's and Don'ts

CATEGORY	DO	DON'T	WHY
Output Pullup Components	Place pullup components close to RFoutA and RFoutB	Go through a Via before getting to the pullup component.	The output impedance is determined by this component and if it is far away, there will be loss in output power.
Fractional Spurs	- Take advantage of TI tools that can simulate these. - Read the section on spurs to better understand them. - Use a systematic process to optimize them	- Assume that raising the phase detector frequency always improves the integer boundary spur. - Assume that changing the loop bandwidth will always impact integer boundary spurs.	Fractional spurs can have more than one mechanism, especially the integer boundary spur.
Dithering	- Understand the trade-offs and when it is appropriate to use. - Combine with larger equivalent fractions.	Use on simple fractions .	Dithering is very effective in eliminating some spurs, but useless for eliminating others. Dithering adds PLL phase noise, so it should be only used for appropriate situations.
VbiasCOMP and VbiasVCO	Put as much capacitance as possible, up to 32 μ F	- Use less than 10 μF of capacitance - Ignore capacitor de-rating factors.	This capacitance impacts the VCO phase noise.

10 Power Supply Recommendations

10.1 Supply Recommendations

Low noise regulators are generally recommended for the supply pins. It is OK to have one regulator supply the part, although it is best to put individual bypassing as shown in the [Layout Guidelines](#) for the best spur performance. The most noise sensitive components are the pullup components for the output buffers since supply noise here will directly go to the output. For purposes of bypassing, below is how the current consumption is approximately distributed through each pin. For this table, default mode is with internal VCO mode with one output buffer powered up with OUTx_PWR=15. External VCO mode assumes the VCO divider and output buffers are off.

Table 16. Current Consumption by Pin

PIN NUMBER	PIN NAME	CONDITION		
		DEFAULT MODE	DEFAULT MODE with VCO DIVIDER ENABLED	EXTERNAL VCO MODE with OUTPUT BUFFER DISABLED
Pin 6	VccCP	12	12	12
Pin 10	VccPLL	28	28	48
Pin 16	VccBUF	23	43	1
Pin 17	VccVCO	83	83	14
Pin 28	VccDIG	10	10	10
Pin 32	VccFRAC	<<1	<<1	<<1
n/a	Output pullup component	22	22	0
TOTAL		178	198	85

10.2 Regulator Output Pins

The recommendation for the VregVCO and VbiasCOMP pins is a minimum of one 10 μ F capacitor, but more capacitance is better. These pins have a bias voltage of about 2.5 V, which means that capacitors of smaller case size and voltage ratings can actually have far less capacitance the labeled value of the capacitor. If there is insufficient capacitance on these pins, then the VCO phase noise may be degraded. This degradation may vary with frequency and how insufficient the capacitance is, but for example, bench tests show a degradation of about 5 dB at 20 KHz offset for a 3 GHz carrier if these capacitors are reduced to 4.7 μ F.

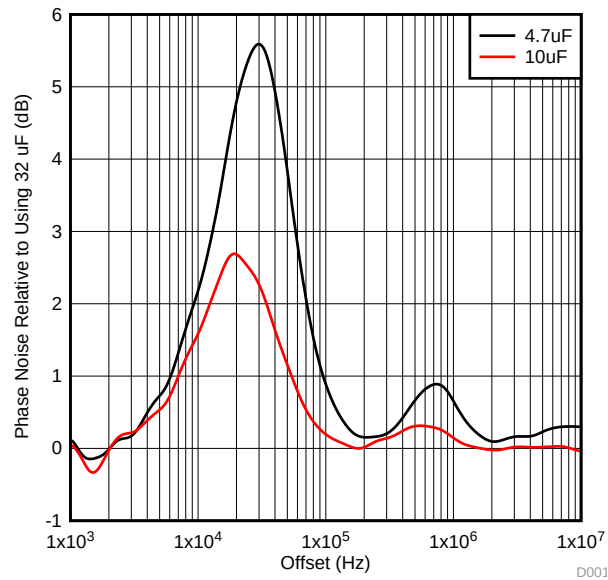


Figure 26. Impact of VregVCO and VbiasCOMP Capacitor on VCO Phase Noise

11 Layout

11.1 Layout Guidelines

For the Layout of the LMX2581E, the pullup component for the output buffers should be as close to the chip as possible in order to get the most possible output power.

The following layout guidelines apply. The designators match those shown in the applications schematic.

1. **RFoutA and B Pullup Components:** The pullup components are close. If using only one output, these components can be made even closer for an improvement in output power
2. **Ground for VbiasVCO and VbiasCOMP:** There is a solid connection for the ground between the VbiasVCO and VbiasCOMP pins and pin 18. This minimizes the VCO phase noise.
3. **Loop Filter:** One loop filter capacitor is next to the VCO. The charge pump output and Vtune input are on opposite sides of the chip. Although one can not get the whole loop filter close to the chip without compromising the grounding for the VbiasVCO and VbiasCOMP pins, it is possible to get the highest order loop filter capacitor there. Also, for the vias used, keep the ground plane far away so it does not couple spur energy into the VCO input.

11.2 Layout Example

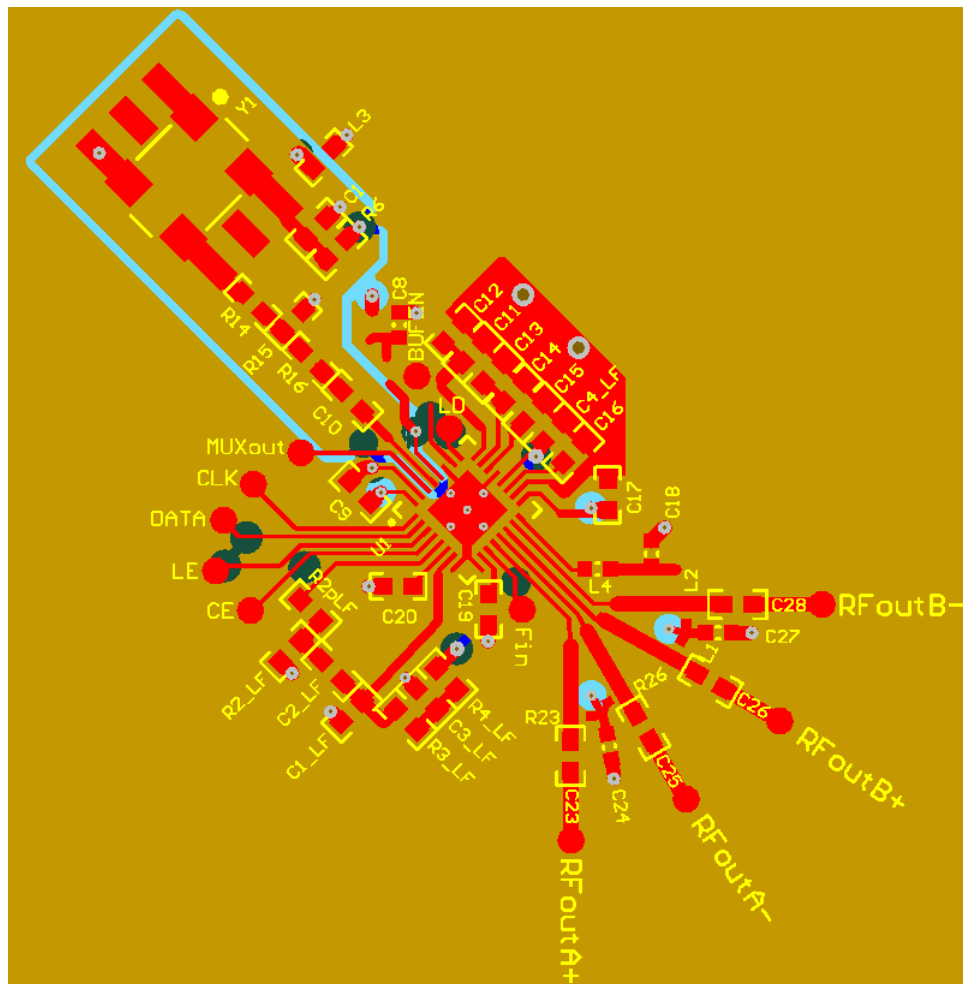


Figure 27. LMX2581E Layout Example

12 器件和文档支持

12.1 器件支持

德州仪器 (TI) 提供了多种软件工具：

- 欲了解如何编程 LMX2581E 和 EVM 板，请参见 [Codeloader](#)。
- 有关在 LMX2581E 上设计回路滤波器、仿真相位噪声以及仿真毛刺的信息，请参见[时钟设计工具](#)。
- 有关典型测量数据、详细测量条件以及完整设计的信息，请参见 EVM 板说明 [《LMX2581EVM 用户指南》](#)。
- 有关如何设计和仿真 LMX2581E 以及将它与其他器件搭配使用的信息，请参见[时钟架构工具](#)。

12.2 文档支持

12.2.1 相关文档

另请参见“AN-1879《分数 N 频率合成》”（文献编号：[SNAA062](#)）。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2581ESQE/NOPB	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	X2581E	Samples
LMX2581ESQX/NOPB	ACTIVE	WQFN	RTV	32	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	X2581E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

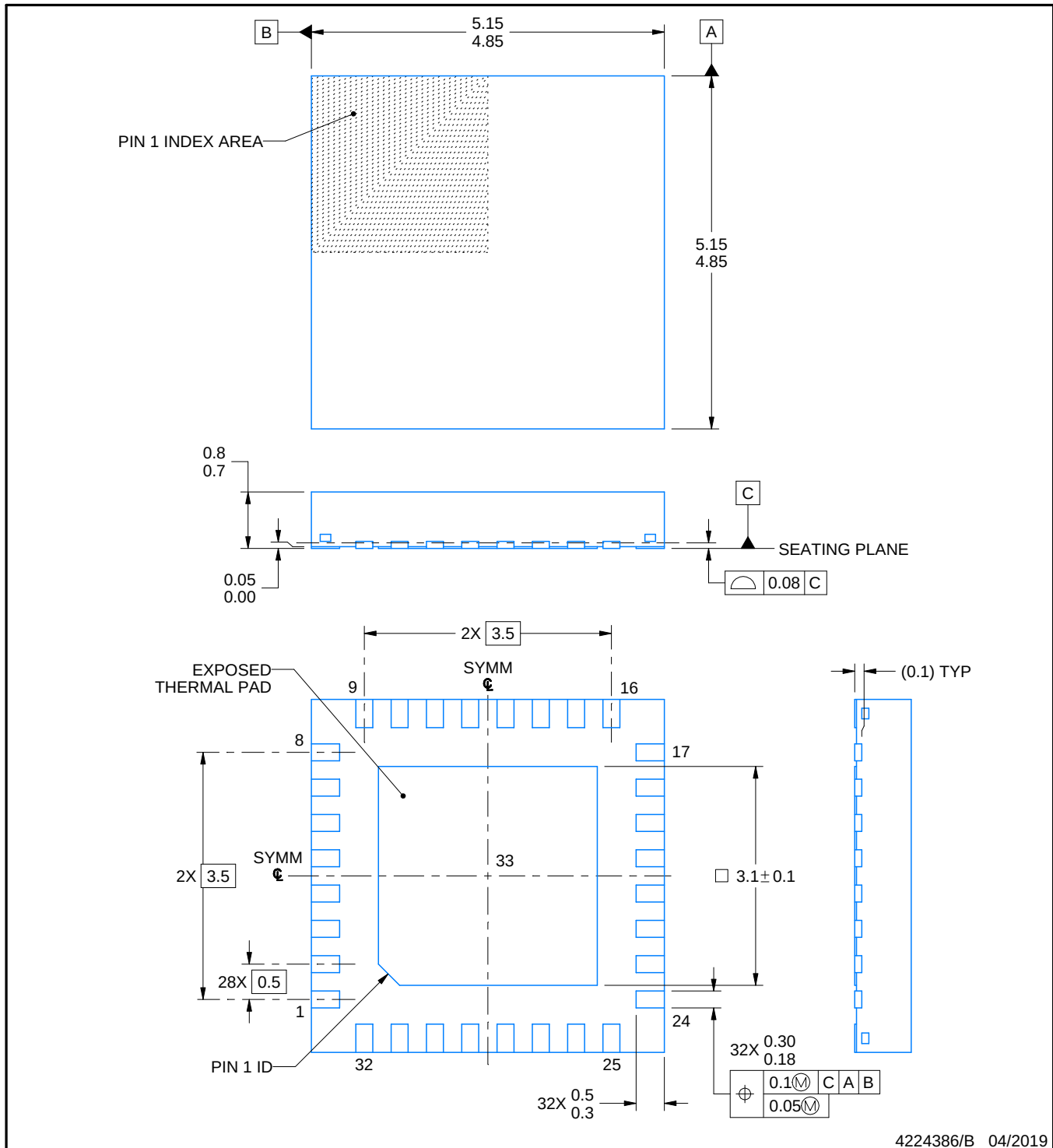
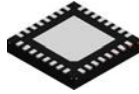
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

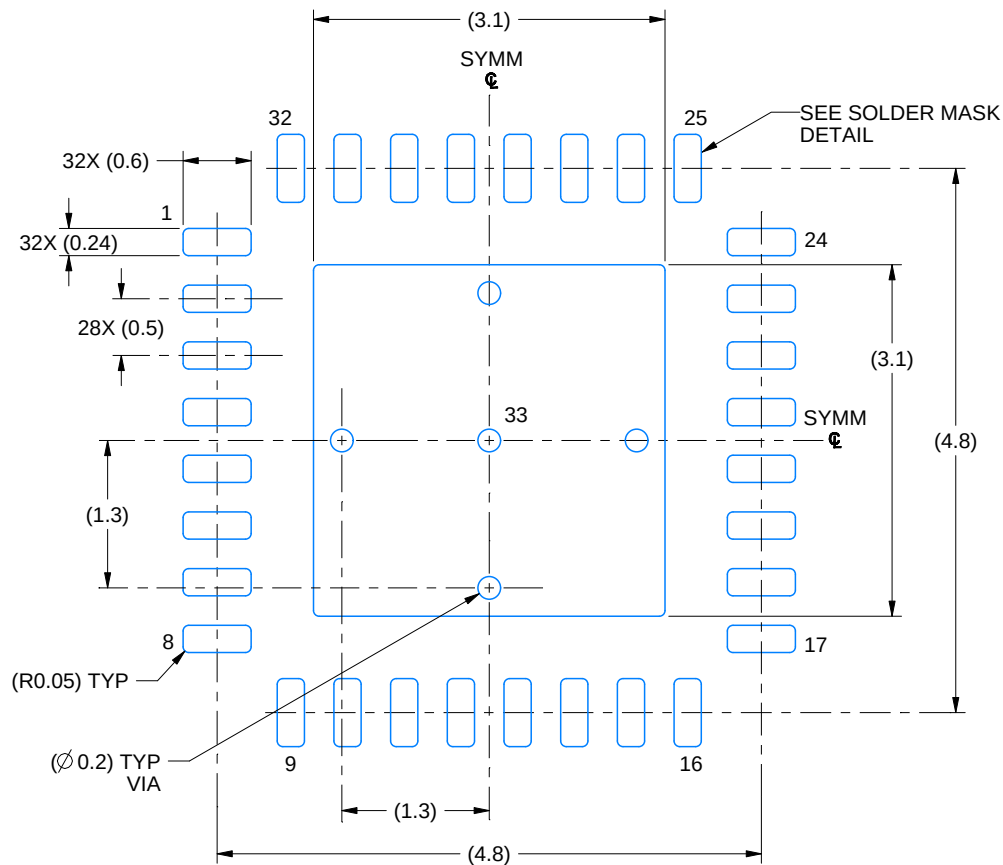
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

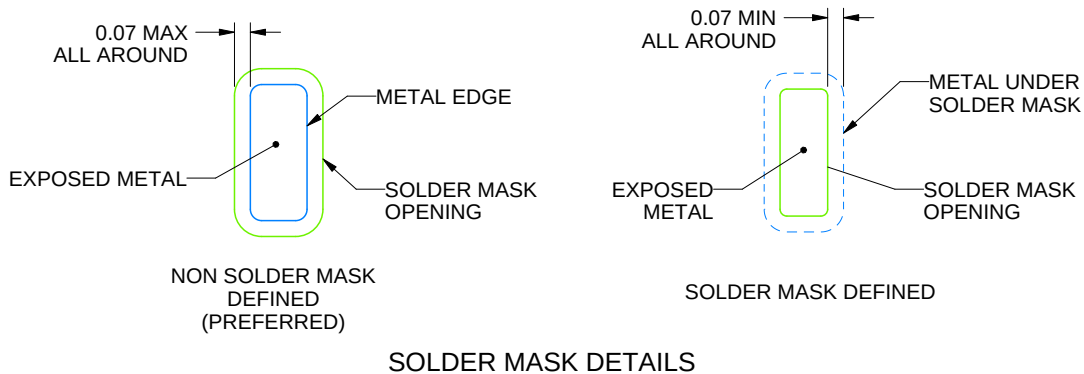
RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



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NOTES: (continued)

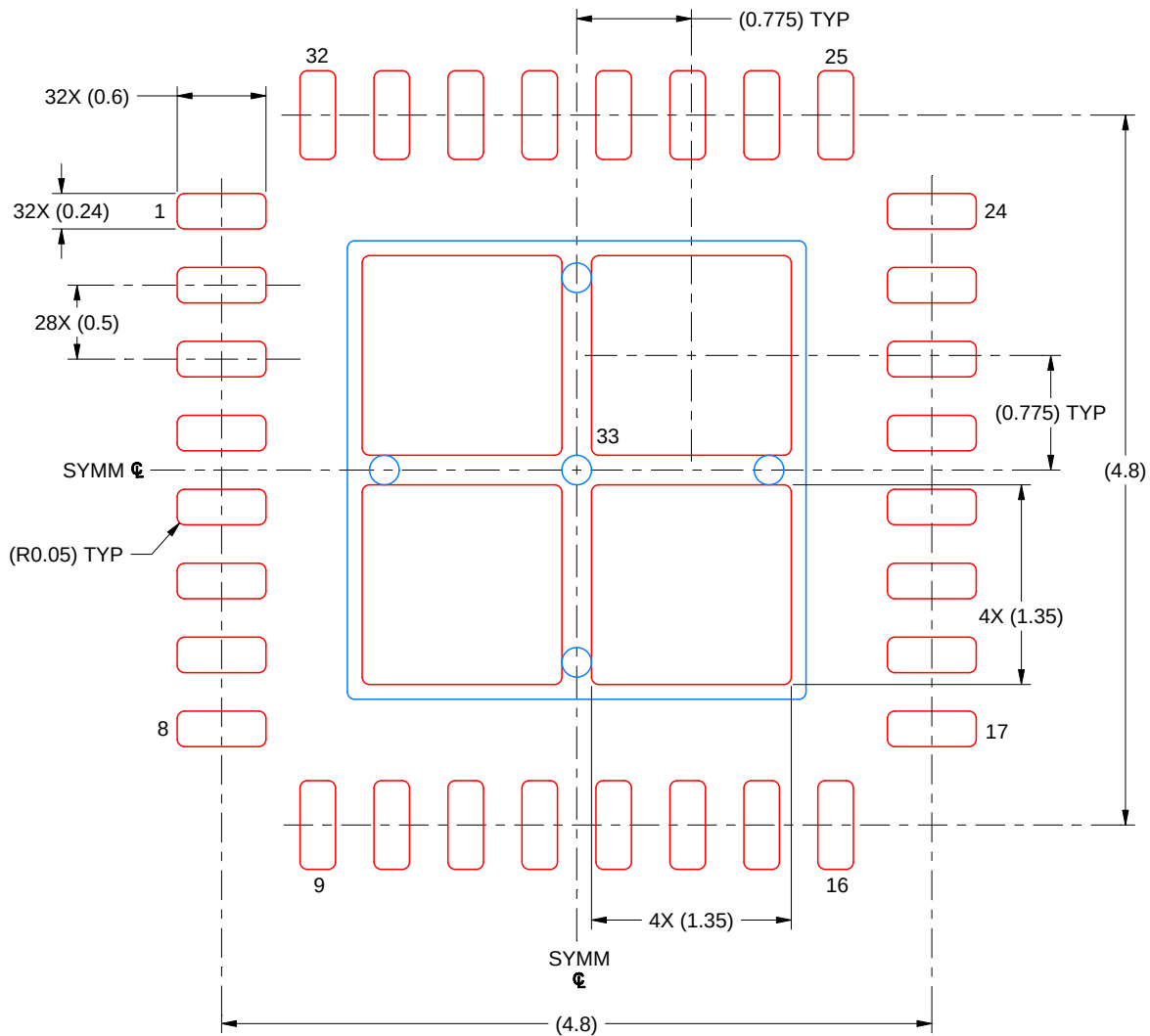
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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