

集成了 VCO 的 LMX2582 高性能宽带 PLLatinum™ 射频合成器

1 特性

- 输出频率范围为 20-5500MHz
- 相位噪声性能行业领先
 - VCO 相位噪声：在 1MHz 偏移时为 -144.5 dBc/Hz（对于 1.8GHz 输出）
 - 标准化锁相环 (PLL) 噪底：-231dBc/Hz
 - 标准化 PLL 闪烁噪声：-126dBc/Hz
 - 47fs RMS 抖动（12kHz 至 20MHz）（对于 1.8GHz 输出）
- 输入时钟频率高达 1400MHz
- 相位检测器频率高达 200MHz，且在整数 N 模式中高达 400MHz
- 支持分数 N 和整数 N 模式
- 双差分输出
- 减少毛刺的创新型解决方案
- 可编程相位调整
- 可编程电荷泵电流
- 可编程输出功率水平
- 串行外设接口 (SPI) 或 uWire（4 线制串行接口）
- 单电源供电：3.3V

2 应用

- 测试和测量设备
- 蜂窝基站
- 微波回程
- 高速数据转换器的高性能时钟源
- 由软件定义的无线电

3 说明

LMX2582 是一款集成了 VCO 的低噪声宽带射频 PLL，支持的频率范围为 20MHz 至 5.5GHz。该器件支持分数 N 和整数 N 模式，具有一个 32 位分数分频器，支持选择合适的频率。其积分噪声为 47fs（对于 1.8GHz 输出），是理想的低噪声源。该器件融入了一流的 PLL 和 VCO 积分噪声与集成的低压线性稳压器 (LDO)，从而无需高性能系统中的多个分立器件。

该器件可接受高达 1.4GHz 的输入频率，与分频器及可编程低噪声乘法器相结合，可灵活设置频率。附加的可编程低噪声乘法器可帮助用户减轻整数边界杂散的影响。在分数 N 模式下，该器件可将输出相位调整 32 位分辨率。对于需要快速频率变化的应用，该器件支持耗时小于 25μs 的快速校准选项。

使用一个 3.3V 电源即可能实现此性能。该器件支持 2 个差分输出，这两个输出也可灵活配置为单端输出。用户可选择将其中一个编程为从 VCO 输出，另一个从通道分配器输出。若不想使用，可分别禁用每个输出。

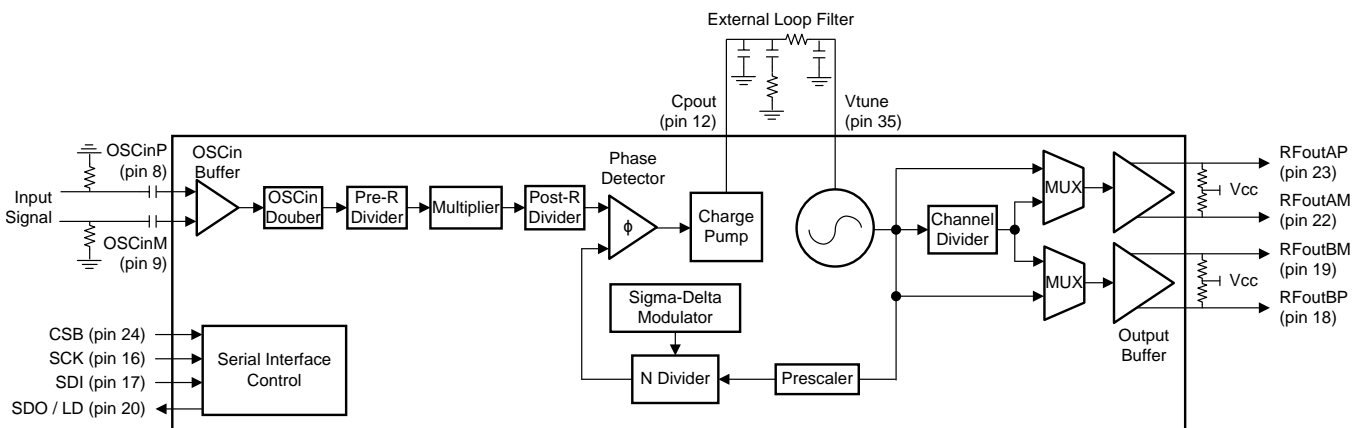
器件信息 (1)

器件型号	说明	封装尺寸 (标称值)
LMX2582RHAT LMX2582RHAR	WQFN (40)	6.00mm × 6.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) T = 带；R = 卷

简化电路原理图



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4 修订历史记录

Changes from Revision B (February 2017) to Revision C Page

•	Changed <i>Channel Divider Setting as a Function of the Desired Output Frequency</i> table	16
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Changes from Revision A (December 2015) to Revision B Page

•	从“特性”中删除了 < 25μs 快速校准模式项	1
•	将产品说明书文本更新为最新的文档和翻译标准	1
•	Changed pin 30 name from: Rext to: NC	4
•	Changed CDM value from: ±1250 V to: ±750 V	6
•	Changed parameter name from: Maximum reference input frequency to: reference input frequency	7
•	Removed the charge pump current TYP range '0 to 12' and split range into MIN (0) and MAX (12) columns	7
•	Added 10 kHz test conditions for the PN _{open loop} parameter	8
•	Added HD2, HD3, and Spur_PFD parameters to the <i>Electrical Characteristics</i> table	8
•	Changed the high level input voltage minimum value of from: 1.8 to: 1.4	8
•	Moved all typical values in the <i>Timing Requirements</i> table to minimum column	8
•	Changed text from: the rising edge of the LE signal to: the rising edge of the last CLK signal	9
•	Changed text from: the shift registers to an actual counter to: the shift registers to a register bank	9
•	Changed high input value from: 700 to: 200	14
•	Changed high input value from: 1400 to: 400	14
•	Changed minimum output frequency step from: Fpd / PLL_DEN to: Fpd × PLL_N_PRE / PLL_DEN / [Channel divider value]	15
•	Added content to the <i>Voltage Controlled Oscillator</i> section	15
•	Changed text from: output dividers to: channel dividers	15
•	Changed <i>Channel Divider Setting as a Function of the Desired Output Frequency</i> table	16
•	Changed output frequency from: 3600 to: 3550	16
•	Changed VCO frequency from: 7200 to: 7100	16
•	Changed Phase shift (degrees) from: 360 × MASH_SEED / PLL_N_DEN / [Channel divider value] to: 360 ×	

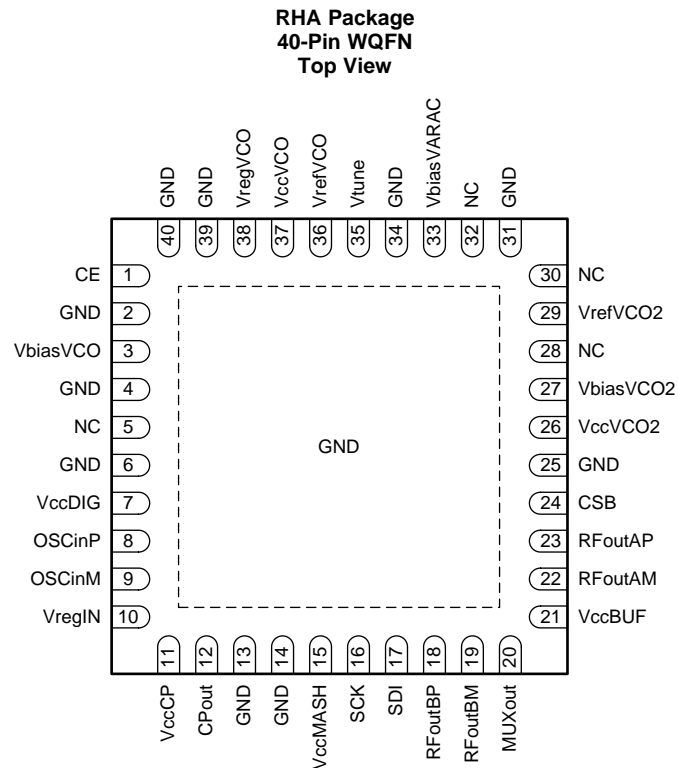
MASH_SEED x PLL_N_PRE / PLL_N_DEN / [Channel divider value]"	17
• Changed register 7, 8, 19, 23, 32, 33, 34, 46, and 64 descriptions	19
• Added registers 20, 22, 25, 59, and 61	19
• Added registers 2, 4, and 62 to <i>Register Table</i>	20
• Changed register 38 in <i>Register Table</i>	20
• Changed register descriptions from: Program to default to: Program to Register Map default values.....	21
• Added <i>R2 Register Field Descriptions</i>	22
• Added <i>R4 Register Field Descriptions</i>	22
• Added <i>R62 Register Field Descriptions</i>	28
• Updated content in the <i>Decreasing Lock Time</i> section	34
• Changed typical application image	36
• Changed charge pump value from: 4.8 to: 20.....	36
• Changed R2 value from: 0.068 to: 68	36

Changes from Original (December 2015) to Revision A

Page

• 将器件状态从“产品预览”更改为“生产数据”并发布了完整版产品说明书.....	1
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5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CE	1	Input	Chip Enable input. Active high powers on the device.
CPout	12	Output	Charge pump output. Recommend connecting C1 of loop filter close to pin.
CSB	24	Input	SPI chip select bar or uWire latch enable (abbreviated as LE in Figure 1). High impedance CMOS input. 1.8 to 3.3-V logic.
DAP	GND	Ground	RFout ground.
GND	2, 4, 6, 13, 14, 25, 31, 34, 39, 40	Ground	VCO ground.
MUXout	20	Output	Programmable with register MUXOUT_SEL to be readback SDO or lock detect indicator (active high).
NC	5, 28, 30, 32	—	Not connected.
OSCinP	8	Input	Differential reference input clock (+). High input impedance. Requires connecting series capacitor (0.1-μF recommended).
OSCinM	9	Input	Differential reference input clock (-). High input impedance. Requires connecting series capacitor (0.1-μF recommended).
RFoutAM	22	Output	Differential output A (-). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
RFoutAP	23	Output	Differential output A (+). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
RFoutBM	19	Output	Differential output B (-). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
RFoutBP	18	Output	Differential output B (+). This output requires a pull up component for proper biasing. A 50-Ω resistor or inductor may be used. Place as close to output as possible.
SCK	16	Input	SPI or uWire clock (abbreviated as CLK in Figure 1). High impedance CMOS input. 1.8 to 3.3-V logic.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SDI	17	Input	SPI or uWire data (abbreviated as DATA in Figure 1). High impedance CMOS input. 1.8 to 3.3-V logic.
VbiasVARAC	33	Bypass	VCO varactor internal voltage, access for bypass. Requires connecting 10-μF capacitor to VCO ground.
VbiasVCO	3	Bypass	VCO bias internal voltage, access for bypass. Requires connecting 10-μF capacitor to VCO ground. Place close to pin.
VbiasVCO2	27	Bypass	VCO bias internal voltage, access for bypass. Requires connecting 1-μF capacitor to VCO ground.
V _{CC} BUF	21	Supply	Output buffer supply. Requires connecting 0.1-μF capacitor to RFout ground.
V _{CC} CP	11	Supply	Charge pump supply. Recommend connecting 0.1-μF capacitor to charge pump ground.
V _{CC} DIG	7	Supply	Digital supply. Recommend connecting 0.1-μF capacitor to digital ground.
V _{CC} MASH	15	Supply	Digital supply. Recommend connecting 0.1-μF and 10-μF capacitor to digital ground.
V _{CC} VCO	37	Supply	VCO supply. Recommend connecting 0.1-μF and 10-μF capacitor to ground.
V _{CC} VCO2	26	Supply	VCO supply. Recommend connecting 0.1-μF and 10-μF capacitor to VCO ground.
VrefVCO	36	Bypass	VCO supply internal voltage, access for bypass. Requires connecting 10-μF capacitor to ground.
VrefVCO2	29	Bypass	VCO supply internal voltage, access for bypass. Requires connecting 10-μF capacitor to VCO ground.
VregIN	10	Bypass	Input reference path internal voltage, access for bypass. Requires connecting 1-μF capacitor to ground. Place close to pin.
VregVCO	38	Bypass	VCO supply internal voltage, access for bypass. Requires connecting 1-μF capacitor to ground.
Vtune	35	Input	VCO tuning voltage input. This signal should be kept away from noise sources.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Power supply voltage	−0.3	3.6	V
V _{IN}	Input voltage to pins other than V _{CC} pins	−0.3	V _{CC} + 0.3	V
V _{OSCin}	Voltage on OSCin (pin 8 and pin 9)	≤1.8 with V _{CC} Applied	≤1 with V _{CC} = 0	V _{pp}
T _L	Lead temperature (solder 4 s)		260	°C
T _J	Junction temperature	−40	150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750
		Machine model (MM) ESD stress voltage	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2500 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1250 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Power supply voltage	3.15		3.45	V
T _A	Ambient temperature	−40		85	°C
T _J	Junction temperature			125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMX2582	UNIT
		RHA (WQFN)	
		40 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	30.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	15.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	5.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	5.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	0.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, −40°C ≤ T_A ≤ 85°C.

Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V _{CC}	Supply voltage			3.3		V
I _{CC}	Supply current	Single 5.4-GHz, 0-dBm output ⁽¹⁾		250		mA
I _{PD}	Powerdown current			3.7		mA
OUTPUT CHARACTERISTICS						
F _{out}	Output frequency		20		5500	MHz
P _{out}	Typical high output power	Output = 3 GHz, 50-Ω pullup, single-ended ⁽²⁾		8		dBm
INPUT SIGNAL PATH						
REF _{in}	Reference input frequency		5		1400	MHz
REF _v	Reference input voltage	AC-coupled, differential ⁽³⁾	0.2		2	V _{ppd}
MUL _{in}	Input signal path multiplier input frequency		40		70	MHz
MUL _{out}	Input signal path multiplier output frequency		180		250	MHz
PHASE DETECTOR AND CHARGE PUMP						
PDF	Phase detector frequency		5		200	MHz
		Extended range mode ⁽⁴⁾	0.25		400	MHz
CPI	Charge pump current	Programmable	0		12	mA
PLL PHASE NOISE						
PLL _{flicker_Norm}	Normalized PLL Flicker Noise ⁽⁵⁾			−126		dBc/Hz
PLL _{FOM}	Normalized PLL Noise Floor (PLL Figure of Merit) ⁽⁵⁾			−231		dBc/Hz
VCO						
ΔT _{CL}	Allowable temperature drift ⁽⁶⁾	VCO not being recalibrated			125	°C

- (1) For typical total current consumption of 250 mA: 100-MHz input frequency, OSC_{in} doubler bypassed, pre-R divider bypassed, multiplier bypassed, post-R divider bypassed, 100-MHz phase detector frequency, 0.468-mA charge pump current, channel divider off, one output on, 5.4GHz output frequency, 50-Ω output pullup, 0-dBm output power (differential). See the [Application and Implementation](#) section for more information.
- (2) For a typical high output power for a single-ended output, with 50-Ω pullup on both M and P side, register OUT_x_POW = 63. Un-used side terminated with 50-Ω load.
- (3) There is internal voltage biasing so the OSC_{inM} and OSC_{inP} pins must always be AC-coupled (capacitor in series). V_{ppd} is differential peak-to-peak voltage swing. If there is a differential signal (two are negative polarity of each other), the total swing is one subtracted by the other, each should be 0.1 to 1-V_{ppd}. If there is a single-ended signal, it can have 0.2 to 2 V_{ppd}. See the [Application and Implementation](#) section for more information.
- (4) To use phase detector frequencies lower than 5-MHz set register FCAL_LPFD_ADJ = 3. To use phase detector frequencies higher than 200 MHz, you must be in integer mode, set register PFD_CTL = 3 (to use single PFD mode), set FCAL_HPFD_ADJ = 3. For more information, see the [Detailed Description](#) section.
- (5) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_{flat} = PLL_{FOM} + 20 × log(F_{vco}/F_{pd}) + 10 × log(F_{pd} / 1Hz). PLL_{flicker} (offset) = PLL_{flicker_Norm} + 20 × log(F_{vco} / 1GHz) − 10 × log(offset / 10kHz). Once these two components are found, the total PLL noise can be calculated as PLL_{Noise} = 10 × log(10^{PLL_{Flat} / 10} + 10^{PLL_{flicker} / 10}).
- (6) Not tested in production. Ensured by characterization. Allowable temperature drift refers to programming the device at an initial temperature and allowing this temperature to drift without reprogramming the device, and still have the device stay in lock. This change could be up or down in temperature and the specification does not apply to temperatures that go outside the recommended operating temperatures of the device.

Electrical Characteristics (continued)

 $3.15\text{ V} \leq V_{CC} \leq 3.45\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.

Typical values are at $V_{CC} = 3.3\text{ V}$, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN _{open loop}	Output = 900 MHz	10 kHz		-105.7		dBc/Hz
		100 kHz		-129.8		
		1 MHz		-150.4		
		10 MHz		-160.6		
		100 MHz		-161.1		
	Output = 1.8 GHz	10 kHz		-99.5		
		100 kHz		-123.6		
		1 MHz		-144.5		
		10 MHz		-157.2		
		100 MHz		-157.7		
	Output = 5.5 GHz	10 kHz		-89.7		
		100 kHz		-114.0		
		1 MHz		-134.9		
		10 MHz		-151.3		
		100 MHz		-153.3		
HD2	2nd Order Harmonic Distortion ⁽⁷⁾	Testing output A, output at 5 GHz, output power level at 8.5-dBm, single-ended output, other end terminated with 50 Ω.	-27		dBc	
HD3	3rd Order Harmonic Distortion ⁽⁷⁾		-25		dBc	
DIGITAL INTERFACE						
V _{IH}	High level input voltage		1.4		V _{CC}	V
V _{IL}	Low level input voltage		0		0.4	V
I _{IH}	High level input current		-25		25	μA
I _{IL}	Low level input current		-25		25	μA
V _{OH}	High level output voltage	Load/Source Current of -350 μA		V _{CC} - 0.4		V
V _{OL}	Low level output voltage	Load/Sink Current of 500 μA		0.4		V
SPIW	Highest SPI write speed			75		MHz
SPIR	SPI read speed			50		MHz
Spur_PFD	Phase frequency detector spur	PFD = 20 MHz, output = 5.4 GHz		-93		dBc

(7) This parameter is verified by characterization on evaluation board, not tested in production.

6.6 Timing Requirements

 $3.15\text{ V} \leq V_{CC} \leq 3.45\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, except as specified. Typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$

		MIN	TYP	MAX	UNIT
MICROWIRE TIMING					
tES	Clock to enable low time	See Figure 1	5		ns
tCS	Data to clock setup time		2		ns
tCH	Data to clock hold time		2		ns
tCWH	Clock pulse width high		5		ns
tCWL	Clock pulse width low		5		ns
tCES	Enable to clock setup time		5		ns
tEWH	Enable pulse width high		2		ns

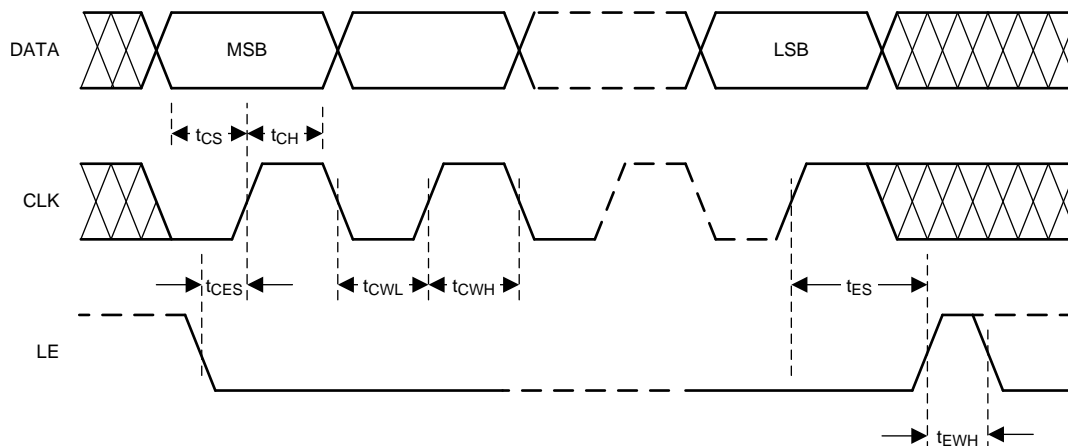


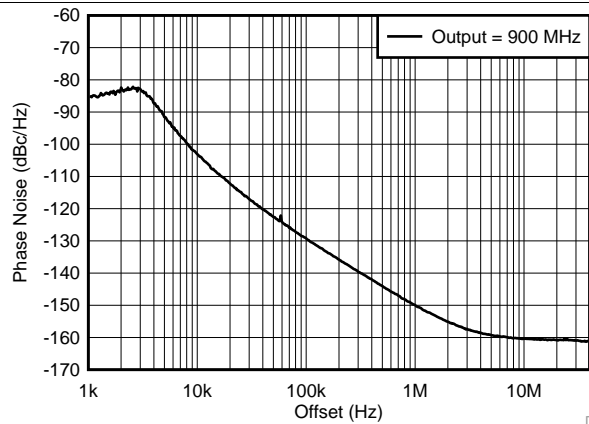
Figure 1. Serial Data Input Timing Diagram

There are several considerations for programming:

- A slew rate of at least 30 V/ μ s is recommended for the CLK, DATA, LE
- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the last CLK signal, the data is sent from the shift registers to a register bank
- The LE pin may be held high after programming and clock pulses are ignored
- The CLK signal should not be high when LE transitions to low
- When CLK and DATA lines are shared between devices, TI recommends diving down the voltage to the CLK, DATA, and LE pins closer to the minimum voltage. This provides better noise immunity
- If the CLK and DATA lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming

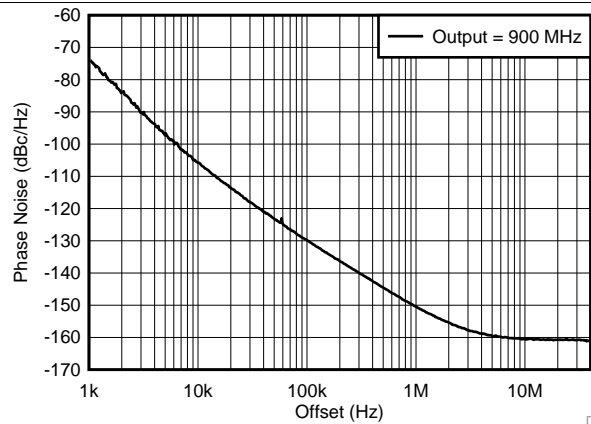
6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)



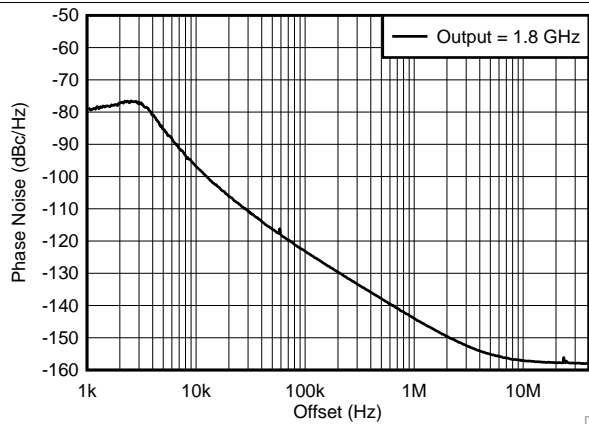
D001

Figure 2. 900-MHz Output - Closed-Loop Phase Noise



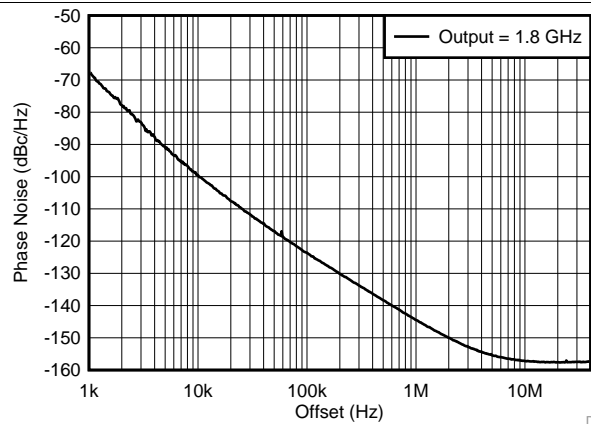
D002

Figure 3. 900-MHz Output - Open-Loop Phase Noise



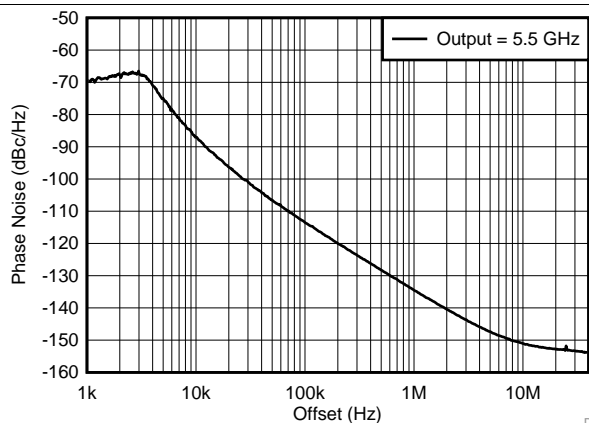
D003

Figure 4. 1.8-GHz Output - Closed-Loop Phase Noise



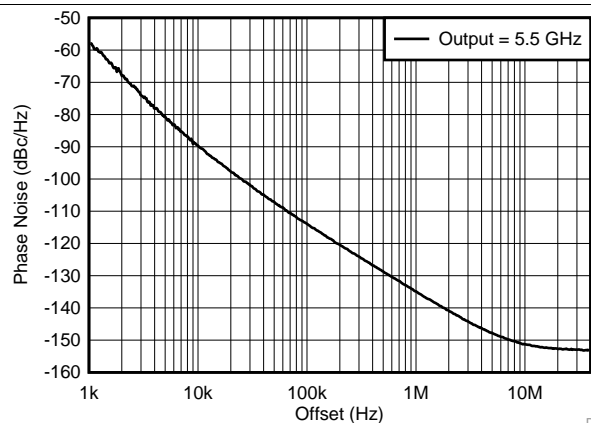
D004

Figure 5. 1.8-GHz Output - Open-Loop Phase Noise



D005

Figure 6. 5.5-GHz Output - Closed-Loop Phase Noise



D006

Figure 7. 5.5-GHz Output - Open-Loop Phase Noise

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

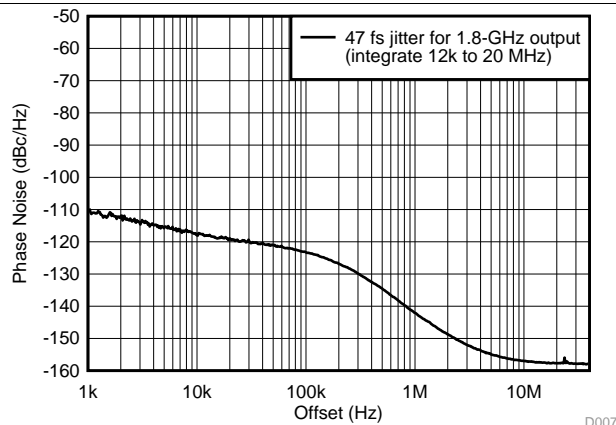


Figure 8. Integrated Jitter (47 fs) - 1.8-GHz Output

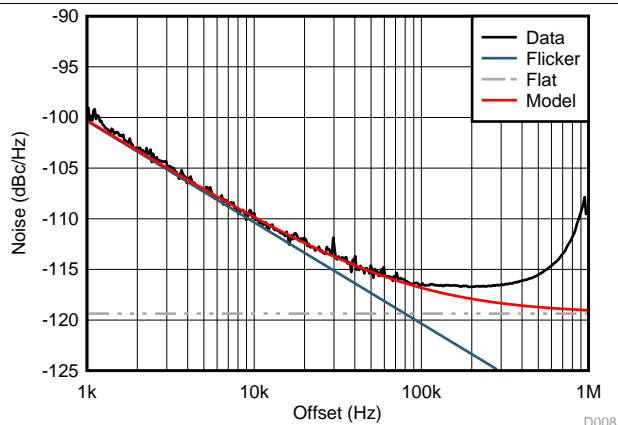


Figure 9. 5.4-GHz Output Wide Loop Bandwidth – Showing PLL Performance

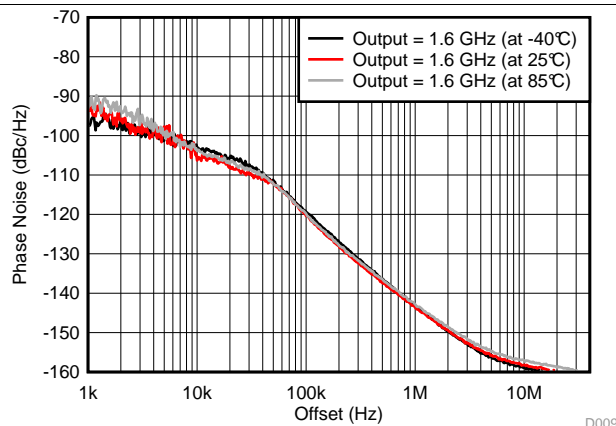


Figure 10. Variation of Phase Noise Across Temperature

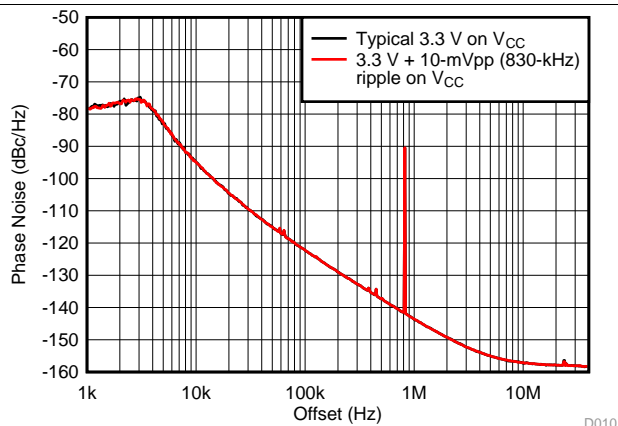


Figure 11. Impact of Supply Ripple on 1.8-GHz Output Phase Noise

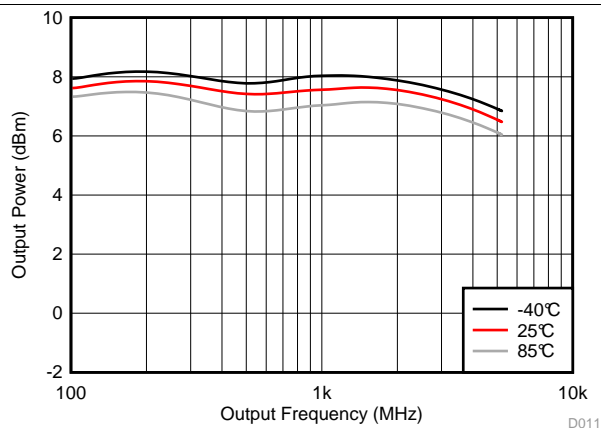


Figure 12. High Output Power (50-Ω Pullup, Single-Ended) vs Output Frequency

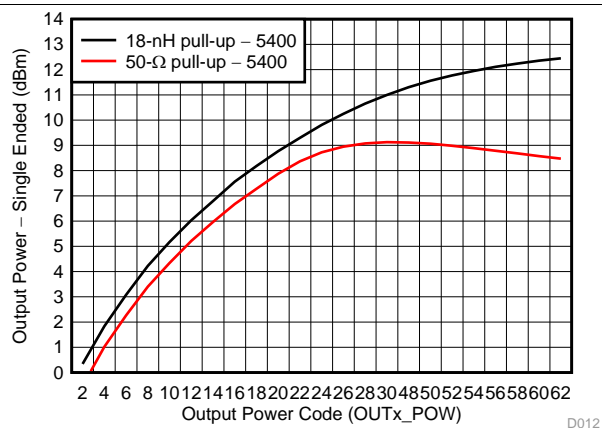


Figure 13. Output Power at 5.4-GHz Output vs OUTx_POW Code (1 - 31, 48 - 63)

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

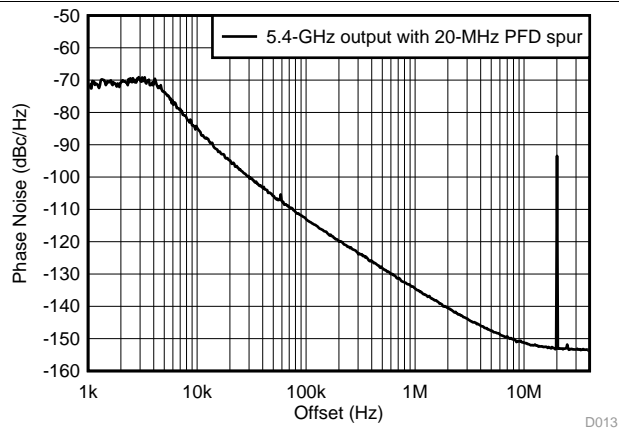


Figure 14. Typical PFD Spur for 5.4-GHz Output

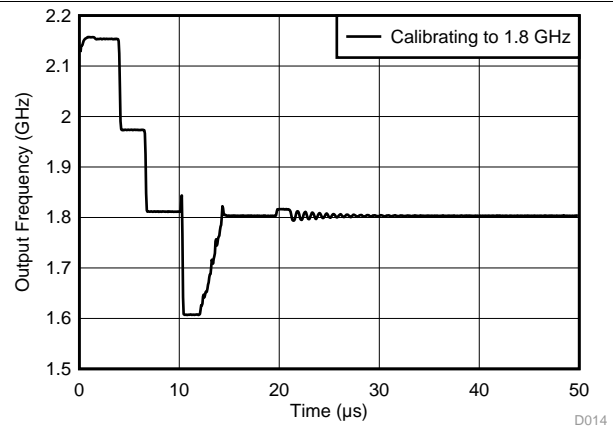


Figure 15. 20- μs Frequency Change Time to 1.8 GHz With Fast Calibration

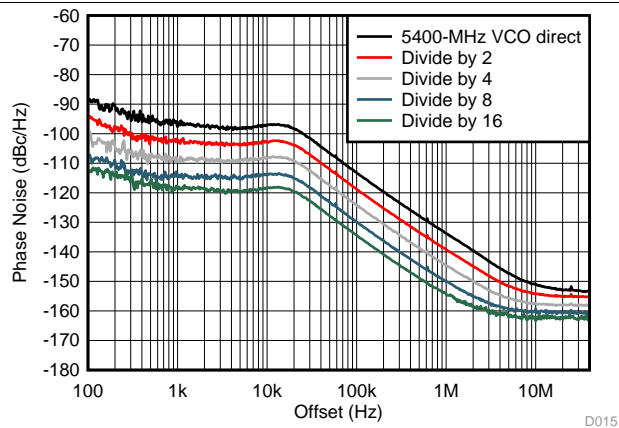


Figure 16. Impact of Channel Divider Settings on Phase Noise

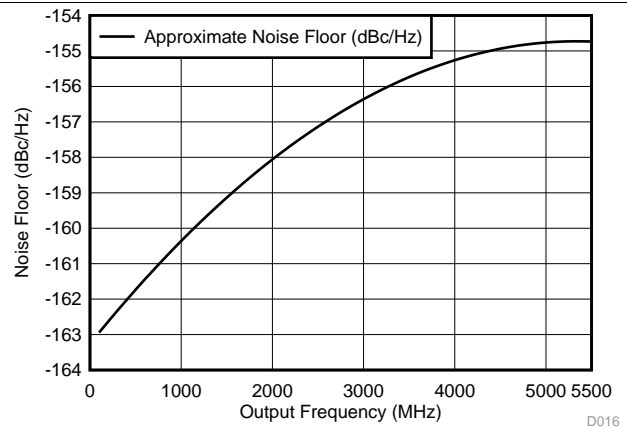


Figure 17. Noise Floor Variation With Output Frequency

7 Detailed Description

7.1 Overview

The LMX2582 is a high performance wideband synthesizer (PLL with integrated VCO). The output frequency range is from 20 MHz to 5.5 GHz. The VCO core covers an octave from 3.55 to 7.1 GHz. The output channel divider covers the frequency range from 20 MHz to the low bound of the VCO core.

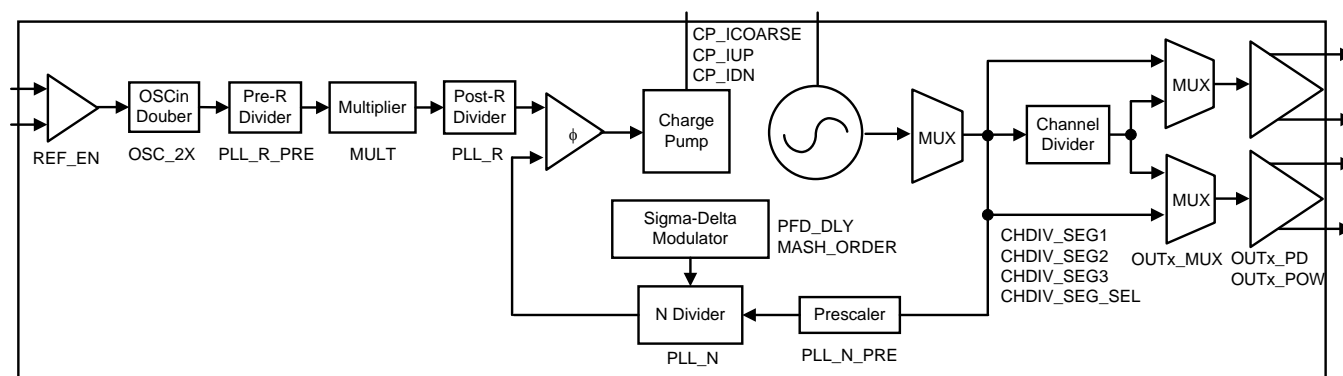
The input signal frequency has a wide range from 5 to 1400 MHz. Following the input, there is an programmable OSCin doubler, a pre-R divider (previous to multiplier), a multiplier, and then a post-R divider (after multiplier) for flexible frequency planning between the input (OSCin) and the phase detector.

The phase detector (PFD) can take frequencies from 5 to 200 MHz, but also has extended modes down to 0.25 MHz and up to 400 MHz. The phase-lock loop (PLL) contains a Sigma-Delta modulator (1st to 4th order) for fractional N-divider values. The fractional denominator is programmable to 32-bit long, allowing a very fine resolution of frequency step. There is a phase adjust feature that allows shifting of the output phase in relation to the input (OSCin) by a fraction of the size of the fractional denominator.

The output power is programmable and can be designed for high power at a specific frequency by the pullup component at the output pin.

The digital logic is a standard 4-wire SPI or uWire interface and is 1.8-V and 3.3-V compatible.

7.2 Functional Block Diagram



7.3 Functional Description

7.3.1 Input Signal

An input signal is required for the PLL to lock. The input signal is also used for the VCO calibration, so a proper signal needs to be applied before the start of programming. The input signal goes to the OSCinP and OSCinM pins of the device (there is internal biasing which requires AC-coupling caps in series before the pin). This is a differential buffer so the total swing is the OSCinM signal subtracted by the OSCinP signal. Both differential signals and single-ended signal can be used. Below is an example of the max signal level in each mode. It is important to have proper termination and matching on both sides (see [Application and Implementation](#)).

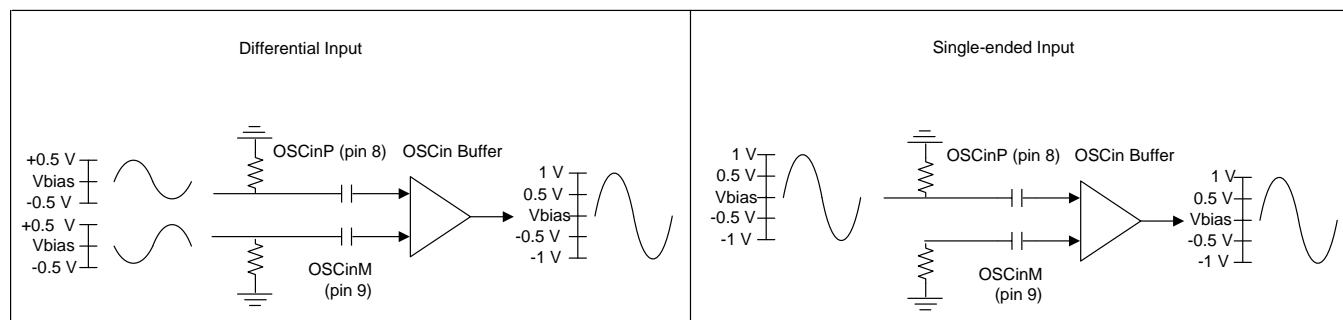


Figure 18. Differential vs Single-Ended Mode

Functional Description (continued)

7.3.2 Input Signal Path

The input signal path contains the components between the input (OSCin) buffer and the phase detector. The best PLL noise floor is achieved with a 200-MHz input signal for the highest dual-phase detector frequency. To address a wide range of applications, the input signal path contains the below components for flexible configuration before the phase detector. Each component can be bypassed. See [Table 1](#) for usage boundaries if engaging a component.

- **OSCin doubler:** This is low noise frequency doubler which can be used to multiply input frequencies by two. The doubler uses both the rising and falling edge of the input signal so the input signal must have 50% duty cycle if enabling the doubler. The best PLL noise floor is achieved with 200-MHz PFD, thus the doubler is useful if, for example, a very low-noise, 100-MHz input signal is available instead.
- **Pre-R divider:** This is a frequency divider capable of very high frequency inputs. Use this to divide any input frequency up to 1400-MHz, and then the post-R divider if lower frequencies are needed.
- **Multiplier:** This is a programmable, low noise multiplier. In combination with the Pre-R and Post-R dividers, the multiplier offers the flexibility to set a PFD away from frequencies that may create critical integer boundary spurs with the VCO and output frequencies. See the [Application and Implementation](#) section for an example. The user should not use the doubler while using the low noise programmable multiplier.
- **Post-R divider:** Use this divider to divide down to frequencies below 5 MHz in extended PFD mode.

Table 1. Boundaries for Input Path Components

	INPUT		OUTPUT	
	LOW (MHz)	HIGH (MHz)	LOW (MHz)	HIGH (MHz)
Input signal	5	1400		
OSCin doubler	5	200	10	400
Pre-R divider	10	1400	5	700
Multiplier	40	70	180	250
Post-R divider	5	250	0.25	125
PFD	0.25	400		

7.3.3 PLL Phase Detector and Charge Pump

The PLL phase detector, also known as phase frequency detector (PFD), compares the outputs of the post-R divider and N divider and generates a correction current with the charge pump corresponding to the phase error until the two signals are aligned in phase (the PLL is locked). The charge pump output goes through external components (loop filter) which turns the correction current pulses into a DC voltage applied to the tuning voltage (Vtune) of the VCO. The charge pump gain level is programmable and allow to modify the loop bandwidth of the PLL.

The default architecture is a dual-loop PFD which can operate between 5 to 200 MHz. To use it in extended range mode the PFD has to be configured differently:

- **Extended low phase detector frequency mode:** For frequencies between 250 kHz and 5 MHz, low PFD mode can be activated (FCAL_LPFD_ADJ = 3). PLL_N_PRE also needs to be set to 4.
- **Extended high phase detector frequency mode:** For frequencies between 200 and 400 MHz, high PFD mode can be activated (FCAL_HPFD_ADJ = 3). The PFD also has to be set to single-loop PFD mode (PFD_CTL = 3). This mode only works if using integer-N, and PLL noise floor will be about 6-dB higher than in dual-loop PFD mode.

7.3.4 N Divider and Fractional Circuitry

The N divider (12 bits) includes a multi-stage noise shaping (MASH) sigma-delta modulator with programmable order from 1st to 4th order, which performs fractional compensation and can achieve any fractional denominator from 1 to $(2^{32} - 1)$. Using programmable registers, PLL_N is the integer portion and PLL_NUM / PLL_DEN is the fractional portion, thus the total N divider value is determined by $PLL_N + PLL_NUM / PLL_DEN$. This allows the output frequency to be a fractional multiplication of the phase detector frequency. The higher the denominator the finer the resolution step of the output. There is a N divider prescaler (PLL_N_PRE) between the VCO and the N divider which performs a division of 2 or 4. 2 is selected typically for higher performance in fractional mode and 4 may be desirable for lower power operation and when N is approaching max value.

$$F_{vco} = F_{pd} \times PLL_N_PRE \times (PLL_N + PLL_NUM / PLL_DEN)$$

$$\text{Minimum output frequency step} = F_{pd} \times PLL_N_PRE / PLL_DEN / [\text{Channel divider value}]$$

Typically, higher modulator order pushes the noise out in frequency and may be filtered out with the PLL. However, several tradeoff needs to be made. [Table 2](#) shows the suggested minimum N value while in fractional mode as a function of the sigma-delta modulator order. It also describe the recommended register setting for the PFD delay (register PFD_DLY_SEL).

Table 2. MASH Order and N Divider

	INTEGER-N	1st ORDER	2nd ORDER	3rd ORDER	4th ORDER
Minimum N divider (low bound)	9	11	16	18	30
PFD delay recommended setting (PFD_DLY_SEL)	1	1	2	2	8

7.3.5 Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) is fully integrated. The frequency range of the VCO is from 3.55 to 7.1 GHz so it covers one octave. Channel dividers allow the generation of all other lower frequencies. The VCO-doubler allow the generation of all other higher frequencies. The output frequency of the VCO is inverse proportional to the DC voltage present at the tuning voltage point on pin Vtune. The tuning range is 0 V to 2.5 V. 0 V generates the maximum frequency and 2.5 V generates the minimum frequency. This VCO requires a calibration procedure for each frequency selected to lock on. Each VCO calibration will force the tuning voltage to mid value and calibrate the VCO circuit. Any frequency setting in fast calibration occurs in the range of Vtune pin 0 V to 2.5 V. The VCO is designed to remained locked over the entire temperature range the device can support. [Table 3](#) shows the VCO gain as a function of frequency.

Table 3. Typical kVCO

VCO FREQUENCY (MHz)	kVCO (MHz/V)
3700	28
4200	30
4700	33
5200	36
5700	41
6200	47
6800	51

7.3.6 VCO Calibration

The VCO calibration is responsible of setting the VCO circuit to the target frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. A valid input (OSCin) signal to the device must present before the VCO calibration begins. To see how to reduce the calibration time, refer to the [Application and Implementation](#) section.

7.3.7 Channel Divider

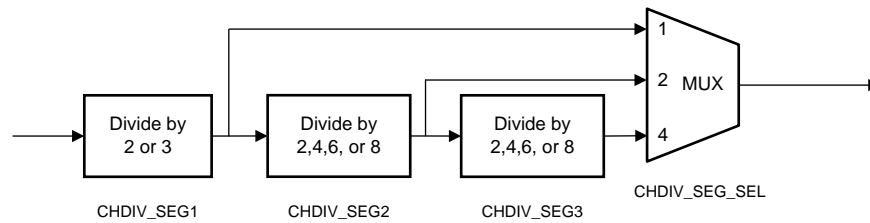


Figure 19. Channel Divider Diagram

To go below the VCO lower bound, the channel divider must be used. The channel divider consists of three programmable dividers controlled by the registers CHDIV_SEG1, CHDIV_SEG2, CHDIV_SEG3. The Multiplexer (programmed with register CHDIV_SEG_SEL) selects which divider is included in the path. The minimum division is 2 while the maximum division is 192. Un-used dividers can be powered down to save current consumption. The entire channel divider can be powered down with register CHDIV_EN = 0 or selectively setting registers CHDIV_SEG1_EN = 0, CHDIV_SEG2_EN = 0, CHDIV_SEG3_EN = 0. Unused buffers may also be powered down with registers CHDIV_DISTA_EN and CHDIV_DIST_EN. See [Table 4](#) for a guideline of what channel divider setting to use when below a specific output frequency.

Table 4. Channel Divider Setting as a Function of the Desired Output Frequency

Output Frequency		CHDIV Segments			total div	VCO Frequency	
min	max	seg1	seg2	seg3		min	max
1775	3550	2	1	1	2	3550	7100
1184	2366.666667	3	1	1	3	3552	7100
888	1184	2	2	1	4	3552	4736
592	888	3	2	1	6	3552	5328
444	592	2	4	1	8	3552	4736
296	444	2	6	1	12	3552	5328
222	296	2	8	1	16	3552	4736
148	222	3	8	1	24	3552	5328
111	148	2	8	2	32	3552	4736
99	111	3	6	2	36	3564	3996
74	99	3	8	2	48	3552	4752
56	74	2	8	4	64	3584	4736
37	56	2	8	6	96	3552	5376
28	37	2	8	8	128	3584	4736
20	28	3	8	8	192	3840	5376

7.3.8 Output Distribution

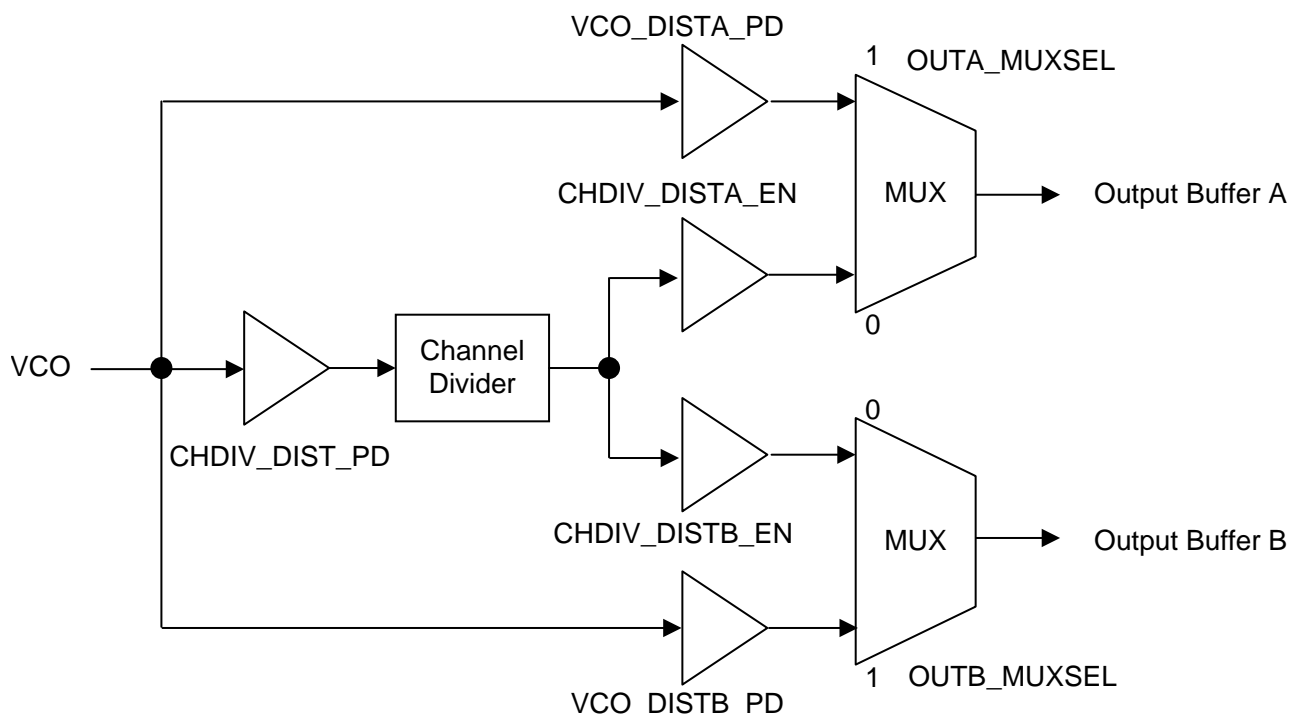


Figure 20. Output Distribution Diagram

For each output A or B, there is a mux which select the VCO output directly or the channel divider output. Before these selection MUX there are several buffers in the distribution path which can be configured depending on the route selected. By disabling unused buffers, unwanted signals can be isolated and unneeded current consumption can be eliminated.

7.3.9 Output Buffer

Each output buffer (A and B) have programmable gain with register OUTA_POW and OUTB_POW. The RF output buffer configuration is open-collector and requires an external pullup from RFout pin to V_{CC} . There are two pullup options that can be used with either resistor or inductor. Refer to the [Application and Implementation](#) section for design considerations.

1. Resistor pullup: placing a 50-Ω resistor pullup matches the output impedance to 50-Ω. However, maximum output power is limited. Output buffer current settings should be set to a value before output power is saturated (output power increases less for every step increase in output current value).
2. Inductor pullup: placing an inductor pullup creates a resonance at the frequency of interest. This offers higher output power for the same current and higher maximum output power. However, the output impedance is higher and additional matching may be required..

7.3.10 Phase Adjust

In fractional mode, the phase relationship between the output and the input can be changed with very fine resolution. Every time MASH_SEED register is written, it will trigger a phase shift of the amount described in [Equation 1](#). The seed value should be less than the fractional-N denominator register PLL_N_DEN. The actual phase shift can be obtained with the following equation:

$$\text{Phase shift (degrees)} = 360 \times \text{MASH_SEED} \times \text{PLL_N_PRE} / \text{PLL_N_DEN} / [\text{Channel divider value}] \quad (1)$$

7.4 Device Functional Modes

7.4.1 Power Down

Power up and down can be achieved using the CE pin (logic HIGH or LOW voltage) or the POWERDOWN register bit (0 or 1). When the device comes out of the powered-down state, either by pulling back CE pin HIGH (if it was powered down by CE pin) or by resuming the POWERDOWN bit to 0 (if it was powered down by register write), it is required that register R0 be programmed again to re-calibrate the device.

7.4.2 Lock Detect

The MUXout pin can be configured to output a signal that gives an indication for the PLL being locked. If lock detect is enabled (LD_EN = 1) and the MUXout pin is configured as lock detect output (MUXOUT_SEL = 1), when the device is locked, the MUXout pin output is a logic HIGH voltage, and when the device is unlocked, MUXout output is a logic LOW voltage.

7.4.3 Register Readback

The MUXout pin can be programmed (MUXOUT_SEL = 0) to use register readback serial data output. To read back a certain register value, use the following steps:

1. Set the R/W bit to 1; the data field contents are ignored.
2. Program this register to the device, readback serial data will be output starting at the 9th clock.

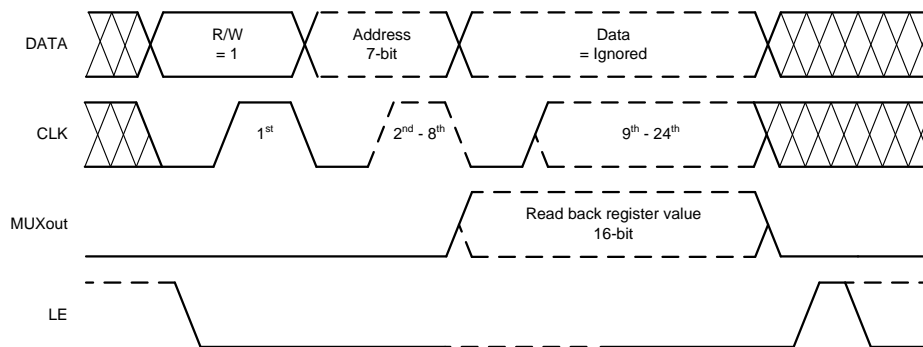


Figure 21. Register Readback Timing Diagram

7.5 Programming

The programming using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W (bit 23), 1 is read and 0 is write. The address field ADDRESS (bits 22:16) is used to decode the internal register address. The remaining 16 bits form the data field DATA (bits 15:0). While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes high, data is transferred from the data field into the selected register bank.

7.5.1 Recommended Initial Power on Programming Sequence

When the device is first powered up, the device needs to be initialized and the ordering of this programming is very important. After this sequence is completed, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure the V_{CC} pins are at the proper levels
2. Ensure that a valid reference is applied to the OSCin pin
3. Soft reset the device (write R0[1] = 1)
4. Program the remaining registers
5. Frequency calibrate (write R0[3] = 1)

Programming (continued)

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Set the new N divider value (write R38[12:1])
2. Set the new PLL numerator (R45 and R44) and denominator (R41 and R40)
3. Frequency calibrate (write R0[3] = 1)

7.6 Register Maps

7.6.1 LMX2582 Register Map – Default Values

Figure 22. Register Table

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	R/W	ADDRESS[6:0]										DATA [15:0]													
0	R/W	0	0	0	0	0	0	0	0	0	LD_EN	0	0	0	1	FCAL_HP FD_ADJ		FCAL_LP FD_ADJ		1	FCAL_EN	MUX_OUT_SEL	RESET	POWERDOWN	
1	R/W	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV			
2	R/W	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	
4	R/W	0	0	0	0	1	0	0	ACAL_CMP_DLY							0	1	0	0	0	0	0	1	1	
7	R/W	0	0	0	0	1	1	1	0	0	1	04	1	0	0	0	1	0	1	1	0	0	1	0	
8	R/W	0	0	0	1	0	0	0	0	0	VCO_IDA C_OVR	1	0	VC_OCAPCTRLOVR	0	0	1	0	0	0	0	1	0	0	
9	R/W	0	0	0	1	0	0	1	0	0	0	0	OSC_2X	0	REF_EN	1	0	0	0	0	0	0	1	0	
10	R/W	0	0	0	1	0	1	0	0	0	0	1	MULT					1	0	1	1	0	0	0	
11	R/W	0	0	0	1	0	1	1	0	0	0	0	PLL_R								1	0	0	0	
12	R/W	0	0	0	1	1	0	0	0	1	1	1	PLL_R_PRE												
13	R/W	0	0	0	1	1	0	1	0	CP_EN	0	0	0	0	PFD_CTL		0	0	0	0	0	0	0	0	
14	R/W	0	0	0	1	1	1	0	0	0	0	0	CP_IDN				CP_IUP				CP_ICOARSE				
19	R/W	0	0	1	0	0	1	1	0	0	0	0	VCO_IDAC									1	0	1	
20	R/W	0	0	1	0	1	0	0	0	0	0	0	0	0	ACAL_VCO_IDAC_STRT										
22	R/W	0	0	1	0	1	1	0	0	0	1	0	0	0	1	1	VCO_CAPCTRL								

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REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W	ADDRESS[6:0]										DATA [15:0]												
23	R/W	0	0	1	0	1	1	1	1	FCAL_VCO_SELECT	VCO_SEL			VCOSelforce	0	0	0	1	0	0	0	0	1	0
24	R/W	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1
25	R/W	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
28	R/W	0	0	1	1	1	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0
29	R/W	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
30	R/W	0	0	1	1	1	1	0	0	0	0	0	0	MASH_DITHER	0	0	0	0	1	1	0	1	0	0
31	R/W	0	0	1	1	1	1	1	0	0	0	0	0	VCO_DISTB_PD	VCO_DISTA_PD	0	CHDIV_IST_PD	0	0	0	0	0	0	1
32	R/W	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	1	0
33	R/W	0	1	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1	0
34	R/W	0	1	0	0	0	1	0	1	1	0	0	0	0	1	1	1	1	CHDIV_EN	0	1	0	1	0
35	R/W	0	1	0	0	0	1	1	0	0	0	CHDIV_SEG2				CHDIV_SEG3_EN	CHDIV_SEG2_EN	0	0	1	1	CHDIV_SEG1	CHDIV_SEG1_EN	1
36	R/W	0	1	0	0	1	0	0	0	0	0	CHDIV_DIB_EN	CHDIV_DISTA_EN	0	0	0	CHDIV_SEG_SEL			CHDIV_SEG3				
37	R/W	0	1	0	0	1	0	1	0	1	0	PLL_NPRE	0	0	0	0	0	0	0	0	0	0	0	0
38	R/W	0	1	0	0	1	1	0	0	0	0	PLL_N											0	
39	R/W	0	1	0	0	1	1	1	1	0	PFD_DLY						0	0	0	0	0	1	0	0
40	R/W	0	1	0	1	0	0	0	PLL_DEN[31:16]															
41	R/W	0	1	0	1	0	0	1	PLL_DEN[15:0]															
42	R/W	0	1	0	1	0	1	0	MASH_SEED[31:16]															
43	R/W	0	1	0	1	0	1	1	MASH_SEED[15:0]															

REG	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R/W ADDRESS[6:0]								DATA [15:0]															
44	R/W	0	1	0	1	1	0	0	PLL_NUM[31:16]															
45	R/W	0	1	0	1	1	0	1	PLL_NUM[15:0]															
46	R/W	0	1	0	1	1	1	0	0	0	OUTA_POW					OUT B_P D	OU TA _P D	MAS H_E N	1	0	MASH_ORDER			
47	R/W	0	1	0	1	1	1	1	0	0	0	OUTA_M UX		0	0	0	1	1	OUTB_POW					
48	R/W	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	OUTB_M UX	
59	R/W	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	MUX OUT _HD RV	0	0	0	0	0
61	R/W	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_ TYP E
62	R/W	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
64	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	ACA L_ F AST	FC AL _ F AST	AJUMP_SIZE		1	FJUMP_SIZE				

7.6.1.1 Register Descriptions

Table 5. R0 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14		R/W		Program to Register Map default values
13	LD_EN	R/W	1	Lock detect enable 1: enable 0: disable
12:9		R/W		Program to Register Map default values
8:7	FCAL_HPFD_ADJ	R/W	0	Used for when PFD freq is high 3: PFD > 200 MHz 2: PFD > 150 MHz 1: PFD > 100 MHz 0: not used
6:5	FCAL_LPFD_ADJ	R/W	0	Used for when PFD freq is low 3: PFD < 5 MHz 2: PFD < 10 MHz 1: PFD < 20 MHz 0: not used
4	ACAL_EN	R/W	1	Enable amplitude calibration 1: enable (calibration algorithm will set VCO amplitude. For manual mode set register VCO_IDAC_OVR=1, and then set the VCO amplitude by register VCO_IDAC) 0: disable
3	FCAL_EN	R/W	1	Enable frequency calibration 1: enable (writing 1 to this register triggers the calibration sequence) 0: disable
2	MUXOUT_SEL	R/W	1	Signal at MUXOUT pin 1: Lock Detect (3.3 V if locked, 0 V if unlocked) 0: Readback (3.3-V digital output)

Table 5. R0 Register Field Descriptions (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1	RESET	R/W	0	Reset Write with a value of 1 to reset device (this register will self-switch back to 0)
0	POWERDOWN	R/W	0	Powerdown whole device 1: power down 0: power up

Table 6. R1 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:3		R/W		Program to Register Map default values
2:0	CAL_CLK_DIV	R/W	3	Divides down the OSCin signal for calibration clock Calibration Clock = OSCin / 2 ^{CAL_CLK_DIV} Set this value so that calibration clock is less than but as close to 200MHz as possible if fast calibration time is desired.

Table 7. R2 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 8. R4 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	ACAL_CMP_DLY	R/W	25	VCO amplitude calibration delay. Lowering this value can speed calibration time
7:0		R/W		Program to Register Map default values

Table 9. R7 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 10. R8 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14		R/W		Program to Register Map default values
13	VCO_IDAC_OVR	R/W	0	This is the over-ride bit for VCO amplitude (or IDAC value). When this is enabled, the VCO amplitude calibration function (ACAL_EN) is not used. VCO_IDAC register can be programmed to set the amplitude. Keep the VCO_IDAC value within 250 and 450.
12:11		R/W		Program to Register Map default values
10	VCO_CAPCTRL_OVR	R/W	0	This is the over-ride bit for VCO capacitor bank code (or CAPCTRL value). When this is enabled, the VCO frequency calibration function (FCAL_EN) is not used. the VCO_CAPCTRL register can be programmed to set the VCO frequency within the selected VCO core. The VCO core is selected by setting VCO_SEL_FORCE=1 and then selecting the core with VCO_SEL=1,2,3,4,5,6, or 7
9:0		R/W		Program to Register Map default values

Table 11. R9 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11	OSC_2X	R/W	0	Reference path doubler 1: enable 0: disable
10		R/W		Program to Register Map default values
9	REF_EN	R/W	1	Enable reference path 1: enable 0: disable
8:0		R/W		Program to Register Map default values

Table 12. R10 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11:7	MULT	R/W	1	Input signal path multiplier (input range from 40 - 70 MHz, output range from 180 - 250 MHz)
6:0		R/W		Program to Register Map default values

Table 13. R11 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11:4	PLL_R	R/W	1	R divider after multiplier and before PFD
3:0		R/W		Program to Register Map default values

Table 14. R12 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11:0	PLL_R_PRE	R/W	1	R divider after OSCin doubler and before multiplier

Table 15. R13 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15		R/W		Program to Register Map default values
14	CP_EN	R/W	1	Enable charge pump 1: enable 0: disable
13:10		R/W		Program to Register Map default values
9:8	PFD_CTL	R/W	0	PFD mode 0: Dual PFD (default) 3: Single PFD (ONLY use if PFD freq is higher than 200MHz)
7:0		R/W		Program to Register Map default values

Table 16. R14 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11:7	CP_IDN	R/W	3	Charge pump current (DN) – must equal to charge pump current (UP). Can activate any combination of bits. <bit 4>: 1.25 mA <bit 3>: 2.5 mA <bit 2>: 0.625 mA <bit 1>: 0.312 mA <bit 0>: 0.156 mA
6:2	CP_IUP	R/W	3	Charge pump current (UP) – must equal to charge pump current (DN). Can activate any combination of bits. <bit 4>: 1.25 mA <bit 3>: 2.5 mA <bit 2>: 0.625 mA <bit 1>: 0.312 mA <bit 0>: 0.156 mA
1:0	CP_ICOARSE	R/W	1	charge pump gain multiplier - multiplies charge pump current by a given factor: 3: multiply by 2.5 2: multiply by 1.5 1: multiply by 2 0: no multiplication

Table 17. R19 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11:3	VCO_IDAC	R/W	300	This is the VCO amplitude (or IDAC value). When VCO_IDAC is over-riden with VCO_IDAC_OVR=1, VCO amplitude calibration function (ACAL_EN) is not used. VCO_IDAC register can be programmed to set the amplitude. VCO_IDAC value must be kept within 250 and 450.

Table 17. R19 Register Field Descriptions (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
2:0		R/W		Program to Register Map default values

Table 18. R20 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:9		R/W		Program to Register Map default values
8:0	ACAL_VCO_IDAC_STRT	R/W	300	This register is used to aid the VCO amplitude calibration function (ACAL_EN). By default the amplitude calibration function searches from the low end of VCO_IDAC until it reaches the target value. This can be set to a value closer to the target value, then the amplitude calibration time can be shortened (suggested value 300).

Table 19. R22 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8		R/W		Program to Register Map default values
7:0	VCO_CAPCTRL	R/W	0	This is the VCO capacitor bank code (or CAPCTRL value). When VCO_CAPCTRL is over-riden with VCO_CAPCTRL_OVR=1, VCO frequency calibration function (FCAL_EN) is not used. VCO_CAPCTRL register can be programmed to set the frequency in that core. VCO_SEL_FORCE=1 has to be set and VCO_SEL to select the VCO core, then CAPCTRL values between 0 to 183 will produce frequencies within this core (0 being the highest frequency and 183 the lowest).

Table 20. R23 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15		R/W		Program to Register Map default values
14	FCAL_VCO_SEL_STRT	R/W	0	This is a register that aids the frequency calibration function. When this is enabled, a VCO core can be selected for the frequency calibration to start at, set by register VCO_SEL. By default the frequency calibration starts from VCO core 7 and works its way down. If you want for example to lock to a frequency in VCO core 1, you can set VCO_SEL to 2, so the calibration will start at VCO core 2 and end at target frequency at VCO core 1 faster.
13:11	VCO_SEL	R/W	1	This is the register used to select VCO cores. It works for VCO_CAPCTRL when VCO_CAPCTRL_OVR=1 and VCO_SEL_FORCE=1. It also aids the frequency calibration function with FCAL_VCO_SEL_STRT.
10	VCO_SEL_FORCE	R/W	0	This register works to force selection of VCO cores. If VCO_CAPCTRL_OVR=1 and this register is enabled, you can select the VCO core to use with VCO_SEL.
9:0		R/W		Program to Register Map default values

Table 21. R24 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to default

Table 22. R25 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 23. R28 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 24. R29 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 25. R30 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11		R/W		Program to Register Map default values
10	MASH_DITHER	R/W	0	MASH dithering: toggle on/off to randomize
9:1		R/W		Program to Register Map default values
0	VCO_2X_EN	R/W	0	Enable VCO doubler 1: enable 0: disable

Table 26. R31 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11		R/W		Program to Register Map default values
10	VCO_DISTB_PD	R/W	1	Power down buffer between VCO and output B 1: power down 0: power up
9	VCO_DISTA_PD	R/W	0	Power down buffer between VCO and output A 1: power down 0: power up
8		R/W		Program to Register Map default values
7	CHDIV_DIST_PD	R/W	0	Power down buffer between VCO and channel divider
6:0		R/W		Program to Register Map default values

Table 27. R32 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 28. R33 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 29. R34 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:6		R/W		Program to Register Map default values
5	CHDIV_EN	R/W	1	Enable entire channel divider 1: enable 0: power down
4:0		R/W		Program to Register Map default values

Table 30. R35 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to Register Map default values
12:9	CHDIV_SEG2	R/W	1	Channel divider segment 2 8: divide-by-8 4: divide-by-6 2: divide-by-4 1: divide-by-2 0: PD
8	CHDIV_SEG3_EN	R/W	0	Channel divider segment 3 1: enable 0: power down (power down if not needed)
7	CHDIV_SEG2_EN	R/W	0	Channel divider segment 2 1: enable 0: power down (power down if not needed)
6:3		R/W		Program to Register Map default values
2	CHDIV_SEG1	R/W	1	Channel divider segment 1 1: divide-by-3 0: divide-by-2
1	CHDIV_SEG1_EN	R/W	0	Channel divider segment 1 1: enable 0: power down (power down if not needed)

Table 30. R35 Register Field Descriptions (continued)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0		R/W		Program to Register Map default values

Table 31. R36 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12		R/W		Program to Register Map default values
11	CHDIV_DISTB_EN	R/W	0	Enable buffer between channel divider and output B 1: enable 0: disable
10	CHDIV_DISTA_EN	R/W	1	Enable buffer between channel divider and output A 1: enable 0: disable
9:7		R/W		Program to Register Map default values
6:4	CHDIV_SEG_SEL	R/W	1	Channel divider segment select 4: includes channel divider segment 1,2 and 3 2: includes channel divider segment 1 and 2 1: includes channel divider segment 1 0: PD
3:0	CHDIV_SEG3	R/W	1	Channel divider segment 3 8: divide-by-8 4: divide-by-6 2: divide-by-4 1: divide-by-2 0: PD

Table 32. R37 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to Register Map default values
12	PLL_N_PRE	R/W	0	N-divider pre-scalar 1: divide-by-4 0: divide-by-2
11:0		R/W		Program to Register Map default values

Table 33. R38 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to Register Map default values
12:1	PLL_N	R/W	27	Integer part of N-divider
0		R/W		Program to Register Map default values

Table 34. R39 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14		R/W		Program to Register Map default values
13:8	PFD_DLY	R/W	2	PFD Delay 32: Not used 16: 16 clock cycle delay 8: 12 clock cycle delay 4: 8 clock cycle delay 2: 6 clock cycle delay 1: 4 clock cycle delay
7:0		R/W		Program to Register Map default values

Table 35. R40 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_DEN[31:16]	R/W	1000	Denominator MSB of N-divider fraction

Table 36. R41 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_DEN[15:0]	R/W	1000	Denominator LSB of N-divider fraction

Table 37. R42 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	MASH_SEED[31:16]	R/W	0	MASH seed MSB

Table 38. R43 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	MASH_SEED[15:0]	R/W	0	MASH seed LSB

Table 39. R44 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_NUM[31:16]	R/W	0	Numerator MSB of N-divider fraction

Table 40. R45 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	PLL_NUM[15:0]	R/W	0	Numerator LSB of N-divider fraction

Table 41. R46 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15		R/W		Program to Register Map default values
13:8	OUTA_POW	R/W	15	Output buffer A power increase power from 0 to 31 extra boost from 48 to 63
7	OUTB_PD	R/W	1	Output buffer B power down 1: power down 0: power up
6	OUTA_PD	R/W	0	Output buffer A power down 1: power down 0: power up
5	MASH_EN	R/W	1	Enable sigma-delta modulator
4:3		R/W		Program to Register Map default values
2:0	MASH_ORDER	R/W	3	Sigma-delta modulator order 4: fourth order 3: third order 2: second order 1: first order 0: integer mode

Table 42. R47 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13		R/W		Program to Register Map default values
12:11	OUTA_MUX	R/W	0	Selects signal to the output buffer 2,3: reserved 1: Selects output from VCO 0: Selects the channel divider output
10:6		R/W		Program to Register Map default values
5:0	OUTB_POW	R/W	0	Output buffer B power increase power from 0 to 31 extra boost from 48 to 63

Table 43. R48 Register Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:2		R/W		Program to Register Map default values
1:0	OUTB_MUX	R/W	0	Selects signal to the output buffer 2,3: reserved 1: Selects output from VCO 0: Selects the channel divider output

Table 44. R59 Register Field Descriptions

BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
15:6		R/W		Program to Register Map default values
5	MUXOUT_HDRV	R/W	0	This bit enables higher current output at MUXOUT pin if value is 1.
4:0		R/W		Program to Register Map default values

Table 45. R61 Register Field Descriptions

BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
15:1		R/W		Program to Register Map default values
0	LD_TYPE	R/W	1	To use lock detect, set MUXOUT_SEL=1. Use this register to select type of lock detect: 0: Calibration status detect (this indicates if the auto-calibration process has completed successfully and will output from MUXout pin a logic HIGH when successful). 1: vtune detect (this checks if vtune is in the expected range of voltages and outputs from MUXout pin a logic HIGH if device is locked and LOW if unlocked).

Table 46. R62 Register Field Descriptions

BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0		R/W		Program to Register Map default values

Table 47. R64 Register Field Descriptions

BITS	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10		R/W		Program to Register Map default values
9	ACAL_FAST	R/W	0	Enable fast amplitude calibration 1: enable 0: disable
8	FCAL_FAST	R/W	0	Enable fast frequency calibration 1: enable 0: disable
7:5	AJUMP_SIZE	R/W	3	When ACAL_FAST=1, use this register to select the jump increment
4		R/W		Program to Register Map default values
3:0	FJUMP_SIZE	R/W	15	When FCAL_FAST=1, use this register to select the jump increment

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Optimization of Spurs

8.1.1.1 Understanding Spurs by Offsets

The first step in optimizing spurs is to be able to identify them by offset. Figure 23 gives a good example that can be used to isolate the following spur types.

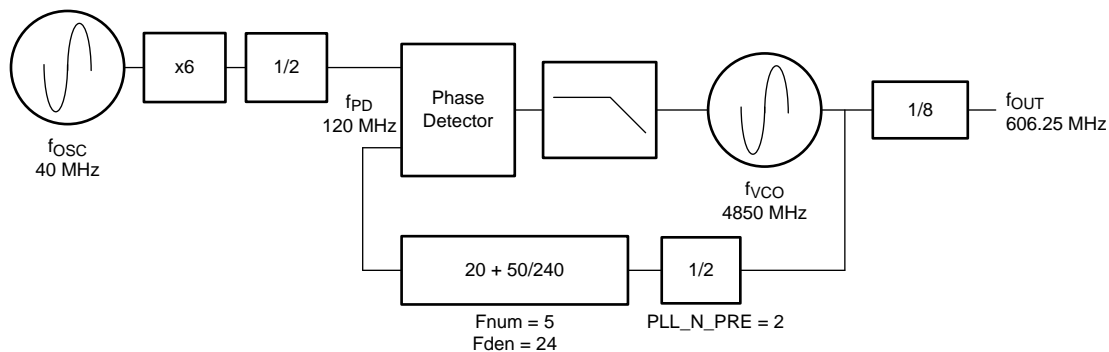


Figure 23. Spur Offset Frequency Example

Based on Figure 23, the most common spurs can be calculated from the frequencies. Note that the % is the modulus operator and is meant to mean the difference to the closest integer multiple. Some examples of how to use this operator are: $36 \% 11 = 3$, $1000.1 \% 50 = 0.1$, and $5023.7 \% 122.88 = 14.38$. Applying this concept, the spurs at various offsets can be identified from Figure 23.

Table 48. Spur Definition Table

SPUR TYPE	OFFSET	OFFSET IN Figure 23	COMMENTS
OSCin	f_{osc}	40 MHz	This spur occurs at harmonics of the OSCin frequency.
Fpd	f_{PD}	120 MHz	The phase detector spur has many possible mechanisms and occurs at multiples of the phase detector frequency.
$f_{OUT} \% f_{OSC}$	$f_{OUT} \% f_{OSC}$	$606.25 \% 40 = 6.25$ MHz	This spur is caused by mixing between the output and input frequencies.
$f_{VCO} \% f_{OSC}$	$f_{VCO} \% f_{OSC}$	$4850 \% 40 = 10$ MHz	This spur is caused by mixing between the VCO and input frequencies.
$f_{VCO} \% f_{PD}$	$f_{VCO} \% f_{PD}$	$4850 \% 120 = 50$ MHz	This spur would be the same offset as the integer boundary spur if PLL_N_PRE=1, but can be different if this value is greater than one.
Integer Boundary	$f_{PD} * (Fnum \% Fden) / Fden$	$120 \times (5 \% 24) / 24 = 25$ MHz	This is a single spur
Primary Fractional	$f_{PD} / Fden$	$120 / 24 = 5$ MHz	The primary fractional

Application Information (continued)
Table 48. Spur Definition Table (continued)

SPUR TYPE	OFFSET	OFFSET IN Figure 23	COMMENTS
Sub-Fractional	$f_{PD} / F_{den} / k$ $k=2,3, \text{ or } 6$	First Order Modulator: None 2nd Order Modulator: $120/24/2 = 2.5$ MHz 3rd Order Modulator: $120/24/6 = 0.83333$ MHz 4th Order Modulator: $120/24/12 = 0.416666$ MHz	To Calculate k: 1st Order Modulator: $k=1$ 2nd Order Modulator: $k=1$ if Fden is odd, $k=2$ if Fden is even 3rd Order Modulator: $k=1$ if Fden not divisible by 2 or 3, $k=2$ if Fden divisible by 2 not 3, $k=3$ if Fden divisible by 3 but not 2, Fden = 6 if Fden divisible by 2 and 3 4th Order Modulator: $k=1$ if Fden not divisible by 2 or 3, $k=3$ if Fden divisible by 3 but not 2, $k=4$ if Fden divisible by 2 but not 3, $k=12$ if Fden divisible by 2 and 3 Sub-Fractional Spurs exist if $k>1$

In the case that two different spur types occur at the same offset, either name would be correct. Some may name this by the more dominant cause, while others would simply name by choosing the name that is near the top of [Table 48](#).

8.1.1.2 Spur Mitigation Techniques

Once the spur is identified and understood, there will likely be a desire to try to minimize them. [Table 49](#) gives some common methods.

Table 49. Spurs and Mitigation Techniques

SPUR TYPE	WAYS TO REDUCE	TRADE-OFF
OSCI _n	1. Use PLL_N_PRE = 2 2. Use an OSC _n signal with low amplitude and high slew rate (like LVDS).	
Phase Detector	1. Decrease PFD_DLY 2. To pin 11, use a series ferrite bead and a shunt 0.1-μF capacitor.	
$f_{OUT} \% f_{OSC}$	Use an OSC _n signal with low amplitude and high slew rate (like LVDS)	
$f_{VCO} \% f_{OSC}$	1. To pin 7, use a series ferrite bead and a shunt 0.1-μF capacitor. 2. Increase the offset of this spur by shifting the VCO frequency 3. If multiple VCO frequencies are possible that yield the same spur offset, choose the higher VCO frequency.	
$f_{VCO} \% f_{PD}$	Avoid this spur by shifting the phase detector frequency (with the programmable input multiplier or R divider) or shifting the VCO frequency. This spur is better at higher VCO frequency.	
Integer Boundary	Methods for PLL Dominated Spurs 1. Avoid the worst case VCO frequencies if possible. 2. Strategically choose which VCO core to use if possible. 3. Ensure good slew rate and signal integrity at the OSC _n pin 4. Reduce the loop bandwidth or add more filter poles for out of band spurs 5. Experiment with modulator order and PFD_DLY	Reducing the loop bandwidth may degrade the total integrated noise if the bandwidth is too narrow.
	Methods for VCO Dominated Spurs 1. Avoid the worst case VCO frequencies if possible. 2. Reduce Phase Detector Frequency 3. Ensure good slew rate and signal integrity at the OSC _n pin 4. Make the impedance looking outwards from the OSC _n pin close to 50 Ω.	Reducing the phase detector may degrade the phase noise and also reduce the capacitance at the Vtune pin.

Table 49. Spurs and Mitigation Techniques (continued)

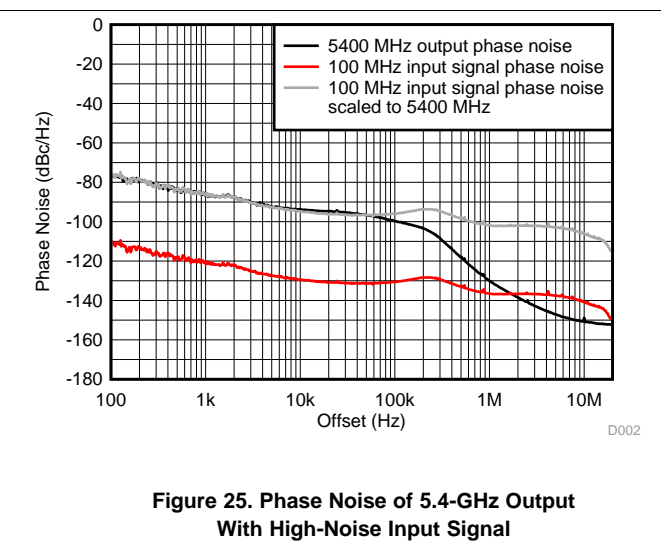
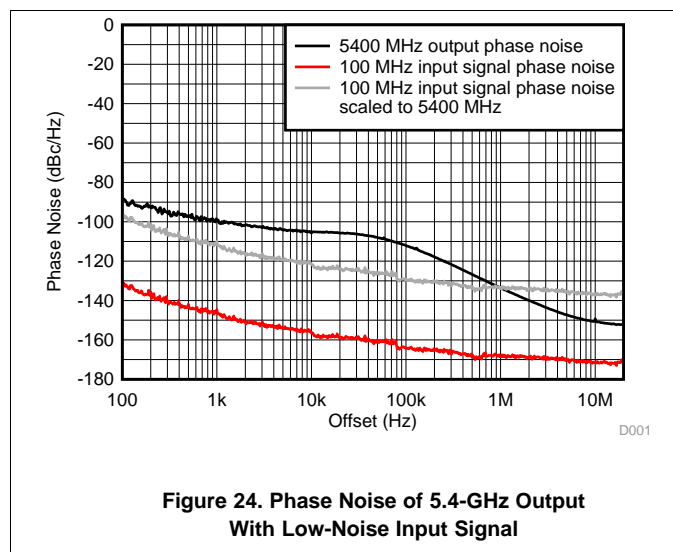
SPUR TYPE	WAYS TO REDUCE	TRADE-OFF
Primary Fractional	<ol style="list-style-type: none"> 1. Decrease Loop Bandwidth 2. Change Modulator Order 3. Use Larger Unequivalent Fractions 	Decreasing the loop bandwidth too much may degrade in-band phase noise. Also, larger unequivalent fractions only sometimes work
Sub-Fractional	<ol style="list-style-type: none"> 1. Use Dithering 2. Use MASH seed 3. Use Larger Equivalent Fractions 4. Use Larger Unequivalent Fractions 5. Reduce Modulator Order 6. Eliminate factors of 2 or 3 in denominator (see AN-1879 Fractional N Frequency Synthesis (SNAA062)) 	Dithering and larger fractions may increase phase noise. MASH_SEED can be set between values 0 and Fden, which changes the sub-fractional spur behavior. This is a deterministic relationship and there will be one seed value that will give best result for this spur.

8.1.2 Configuring the Input Signal Path

The input path is considered the portion of the device between the OSCin pin and the phase detector, which includes the input buffer, R dividers, and programmable multipliers. The way that these are configured can have a large impact on phase noise and fractional spurs.

8.1.2.1 Input Signal Noise Scaling

The input signal noise scales by $20 \times \log(\text{output frequency} / \text{input signal frequency})$, so always check this to see if the noise of the input signal scaled to the output frequency is close to the PLL in-band noise level. When that happens, the input signal noise is the dominant noise source, not the PLL noise floor.



8.1.3 Input Pin Configuration

The OSCinM and OSCinP can be used to support both a single-ended or differential clock. In either configuration, the termination on both sides should match for best common-mode noise rejection. The slew rate and signal integrity of this signal can have an impact on both the phase noise and fractional spurs. Standard clocking types, LVDS, LVPECL, HCSL, and CMOS can all be used.

8.1.4 Using the OSCin Doubler

The lowest PLL flat noise is achieved with a low-noise 200-MHz input signal. If only a low-noise input signal with lower frequency is available (for example a 100-MHz source), you can use the low noise OSCin doubler to attain 200-MHz phase detector frequency. Because $\text{PLL_flat} = \text{PLL_FOM} + 20 \times \log(\text{Fvco}/\text{Fpd}) + 10 \times \log(\text{Fpd} / 1\text{Hz})$, doubling Fpd theoretically gets -6 dB from the $20 \times \log(\text{Fvco}/\text{Fpd})$ component, $+3$ dB from the $10 \times \log(\text{Fpd} / 1\text{Hz})$ component, and cumulatively a -3 -dB improvement.

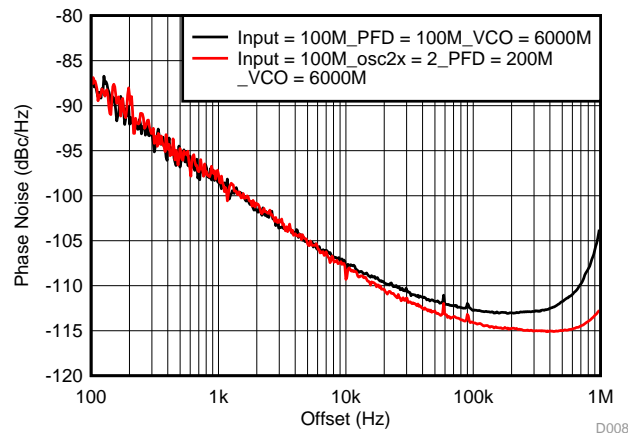


Figure 26. 100MHz Input With OSCin Doubler

8.1.5 Using the Input Signal Path Components

The ideal input is a low-noise, 200-MHz (or multiples of it) signal and 200-MHz phase detector frequency (highest dual PFD frequency). However, if spur mechanisms are understood, certain combinations of the R-divider and Multiplier can help. Refer to the [Optimization of Spurs](#) section for understanding spur types and their mechanisms first, then try this section for these specific spurs.

8.1.5.1 Moving Phase Detector Frequency

Engaging the multiplier in the reference path allows more flexibility in setting the PFD frequency. One example use case of this is if $F_{vco} \% F_{pd}$ is the dominant spur. This method can move the PFD frequency and thus the $F_{vco} \% F_{pd}$.

Example: $F_{vco} = 3720.12$ MHz, $F_{osc} = 300$ MHz, Pre-R divider = 5, $F_{pd} = 60$ MHz, $F_{vco} \% F_{osc} = 120.12$ MHz (Far out), $F_{vco} \% F_{pd} = 120$ kHz (dominant). There is a $F_{vco} \% F_{pd}$ spur at 120 kHz (refer to [Figure 27](#)).

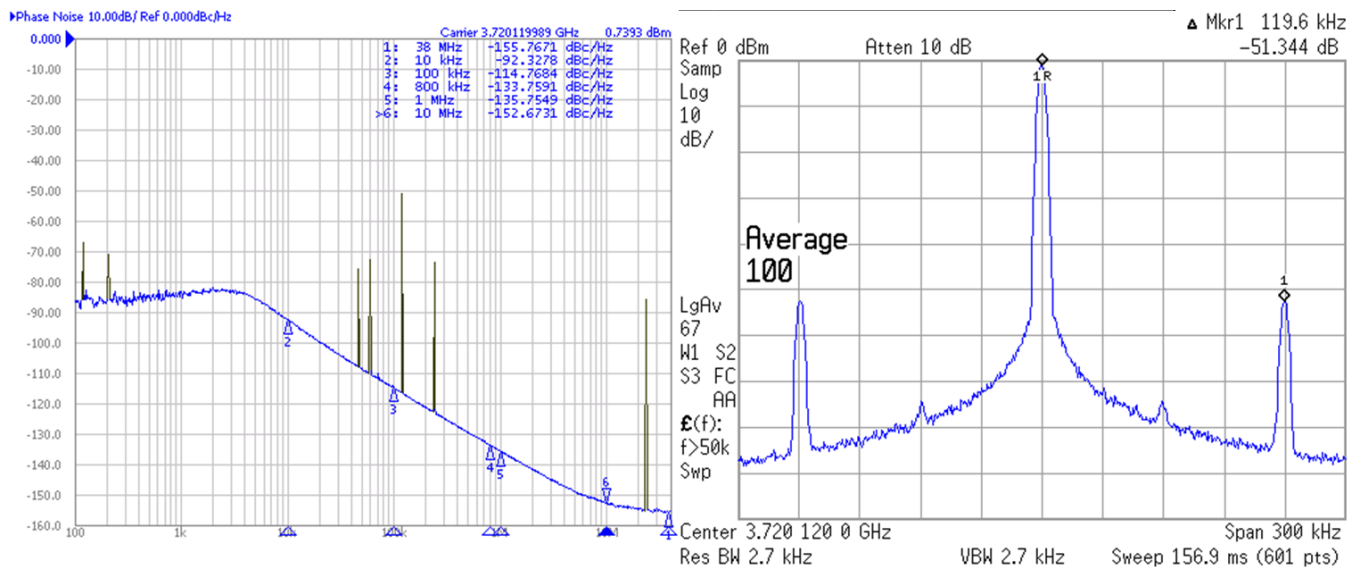


Figure 27. $F_{vco} \% F_{pd}$ Spur

Then second case, using divider and multiplier, is $F_{pd} = 53.57$ MHz away from 120-kHz spur. $F_{vco} = 3720.12$ MHz, $F_{osc} = 300$ MHz, Pre-R divider = 7, Multiplier = 5, Post-R divider = 4, $F_{pd} = 53.57$ MHz, $F_{vco} \% F_{osc} = 120.12$ MHz (Far out). $F_{vco} \% F_{pd} = 23.79$ MHz (far out). There is a 20-dB reduction for the $F_{vco} \% F_{pd}$ spur at 120 kHz (refer to [Figure 28](#)).

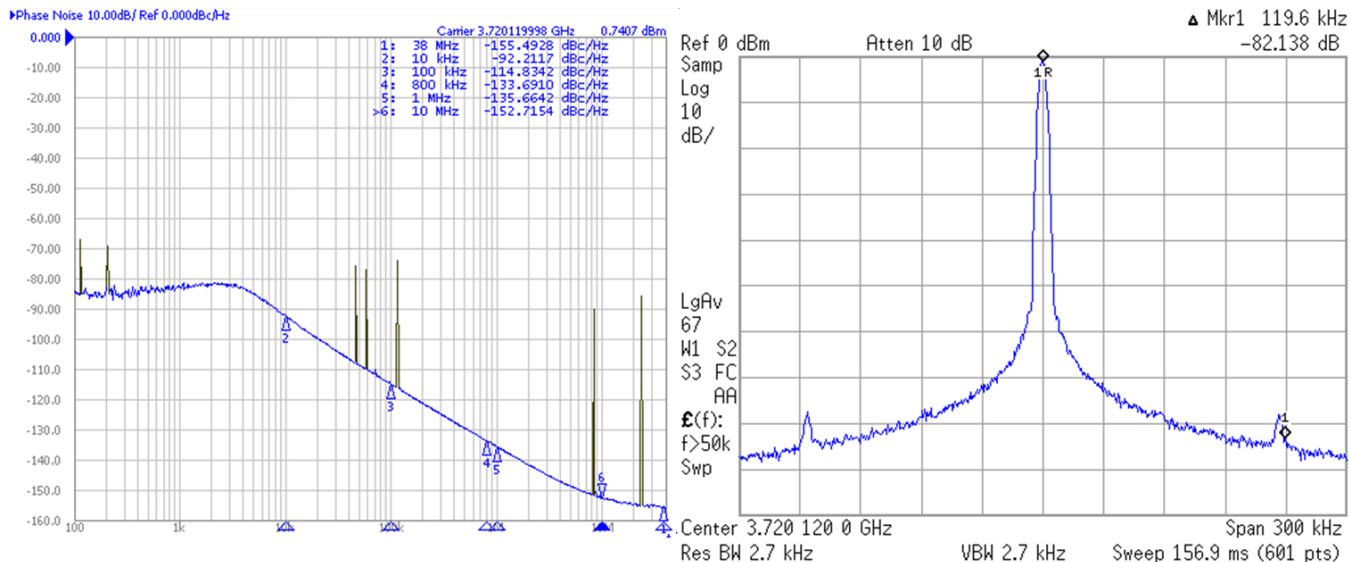


Figure 28. Moving Away From Fvco % Fpd Spur

8.1.5.2 Multiplying and Dividing by the Same Value

Although it may not seem like the first thing to try, the Fvco%Fosc and Fout%Fosc spur can sometimes be improved engaging the OSC_2X bit and then dividing by 2. Although this gives the same phase detector frequency, the spur can be improved.

8.1.6 Designing for Output Power

If there is a desired frequency for highest power, use an inductor pullup and design for the value so that the resonance is at that frequency. Use the formula $SRF = 1 / (2\pi \times \sqrt{L \times C})$.

Example: C = 1.4 pF (characteristic). If maximum power is targeted at 1 GHz, L = 18 nH. If maximum power is targeted at 3.3 GHz, L = 1.6 nH

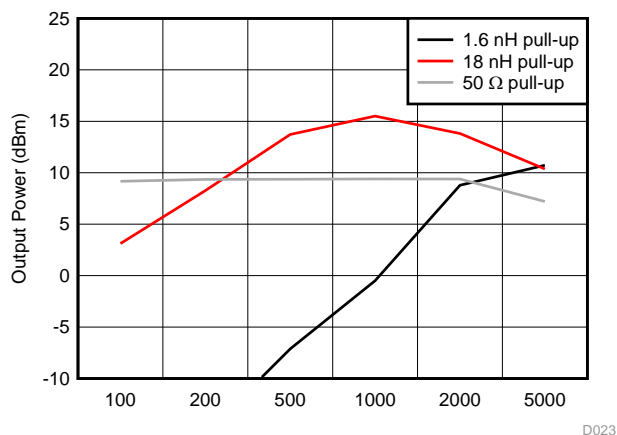


Figure 29. Output Power vs Pullup Type

8.1.7 Current Consumption Management

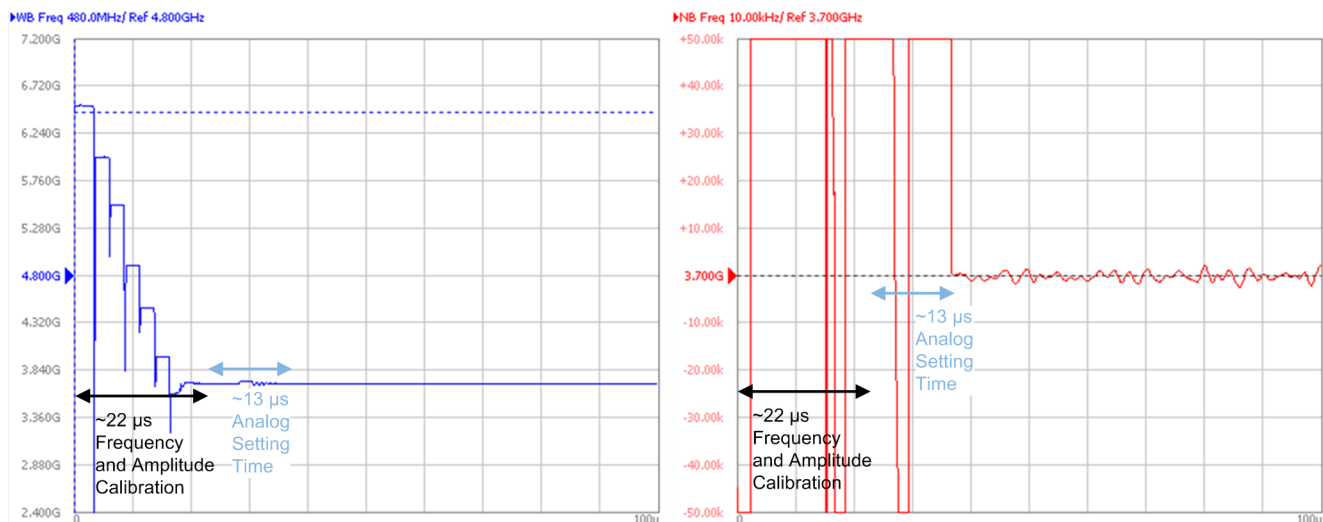
The starting point is the typical total current consumption of 250 mA: 100-MHz input frequency, OSCin doubler bypassed, Pre-R divider bypassed, multiplier bypassed, post-R divider bypassed, 100-MHz phase detector frequency, 0.468-mA charge pump current, channel divider off, one output on, 5400-MHz output frequency, 50-Ω output pullup, 0-dBm output power (differential). To understand current consumption changes due to engaging different functional blocks, refer to Table 50.

Table 50. Typical Current Consumption Impact By Function

ACTION	STEPS	PROGRAMMING	INCREASE IN CURRENT (mA)
Use input signal path	Enable OSCin doubler	OSC_2X = 1	7
	Enable multiplier	MULT = 3,4,5, or 6	10
Add an output	Route VCO to output B	VCO_DISTB_PD = 0	8
	Enable output B buffer	OUTB_PD = 0	54
Increase output power from 0 to +10dBm (differential)	Set highest output buffer current	OUTA_POW = 63	53
Use channel divider	Route channel divider to output	CHDIV_DISTA_EN = 1	5
	Enable channel divider	CHDIV_EN = 1	18
	Enable chdiv_seg1	CHDIV_SEG1_EN = 1	2
	Enable chdiv_seg2	CHDIV_SEG2_EN = 1	5
	Enable chdiv_seg3	CHDIV_SEG3_EN = 1	5

8.1.8 Decreasing Lock Time

A calibration time of 590 μ s typically to lock to 7-GHz VCO can be achieved with default settings as specified in the [Electrical Characteristics](#) table. There are several registers that can be programmed to speed up this time. Lock time consists of the calibration time (time required to calibrate the VCO to the correct frequency range) plus the analog settling time (time lock the PLL in phase and frequency). For fast calibration set registers FCAL_FAST = 1 and ACAL_FAST = 1. Also set the calibration clock frequency [input reference frequency] / 2[^]CAL_CLK_DIV) to 200 MHz. The 20- μ s range lock time can be achieved if the amplitude comparator delay is low, set by register ACAL_CMP_DLY (5 in this example). If this is too low there is not enough time to make the decision of VCO amplitude to use and may result in non-optimal phase noise. The other approach is to turn off amplitude calibration with ACAL_EN=0, then manually choose the amplitude with VCO_IDAC (350 for example). This will also result in 20- μ s range calibration time. There are many other registers that can aid calibration time, for example ACAL_VCO_IDAC_STRT lets the user choose what VCO amplitude to start with during amplitude calibration. Setting this value to around 350 will give faster times because it is close to the final amplitude for most final frequencies. FCAL_VCO_SEL_START allows you to choose the VCO core to start with for the calibration instead of starting from core 7 by default. If you know you are locking to a frequency around VCO core 1, you can start from VCO 2 by setting VCO_SEL=2, which should give faster lock times. Go to the [Register Maps](#) section for detailed information of these registers and their related registers. For fast analog settling time, design loop filter for very wide loop bandwidth (MHz range).


Figure 30. Lock Time Screenshot

The calibration sweeps from the top of the VCO frequency range to the bottom. This example does a calibration to lock at 3.7 GHz (which is the worst case). For the left screenshot (Wideband Frequency view), see the sweeping from top to bottom of the VCO range. On the right screenshot (Narrowband Frequency view), see the analog settling time to the precise target frequency.

8.1.9 Modeling and Understanding PLL FOM and Flicker Noise

Follow these recommended settings to design for wide loop bandwidth and extract FOM and flicker noise. The flat model is the PLL noise floor modeled by: $PLL_flat = PLL_FOM + 20 \times \log(F_{vco}/F_{pd}) + 10 \times \log(F_{pd} / 1 \text{ Hz})$. The flicker noise (also known as 1/f noise) which changes by $-10\text{dB} / \text{decade}$, is modeled by: $PLL_flicker(\text{offset}) = PLL_flicker_Norm + 20 \times \log(F_{vco} / 1 \text{ GHz}) - 10 \times \log(\text{offset} / 10\text{k Hz})$. The cumulative model is the addition of both components: $PLL_Noise = 10 \times \log(10 \times PLL_Flat / 10 + 10 \times PLL_flicker / 10)$. This is adjusted to fit the the measured data to extract the PLL_FOM and $PLL_flicker_Norm$ spec numbers.

Table 51. Wide Loop Filter Design

PARAMETER	VALUE
PFD (MHz)	200
Charge pump (mA)	12
VCO frequency (MHz)	5400
Loop bandwidth (kHz)	2000
Phase margin (degrees)	30
Gamma	1.4
Loop filter (2nd order)	
C1 (nF)	0.01
C2 (nF)	0.022
R2 (kΩ)	4.7

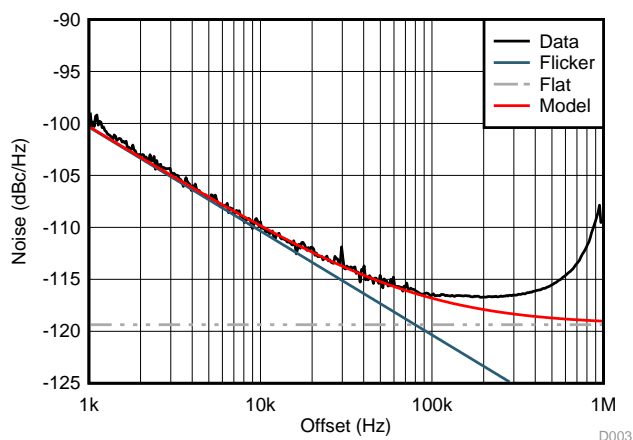


Figure 31. FOM and Flicker Noise Modeling

8.2.1.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. As a rule of thumb, jitter is lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this as longer lock times and spurs should be considered in design as well.

8.2.1.3 Application Curve

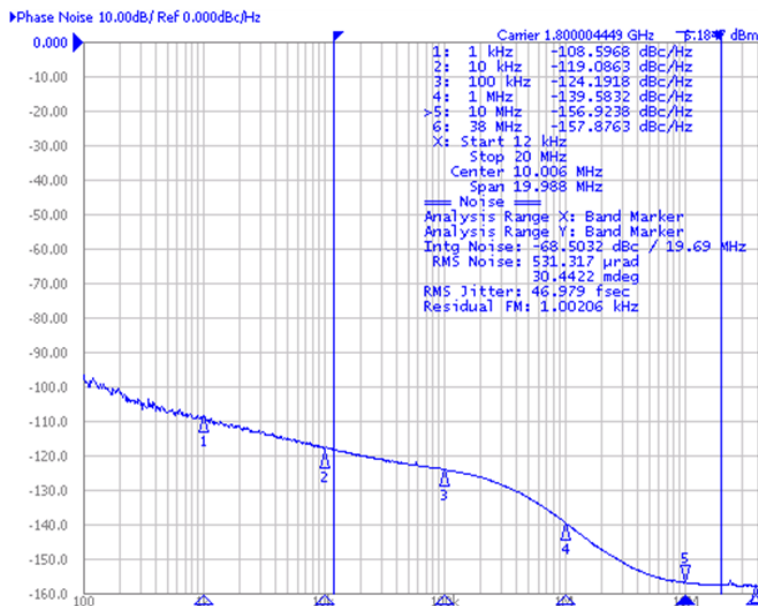


Figure 33. Typical Jitter

9 Power Supply Recommendations

TI recommends placing 100-nF spurs close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree.

10 Layout

10.1 Layout Guidelines

See EVM instructions for details. In general, the layout guidelines are similar to most other PLL devices. The followings are some outstanding guidelines.

- Place output pull up components close to the pin.
- Place capacitors close to the pins.
- Make sure input signal trace is well matched.
- Do not route any traces that carrying switching signal close to the charge pump traces and external VCO.

10.2 Layout Example

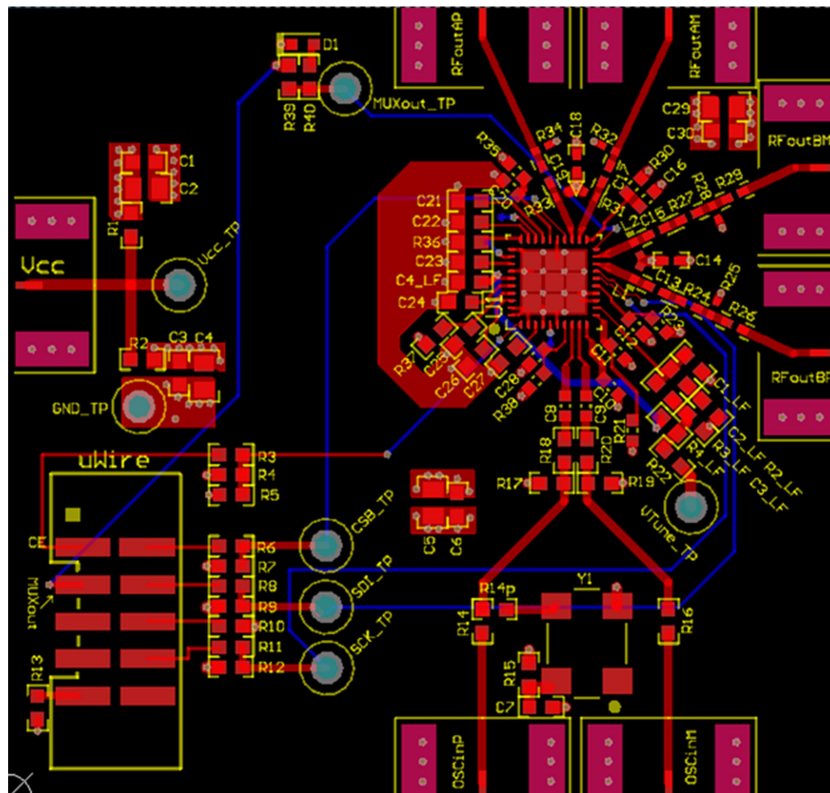


Figure 34. Recommended Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

德州仪器 (TI) 在 www.ti.com 提供了多种辅助开发的软件工具。其中包括:

- **CodeLoader**, 通过该工具可以了解如何对 EVM 板编程。
- **时钟设计工具**, 用于设计回路滤波器以及对相位噪声和杂散进行仿真。
- **EVM 板说明**, 用于了解包含详细测量条件的典型测量数据以及完整设计。
- **时钟架构**, 用于相应器件的设计和仿真并了解其如何与其他器件搭配使用。

11.2 文档支持

11.2.1 相关文档

以下为推荐读物。

- 《**AN-1879 分数 N 频率合成**》(SNAA062)
- 《**PLL 性能、仿真和设计手册**》(SNAA106)
- 《**通过降压转换器运行的 9.8GHz 射频高性能合成器参考设计**》(TIDUC22)
- 《**射频采样 S 频带雷达接收器参考设计**》(TIDUBS6)
- 《**采用集成式合成器和杂散抑制技术的 9.8GHz 射频 CW 信号发生器参考设计**》(TIDUBM1)
- 《**2GHz 复合带宽直流耦合 14 位数字转换器参考设计**》(TIDRLM6)

11.3 接收文档更新通知

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11.4 社区资源

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时, 我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本, 请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2582RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2582	Samples
LMX2582RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	LMX2582	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2582RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
LMX2582RHAT	VQFN	RHA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

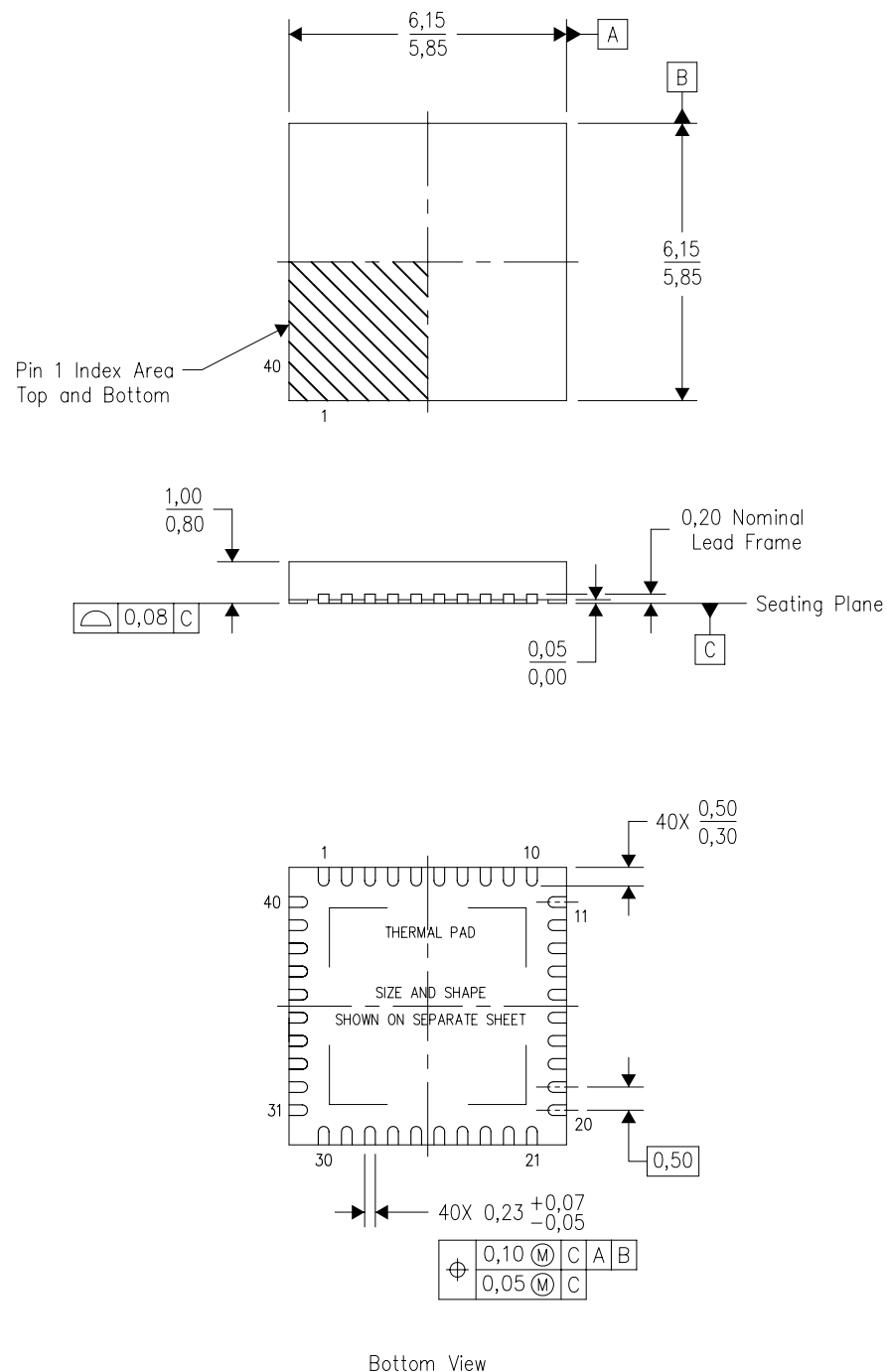


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2582RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
LMX2582RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Package complies to JEDEC MO-220 variation VJJD-2.

THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

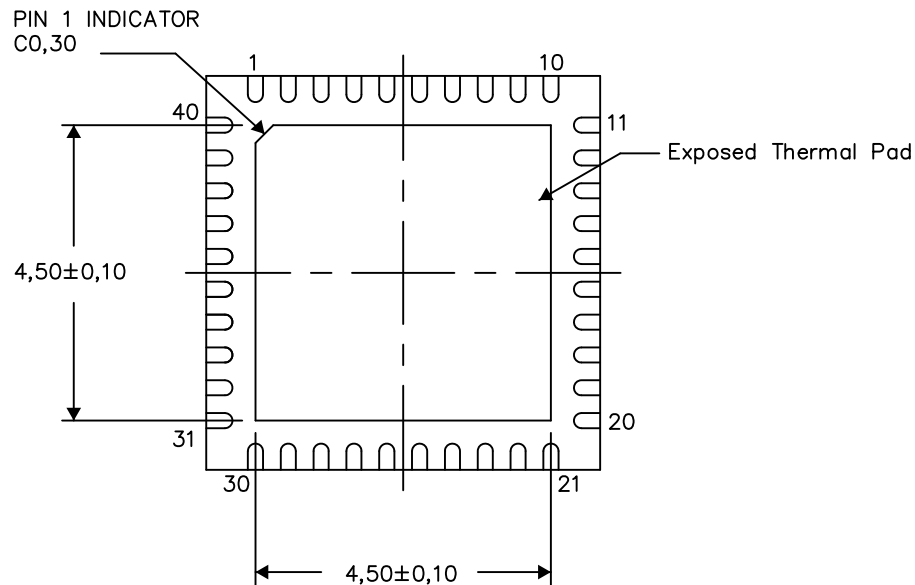
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

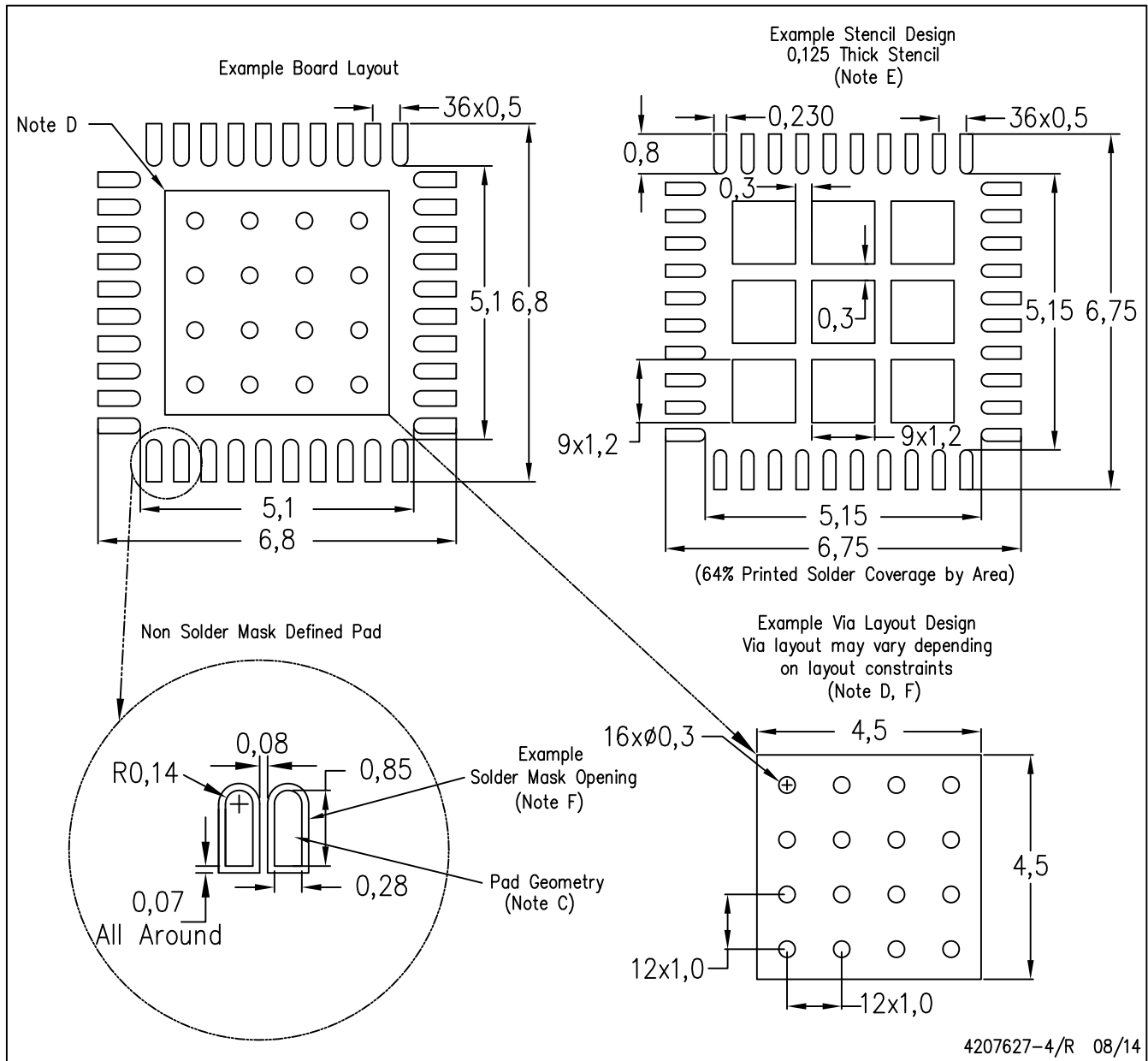
Exposed Thermal Pad Dimensions

4206355-4/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4207627-4/R 08/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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