

适用于汽车类应用的 CC2640R2F-Q1 SimpleLink™ 低功耗 Bluetooth® 无线 MCU

1 器件概述

1.1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
 - 器件温度 2 级：-40℃ 至 +105℃ 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 2
 - 器件 CDM ESD 分类等级 C3
- 微控制器
 - 强大的 ARM® Cortex®-M3
 - EEMBC CoreMark®评分：142
 - 高达 48MHz 的时钟速度
 - 275KB 非易失性存储器，包括 128KB 系统内可编程闪存
 - 高达 28KB 系统 SRAM，其中 20KB 为超低泄漏 SRAM
 - 8KB SRAM 作为缓存或系统 RAM 用途
 - 2 引脚 JTAG 和 JTAG 调试
 - 支持无线升级 (OTA)
- 超低功耗传感器控制器
 - 可独立于系统其余部分自主运行
 - 16 位架构
 - 2KB 超低泄漏电流代码和数据 SRAM
- 高效代码大小架构，ROM 中装载驱动程序、低功耗 Bluetooth® 控制器和引导加载程序，让更多闪存供应用使用
- 符合 RoHS 标准的汽车级封装
 - 具有可湿性侧面的 7mm × 7mm RGZ VQFN48 封装
- 外设
 - 31 个 GPIO，所有数字外设引脚均可连接至任何 GPIO
 - 四个通用计时器模块（八个 16 位或四个 32 位计时器，均采用 PWM）
 - 12 位模数转换器 (ADC)、200ksps、8 通道模拟多路复用器
 - 持续时间比较器
 - 超低功耗模拟比较器
 - 可编程电流源
 - UART
 - 2 个同步串行接口 (SSI) (SPI、MICROWIRE 和 TI)
 - I2C、I2S
 - 实时时钟 (RTC)
 - AES-128 安全模块
 - 真随机数发生器 (TRNG)
 - 支持八个电容感测按钮
 - 集成温度传感器
- 外部系统
 - 片上内部直流/直流转换器
 - 极少的外部组件
 - 无缝集成 SimpleLink™CC2590 和 CC2592 范围扩展器
- 低功耗
 - 宽电源电压范围：1.8 至 3.8V
 - 有源模式 RX：6.1mA
 - 有源模式 TX (0dBm)：7.0mA
 - 有源模式 TX (+5dBm)：9.3mA
 - 有源模式 MCU：61μA/MHz
 - 有源模式 MCU：48.5 CoreMark/mA
 - 有源模式传感器控制器：0.4mA + 8.2μA/MHz
 - 待机电流：1.3μA（RTC 运行，RAM/CPU 保持）
 - 关断电流：150nA（发生外部事件时唤醒）
- 射频部分
 - 与低功耗蓝牙 (BLE) 4.2 和 5 规范兼容的 2.4GHz 射频收发器
 - 出色的接收器灵敏度（对于低功耗蓝牙 1Mbps 为 -97dBm）、可选择性和阻断性能
 - 最高达 +5dBm 的可编程输出功率
 - 对于低功耗蓝牙 1Mbps，链路预算为 102dB
 - 适用于需要符合全球射频规范的系统
 - ETSI EN 300 328 和 EN 300 440（欧洲）
 - FCC CFR47 第 15 部分（美国）
 - ARIB STD-T66（日本）
- 工具和开发环境
 - 全功能开发套件
 - Sensor Controller Studio
 - SmartRF™工具产品组合
 - IAR Embedded Workbench®（用于 ARM）
 - Code Composer Studio™(CCS)
 - CCS Cloud



1.2 应用

- 汽车 应用
 - 汽车门禁
 - 无钥匙进入
 - 被动进入/被动启动 (PEPS) 系统
 - 汽车共享
 - 泊车引导
 - 无线车载诊断 (OBD)
 - 电缆更换
 - 远程控制
 - 传感器
- 工业
 - 物流
 - 生产制造自动化
 - 资产跟踪和管理
 - HMI 和远程显示
 - 访问控制

1.3 说明

SimpleLink™ 低功耗 *Bluetooth*® CC2640R2F-Q1 器件是符合 AEC-Q100 标准的无线微控制器 (MCU)，适用于低功耗蓝牙 4.2 和 5 汽车 应用，例如被动进入/被动启动 (PEPS)、遥控无钥匙进入 (RKE)、汽车共享、泊车引导、电缆更换和智能手机连接。

此器件属于 SimpleLink 超低功耗系列中的经济高效型 2.4GHz 射频器件。极低的有源射频和 MCU 电流以及低功耗模式电流消耗可确保卓越的电池寿命，因此可让连接到汽车蓄电池的节点采用小型纽扣电池供电并具有低功耗。出色的接收灵敏度和可编程输出功率，为严苛的汽车射频环境提供其所需的行业顶级射频性能。

CC2640R2F-Q1 无线 MCU 包含一个作为主应用处理器以 48MHz 速率运行的 32 位 ARM® Cortex®-M3 处理器，并包含嵌入于 ROM 中的低功耗蓝牙 4.2 控制器库和主机库。此架构可改善整体系统性能和功耗，并释放大容量闪存以供应用使用。

此外，该器件通过了 AEC-Q100 认证，达到 2 级温度范围（-40°C 至 +105°C），并采用具有可湿性侧面的 7mm × 7mm VQFN 封装。可湿性侧面有助于降低生产线成本，并通过光学检查焊点的方式提高可靠性。

可从 ti.com.cn 免费获取低功耗蓝牙软件栈。

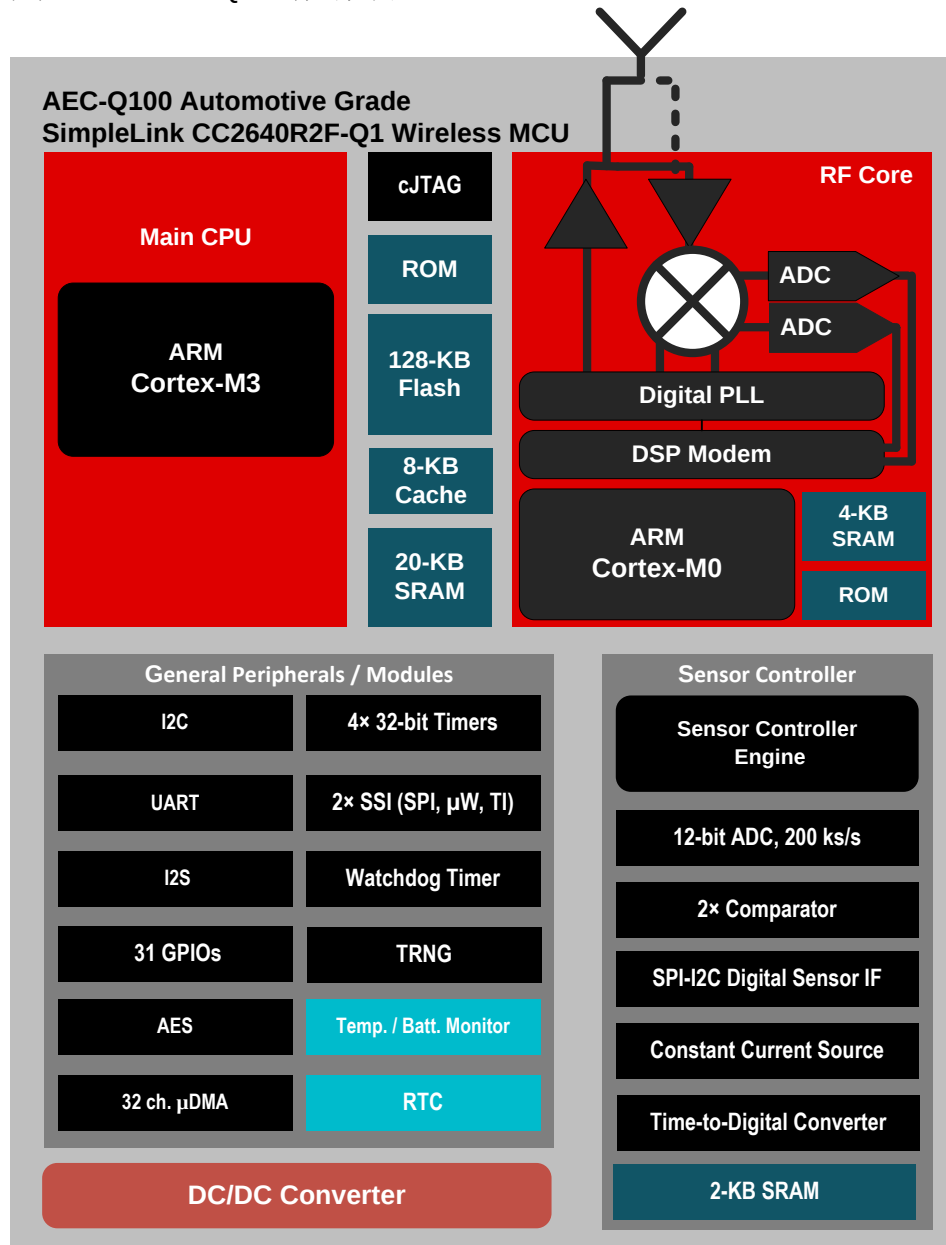
器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
CC2640R2FTWRGZQ1	具有可湿性侧面的 VQFN (48) 封装	7.00mm × 7.00mm

(1) 详细信息请参见 节 9。

1.4 功能框图

图 1-1 显示了 CC2640R2F-Q1 器件的框图。



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图 1-1. 方框图

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2 修订历史记录

Changes from January 16, 2017 to August 29, 2017	Page
• 已更改 将状态更改为生产数据	1

3 Device Comparison

Table 3-1. Device Family Overview

DEVICE	PHY SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE ⁽¹⁾
CC2640R2F-Q1 ⁽²⁾	Bluetooth low energy (Automotive)	128	20	31	RGZ (Wettable Flanks)
CC2640R2Fxxx ⁽²⁾	Bluetooth low energy (Normal, High Speed, Long Range)	128	20	31, 15, 14, 10	RGZ, RHB, YFV, RSM
CC2650F128xxx	Multi-Protocol	128	20	31, 15, 10	RGZ, RHB, RSM
CC2640F128xxx	Bluetooth low energy (Normal)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2630F128xxx	IEEE 802.15.4 (ZigBee [®] /6LoWPAN)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2620F128xxx	IEEE 802.15.4 (RF4CE)	128	20	31, 10	RGZ, RSM

- (1) Package designator replaces the xxx in device name to form a complete device name, RGZ is 7-mm × 7-mm VQFN48, RHB is 5-mm × 5-mm VQFN32, RSM is 4-mm × 4-mm VQFN32, and YFV is 2.7-mm × 2.7-mm DSBGA.
- (2) CC2640R2Fxxx devices contain Bluetooth 4.2 Host and Controller libraries in ROM, leaving more of the 128KB of flash available for the customer application when used with supported BLE-Stack software protocol stack releases. Actual use of ROM and flash by the protocol stack may vary depending on device software configuration. See [Bluetooth low energy Stack](#) for more details.

Table 3-2. Typical⁽¹⁾ Flash Memory Available for Customer Applications

Device	Simple BLE Peripheral (BT 4.0) ⁽²⁾	Simple BLE Peripheral (BT 4.2) ^{(2) (3)}
CC2640R2Fxxx, CC2640R2F-Q1 ⁽⁴⁾	83 KB	80 KB
CC2640F128xxx, CC2650F128xxx	41 KB	31 KB

- (1) Actual use of ROM and flash by the protocol stack will vary depending on device software configuration. The values in this table are provided as guidance only.
- (2) Application example with two services (GAP and Simple Profile). Compiled using IAR.
- (3) BT4.2 configuration including Secure Pairing, Privacy 1.2, and Data Length Extension
- (4) Bluetooth low energy applications running on the CC2640R2F-Q1 device make use of up to 115 KB of system ROM and up to 32 KB of RF Core ROM in order to minimize the flash usage. The maximum amount of nonvolatile memory available for Bluetooth low energy applications on the CC2640R2F-Q1 device is thus 275 KB (128-KB flash + 147-KB ROM).

3.1 Related Products

Wireless Connectivity The wireless connectivity portfolio offers a wide selection of low power RF solutions suitable for a broad range of applications. The offerings range from fully customized solutions to turn key offerings with pre-certified hardware and software (protocol).

TI's SimpleLink™ Sub-1 GHz Wireless MCUs Long-range, low-power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands.

Companion Products Review products that are frequently purchased or used in conjunction with this product.

SimpleLink™ CC2640R2 Wireless MCU LaunchPad™ Development Kit

The CC2640R2 LaunchPad™ development kit brings easy Bluetooth low energy (BLE) connection to the LaunchPad ecosystem with the SimpleLink ultra-low power CC26xx family of devices. Compared to the CC2650 LaunchPad, the CC2640R2 LaunchPad provides the following:

- More free flash memory for the user application in the CC2640R2 wireless MCU
- Out-of-the-box support for Bluetooth 4.2 specification
- 4× faster over-the-air download speed compared to Bluetooth 4.1

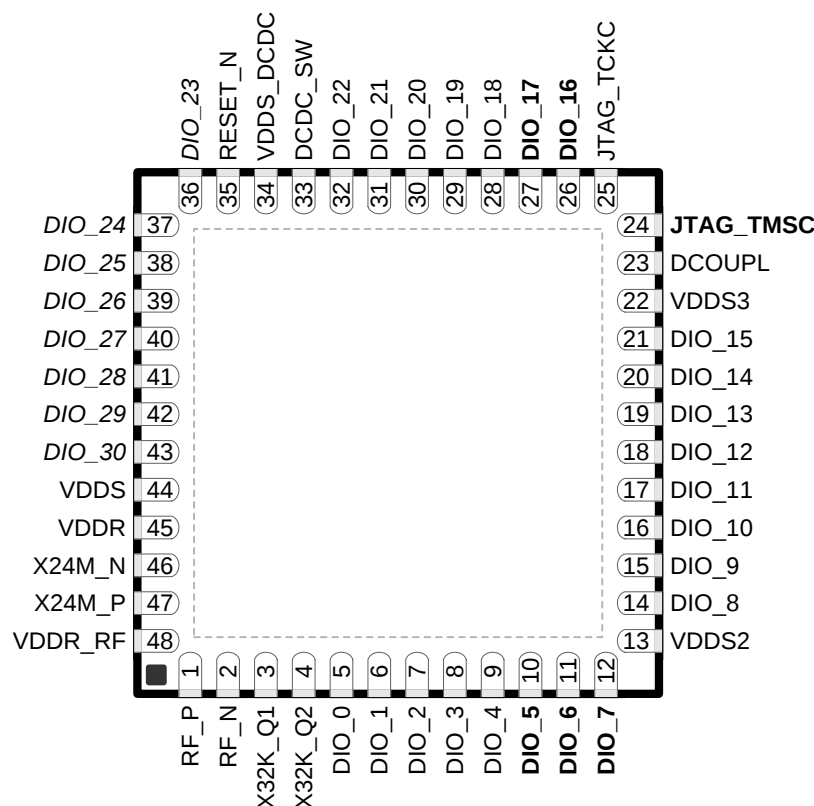
SimpleLink™ Bluetooth low energy/Multistandard SensorTag

The SensorTag IoT kit invites you to realize your cloud-connected product idea. The SensorTag includes 10 low-power MEMS sensors in a tiny red package, and it is expandable with DevPacks to make it easy to add your own sensors or actuators.

Reference Designs for CC2640 TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagram – RGZ Package



Note: The following I/O pins marked in **bold** have high-drive capabilities:

- Pin 10: **DIO_5**
- Pin 11: **DIO_6**
- Pin 12: **DIO_7**
- Pin 24: **JTAG_TMSC**
- Pin 26: **DIO_16**
- Pin 27: **DIO_17**

Note: The following I/O pins marked in *italics* have analog capabilities:

- Pin 36: *DIO_23*
- Pin 37: *DIO_24*
- Pin 38: *DIO_25*
- Pin 39: *DIO_26*
- Pin 40: *DIO_27*
- Pin 41: *DIO_28*
- Pin 42: *DIO_29*
- Pin 43: *DIO_30*

Figure 4-1. 48-Pin RGZ Package with Wettable Flanks
7-mm × 7-mm Pinout, 0.5-mm Pitch
Top View

4.2 Signal Descriptions – RGZ Package

Table 4-1. Signal Descriptions – RGZ Package

NAME	NO.	TYPE	DESCRIPTION
DCDC_SW	33	Power	Output from internal DC/DC ⁽¹⁾
DCOUP_L	23	Power	1.27-V regulated digital-supply decoupling capacitor ⁽²⁾
DIO_0	5	Digital I/O	GPIO, Sensor Controller
DIO_1	6	Digital I/O	GPIO, Sensor Controller
DIO_2	7	Digital I/O	GPIO, Sensor Controller
DIO_3	8	Digital I/O	GPIO, Sensor Controller
DIO_4	9	Digital I/O	GPIO, Sensor Controller
DIO_5	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_6	11	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_7	12	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_24	37	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_25	38	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_26	39	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_27	40	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_28	41	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_29	42	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_30	43	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMISC	24	Digital I/O	JTAG TMISC, high-drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCKC
RESET_N	35	Digital input	Reset, active-low. No internal pullup.
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
VDDR	45	Power	Connect to output of internal DC/DC ⁽²⁾⁽³⁾
VDDR_RF	48	Power	Connect to output of internal DC/DC ⁽²⁾⁽⁴⁾

(1) See the technical reference manual listed in [§ 8.3](#) for more details.

(2) Do not supply external circuitry from this pin.

(3) If internal DC/DC is not used, this pin is supplied internally from the main LDO.

(4) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

Table 4-1. Signal Descriptions – RGZ Package (continued)

NAME	NO.	TYPE	DESCRIPTION
VDDS	44	Power	1.8-V to 3.8-V main chip supply ⁽¹⁾
VDDS2	13	Power	1.8-V to 3.8-V DIO supply ⁽¹⁾
VDDS3	22	Power	1.8-V to 3.8-V DIO supply ⁽¹⁾
VDDS_DCDC	34	Power	1.8-V to 3.8-V DC/DC supply
X32K_Q1	3	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	4	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2
EGP		Power	Ground – Exposed Ground Pad

4.3 Wettable Flanks

The automotive industry requires original equipment manufacturers (OEMs) to perform 100% automated visual inspection (AVI) post-assembly to ensure that cars meet the current demands for safety and high reliability. Standard quad-flat no-lead (VQFN) packages do not have solderable or exposed pins/terminals that are easily viewed. It is therefore difficult to determine visually whether or not the package is successfully soldered onto the printed circuit board (PCB). To resolve the issue of side-lead wetting of leadless packaging for automotive and commercial component manufacturers, the wettable-flank process was developed. The wettable flanks on the VQFN package provide a visual indicator of solderability and thereby lower the inspection time and manufacturing costs.

The CC2640R2F-Q1 device is assembled using an automotive-grade VQFN package with wettable flanks.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Supply voltage, VDD _S ⁽³⁾	VDDR supplied by internal DC/DC regulator or internal GLDO. VDD _S _DCDC connected to VDD _S on PCB.	−0.3	4.1	V
Voltage on any digital pin ⁽⁴⁾		−0.3	VDD _S + 0.3, max 4.1	V
Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P		−0.3	VDDR + 0.3, max 2.25	V
Voltage on ADC input (V _{in})	Voltage scaling enabled	−0.3	VDD _S	V
	Voltage scaling disabled, internal reference	−0.3	1.49	
	Voltage scaling disabled, VDD _S as reference	−0.3	VDD _S / 2.9	
Input RF level			5	dBm
T _{stg}	Storage temperature	−40	150	°C

(1) All voltage values are with respect to ground, unless otherwise noted.

(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) VDD_{S2} and VDD_{S3} need to be at the same potential as VDD_S.

(4) Including analog-capable DIO.

5.2 ESD Ratings

			VALUE	UNIT
V _{ESD}	Electrostatic discharge	Human Body Model (HBM), per AEC Q100-002 ⁽¹⁾⁽²⁾	±2000	V
		XOCS pins 46, 47	±250	
		Charged Device Model (CDM), per AEC Q100-011 ⁽³⁾	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Ambient temperature		−40	105	°C
Operating supply voltage, VDD _S	For operation in battery-powered and 3.3-V systems (internal DC/DC can be used to minimize power consumption)	1.8	3.8	V

5.4 Power Consumption Summary

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$ with internal DC/DC converter, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{core}	Core current consumption	Reset. RESET_N pin asserted or VDDs below power-on-reset (POR) threshold	100			nA
		Shutdown. No clocks running, no retention	150			
		Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF	1.3			μA
		Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF	1.5			
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF	3.4			
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF	3.6			
		Idle. Supply Systems and RAM powered.	650			
		Active. Core running CoreMark	1.45 mA + 31 μA/MHz			
		Radio RX	6.1			mA
		Radio TX, 0-dBm output power	7.0			
		Radio TX, 5-dBm output power	9.3			
Peripheral Current Consumption (Adds to core current I _{core} for each peripheral unit activated) ⁽¹⁾						
I _{peri}	Peripheral power domain	Delta current with domain enabled	20			μA
	Serial power domain	Delta current with domain enabled	13			μA
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	237			μA
	μDMA	Delta current with clock enabled, module idle	130			μA
	Timers	Delta current with clock enabled, module idle	113			μA
	I ² C	Delta current with clock enabled, module idle	12			μA
	I2S	Delta current with clock enabled, module idle	36			μA
	SSI	Delta current with clock enabled, module idle	93			μA
	UART	Delta current with clock enabled, module idle	164			μA

(1) I_{peri} is not supported in Standby or Shutdown.

5.5 General Characteristics

$T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLASH MEMORY					
Supported flash erase cycles before failure		100			k Cycles
Maximum number of write operations per row before erase ⁽¹⁾				83	write operations
Flash retention	105°C	11.4			Years at 105°C
Flash page/sector erase current	Average delta current		12.6		mA
Flash page/sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash page/sector erase time ⁽²⁾			8		ms
Flash write time ⁽²⁾	4 bytes at a time		8		μs

(1) Each row is 2048 bits (or 256 bytes) wide.

(2) This number is dependent on Flash aging and will increase over time and erase cycles.

5.6 1-Mbps GFSK (Bluetooth low energy Technology) – RX

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2640Q1EM-7ID SMA connector, $\text{BER} = 10^{-3}$		–97		dBm
Receiver saturation	Differential mode. Measured at the CC2640Q1EM-7ID SMA connector, $\text{BER} = 10^{-3}$		4		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–350		350	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	–750		750	ppm
Co-channel rejection ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer in channel, $\text{BER} = 10^{-3}$		–6		dB
Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 1\text{ MHz}$, $\text{BER} = 10^{-3}$		7 / 2 ⁽²⁾		dB
Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 2\text{ MHz}$, Image frequency is at –2 MHz, $\text{BER} = 10^{-3}$		39 / 17 ⁽²⁾		dB
Selectivity, $\pm 3\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 3\text{ MHz}$, $\text{BER} = 10^{-3}$		38 / 30 ⁽²⁾		dB
Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 4\text{ MHz}$, $\text{BER} = 10^{-3}$		42 / 36 ⁽²⁾		dB
Selectivity, $\pm 5\text{ MHz}$ or more ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\geq \pm 5\text{ MHz}$, $\text{BER} = 10^{-3}$		32		dB
Selectivity, Image frequency ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at image frequency, $\text{BER} = 10^{-3}$		17		dB
Selectivity, Image frequency $\pm 1\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 1\text{ MHz}$ from image frequency, $\text{BER} = 10^{-3}$		2 / 30 ⁽²⁾		dB
Out-of-band blocking ⁽³⁾	30 MHz to 2000 MHz		–20		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–5		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–8		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–8		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–34		dBm
Spurious emissions, 30 MHz to 1000 MHz	Conducted measurement in a 50- Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47, Part 15 and ARIB STD-T-66		–65		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Conducted measurement in a 50- Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47, Part 15 and ARIB STD-T-66		–52		dBm
RSSI dynamic range			70		dB
RSSI accuracy			± 4		dB

(1) Numbers given as I/C dB.

(2) X / Y, where X is +N MHz and Y is –N MHz.

(3) Excluding one exception at $F_{\text{wanted}} / 2$, per Bluetooth Specification.

5.7 1-Mbps GFSK (Bluetooth low energy Technology) – TX

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Differential mode, delivered to a single-ended 50-Ω load through a balun		5		dBm
Output power, lowest setting	Delivered to a single-ended 50-Ω load through a balun		–21		dBm
Spurious emission conducted measurement ⁽¹⁾	$f < 1\text{ GHz}$, outside restricted bands		–44		dBm
	$f < 1\text{ GHz}$, restricted bands ETSI		–62		dBm
	$f < 1\text{ GHz}$, restricted bands FCC		–62		dBm
	$f > 1\text{ GHz}$, including harmonics		–55		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

5.8 24-MHz Crystal Oscillator (XOSC_HF)

$T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR Equivalent series resistance ⁽²⁾	$6\text{ pF} < C_L \leq 9\text{ pF}$		20	60	Ω
ESR Equivalent series resistance ⁽²⁾	$5\text{ pF} < C_L \leq 6\text{ pF}$			80	Ω
L_M Motional inductance ⁽²⁾	Relates to load capacitance (C_L in Farads)		$< 1.6 \times 10^{-24} / C_L^2$		H
C_L Crystal load capacitance ⁽²⁾		5		9	pF
Crystal frequency ⁽²⁾⁽³⁾			24		MHz
Crystal frequency tolerance ⁽²⁾⁽⁴⁾		–40		40	ppm
Start-up time ⁽³⁾⁽⁵⁾			150		μs

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.

(2) The crystal manufacturer's specification must satisfy this requirement

(3) Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$

(4) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance, as per Bluetooth specification.

(5) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection.

5.9 32.768-kHz Crystal Oscillator (XOSC_LF)

$T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency ⁽¹⁾			32.768		kHz
Crystal frequency tolerance, Bluetooth low-energy applications ⁽¹⁾⁽²⁾		–500		500	ppm
ESR Equivalent series resistance ⁽¹⁾			30	100	kΩ
C_L Crystal load capacitance ⁽¹⁾		6		12	pF

(1) The crystal manufacturer's specification must satisfy this requirement.

(2) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance, as per Bluetooth specification.

5.10 48-MHz RC Oscillator (RCOSC_HF)

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			48		MHz
Uncalibrated frequency accuracy			$\pm 1\%$		
Calibrated frequency accuracy ⁽¹⁾			$\pm 0.25\%$		
Start-up time			5		μs

(1) Accuracy relative to the calibration source (XOSC_HF).

5.11 32-kHz RC Oscillator (RCOSC_LF)

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency ⁽¹⁾			32.8		kHz
Temperature coefficient			50		ppm/ $^\circ\text{C}$

(1) The frequency accuracy of the real time clock (RTC) is not directly dependent on the frequency accuracy of the 32-kHz RC oscillator. The RTC can be calibrated by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating the RTC tick speed.

5.12 ADC Characteristics

$T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ without internal DC/DC converter and with voltage scaling enabled, unless otherwise noted.⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V _{DDS}	V
Resolution			12		Bits
Sample rate				200	ksps
Offset	Internal 4.3-V equivalent reference ⁽²⁾		2		LSB
Gain error	Internal 4.3-V equivalent reference ⁽²⁾		2.4		LSB
DNL ⁽³⁾ Differential nonlinearity			> -1		LSB
INL ⁽⁴⁾ Integral nonlinearity			± 3		LSB
ENOB Effective number of bits	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		9.8		Bits
	V _{DDS} as reference, 200 ksps, 9.6-kHz input tone		10		
	Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		11.1		
THD Total harmonic distortion	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		-65		dB
	V _{DDS} as reference, 200 ksps, 9.6-kHz input tone		-69		
	Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		-71		
SINAD, SNDR Signal-to-noise and Distortion ratio	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		60		dB
	V _{DDS} as reference, 200 ksps, 9.6-kHz input tone		63		
	Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		69		
SFDR Spurious-free dynamic range	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		67		dB
	V _{DDS} as reference, 200 ksps, 9.6-kHz input tone		72		
	Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		73		
Conversion time	Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles

(1) Using IEEE Std 1241™-2010 for terminology and test methods.

(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.

(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device (see [Figure 5-21](#)).

(4) For a typical example, see [Figure 5-22](#).

ADC Characteristics (continued)

$T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ without internal DC/DC converter and with voltage scaling enabled, unless otherwise noted.⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption	Internal 4.3-V equivalent reference ⁽²⁾		0.66		mA
Current consumption	VDDS as reference		0.75		mA
Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain/offset compensation factors stored in FCFG1.		4.3 ⁽²⁾⁽⁵⁾		V
Reference voltage	Fixed internal reference (input-voltage scaling disabled). For the best accuracy, the ADC conversion should be initiated through the TI-RTOS API to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows. $V_{\text{ref}} = 4.3\text{ V} \times 1408 / 4095$		1.48		V
Reference voltage	VDDS as reference (also known as <i>RELATIVE</i>) (input voltage scaling enabled)		VDDS		V
Reference voltage	VDDS as reference (also known as <i>RELATIVE</i>) (input voltage scaling disabled)		VDDS / 2.82 ⁽⁵⁾		V
Input Impedance	200 ksp/s, voltage scaling enabled. Capacitive input, input impedance depends on sampling frequency and sampling time		>1		MΩ

(5) Applied voltage must be within absolute maximum ratings at all times (see [Section 5.1](#)).

5.13 Temperature Sensor

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		–40		105	°C
Accuracy			±5		°C
Supply voltage coefficient ⁽¹⁾			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

5.14 Battery Monitor

Measured on the TI CC2640Q1EM-7ID reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V
Accuracy			13		mV

5.15 Continuous Time Comparator

$T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		VDDS	V
External reference voltage		0		VDDS	V
Internal reference voltage	DCOUPPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from –10 mV to 10 mV		0.72		μs
Current consumption when enabled ⁽¹⁾			8.6		μA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.16 Low-Power Clocked Comparator

$T_c = 25^\circ\text{C}$, $V_{DDS} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32		kHz
Internal reference voltage, $V_{DDS} / 2$			1.49–1.51		V
Internal reference voltage, $V_{DDS} / 3$			1.01–1.03		V
Internal reference voltage, $V_{DDS} / 4$			0.78–0.79		V
Internal reference voltage, $DCOUP_L / 1$			1.25–1.28		V
Internal reference voltage, $DCOUP_L / 2$			0.63–0.65		V
Internal reference voltage, $DCOUP_L / 3$			0.42–0.44		V
Internal reference voltage, $DCOUP_L / 4$			0.33–0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from –50 mV to 50 mV		<1		clock-cycle
Current consumption when enabled			362		nA

5.17 Programmable Current Source

$T_c = 25^\circ\text{C}$, $V_{DDS} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25–20		μA
Resolution			0.25		μA
Current consumption ⁽¹⁾	Including current source at maximum programmable output		23		μA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.18 Synchronous Serial Interface (SSI)

$T_c = 25^\circ\text{C}$, $V_{DDS} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$S1^{(1)} t_{clk_per}$ (SSIClk period)	Device operating as SLAVE	12		65024	system clocks
$S2^{(1)} t_{clk_high}$ (SSIClk high time)	Device operating as SLAVE		0.5		t_{clk_per}
$S3^{(1)} t_{clk_low}$ (SSIClk low time)	Device operating as SLAVE		0.5		t_{clk_per}
$S1$ (TX only) ⁽¹⁾ t_{clk_per} (SSIClk period)	One-way communication to SLAVE: Device operating as MASTER	4		65024	system clocks
$S1$ (TX and RX) ⁽¹⁾ t_{clk_per} (SSIClk period)	Normal duplex operation: Device operating as MASTER	8		65024	system clocks
$S2^{(1)} t_{clk_high}$ (SSIClk high time)	Device operating as MASTER		0.5		t_{clk_per}
$S3^{(1)} t_{clk_low}$ (SSIClk low time)	Device operating as MASTER		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams [Figure 5-1](#), [Figure 5-2](#), and [Figure 5-3](#).

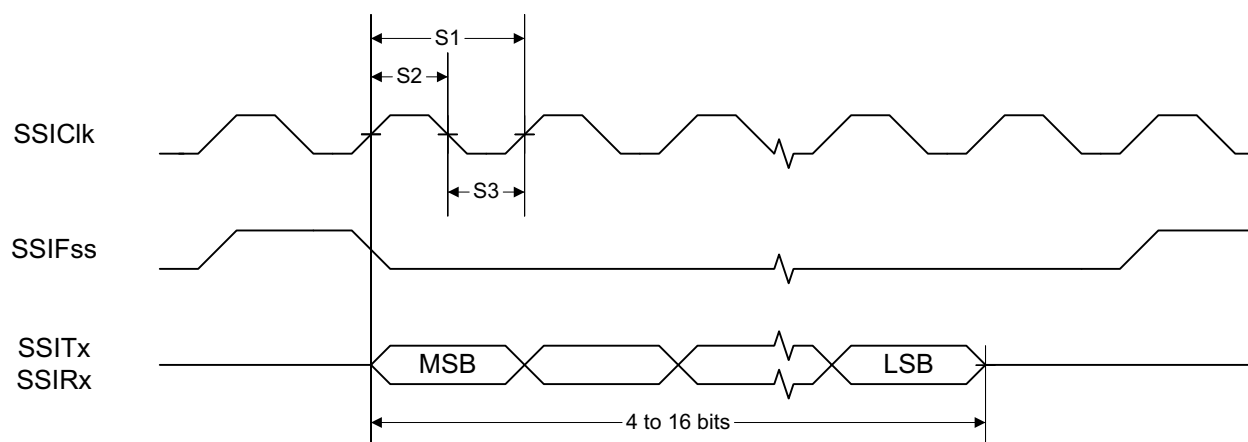


Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

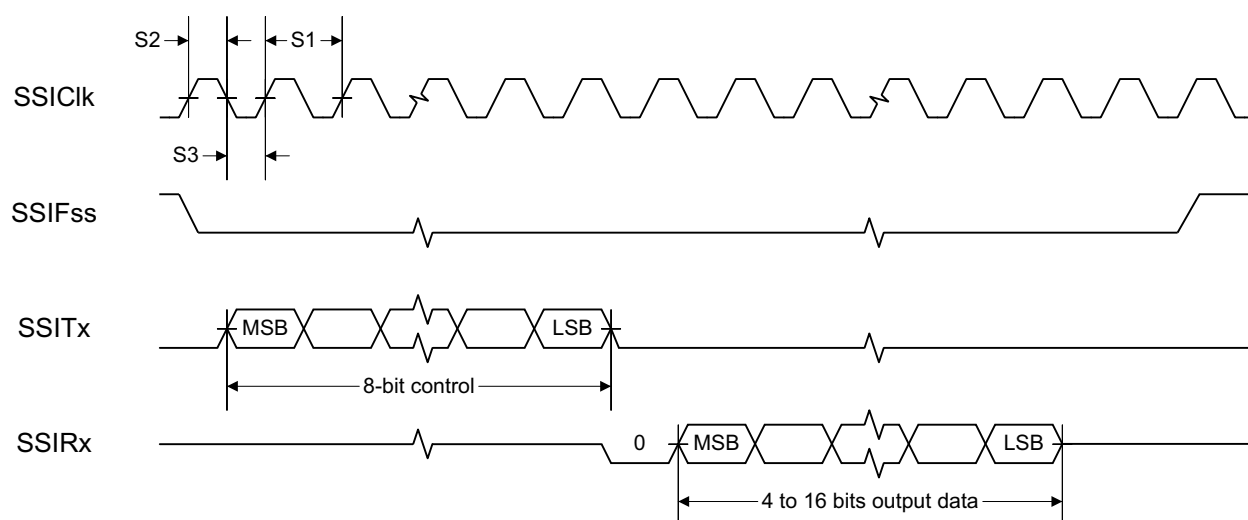


Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

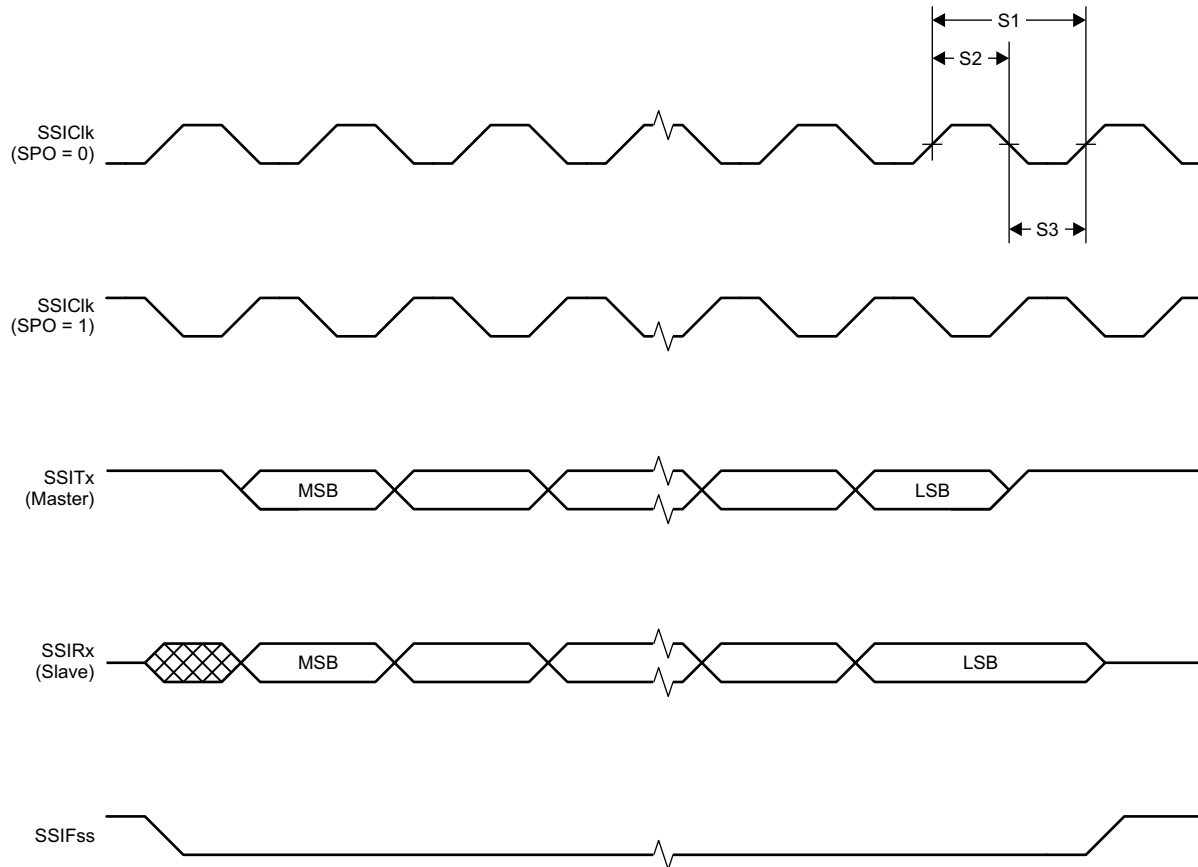


Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.19 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DD}S = 1.8 V					
GPIO V _{OH} at 8-mA load	IOCURR = 2, high-drive GPIOs only	1.32	1.54		V
GPIO V _{OL} at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.26	0.32	V
GPIO V _{OH} at 4-mA load	IOCURR = 1	1.32	1.58		V
GPIO V _{OL} at 4-mA load	IOCURR = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, V _(pad) = 0 V		71.7		μA
GPIO pulldown current	Input mode, pulldown enabled, V _(pad) = V _{DD} S		21.1		μA
GPIO high/low input transition, no hysteresis	I _H = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	I _H = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	I _H = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	I _H = 1, difference between 0 → 1 and 1 → 0 points		0.33		V

DC Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DD5} = 3.0 V					
GPIO V _{OH} at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.68		V
GPIO V _{OL} at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.33		V
GPIO V _{OH} at 4-mA load	IOCURR = 1		2.72		V
GPIO V _{OL} at 4-mA load	IOCURR = 1		0.28		V
T_A = 25°C, V_{DD5} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, V _(pad) = 0 V		277		μA
GPIO pulldown current	Input mode, pulldown enabled, V _(pad) = V _{DD5}		113		μA
GPIO high/low input transition, no hysteresis	I _H = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	I _H = 1, transition voltage for input read as 0 → 1		1.94		V
GPIO high-to-low input transition, with hysteresis	I _H = 1, transition voltage for input read as 1 → 0		1.54		V
GPIO input hysteresis	I _H = 1, difference between 0 → 1 and 1 → 0 points		0.4		V
T_A = 25°C					
V _(IH)	Lowest GPIO input voltage reliably interpreted as a «High»			0.8	V _{DD5} ⁽¹⁾
V _(IL)	Highest GPIO input voltage reliably interpreted as a «Low»	0.2			V _{DD5} ⁽¹⁾

(1) Each GPIO is referenced to a specific V_{DD5} pin. See the technical reference manual listed in [§ 8.3](#) for more details.

5.20 Thermal Resistance Characteristics for RGZ Package

over operating free-air temperature range (unless otherwise noted)

NAME	DESCRIPTION	(°C/W) ^{(1) (2)}
R _{θJA}	Junction-to-ambient thermal resistance	29.6
R _{θJC(top)}	Junction-to-case (top) thermal resistance	15.7
R _{θJB}	Junction-to-board thermal resistance	6.2
Ψ _{sjT}	Junction-to-top characterization parameter	0.3
Ψ _{sjB}	Junction-to-board characterization parameter	6.2
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	1.9

(1) °C/W = degrees Celsius per watt.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see the following EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

5.21 Timing Requirements

		MIN	NOM	MAX	UNIT
Rising supply-voltage slew rate		0		100	mV/μs
Falling supply-voltage slew rate		0		20	mV/μs
Falling supply-voltage slew rate, with low-power flash settings ⁽¹⁾				3	mV/μs
Positive temperature gradient in standby ⁽²⁾	No limitation for negative temperature gradient, or outside standby mode			5	°C/s
CONTROL INPUT AC CHARACTERISTICS ⁽³⁾					
RESET_N low duration		1			μs

- (1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-μF VDD5 input capacitor (see [Figure 7-1](#)) must be used to ensure compliance with this slew rate.
- (2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see [Section 5.11](#)).
- (3) T_A = –40°C to +105°C, V_{DD5} = 1.8 V to 3.8 V, unless otherwise noted.

5.22 Switching Characteristics

Measured on the TI CC2640Q1EM-7ID reference design with T_c = 25°C, V_{DD5} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKEUP and TIMING					
Idle → Active			14		μs
Standby → Active			151		μs
Shutdown → Active			1015		μs

5.23 Typical Characteristics

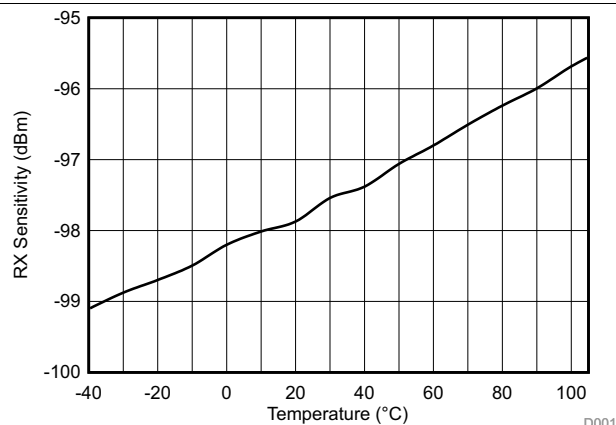


Figure 5-4. Bluetooth low energy Sensitivity vs Temperature

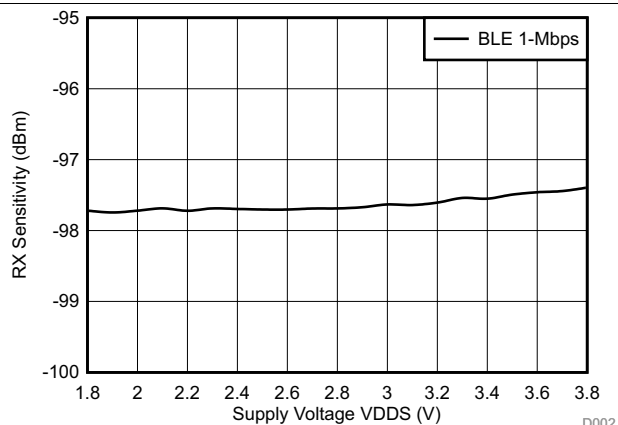


Figure 5-5. Bluetooth low energy Sensitivity vs Supply Voltage (VDD5)

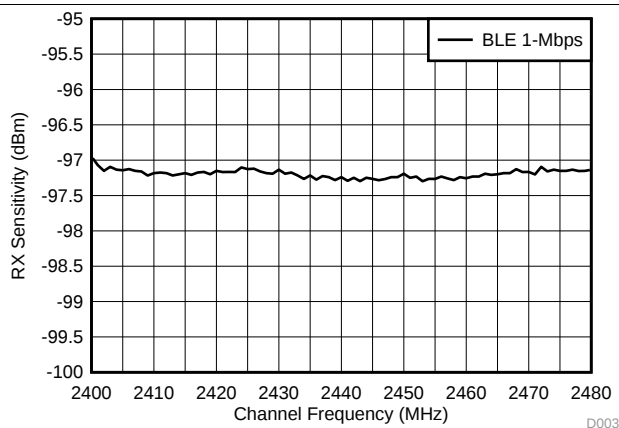


Figure 5-6. Bluetooth low energy Sensitivity vs Channel Frequency

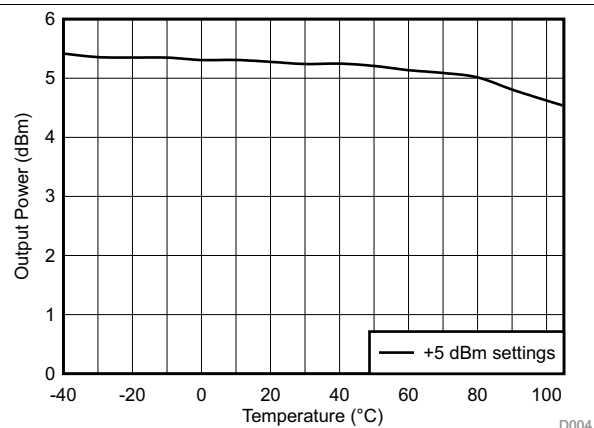


Figure 5-7. TX Output Power vs Temperature

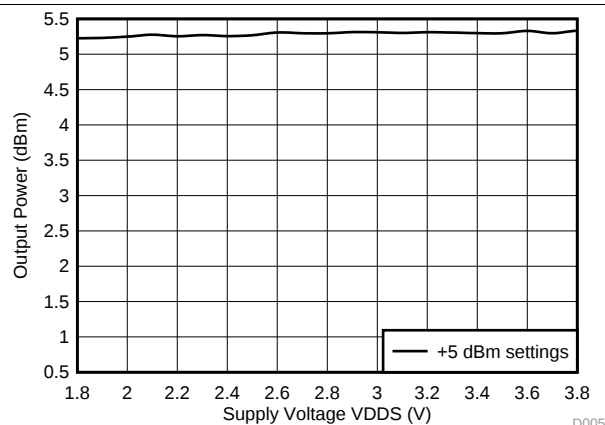


Figure 5-8. TX Output Power vs Supply Voltage (VDD5)

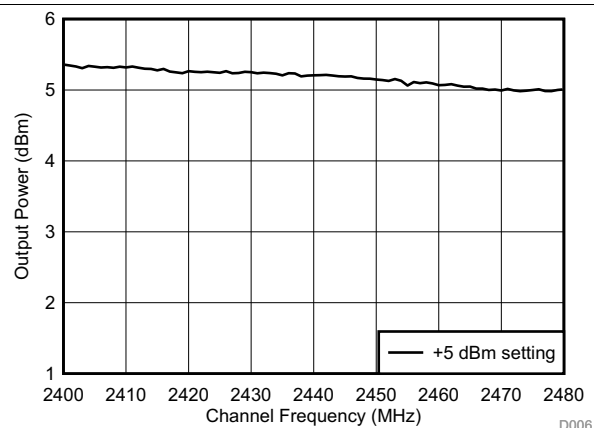


Figure 5-9. TX Output Power vs Channel Frequency

Typical Characteristics (continued)

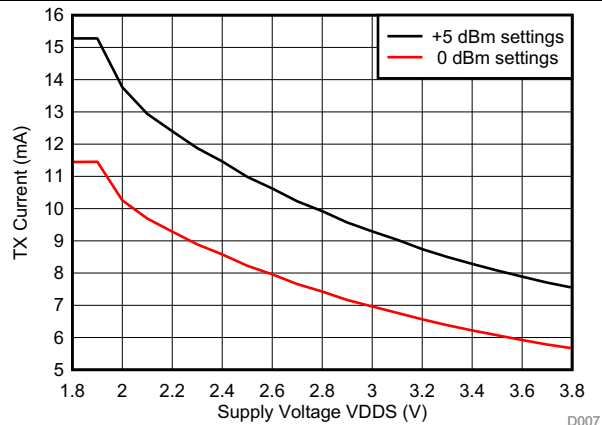


Figure 5-10. TX Current Consumption vs Supply Voltage (VDD5)

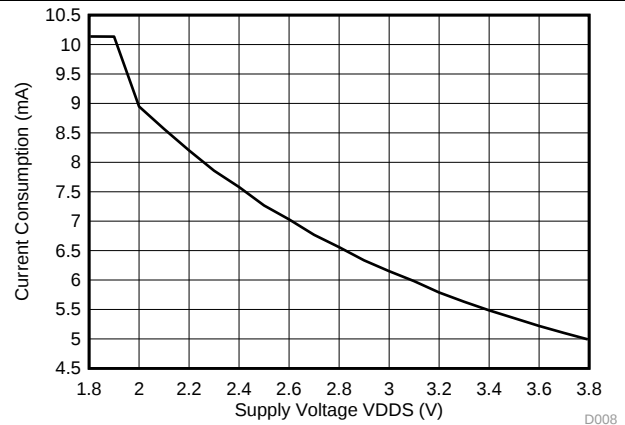


Figure 5-11. RX Mode Current vs Supply Voltage (VDD5)

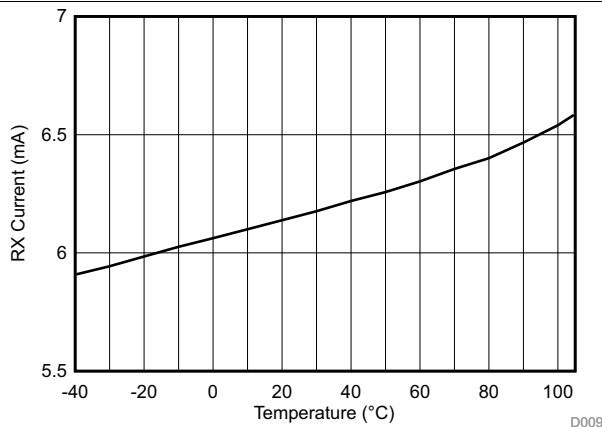


Figure 5-12. RX Mode Current Consumption vs Temperature

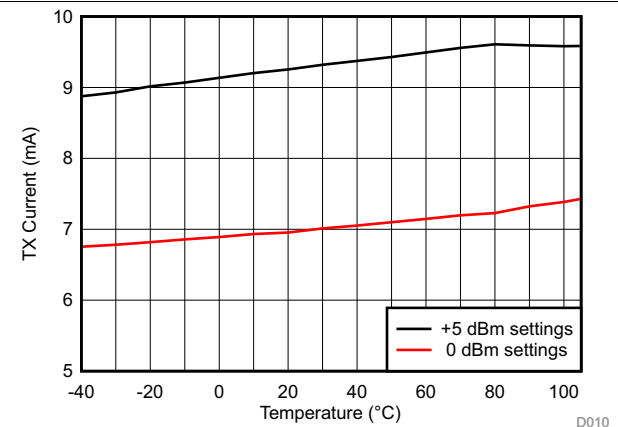


Figure 5-13. TX Mode Current Consumption vs Temperature

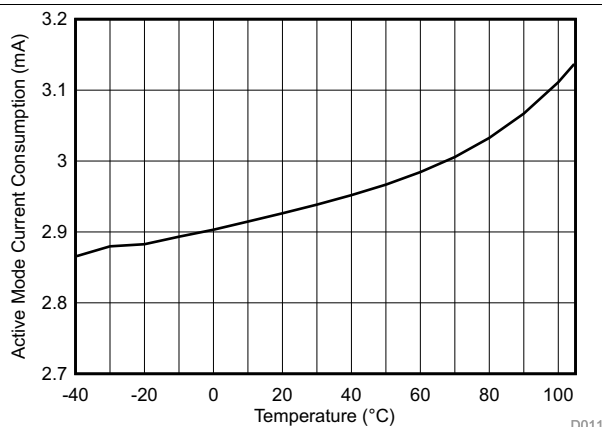


Figure 5-14. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature

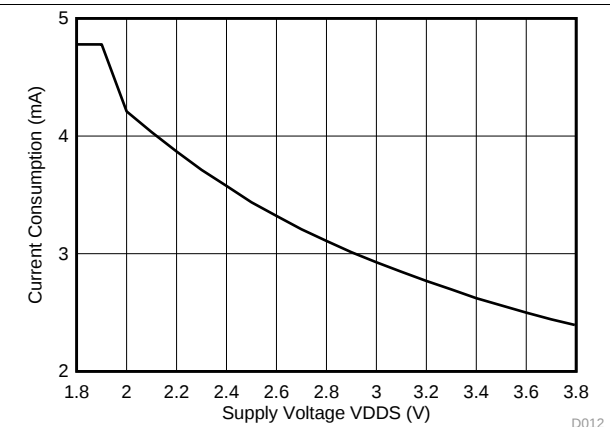


Figure 5-15. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDD5)

Typical Characteristics (continued)

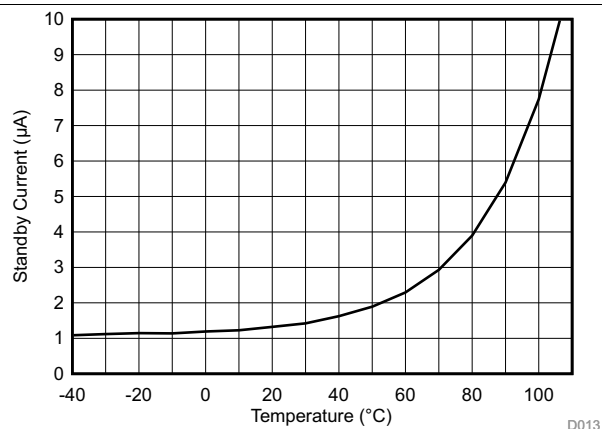


Figure 5-16. Standby Mode Current Consumption vs Temperature

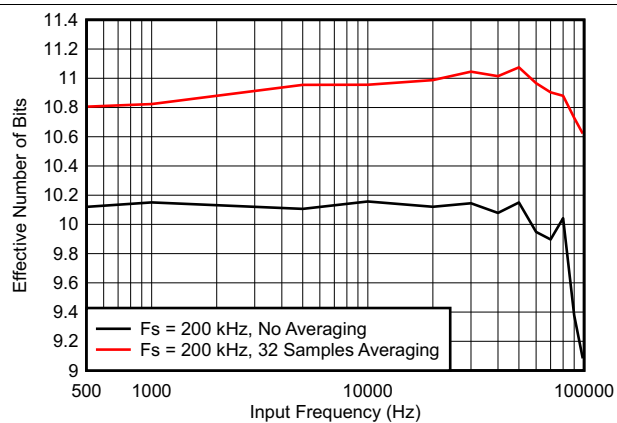


Figure 5-17. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference, No Scaling)

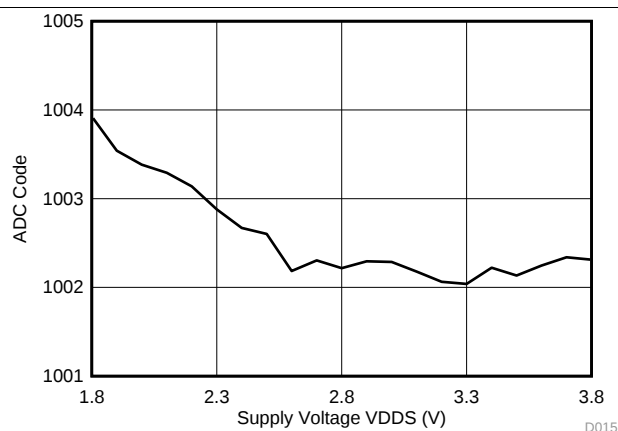


Figure 5-18. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

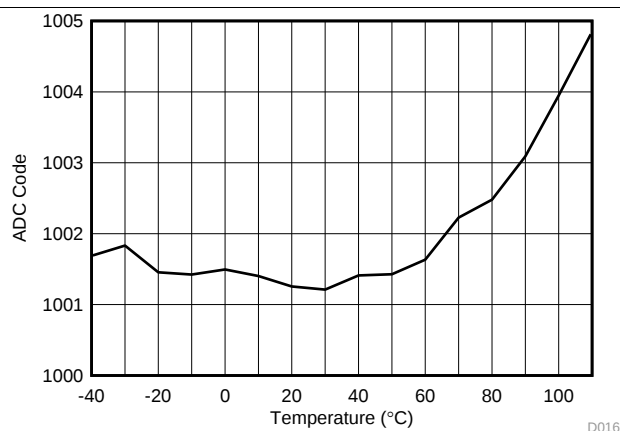


Figure 5-19. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)

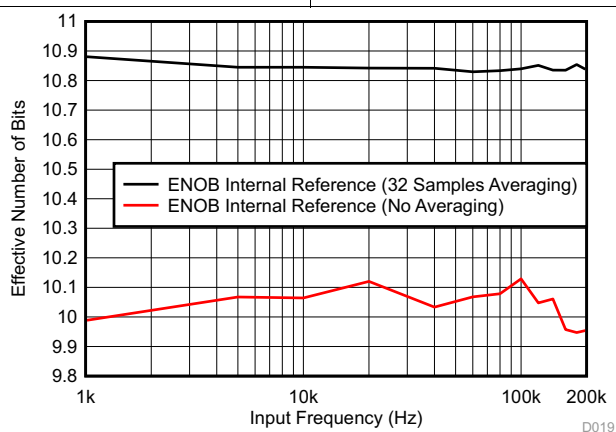


Figure 5-20. SoC ADC ENOB vs Sampling Frequency (Input Frequency = FS / 10)

Typical Characteristics *(continued)*

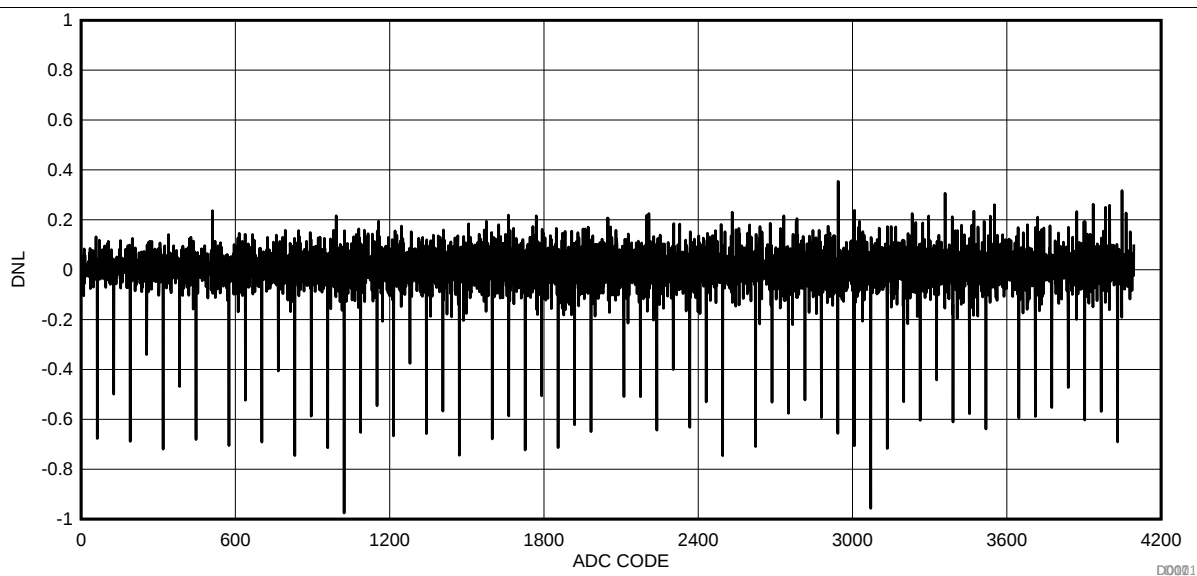


Figure 5-21. SoC ADC DNL vs ADC Code (Internal Reference, No Scaling)

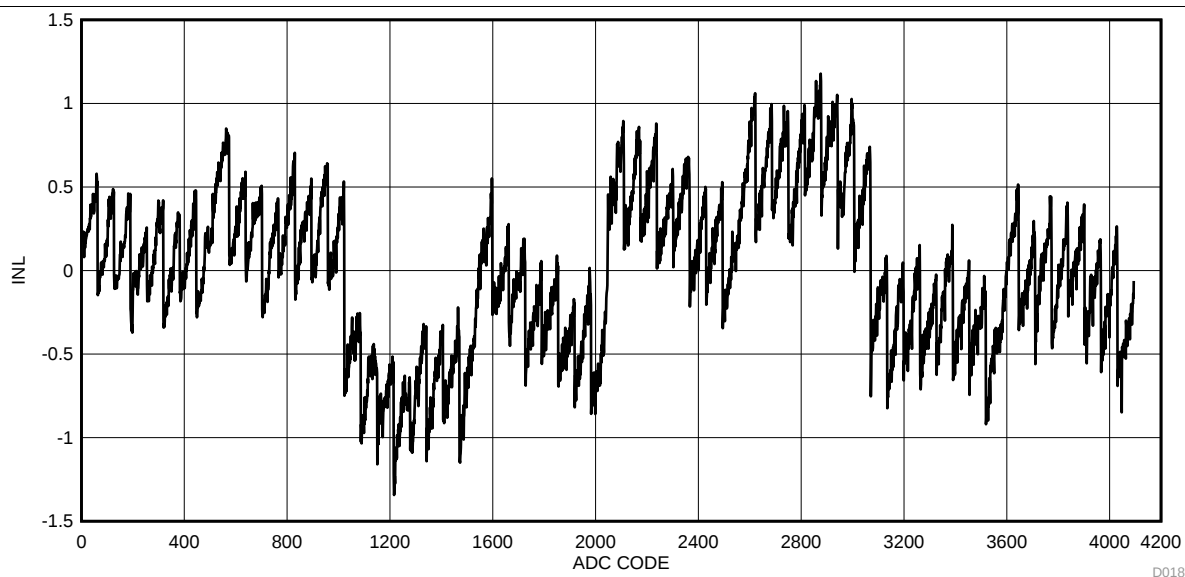


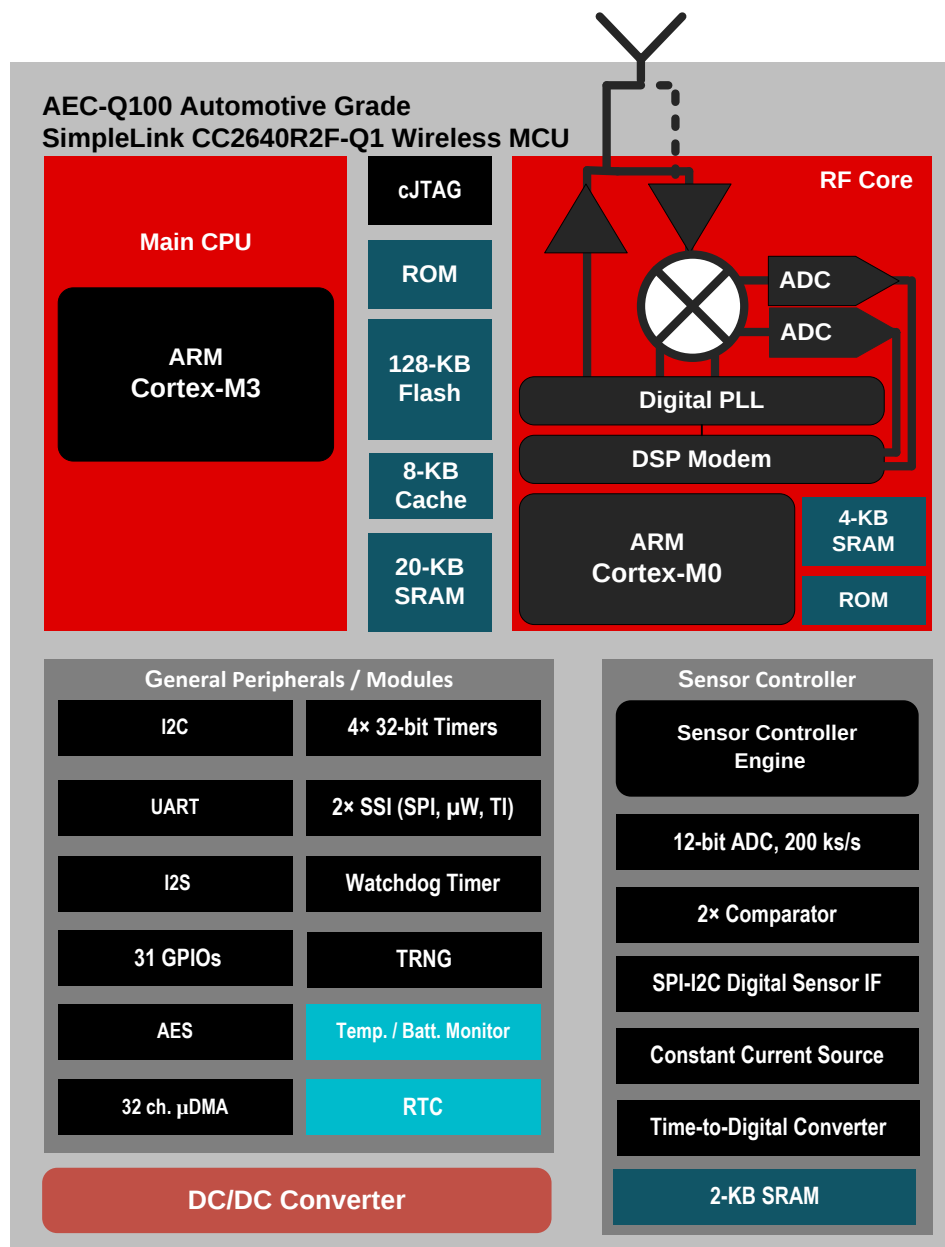
Figure 5-22. SoC ADC INL vs ADC Code (Internal Reference, No Scaling)

6 Detailed Description

6.1 Overview

Section 6.2 shows the core modules of the CC26xx product family.

6.2 Functional Block Diagram



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6.3 Main CPU

The automotive grade SimpleLink CC2640R2F-Q1 Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The Cortex-M3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Cortex-M3 features include the following:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb[®]-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
 - Single-cycle multiply instruction and hardware divide
 - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
 - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7[™] processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.4 RF Core

The RF Core contains an ARM Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (Bluetooth low energy) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The ARM Cortex-M0 processor is not programmable by customers.

6.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main Cortex-M3 CPU.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and potential use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs, bit-banged I²C, and SPI
- UART communication for sensor reading or debugging
- Capacitive sensing
- Waveform generation
- Pulse counting
- Keyboard scan
- Quadrature decoder for polling rotation sensors
- Oscillator calibration

NOTE

Texas Instruments provides application examples for some of these use cases, but not for all of them.

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI–I²C digital interface.
- The analog modules can be connected to up to eight different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1. GPIOs Connected to the Sensor Controller⁽¹⁾

ANALOG CAPABLE	7 × 7 RGZ DIO NUMBER
Y	30
Y	29
Y	28
Y	27
Y	26
Y	25
Y	24
Y	23
N	7
N	6
N	5
N	4
N	3
N	2
N	1
N	0

(1) Up to 16 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules.

6.6 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI-RTOS kernel, Driver Library, and lower layer protocol stack software (Bluetooth low energy Controller). It also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.7 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.8 Power Management

To minimize power consumption, the CC2640R2F-Q1 device supports a number of power modes and power management features (see [Table 6-2](#)).

Table 6-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.45 mA + 31 µA/MHz	650 µA	1.3 µA	0.15 µA	0.1 µA
Wake-up Time to CPU Active ⁽¹⁾	–	14 µs	151 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake up on RTC	Available	Available	Available	Off	Off
Wake up on Pin Edge	Available	Available	Available	Available	Off
Wake up on Reset Pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead

In active mode, the application Cortex-M3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [Table 6-2](#)).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake event, RTC event, or sensor-controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain and the Sensor Controller. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from Shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU, which means that the main CPU does not have to wake up, for example, to execute an ADC sample or poll a digital sensor over SPI. The main CPU saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the sensor controller and choose which peripherals are controlled and which conditions wake up the main CPU.

6.9 Clock Systems

The CC2640R2F-Q1 device supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. Bluetooth low energy requires a slow-speed clock with better than ± 500 ppm accuracy if the device is to enter any sleep mode while maintaining a connection. The internal 32-kHz RC oscillator can in some use cases be compensated to meet the requirements. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.10 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in [Section 4](#)).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and synchronous serial interfaces from Texas Instruments™. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps and is compatible with the Bluetooth HCI specifications.

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I²C interface is used to communicate with devices compatible with the I²C standard. The I²C interface is capable of 100-kHz and 400-kHz operation, and can serve as both I²C master and I²C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (μ DMA) controller. The μ DMA controller provides a way to offload data transfer tasks from the Cortex-M3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The μ DMA controller can perform transfer between memory and peripherals. The μ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the μ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory
 - Peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except in Shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

6.11 System Architecture

Depending on the product configuration, the CC2640R2F-Q1 device can function either as a wireless network processor (WNP—a device running the wireless protocol stack with the application running on a separate MCU), or as a system-on-chip (SoC), with the application and protocol stack running on the ARM Cortex-M3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

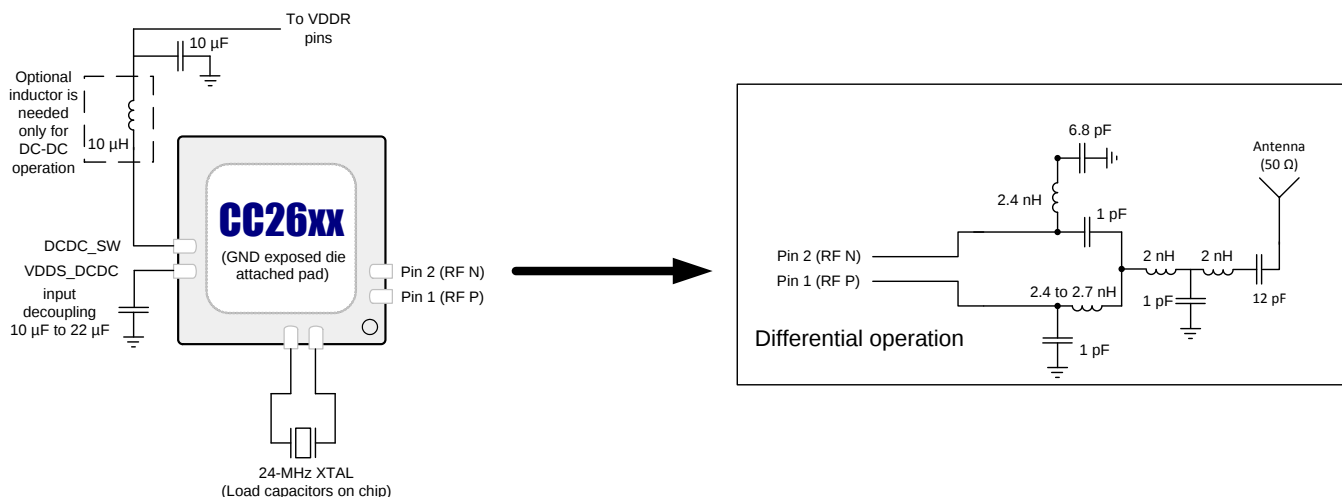
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Very few external components are required for the operation of the CC2640R2F-Q1 device. This section provides general information about the differential configuration when using the CC2640R2F-Q1 device in an application, and an example application circuit with schematics and layout is shown in Figure 7-1, Figure 7-2, Figure 7-3, and Figure 7-4. This is only a small selection of the many application circuit examples available as complete reference designs from the product folder on www.ti.com.

Figure 7-1 shows the differential RF front-end configuration option with internal biasing. See the CC2640Q1EM-7ID reference design for this option.



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Figure 7-1. CC2640R2F-Q1 Application Circuit

Figure 7-2 shows the various supply voltage configuration options for the CC2640R2F-Q1 device. Not all power supply decoupling capacitors or digital I/Os are shown. For a detailed overview of power supply decoupling and wiring, see the TI reference designs and the [CC13x0, CC26x0 SimpleLink Wireless MCU Technical Reference Manual](#).

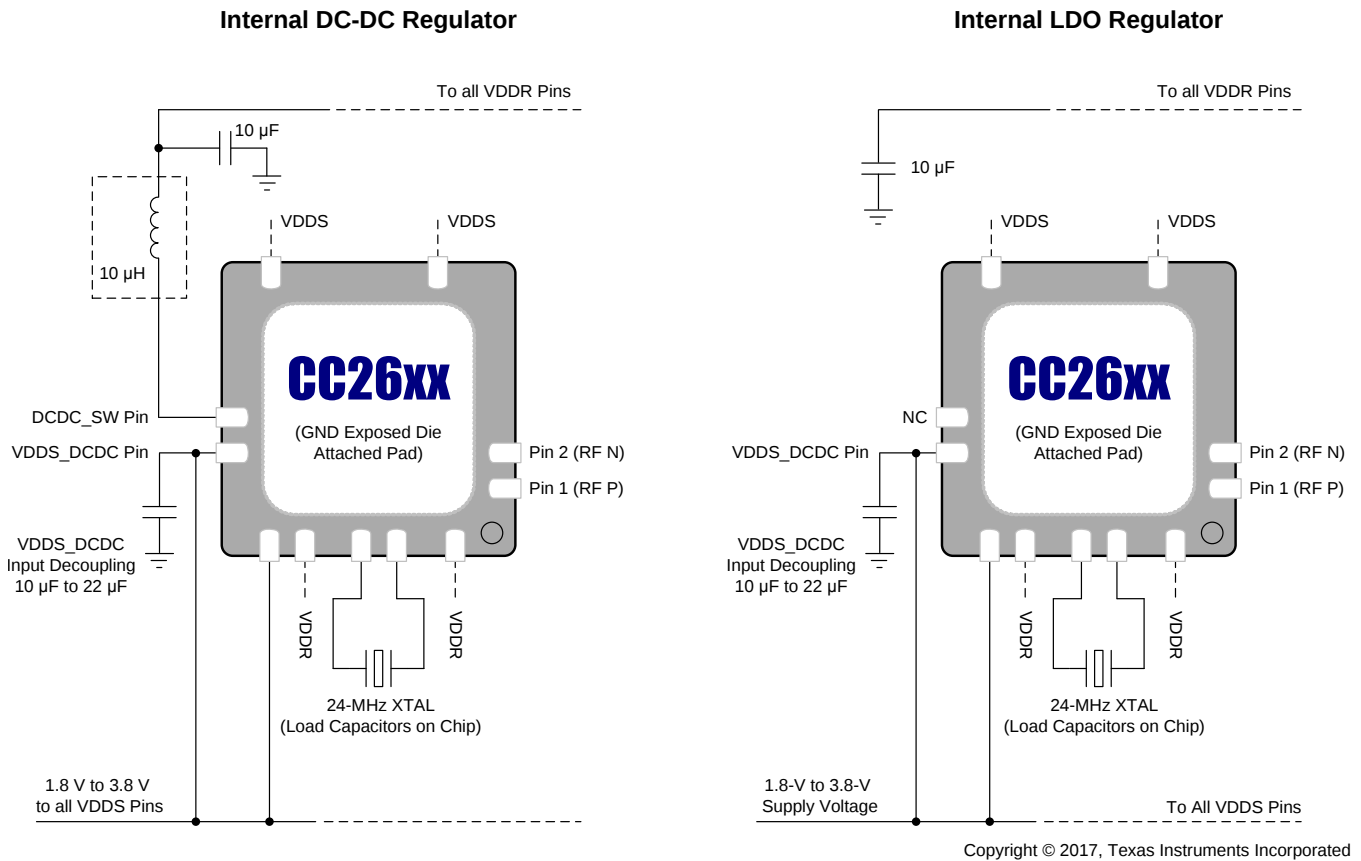


Figure 7-2. Supply Voltage Configurations

7.2 7 × 7 Internal Differential (7ID) Application Circuit

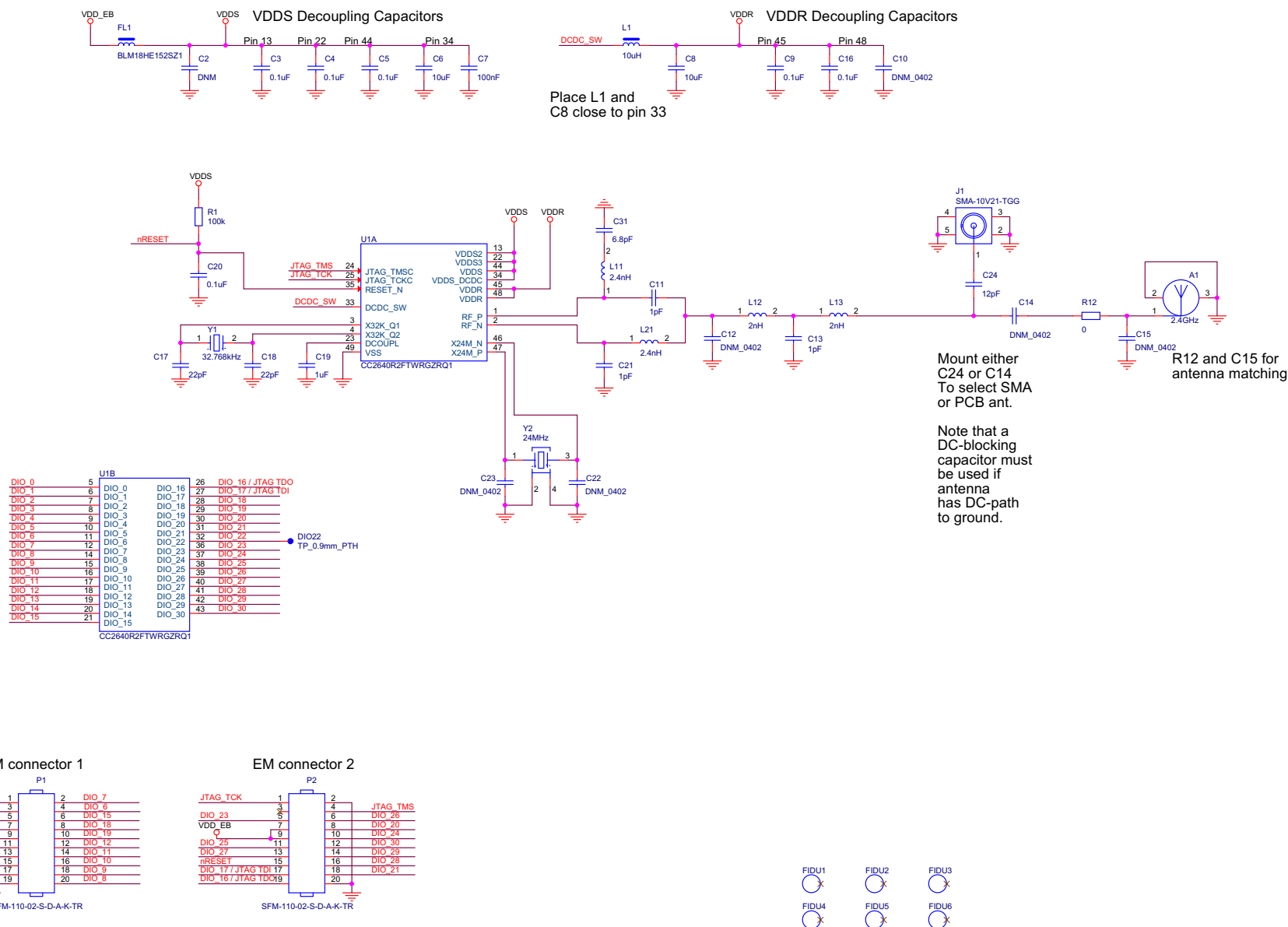


Figure 7-3. 7 × 7 Internal Differential (7ID) Application Circuit

7.2.1 Layout

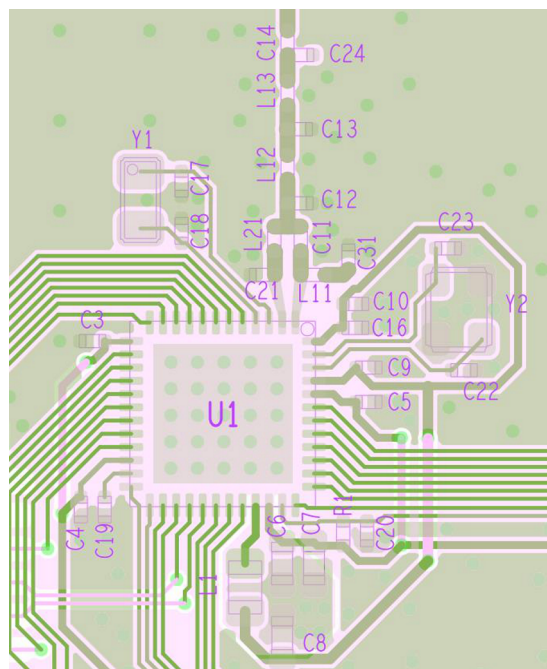


Figure 7-4. Layout

8 器件和文档支持

8.1 器件命名规则

为了标明产品开发周期的各个产品阶段，TI 为所有部件号和日期代码添加了前缀。每个器件都具有以下三个前缀/标识中的一个：X、P 或无（无前缀）（例如 **CC2640R2F-Q1** 正在批量生产，因此未分配前缀/标识）。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如 **RSM**）。

如需 **CC2640R2F-Q1** 器件封装类型的可订购器件号，请参阅本文档的封装选项附录、访问 TI 网站 (www.ti.com.cn) 或联系您的 TI 销售代表。

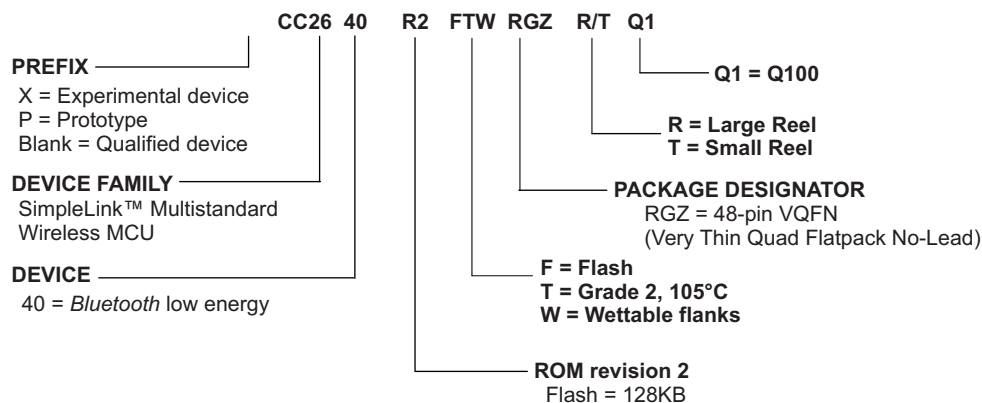


图 8-1. 器件命名规则

8.2 工具和软件

德州仪器 (TI) 提供大量的开发工具，其中包括评估处理器性能、生成代码、开发算法工具、以及完全集成和调试软件及硬件模块的工具。

以下产品为 CC2640R2F-Q1 器件 应用的开发提供支持：

软件工具：

SmartRF Studio 7:

SmartRF Studio 是一款 PC 应用程序，可帮助无线电系统设计人员评估早期设计过程的 RF-IC。

- 测试无线数据包收发功能，连续波收发功能
- 将相关数据写入支持的评估板或调试器，评估定制板上的 RF 性能
- 可以不搭配任何硬件使用，但此时只能生成、编辑并导出无线配置设置
- 可与德州仪器 (TI) CCxxxx 系列 RF-IC 的多款开发套件搭配使用

Sensor Controller Studio:

Sensor Controller Studio 为 CC26xx 传感器控制器提供开发环境。此传感器控制器是 CC26xx 系列中的一款专用功率优化型 CPU，可独立于系统 CPU 状态自主执行简单的后台任务。

- 允许使用 C 语言这类编程语言实现传感器控制器任务算法
- 输出传感器控制器接口驱动程序，其中整合了生成的传感器控制器机械代码和相关定义
- 通过使用集成传感器控制器任务测试和调试功能实现快速开发这有助于实现有效的传感器数据和算法验证可视化。

IDE 和编译器:

Code Composer Studio:

- 带有项目管理工具和编辑器的集成开发环境
- Code Composer Studio (CCS) 6.1 及更高版本内置对 CC26xx 系列器件的支持功能。
- 优先支持的 XDS 调试器：XDS100v3、XDS110 和 XDS200
- 与 TI-RTOS 高度集成，支持 TI-RTOS 对象视图

IAR ARM Embedded Workbench

- 带有项目管理工具和编辑器的集成开发环境
- IAR EWARM 7.30.3 及更高版本内置对 CC26xx 系列器件的支持功能。
- 广泛的调试器支持，支持 XDS100v3、XDS200、IAR I-Jet 和 Segger J-Link
- 带有项目管理工具和编辑器的集成开发环境
- 适用于 TI-RTOS 的 RTOS 插件

有关 CC2640R2F-Q1 平台开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com.cn。有关定价和购买信息，请联系最近的 TI 销售办事处或授权分销商。

8.3 文档支持

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹 ([CC2640R2F-Q1](#))。单击右上角的“通知我”进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

下面列出了介绍 CC2640R2F-Q1 器件、相关外设以及其他技术材料的最新文档。

技术参考手册

[《CC13xx、CC26xx SimpleLink™ 无线 MCU 技术参考手册》](#)

勘误

[《CC2640R2F-Q1 SimpleLink™ 无线 MCU 勘误表》](#)

8.4 德州仪器 (TI) 低功耗射频网站

德州仪器 (TI) 的低功耗射频网站提供所有最新产品、应用和设计笔记、FAQ 部分、新闻资讯以及活动更新。请访问 www.ti.com.cn/lprf。

8.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 为了促进工程师之间的合作，我们创建了 TI 工程师对工程师 (E2E) 社区。在 e2e.ti.com 中，您可以提问、分享知识、拓展思路并与同行工程师一道帮助解决问题。

TI 嵌入式处理器维基网页 德州仪器 (TI) 嵌入式处理器维基网站。此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

低功耗射频在线社区 TI E2E 支持社区的无线连接

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- 射频设计帮助
- E2E 交流互动

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低功耗射频开发者网络 德州仪器 (TI) 建立了一个大型低功耗射频开发合作伙伴网络，帮助客户加快应用开发。此网络中包括推荐的公司、射频顾问和独立设计工作室，他们可提供一系列硬件模块产品和设计服务，其中包括：

- 射频电路、低功耗射频和 ZigBee 设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

如果需要有关模块、工程服务或开发工具的帮助：

请搜索**低功耗射频开发者网络**查找适合的合作伙伴。www.ti.com.cn/lprfnetwork

8.6 其他信息

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此外, 德州仪器 (TI) 还提供广泛的相关支持, 例如开发工具、技术文档、参考设计、应用专业技术、客户支持、第三方服务以及大学计划。

[低功耗射频 E2E 在线社区](#) 设有技术支持论坛并提供视频和博客, 您有机会在此与全球同领域工程师交流互动。

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8.8 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.9 出口管制提示

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8.10 术语表

TI 术语表 这份术语表列出并解释术语、缩写和定义。

9 机械、封装和可订购信息

9.1 封装信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更, 恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本, 请参阅左侧的导航。

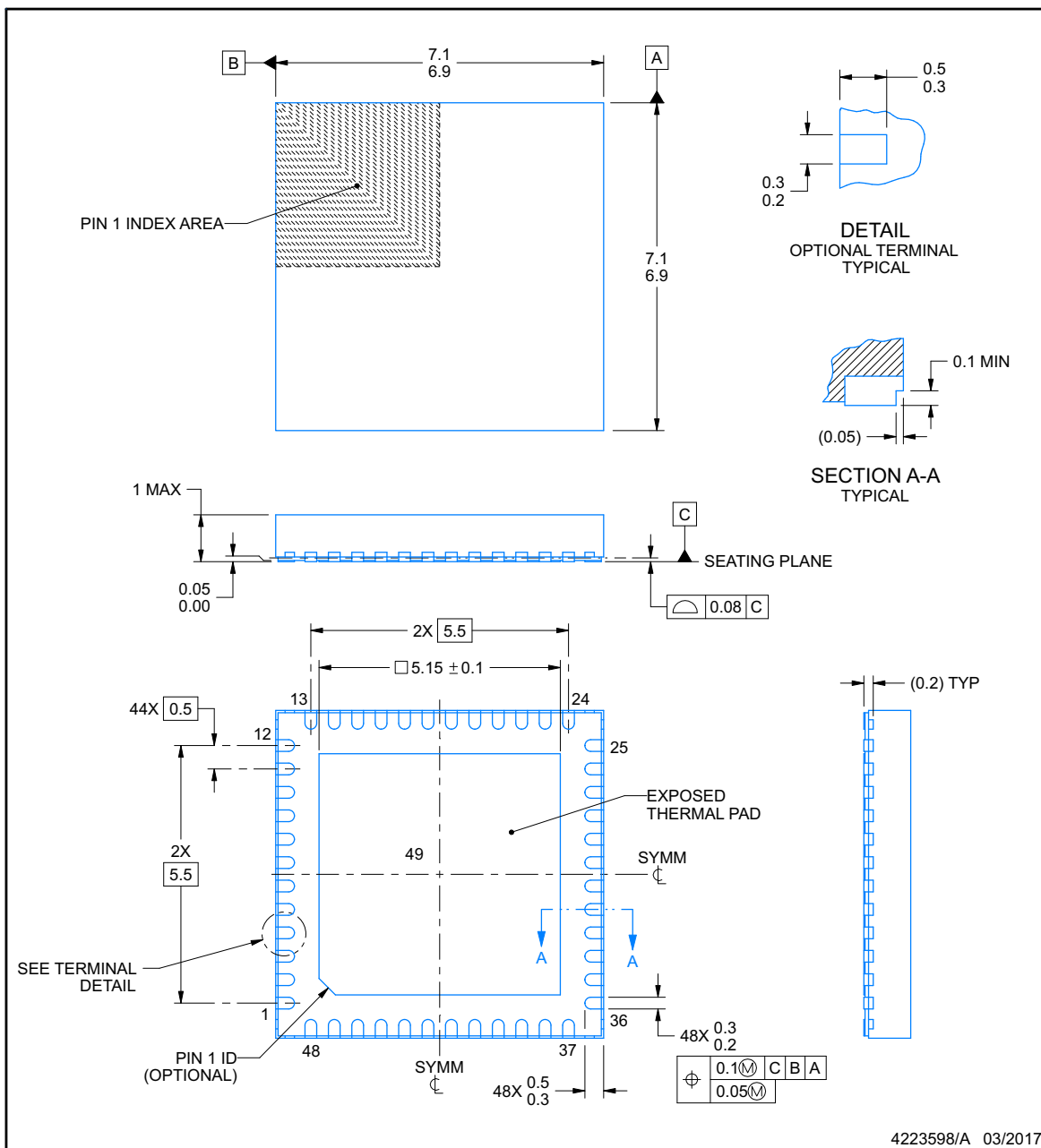


RGZ0048N

PACKAGE OUTLINE

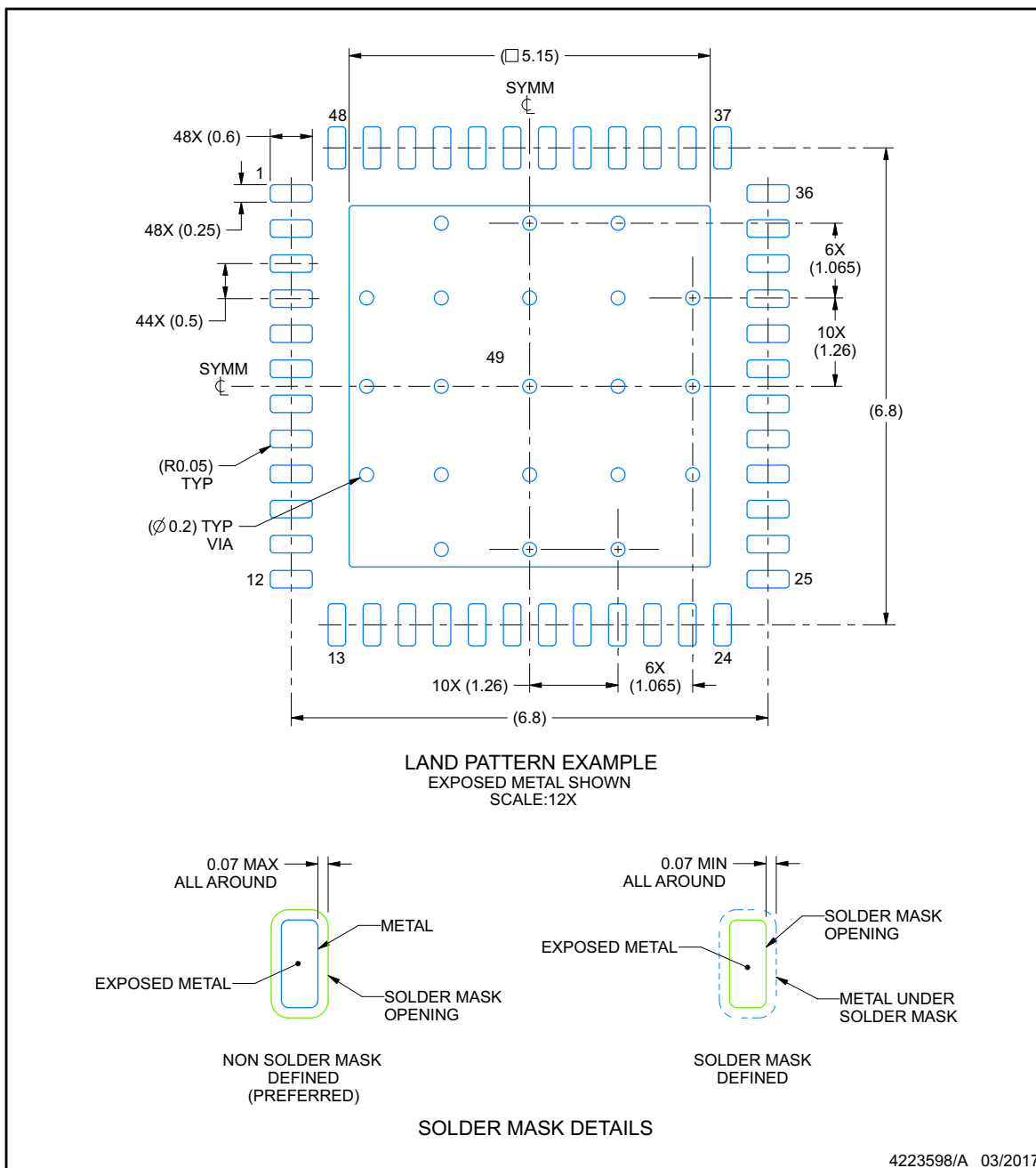
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



EXAMPLE BOARD LAYOUT**RGZ0048N****VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

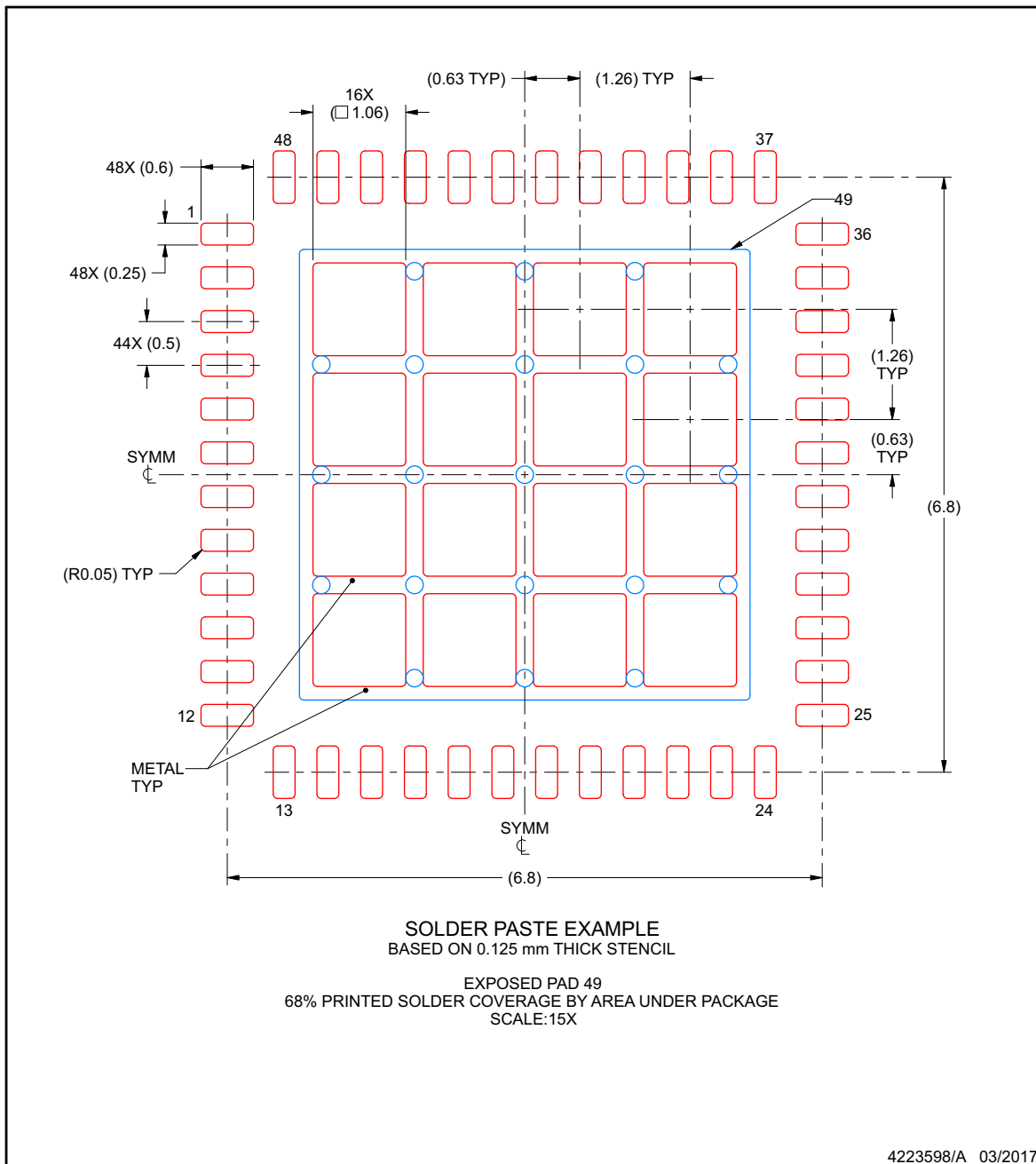
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2640R2FTWRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	CC2640Q1 R2F	Samples
CC2640R2FTWRGZTQ1	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	CC2640Q1 R2F	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2640R2FTWRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC2640R2FTWRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2640R2FTWRGZRQ1	VQFN	RGZ	48	2500	336.6	336.6	31.8
CC2640R2FTWRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0

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