- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  Active Mode: 250 μA at 1 MHz, 2.2 V
  Standby Mode: 1.1 μA
  Off Mode (RAM Retention): 0.1 μA
- **Five Power Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Sigma-Delta A/D Converter With Internal Reference and Five Differential Analog Inputs**
- **12-Bit D/A Converter**
- **Two Configurable Operational Amplifiers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Brownout Detector**
- **Bootstrap Loader**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Integrated LCD Driver With Contrast Control for up to 56 Segments**
- **MSP430FG42x0 Family Members Include:**
  MSP430FG4250: 16KB+256B Flash Memory 256B RAM
  MSP430FG4260: 24KB+256B Flash Memory 256B RAM
  MSP430FG4270: 32KB+256B Flash Memory 256B RAM
- **For Complete Module Descriptions, See *MSP430x4xx Family User's Guide*, Literature Number SLAU056**
- **For Additional Device Information, See *MSP430FG42x0 Device Erratasheet,* Literature Number SLAZ038**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430FG42x0 is a microcontroller configuration with a 16-bit timer, a high-performance 16-bit sigma-delta A/D converter, 12-bit D/A converter, two configurable operational amplifiers, 32 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 48-PIN SSOP (DL)	PLASTIC 48-PIN QFN (RGZ)
–40°C to 85°C	MSP430FG4250IDL	MSP430FG4250IRGZ
	MSP430FG4260IDL	MSP430FG4260IRGZ
	MSP430FG4270IDL	MSP430FG4270IRGZ



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



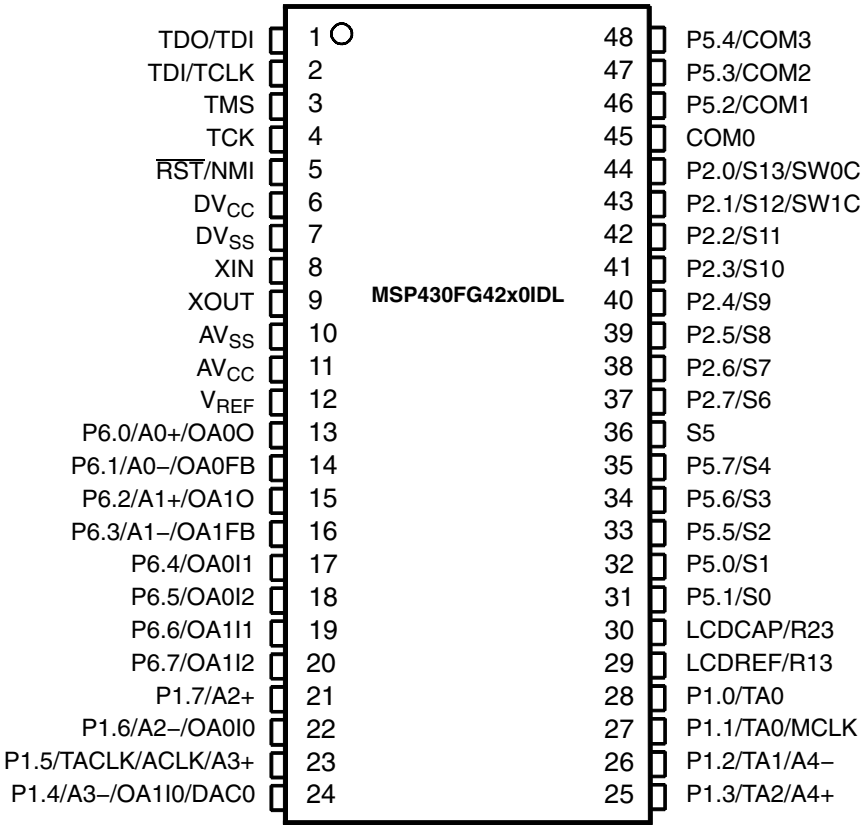
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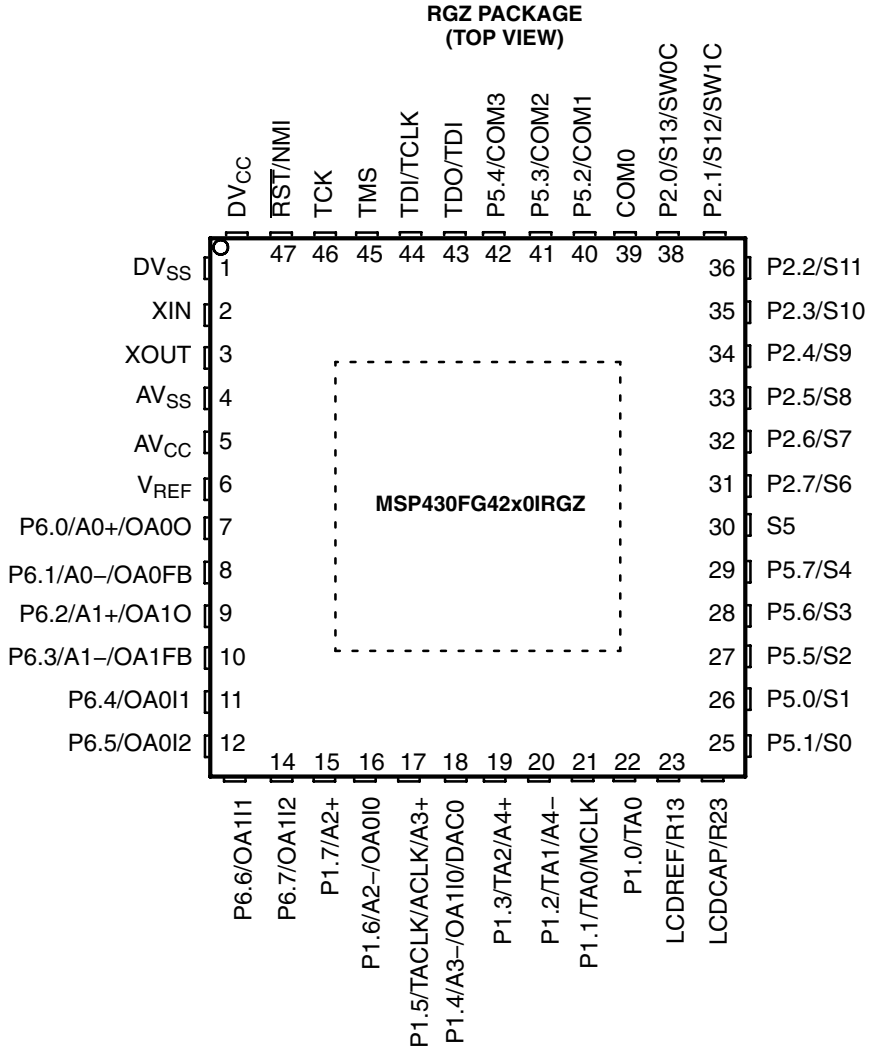
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pin designation, DL package

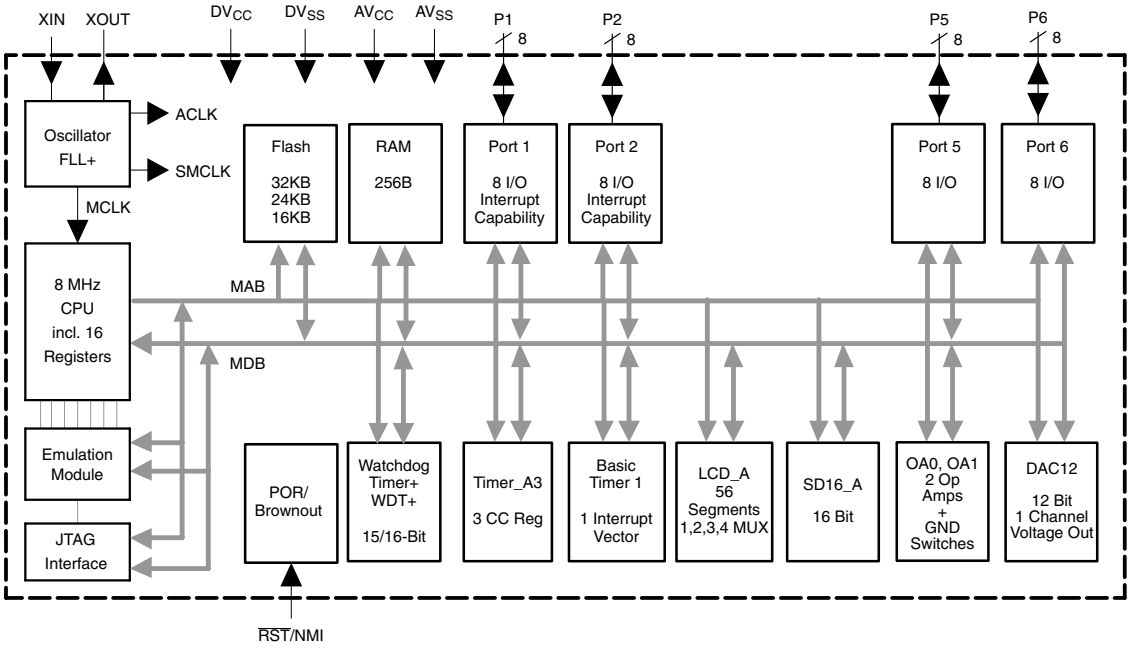
**DL PACKAGE
(TOP VIEW)**



pin designation, RGZ package



functional block diagram



Terminal Functions

TERMINAL				DESCRIPTION
NAME	DL NO.	RGZ NO.	I/O	
TDO/TDI	1	43	I/O	Test data output. TDO/TDI data output or programming data input terminal
TDI/TCLK	2	44	I	Test data input / test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	3	45	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	4	46	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	5	47	I	General-purpose digital I/O / reset input / nonmaskable interrupt input
DV_{CC}	6	48		Digital supply voltage, positive terminal
DV_{SS}	7	1		Digital supply voltage, negative terminal
XIN	8	2	I	Input terminal of crystal oscillator XT1
XOUT	9	3	O	Output terminal of crystal oscillator XT1
AV_{SS}	10	4		Analog supply voltage, negative terminal
AV_{CC}	11	5		Analog supply voltage, positive terminal
V_{REF}	12	6	I/O	Analog reference voltage
P6.0/A0+/OA0O	13	7	I/O	General-purpose digital I/O / analog input A0+ / OA0 output
P6.1/A0–/OA0FB	14	8	I/O	General-purpose digital I/O / analog input A0– / OA0 feedback input
P6.2/A1+/OA1O	15	9	I/O	General-purpose digital I/O / analog input A1+ / OA1 output
P6.3/A1–/OA1FB	16	10	I/O	General-purpose digital I/O / analog input A1– / OA1 feedback input
P6.4/OA0I1	17	11	I/O	General-purpose digital I/O / OA0 input multiplexer on –terminal
P6.5/OA0I2	18	12	I/O	General-purpose digital I/O / OA0 input multiplexer on –terminal
P6.6/OA1I1	19	13	I/O	General-purpose digital I/O / OA1 input multiplexer on –terminal
P6.7/OA1I2	20	14	I/O	General-purpose digital I/O / OA1 input multiplexer on –terminal
P1.7/A2+	21	15	I/O	General-purpose digital I/O / analog input A2+
P1.6/A2–/OA0I0	22	16	I/O	General-purpose digital I/O / analog input A2– / OA0 input multiplexer on +terminal
P1.5/TACLK/ACLK/A3+	23	17	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8) / analog input A3+
P1.4/A3–/OA1I0/DAC0	24	18	I/O	General-purpose digital I/O / analog input A3– / OA1 input multiplexer on +terminal / DAC12 output
P1.3/TA2/A4+	25	19	I/O	General-purpose digital I/O / Timer_A, Capture: CCI2A, compare: Out2 output / analog input A4+
P1.2/TA1/A4–	26	20	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A, compare: Out1 output / analog input A4–
P1.1/TA0/MCLK	27	21	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin / BSL Receive
P1.0/TA0	28	22	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
LCDREF/R13	29	23		External LCD reference voltage input / input port of third most positive analog LCD level (V4 or V3)
LCDCAP/R23	30	24		Capacitor connection for LCD charge pump / input port of second most positive analog LCD level (V2)
P5.1/S0	31	25	I/O	General-purpose digital I/O / LCD segment output 0
P5.0/S1	32	26	I/O	General-purpose digital I/O / LCD segment output 1
P5.5/S2	33	27	I/O	General-purpose digital I/O / LCD segment output 2
P5.6/S3	34	28	I/O	General-purpose digital I/O / LCD segment output 3
P5.7/S4	35	29	I/O	General-purpose digital I/O / LCD segment output 4
S5	36	30	O	LCD segment output 5
P2.7/S6	37	31	I/O	General-purpose digital I/O / LCD segment output 6
P2.6/S7	38	32	I/O	General-purpose digital I/O / LCD segment output 7

Terminal Functions (Continued)

TERMINAL				DESCRIPTION
NAME	DL NO.	RGZ NO.	I/O	
P2.5/S8	39	33	I/O	General-purpose digital I/O / LCD segment output 8
P2.4/S9	40	34	I/O	General-purpose digital I/O / LCD segment output 9
P2.3/S10	41	35	I/O	General-purpose digital I/O / LCD segment output 10
P2.2/S11	42	36	I/O	General-purpose digital I/O / LCD segment output 11
P2.1/S12/SW1C	43	37	I/O	General-purpose digital I/O / LCD segment output 12 / Low resistance switch to V_{SS}
P2.0/S13/SW0C	44	38	I/O	General-purpose digital I/O / LCD segment output 13 / Low resistance switch to V_{SS}
COM0	45	39	O	Common output. COM0–COM3 are used for LCD backplanes.
P5.2/COM1	46	40	I/O	General-purpose digital I/O / common output. COM0–COM3 are used for LCD backplanes.
P5.3/COM2	47	41	I/O	General-purpose digital I/O / common output. COM0–COM3 are used for LCD backplanes.
P5.4/COM3	48	42	I/O	General-purpose digital I/O / common output. COM0–COM3 are used for LCD backplanes.
QFN Pad	NA	None	NA	QFN package pad connection to DV_{SS} is recommended.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats. Table 2 lists the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 –––> R5
Single operands, destination only	e.g., CALL R8	PC –––>(TOS), R8–––> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	●	●	MOV & MEM, & TCDAT		M(MEM) —> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is available to modules
    FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is available to modules
    FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 3. Interrupt Sources, Flags, and Vectors of MSP430FG42x0 Configuration

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory PC Out-of-Range (see Note 4)	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
			0FFFAh	13
SD16_A	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG (see Notes 1 and 2)	Maskable	0FFF8h	12
			0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
DAC12	DAC12_0IFG (see Note 2)	Maskable	0FFE6h	3
			0FFE4h	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address ranges (MSP430FG4270, MSP430FG4260: from 0300h to 0BFFh and from 01100h to 07FFFh, MSP430FG4250: from 0300h to 0BFFh and from 01100h to 0BFFFh).

special function registers (SFRs)

The MSP430 SFRs are located in the lowest address space and are organized as byte-mode registers. SFRs should be accessed with byte instructions.

interrupt enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw–0	rw–0			rw–0	rw–0

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE							
	rw–0							

BTIE: Basic timer interrupt enable

interrupt flag registers 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw–0			rw–1	rw–(0)

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode

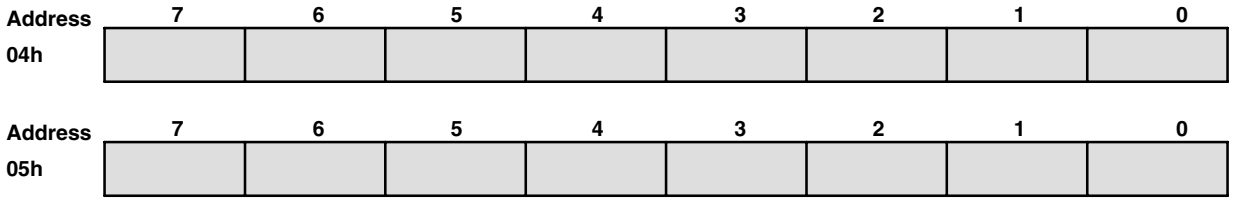
OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG							
	rw–0							

BTIFG: Basic timer flag

module enable registers 1 and 2



Legend: rw: Bit Can Be Read and Written
rw–0,1: Bit Can Be Read and Written. It Is Reset or Set by PUC.
rw–(0,1): Bit Can Be Read and Written. It Is Reset or Set by POR.
SFR Bit Not Present in Device

memory organization

		MSP430FG4250	MSP430FG4260	MSP430FG4270
Memory Main: interrupt vector Main: code memory	Size Flash Flash	16KB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	24KB 0FFFFh – 0FFE0h 0FFFFh – 0A000h	32KB 0FFFFh – 0FFE0h 0FFFFh – 08000h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	256 Byte 02FFh – 0200h	256 Byte 02FFh – 0200h	256 Byte 02FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

bootstrap loader (BSL)

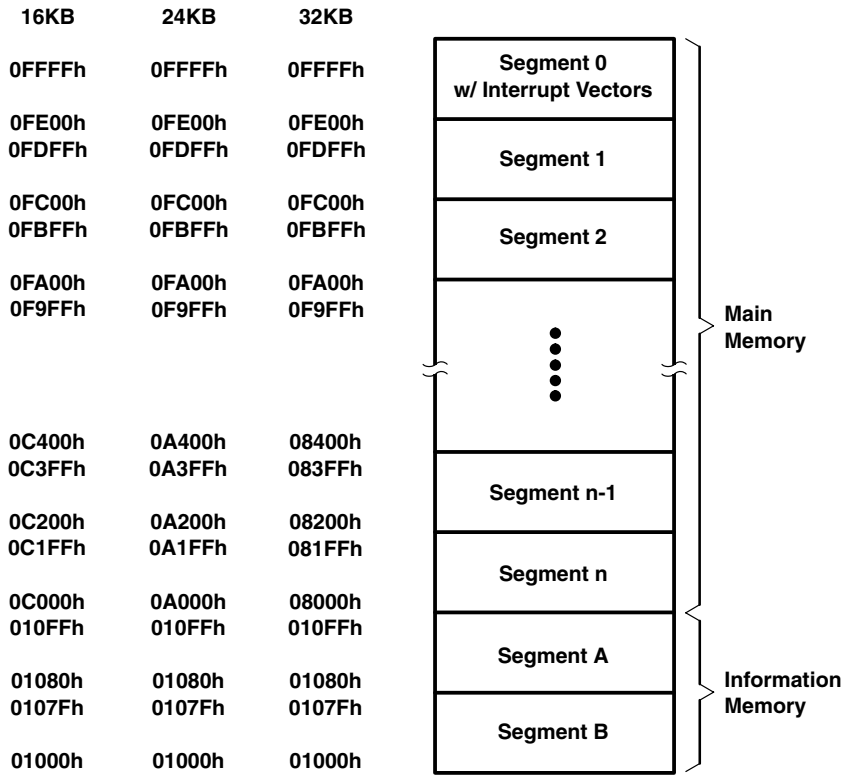
The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

BSL Function	DL Package Pins	RGZ Package Pins
Data Transmit	28 - P1.0	22 - P1.0
Data Receive	27 - P1.1	21 - P1.1

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, literature number SLAU056.

oscillator and system clock

The clock system in the MSP430FG42x0 family of devices is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P5, and P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 can be used to generate periodic interrupts.

LCD driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2–MUX, 3–MUX, and 4–MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and thus contrast in software.

watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections							
Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
DL	RGZ					DL	RGZ
23 - P1.5	17 - P1.5	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
23 - P1.5	17 - P1.5	$\overline{\text{TACLK}}$	INCLK				
28 - P1.0	22 - P1.0	TA0	CCI0A	CCR0	TA0	28 - P1.0	22 - P1.0
27 - P1.1	21 - P1.1	TA0	CCI0B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
26 - P1.2	20 - P1.2	TA1	CCI1A	CCR1	TA1	26 - P1.2	20 - P1.2
26 - P1.2	20 - P1.2	TA1	CCI1B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
25 - P1.3	19 - P1.3	TA2	CCI2A	CCR2	TA2	25 - P1.3	19 - P1.3
		ACLK (internal)	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

SD16_A

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and reference generator. In addition to external analog inputs, an internal V_{CC} sense and temperature sensor are also available.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode.

operational amplifier (OA)

The MSP430FG42x0 has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offers a flexible choice of connections for various applications. The OAs primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

OA Signal Connections							
Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
DL	RGZ					DL	RGZ
22 - P1.6	16 - P1.6	OA0I0	OA0I0	OA0	OA0O	13 - P6.0	7 - P6.0
17 - P6.4	11 - P6.4	OA0I1	OA0I1				
18 - P6.5	12 - P6.5	OA0I2	OA0I2				
14 - P6.1	8 - P6.1	OA0FB	OA0FB				
24 - P1.4	18 - P1.4	OA1I0	OA1I0	OA1	OA1O	15 - P6.0	9 - P6.0
19 - P6.6	13 - P6.6	OA1I1	OA1I1				
20 - P6.7	14 - P6.7	OA1I2	OA1I2				
16 - P6.1	10 - P6.1	OA1FB	OA1FB				

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DAC12	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
SD16_A (see also Peripherals With Byte Access)	General control	SD16CTL	0100h
	Channel 0 control	SD16CCTL0	0102h
	Interrupt vector word register	SD16IV	0110h
	Channel 0 conversion memory	SD16MEM0	0112h
PERIPHERALS WITH BYTE ACCESS			
OA/GND Switches	Switch control register	SWCTL	0CFh
OA1	Operational amplifier 1 control register 1	OA1CTL1	0C3h
	Operational amplifier 1 control register 0	OA1CTL0	0C2h
OA0	Operational amplifier 0 control register 1	OA0CTL1	0C1h
	Operational amplifier 0 control register 0	OA0CTL0	0C0h
SD16_A (see also: Peripherals with Word Access)	Channel 0 input control	SD16INCTL0	0B0h
	Analog enable	SD16AE	0B7h
LCD_A	LCD voltage control 1	LCDAVCTL1	0AFh
	LCD voltage control 0	LCDAVCTL0	0AEh
	LCD voltage port control 1	LCDAPCTL1	0ADh
	LCD voltage port control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDACTL	090h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
FLL+ Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 1) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: Unprogrammed device . . . . . –55°C to 150°C
Programmed device . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage during program execution (see Note 1), V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			1.8		3.6	V
Supply voltage during flash memory programming (see Note 1), V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			2.5		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})			0		0	V
Operating free-air temperature, T_A			–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL=0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

NOTES: 1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

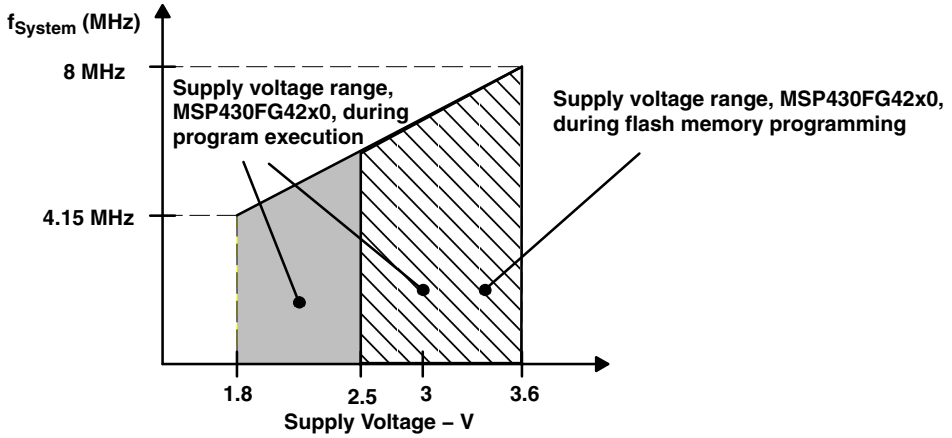


Figure 1. Frequency vs Supply Voltage, Typical Characteristic

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode (see Note 1), $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		250	370	µA
			V_{CC} = 3 V		400	520	
$I_{(LPM0)}$	Low-power mode (LPM0) (see Note 1 and Note 4)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		55	70	µA
			V_{CC} = 3 V		95	110	
$I_{(LPM2)}$	Low-power mode (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0 (see Note 2 and Note 4)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode (LPM3), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0 (static mode, $f_{LCD} = f_{(ACLK)}/32$), (see Note 2, Note 3, and Note 4)	T_A = –40°C	V_{CC} = 2.2 V		1.0	2.0	µA
		T_A = 25°C			1.1	2.0	
		T_A = 60°C			2.0	3.0	
		T_A = 85°C			3.5	6.0	
		T_A = –40°C	V_{CC} = 3 V		1.8	2.8	
		T_A = 25°C			1.6	2.7	
		T_A = 60°C			2.5	3.5	
		T_A = 85°C			4.2	7.5	
$I_{(LPM3)}$	Low-power mode (LPM3), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0 (4-mux mode, $f_{LCD} = f_{(ACLK)}/32$), (see Note 2, Note 3, and Note 4)	T_A = –40°C	V_{CC} = 2.2 V		2.5	3.5	µA
		T_A = 25°C			2.5	3.5	
		T_A = 85°C			3.8	6.0	
		T_A = –40°C	V_{CC} = 3 V		2.9	4.0	
		T_A = 25°C			2.9	4.0	
		T_A = 85°C			4.4	7.5	
$I_{(LPM4)}$	Low-power mode (LPM4), $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2 and Note 4)	T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.7	1.1	
		T_A = 85°C			1.7	3.0	
		T_A = –40°C	V_{CC} = 3 V		0.1	0.8	
		T_A = 25°C			0.1	0.8	
		T_A = 60°C			0.8	1.2	
		T_A = 85°C			1.9	3.5	

NOTES: 1. Timer_A is clocked by $f_{(DCOCLK)} = f_{(DCO)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V–T1A (9 pF) crystal and OSCCAPx = 01h.
4. Current for brownout included.

current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)}\ [1\ MHz] \times f_{(System)}\ [MHz]$$

current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P5, and P6; $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.55	V
		V_{CC} = 3 V	1.5		1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – ports P1, P2, P5, and P6 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(x = 1, 2, 5, 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V / 3 V	DC		f_{System}	MHz
$f_{(MCLK)}$	P1.1/TA0/MCLK	C_L = 20 pF				f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

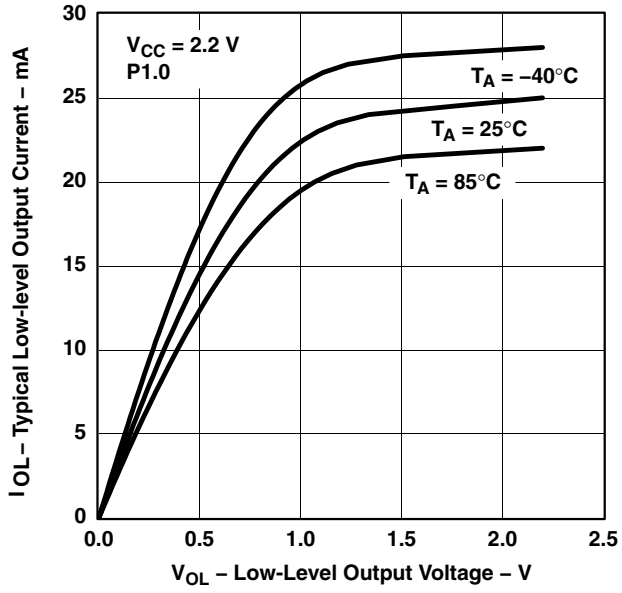


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

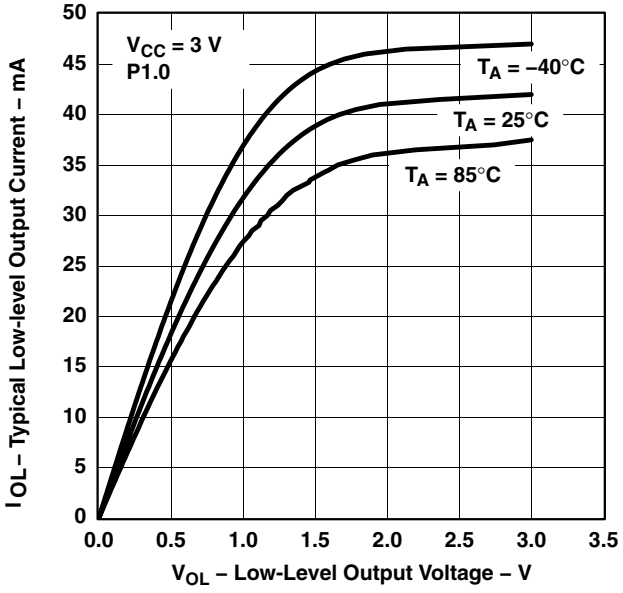


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

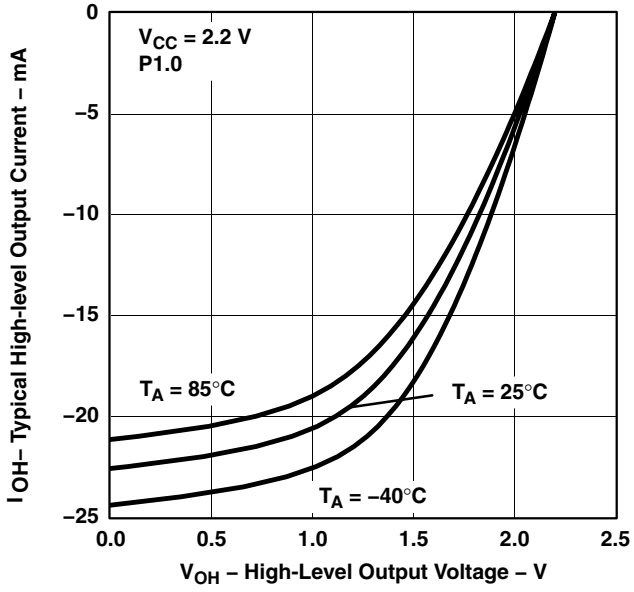


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

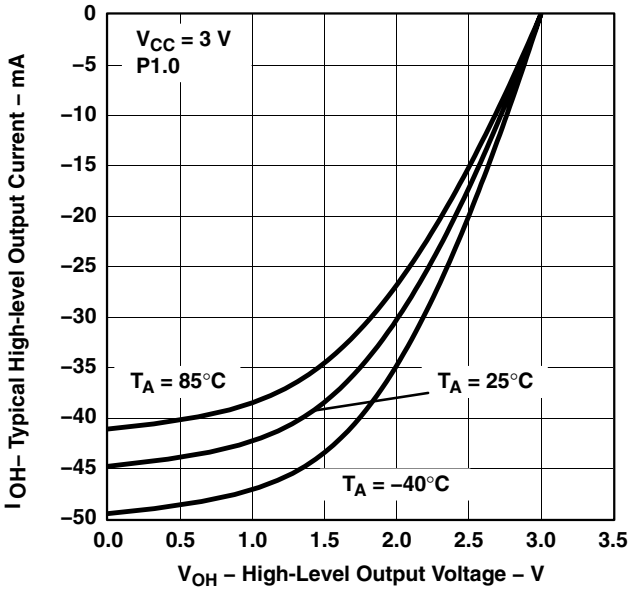


Figure 5

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD_A

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply voltage	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP (see Note 1)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		4.7			µF
$I_{CC(LCD)}$	Average supply current (see Note 2)	$V_{LCD(typ)}$=3V, LCDCPEN = 1, VLCDx= 1000, all segments on f_{LCD}= f_{ACLK}/32 no LCD connected (see Note 3) T_A = 25°C	2.2 V		3.8		µA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			VCC		V
		VLCDx = 0001			2.60		
		VLCDx = 0010			2.66		
		VLCDx = 0011			2.72		
		VLCDx = 0100			2.78		
		VLCDx = 0101			2.84		
		VLCDx = 0110			2.90		
		VLCDx = 0111			2.96		
		VLCDx = 1000			3.02		
		VLCDx = 1001			3.08		
		VLCDx = 1010			3.14		
		VLCDx = 1011			3.20		
		VLCDx = 1100			3.26		
		VLCDx = 1101			3.32		
		VLCDx = 1110			3.38		
		VLCDx = 1111			3.44	3.60	
R_{LCD}	LCD driver output impedance	V_{LCD} = 3V, LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 µA	2.2 V			10	kΩ

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Refer to the supply current specifications $I_{(LPM3)}$ for additional current specifications with the LCD_A module active.
3. Connecting an actual display will increase the current consumption depending on the size of the LCD.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 6)		$0.7 \times V_{(B_IT-)}$		V
$V_{(B_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 6 through Figure 8)			1.71	V
$V_{hys(B_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 6)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout.

typical characteristics

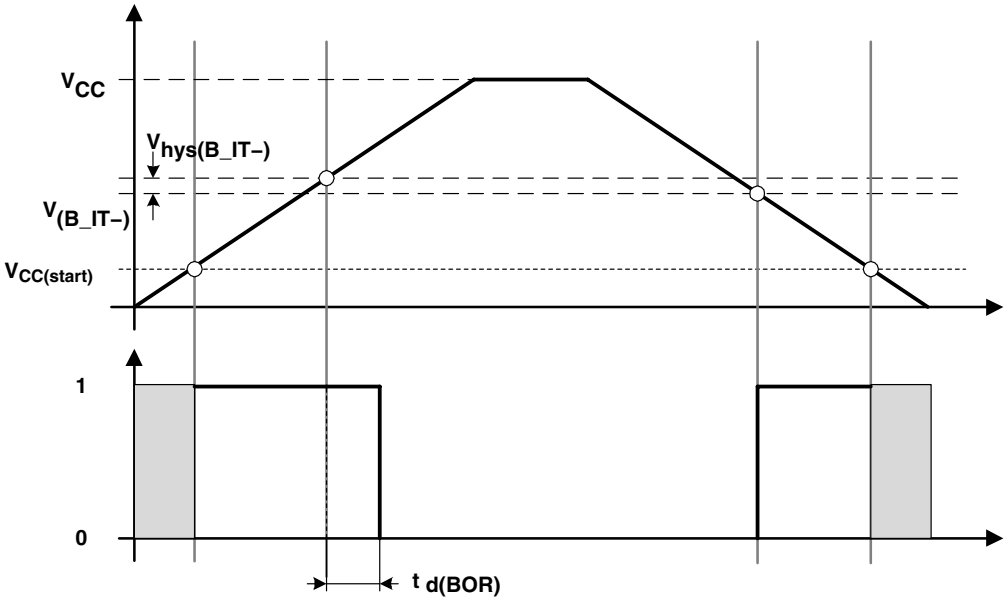


Figure 6. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics (continued)

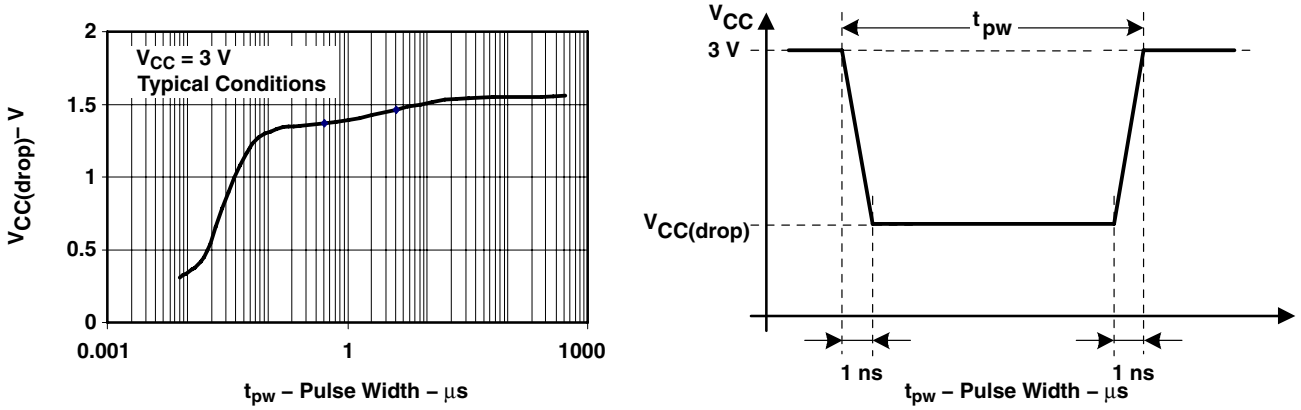


Figure 7. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

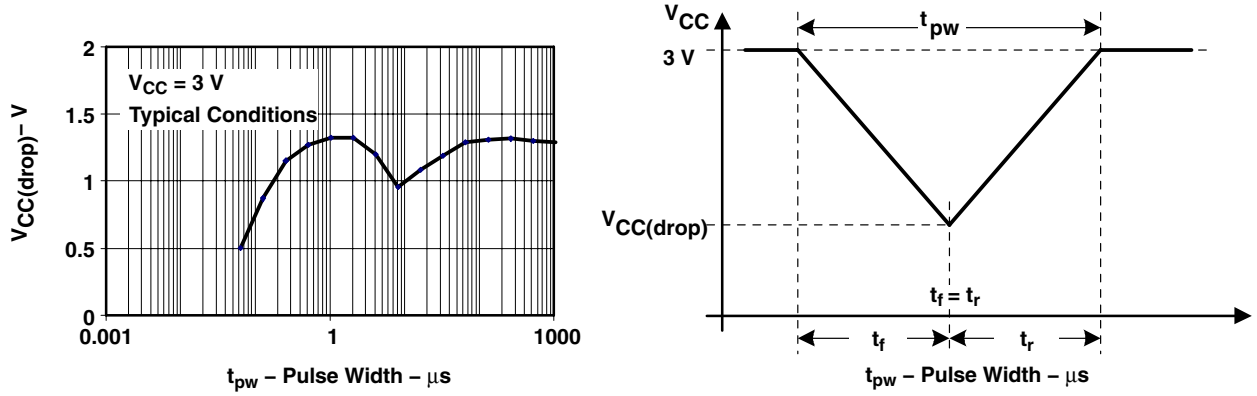


Figure 8. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01Eh, FN_8=FN_4=FN_3=FN_2=0, D = 2, DCOPLUS= 0, $f_{Crystal}$ = 32.768 kHz	2.2 V/3 V		1		MHz
$f_{(DCO=2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO=27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO=2)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO=27)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO=2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO=27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO=2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO=27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO=2)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO=27)}$	FN_8= 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 10 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0 (see Note 2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		0	5	15	%/V

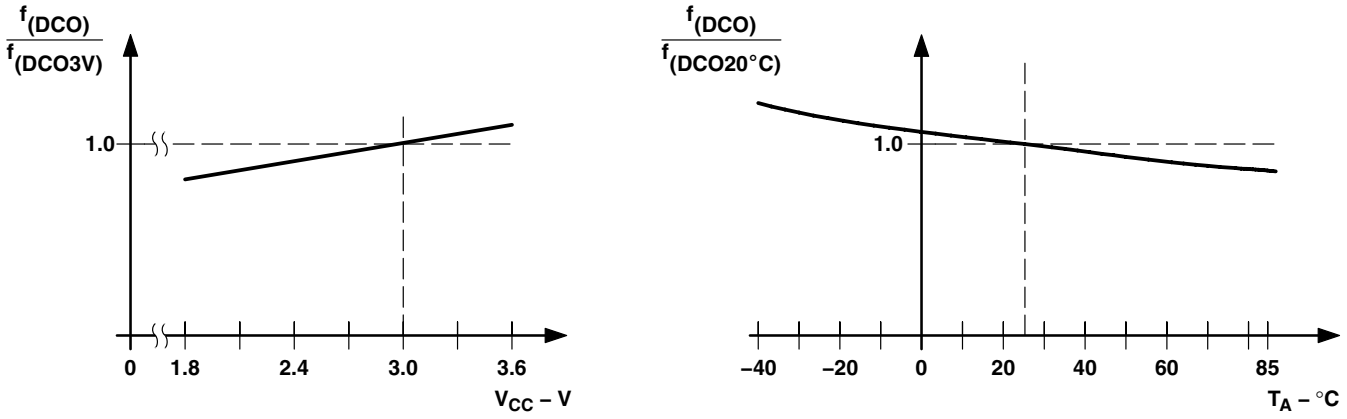


Figure 9. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

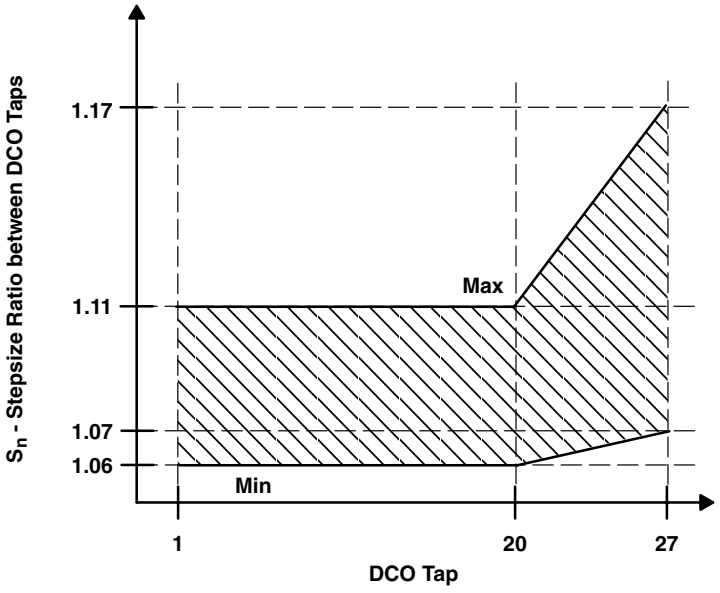


Figure 10. DCO Tap Step Size

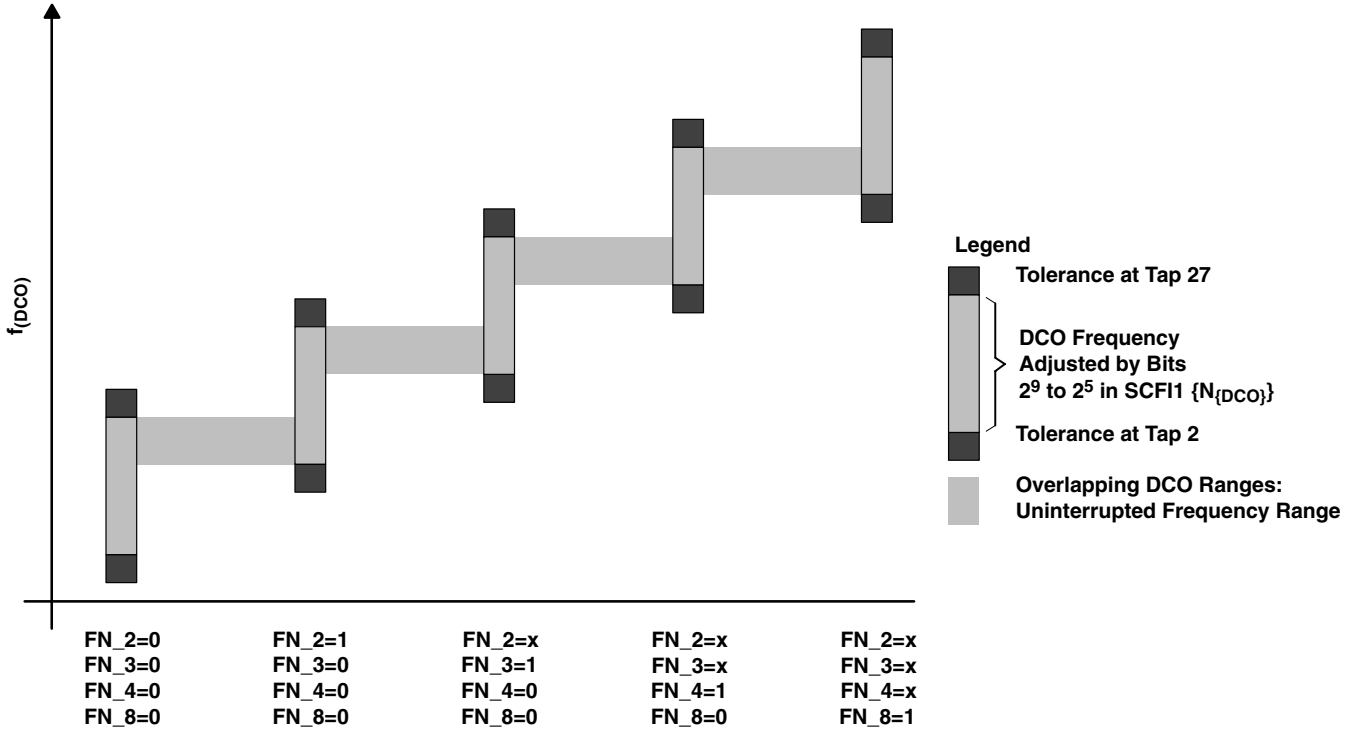


Figure 11. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
C_{XOUT}	Integrated output capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 3)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. This is independent of XTS_FLL.

2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep as short of a trace as possible between the ’FG42x0 and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications, OSCCAPx = 0h.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, power supply and recommended operating conditions

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$			2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1,2	3 V		650	950	µA
			SD16BUFx = 00, GAIN: 4,8,16			730	1100	
			SD16BUFx = 00, GAIN: 32			1050	1550	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1			620	930	
			SD16BUFx = 00, GAIN: 32			700	1060	
		SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 01, GAIN: 1			850		
			SD16BUFx = 10, GAIN: 1			1130		
			SD16BUFx = 11, GAIN: 1			1130		
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)			0.03	0.5		

SD16_A, input range

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full scale input voltage range	Bipolar mode, SD16UNI = 0			$-V_{REF}/2GAIN$		$+V_{REF}/2GAIN$	mV
		Unipolar mode, SD16UNI = 1			0		$+V_{REF}/2GAIN$	
V_{ID}	Differential input voltage range for specified performance (see Note 1)	SD16REFON=1	SD16GAINx = 1			±500		mV
			SD16GAINx = 2			±250		
			SD16GAINx = 4			±125		
			SD16GAINx = 8			±62		
			SD16GAINx = 16			±31		
			SD16GAINx = 32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1MHz, SD16BUFx = 00	SD16GAINx = 1	3 V		200		kΩ
			SD16GAINx = 32			75		
		f_{SD16} = 1MHz, SD16BUFx = 01	SD16GAINx = 1			>10		MΩ
Z_{ID}	Differential Input impedance (IN+ to IN–)	f_{SD16} = 1MHz, SD16BUFx = 00	SD16GAINx = 1	3 V	300	400		kΩ
			SD16GAINx = 32		100	150		
		f_{SD16} = 1MHz, SD16BUFx > 00	SD16GAINx = 1			>10		MΩ
V_I	Absolute input voltage range	SD16BUFx = 00			AV_{SS} – 0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS}		AV_{CC} –1.2V	
V_{IC}	Common-mode input voltage range	SD16BUFx = 00			AV_{SS} – 0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS}		AV_{CC} –1.2V	

NOTES: 1. The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, performance (f_{SD16} = 30kHz, SD16REFON = 1, SD16BUFx = 01)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 256	f_{IN} = 2.8Hz	3 V		84		dB
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 512				84		
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 1024				84		
	Nominal gain	SD16GAINx = 1, SD16OSRx = 1024		3 V	0.97	1.00	1.02	
dG/dT	Gain temperature drift	SD16GAINx = 1, SD16OSRx = 1024 (see Note 1)		3 V		15		ppm/°C
dG/dV_{CC}	Gain supply voltage drift	SD16GAINx = 1, SD16OSRx = 1024, V_{CC} = 2.5 V to 3.6 V (see Note 2)				0.35		%/V

NOTES: 1. Calculated using the box method: (MAX(–40...85°C) – MIN(–40...85°C))/MIN(–40...85°C)/(85C – (–40°C))
2. Calculated using the box method: (MAX(2.5...3.6V) – MIN(2.5...3.6V))/MIN(2.5...3.6V)/(3.6V – 2.5V)

SD16_A, performance (f_{SD16} = 1MHz, SD16OSRx = 256, SD16REFON = 1, SD16BUFx = 00)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500mV	f_{IN} = 50 Hz, 100 Hz	3 V	83.5	85		dB
		SD16GAINx = 2,Signal Amplitude = 250mV			81.5	84		
		SD16GAINx = 4,Signal Amplitude = 125mV			76	79.5		
		SD16GAINx = 8,Signal Amplitude = 62mV			73	76.5		
		SD16GAINx = 16,Signal Amplitude = 31mV			69	73		
		SD16GAINx = 32,Signal Amplitude = 15mV			62	69		
G	Nominal gain	SD16GAINx = 1		3 V	0.97	1.00	1.02	
		SD16GAINx = 2			1.90	1.96	2.02	
		SD16GAINx = 4			3.76	3.86	3.96	
		SD16GAINx = 8			7.36	7.62	7.84	
		SD16GAINx = 16			14.56	15.04	15.52	
		SD16GAINx = 32			27.20	28.35	29.76	
E_{OS}	Offset error	SD16GAINx = 1		3 V			±0.2	%FSR
		SD16GAINx = 32					±1.5	
dE_{OS}/dT	Offset error temperature coefficient	SD16GAINx = 1		3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32				±20	±100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz				>75		
AC PSRR	AC power supply rejection ratio	SD16GAINx = 1, V_{CC} = 3 V ± 100 mV, f_{VCC} = 50 Hz		3 V		>80		dB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, temperature sensor

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/K
$V_{Offset,sensor}$	Sensor offset voltage			–100		100	mV
V_{Sensor}	Sensor output voltage (see Note 2)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C		355	395	435	
		Temperature sensor voltage at T_A = 0°C		320	360	400	

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor} (273 + T [°C]) + V_{Offset,sensor}$ [mV]
2. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.

SD16_A, built-in voltage reference

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	µA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0	3 V		18	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0 (see Note 1)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1, SD16VMIDON = 0	3 V			±200	nA
t_{ON}	Turn-on time	SD16REFON = 0–>1, SD16VMIDON = 0, C_{REF} = 100 nF	3 V		5		ms
DC PSR	DC power-supply rejection, $\Delta V_{REF}/\Delta V_{CC}$	SD16REFON = 1, SD16VMIDON = 0, V_{CC} = 2.5 V to 3.6 V			100		µV/V

NOTES: 1. There is no capacitance required on V_{REF}. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

SD16_A, reference output buffer

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference supply + reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	µA
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			±1	mA
	Maximum voltage variation vs load current	$\|I_{LOAD}\|$ = 0 to 1 mA	3 V	–15		+15	mV
t_{ON}	Turn-on time	SD16REFON = 0–>1, SD16VMIDON = 1, C_{REF} = 470 nF	3 V		100		µs

SD16_A, external reference input

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.20		3.60	V
I_{DD}	Supply current (see Notes 1 and 2)	DAC12AMPx = 2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		50	110	µA
		DAC12AMPx = 2, DAC12IR=1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			50	110	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			200	440	
		DAC12AMPx=7, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, $V_{REF,DAC12}$ = 1.2V ΔAV_{CC} = 100 mV	2.7V		70		dB

NOTES: 1. No load at the output pin assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. $PSRR = 20 \times \log\{\Delta AV_{CC}/\Delta V_{DAC12_xOUT}\}$.
4. V_{REF} is applied externally. The internal reference is not used.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic		12			bits
INL	Integral nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V		±2.0	±8.0	LSB
DNL	Differential nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V		±0.4	±1.0	LSB
E_O	Offset voltage w/o calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V			±20	mV
	Offset voltage with calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V			±2.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.7 V		±30		µV/C
E_G	Gain error (see Note 1)	$V_{REF,DAC12}$ = 1.2 V	2.7 V			±3.50	% FSR
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.7 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx = 2	2.7 V			100	ms
		DAC12AMPx = 3, 5	2.7 V			32	
		DAC12AMPx = 4, 6, 7	2.7 V			6	

NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b*x. $V_{DAC12_xOUT} = E_O + (1 + E_G) * (V_{REF,DAC12}/4095) *$ DAC12_xDAT, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

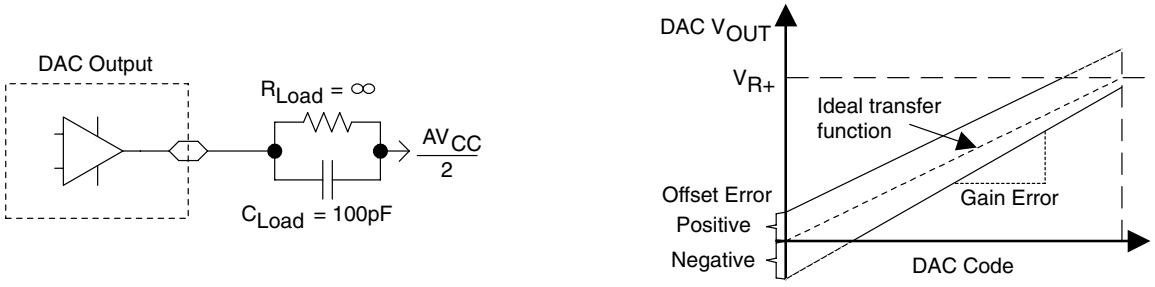
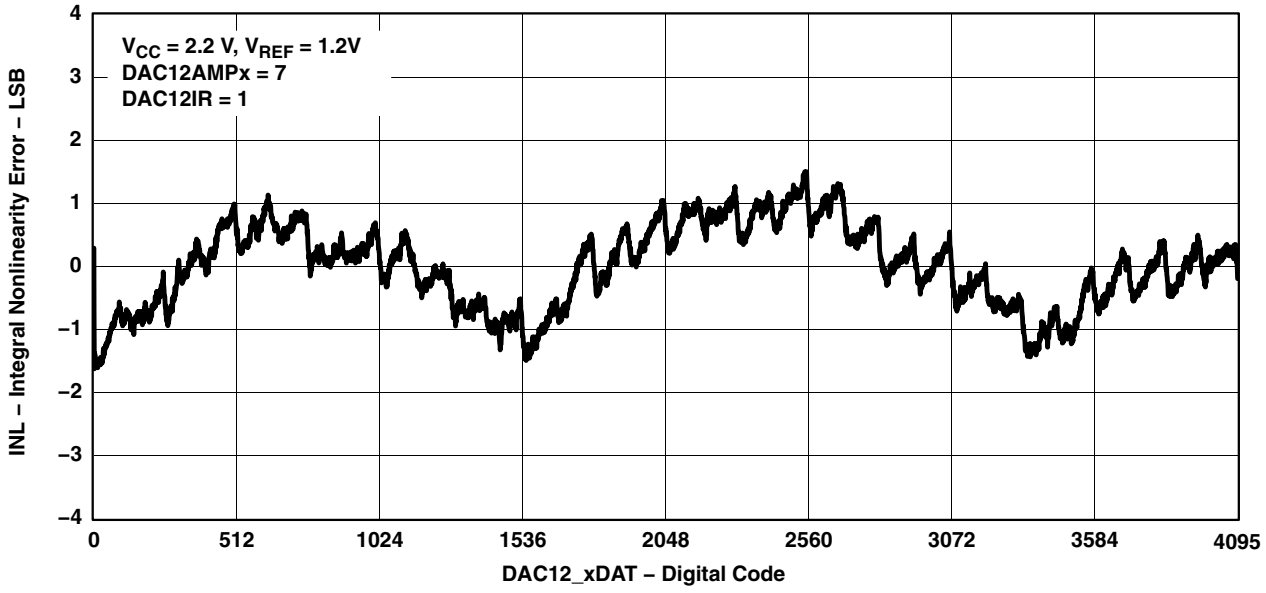


Figure 12. Linearity Test Load Conditions and Gain/Offset Definition

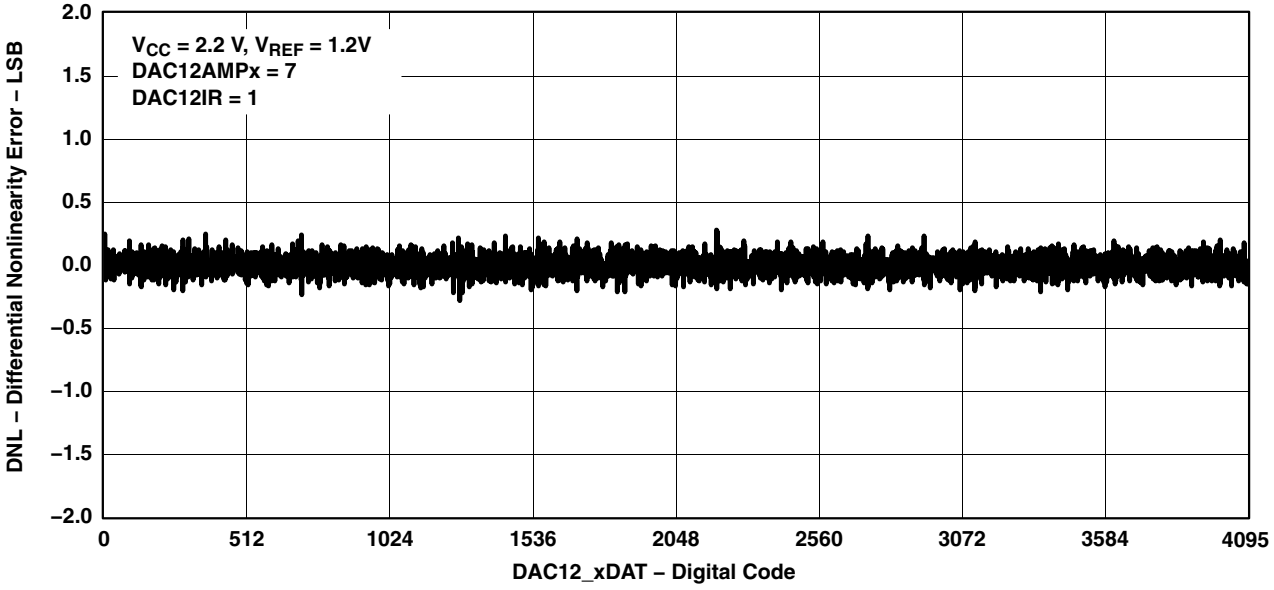
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

TYPICAL INL ERROR vs DIGITAL INPUT DATA



TYPICAL DNL ERROR vs DIGITAL INPUT DATA



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1, Figure 15)	No load, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.005	V
		No load, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC}–0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC}–0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2V/3V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2V	–0.5		+0.5	mA
			3V	–1.0		+1.0	
$R_{O/P(DAC12)}$	Output resistance (see Figure 15)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2V/3V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$ – 0.3 V DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)} \le AV_{CC}$ – 0.3 V			1	4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

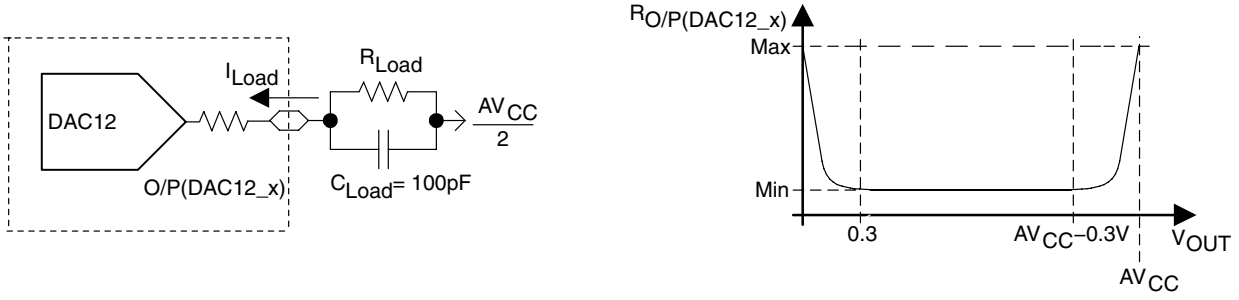


Figure 15. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Reference input voltage range	DAC12IR=0 (see Notes 1 and 2)	2.2V/3V		$AV_{CC}/3$	AV_{CC}+0.2	V
		DAC12IR=1 (see Notes 3 and 4)			AV_{CC}	AV_{CC}+0.2	
$Ri_{(VREF)}$	Reference input resistance	DAC12IR=0	2.2V/3V	20			MΩ
		DAC12IR=1		40	48	56	kΩ

NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
2. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} – V_{E(O)}] / [3*(1 + E_G)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
4. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} – V_{E(O)}] / (1 + E_G)$.

12-bit DAC, dynamic specifications, $V_{REF,DAC12} = AV_{CC}$, DAC12IR = 1 (see Figure 16 and Figure 17)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (see Note 1,Figure 16)	DAC12AMPx=0 → {2, 3, 4}	2.2V/3V		60	120	µs
			DAC12AMPx=0 → {5, 6}			15	30	
			DAC12AMPx=0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		100	200	µs
			DAC12AMPx=3,5			40	80	
			DAC12AMPx=4,6,7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12AMPx=2	2.2V/3V		5		µs
			DAC12AMPx=3,5			2		
			DAC12AMPx=4,6,7			1		
SR	Slew rate	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V	0.05	0.12		V/µs
			DAC12AMPx=3,5		0.35	0.7		
			DAC12AMPx=4,6,7		1.5	2.7		
Glitch energy, full scale		DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		10		nV-s
			DAC12AMPx=3,5			10		
			DAC12AMPx=4,6,7			15		

NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 16.
2. Slew rate applies to output voltage steps ≥ 200mV.

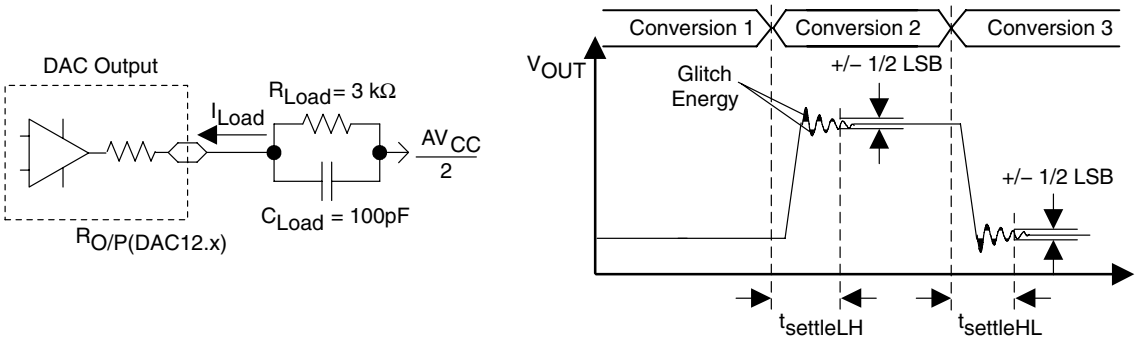


Figure 16. Settling Time and Glitch Energy Testing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

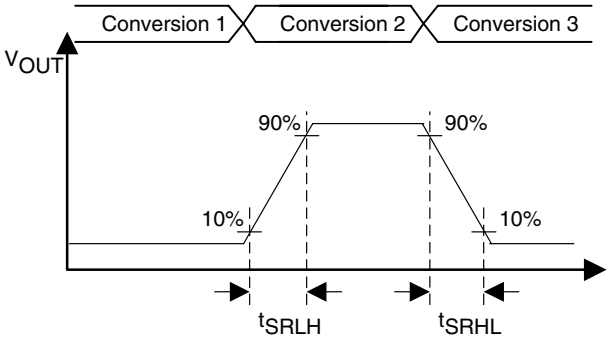


Figure 17. Slew Rate Testing

12-bit DAC, dynamic specifications (continued) (T_A = 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC}=1.5 V, V_{AC}=0.1 V_{PP} (see Figure 18)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550			

NOTES: 1. R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

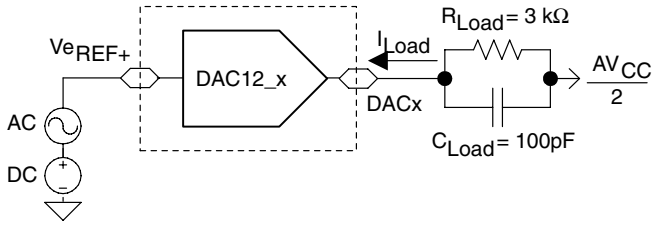


Figure 18. Test Conditions for 3-dB Bandwidth Specification

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		—	2.2		3.6	V
I_{CC}	Supply current (see Note 1)	Fast Mode	2.2 V/3 V		180	290	μA
		Medium Mode			110	190	
		Slow Mode			50	80	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V/3 V		70		dB

NOTES: 1. P6SEL.x = 1 or SD16AE.x = 1 for each corresponding pin when used in OA input or OA output mode.

operational amplifier OA, input/output specifications

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Input voltage, I/P			—	–0.1		V_{CC}–1.2	V
I_{lkg}	Input leakage current, I/P (see Notes 1 and 2)	T_A = –40°C to 55°C		—	–5	±0.5	5	nA
		T_A = 55°C to 85°C			–20	±5	20	nA
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz	—		50		nV/√Hz
		Medium Mode				80		
		Slow Mode				140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium Mode				50		
		Slow Mode				65		
V_{IO}	Offset voltage, I/P			2.2 V/3 V			±10	mV
	Offset temperature drift, I/P	see Note 3		2.2 V/3 V		±10		μV/°C
	Offset voltage drift with supply, I/P	0.3V ≤ V_{IN} ≤ V_{CC}–0.3 V ΔV_{CC}≤ ± 10%, T_A = 25°C		2.2 V/3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ –500 μA		2.2 V	V_{CC}–0.2		V_{CC}	V
		Slow Mode,I_{SOURCE} ≤ –150 μA		3 V	V_{CC}–0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500 μA		2.2 V	V_{SS}		0.2	V
		Slow Mode,I_{SOURCE} ≤ +150 μA		3 V	V_{SS}		0.1	
CMRR	Common-mode rejection ratio	Non-inverting		2.2 V/3 V		70		dB

NOTES: 1. ESD damage can degrade input current leakage.
2. The input bias current is overridden by the input leakage current.
3. Characterized and calculated using the box method, not production tested.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, dynamic specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode	—		1.2		V/μs
		Medium Mode			0.8		
		Slow Mode			0.3		
	Open-loop voltage gain		—		100		dB
ϕ_m	Phase margin	C_L = 50 pF	—		60		deg
	Gain margin	C_L = 50 pF	—		20		dB
GBW	Gain-bandwidth product (see Figure 19 and Figure 20)	Noninverting, Fast Mode, R_L = 47kΩ, C_L = 50pF	2.2 V/3 V		2.2		MHz
		Noninverting, Medium Mode, R_L =300kΩ, C_L = 50pF			1.4		
		Noninverting, Slow Mode, R_L =300kΩ, C_L = 50pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, noninverting, Gain = 1	2.2 V/3 V		10	20	μs
$t_{en(off)}$	Enable time off		2.2 V/3 V			1	μs

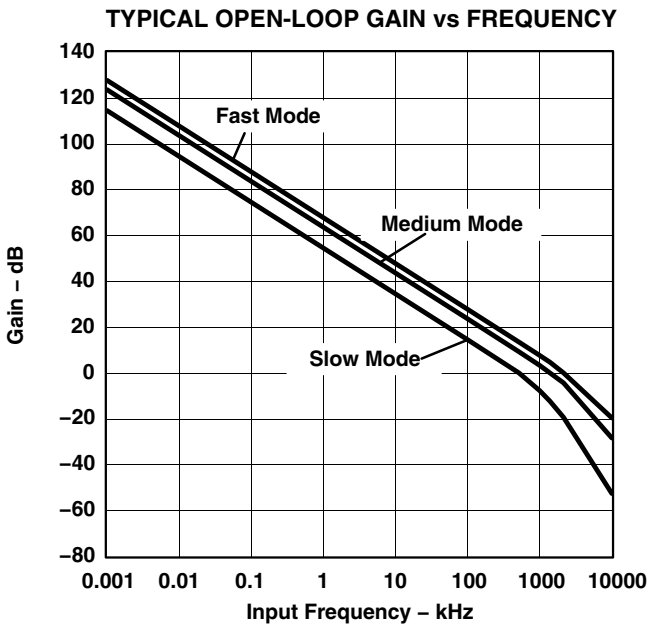


Figure 19

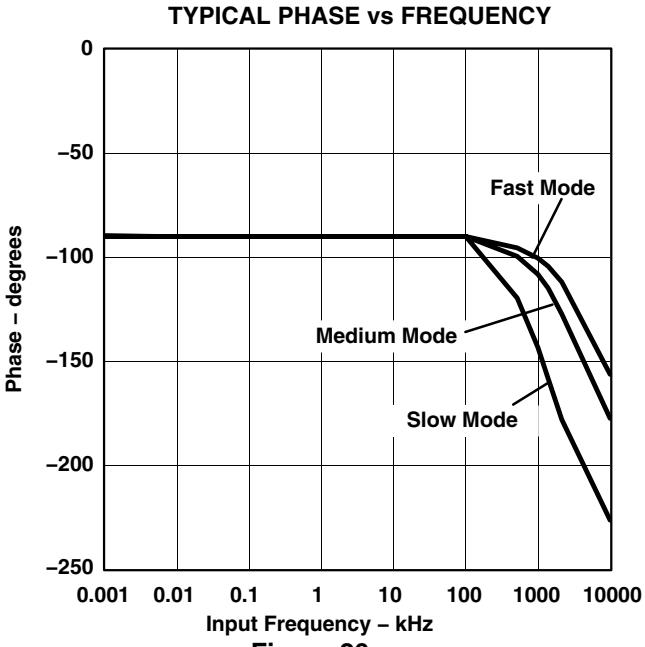


Figure 20

switches to ground

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			2.5		3.6	V
I_{lkg}	Input leakage current (see Note 1)	T_A = –40°C to + 55°C			±1	±10	nA
		T_A = 55°C to 85°C				±50	
I_{IN}	Input current	Input switched to Ground.		0		100	μA
R_{ON}	On resistance	I_{IN}=100 μA, T_A=–40°C to 85°C				10	Ω

NOTES: 1. ESD damage can degrade input current leakage.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.5		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.5V/3.6V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.5V/3.6V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.5V/3.6V			10	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.5V/3.6V	200			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64–byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

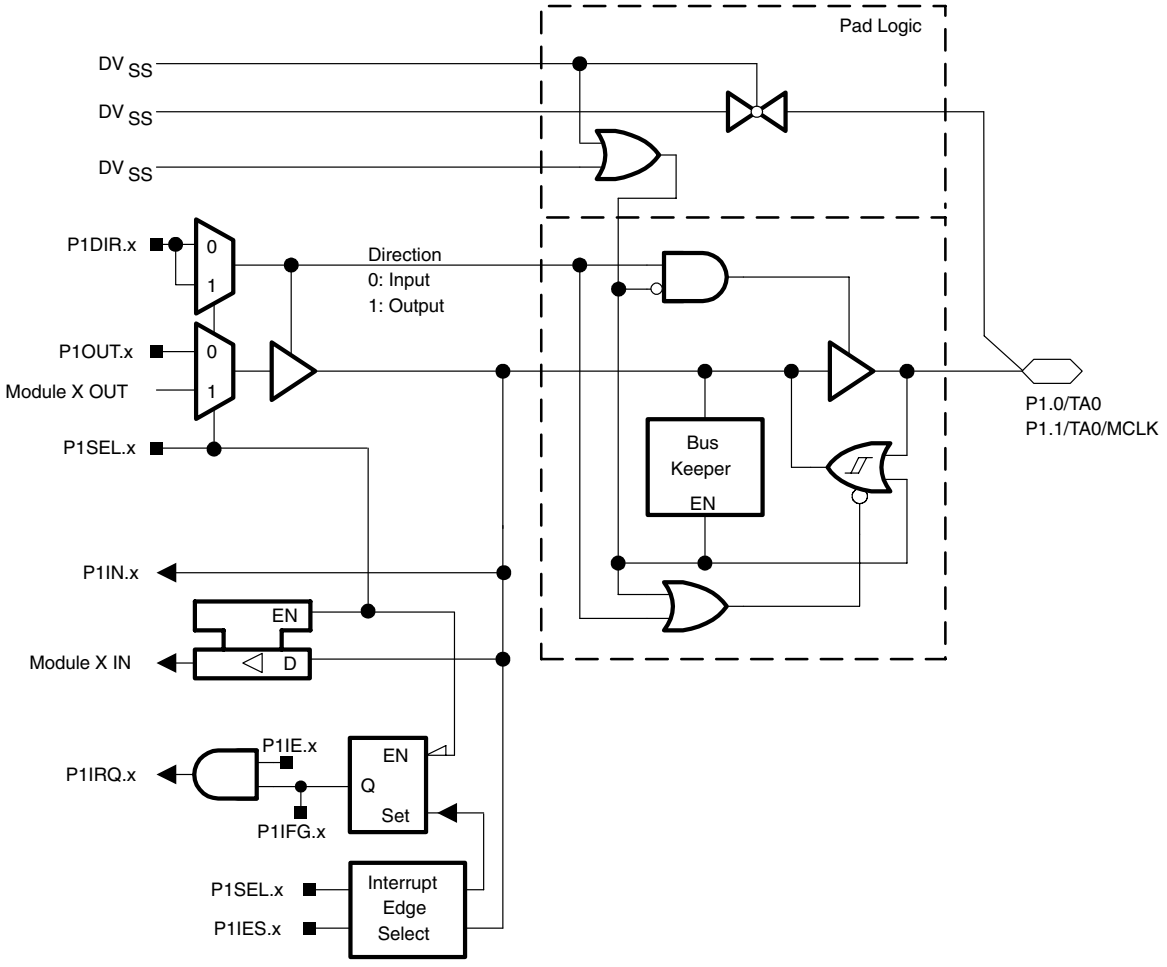
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

input/output schematics

Port P1 pin schematic: P1.0, P1.1, input/output with Schmitt trigger



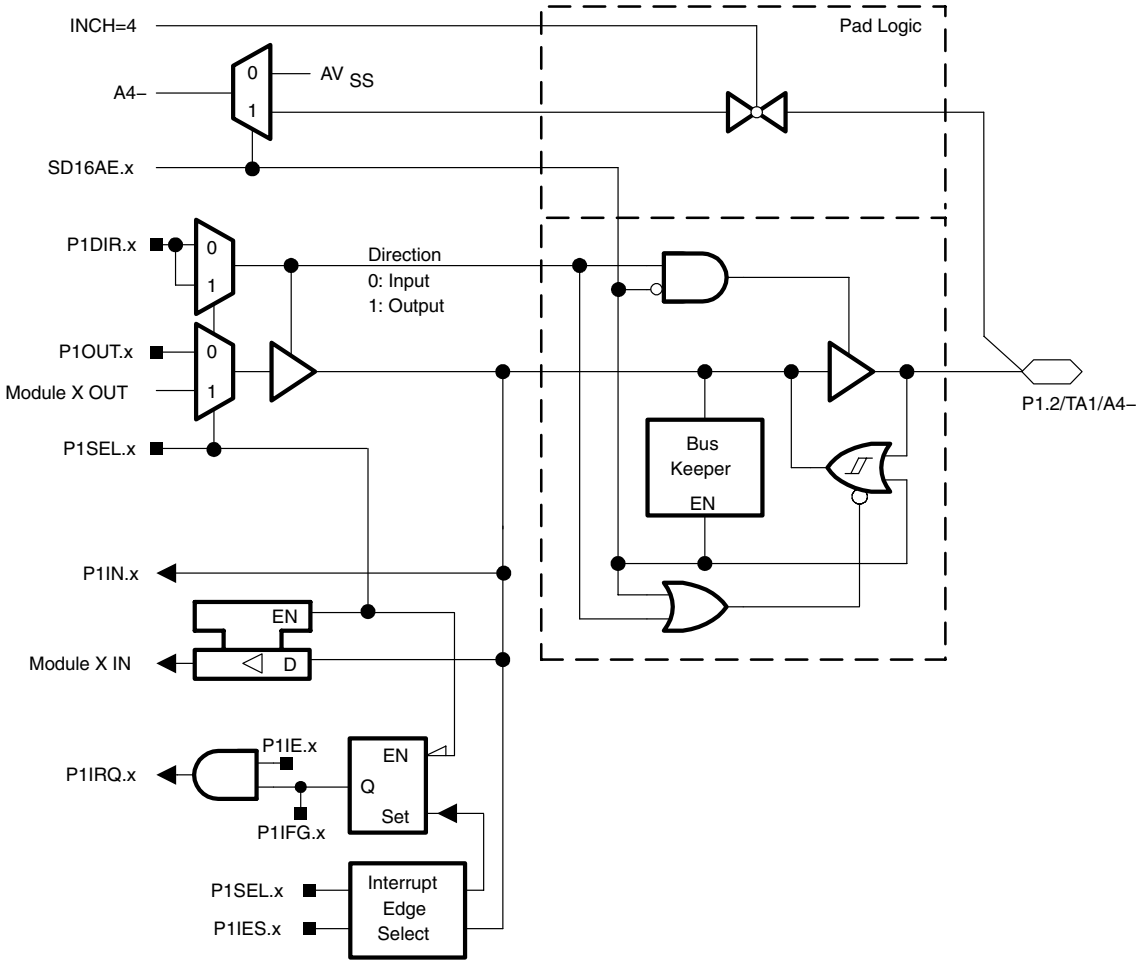
Note: x = 0,1

Port P1 (P1.0, P1.1) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0	0	P1.0† Input/Output	0/1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.1/TA0/MCLK	1	P1.1† Input/Output	0/1	0
		Timer_A3.CCI0B	0	1
		MCLK	1	1

† Default after reset (PUC/POR)
NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

Port P1 pin schematic: P1.2, input/output with Schmitt trigger and analog functions



Note: x = 2

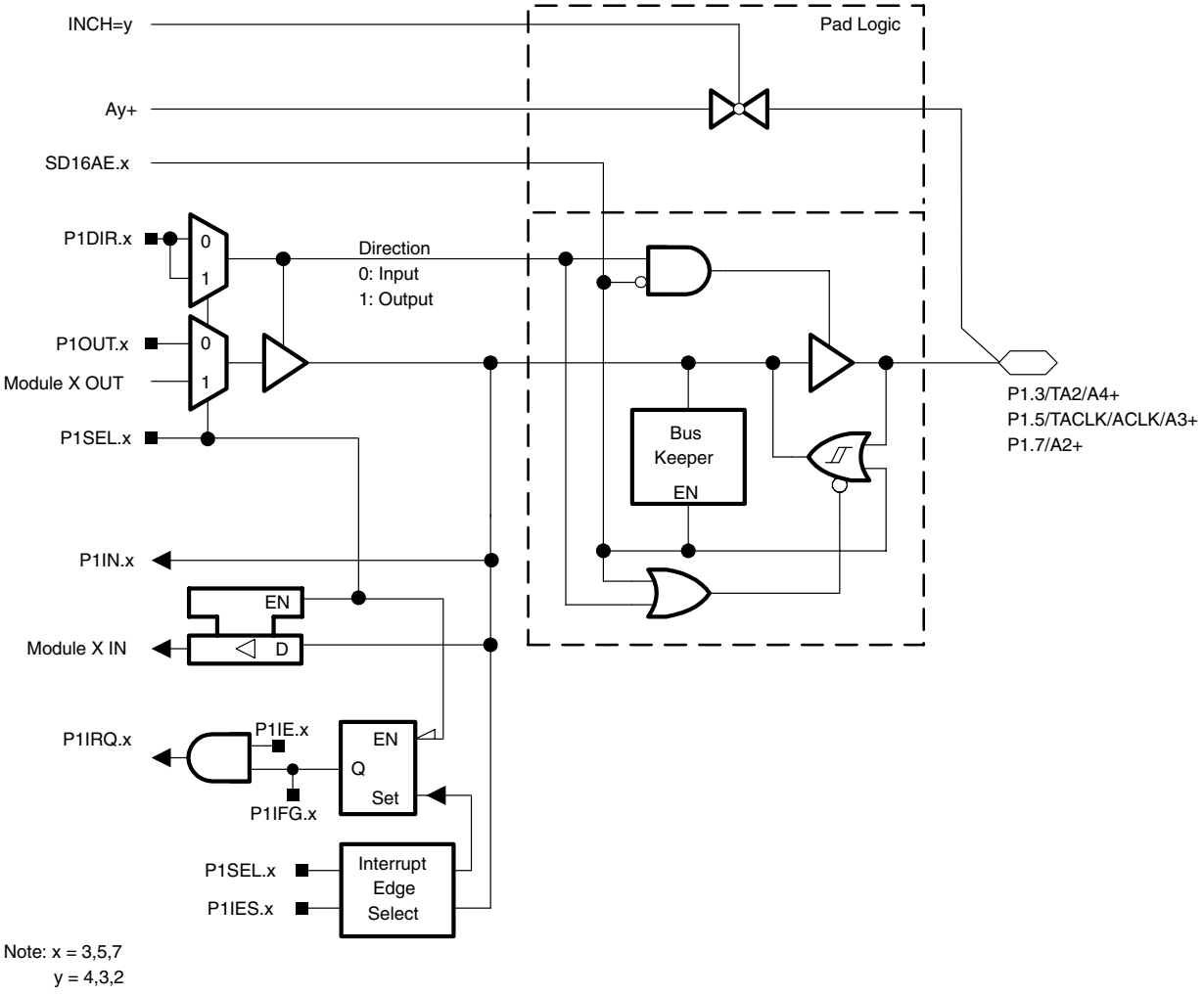
Port P1 (P1.2) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	SD16AE.x
P1.2/TA1/A4–	2	P1.2† Input/Output	0/1	0	0
		Timer_A3.CCI1A	0	1	0
		Timer_A3.TA1	1	1	0
		A4– (see Notes 3, 4)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A4–) connected to V_{SS} if corresponding SD16AE.x bit is cleared.

Port P1 pin schematic: P1.3, P1.5, P1.7, input/output with Schmitt trigger and analog functions



Note: x = 3,5,7
y = 4,3,2

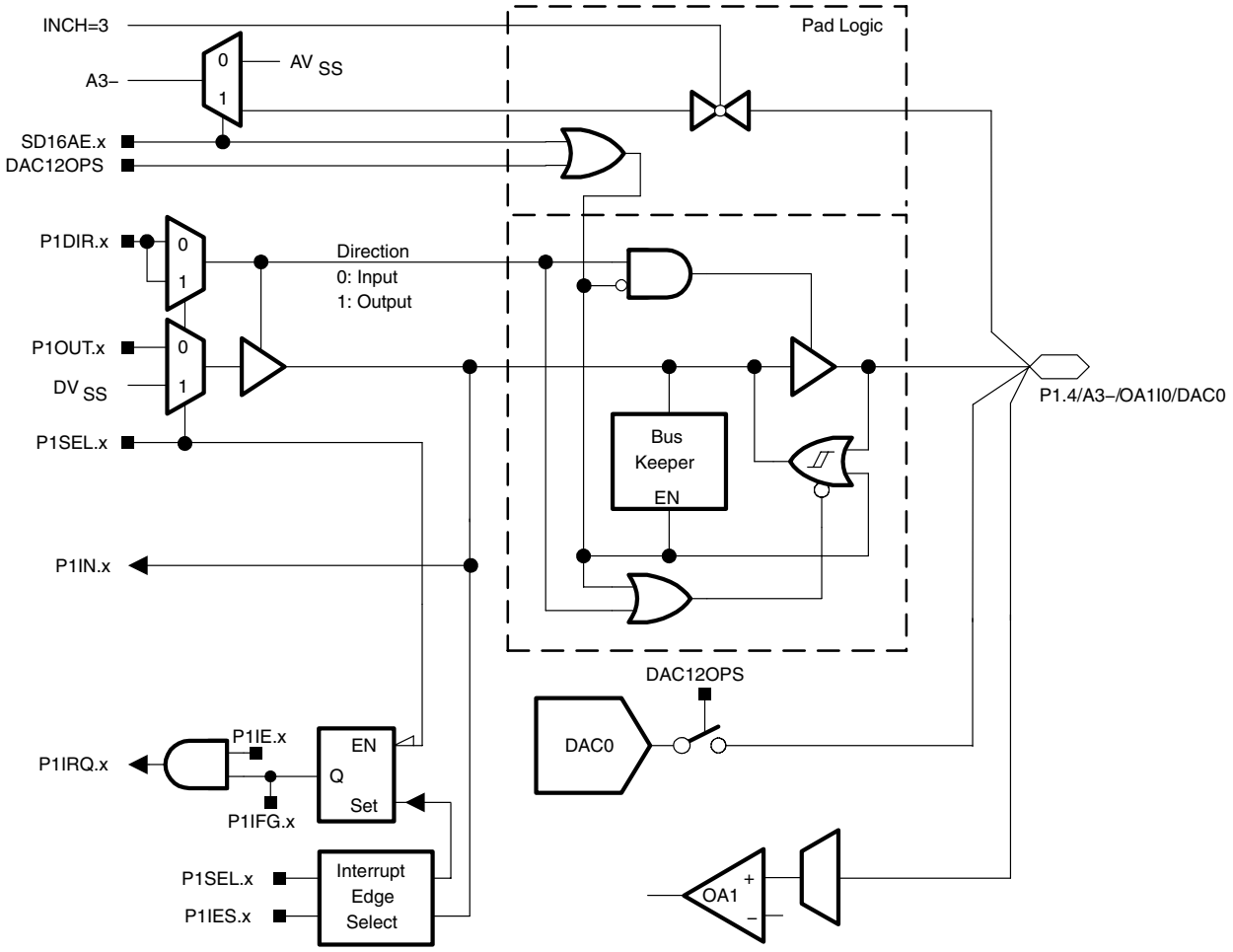
Port P1 (P1.3, P1.5, P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	SD16AE.x
P1.3/TA2/A4+	3	P1.3† Input/Output	0/1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		A4+ (see Note 3)	X	X	1
P1.5/TACLK/ACLK/A3+	5	P1.5† Input/Output	0/1	0	0
		Timer_A3.TACLK/INCLK	0	1	0
		ACLK	1	1	0
		A3+ (see Note 3)	X	X	1
P1.7/A2+	7	P1.5† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		A2+ (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P1 pin schematic: P1.4, input/output with Schmitt trigger and analog functions



Note: x = 4

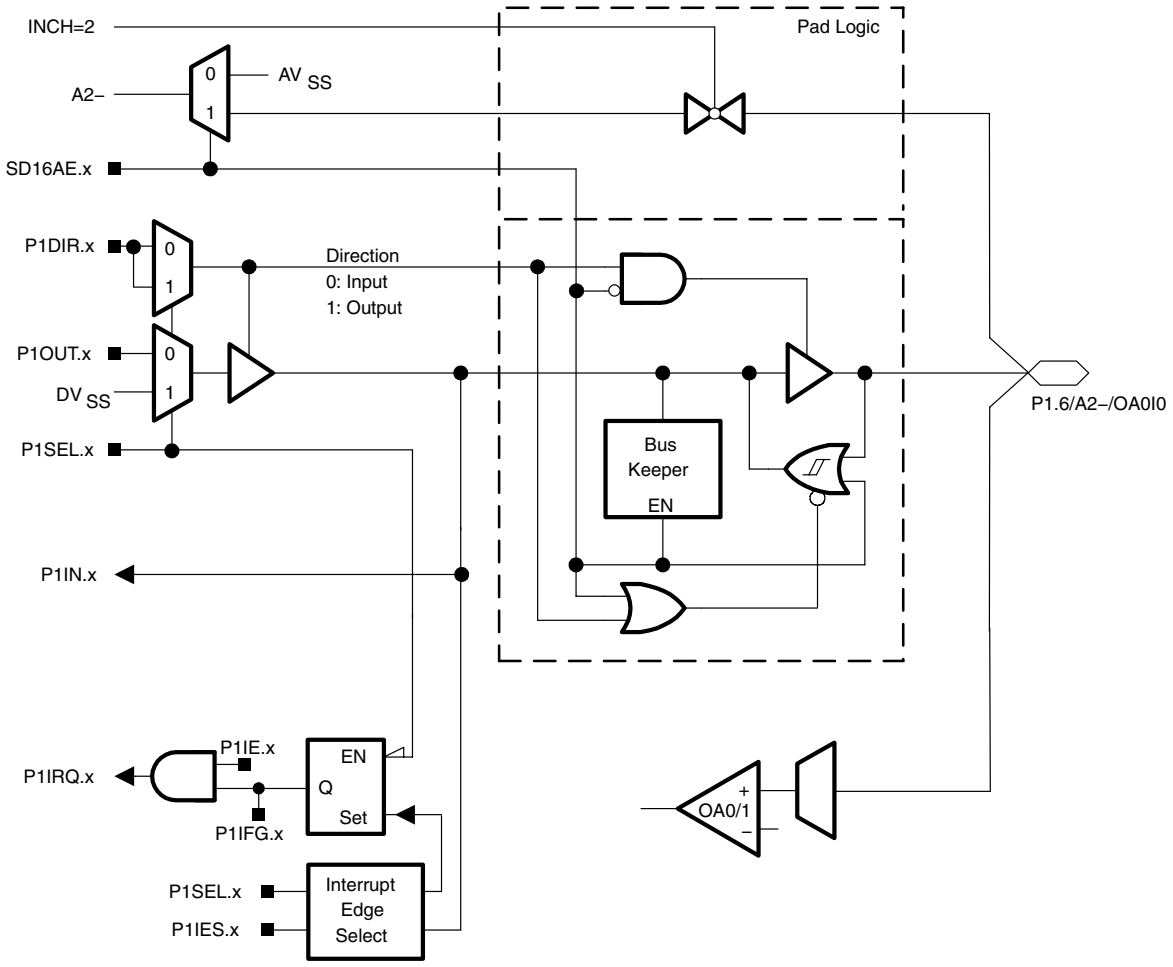
Port P1 (P1.4) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P1DIR.x	P1SEL.x	SD16AE.x	OAPx (OA1)	DAC12OPS
P1.4/A3–/OA1I0/DAC0	4	P1.4† Input/Output	0/1	0	0	XX	0
		N/A	0	1	0	XX	0
		DVSS	1	1	0	XX	0
		A3– (see Notes 3, 4)	X	X	1	XX	0
		OA1I0	X	X	1	00	0
		DAC0 (see Note 5)	X	X	X	XX	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A3–) connected to AV_{SS} if corresponding SD16AE.x bit is cleared.
5. Setting the DAC12OPS bit also disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P1 pin schematic: P1.6, input/output with Schmitt trigger and analog functions



Note: x = 6

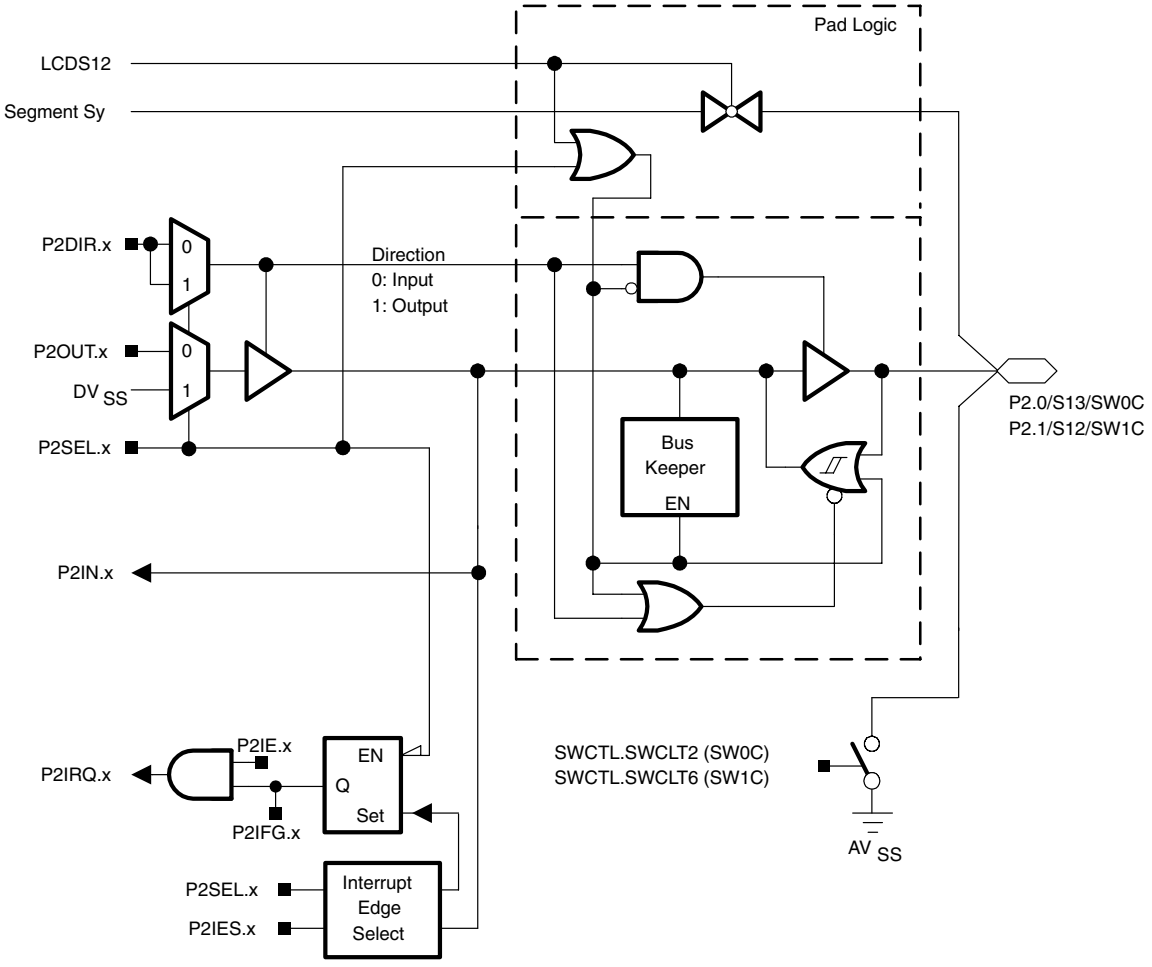
Port P1 (P1.6) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P1DIR.x	P1SEL.x	SD16AE.x	OAPx (OA0)	OAPx (OA1)
P1.6/A2–/OA0I0	6	P1.6† Input/Output	0/1	0	0	XX	XX
		N/A	0	1	0	XX	XX
		DVSS	1	1	0	XX	XX
		A2– (see Notes 3, 4)	X	X	1	XX	XX
		OA0I0 (see Note 5)	X	X	1	00 or 01	XX
			X	X	1	XX	01

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A2–) connected to AV_{SS} if corresponding SD16AE.x bit is cleared.
5. OA0I0 connected to pin if for OA0 the OAPx bits are cleared or set to 01, or if for OA1 the OAPx bits are set to 01.

Port P2 pin schematic: P2.0 to P2.1, input/output with Schmitt trigger, LCD and analog functions



Note: x = 0,1
y = 13,12

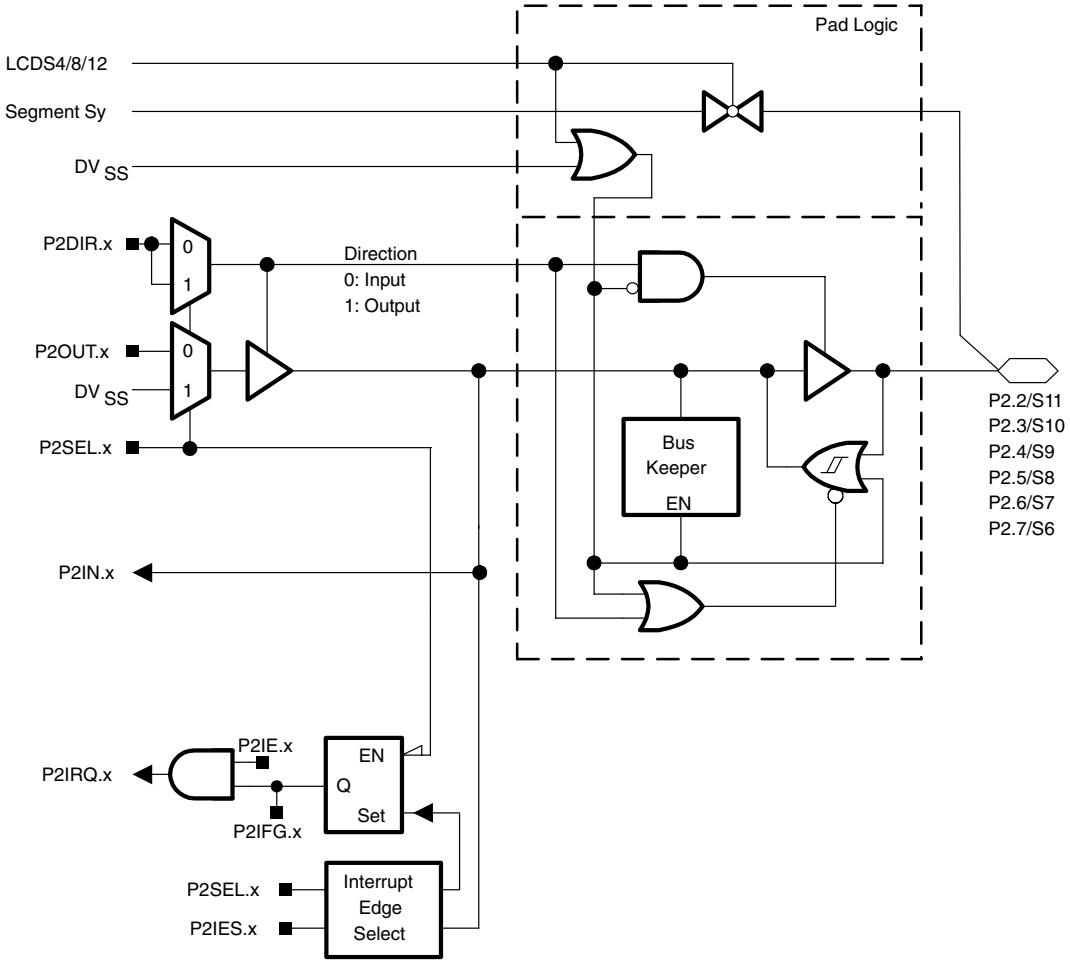
Port P2 (P2.0, P2.1) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS12
P2.0/S13/SW0C	0	P2.0† Input/Output	0/1	0	0
		SW0C (see Notes 3, 4)	X	1	0
		S13	X	X	1
P2.1/S12/SW1C	1	P2.1† Input/Output	0/1	0	0
		SW1C (see Notes 3, 4)	X	1	0
		S12	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the P2SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. The low impedance switch to ground is closed by setting the corresponding bits in SWCTL register.

Port P2 pin schematic: P2.2 to P2.7, input/output with Schmitt trigger, LCD and analog functions



Note: x = 2 to 7
y = 11 to 6

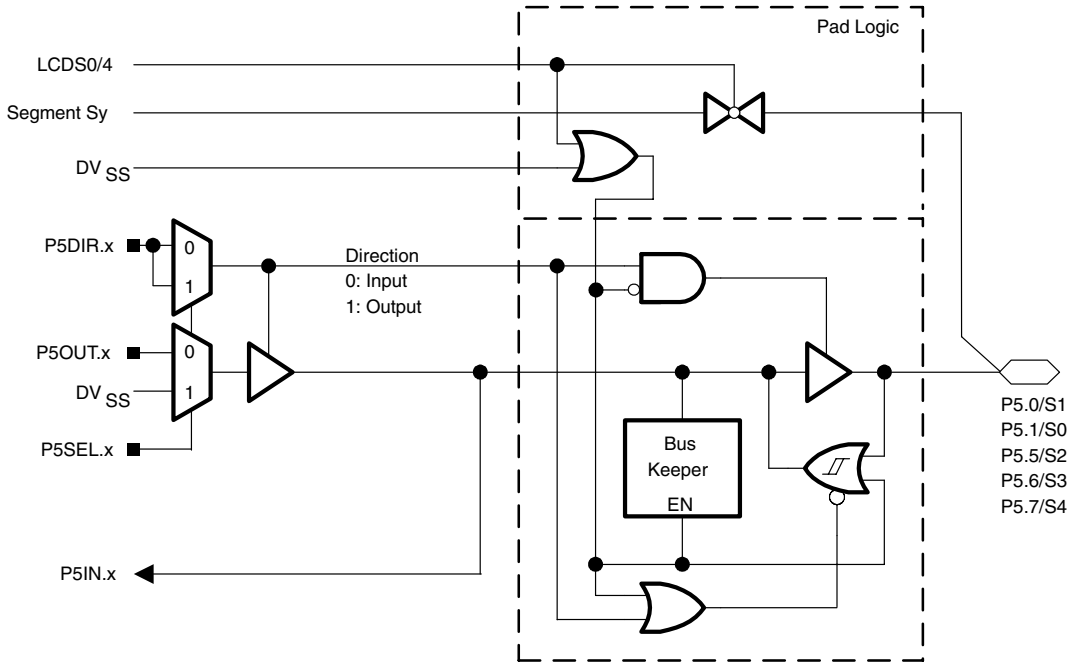
Port P2 (P2.0 to P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS12
P2.2/S11	2	P2.2† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S11	X	X	1
P2.3/S10	3	P2.3† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S10	X	X	1
P2.4/S9	4	P2.4† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S9	X	X	1
P2.5/S8	5	P2.5† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S8	X	X	1
P2.6/S7	6	P2.6† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S7	X	X	1
P2.7/S6	7	P2.7† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S6	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.

Port P5 pin schematic: P5.0, P5.1, P5.5 to P5.7, input/output with Schmitt trigger and LCD functions



Note: x = 0,1,5,6,7
y = 1,0,2,3,4

Port P5 (P5.0, P5.1, P5.5, P5.6) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS0
P5.0/S1	0	P5.0† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S1	X	X	1
P5.1/S0	1	P5.1† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S0	X	X	1
P5.5/S2	5	P5.5† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S2	X	X	1
P5.6/S3	6	P5.6† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S3	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

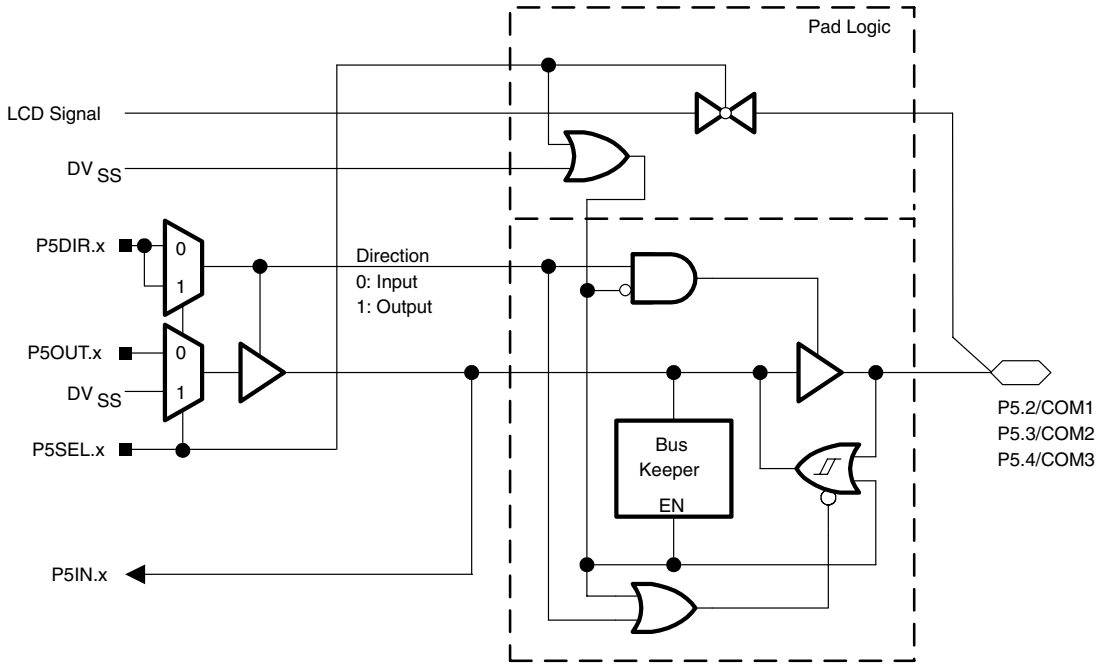
Port P5 (P5.7) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS4
P5.7/S4	7	P5.7† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S4	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

Port P5 pin schematic: P5.2 to P5.4, input/output with Schmitt trigger and LCD functions



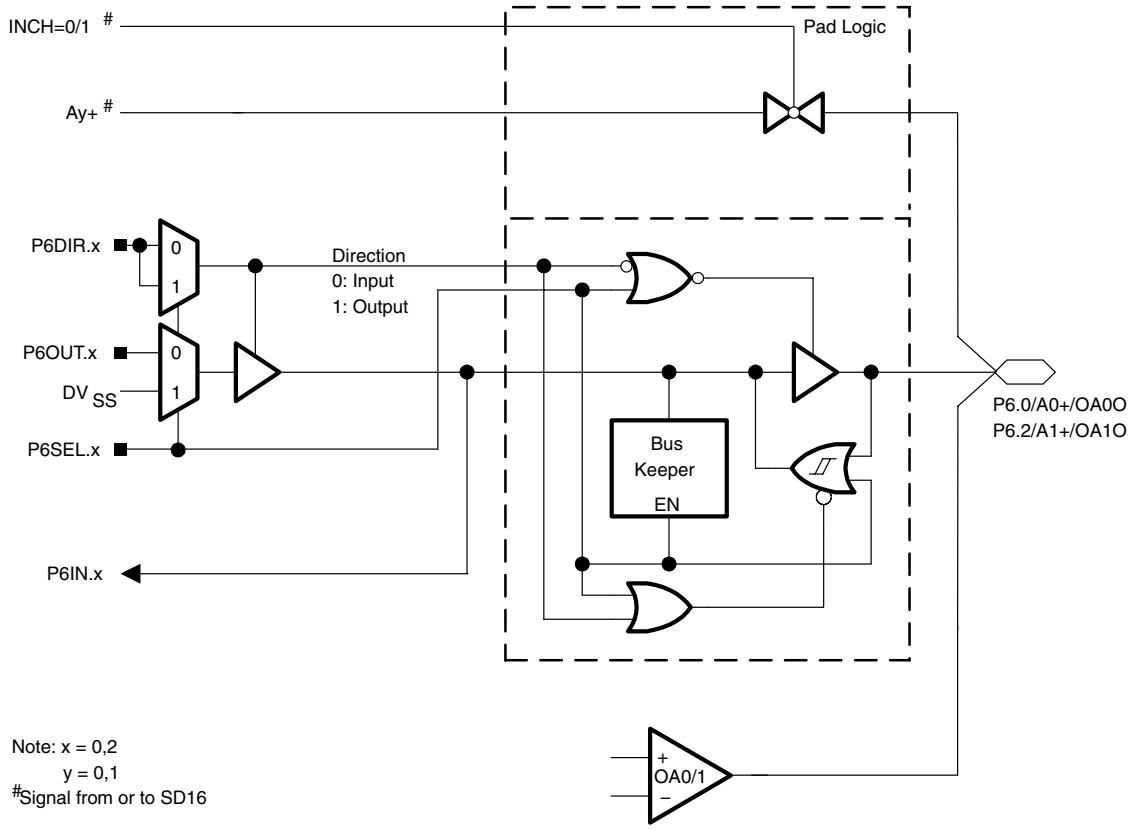
Note: x = 2 to 4

Port P5 (P5.2 to P5.4) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.2† Input/Output	0/1	0
		COM1	X	1
P5.3/COM2	3	P5.3† Input/Output	0/1	0
		COM2	X	1
P5.4/COM3	4	P5.4† Input/Output	0/1	0
		COM3	X	1

† Default after reset (PUC/POR)
NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

Port P6 pin schematic: P6.0, P6.2, input/output with Schmitt trigger and analog functions



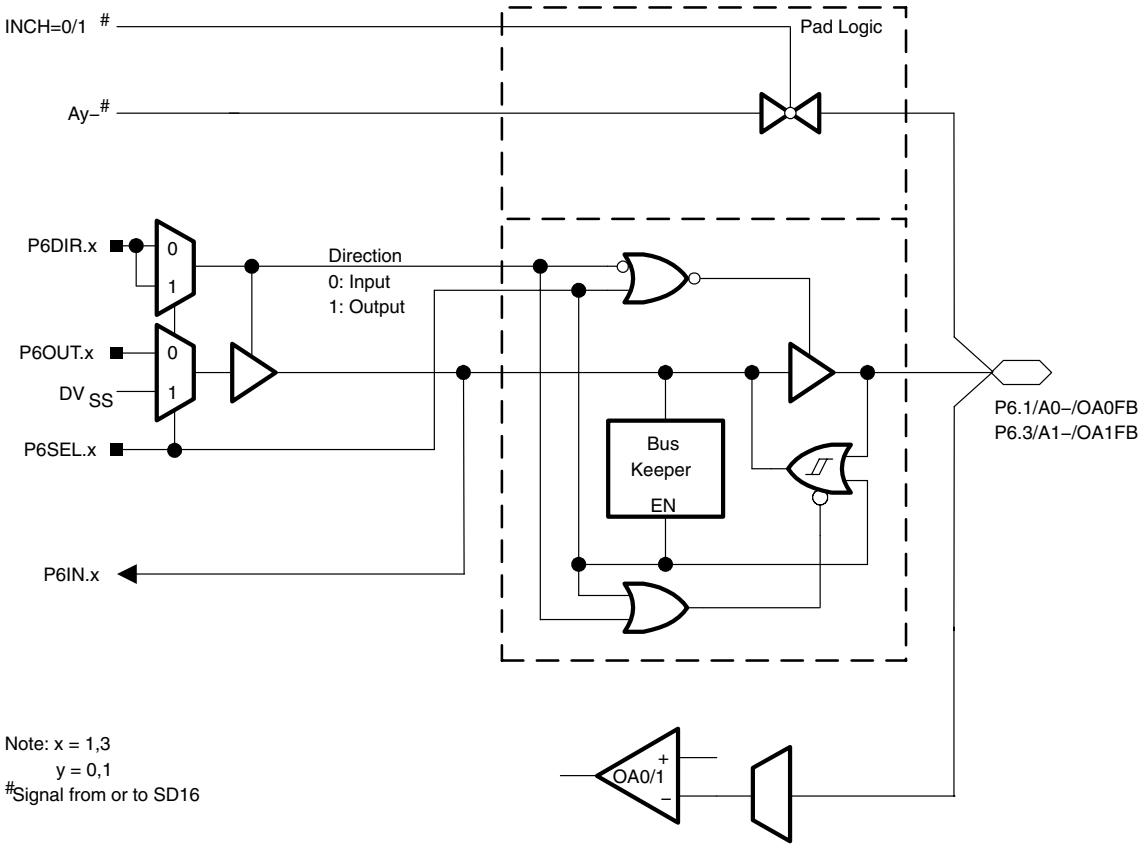
Port P6 (P6.0, P6.2) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.0/A0+/OA0O	0	P6.0† Input/Output	0/1	0
		A0+/OA0O (see Note 3)	X	1
P6.2/A1+/OA1O	2	P6.2† Input/Output	0/1	0
		A1+/OA1O (see Note 3)	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P6 pin schematic: P6.1, P6.3, input/output with Schmitt trigger and analog functions



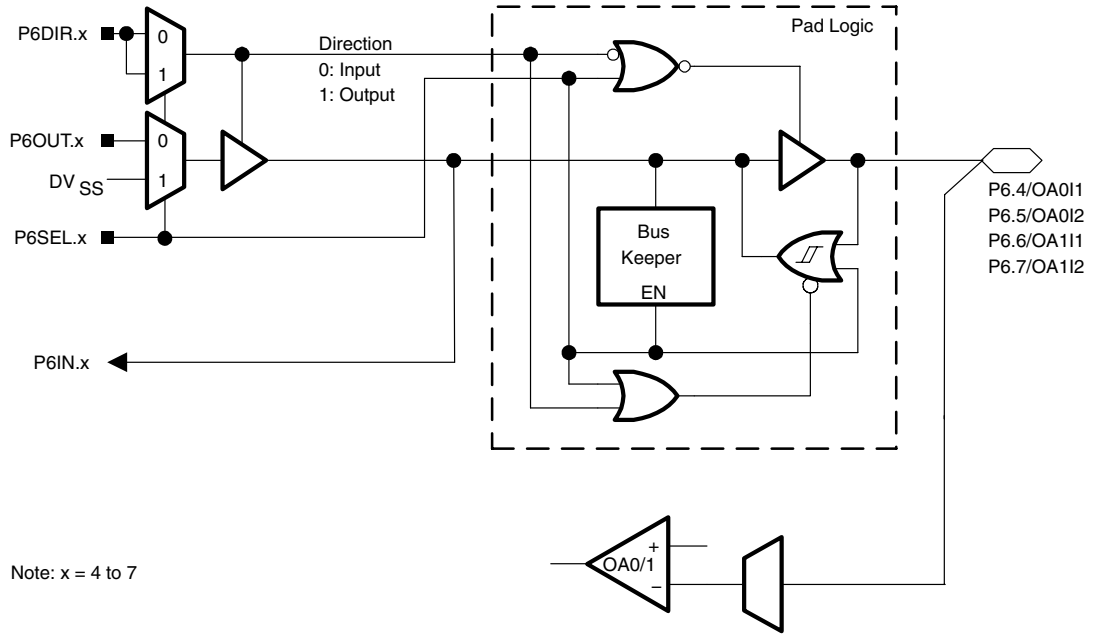
Port P6 (P6.1, P6.3) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.1/A0–/OA0FB	1	P6.1† Input/Output	0/1	0
		A0–/OA0FB (see Note 3)	X	1
P6.3/A1–/OA1FB	3	P6.3† Input/Output	0/1	0
		A1–/OA1FB (see Note 3)	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P6 pin schematic: P6.4 to P6.7, input/output with Schmitt trigger and analog functions



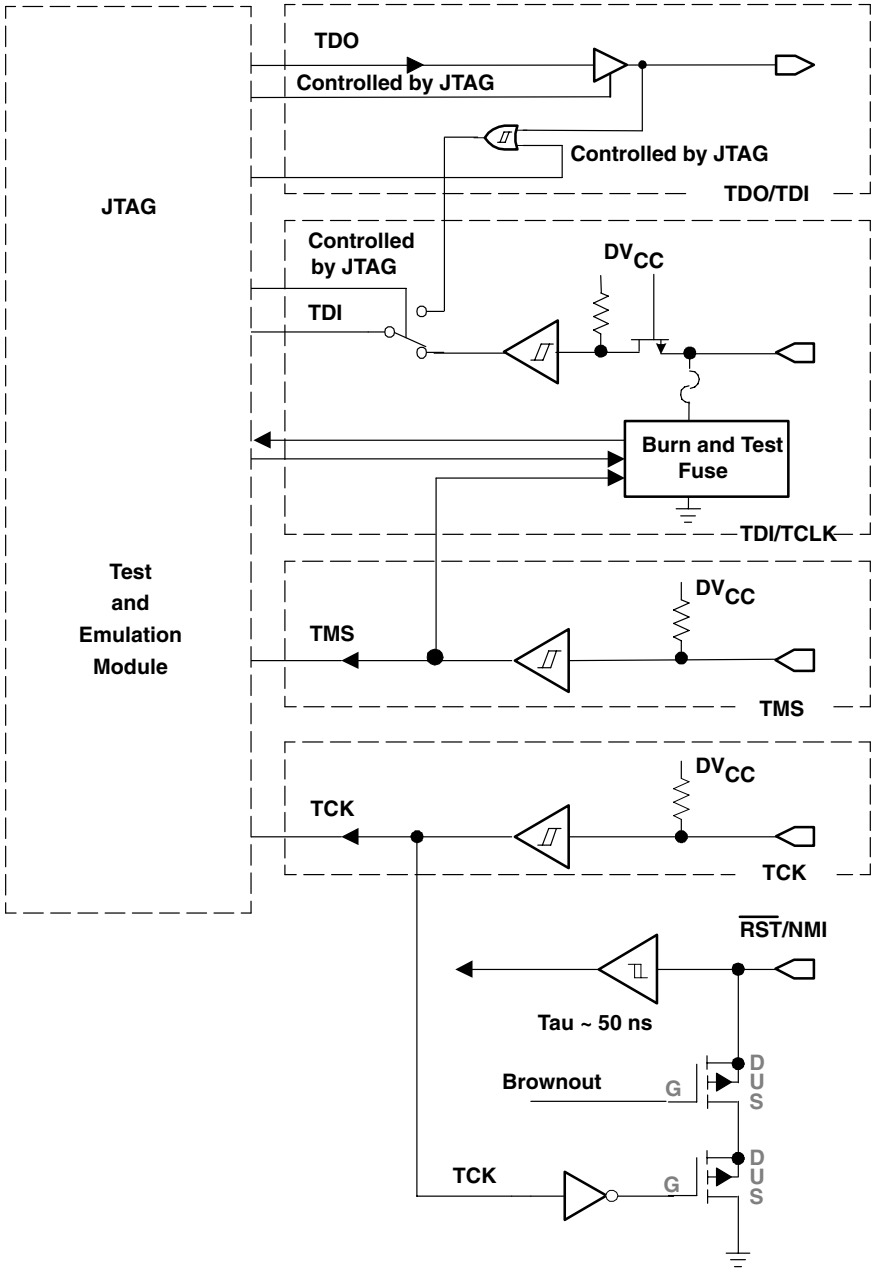
Port P6 (P6.4 to P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.4/OA0I1	4	P6.4† Input/Output	0/1	0
		OA0I1 (see Note 3)	X	1
P6.5/OA0I2	5	P6.5† Input/Output	0/1	0
		OA0I2 (see Note 3)	X	1
P6.6/OA1I1	6	P6.6† Input/Output	0/1	0
		OA1I1 (see Note 3)	X	1
P6.7/OA1I2	7	P6.7† Input/Output	0/1	0
		OA1I2 (see Note 3)	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger or output



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 21). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

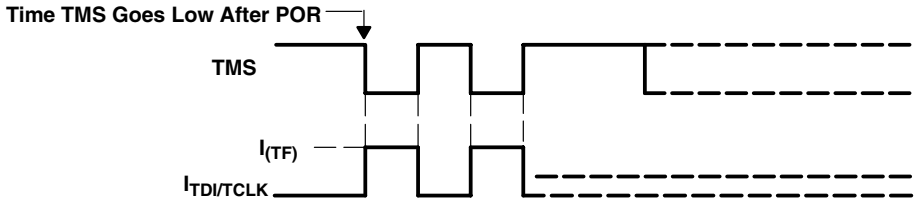


Figure 21. Fuse Check Mode Current

Data Sheet Revision History

Literature Number	Summary
SLAS556	Product Preview data sheet release
SLAS556A	Production Data data sheet release

NOTE: Page and figure numbers refer to the respective document revision.

Corrections to MSP430FG42x0 Data Sheet (SLAS556A)

Document Being Updated: *MSP430FG42x0 Mixed Signal Microcontroller*

Literature Number Being Updated: SLAS556A

Page	Change or Add
48	At the top left of the image, *LCDS4/8/12* should be changed to **LCDS4, LCDS8**.
49	The table includes *LCDS12* in the "CONTROL BITS / SIGNALS" column. For P2.2/S11, P2.3/S10, P2.4/S9, and P2.5/S8, the correct control bit is **LCDS8**. For P2.6/S7 and P2.7/S6, the correct control bit is **LCDS4**.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FG4250IDL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FG4250	Samples
MSP430FG4250IDLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FG4250	Samples
MSP430FG4250IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FG4250	Samples
MSP430FG4250IRGZT	NRND	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FG4250	
MSP430FG4260IDLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FG4260	Samples
MSP430FG4260IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FG4260	Samples
MSP430FG4270IDL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FG4270	Samples
MSP430FG4270IDLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430FG4270	Samples
MSP430FG4270IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FG4270	Samples
MSP430FG4270IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 FG4270	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

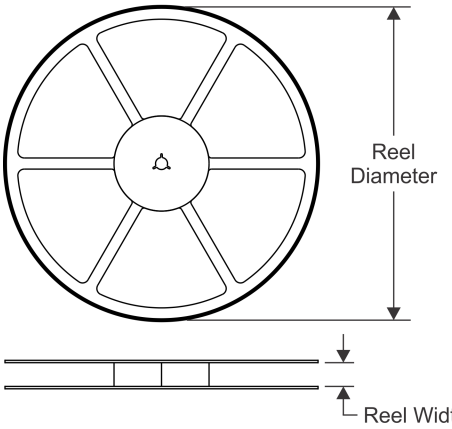
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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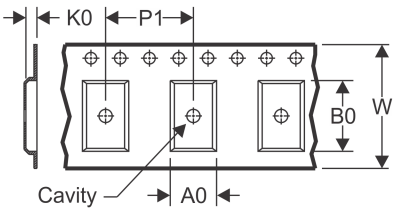
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

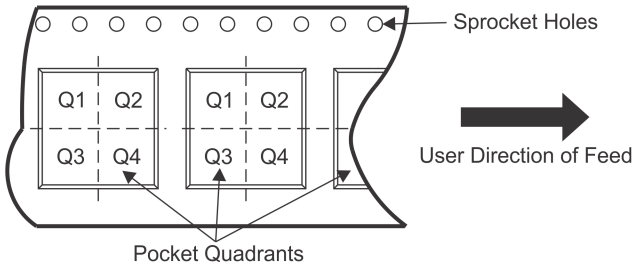


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

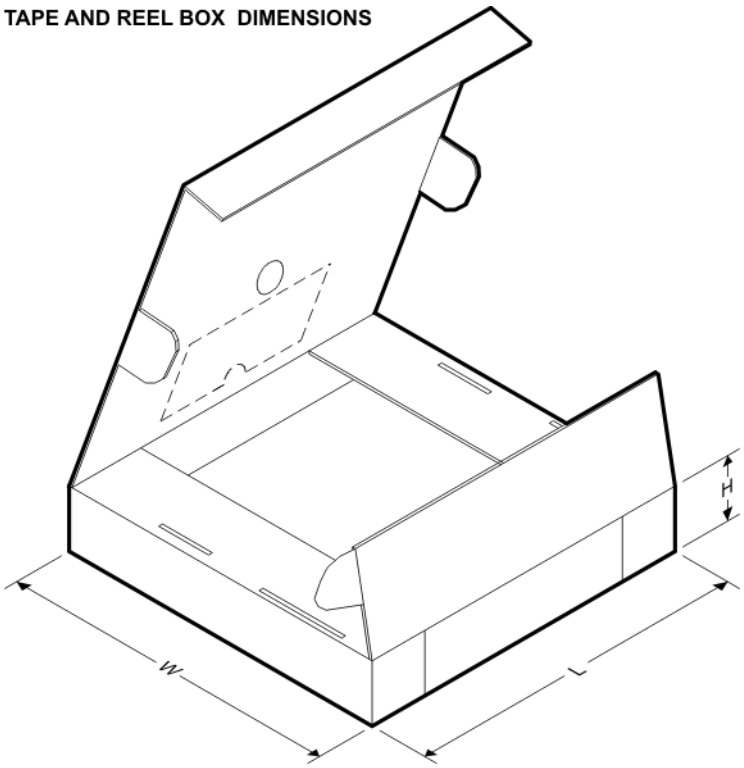
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FG4250IDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
MSP430FG4250IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430FG4260IDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
MSP430FG4260IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430FG4270IDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
MSP430FG4270IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

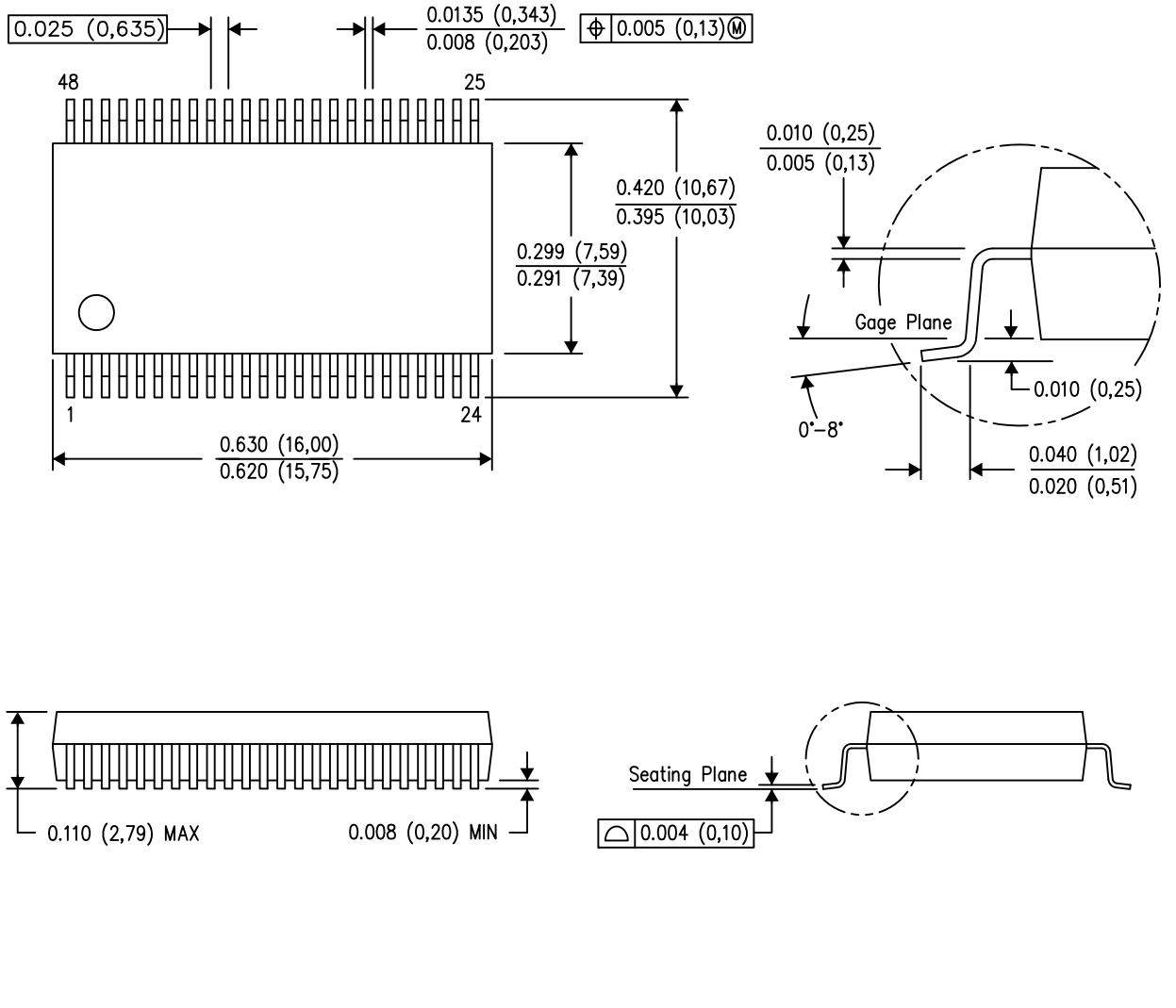
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FG4250IDLR	SSOP	DL	48	1000	367.0	367.0	55.0
MSP430FG4250IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430FG4260IDLR	SSOP	DL	48	1000	367.0	367.0	55.0
MSP430FG4260IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430FG4270IDLR	SSOP	DL	48	1000	367.0	367.0	55.0
MSP430FG4270IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

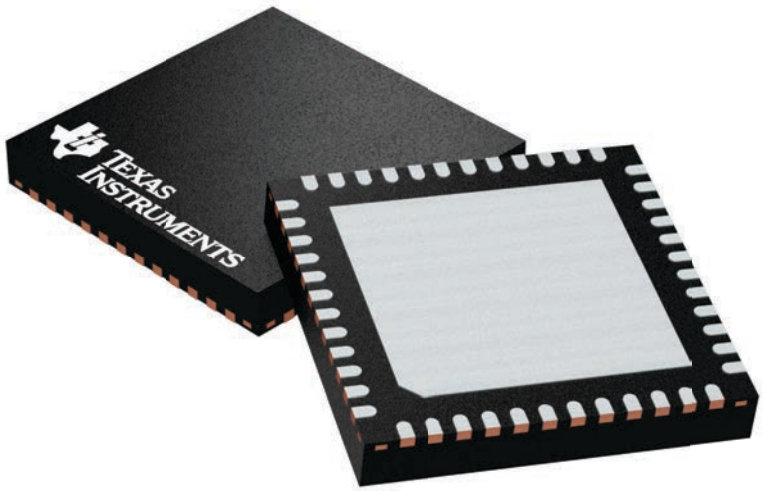
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

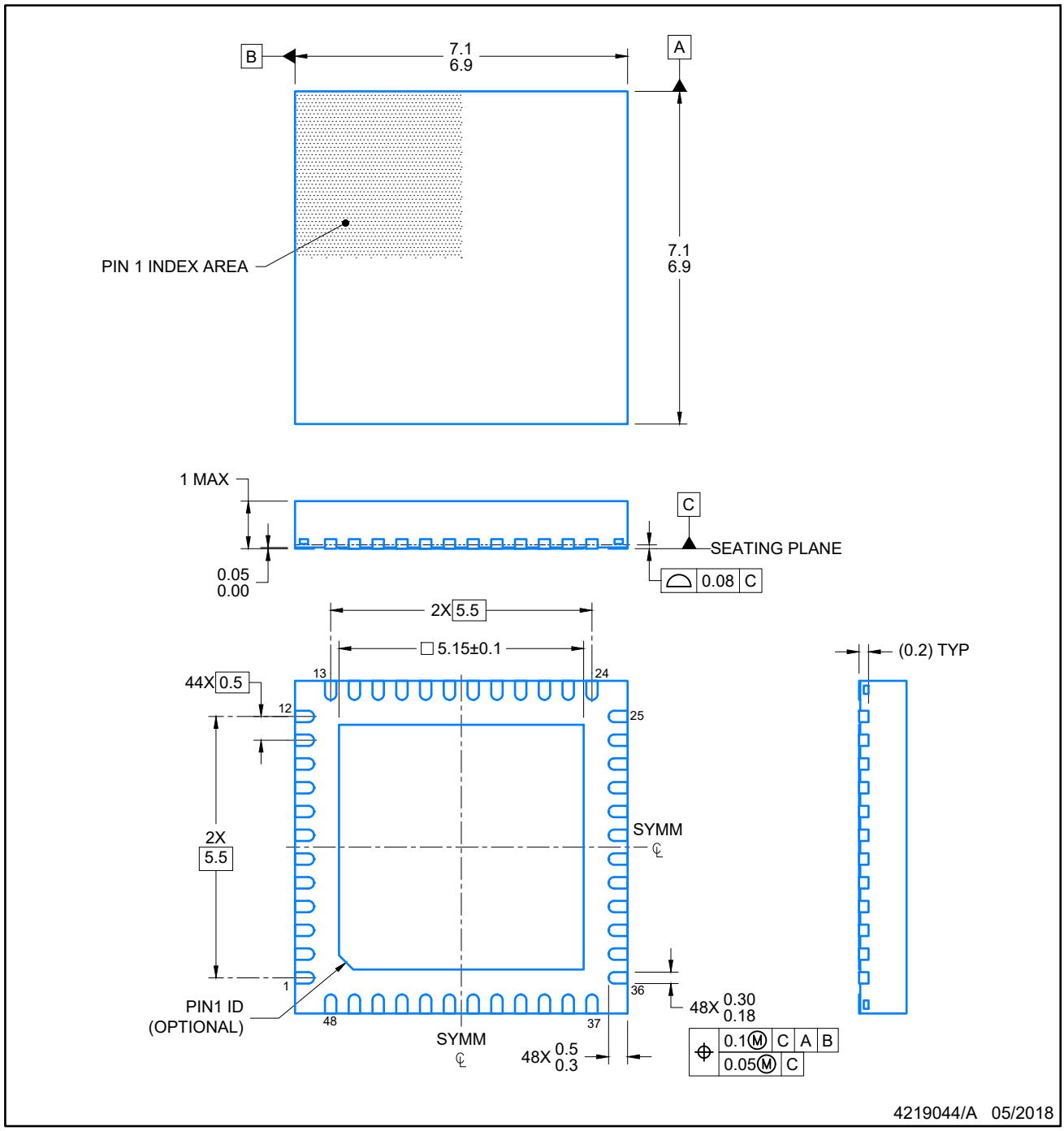
4224671/A

PACKAGE OUTLINE

RGZ0048A

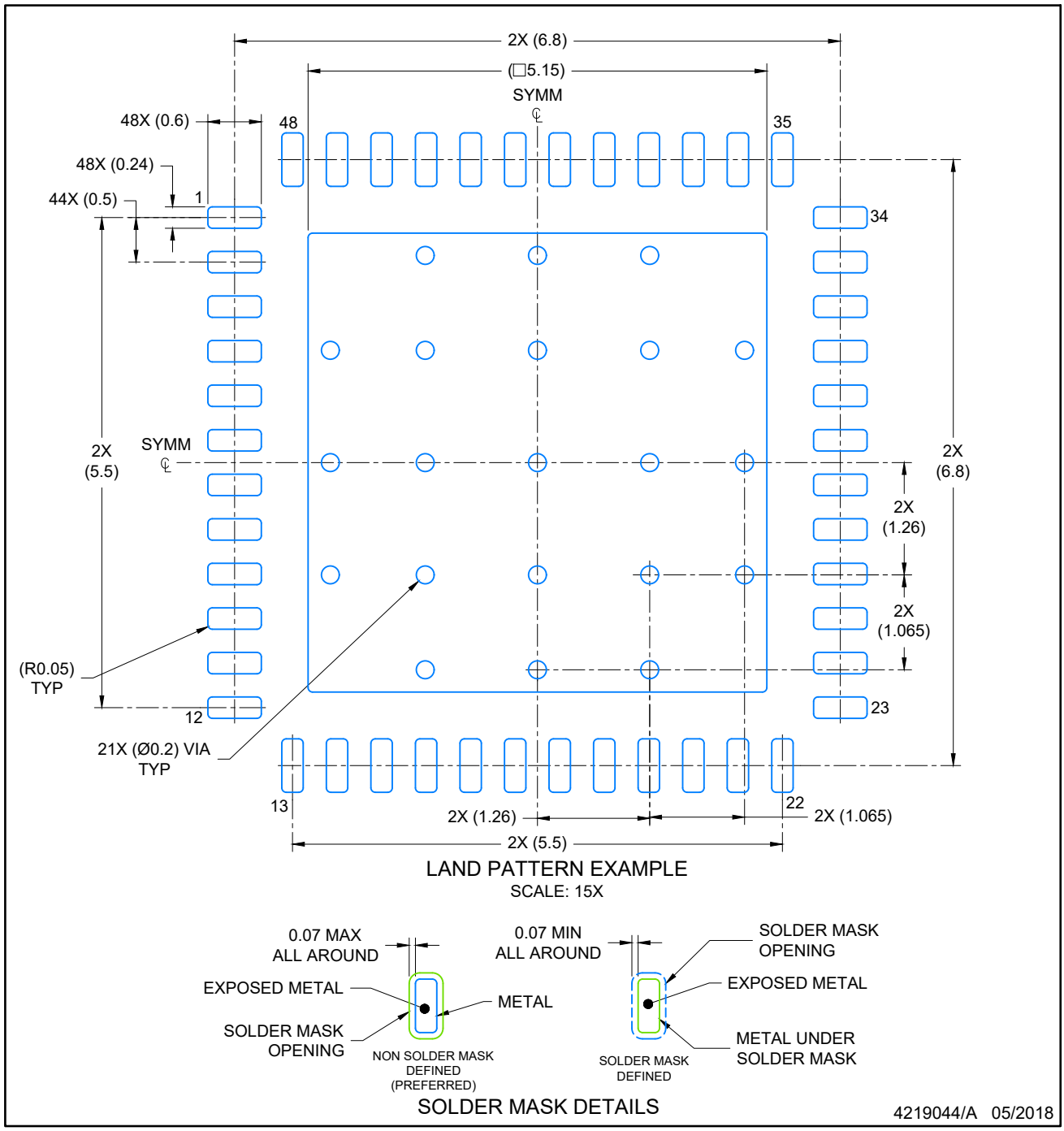
VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



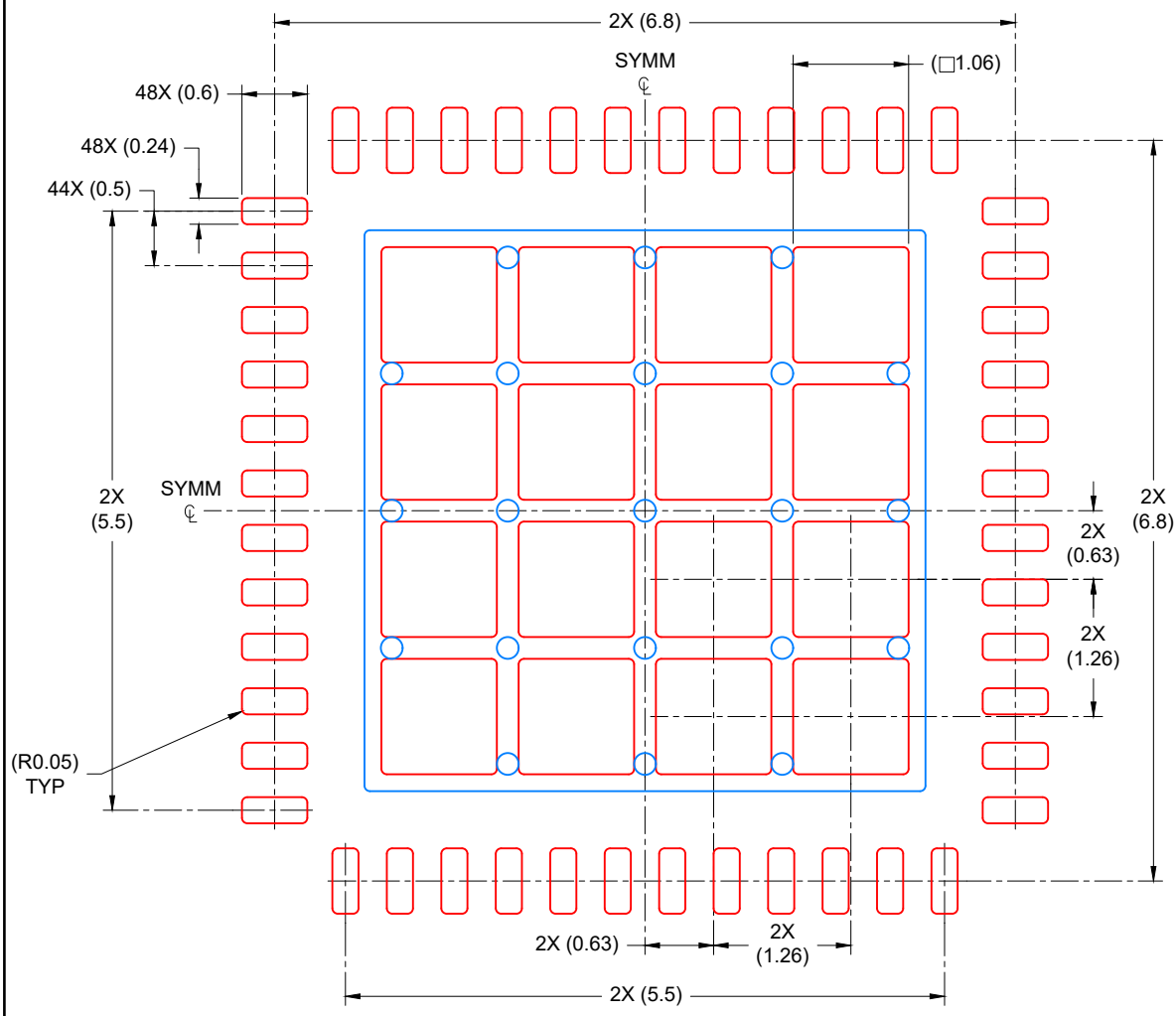
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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