SLAS580D – OCTOBER 2008 – REVISED MARCH 2011

- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption:**
  Active Mode: 262 μA at 1 MHz, 2.2 V
  Standby Mode: 1.1 μA
  Off Mode (RAM Retention): 0.1 μA
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Sigma-Delta Analog-to-Digital (A/D) Converter With Internal Reference and Five Differential Analog Inputs**
- **Dual 12-Bit Digital-to-Analog (D/A) Converter**
- **Dual Configurable Operational Amplifiers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers**
- **Two Universal Serial Communication Interfaces (USCI)**
  USCI_A0
  - **Enhanced UART Supporting Auto-Baudrate Detection**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**

  USCI_B0
  - **I²C™**
  - **Synchronous SPI**
- **Integrated LCD Driver With Contrast Control for Up to 128 Segments**
- **Brownout Detector**
- **Basic Timer With Real-Time Clock Feature**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **On-Chip Comparator**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On-Chip Emulation Module**
- **MSP430FG47x Family Members Include**
  MSP430FG477: 32KB+256B Flash Memory, 2KB RAM
  MSP430FG478: 48KB+256B Flash Memory, 2KB RAM
  MSP430FG479: 60KB+256B Flash Memory, 2KB RAM
- **Available in 113-Ball BGA (ZQW) and 80-Pin QFP (PN) Packages (see Available Options)**
- **For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430FG47x is a microcontroller configuration with two 16-bit timers, a basic timer with a real-time clock, a high performance 16-bit sigma-delta A/D converter, dual 12-bit D/A converters, two configurable operational amplifiers, two universal serial communication interface, 48 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS†

T_A	PACKAGED DEVICES‡	
	PLASTIC 113-BALL BGA (ZQW)	PLASTIC 80-PIN QFP (PN)
–40°C to 85°C	MSP430FG477IZQW MSP430FG478IZQW MSP430FG479IZQW	MSP430FG477IPN MSP430FG478IPN MSP430FG479IPN

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

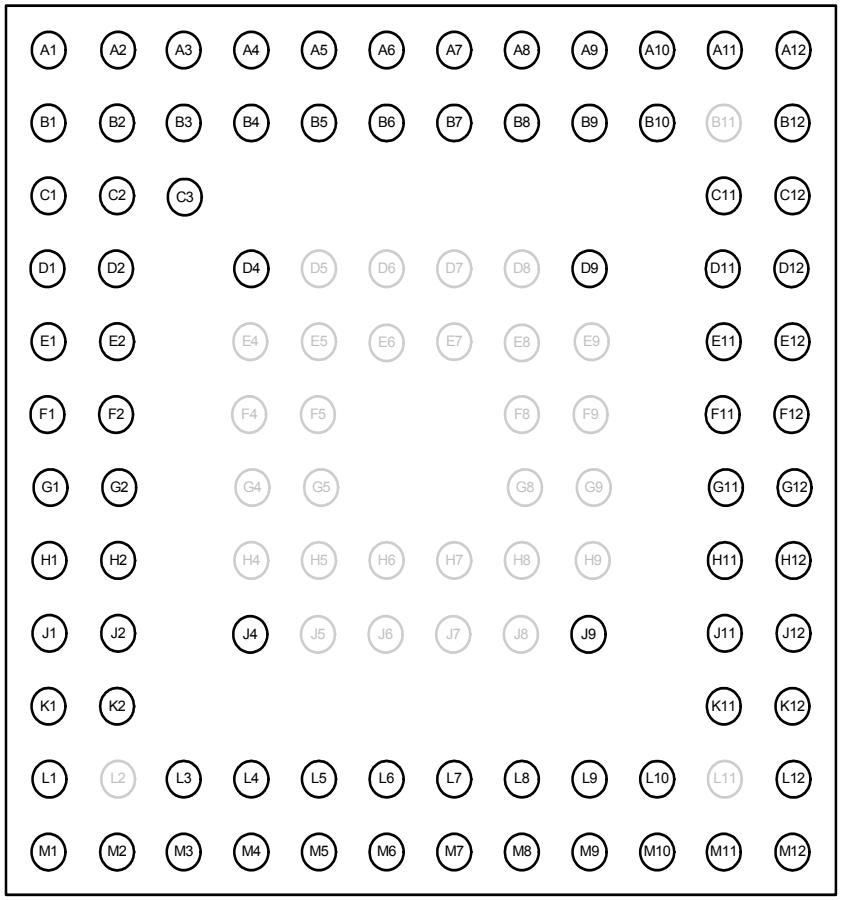
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

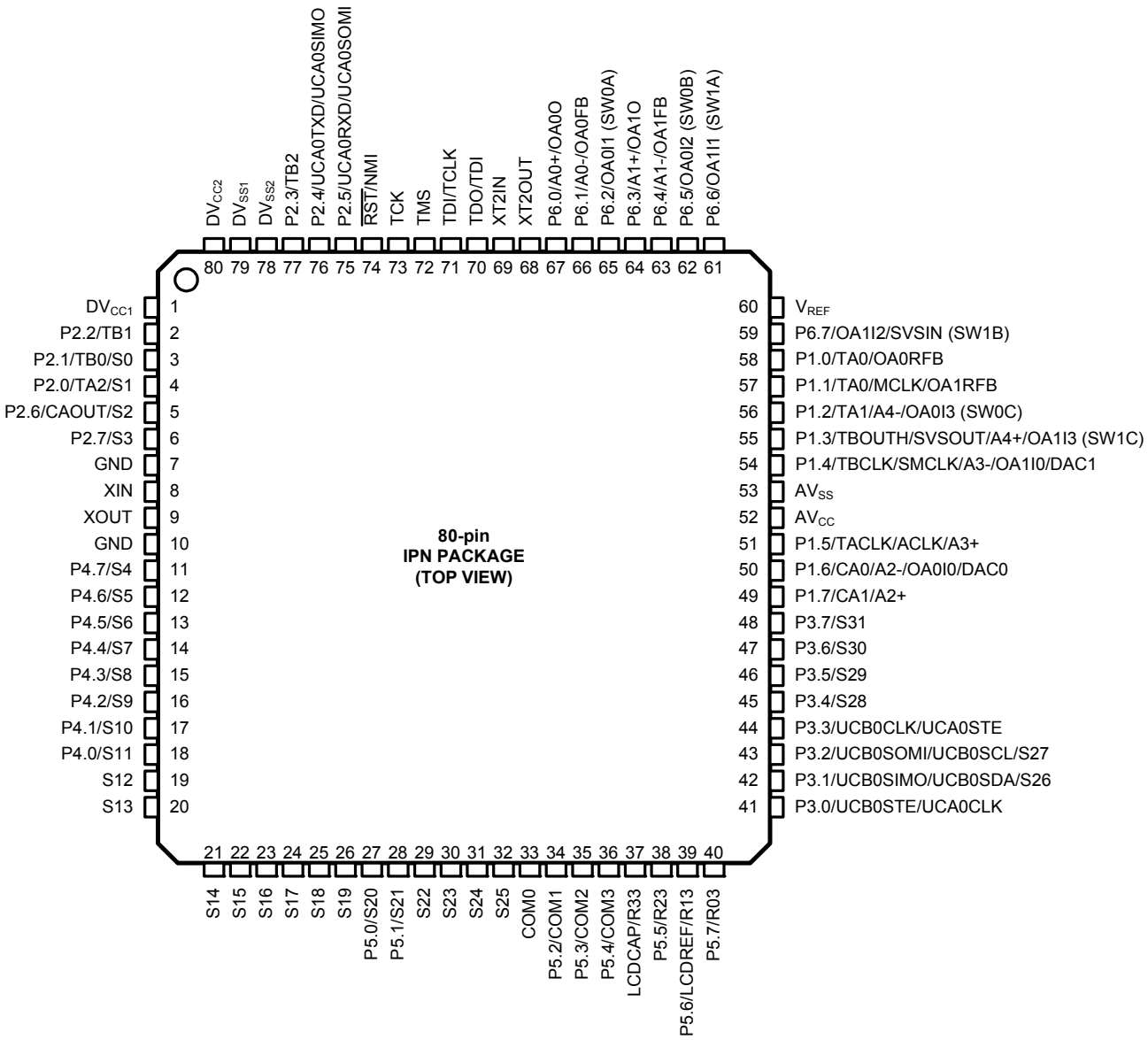
- Debugging and Programming Interface
  - MSP–FET430UIF (USB)
  - MSP–FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP–FET430U80 (PN package)
- Production Programmer
  - MSP–GANG430

pin designation, MSP430FG47xIZQW

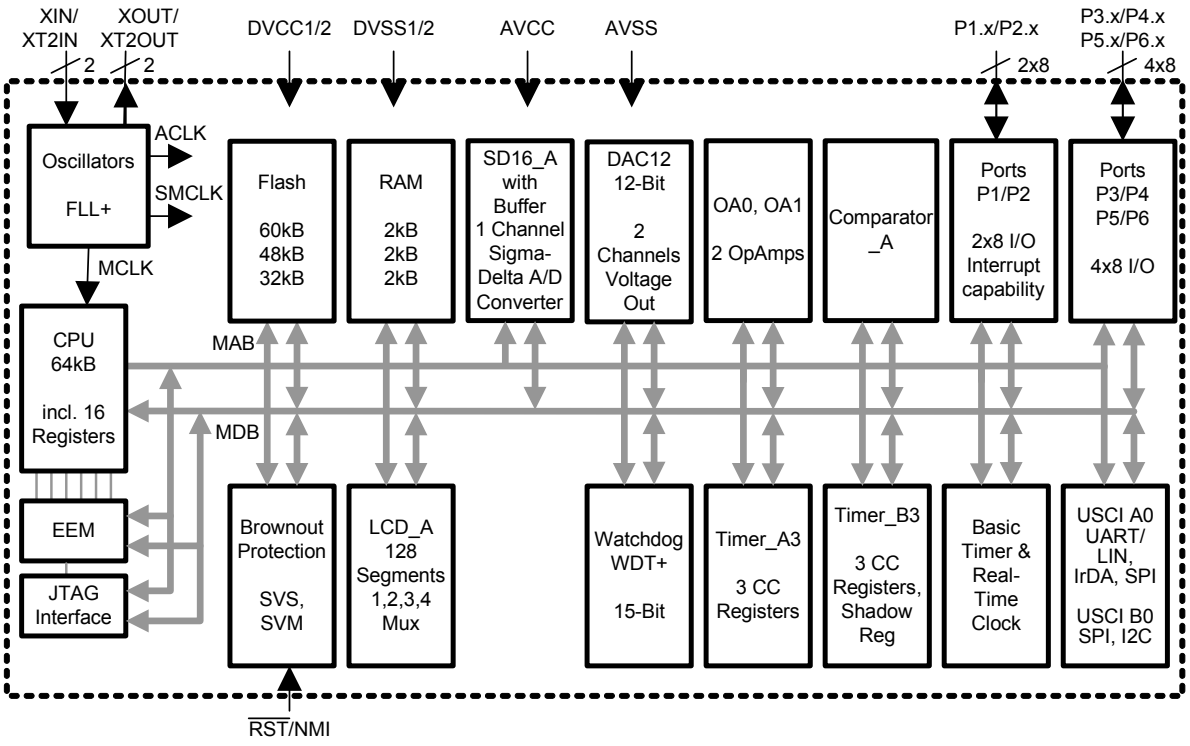


Note: For terminal assignments, see the *MSP430xG47x Terminal Functions* table.

pin designation, MSP430FG47xIPN



functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
AV_{CC}	52	F12		Analog supply voltage, positive terminal.
AV_{SS}	53	E12		Analog supply voltage, negative terminal.
DV_{CC1}	1	A1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS1}	79	A3		Digital supply voltage, negative terminal. Supplies all digital parts.
DV_{CC2}	80	A2		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS2}	78	B2 B3		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TA0/ OA0RFB	58	C11	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output Range switch to OA0 output BSL transmit
P1.1/TA0/MCLK/ OA1RFB	57	C12	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input, compare: Out0 output MCLK signal output Range switch to OA1 output BSL receive
P1.2/TA1/A4–/ OA0I3 (SW0C)	56	D11	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output SD16 negative analog input A4 OA0, analog input I3
P1.3/TBOUTH/ SVSOUT/A4+/ OA1I3 (SW1C)	55	D12	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output switch all PWM digital output ports to high impedance – Timer_B TB0 to TB2 SVS comparator output SD16 positive analog input A4 OA1, analog input I3
P1.4/TBCLK/ SMCLK/A3–/ OA1I0/DAC1	54	E11	I/O	General-purpose digital I/O pin/ Timer_B, clock signal TBCLK input SMCLK signal output SD16 negative analog input A3 OA1, analog input I0 DAC12.1 output
P1.5/TACLK/ ACLK/A3+	51	F11	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal output SD16 positive analog input A3
P1.6/CA0/A2–/ OA0I0/DAC0	50	G12	I/O	General-purpose digital I/O pin Comparator_A input 0 SD16 negative analog input A2 OA0, analog input I0 DAC12.0 output
P1.7/CA1/A2+	49	G11	I/O	General-purpose digital I/O pin Comparator_A input 1 SD16 positive analog input A2
P2.0/TA2/S1	4	C2 C3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A/B input, compare: Out2 output LCD segment output 1
P2.1/TB0/S0	3	C1	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A/B input, compare: Out0 output LCD segment output 0

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
P2.2/TB1	2	B1	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A/B input, compare: Out1 output
P2.3/TB2	77	B4	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A/B input, compare: Out2 output
P2.4/UCA0TXD/ UCA0SIMO	76	A4	I/O	General-purpose digital I/O pin USCIA transmit data output in UART mode, slave data in/master out in SPI mode
P2.5/UCA0RXD/ UCA0SOMI	75	D4	I/O	General-purpose digital I/O pin USCI A0 receive data input in UART mode, slave data out/master in in SPI mode
P2.6/CAOUT/S2	5	D1	I/O	General-purpose digital I/O pin Comparator_A output LCD segment output 2
P2.7/S3	6	D2	I/O	General-purpose digital I/O pin LCD segment output 3
P3.0/UCB0STE/ UCA0CLK	41	M12	I/O	General-purpose digital I/O pin USCI B0 slave transmit enable/USCI A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA/S26	42	L12	I/O	General-purpose digital I/O pin USCI B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode LCD segment output 26
P3.2/UCB0SOMI/ UCB0SCL/S27	43	K11	I/O	General-purpose digital I/O pin USCI B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode LCD segment output 27
P3.3/UCB0CLK/ UCA0STE	44	K12	I/O	General-purpose digital I/O USCI B0 clock input/output, USCI A0 slave transmit enable
P3.4/S28	45	J11	I/O	General-purpose digital I/O pin LCD segment output 28
P3.5/S29	46	J12	I/O	General-purpose digital I/O pin LCD segment output 29
P3.6/S30	47	H11	I/O	General-purpose digital I/O pin LCD segment output 30
P3.7/S31	48	H12	I/O	General-purpose digital I/O pin LCD segment output 31
P4.0/S11	18	K2	I/O	General-purpose digital I/O pin LCD segment output 11
P4.1/S10	17	K1	I/O	General-purpose digital I/O pin LCD segment output 10
P4.2/S9	16	J2	I/O	General-purpose digital I/O pin LCD segment output 9
P4.3/S8	15	J1	I/O	General-purpose digital I/O pin LCD segment output 8
P4.4/S7	14	H2	I/O	General-purpose digital I/O pin LCD segment output 7
P4.5/S6	13	H1	I/O	General-purpose digital I/O pin LCD segment output 6
P4.6/S5	12	G2	I/O	General-purpose digital I/O pin LCD segment output 5
P4.7/S4	11	G1	I/O	General-purpose digital I/O pin LCD segment output 4

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
COM0	33	L8	O	Common output, COM0–3 are used for LCD backplanes
P5.0/S20	27	L5	I/O	General-purpose digital I/O pin LCD segment output 20
P5.1/S21	28	M5	I/O	General-purpose digital I/O pin LCD segment output 21
P5.2/COM1	34	M8	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.3/COM2	35	L9	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.4/COM3	36	M9	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
LCDCAP/R33	37	J9	I/O	Capacitor connection for LCD charge pump input port of most positive analog LCD level (V4)
P5.5/R23	38	M10	I/O	General-purpose digital I/O pin input port of the second most positive analog LCD level (V3)
P5.6/LCDREF/ R13	39	L10	I/O	General-purpose digital I/O pin External LCD reference voltage input input port of the third most positive analog LCD level (V3 or V2)
P5.7/R03	40	M11	I/O	General-purpose digital I/O pin input port of the fourth most positive analog LCD level (V1)
P6.0/A0+/OA0O	67	B8	I/O	General-purpose digital I/O pin SD16 positive analog input A0 OA0, output
P6.1/A0–/OA0FB	66	B9	I/O	General-purpose digital I/O pin SD16 positive negative input A0 OA0, analog input feedback
P6.2/OA0I1 (SW0A)	65	A9	I/O	General-purpose digital I/O pin OA0, analog input I1
P6.3/A1+/OA1O	64	D9	I/O	General-purpose digital I/O pin SD16 positive analog input A1 OA1, output
P6.4/A1–/OA1FB	63	A10	I/O	General-purpose digital I/O pin SD16 positive negative input A1 OA1, analog input feedback
P6.5/OA0I2 (SW0B)	62	B10	I/O	General-purpose digital I/O pin OA0, analog input I2
P6.6/OA1I1 (SW1A)	61	A11	I/O	General-purpose digital I/O pin OA1, analog input I1
P6.7/OA1I2/ SVSIN (SW1B)	59	B12	I/O	General-purpose digital I/O pin OA1, analog input I2 SVS input
S12	19	L1	O	LCD segment output 12
S13	20	M1	O	LCD segment output 13
S14	21	M2	O	LCD segment output 14
S15	22	M3	O	LCD segment output 15
S16	23	L3	O	LCD segment output 16

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
S17	24	L4	O	LCD segment output 17
S18	25	M4	O	LCD segment output 18
S19	26	J4	O	LCD segment output 19
S22	29	L6	O	LCD segment output 22
S23	30	M6	O	LCD segment output 23
S24	31	L7	O	LCD segment output 24
S25	32	M7	O	LCD segment output 25
GND	7	E2		Ground. It is used to shield the oscillator. See Note 1.
XIN	8	E1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	F1	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.
GND	10	F2		Ground. It is used to shield the oscillator. See Note NO TAG.
V_{REF}	60	A12	O	Input for an external reference voltage/internal reference voltage output
$\overline{RST}$/NMI	74	B5	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices).
TCK	73	A5	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start.
TDI/TCLK	71	A6	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	70	B7	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	72	B6	I	Test mode select. TMS is used as an input port for device programming and test.
XT2OUT	68	A8	O	Output terminal of crystal oscillator XT2
XT2IN	69	A7	I	Input port for crystal oscillator XT2
Reserved	NA	B11, D6, D7, D8, E4, E5, E6, E7, E8, E9, F4, F5, F8, F9, G4, G5,G8, G9, H4, H5, H6, H7, H8, H9, J5, J6, J7, J8, L2, L11		BGA package unused balls. Connection to DV_{SS}/AV_{SS} recommended.

NOTE 1: It is recommended to connect GND externally to DVss.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats, and Table 2 lists the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	●	●	MOV & MEM, & TCDAT		M(MEM) —> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

If the reset vector (located at address 0xFFFE) contains 0xFFFF (e.g., flash is not programmed) the CPU goes into LPM4 immediately after power–up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory PC Out–of–Range (see Note 4)	PORIFG RSTIFG WDTIFG KEYV (see Note 1)	Reset	0xFFFE	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1, 2 and 4)	(Non)maskable (Non)maskable (Non)maskable	0xFFFC	14
Timer_B3	TBCCR0 CCIFG0 (see Note 2)	Maskable	0xFFFA	13
Timer_B3	TBCCR1 CCIFG1 ... TBCCR3 CCIFG3, TBIFG (see Notes 1 and 2)	Maskable	0xFFF8	12
Comparator_A	CAIFG	Maskable	0xFFF6	11
Watchdog Timer+	WDTIFG	Maskable	0xFFF4	10
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (see Notes 1 and 5)	Maskable	0xFFF2	9
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG (see Note 1 and 6)	Maskable	0xFFF0	8
SD16_A	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG (see Notes 1 and 2)	Maskable	0xFFEE	7
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0xFFEC	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0xFFEA	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0xFFE8	4
DAC12	DAC12_0IFG, DAC12_1IFG	Maskable	0xFFE6	3
		Maskable	0xFFE4	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0xFFE2	1
Basic Timer1/RTC	BTIFG	Maskable	0xFFE0	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. Access and key violations, KEYV and ACCVIFG.
5. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
6. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE				UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw-0				rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive interrupt enable
UCA0TXIE	USCI_A0 transmit interrupt enable
UCB0RXIE	USCI_B0 receive interrupt enable
UCB0TXIE	USCI_B0 transmit interrupt enable
BTIE	Basic timer interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault.

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.

PORIFG Power-on interrupt flag. Set on V_{CC} power-up.

NMIIFG Set via $\overline{RST}$/NMI pin.

Address	7	6	5	4	3	2	1	0
03h	BTIFG				UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
	rw-0				rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive interrupt flag

UCA0TXIFG USCI_A0 transmit interrupt flag

UCB0RXIFG USCI_B0 receive interrupt flag

UCB0TXIFG USCI_B0 transmit interrupt flag

BTIFG Basic Timer1 interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

memory organization

		MSP430FG477	MSP430FG478	MSP430FG479
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0FFFFh to 0FFE0h 0FFFFh to 08000h	48KB 0FFFFh to 0FFE0h 0FFFFh to 04000h	60KB 0FFFFh to 0FFE0h 0FFFFh to 01100h
Information memory	Size Flash	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h
Boot memory	Size ROM	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h
RAM	Size	2KB 09FFh to 0200h	2KB 09FFh to 0200h	2KB 09FFh to 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

BSL FUNCTION	PN PACKAGE PINS	ZQW PACKAGE PINS
Data Transmit	58 - P1.0	C11 - P1.0
Data Receive	57 - P1.1	C12 - P1.1

flash memory (Flash)

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*
- Segment A might contain calibration data. After reset, segment A is protected against programming or erasing. It can be unlocked, but care should be taken not to erase this segment if this calibration data is required.
- Flash content integrity check with marginal read modes.

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

oscillator and system clock

The clock system in the MSP430FG47x is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a 8-MHz high-frequency crystal oscillator (XT1), plus a 8-MHz high-frequency crystal oscillator (XT2). The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented, ports P1 through P6.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Basic Timer1 and Real-Time Clock

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for month with less than 31 days and includes leap year correction.

LCD_A driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and, thus, contrast in software.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW					PN	ZQW
P1.5 – 51	F11	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.5 – 51	F11	TAINCLK	INCLK				
P1.0 – 58	C11	TA0	CCI0A	CCR0	TA0	P1.0 – 58	C11
P1.1 – 57	C12	TA0	CCI0B			P1.1 – 57	C12
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
P1.2 – 56	D11	TA1	CCI1A	CCR1	TA1	P1.2 – 56	D11
		CAOUT (internal)	CCI1B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
P2.0 – 4	C2	TA2	CCI2A	CCR2	TA2	P2.0 – 4	C2
		ACLK (internal)	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW					PN	ZQW
P1.4 – 54	E11	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.4 – 54	E11	$\overline{\text{TBCLK}}$ (See Note 1)	INCLK				
P2.1 – 3	C1	TB0	CCI0A	CCR0	TB0	P2.1 – 3	C1
P2.1 – 3	C1	TB0	CCI0B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				
P2.2 – 2	B1	TB1	CCI1A	CCR1	TB1	P2.2 – 2	B1
P2.2 – 2	B1	TB1	CCI1B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				
P2.3 – 77	B4	TB2	CCI2A	CCR2	TB2	P2.3 – 77	B4
		ACLK (internal)	CCI2B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				

NOTE 1: The inversion of TBCLK is done inside the module.

universal serial communication interfaces (USCIs) (USCI_A0, USCI_B0)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin), I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 pin or 4 pin), UART, enhanced UART and IrDA.

USCI_B0 provides support for SPI (3 pin or 4 pin) and I2C.

Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

SD16_A

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and a reference generator. In addition to external analog inputs, an internal V_{CC} sense and temperature sensor are also available.

DAC12

The DAC12 module is a 12-bit R-ladder voltage-output DAC. The DAC12 may be used in 8-bit or 12-bit mode. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

OA

The MSP430FG47x has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

OA0 SIGNAL CONNECTIONS								
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK		MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW						PN	ZQW
P1.6 – 50	G12	OA0I0	OAxI0	OA0	OA0OUT	OA0O	P6.0 – 67	B8
P6.2 – 65	A9	OA0I1	OAxI1					
P6.5 – 62	B10	OA0I2	OAxIA					
P1.2 – 56	D11	OA0I3	OAxIB					
P1.4 – 54	E11	OA1I0	OAxI0	OA1	OA1OUT	OA1O	P6.4 – 64	A10
P6.6 – 61	A11	OA1I1	OAxI1					
P6.7 – 59	B12	OA1I2	OAxIA					
P1.3 – 55	D12	OA1I3	OAxIB					

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B3	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 4	FCTL4	01BEh
	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
SD16_A (see also: Peripherals with Byte Access)	General control	SD16CTL	0100h
	Channel 0 control	SD16CCTL0	0102h
	Channel 0 conversion memory	SD16MEM0	0112h
	Interrupt vector word register	SD16IV	0110h
OA switches	Switch control register 1	SWCTL_1	00CEh
PERIPHERALS WITH BYTE ACCESS			
OA switches	Switch control register	SWCTL	00CFh
	Switch control register 1	SWCTL1	00CEh
OA1	Operational amplifier 1 control register 1	OA1CTL1	00C3h
	Operational amplifier 1 control register 0	OA1CTL0	00C2h
OA0	Operational amplifier 0 control register 1	OA0CTL1	00C1h
	Operational amplifier 0 control register 0	OA0CTL0	00C0h
SD16_A (see also: Peripherals with Word Access)	Channel 0 input control	SD16INCTL0	0B0h
	Analog enable	SD16AE	0B7h

peripheral file map (continued)

LCD_A	LCD voltage control 1	LCDAVCTL1	0AFh
	LCD voltage control 0	LCDAVCTL0	0AEh
	LCD voltage port control 1	LCDAPCTL1	0ADh
	LCD voltage port control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDACTL	090h
USCI A0/B0	USCI A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCTL	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I2C Interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I2C slave address	UCB0SA	0x011A
	USCI B0 I2C own address	UCB0OA	0x0118
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ control 1	FLL_CTL1	054h
	FLL+ control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
RTC (Basic Timer1)	Real-time clock year high byte	RTCYEARH	04Fh
	Real-time clock year low byte	RTCYEARL	04Eh
	Real-time clock month	RTCMON	04Dh
	Real-time clock day of month	RTCDAY	04Ch
	Basic Timer1 counter	BTCNT2	047h
	Basic Timer1 counter	BTCNT1	046h
	Real-time counter 4	RTCNT4	045h
	(Real-time clock day of week)	(RTCDOW)	
	Real-time counter 3	RTCNT3	044h
	(Real-time clock hour)	(RTCHOUR)	
	Real-time counter 2	RTCNT2	043h
	(Real-time clock minute)	(RTCMIN)	
	Real-time counter 1	RTCNT1	042h
	(Real-time clock second)	(RTCSEC)	
	Real-time clock control	RTCCTL	041h
	Basic Timer1 control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P1	Port P1 selection 2 register	P1SEL2	057h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (see Note 1)

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: (unprogrammed device, see Note 3) . . . . . –55°C to 150°C
(programmed device, see Note 3) . . . . . –40°C to 85°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			2.2		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})			0		0	V
Operating free-air temperature range, T_A			–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 1)	LF selected, XTS_FLL = 0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL = 1	Ceramic resonator	0.45		6	MHz
	XT1 selected, XTS_FLL = 1	Crystal	1		6	MHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	0.45		8	MHz
		Crystal	1		8	
System frequency, MCLK, ACLK, SMCLK , $f_{(System)}$		V_{CC} = 1.8 V	dc		4.15	MHz
		V_{CC} = 2.5 V	dc		8	

NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

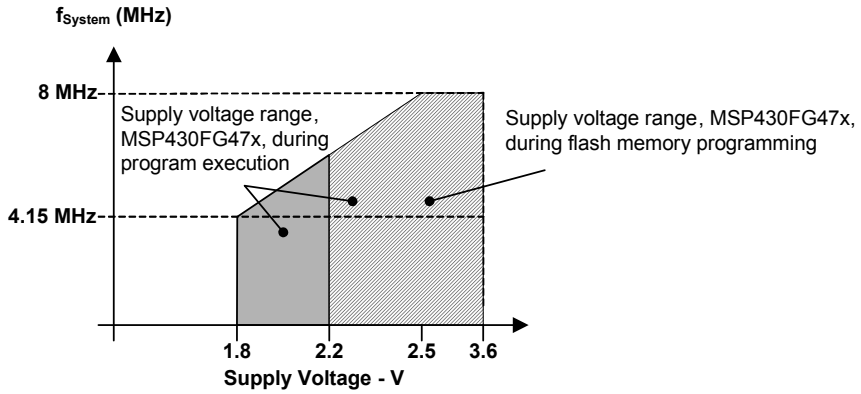


Figure 1. Frequency vs Supply Voltage, Typical Characteristics

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS = 0, SELM = (0,1)	T_A = –40°C to 85°C	2.2 V		262	295	µA
			3 V		420	460	
$I_{(LPM0)}$	Low-power mode (LPM0) (see Note 1)	T_A = –40°C to 85°C	2.2 V		32	62	µA
			3 V		51	77	
$I_{(LPM2)}$	Low-power mode (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32,768 Hz, SCG0 = 0 (see Note 2)	T_A = –40°C to 85°C	2.2 V		5	9	µA
			3 V		7	13	
$I_{(LPM3)}$	Low-power mode (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled , ACLK selected LCD_A enabled, LCDCPEN = 0: (static mode , $f_{LCD} = f_{(ACLK)}/32$) (see Note 2 and Note 3)	T_A = –40°C	2.2 V		1.0	1.8	µA
		T_A = 25°C			1.0	1.8	
		T_A = 60°C			1.1	2.0	
		T_A = 85°C			2.3	4.0	
		T_A = –40°C	3 V		1.2	2.0	
		T_A = 25°C			1.2	2.0	
		T_A = 60°C			1.4	2.2	
		T_A = 85°C			2.7	4.5	
$I_{(LPM3)}$	Low-power mode (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled , ACLK selected LCD_A enabled, LCDCPEN = 0: (4-mux mode, $f_{LCD} = f_{(ACLK)}/32$) (see Note 2 and Note 3)	T_A = –40°C	2.2 V		1.0	3.0	µA
		T_A = 25°C			1.1	3.2	
		T_A = 85°C			3.5	6.0	
		T_A = –40°C	3 V		1.8	3.3	
		T_A = 25°C			2.0	4.0	
		T_A = 85°C			4.2	7.5	
$I_{(LPM4)}$	Low-power mode (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2)	T_A = –40°C	2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.7	1.1	
		T_A = 85°C			1.7	3.0	
		T_A = –40°C	3 V		0.1	0.8	
		T_A = 25°C			0.1	0.8	
		T_A = 60°C			0.8	1.2	
		T_A = 85°C			1.5	3.5	

NOTES: 1. Timer_A is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V-T1A (9pF) crystal and OSCCAPx = 01h.

Current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)}\ [1\ MHz] \times f_{(System)}\ [MHz]$$

Current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 200\ \mu A/V \times (V_{CC} - 2.2\ V)$$

typical characteristics – LPM4 current

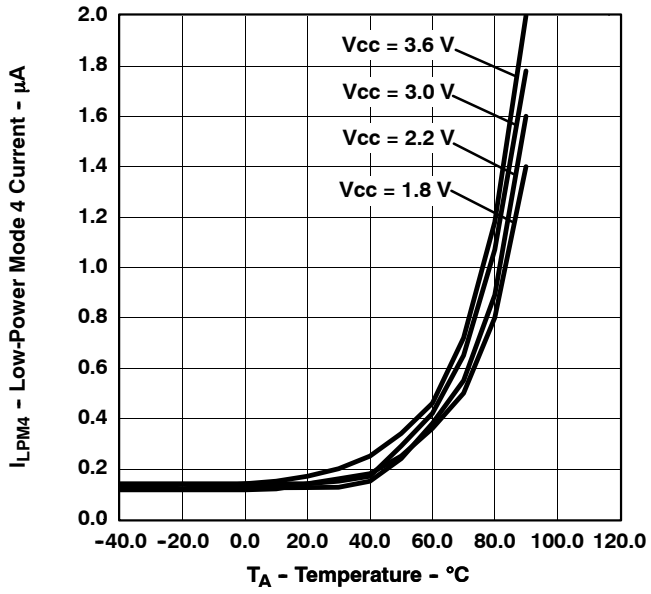


Figure 2. I_{LPM4} – LPM4 Current vs Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P3, P4, P5, and P6, $\overline{\text{RST}}$/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1	1.55	V
		V_{CC} = 3 V	1.5	1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4	0.9	V
		V_{CC} = 3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})	V_{CC} = 2.2 V	0.3	1.1	V
		V_{CC} = 3 V	0.5	1	

inputs Px.y, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag (see Note 1)	2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
			3 V		10	
$f_{(TAint)}$	Timer_A, clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – Ports P1, P2, P3, P4, P5, and P6 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	V_{CC} = 2.2 V/3 V		±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25	V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6	V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25	V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}	V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}	V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}	V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}	V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(x = 1, 2, 3, 4, 5, 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V / 3 V	DC		f_{System}	MHz
$f_{(MCLK)}$	P1.1/TA0/MCLK	C_L = 20 pF				f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

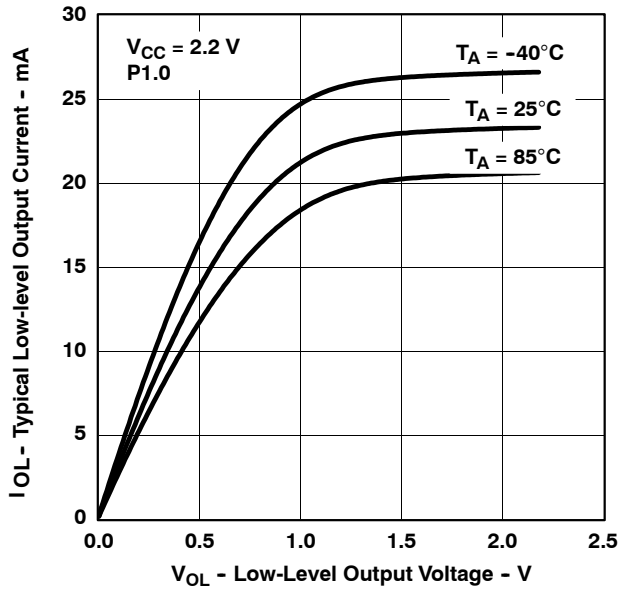


Figure 3

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

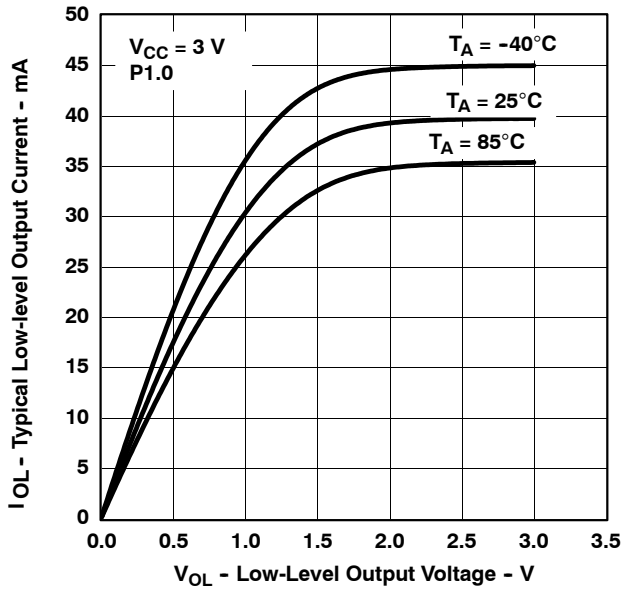


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

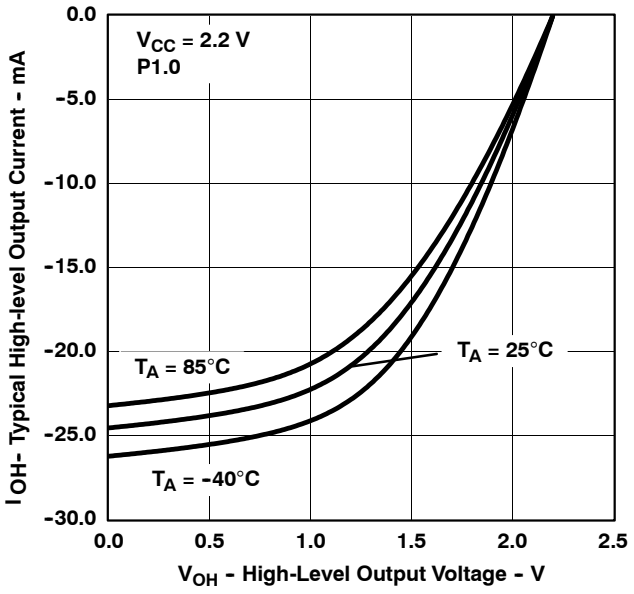


Figure 5

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

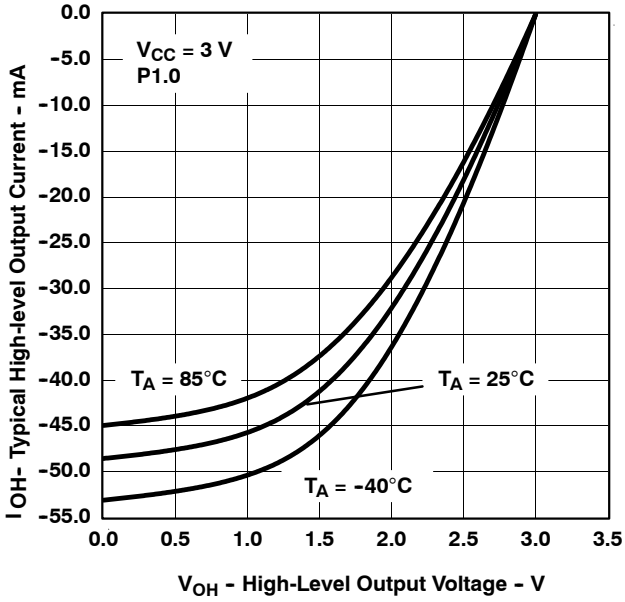


Figure 6

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 7)		0.7 × $V_{(B_IT-)}$		V
$V_{(B_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 7 through Figure 9)			1.71	V
$V_{hys(B_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 7)				mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)}$ + $V_{hys(B_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout.

typical characteristics

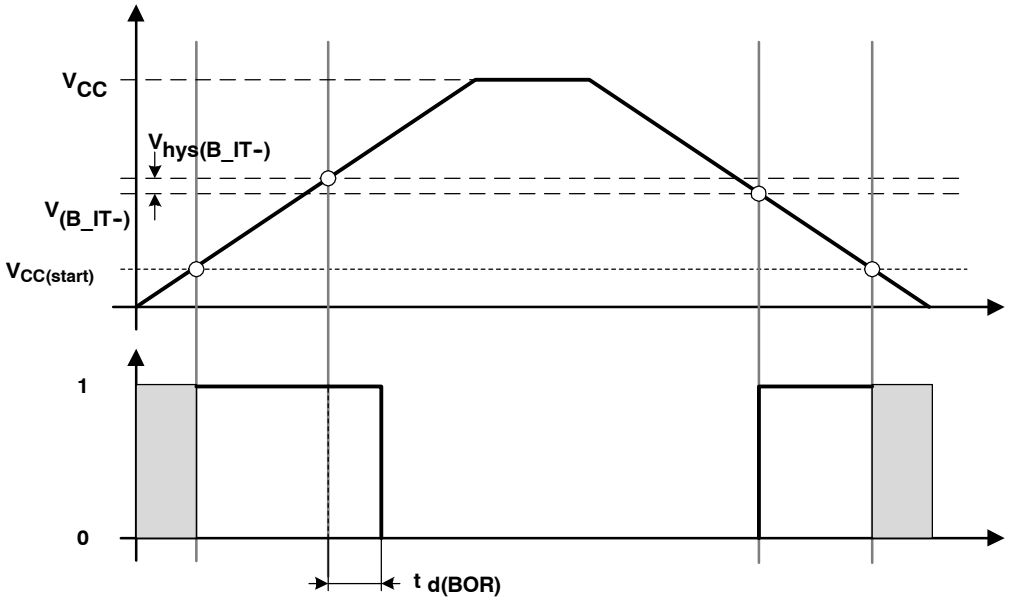


Figure 7. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics (continued)

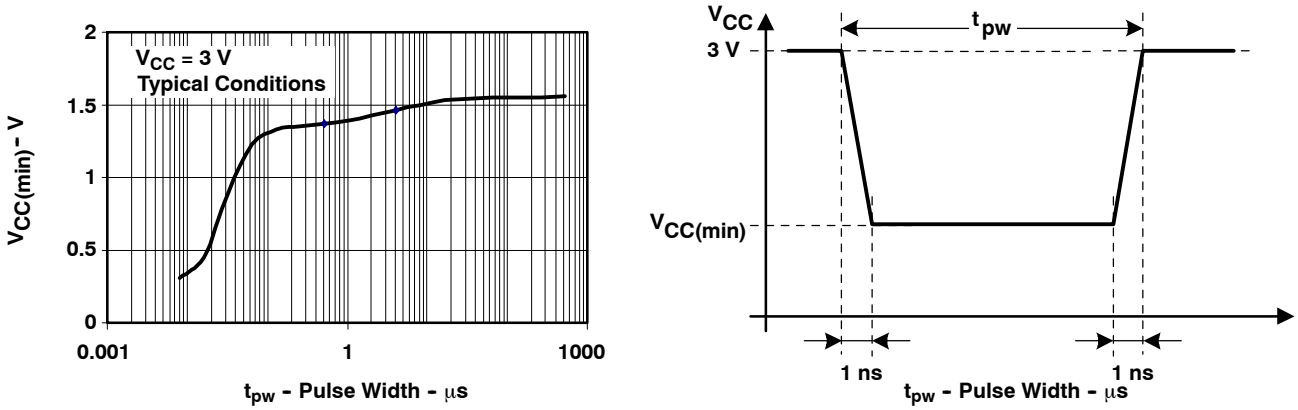


Figure 8. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

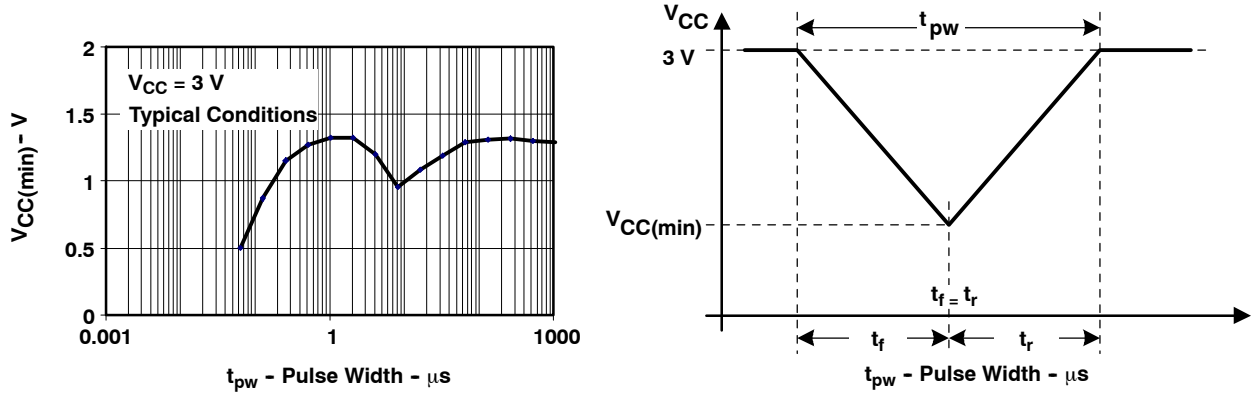


Figure 9. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 10)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	µs
$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 10)			1.55	1.7	V
$V_{hys(SVS_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 10)	VLD = 1	70	120	210	mV
		VLD = 2 .. 14	$V_{(SVS_IT-)}$ x 0.001		$V_{(SVS_IT-)}$ x 0.016	
	$V_{CC}/dt \le 3$ V/s (see Figure 10), External voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 10 and Figure 11)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \le 3$ V/s (see Figure 10 and Figure 11), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

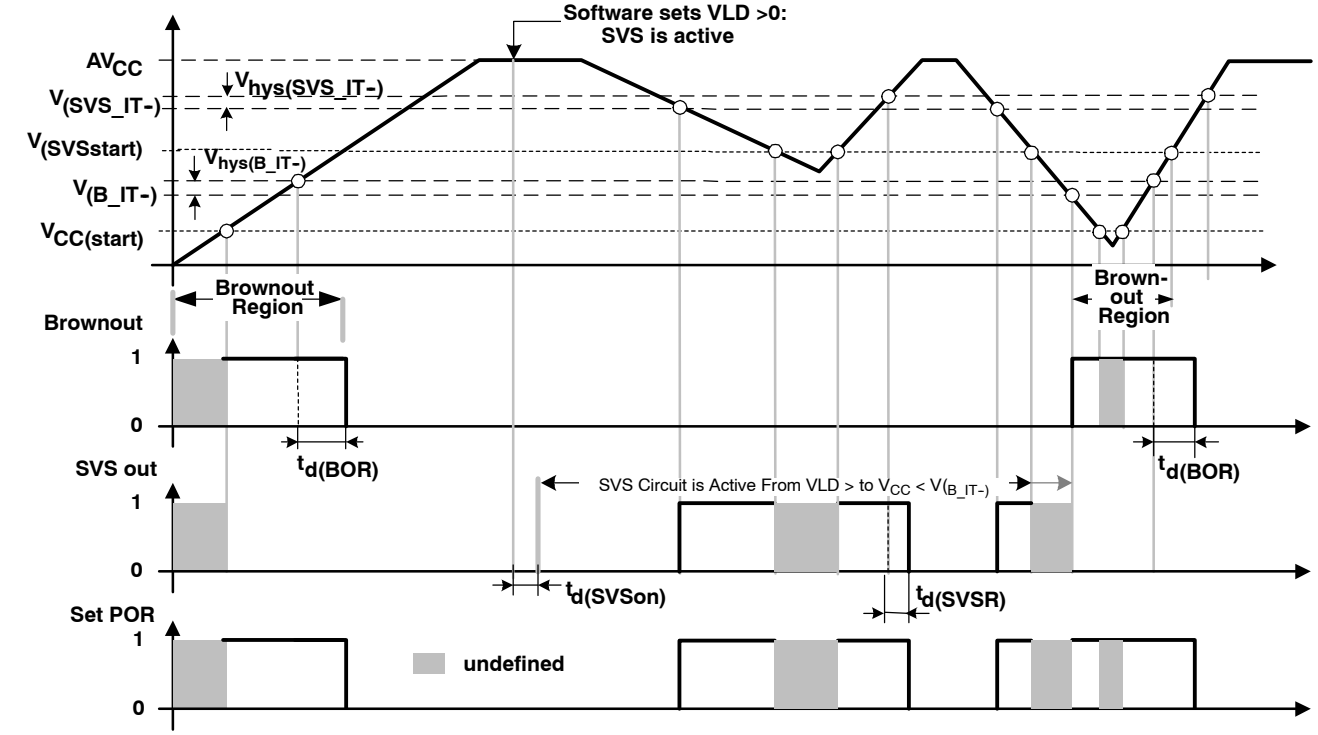


Figure 10. SVS Reset (SVSR) vs Supply Voltage

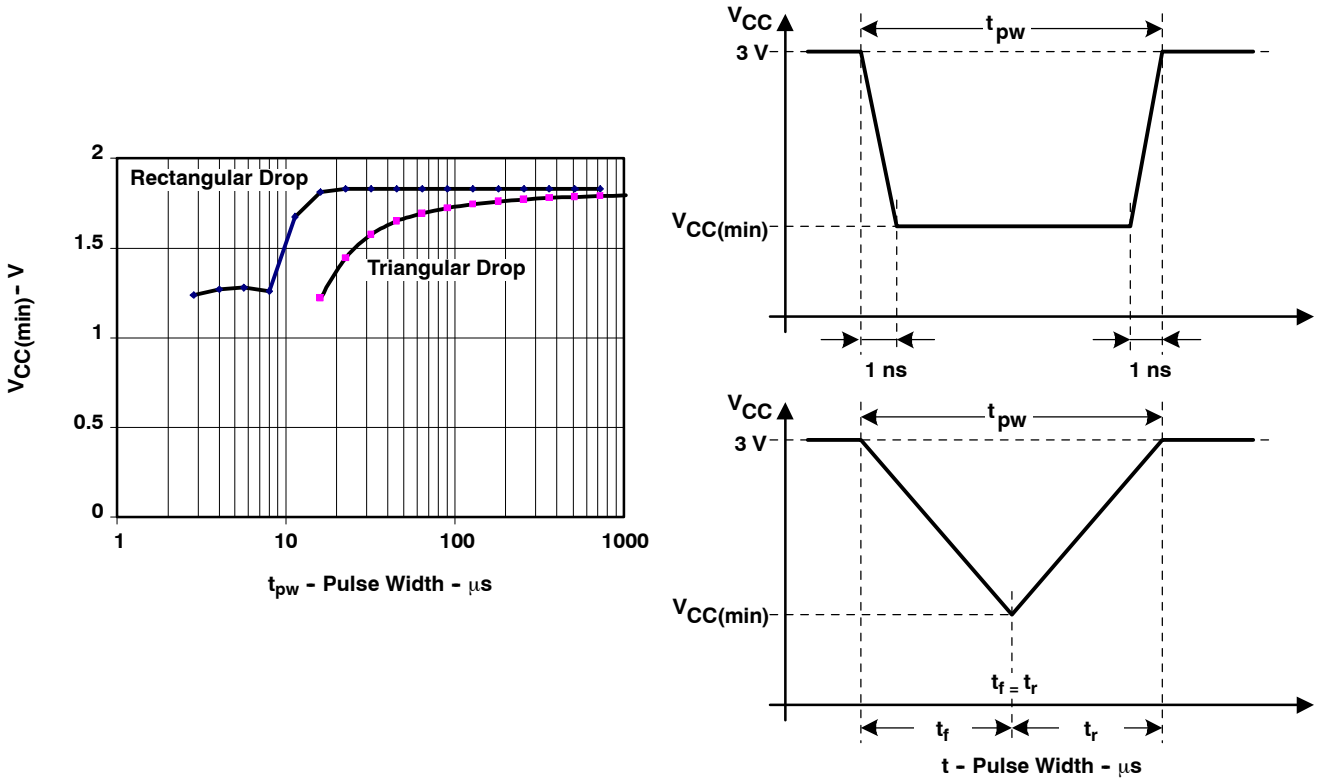


Figure 11. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01E0h, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0 , DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1 (see Note 1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO2)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO27)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1 (see Note 1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1 (see Note 1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1 (see Note 1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO2)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO27)}$	FN_8 = 1,FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1 (see Note 1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 13 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8 = FN_4 = FN_3 = FN_2 = 0 D = 2, DCOPLUS = 0 (see Note 2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0 (see Note 2)		0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.
2. This parameter is not production tested.

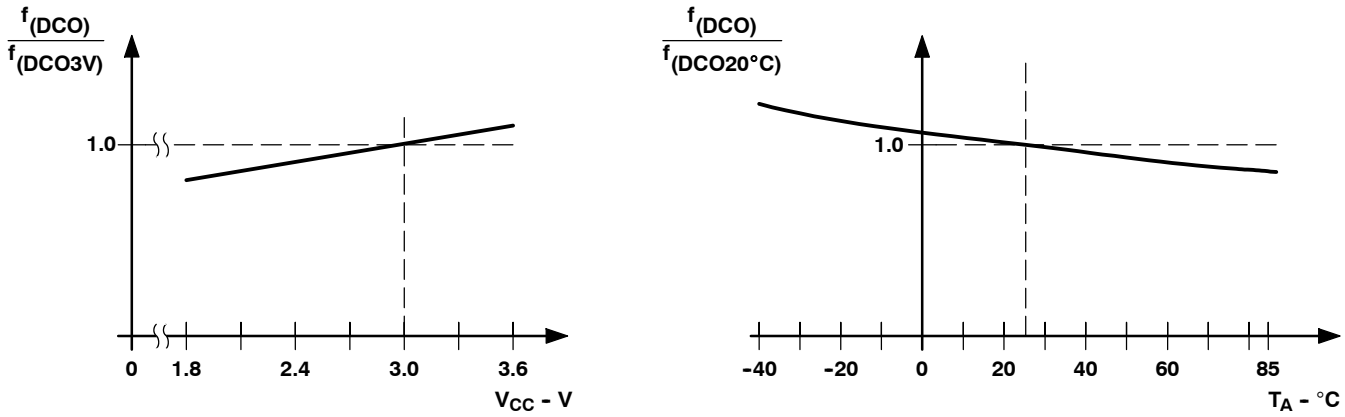


Figure 12. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

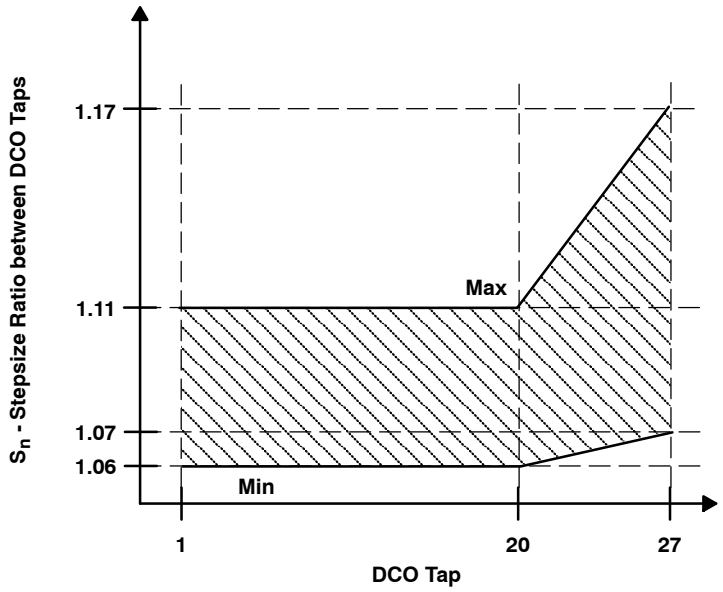


Figure 13. DCO Tap Step Size

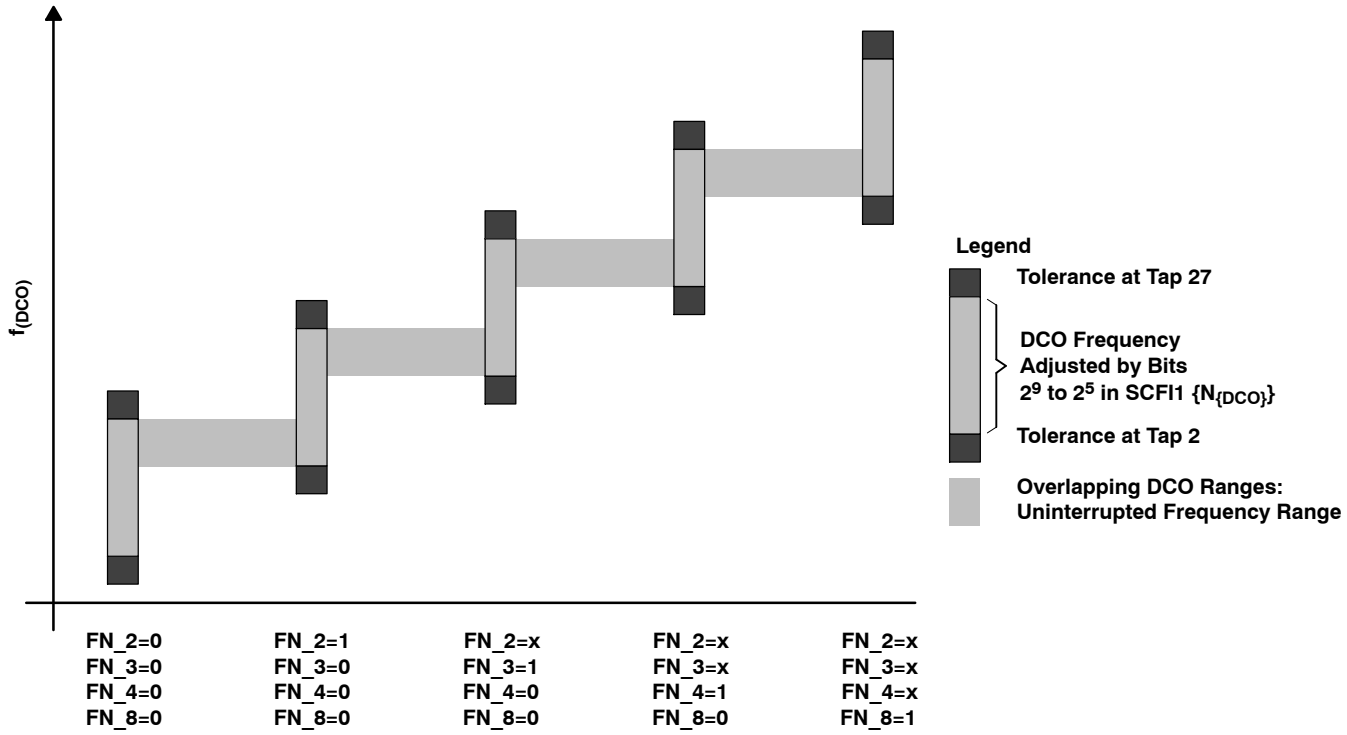


Figure 14. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32,768		Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P1.5/ACLK, $f_{LFXT1,LF}$ = 32,768Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, XCAPx = 0. LFXT1Sx = 3 (see Note 2)	2.2 V/3 V	10		10,000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1, high frequency modes

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{LFXT1}	LFXT1 oscillator crystal frequency	Ceramic resonator	1.8 V to 3.6 V	0.45		8	MHz
f_{LFXT1}	LFXT1 oscillator crystal frequency	Crystal resonator	1.8 V to 3.6 V	1		8	MHz
$C_{L,eff}$	Integrated effective load capacitance, HF mode (see Note 1)	(see Note 2)			1		pF
Duty cycle		Measured at P1.5/ACLK,	2.2 V/3 V	40	50	60	%

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

crystal oscillator, XT2, high frequency modes

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency	Ceramic resonator	1.8 V to 3.6 V	0.45		8	MHz
f_{XT2}	XT2 oscillator crystal frequency	Crystal resonator	1.8 V to 3.6 V	1		8	MHz
$C_{L,eff}$	Integrated effective load capacitance, HF mode (see Note 1)	(see Note 2)			1		pF
Duty cycle		Measured at P1.4/SMCLK,	2.2 V/3 V	40	50	60	%

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

RAM

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6		V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply Voltage Range	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP (see Note 1)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		4.7			μF
$I_{CC(LCD)}$	Average Supply Current (see Note 2)	$V_{LCD(typ)}$ = 3 V, LCDCPEN = 1, VLCDx = 1000, All segments on, $f_{LCD} = f_{ACLK}/32$, No LCD connected (see Note 3), T_A = 25°C	2.2 V		3.8		μA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			V_{CC}		V
V_{LCD}	LCD voltage	VLCDx = 0001			2.60		V
V_{LCD}	LCD voltage	VLCDx = 0010			2.66		V
V_{LCD}	LCD voltage	VLCDx = 0011			2.72		V
V_{LCD}	LCD voltage	VLCDx = 0100			2.78		V
V_{LCD}	LCD voltage	VLCDx = 0101			2.84		V
V_{LCD}	LCD voltage	VLCDx = 0110			2.90		V
V_{LCD}	LCD voltage	VLCDx = 0111			2.96		V
V_{LCD}	LCD voltage	VLCDx = 1000			3.02		V
V_{LCD}	LCD voltage	VLCDx = 1001			3.08		V
V_{LCD}	LCD voltage	VLCDx = 1010			3.14		V
V_{LCD}	LCD voltage	VLCDx = 1011			3.20		V
V_{LCD}	LCD voltage	VLCDx = 1100			3.26		V
V_{LCD}	LCD voltage	VLCDx = 1101			3.32		V
V_{LCD}	LCD voltage	VLCDx = 1110			3.38		V
V_{LCD}	LCD voltage	VLCDx = 1111			3.44	3.60	V
R_{LCD}	LCD Driver Output impedance	V_{LCD} = 3 V, LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 μA	2.2 V			10	kΩ

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Refer to the supply current specifications $I_{(LPM3)}$ for additional current specifications with the LCD_A module active.
3. Connecting an actual display will increase the current consumption depending on the size of the LCD.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	V_{CC} = 2.2 V		25	40	μA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V		30	50	μA
			V_{CC} = 3 V		45	80	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 15 and Figure 16	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1, $T_{A\ =}$ 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON = 1	V_{CC} = 2.2 V / 3 V	0		V_{CC}–1	V
V_p–V_S	Offset voltage	See Note 2	VCC = 2.2 V / 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH\ and\ HL)}$, see Note 3		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	80	165	300	ns
			V_{CC} = 3 V	70	120	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	2.8	μs
			V_{CC} = 3 V	0.9	1.5	2.2	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.
3. The response time is measured at P1.6/CA0 with an input voltage step and the Comparator_A already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300ns is added to the response time.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

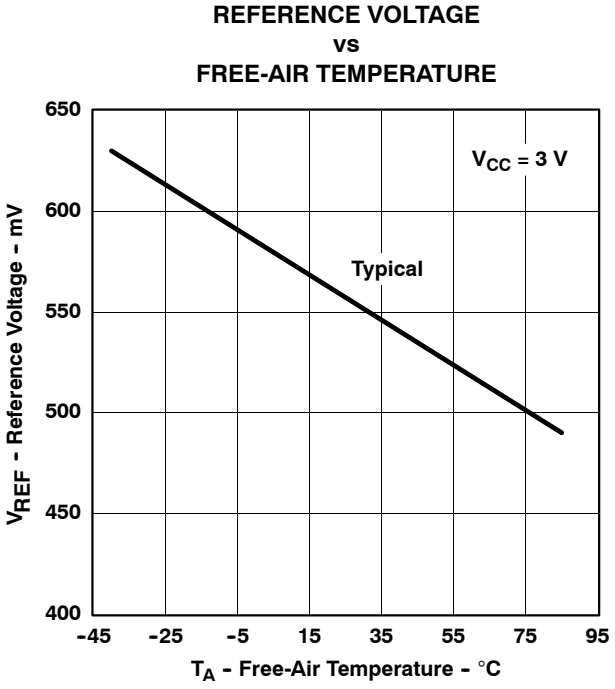


Figure 15. $V_{(RefVT)}$ vs Temperature

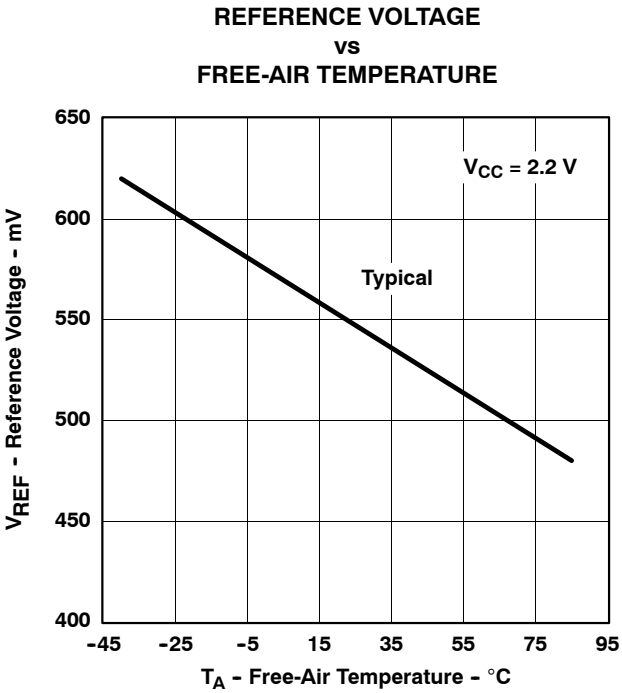


Figure 16. $V_{(RefVT)}$ vs Temperature

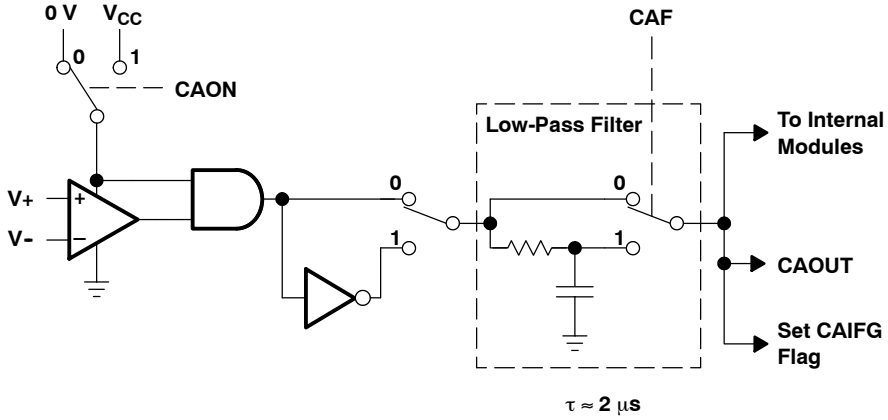


Figure 17. Block Diagram of Comparator_A Module

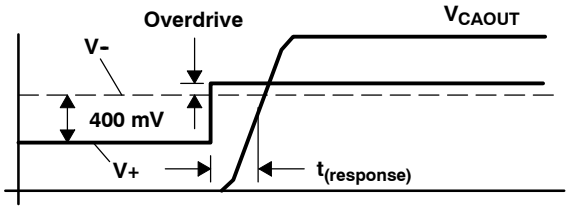


Figure 18. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, power supply and recommended operating conditions

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$			2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1,2	3 V		750	1050	μA
			SD16BUFx = 00, GAIN: 4,8,16	3 V		830	1150	
			SD16BUFx = 00, GAIN: 32	3 V		1150	1700	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1	3 V		730	1030	
			SD16BUFx = 00, GAIN: 32	3 V		830	1150	
		SD16LP = 0, SD16OSR = 256	SD16BUFx = 01, GAIN: 1	3 V		850		
			SD16BUFx = 10, GAIN: 1	3 V		1000		
			SD16BUFx = 11, GAIN: 1	3 V		1130		
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)		3 V	0.03	0.5		

SD16_A, input range

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_I	Absolute input voltage range	SD16BUFx = 00			AV_{SS} -0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS} +0.2V		AV_{CC} –1.2 V	
V_{IC}	Common-mode input voltage range	SD16BUFx = 00			AV_{SS} -0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS} +0.2V		AV_{CC} –1.2 V	
$V_{ID,FSR}$	Differential full scale input voltage range	Bipolar mode, SD16UNI = 0			$-V_{REF}/2GAIN$		$+V_{REF}/2GAIN$	mV
		Unipolar mode, SD16UNI = 1			0		$+V_{REF}/2GAIN$	mV
V_{ID}	Differential input voltage range for specified performance (see Note 1)	SD16REFON = 1	SD16GAINx = 1			±500		mV
			SD16GAINx = 2			±250		
			SD16GAINx = 4			±125		
			SD16GAINx = 8			±62		
			SD16GAINx = 16			±31		
			SD16GAINx = 32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1 MHz, SD16BUFx = 00	SD16GAINx = 1	3 V		200		kΩ
			SD16GAINx = 32	3 V		75		
		f_{SD16} = 1 MHz, SD16BUFx = 01	SD16GAINx = 1	3 V		>10		MΩ
Z_{ID}	Differential input impedance (IN+ to IN–)	f_{SD16} = 1 MHz, SD16BUFx = 00	SD16GAINx = 1	3 V	300	400		kΩ
			SD16GAINx = 32	3 V	100	150		
		f_{SD16} = 1 MHz, SD16BUFx > 00	SD16GAINx = 1	3 V		>10		MΩ

NOTES: 1. The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, performance (f_{SD16} = 30kHz, SD16REFON = 1, SD16BUFx = 01)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 256	f_{IN} = 2.8Hz	3 V		84		dB
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 512		3 V		84		
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 1024		3 V		84		
	Nominal gain	SD16GAINx = 1, SD16OSRx = 1024		3 V	0.97	1.00	1.02	
dG/dT	Gain temperature drift	SD16GAINx = 1, SD16OSRx = 1024 (see Note 1)		3 V		15		ppm/°C
dG/dV_{CC}	Gain supply voltage drift	SD16GAINx = 1, SD16OSRx = 1024, V_{CC} = 2.5 V to 3.6 V (see Note 2)				0.35		%/V

NOTES: 1. Calculated using the box method: (MAX(–40...85°C) – MIN(–40...85°C))/MIN(–40...85°C)/(85C – (–40°C))
2. Calculated using the box method: (MAX(2.5...3.6V) – MIN(2.5...3.6V))/MIN(2.5...3.6V)/(3.6V – 2.5 V)

SD16_A, performance (f_{SD16} = 1MHz, SD16OSRx = 256, SD16REFON = 1, SD16BUFx = 00)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500mV	f_{IN} = 50Hz, 100Hz	3 V	83.5	85		dB
		SD16GAINx = 2,Signal Amplitude = 250mV		3 V	81.5	84		
		SD16GAINx = 4,Signal Amplitude = 125mV		3 V	76	79.5		
		SD16GAINx = 8,Signal Amplitude = 62mV		3 V	73	76.5		
		SD16GAINx = 16,Signal Amplitude = 31mV		3 V	69	73		
		SD16GAINx = 32,Signal Amplitude = 15mV		3 V	62	69		
G	Nominal gain	SD16GAINx = 1		3 V	0.97	1.00	1.02	
		SD16GAINx = 2		3 V	1.90	1.96	2.02	
		SD16GAINx = 4		3 V	3.76	3.86	3.96	
		SD16GAINx = 8		3 V	7.36	7.62	7.84	
		SD16GAINx = 16		3 V	14.56	15.04	15.52	
		SD16GAINx = 32		3 V	27.20	28.35	29.76	
E_{OS}	Offset error	SD16GAINx = 1		3 V			±0.2	%FSR
		SD16GAINx = 32		3 V			±1.5	
dE_{OS}/dT	Offset error temperature coefficient	SD16GAINx = 1		3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32		3 V		±20	±100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>75		
PSRR	Power supply rejection ratio	SD16GAINx = 1		3 V		>80		dB

NOTES: 1. Calculated using the box method: (MAX(–40...85°C) – MIN(–40...85°C)) / MIN(–40...85°C) / (85°C – (–40°C))
2. Calculated using the ADC output code and the box method:
(MAX-code(2.5...3.6V) – MIN-code(2.5...3.6V)) / MIN-code(2.5...3.6V) / (3.6V – 2.5 V)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, linearity (f_{SD16} = 1MHz, SD16REFON = 1, SD16BUFx = 00)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
INL	Integral non-linearity	SD16OSR = 256, SD16GAINx = 000b, Signal Amplitude = 500 mV	3 V		1.5		LSB
		SD16OSR = 256, SD16GAINx = 101b, Signal Amplitude = 15 mV	3 V		6		
		SD16OSR = 1024, SD16GAINx = 000b, Signal Amplitude = 500 mV	3 V		0.8		LSB
		SD16OSR = 1024, SD16GAINx = 101b, Signal Amplitude = 15 mV	3 V		3.5		

typical characteristics - SD16_A SINAD performance over OSR

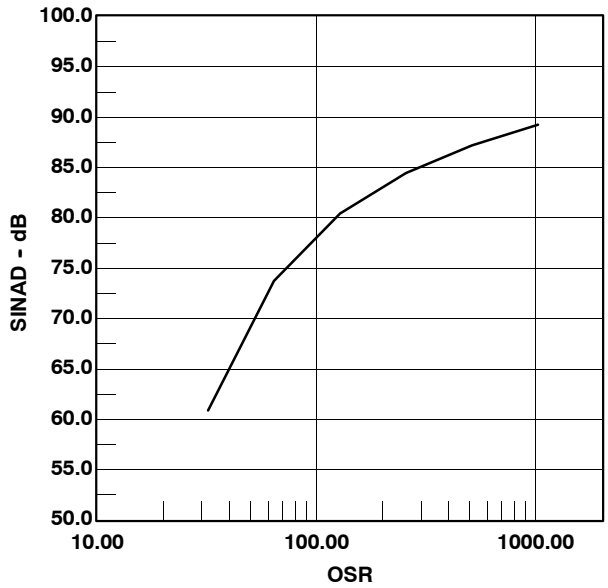


Figure 19. SINAD performance over OSR, f_{SD16} = 1MHz, SD16REFON = 1, SD16GAINx = 1

SD16_A, temperature sensor and built-in V_{CC} sense

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient	See Note 1		1.18	1.32	1.46	mV/K
$V_{Offset,sensor}$	Sensor offset voltage	See Note 1		–100		100	mV
V_{Sensor}	Sensor output voltage (see Note 3)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C	3 V	355	395	435	
		Temperature sensor voltage at T_A = 0°C (see Note 1)	3 V	320	360	400	
$V_{CC,Sense}$	V_{CC} divider at input 5	f_{SD16} = 32kHz, SD16OSRx = 256, SD16REFON = 1		0.08	1/11	0.1	V

NOTES: 1. Not production tested, limits characterized.
2. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV]
3. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, built-in voltage reference

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	μA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0 (see Note 1)	3 V		18	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0 (see Note 2)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1, SD16VMIDON = 0	3 V			±200	nA
t_{ON}	Turn on time	SD16REFON = 0->1, SD16VMIDON = 0, C_{REF} = 100nF	3 V		5		ms
PSRR	Line regulation	SD16REFON = 1, SD16VMIDON = 0	3 V		100		uV/V

NOTES: 1. Calculated using the box method: (MAX(–40...85°C) – MIN(–40...85°C))/MIN(–40...85°C)/(85C – (–40°C))
2. There is no capacitance required on V_{REF}. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

SD16_A, reference output buffer

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference Supply + Reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	μA
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			±1	mA
	Maximum voltage variation vs load current	$\|I_{LOAD}\|$ = 0 to 1mA	3 V	–15		+15	mV
t_{ON}	Turn on time	SD16REFON = 0->1, SD16VMIDON = 1, C_{REF} = 470nF	3 V		100		μs

SD16_A, external reference input

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} = 0 V		2.20		3.60	V
I_{DD}	Supply current (see Notes 1 and 2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0800h	2.2 V/3 V		50	110	μA
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12}$ = AV_{CC}	2.2 V/3 V		50	110	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12}$ = AV_{CC}	2.2 V/3 V		200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12}$ = AV_{CC}	2.2 V/3 V		700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, $V_{REF,DAC12}$ = 1.2 V, ΔAV_{CC} = 100 mV	2.7 V		70		dB

NOTES: 1. No load at the output pin assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. PSRR = $20*\log\{\Delta AV_{CC}/\Delta V_{DAC12_xOUT}\}$.
4. V_{REF} is applied externally. The internal reference is not used.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 20)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
INL	Integral nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2 V or $V_{REF,ext}$ = 2.5 V DAC12AMPx = 7, DAC12IR = 1	2.7 V		±2.0	±8.0	LSB
DNL	Differential nonlinearity (see Note 1)	$V_{REF,ext}$ = 1.2 V DAC12AMPx = 7, DAC12IR = 1	2.7 V	–1	±0.4	+1.3	LSB
		$V_{REF,ext}$ = 2.5 V DAC12AMPx = 7, DAC12IR = 1	2.7 V		±0.4	±1.0	LSB
DNL	Differential nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2 V DAC12AMPx = 7, DAC12IR = 1	2.7 V		±0.4	±1.0	LSB
E_O	Offset voltage without calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2 V DAC12AMPx = 7, DAC12IR = 1	2.7 V			±20	mV
	Offset voltage with calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2 V DAC12AMPx = 7, DAC12IR = 1	2.7 V			±2.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.7 V		±30		µV/C
E_G	Gain error (see Note 1)	$V_{REF,DAC12}$ = 1.2 V	2.7 V			±3.50	% FSR
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.7 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx = 2	2.7 V			100	ms
		DAC12AMPx = 3,5	2.7 V			32	
		DAC12AMPx = 4,6,7	2.7 V			6	

NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b*x. $V_{DAC12_xOUT} = E_O + (1 + E_G) * (V_{REF,DAC12}/4095) *$ DAC12_xDAT, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

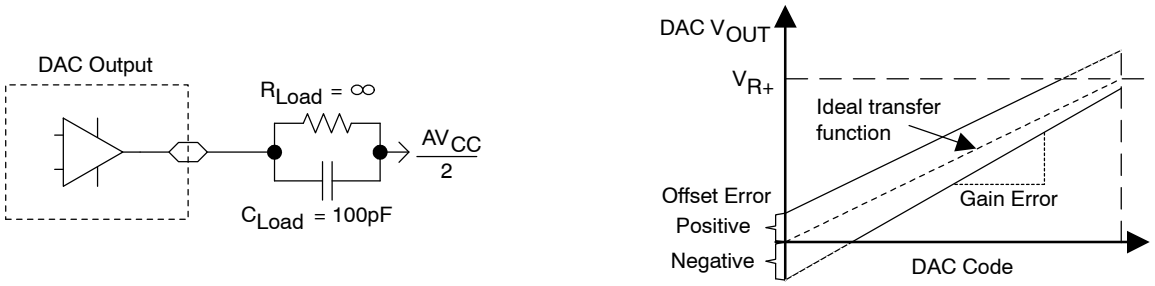
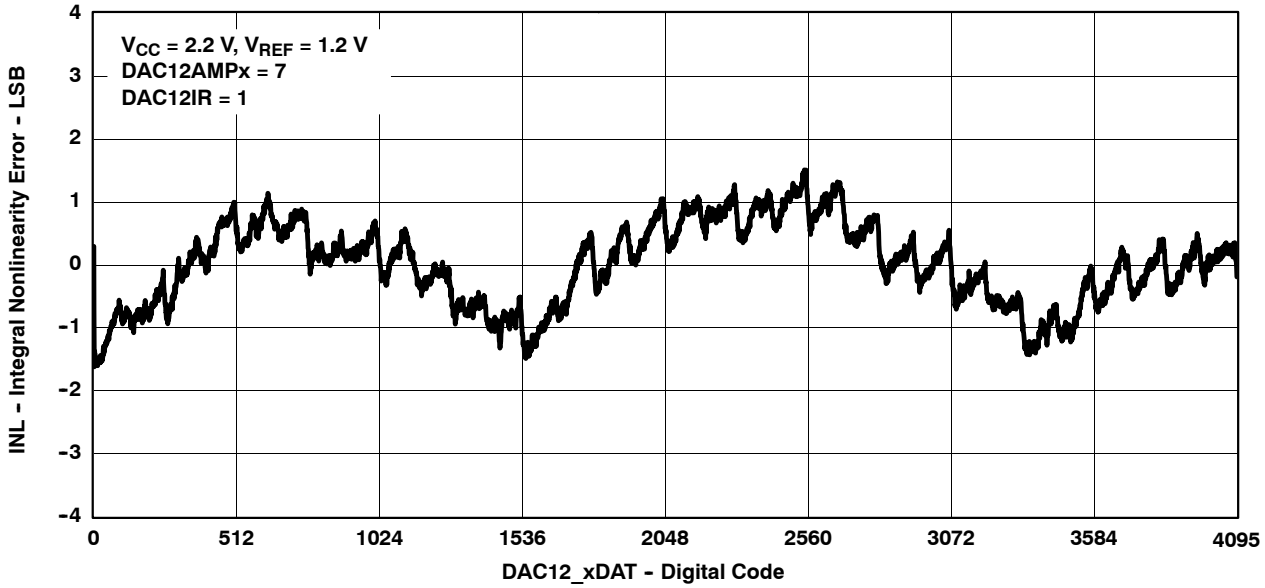


Figure 20. Linearity Test Load Conditions and Gain/Offset Definition

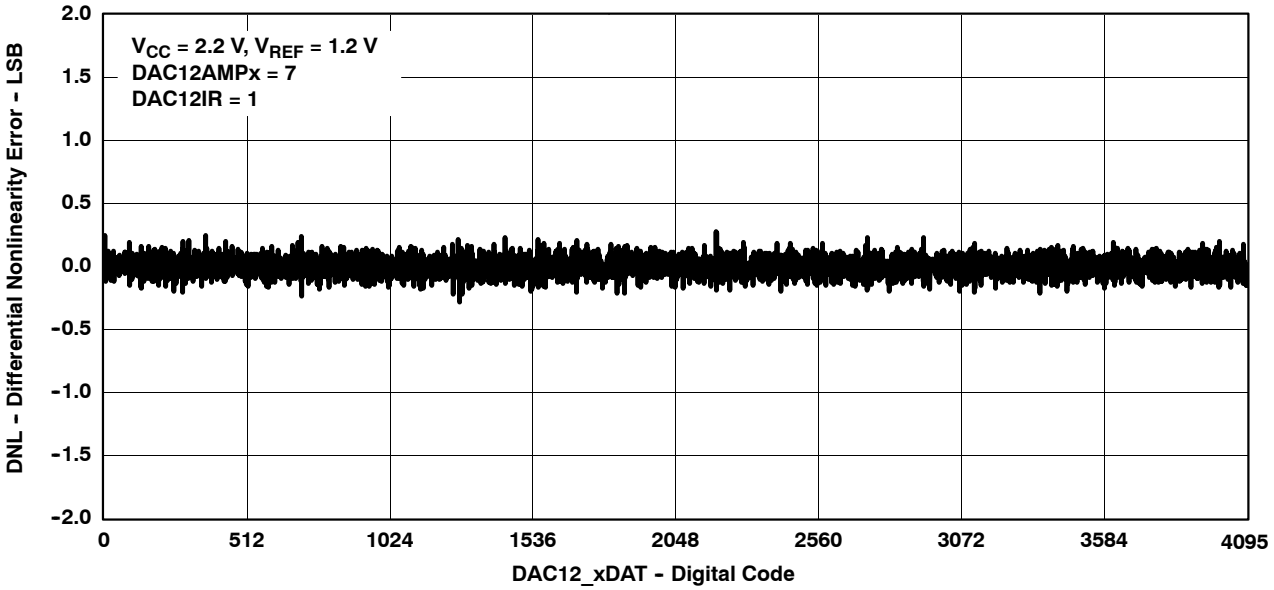
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

TYPICAL INL ERROR
vs
DIGITAL INPUT DATA



TYPICAL DNL ERROR
vs
DIGITAL INPUT DATA

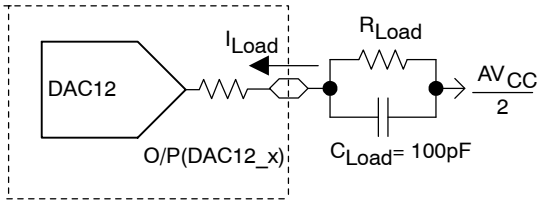


electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1, Figure 23)	No Load, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V/3 V	0		0.005	V
		No Load, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2 V/3 V	AV_{CC}–0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V/3 V	0		0.1	
		R_{Load} = 3 kΩ, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2 V/3 V	AV_{CC}–0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2 V/3 V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2V	–0.5		+0.5	mA
			3V	–1.0		+1.0	
$R_{O/P(DAC12)}$	Output resistance (see Figure 23)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2 V/3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$–0.3 V DAC12_xDAT = 0FFFh	2.2 V/3 V		150	250	
		R_{Load} = 3 kΩ, 0.3V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} – 0.3V	2.2 V/3 V		1	4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.



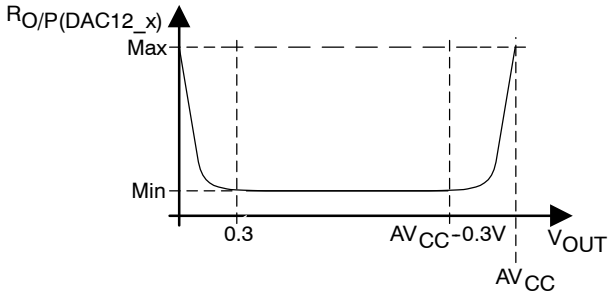


Figure 23. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Reference input voltage range	DAC12IR = 0 (see Notes 1 and 2)	2.2 V/3 V		AV_{CC}/3	AV_{CC}+0.2	V
		DAC12IR = 1 (see Notes 3 and 4)	2.2 V/3 V		AV_{CC}	AV_{CC}+0.2	
$Ri_{(VREF)}$	Reference input resistance	DAC12IR = 0, SD16VMIDON = 1 (see Note 5)	2.2 V/3 V	20			MΩ
		DAC12IR = 1, SD16VMIDON = 1	2.2 V/3 V	40	48	56	kΩ

NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
2. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} - V_{E(O)}] / [3*(1 + E_G)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
4. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.
5. Characterized, not production tested

12-bit DAC, dynamic specifications ($V_{REF,DAC12} = AV_{CC}$, DAC12IR = 1) (see Figure 24 and Figure 25)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (see Note 1, Figure 24)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V/3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}	2.2 V/3 V		15	30	
			DAC12AMPx = 0 → 7	2.2 V/3 V		6	12	
$t_{S(FS)}$	Settling time,full-scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx = 2	2.2 V/3 V		100	200	µs
			DAC12AMPx = 3,5	2.2 V/3 V		40	80	
			DAC12AMPx = 4,6,7	2.2 V/3 V		15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12AMPx = 2	2.2 V/3 V		5		µs
			DAC12AMPx = 3,5	2.2 V/3 V		2		
			DAC12AMPx = 4,6,7	2.2 V/3 V		1		
SR	Slew Rate	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx = 2	2.2 V/3 V	0.05	0.12		V/µs
			DAC12AMPx = 3,5	2.2 V/3 V	0.35	0.7		
			DAC12AMPx = 4,6,7	2.2 V/3 V	1.5	2.7		
Glitch energy: full-scale		DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx = 2	2.2 V/3 V		600		nV-s
			DAC12AMPx = 3,5	2.2 V/3 V		150		
			DAC12AMPx = 4,6,7	2.2 V/3 V		30		

NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not AV_{CC}/2) in Figure 24.
2. Slew rate applies to output voltage steps > = 200 mV.

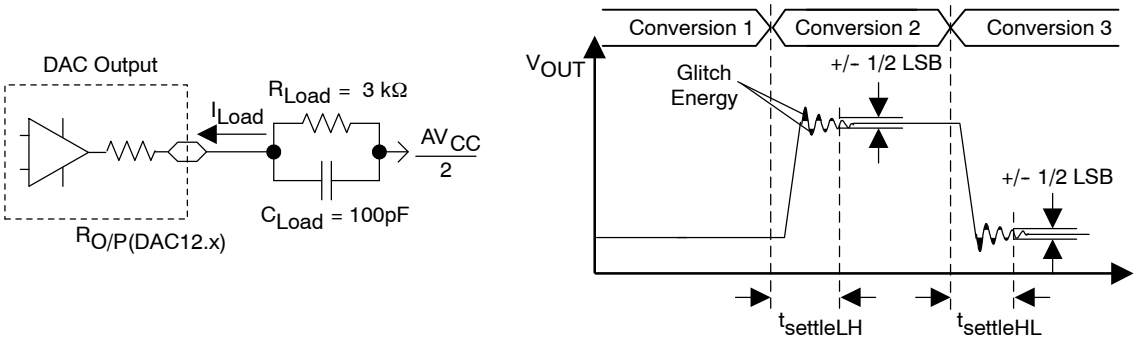


Figure 24. Settling Time and Glitch Energy Testing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

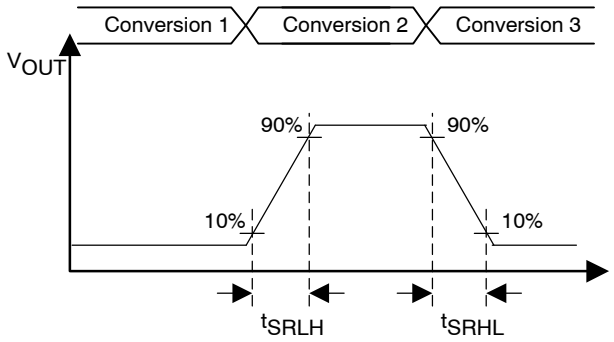


Figure 25. Slew Rate Testing

12-bit DAC, dynamic specifications continued (T_A = 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1V_{PP} (see Figure 26)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V/3 V	40		kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V/3 V	180		
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V/3 V	550		

NOTES: 1. R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

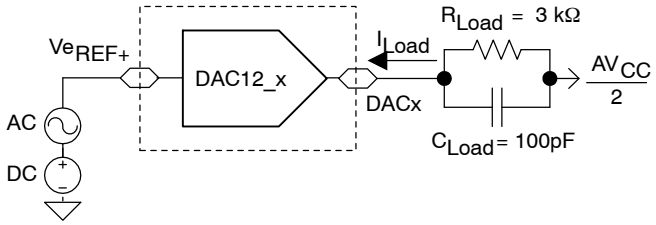


Figure 26. Test Conditions for 3-dB Bandwidth Specification

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

operational amplifier OA, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			2.2		3.6	V
I_{CC}	Supply current (see Note 1)	Fast Mode	2.2 V/3 V		180	290	μA
		Medium Mode			110	190	
		Slow Mode			50	80	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V/3 V		70		dB

NOTES: 1. Corresponding pins configured as OA inputs and outputs respectively.

operational amplifier OA, input/output specification

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Input voltage range				–0.1		V_{CC}–1.2	V
I_{lkg}	Input leakage current (see Notes 1 and 2)	T_A = –40 to +55°C		2.2 V/3 V	–5	±0.5	5	nA
		T_A = +55 to +85°C			–20	±5	20	
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz			50		nV/√Hz
		Medium Mode				80		
		Slow Mode				140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium Mode				50		
		Slow Mode				65		
V_{IO}	Offset voltage, I/P			2.2 V/3 V			±10	mV
	Offset temperature drift, I/P	see Note 3		2.2 V/3 V		±10		μV/°C
	Offset voltage drift with supply, I/P	0.3 V ≤ V_{IN} ≤ V_{CC}–1.0 V ΔV_{CC} ≤ ± 10%, T_A = 25°C		2.2 V/3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ –500 μA		2.2 V/3 V	V_{CC}–0.2		V_{CC}	V
		Slow Mode, I_{SOURCE} ≤ –150 μA			V_{CC}–0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500 μA		2.2 V/3 V	V_{SS}		0.2	V
		Slow Mode, I_{SOURCE} ≤ +150 μA			V_{SS}		0.1	
CMRR	Common-mode rejection ratio	Noninverting		2.2 V/3 V		70		dB

NOTES: 1. ESD damage can degrade input current leakage.
2. The input bias current is overridden by the input leakage current.
3. Calculated using the box method
4. Specification valid for voltage-follower OAx configuration

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

operational amplifier OA, dynamic specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode			1.2		V/μs
		Medium Mode			0.8		
		Slow Mode			0.3		
	Open-loop voltage gain				100		dB
ϕ_m	Phase margin	C_L = 50 pF			60		deg
	Gain margin	C_L = 50 pF			20		dB
GBW	Gain-bandwidth product (see Figure 27 and Figure 28)	Noninverting, Fast Mode, R_L = 47 kΩ, C_L = 50 pF	2.2 V/3 V		2.2		MHz
		Noninverting, Medium Mode, R_L = 300 kΩ, C_L = 50pF			1.4		
		Non-inverting, Slow Mode, R_L = 300 kΩ, C_L = 50pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, Noninverting, Gain = 1	2.2 V/3 V		10	20	μs
$t_{en(off)}$	Enable time off		2.2 V/3 V			1	μs

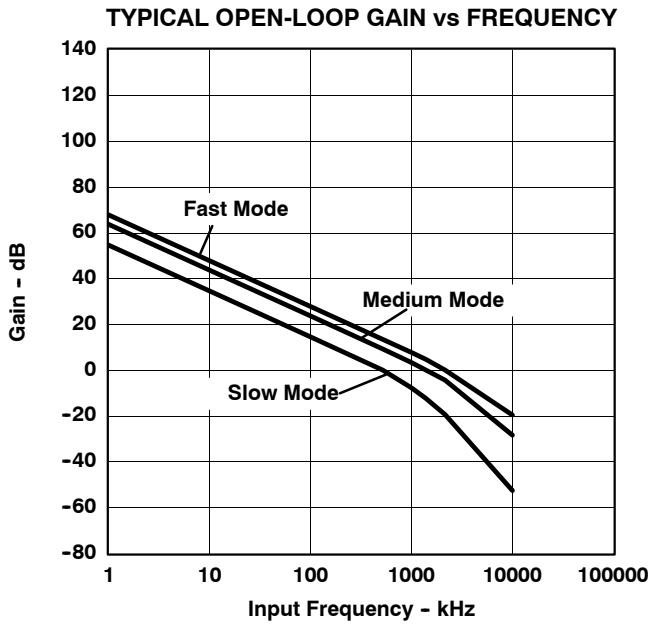


Figure 27

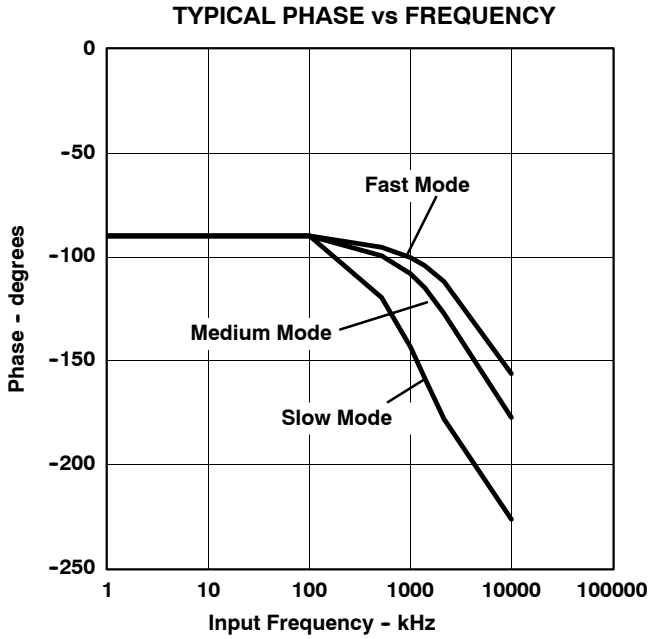


Figure 28

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

switches between OA terminals and pins

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		–	2.2		3.6	V
I_{lkg}	Input leakage current (see Note 1)	T_A = –40°C to 55°C			±1	±10	nA
		T_A = 55°C to 85°C				±50	
I_{IN}	Input current	Input switched to ON		0		100	μA
R_{ON}	On resistance	I_{IN} = 100 μA			1		kΩ

NOTES: 1. ESD damage can degrade input current leakage.

typical characteristics

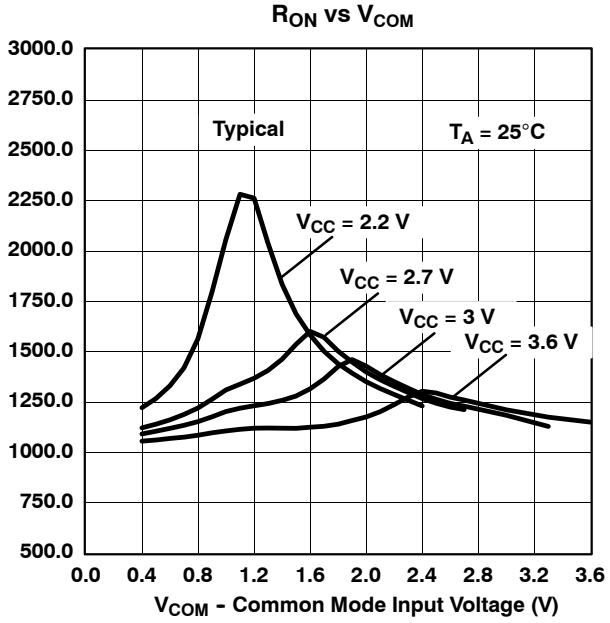


Figure 29

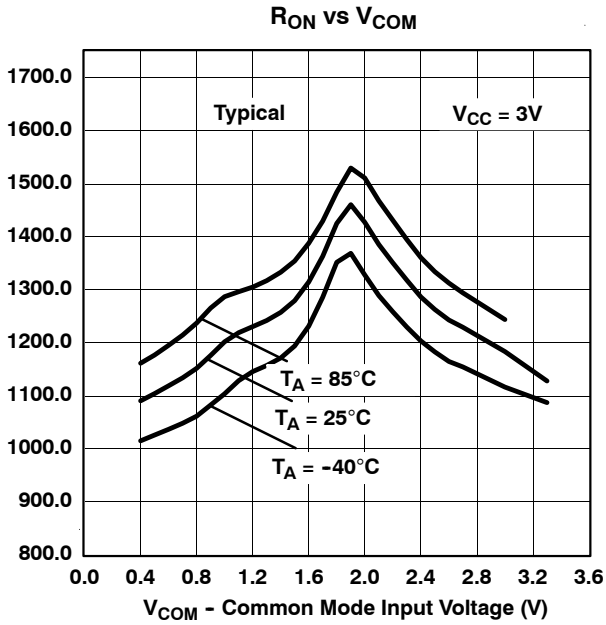


Figure 30

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

Timer_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V		8	MHz
			3 V		10	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

Timer_B

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V		8	MHz
			3 V		10	
$t_{TB,cap}$	Timer_B, capture timing	TB0, TB1, TB2	2.2 V/3 V	20		ns

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baudrate in MBaud) (see Note 1)		2.2V /3 V	2			MHz
t_{τ}	UART receive deglitch time (see Note NO TAG)		2.2 V	50	150		ns
			3 V	50	100		ns

NOTES: 1. The DCO wake-up time must be considered in LPM3/4 for baudrates above 1 MHz.
2. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

USCI (SPI master mode) (see Figure 31 and Figure 32)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLKm Duty cycle = 50% ± 10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		ns
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0		ns
			3 V	0		ns
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	ns

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 33 and Figure 34)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			ns
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			ns
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	ns

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

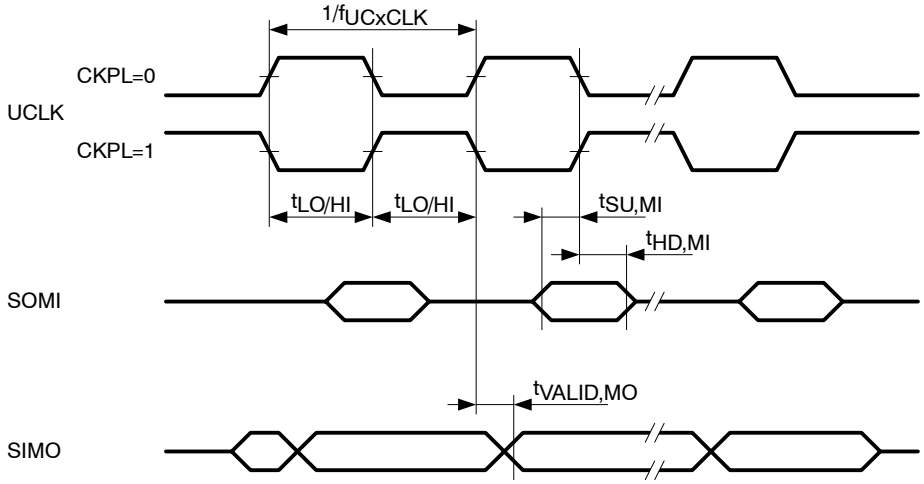


Figure 31. SPI Master Mode, CKPH = 0

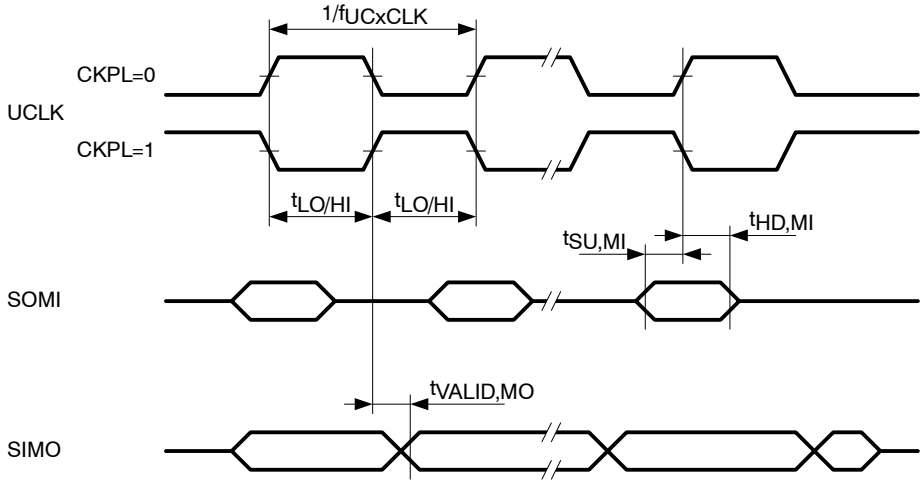


Figure 32. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

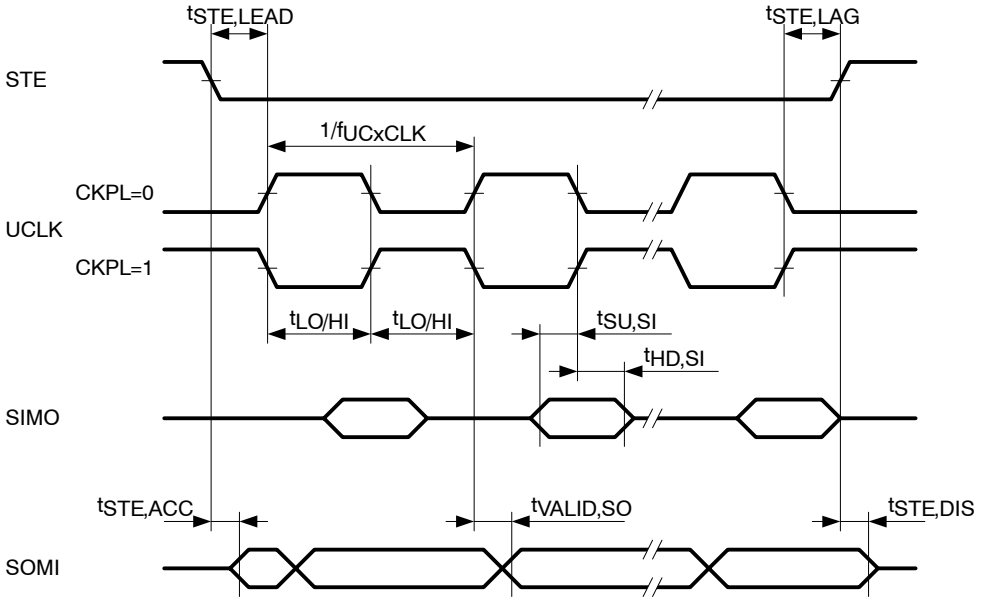


Figure 33. SPI Slave Mode, CKPH = 0

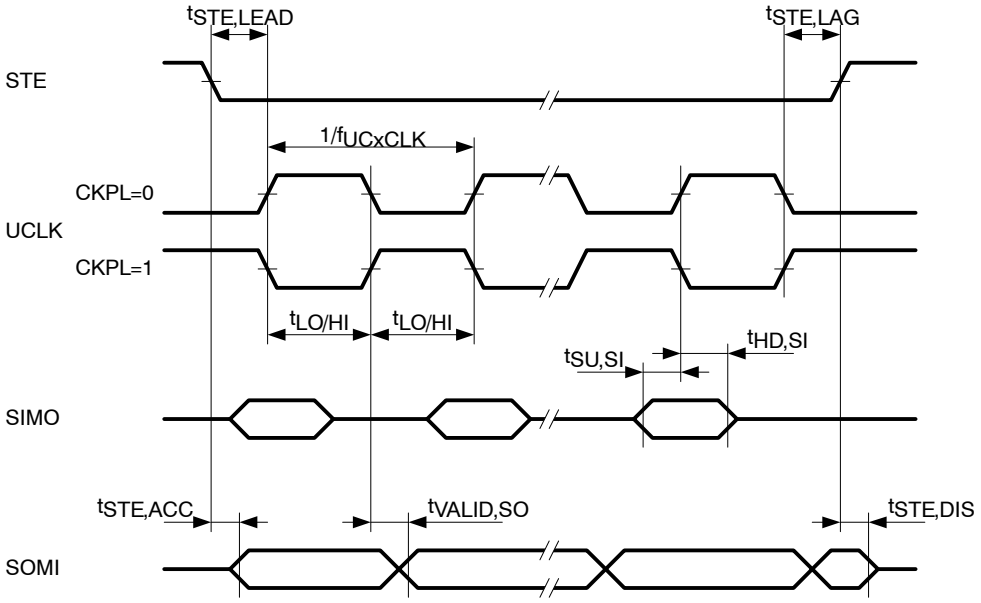


Figure 34. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I2C mode) (see Figure 35)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.0			μs
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			μs
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.7			μs
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			μs
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4.0			μs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	ns

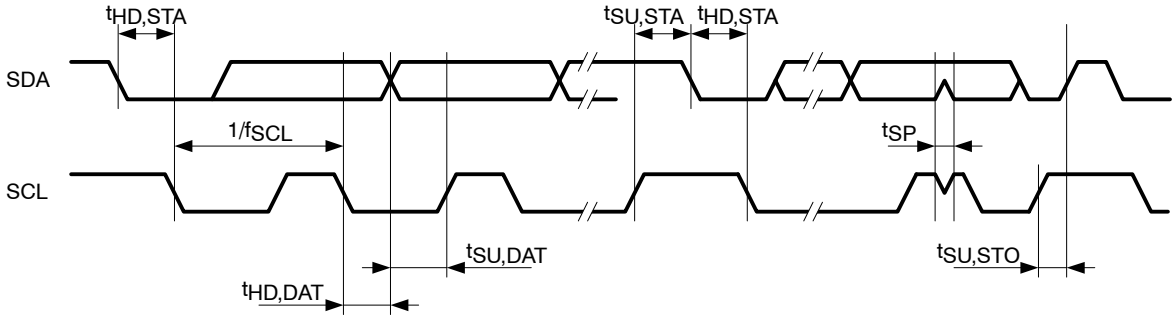


Figure 35. I2C Mode Timing

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.5 V/3.6V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.5 V/3.6V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.5 V/3.6V			10	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.5 V/3.6V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	See Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

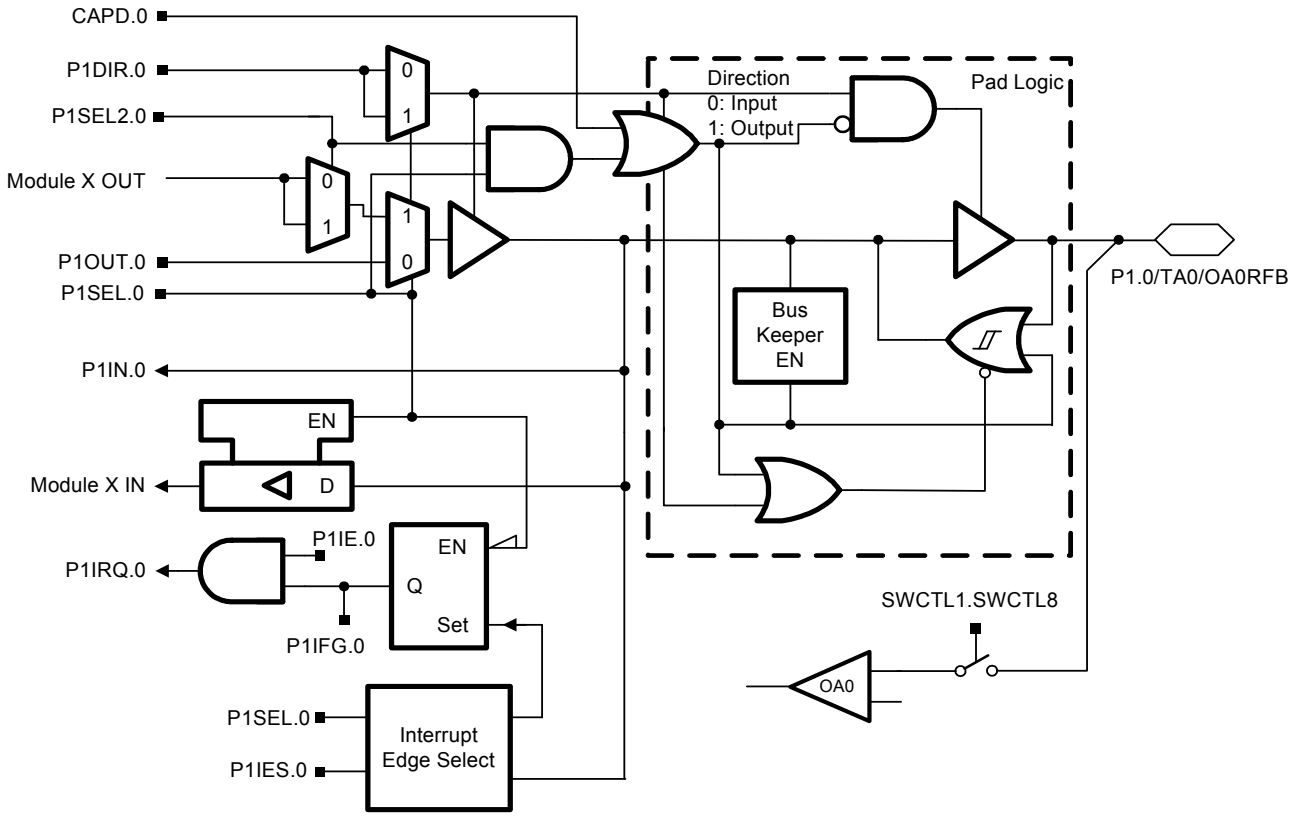
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow				100	mA
t_{FB}	Time to blow fuse				1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

Port P1 pin schematic: P1.0, input/output with Schmitt trigger

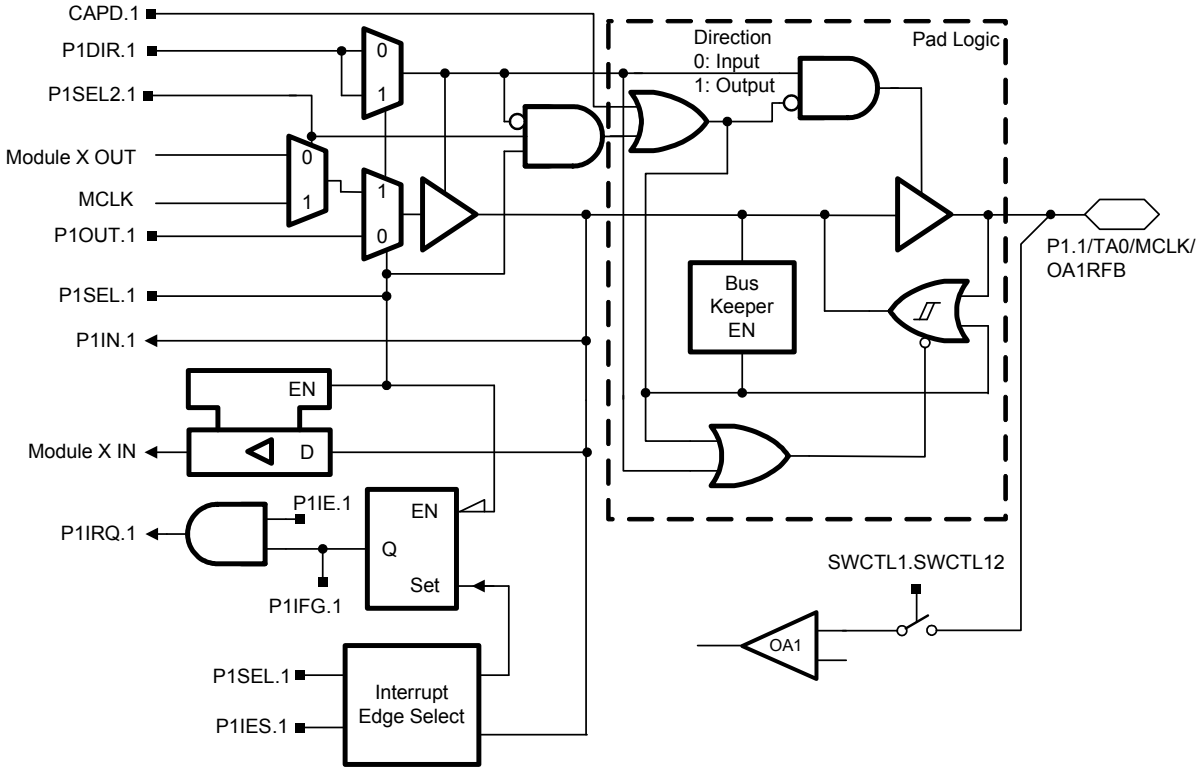


Port P1 (P1.0) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/TA0/OA0RFB	0	P1.x (I/O)	0	I: 0, O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0
		OA0RFB	x	x	1	1

APPLICATION INFORMATION

Port P1 pin schematic: P1.1, input/output with Schmitt trigger

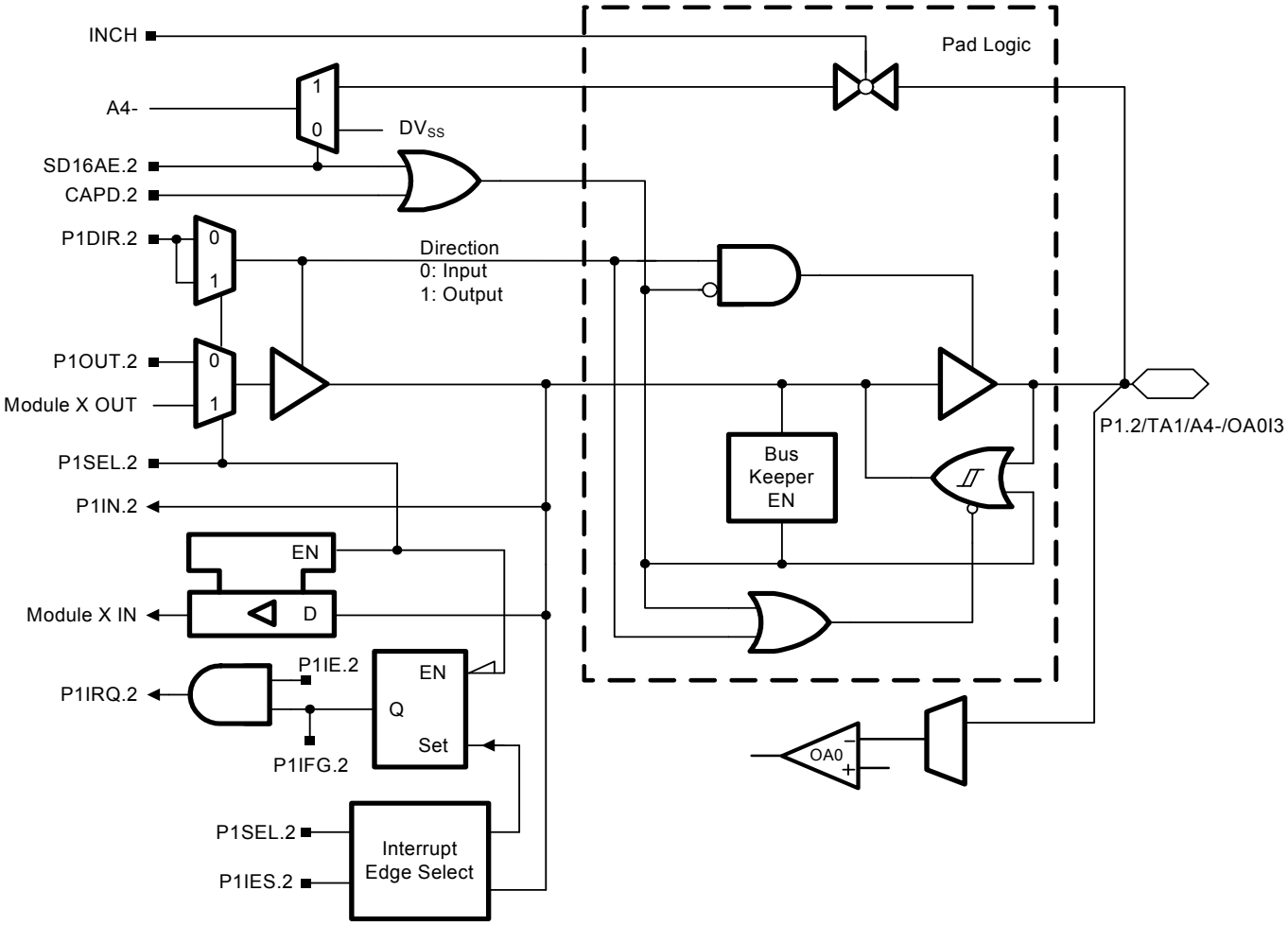


Port P1 (P1.1) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.1/TA0/MCLK OA1RFB	1	P1.x (I/O)	0	I: 0, O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0
		OA1RFB	x	0	1	1
		MCLK	0	1	1	1

APPLICATION INFORMATION

Port P1 pin schematic: P1.2 input/output with Schmitt trigger



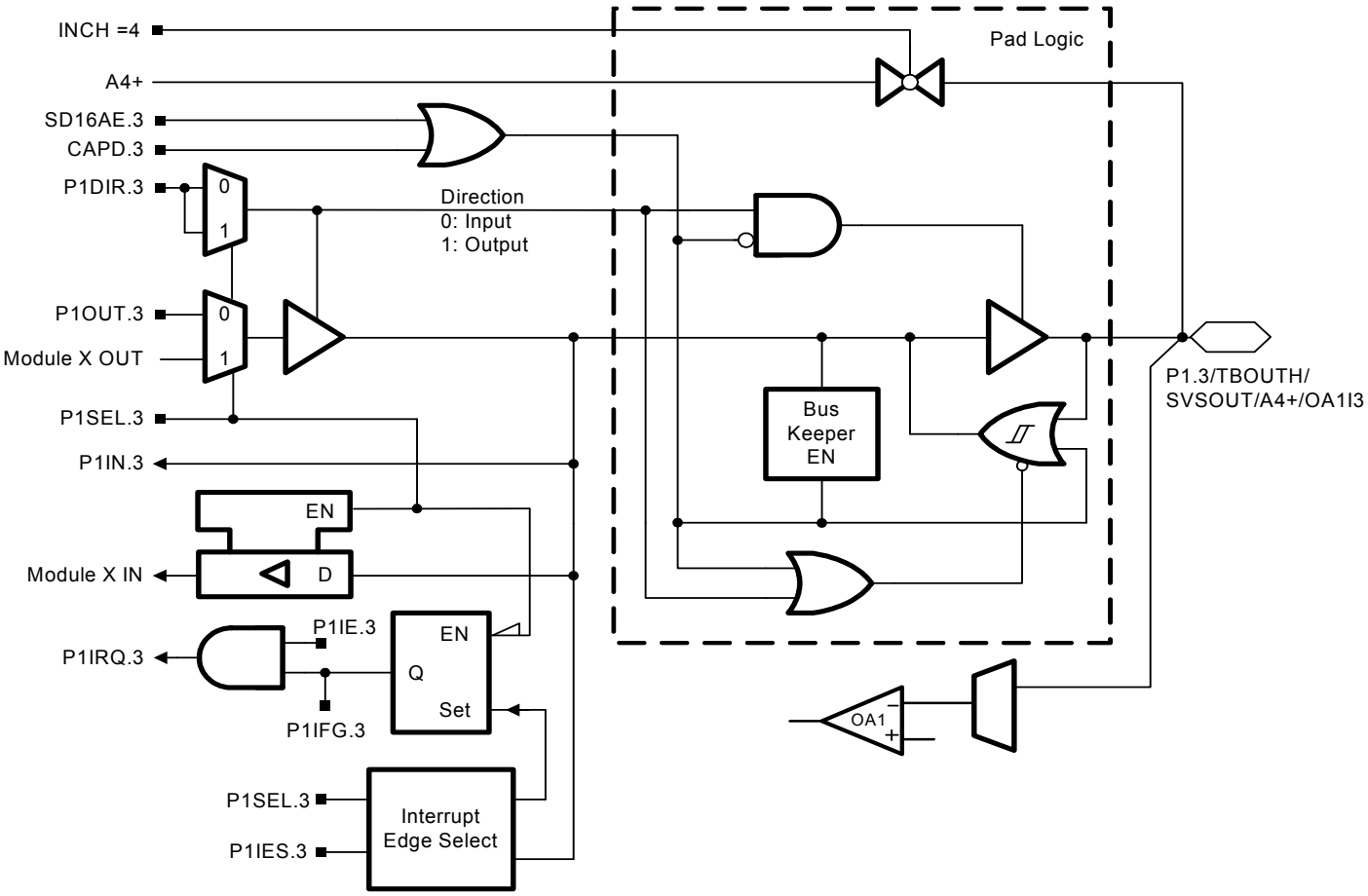
Port P1 (P1.2) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 OAN (OA0)	P1SEL2.x = 0 SD16AE.x
P1.2/TA1/A4-/OA0I3	2	P1.x (I/O)	0	I: 0, O: 1	0	xx	0
		Timer_A3.CCI1A	0	0	1	xx	0
		Timer_A3.TA1	0	1	1	xx	0
		A4-	x	x	x	xx	1
		OA0I3	x	x	x	10	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P1 pin schematic: P1.3, input/output with Schmitt trigger



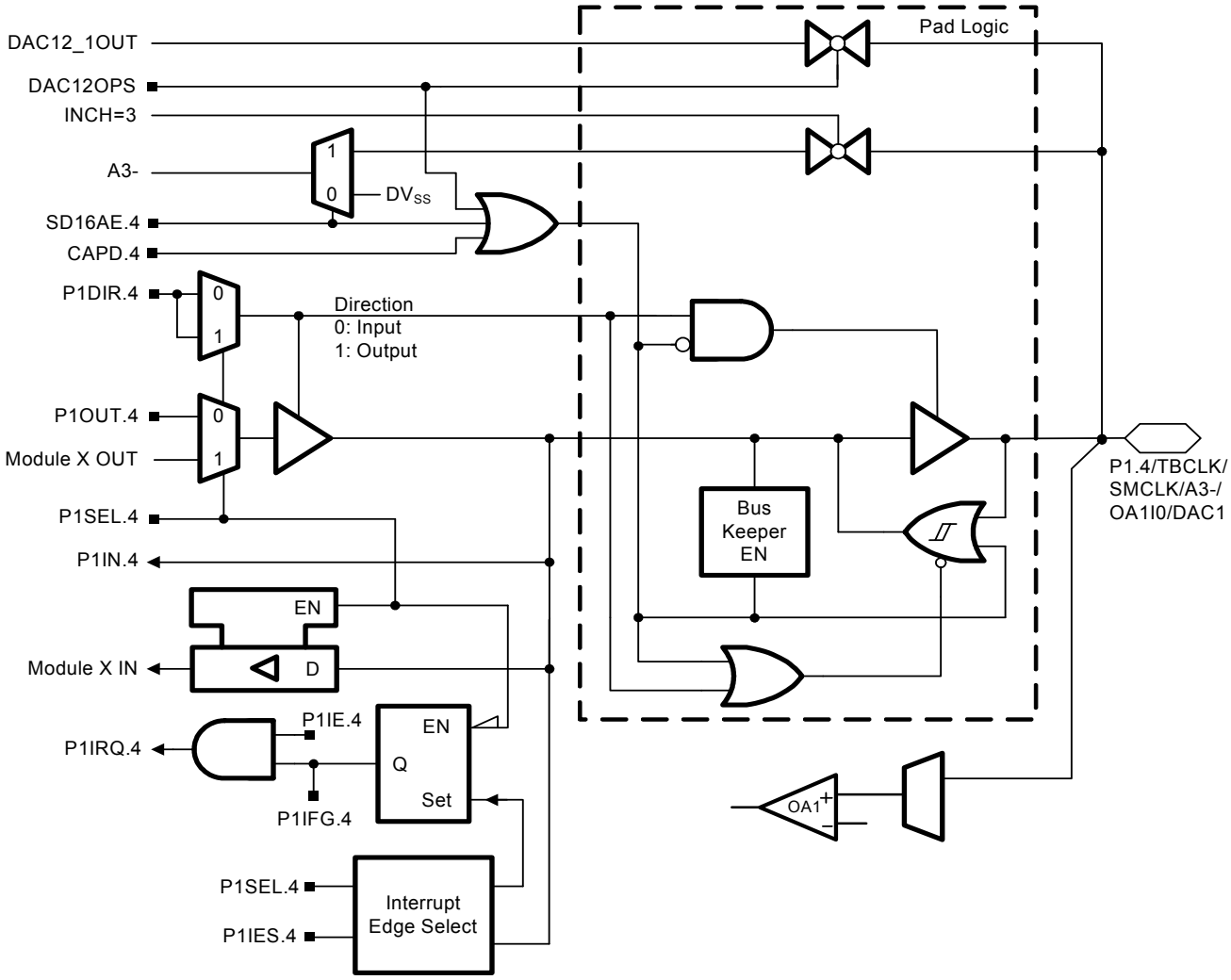
Port P1 (P1.3) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 OAN (OA1)	P1SEL2.x = 0 SD16AE.x
P1.3/TBOUTH/ SVSOUT/A4+/OA1I3	3	P1.x (I/O)	0	I: 0, O: 1	0	xx	0
		TBOUTH	0	0	1	xx	0
		SVSOUT	0	1	1	xx	0
		A4+	x	x	x	xx	1
		OA1I3	x	x	x	10	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P1 pin schematic: P1.4, input/output with Schmitt trigger



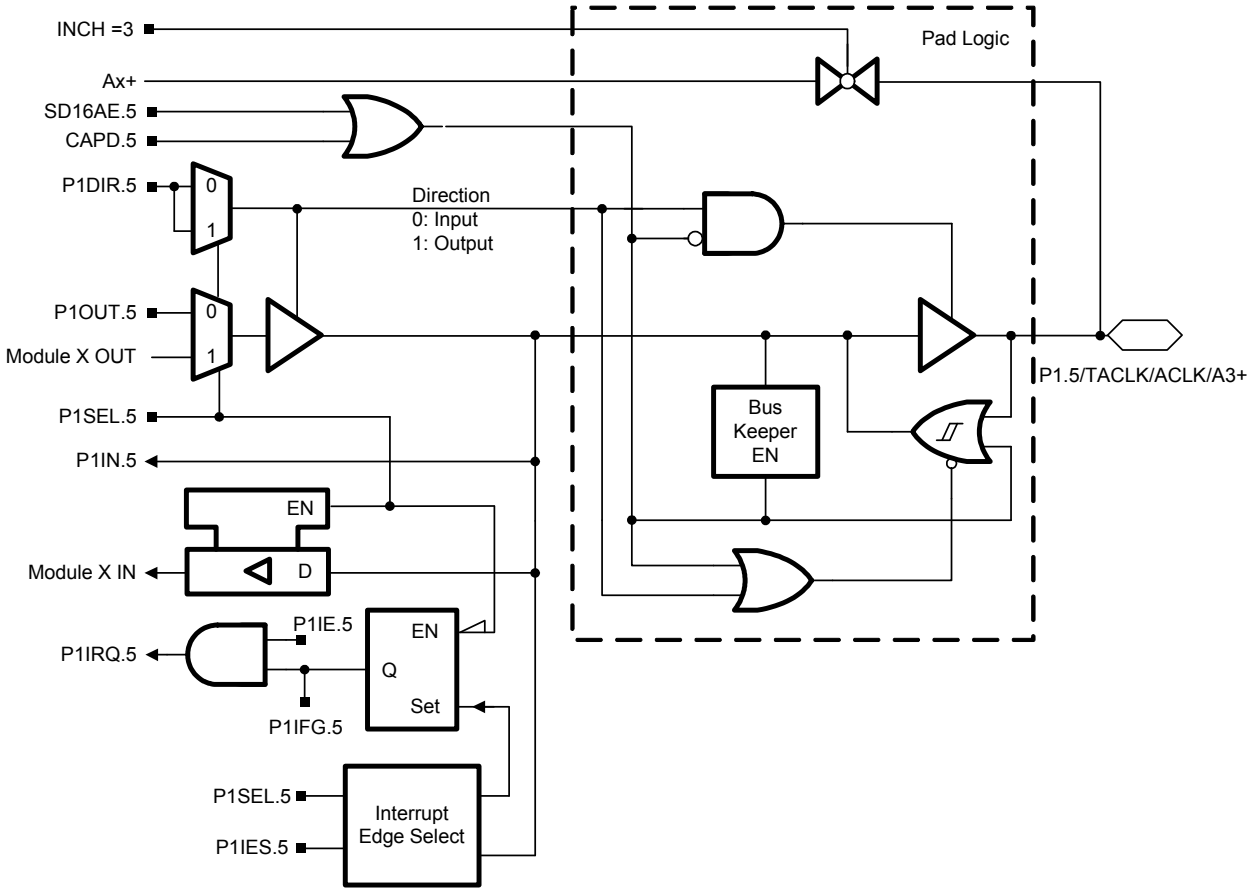
Port P1 (P1.4) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x	P1SEL2.x = 0 OAP (OA1)	P1SEL2.x = 0 DAC12OPS (DAC12_1)
P1.4TBCLK/SMCLK/ A3–/OA1I0/DAC1	4	P1.x (I/O)		I: 0, O: 1	0	0	xx	0
		TBCLK		0	1	0	xx	0
		SMCLK		1	1	0	xx	0
		A3–		x	x	1	xx	0
		OA1I0		x	x	1	00	0
		DAC1		x	x	x	xx	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P1 pin schematic: P1.5, input/output with Schmitt trigger



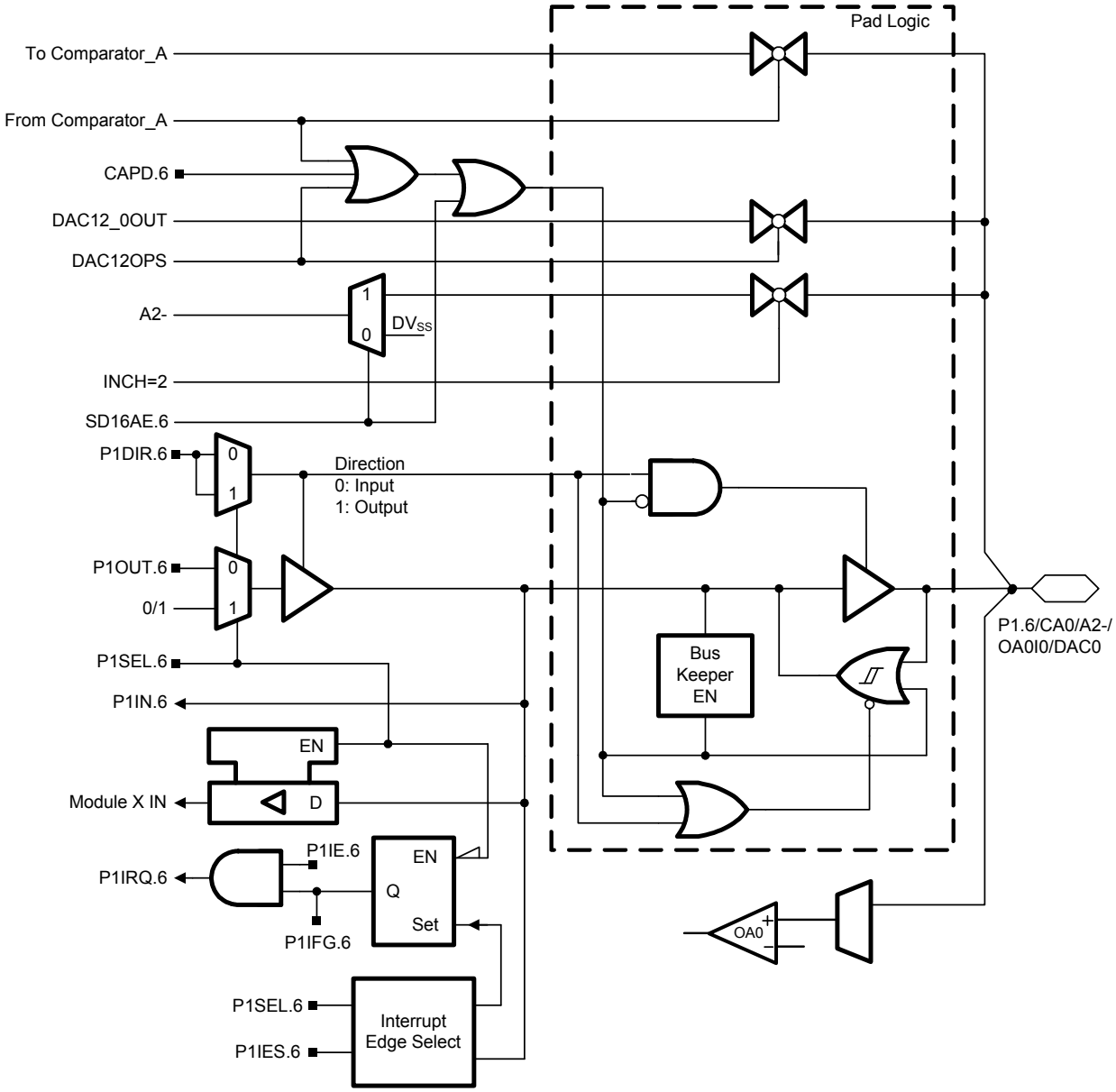
Port P1 (P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.5/TACLK/ACLK/ A3+	5	P1.x (I/O)	0	I: 0, O: 1	0	0
		TACLK	0	0	1	0
		ACLK	0	1	1	0
		A3+	x	x	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P1 pin schematic: P1.6, input/output with Schmitt trigger



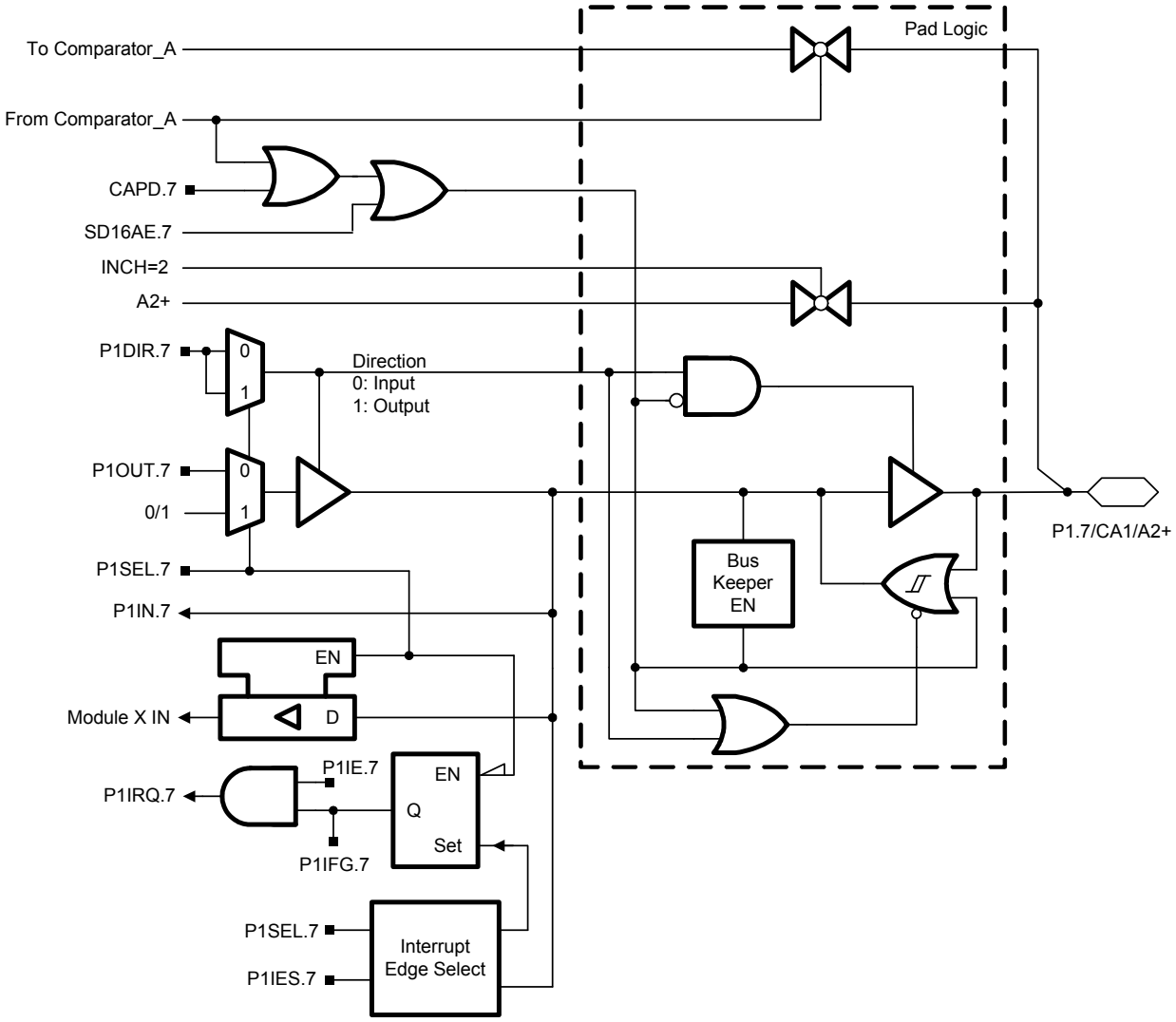
Port P1 (P1.6) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P1DIR.x	P1SEL.x	P1SEL2.x = 0 CAPD.x	P1SEL2.x = 0 SD16AE.x	P1SEL2.x = 0 OAP (OA0)	P1SEL2.x = 0 DAC12OPS (DAC12_0)
P1.6/CA0/A2–/OA0I0/ DAC0	6	P1.x (I/O)	I: 0, O: 1	0	0	0	xx	0
		CA0	x	x	1 or selected	x	xx	x
		A2–	x	x	x	1	xx	x
		OA0I0	x	x	x	x	00	x
		DAC0	x	x	x	x	xx	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P1 pin schematic: P1.7, input/output with Schmitt trigger



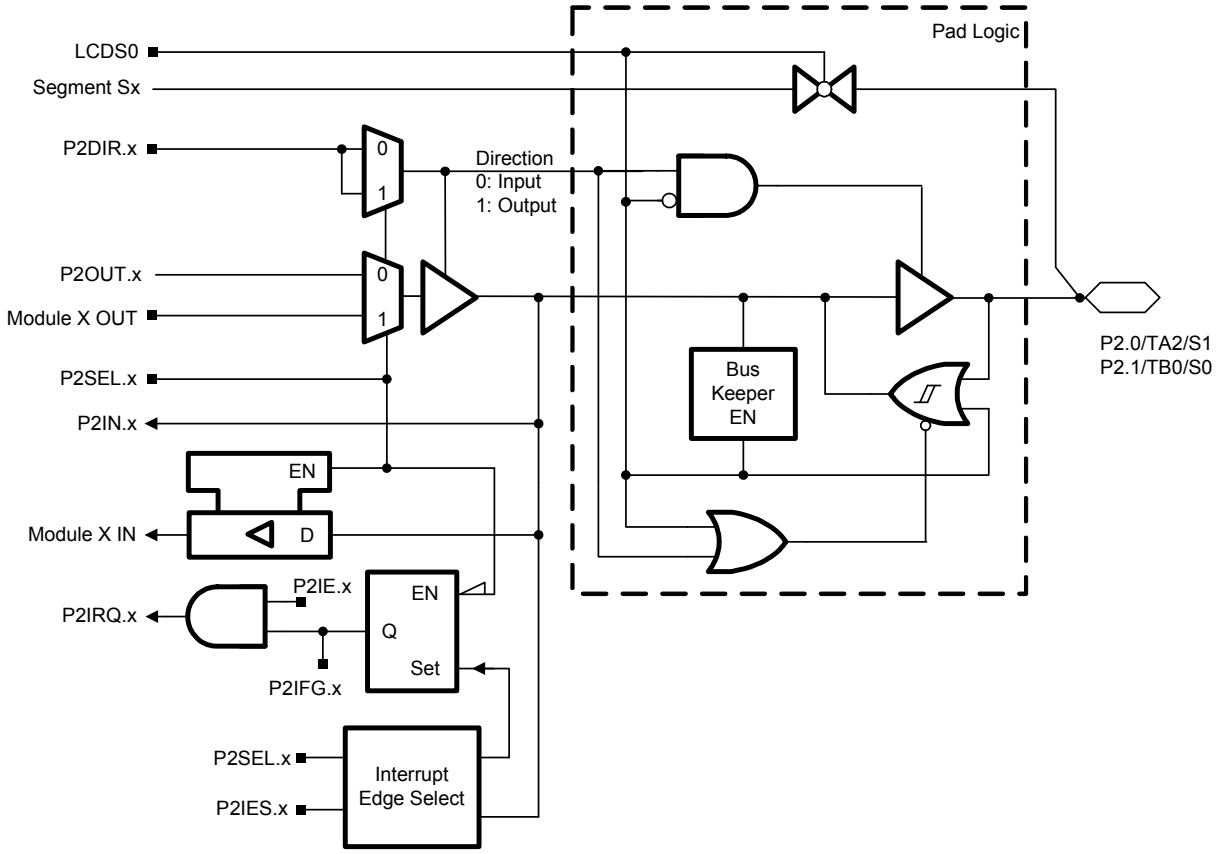
Port P1 (P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	P1SEL2.x = 0 CAPD.x	P1SEL2.x = 0 SD16AE.x
P1.7/CA1/A2+	7	P1.x (I/O)	I: 0, O: 1	0	0	0
		CA1	x	x	1 or selected	x
		A2+	x	x	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P2 pin schematic: P2.0 to P2.1, input/output with Schmitt trigger



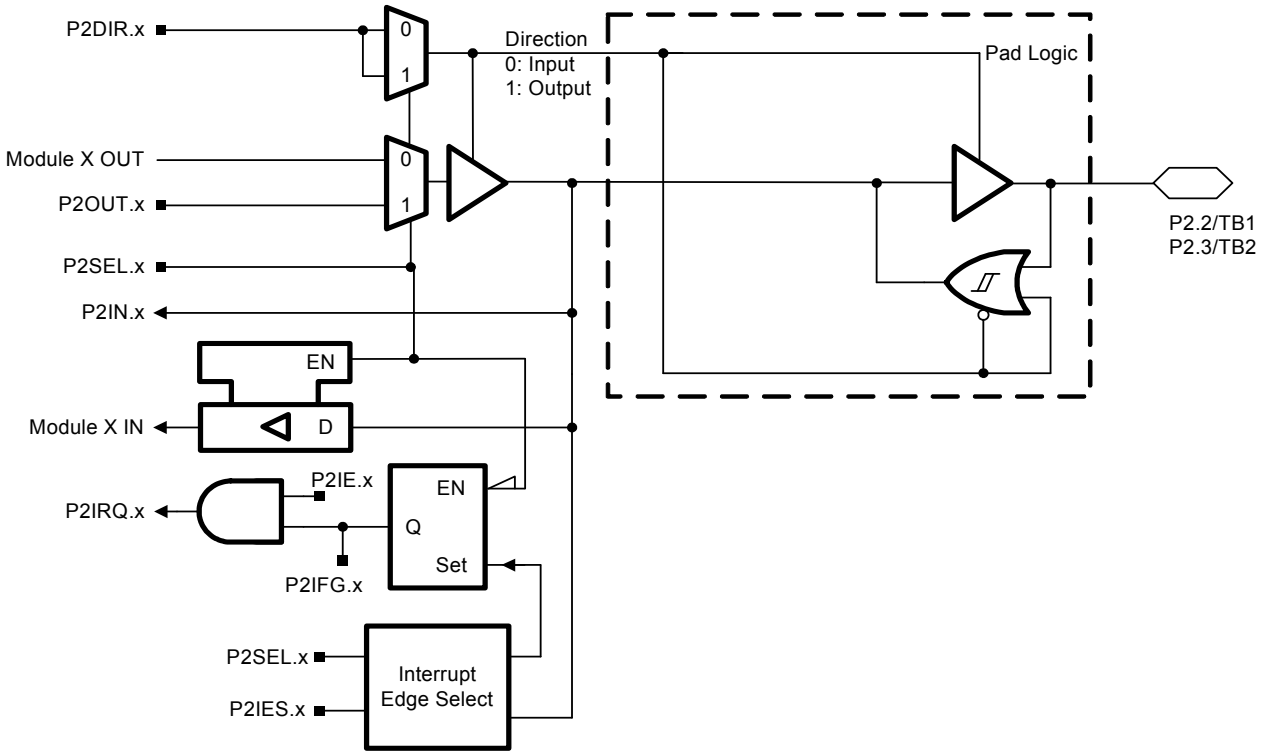
Port P2 (P2.0 to P2.1) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS0
P2.0/TA2/S1	0	P2.x (I/O)	I: 0, O: 1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		S1	x	x	1
P2.1/TB0/S0	1	P2.x (I/O)	I: 0, O: 1	0	0
		Timer_B3.CCI0A	0	1	0
		Timer_B3.TB0	1	1	0
		S0	x	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P2 pin schematic: P2.2 to P2.3, input/output with Schmitt trigger

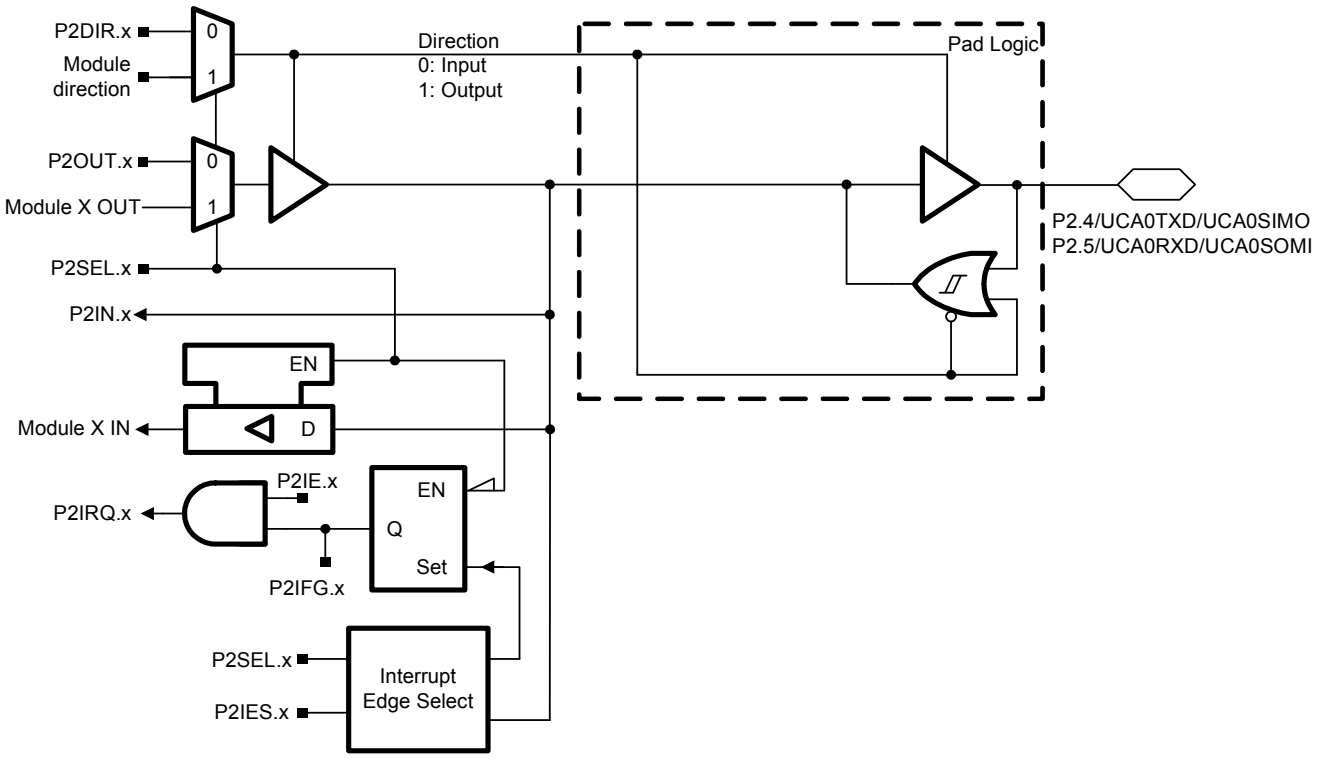


Port P2 (P2.2 to P2.3) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.2/TB1	2	P2.x (I/O)	I: 0, O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P2.3/TB2	3	P2.x (I/O)	I: 0, O: 1	0
		Timer_B3.CCI2A	0	1
		TimerB3.TB2	1	1

APPLICATION INFORMATION

Port P2 pin schematic: P2.4 and P2.5, input/output with Schmitt trigger



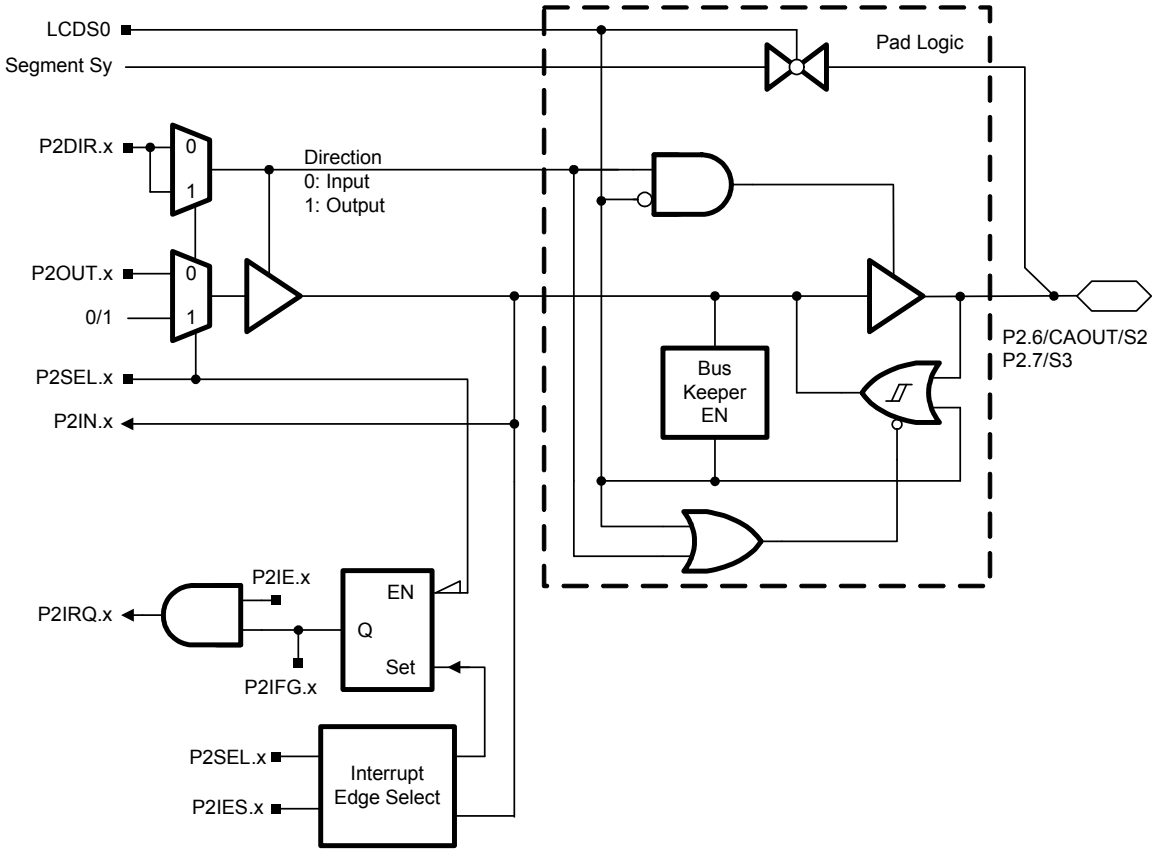
Port P2 (P2.4 and P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD/ UCA0SIMO	4	P2.x (I/O)	I: 0, O: 1	0
		UCA0TXD/UCA0SIMO (see Notes 2)	x	1
P2.5/UCA0RXD/ UCA0SOMI	5	P2.x (I/O)	I: 0, O: 1	0
		UCA0RXD/UCA0SOMI (see Notes 2)	x	1

NOTES: 1. x: Don't care.
2. The pin direction is controlled by the USCI module.

APPLICATION INFORMATION

Port P2 pin schematic: P2.6 and P2.7, inpututput with Schmitt trigger



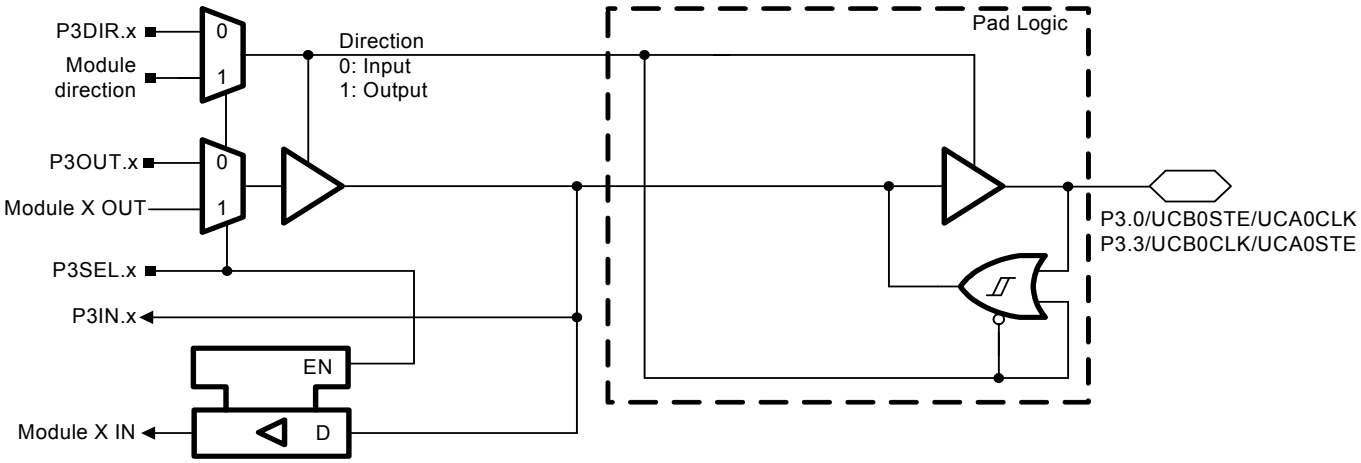
Port P2 (P2.6 and P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS0
P2.6/CAOUT/S2	6	P2.x (I/O)	I: 0, O: 1	0	0
		CAOUT	1	1	0
		S2	x	x	1
P2.7/S3	7	P2.x (I/O)	I: 0, O: 1	0	0
		V_{ss}	1	1	0
		S3	x	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P3 pin schematic: P3.0 and P3.3, input/output with Schmitt trigger



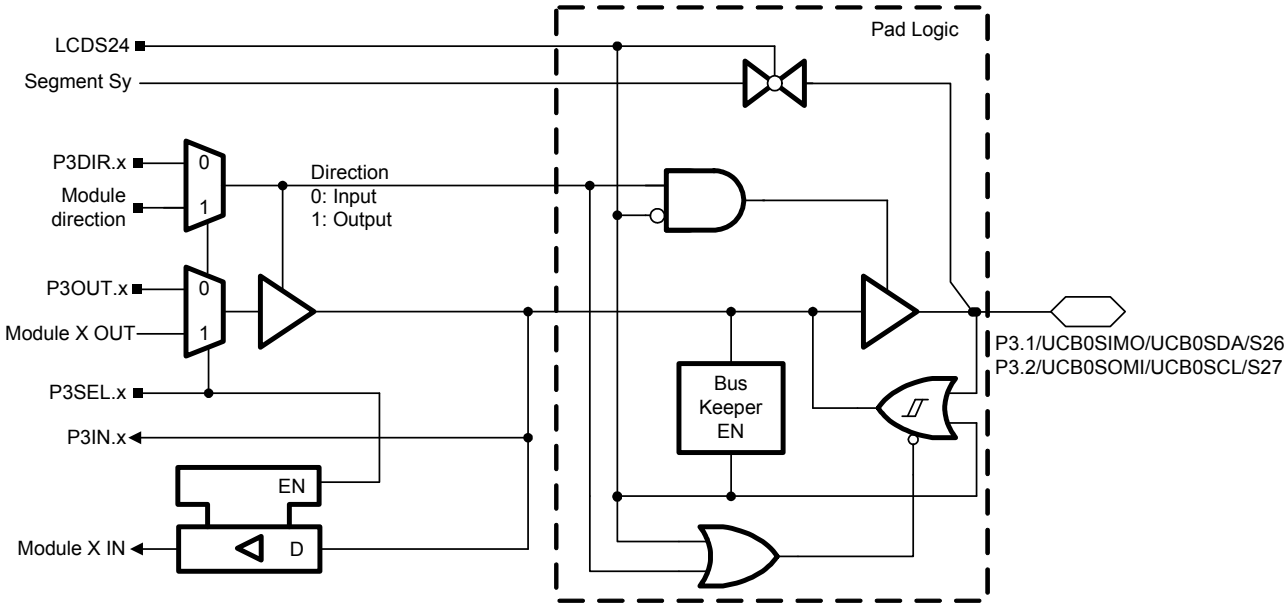
Port P3 (P3.0 and P3.3) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/ UCA0CLK	0	P3.x (I/O)	I: 0, O: 1	0
		UCB0STE/UCA0CLK (see Note 2)	x	1
P3.3/UCB0CLK/ UCA0STE	3	P3.x (I/O)	I: 0, O: 1	0
		UCB0CLK/UCA0STE (see Note 2)	x	1

NOTES: 1. x: Don't care.
2. The pin direction is controlled by the USCI module.

APPLICATION INFORMATION

Port P3 pin schematic: P3.1 and P3.2, input/output with Schmitt trigger



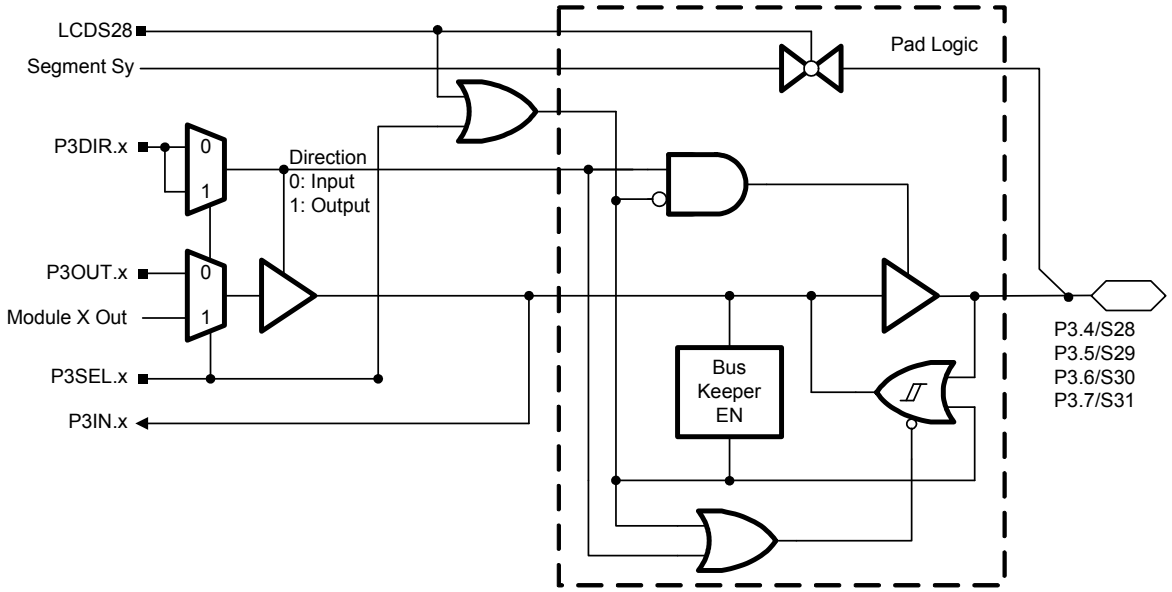
Port P3 (P3.1 and P3.2) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P3DIR.x	P3SEL.x	LCDS24
P3.1/UCB0SIMO/ UCB0SDA/S26	1	P3.x (I/O)	I: 0, O: 1	0	0
		UCB0SIMO/UCB0SDA (see Notes 2 and 3)	x	1	0
		S26	x	x	1
P3.2/UCB00SOMI/ UCB0SCL/S27	2	P3.x (I/O)	I: 0, O: 1	0	0
		UCB0SOMI/UCB0SCL (see Notes 2 and 3)	x	1	0
		S27	x	x	1

NOTES: 1. x: Don't care.
2. The pin direction is controlled by the USCI module.
3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

APPLICATION INFORMATION

Port P3 pin schematic: P3.4 to P3.7, input/output with Schmitt trigger



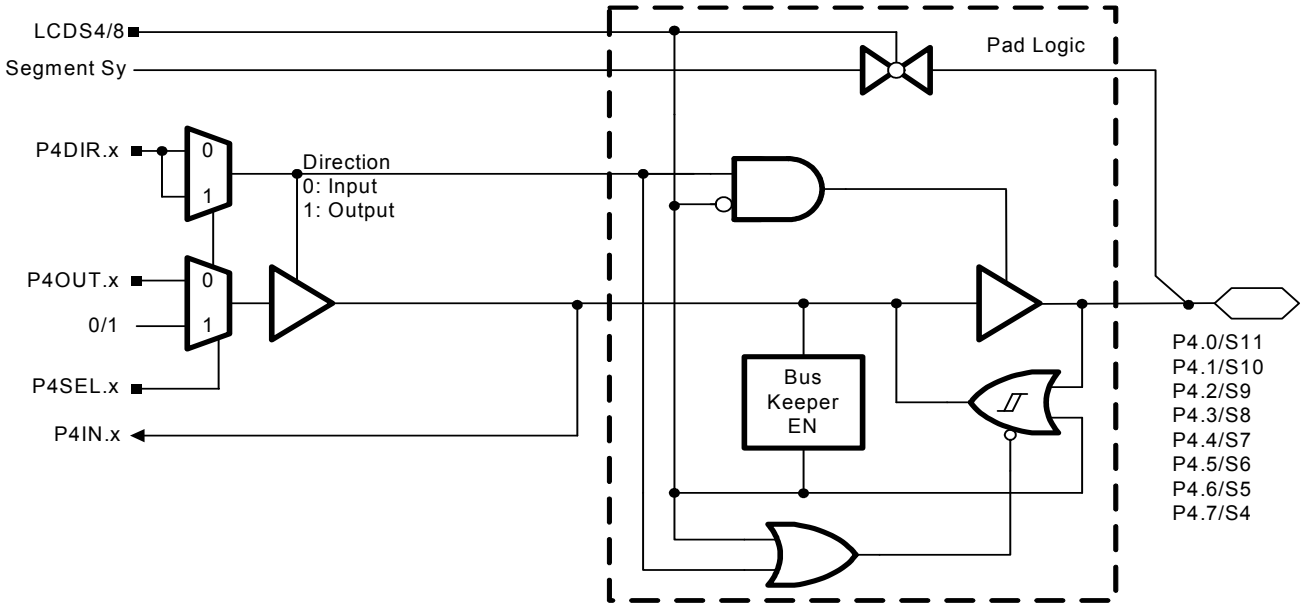
Port P3 (P3.4 to P3.7) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P3DIR.x	P3SEL.x	LCDS28
P3.4/S28	4	P3.x (I/O)	I: 0, O: 1	0	0
		S28	x	x	1
P3.5/S29	5	P3.x (I/O)	I: 0, O: 1	0	0
		S29	x	x	1
P3.6/S30	6	P3.x (I/O)	I: 0, O: 1	0	0
		S30	x	x	1
P3.7/S31	7	P3.x (I/O)	I: 0, O: 1	0	0
		S31	x	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P4 pin schematic: P4.0 to P4.7, input/output with Schmitt trigger



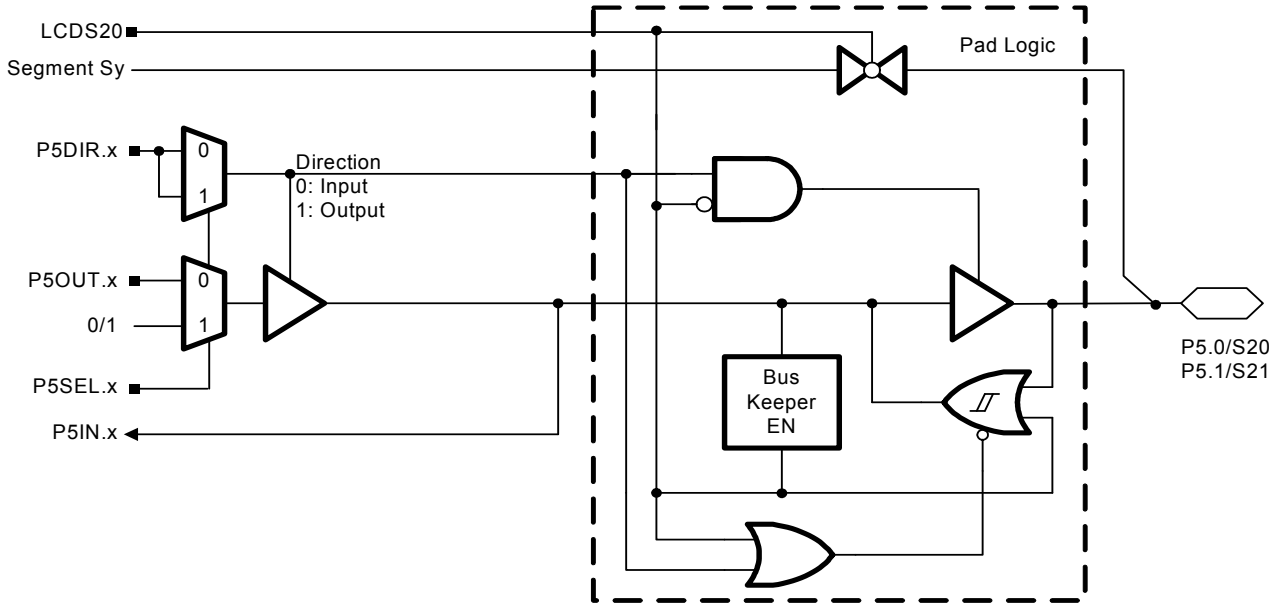
Port P4 (P4.0 and P4.7) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS4/8
P4.0/S11	0	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S11	x	x	1 (LCDS8)
P4.1/S10	1	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S10	x	x	1 (LCDS8)
P4.2/S9	2	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S9	x	x	1 (LCDS8)
P4.3/S8	3	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS8)
		S8	x	x	1 (LCDS8)
P4.4/S7	4	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S7	x	x	1 (LCDS4)
P4.5/S6	5	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S6	x	x	1 (LCDS4)
P4.6/S5	6	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S5	x	x	1 (LCDS4)
P4.7/S4	7	P4.x (I/O)	I: 0, O: 1	0	0 (LCDS4)
		S4	x	x	1 (LCDS4)

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P5 pin schematic: P5.0 and P5.1, input/output with Schmitt trigger



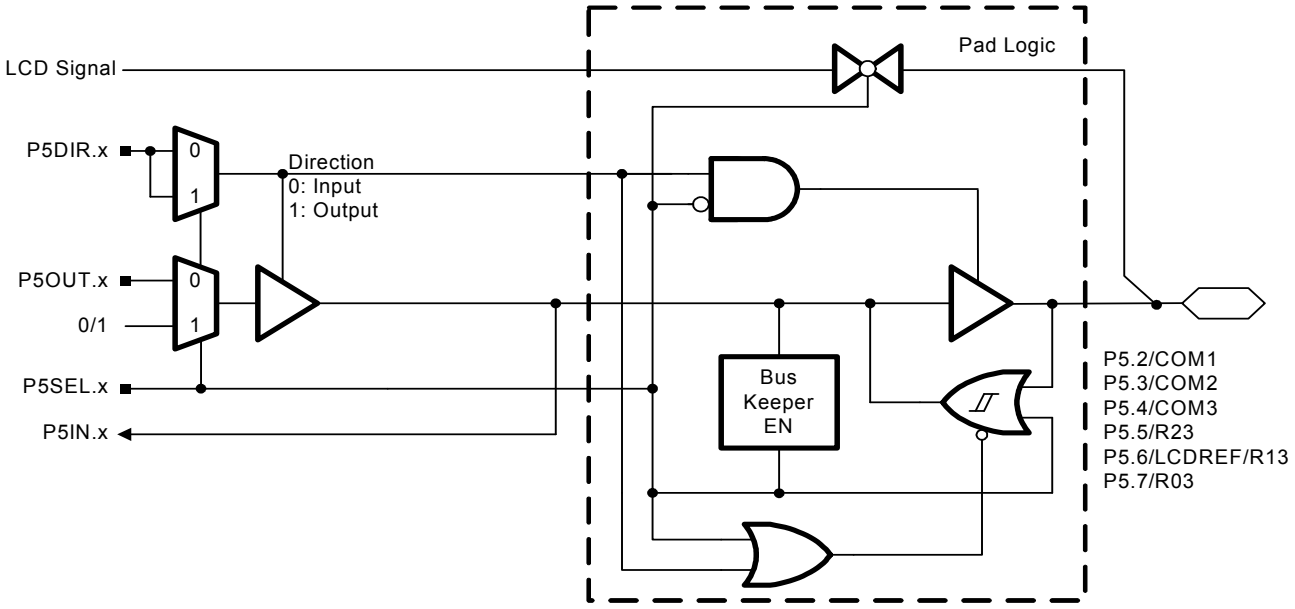
Port P5 (P5.0 and P5.1) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS20
P5.0/S20	0	P5.x (I/O)	I: 0, O: 1	0	0
		S20	x	x	1
P5.1/S21	1	P5.x (I/O)	I: 0, O: 1	0	0
		S21	x	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P5 pin schematic: P5.2 to P5.7, input/output with Schmitt trigger



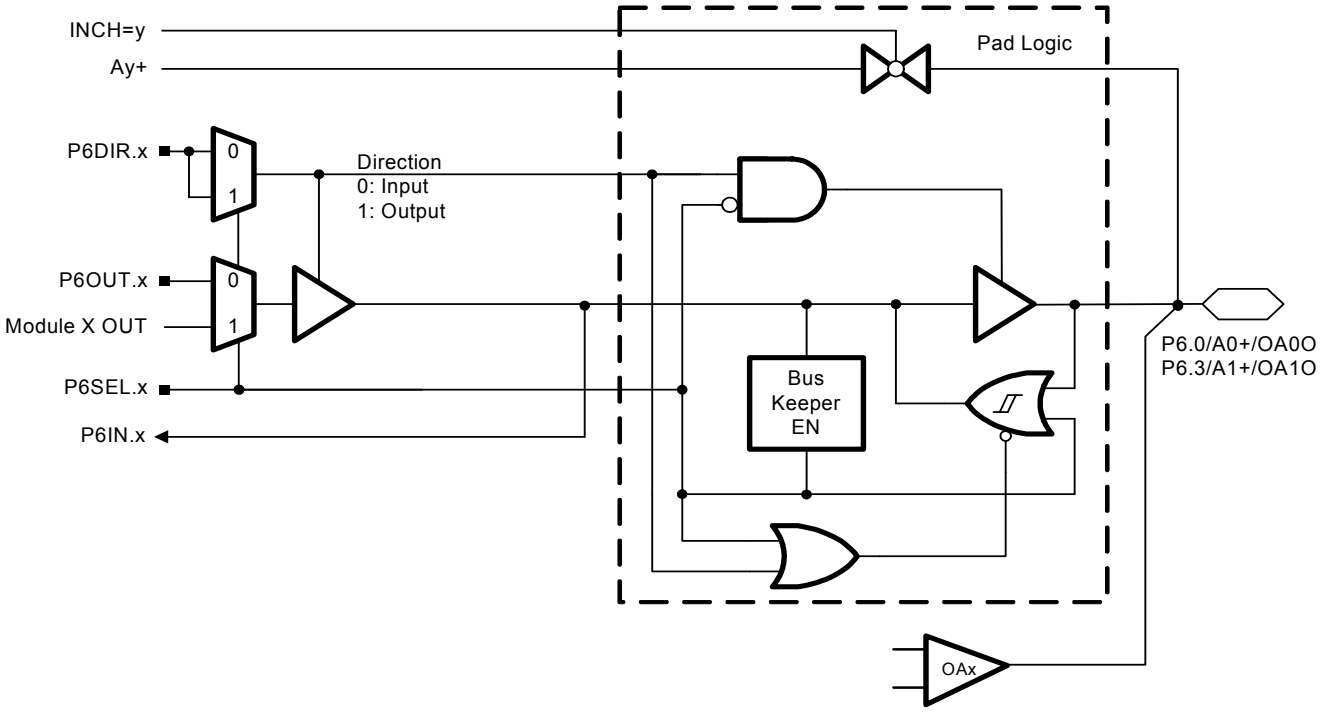
Port P5 (P5.2 to P5.7) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.x (I/O)	I: 0, O: 1	0
		COM1	x	1
P5.3/COM2	3	P5.x (I/O)	I: 0, O: 1	0
		COM2	x	1
P5.4/COM3	4	P5.x (I/O)	I: 0, O: 1	0
		COM3	x	1
P5.5/R23	5	P5.x (I/O)	I: 0, O: 1	0
		R23	x	1
P5.6/LCDREF/R13	6	P5.x (I/O)	I: 0, O: 1	0
		R13 or LCDREF	x	1
P5.7/R03	7	P5.x (I/O)	I: 0, O: 1	0
		R03	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P6 pin schematic: P6.0 and P6.3, input/output with Schmitt trigger



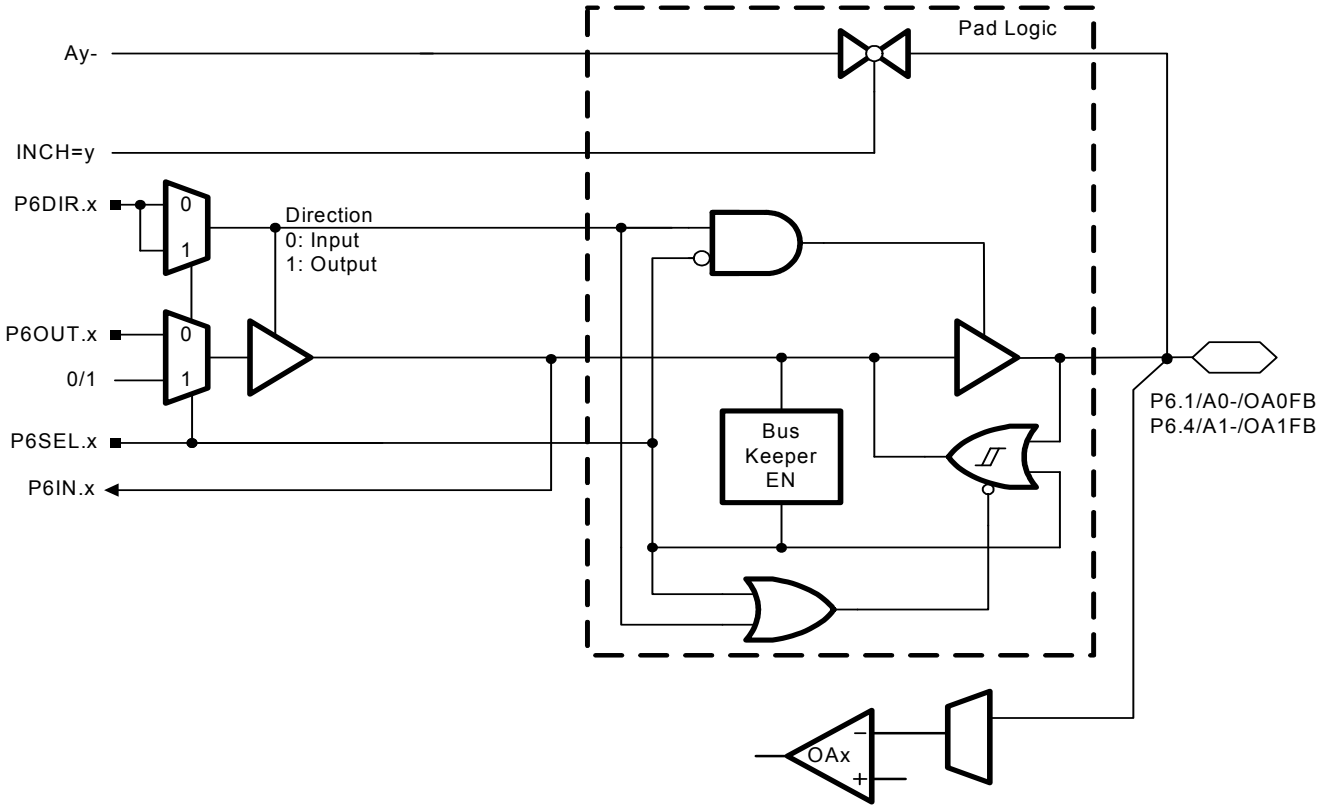
Port P6 (P6.0 and P6.3) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.0/A0+/OA0O	0	P6.x (I/O)	I: 0, O: 1	0
		A0+	x	1
		OA0O	x	1
P6.3/A1+/OA1O	3	P6.x (I/O)	I: 0, O: 1	0
		A1+	x	1
		OA1O	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P6 pin schematic: P6.1 and P6.4, input/output with Schmitt trigger



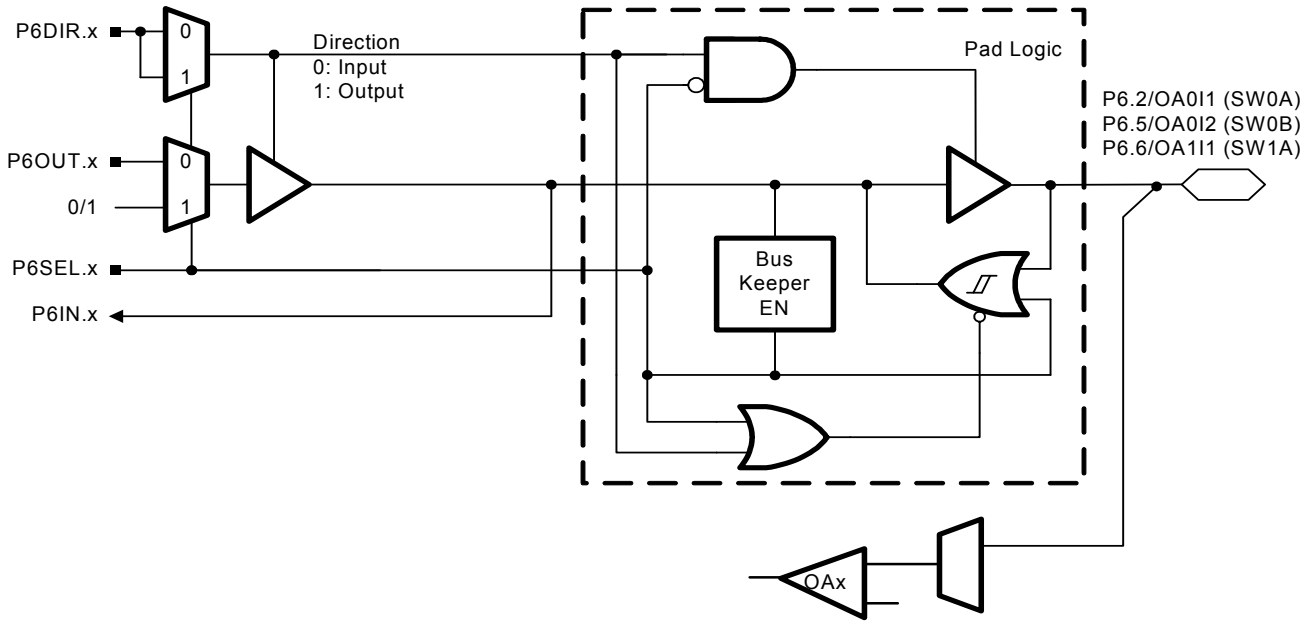
Port P6 (P6.1 and P6.4) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.1/A0–/OA0FB	1	P6.x (I/O)	I: 0, O: 1	0
		A0–	x	1
		OA0FB	x	1
P6.4/A1–/OA1FB	4	P6.x (I/O)	I: 0, O: 1	0
		A1–	x	1
		OA1FB	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P6 pin schematic: P6.2, P6.5 and P6.6, input/output with Schmitt trigger



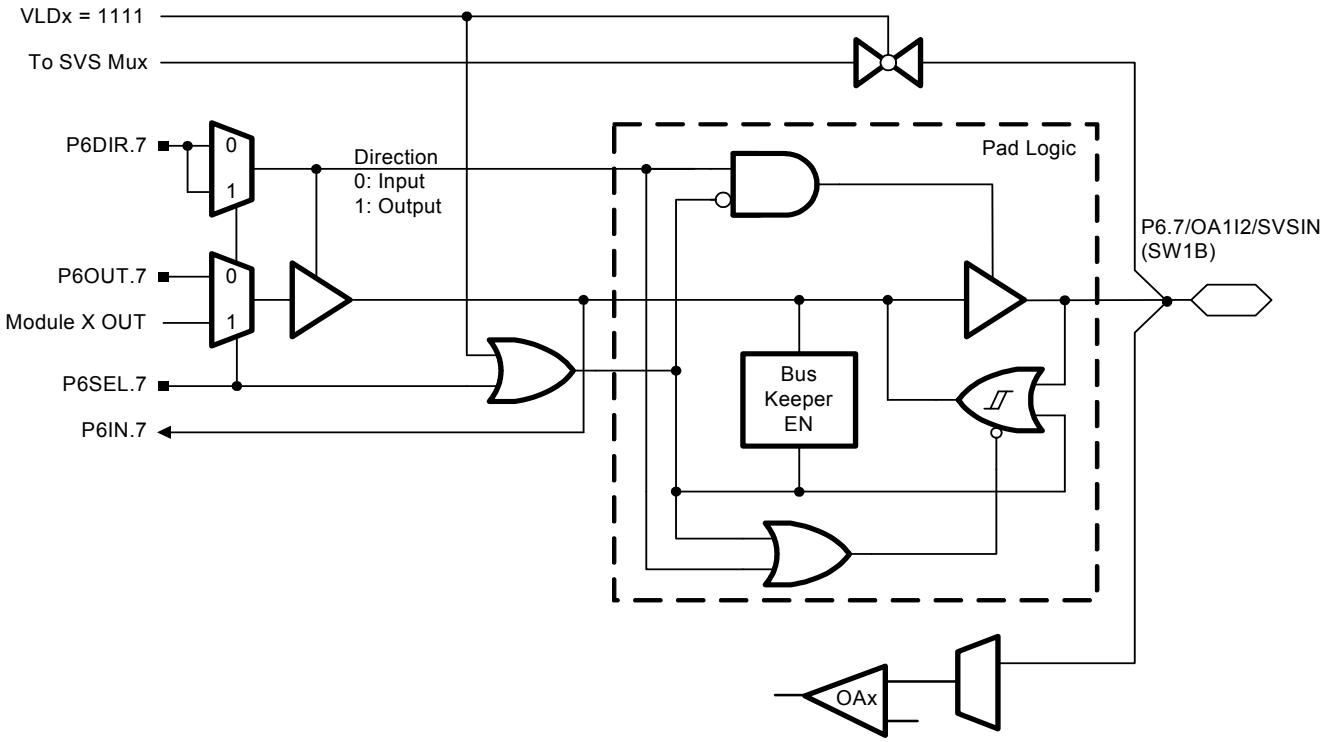
Port P6 (P6.2, P6.5 and P6.6) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.2/OA0I1	2	P6.x (I/O)	I: 0, O: 1	0
		OA0I1	x	1
P6.5/OA0I2	5	P6.x (I/O)	I: 0, O: 1	0
		OA0I2	x	1
P6.6/OA1I1	6	P6.x (I/O)	I: 0, O: 1	0
		OA1I1	x	1

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

Port P6 pin schematic: P6.7, input/output with Schmitt trigger



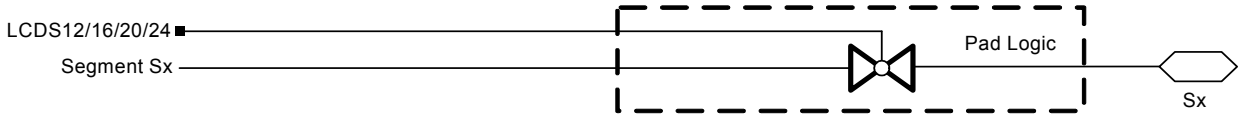
Port P6 (P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	VLDx
P6.7/OA1I2/SVSIN	7	P6.x (I/O)	I: 0, O: 1	0	x
		OA1I2	x	1	x
		SVSIN	x	1	1111

NOTES: 1. x: Don't care.

APPLICATION INFORMATION

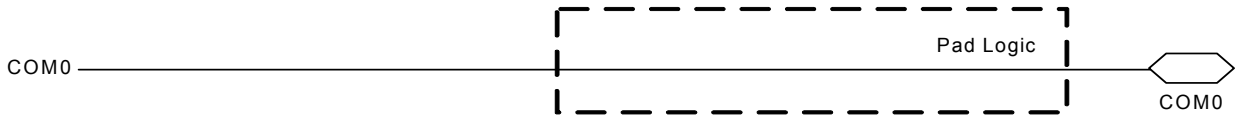
Segment pin schematic: Sx, dedicated Segment Pins



Sx pin functions

PIN NAME	X	FUNCTION	CONTROL BITS / SIGNALS
			LCDSy
Sx	12	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	13	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	14	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	15	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	16	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	17	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	18	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	19	Sx	1 (LCDS16)
		3-state	0 (LCDS16)
Sx	22	Sx	1 (LCDS20)
		3-state	0 (LCDS20)
Sx	23	Sx	1 (LCDS20)
		3-state	0 (LCDS20)
Sx	24	Sx	1 (LCDS24)
		3-state	0 (LCDS24)
Sx	25	Sx	1 (LCDS24)
		3-state	0 (LCDS24)

Segment pin schematic: COM0, dedicated COM0 pin

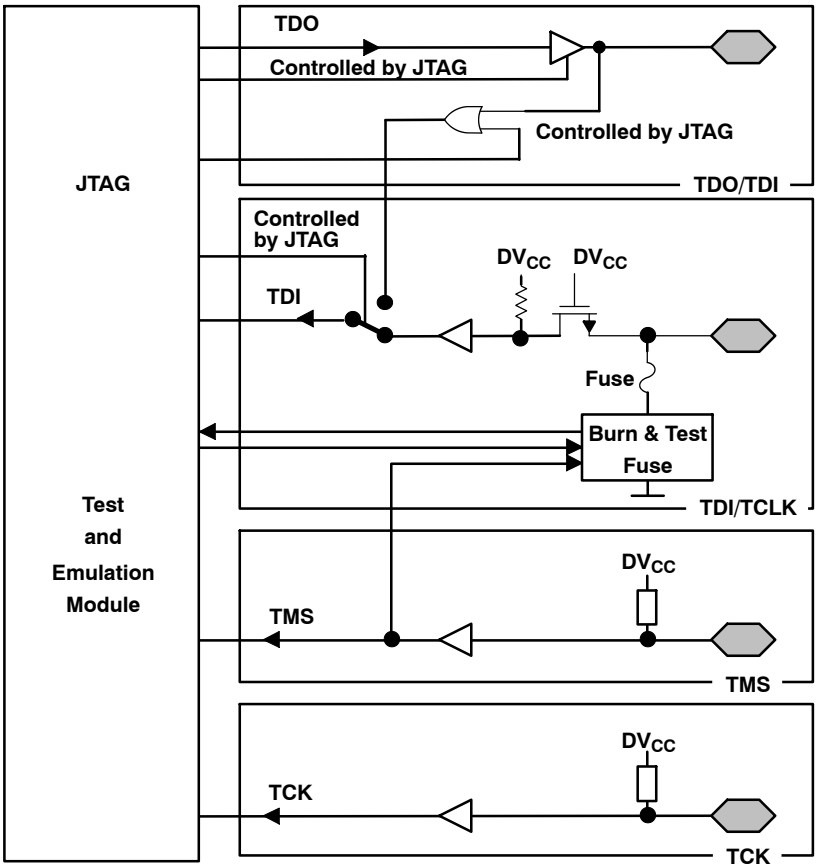


Sx pin functions

PIN NAME	X	FUNCTION
COM0	–	COM0

APPLICATION INFORMATION

JTAG pins: TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

JTAG fuse check mode

For details on the JTAG fuse check mode, see the *MSP430 Memory Programming User's Guide* (SLAU265) chapter "Fuse Check and Reset of the JTAG State Machine (TAP Controller)".

Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS580	Product Preview release
SLAS580A	Changes throughout to update Product Preview
SLAS580B	Production Data release
SLAS580C	In recommended operating conditions table, changed maximum LFXT1 crystal frequency, $f_{(LFXT1)}$, with XT1 selected from 8 MHz to 6 MHz (page 24)
SLAS580D	Changed limits on $t_{d(SVSon)}$ parameter (page 32) Corrected measurement pin name for “Duty cycle, LF mode” parameter (page 37)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FG477IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG477	Samples
MSP430FG477IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG477	Samples
MSP430FG477IZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430FG477	
MSP430FG478IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG478	Samples
MSP430FG478IZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430FG478	
MSP430FG479IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG479	Samples
MSP430FG479IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG479	Samples
MSP430FG479IZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430FG479	
MSP430FG479IZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430FG479	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

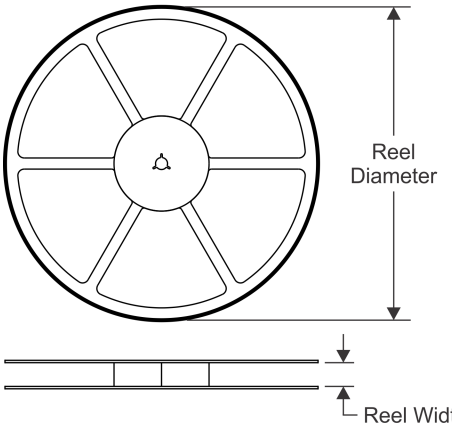
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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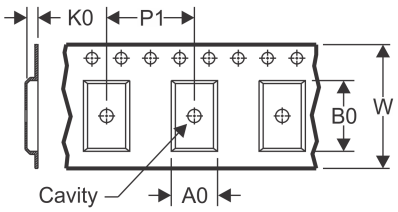
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

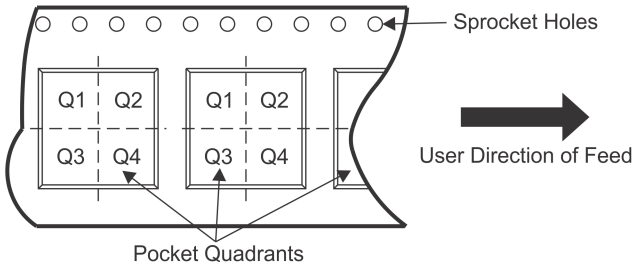


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

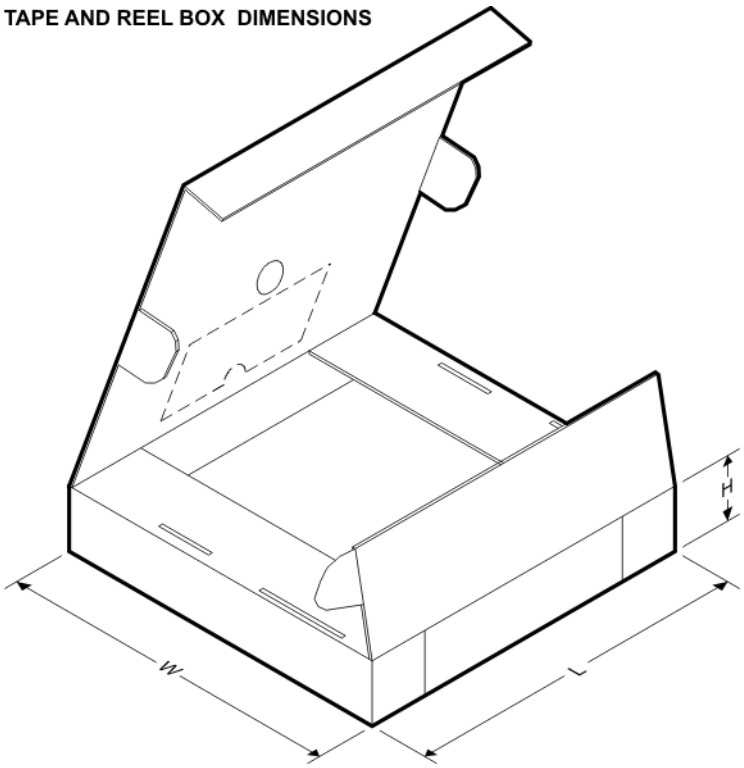
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FG477IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG478IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG479IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

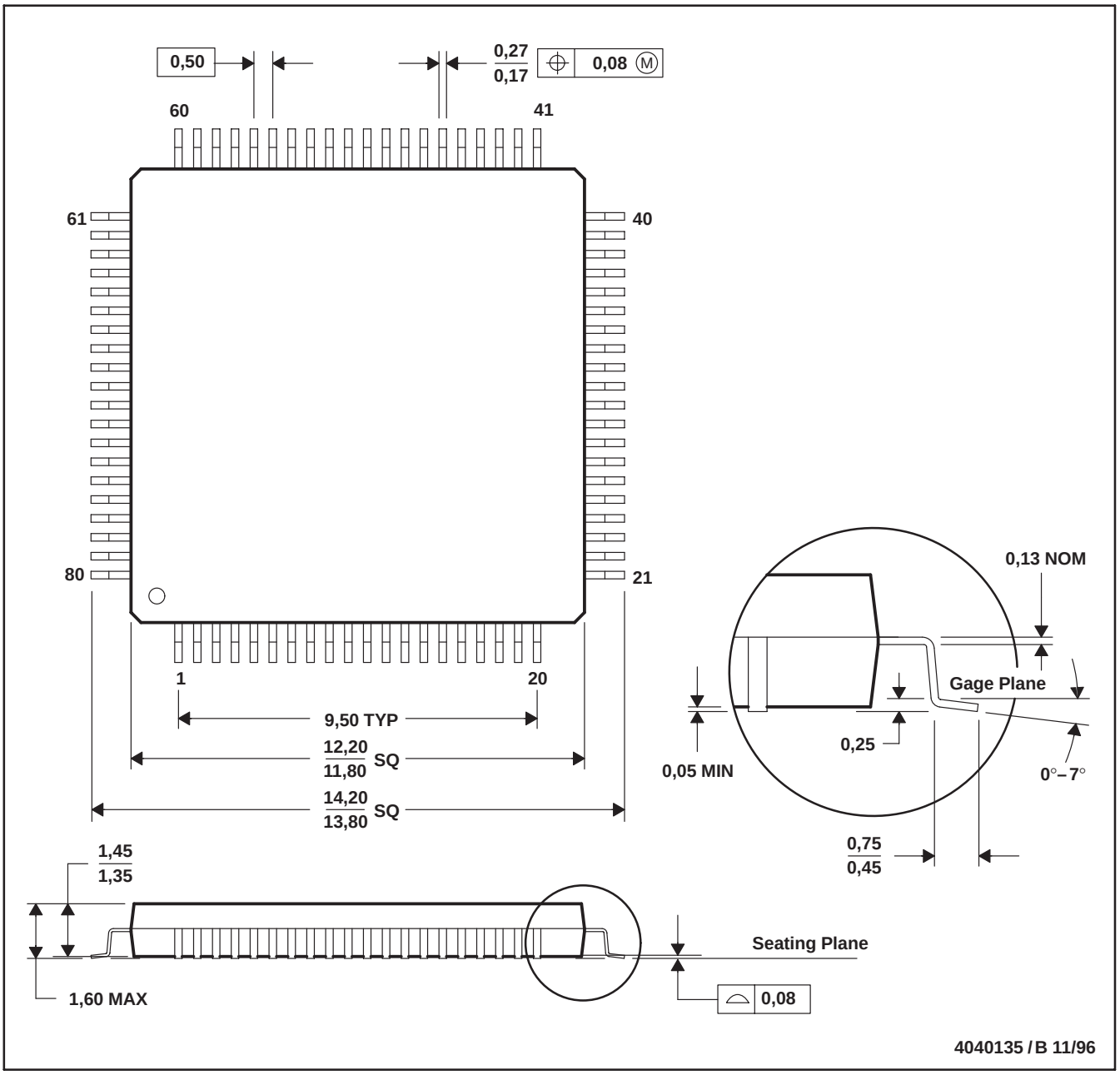


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FG477IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430FG478IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430FG479IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0

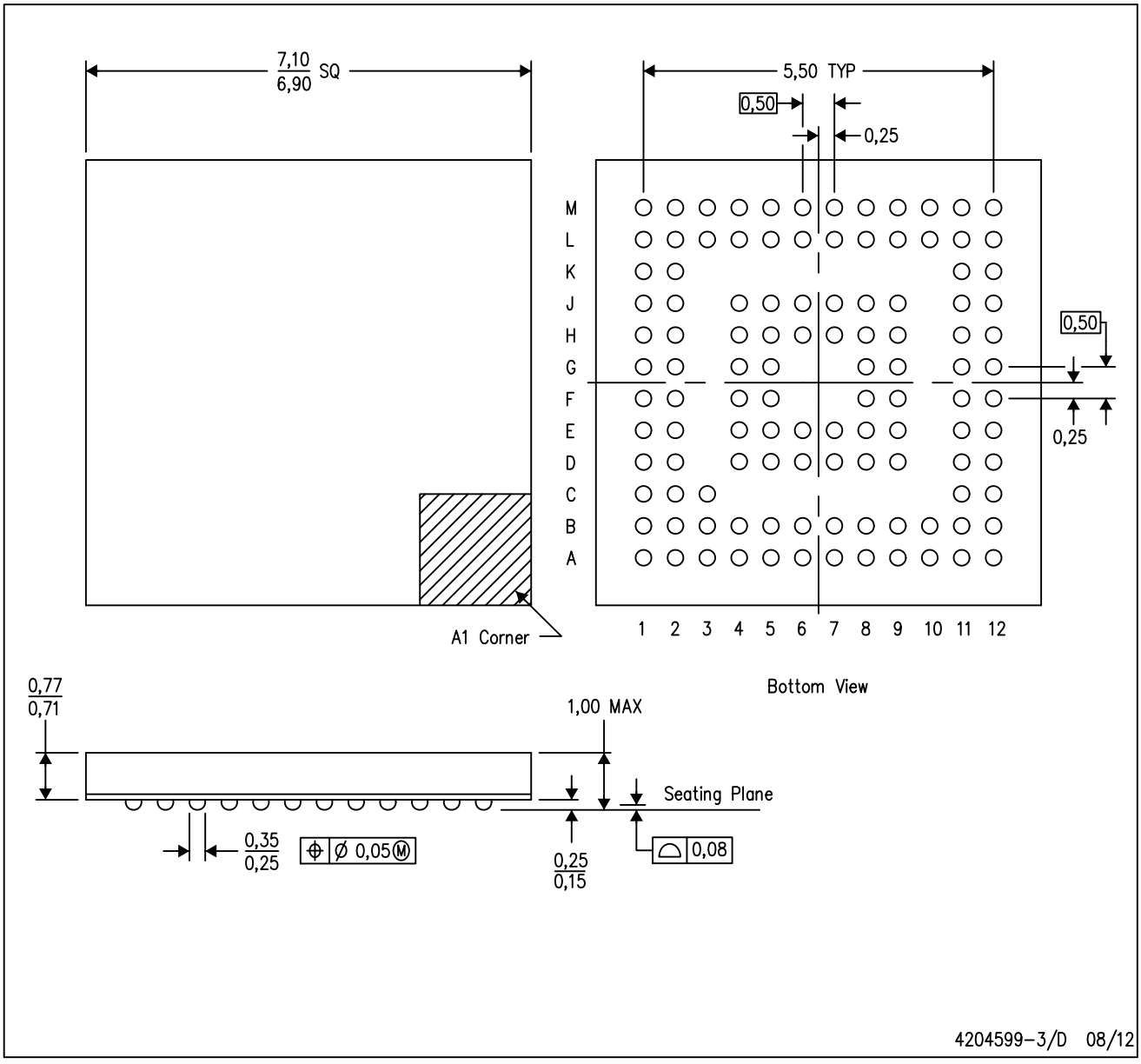
MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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