

目录

1	特性	1	9	Detailed Description	20
2	应用	1	9.1	Overview	20
3	说明	1	9.2	Functional Block Diagram	20
4	修订历史记录	2	9.3	Feature Description	21
5	说明 (续)	4	9.4	Device Functional Modes	22
6	Pin Configuration and Function	5	10	Application and Implementation	23
7	Specifications	6	10.1	Application Information	23
7.1	Absolute Maximum Ratings	6	10.2	Typical Applications	23
7.2	ESD Ratings	6	11	Power Supply Recommendations	33
7.3	Recommended Operating Conditions	6	12	Layout	33
7.4	Thermal Information	6	12.1	Layout Guidelines	33
7.5	Power Ratings	7	12.2	PCB Material	33
7.6	Insulation Characteristics	7	12.3	Layout Example	33
7.7	Safety-Related Certifications	8	13	器件和文档支持	34
7.8	Safety Limiting Values	8	13.1	文档支持	34
7.9	Electrical Characteristics	9	13.2	接收文档更新通知	34
7.10	Switching Characteristics	10	13.3	社区资源	34
7.11	Insulation Characteristics Curves	11	13.4	商标	34
7.12	Typical Characteristics	12	13.5	静电放电警告	34
8	Parameter Measurement Information	18	13.6	Glossary	34
			14	机械、封装和可订购信息	35

4 修订历史记录

Changes from Revision A (June 2015) to Revision B	Page
• 已将标题由“有源安全 特性”更改至“有源保护 功能”	1
• 已将特性“浪涌抗扰度高达 12800V _{PK} (根据 IEC 61000-4-5)”更改为“可承受的浪涌隔离电压达 12800V _{PK} ”	1
• Added the <i>Power Ratings</i> table	7
• Moved <i>Insulation Characteristics</i> to the <i>Specifications</i>	7
• Changed the Test Conditions and values for q_{pd} in <i>Insulation Characteristics</i>	7
• Changed R_{IO} From: $100^{\circ}\text{C} \leq T_A \leq \text{max To: } 100^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ in the <i>Insulation Characteristics</i>	7
• Moved <i>Safety-Related Certifications</i> to the <i>Specifications</i>	8
• Changed the CSA status from planned to certified	8
• Moved <i>Safety Limiting Values</i> to the <i>Specifications</i>	8
• Added the <i>Reinforced High-Voltage Capacitor Life Time Projection</i> figure to <i>Insulation Characteristics Curves</i>	11
• Changed the <i>Thermal Derating Curve for Limiting Current per VDE</i> figure and Added the <i>Thermal Derating Curve for Limiting Power per VDE</i> figure	11
• Added the I_{CC1} <i>Supply Current vs Temperature</i> figure to the <i>Typical Characteristics</i>	13
• Changed the <i>OUT Propagation Delay, Non-Inverting Configuration</i> figure	18
• Changed the <i>OUT Propagation Delay, Inverting Configuration</i> figure	18
• Added text ", but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue." to <i>Supply and Active Miller Clamp</i>	21
• Changed the second paragraph of the <i>Typical Applications</i>	23
• Added text "and $\overline{\text{RST}}$ input signal" to <i>Design Requirements</i>	24
• Deleted text " and a 220-pF filtering capacitor." from <i>Recommended ISO5851 Application Circuit</i>	25
• Deleted text "thereby, providing protection against further catastrophic failures." From: the <i>Global-Shutdown and Reset</i> section	27
• Changed the <i>Normal Operation - Bipolar Supply</i> and <i>Normal Operation - Unipolar Supply</i> figures	32
• Changed the <i>PCB Material</i> section	33

修订历史记录 (接下页)

- 已更改 静电放电注意事项 [34](#)

Changes from Original (June 2015) to Revision A

Page

- 已从单页产品预览更改为完整数据表。 [1](#)

5 说明（续）

如果在由双极输出电源供电的正常运行期间关断 IGBT，输出电压会被硬钳位为 V_{EE2} 。如果输出电源为单极，那么可采用有源米勒钳位，这种钳位会在一条低阻抗路径上灌入米勒电流，从而防止 IGBT 在高电压瞬态条件下发生动态导通。

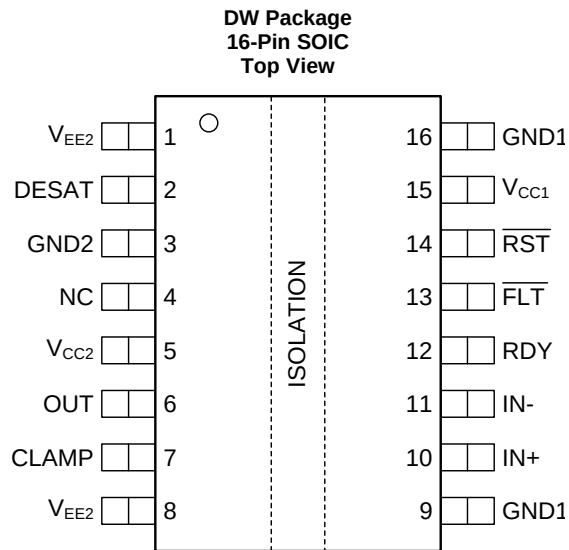
当发生去饱和故障时，器件会通过隔离栅发送故障信号，以将输入端的 $\overline{FLT}$ 输出拉为低电平并阻断隔离器的输入。 $\overline{FLT}$ 的输出状态将被锁存，可通过 $\overline{RST}$ 输入上的低电平有效脉冲复位。

如果在由双极输出电源供电的正常运行期间关断 IGBT，输出电压会被硬钳位为 V_{EE2} 。如果输出电源为单极，那么可采用有源米勒钳位，这种钳位会在一条低阻抗路径上灌入米勒电流，从而防止 IGBT 在高电压瞬态条件下发生动态导通。

栅极驱动器是否准备就绪待运行由两个欠压锁定电路控制，这两个电路会监视输入端和输出端的电源。如果任意一端电源不足，RDY 输出会变为低电平；否则，该输出为高电平。

ISO5851 采用 16 引脚小外形尺寸集成电路 (SOIC) 封装。此器件的额定工作环境温度范围为 -40°C 至 $+125^{\circ}\text{C}$ 。

6 Pin Configuration and Function



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLAMP	7	O	Miller clamp output
DESAT	2	I	Desaturation voltage input
$\overline{\text{FLT}}$	13	O	Fault output, low-active during DESAT condition
GND1	9, 16	—	Input ground
GND2	3	—	Gate drive common. Connect to IGBT emitter.
IN+	10	I	Non-inverting gate drive voltage control input
IN–	11	I	Inverting gate drive voltage control input
NC	4	—	Not connected
OUT	6	O	Gate drive voltage output
RDY	12	O	Power-good output, active high when both supplies are good.
$\overline{\text{RST}}$	14	I	Reset input, apply a low pulse to reset fault latch.
V _{CC1}	15	—	Positive input supply (3 V to 5.5 V)
V _{CC2}	5	—	Most positive output supply potential.
V _{EE2}	1, 8	—	Output negative supply. Connect to GND2 for Unipolar supply application.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC1}	Supply voltage input side		GND1 – 0.3	6	V
V _{CC2}	Positive supply voltage output side	V _{CC2} – GND2	–0.3	35	V
V _{EE2}	Negative supply voltage output side	V _{EE2} – GND2	–17.5	0.3	V
V _(SUP2)	Total supply output voltage	V _{CC2} – V _{EE2}	–0.3	35	V
V _{OUT}	Gate driver output voltage		V _{EE2} – 0.3	V _{CC2} + 0.3	V
I _(OUTH)	Gate driver high output current	Gate driver high output current max pulse width = 10 μs, max duty cycle = 0.2%	2.7		A
I _(OUTL)	Gate driver low output current	Gate driver high output current max pulse width = 10 μs, max duty cycle = 0.2%	5.5		A
V _(LIP)	Voltage at IN+, IN–, $\overline{\text{FLT}}$, RDY, $\overline{\text{RST}}$		GND1 – 0.3	V _{CC1} + 0.3	V
I _(LOP)	Output current of $\overline{\text{FLT}}$, RDY		10		mA
V _(DESAT)	Voltage at DESAT		GND2 – 0.3	V _{CC2} + 0.3	V
V _(CLAMP)	Clamp voltage		V _{EE2} – 0.3	V _{CC2} + 0.3	V
T _J	Junction temperature		–40	150	°C
T _{STG}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC1}	Supply voltage input side	3		5.5	V
V _{CC2}	Positive supply voltage output side (V _{CC2} – GND2)	15		30	V
V _{EE2}	Negative supply voltage output side (V _{EE2} – GND2)	–15		0	V
V _(SUP2)	Total supply voltage output side (V _{CC2} – V _{EE2})	15		30	V
V _{IH}	High-level input voltage (IN+, IN–, $\overline{\text{RST}}$)	0.7 × V _{CC1}		V _{CC1}	V
V _{IL}	Low-level input voltage (IN+, IN–, $\overline{\text{RST}}$)	0		0.3 × V _{CC1}	V
t _{UI}	Pulse width at IN+, IN– for full output (C _{LOAD} = 1 nF)	40			ns
t _{RST}	Pulse width at $\overline{\text{RST}}$ for resetting fault latch	800			ns
T _A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO5851	UNIT
		DW (SOIC)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	99.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	48.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	29.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	56.5	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

7.5 Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation ⁽¹⁾				1255	mW
P_{ID} Maximum input power dissipation				175	mW
P_{OD} Maximum output power dissipation				1080	mW

- (1) Full chip power dissipation is de-rated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that Junction temperature does not exceed 150°C.

7.6 Insulation Characteristics

PARAMETER	TEST CONDITIONS	SPECIFICATION	UNIT
CLR External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	8	mm
CPG External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI Distance through the insulation	Minimum internal gap (internal clearance)	21	μm
CTI Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	V
Material group	According to IEC 60664-1	I	
Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V _{RMS}	I-IV	
	Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12⁽²⁾			
V_{IORM} Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V _{PK}
V_{IOWM} Maximum isolation working voltage	AC voltage, Time dependent dielectric breakdown (TDDB) Test, see Figure 1	1500	V _{RMS}
	DC voltage	2121	V _{DC}
V_{IOTM} Maximum Transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 sec (qualification), t = 1 sec (100% production)	8000	V _{PK}
V_{IOSM} Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800 V_{PK}$ (qualification)	8000	
q_{pd} Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545 V_{PK}$, $t_m = 10$ s	≤5	pC
	Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394 V_{PK}$, $t_m = 10$ s	≤5	
	Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3977 V_{PK}$, $t_m = 10$ s	≤5	
R_{IO} Isolation resistance, input to output ⁽⁵⁾	$V_{IO} = 500$ V at T _S	> 10 ⁹	Ω
	$V_{IO} = 500$ V, T _A = 25°C	>10 ¹²	Ω
	$V_{IO} = 500$ V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	Ω
C_{IO} Barrier capacitance, input to output ⁽⁵⁾	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~1	pF
Pollution degree		2	
Climatic category		40/125/21	
UL 1577			
V_{ISO} Withstanding Isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 sec (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840 V_{RMS}$, t = 1 sec (100% production)	5700	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Certified according to CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced Insulation Maximum Transient isolation voltage, 8000 V _{PK} ; Maximum surge isolation voltage, 8000 V _{PK} ; Maximum repetitive peak isolation voltage, 2121 V _{PK}	Isolation Rating of 5700 V _{RMS} ; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 V _{RMS} max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V _{RMS} (354 V _{PK}) max working voltage	Single Protection, 5700 V _{RMS}	Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 V _{RMS} maximum working voltage	5700 V _{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V _{RMS} 5700 V _{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V _{RMS}
Certification completed Certificate number: 40040142	Certification completed Master contract number: 220991	Certification completed File number: E181974	Certification completed Certificate number: CQC16001141761	Certification completed Client ID number: 77311

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S Safety input, output or supply current	R _{θJA} = 99.6°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C			349	mA
	R _{θJA} = 99.6°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C			228	
	R _{θJA} = 99.6°C/W, V _I = 15 V, T _J = 150°C, T _A = 25°C			84	
	R _{θJA} = 99.6°C/W, V _I = 30 V, T _J = 150°C, T _A = 25°C			42	
P _S Safety input, output, or total power	R _{θJA} = 99.6°C/W, T _J = 150°C, T _A = 25°C			1255 ⁽¹⁾	mW
T _S Maximum ambient safety temperature				150	°C

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - \text{GND2} = 15\text{ V}$, $\text{GND2} - V_{EE2} = 8\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE SUPPLY						
$V_{IT+}(\text{UVLO1})$	Positive-going UVLO1 threshold voltage input side ($V_{CC1} - \text{GND1}$)				2.25	V
$V_{IT-}(\text{UVLO1})$	Negative-going UVLO1 threshold voltage input side ($V_{CC1} - \text{GND1}$)		1.7			V
$V_{HYS}(\text{UVLO1})$	UVLO1 Hysteresis voltage ($V_{IT+} - V_{IT-}$) input side			0.24		V
$V_{IT+}(\text{UVLO2})$	Positive-going UVLO2 threshold voltage output side ($V_{CC2} - \text{GND2}$)			12	13	V
$V_{IT-}(\text{UVLO2})$	Negative-going UVLO2 threshold voltage output side ($V_{CC2} - \text{GND2}$)		9.5	11		V
$V_{HYS}(\text{UVLO2})$	UVLO2 Hysteresis voltage ($V_{IT+} - V_{IT-}$) output side			1		V
I_{Q1}	Input supply quiescent current			2.8	4.5	mA
I_{Q2}	Output supply quiescent current			3.6	6	mA
LOGIC I/O						
$V_{IT+}(\text{IN}, \text{RST})$	Positive-going input threshold voltage ($\text{IN}+$, $\text{IN}-$, RST)				$0.7 \times V_{CC1}$	V
$V_{IT-}(\text{IN}, \text{RST})$	Negative-going input threshold voltage ($\text{IN}+$, $\text{IN}-$, RST)		$0.3 \times V_{CC1}$			V
$V_{HYS}(\text{IN}, \text{RST})$	Input hysteresis voltage ($\text{IN}+$, $\text{IN}-$, RST)			$0.15 \times V_{CC1}$		V
I_{IH}	High-level input leakage at ($\text{IN}+$)	$\text{IN}+ = V_{CC1}$		100		μA
I_{IL}	Low-level input leakage at ($\text{IN}-$, RST)	$\text{IN}- = \text{GND1}$, $\text{RST} = \text{GND1}$		-100		μA
I_{PU}	Pull-up current of FLT , RDY	$V_{(\text{RDY})} = \text{GND1}$, $V_{(\text{FLT})} = \text{GND1}$		100		μA
V_{OL}	Low-level output voltage at FLT , RDY	$I_{(\text{FLT})} = 5\text{ mA}$			0.2	V
GATE DRIVER STAGE						
$V_{(\text{OUTPD})}$	Active output pulldown voltage	$I_{\text{OUT}} = 200\text{ mA}$, $V_{CC2} = \text{open}$			2	V
$V_{(\text{OUTH})}$	High-level output voltage	$I_{\text{OUT}} = -20\text{ mA}$	$V_{CC2} - 0.5$	$V_{CC2} - 0.24$		V
$V_{(\text{OUTL})}$	Low-level output voltage	$I_{\text{OUT}} = 20\text{ mA}$		$V_{EE2} + 13$	$V_{EE2} + 50$	mV
$I_{(\text{OUTH})}$	High-level output peak current	$\text{IN}+ = \text{high}$, $\text{IN}- = \text{low}$, $V_{\text{OUT}} = V_{CC2} - 15\text{ V}$	1.5	2.5		A
$I_{(\text{OUTL})}$	Low-level output peak current	$\text{IN}+ = \text{low}$, $\text{IN}- = \text{high}$, $V_{\text{OUT}} = V_{EE2} + 15\text{ V}$	3.4	5		A
ACTIVE MILLER CLAMP						
$V_{(\text{CLP})}$	Low-level clamp voltage	$I_{(\text{CLP})} = 20\text{ mA}$		$V_{EE2} + 0.015$	$V_{EE2} + 0.08$	V
$I_{(\text{CLP})}$	Low-level clamp current	$V_{(\text{CLAMP})} = V_{EE2} + 2.5\text{ V}$	1.6	2.5		A
$V_{(\text{CLTH})}$	Clamp threshold voltage		1.6	2.1	2.5	V
SHORT CIRCUIT CLAMPING						
$V_{(\text{CLP_OUT})}$	Clamping voltage ($V_{\text{OUT}} - V_{CC2}$)	$\text{IN}+ = \text{high}$, $\text{IN}- = \text{low}$, $t_{\text{CLP}} = 10\text{ }\mu\text{s}$, $I_{(\text{OUTH})} = 500\text{ mA}$		0.8	1.3	V
$V_{(\text{CLP_CLAMP})}$	Clamping voltage ($V_{\text{CLP}} - V_{CC2}$)	$\text{IN}+ = \text{high}$, $\text{IN}- = \text{low}$, $t_{\text{CLP}} = 10\text{ }\mu\text{s}$, $I_{(\text{CLP})} = 500\text{ mA}$		1.3		V
$V_{(\text{CLP_CLAMP})}$	Clamping voltage at CLAMP	$\text{IN}+ = \text{High}$, $\text{IN}- = \text{Low}$, $I_{(\text{CLP})} = 20\text{ mA}$		0.7	1.1	V
DESAT PROTECTION						
$I_{(\text{CHG})}$	Blanking capacitor charge current	$V_{(\text{DESAT})} - \text{GND2} = 2\text{ V}$	0.42	0.5	0.58	mA
$I_{(\text{DCHG})}$	Blanking capacitor discharge current	$V_{(\text{DESAT})} - \text{GND2} = 6\text{ V}$	9	14		mA
$V_{(\text{DSTH})}$	DESAT threshold voltage with respect to GND2		8.3	9	9.5	V
$V_{(\text{DSL})}$	DESAT voltage with respect to GND2, when OUT is driven low		0.4		1	V

7.10 Switching Characteristics

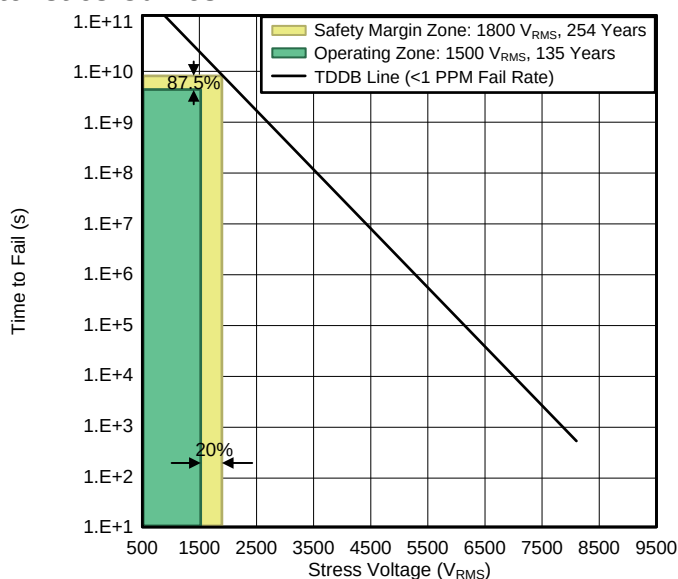
Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - \text{GND2} = 15\text{ V}$, $\text{GND2} - V_{EE2} = 8\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time	$C_{\text{LOAD}} = 1\text{ nF}$, see Figure 38 , Figure 39 , and Figure 40	12	20	35	ns
t_f	Output signal fall time		12	20	37	ns
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay			76	110	ns
$t_{\text{sk-p}}$	Pulse Skew $ t_{\text{PHL}} - t_{\text{PLH}} $				20	ns
$t_{\text{sk-pp}}$	Part-to-part skew				30 ⁽¹⁾	ns
t_{GF}	Glitch filter on IN+ , IN- , $\overline{\text{RST}}$		20	30	40	ns
$t_{\text{DESAT}} (10\%)$	DESAT sense to 10% OUT delay		300	415	500	ns
$t_{\text{DESAT}} (\text{GF})$	DESAT glitch filter delay			330		ns
$t_{\text{DESAT}} (\overline{\text{FLT}})$	DESAT sense to $\overline{\text{FLT}}$ -low delay	see Figure 40		2000	2420	ns
t_{LEB}	Leading edge blanking time	see Figure 38 and Figure 39	330	400	500	ns
$t_{\text{GF}}(\text{RSTFLT})$	Glitch filter on $\overline{\text{RST}}$ for resetting $\overline{\text{FLT}}$		300		800	ns
C_i	Input capacitance ⁽²⁾	$V_i = V_{CC1} / 2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{CC1} = 5\text{ V}$		2		pF
CMTI	Common-mode transient immunity	$V_{\text{CM}} = 1500\text{ V}$, see Figure 41	100	120		kV/ μs

(1) Measured at same supply voltage and temperature condition

(2) Measured from input pin to ground.

7.11 Insulation Characteristics Curves



T_A upto 150°C

Stress-voltage frequency = 60 Hz

Figure 1. Reinforced High-Voltage Capacitor Life Time Projection

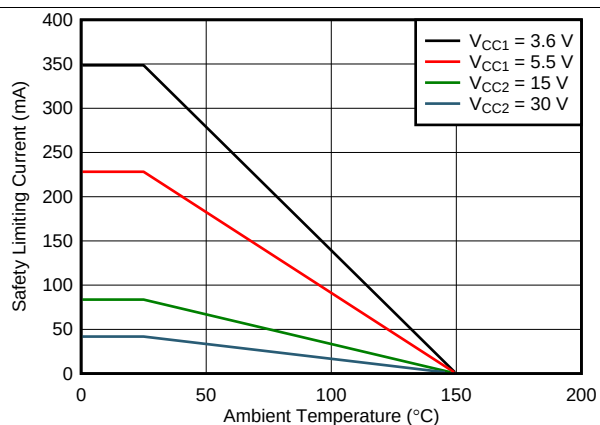


Figure 2. Thermal Derating Curve for Limiting Current per VDE

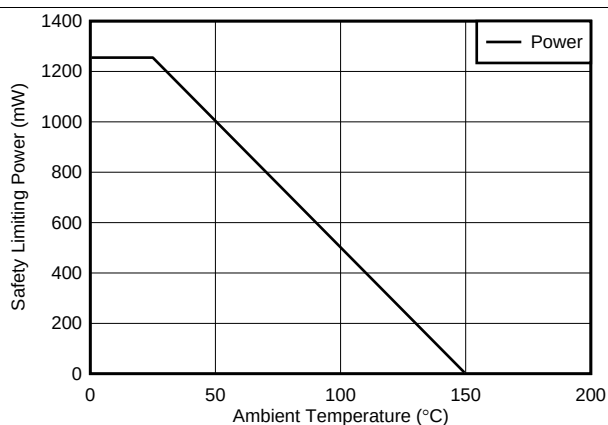
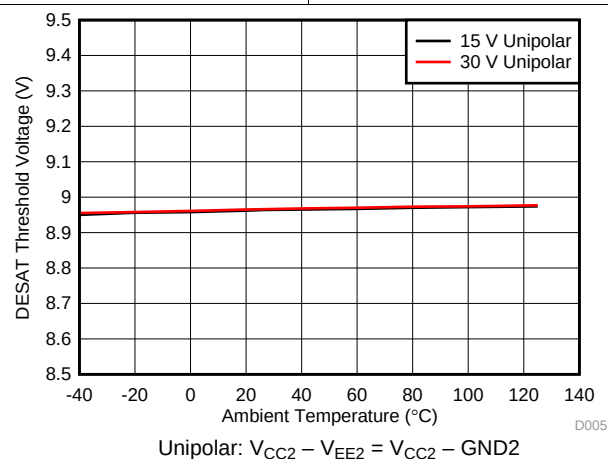
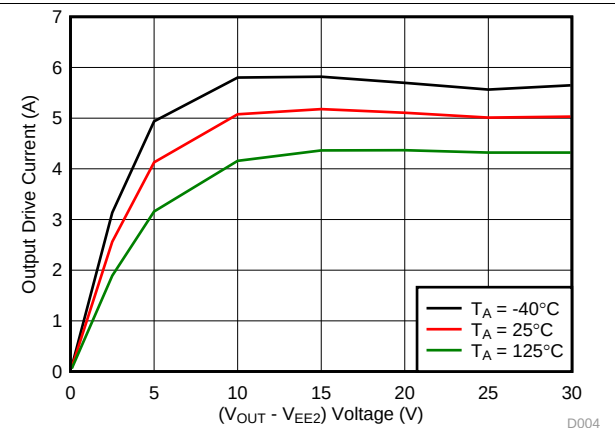
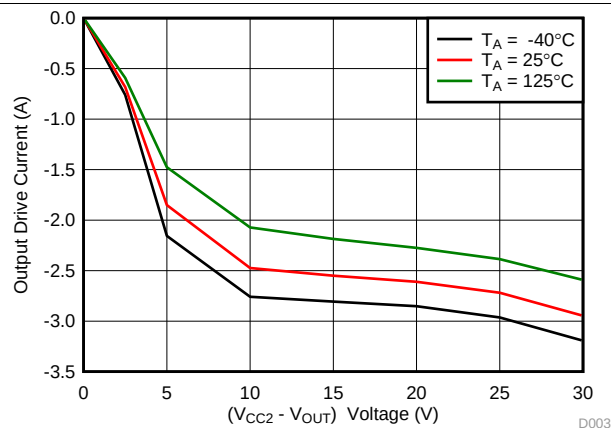
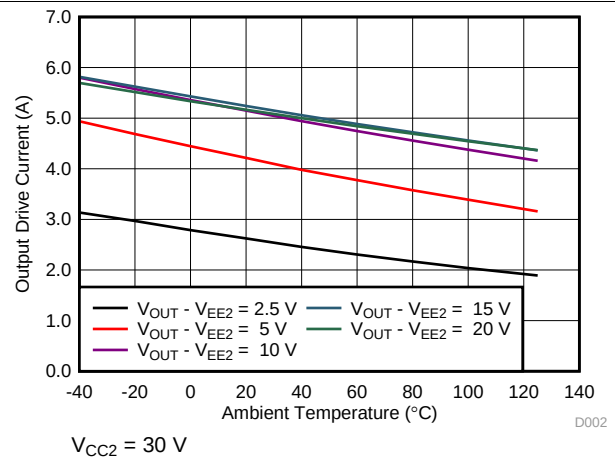
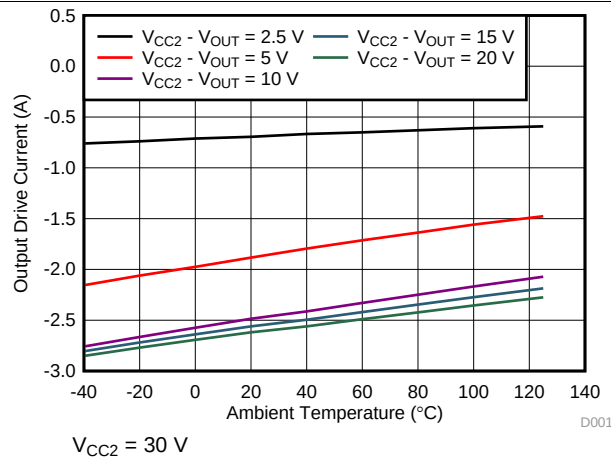
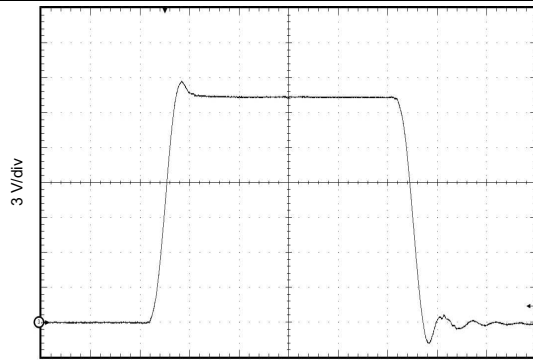


Figure 3. Thermal Derating Curve for Limiting Power per VDE

7.12 Typical Characteristics

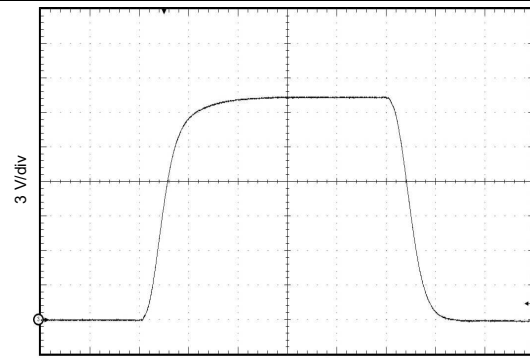


Typical Characteristics (continued)



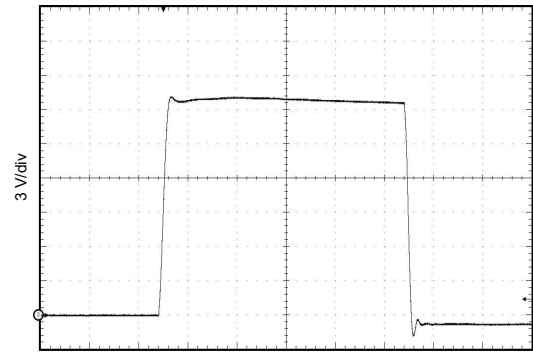
$C_L = 1 \text{ nF}$
 $R_G = 0 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

Figure 9. OUT Transient Waveform



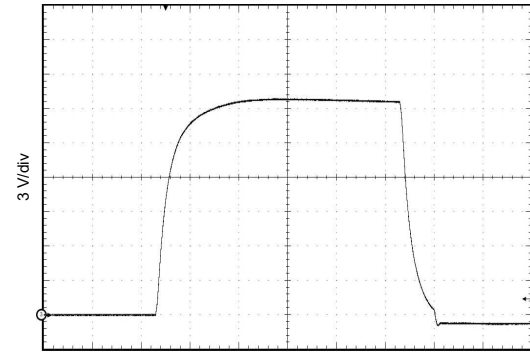
$C_L = 1 \text{ nF}$
 $R_G = 10 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

Figure 10. OUT Transient Waveform



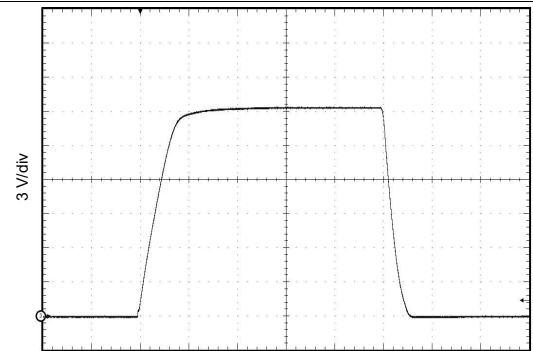
$C_L = 10 \text{ nF}$
 $R_G = 0 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

Figure 11. OUT Transient Waveform



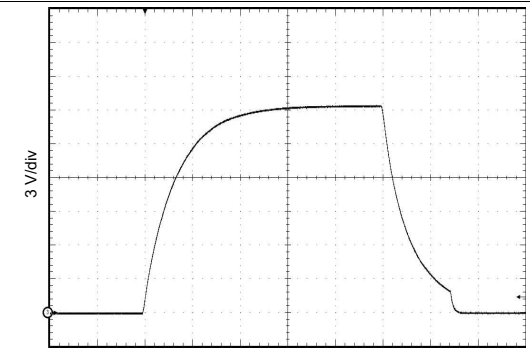
$C_L = 10 \text{ nF}$
 $R_G = 10 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

Figure 12. OUT Transient Waveform



$C_L = 100 \text{ nF}$
 $R_G = 0 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

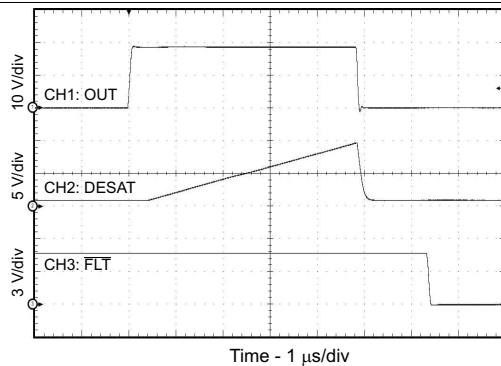
Figure 13. OUT Transient Waveform



$C_L = 100 \text{ nF}$
 $R_G = 10 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

Figure 14. OUT Transient Waveform

Typical Characteristics (continued)



$C_L = 100 \text{ nF}$ $R_G = 10 \Omega$
 $V_{CC2} - V_{EE2} = V_{CC2} - \text{GND2} = 20 \text{ V}$

Figure 15. OUT Transient Waveform DESAT and $\overline{\text{FLT}}$

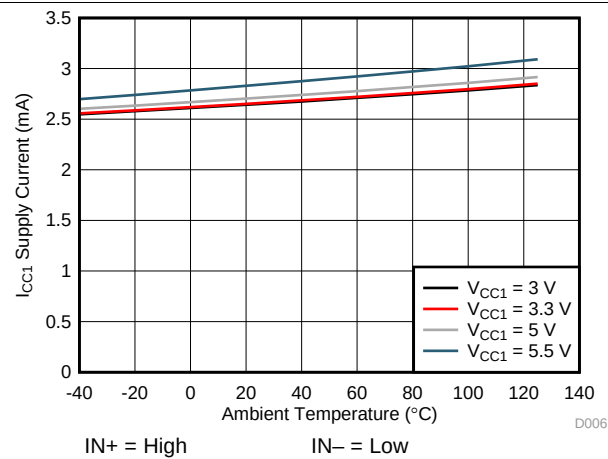


Figure 16. I_{CC1} Supply Current vs Temperature

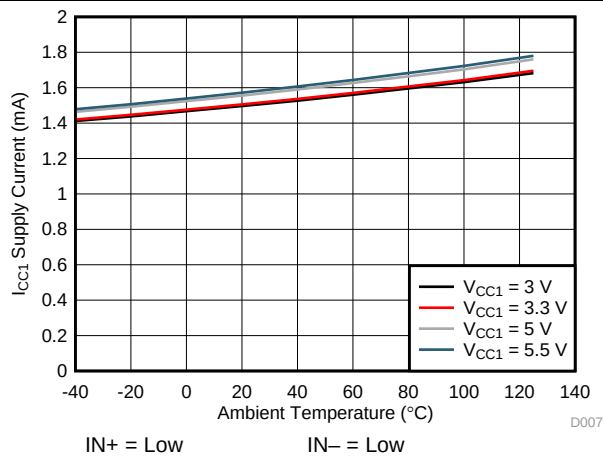


Figure 17. I_{CC1} Supply Current vs Temperature

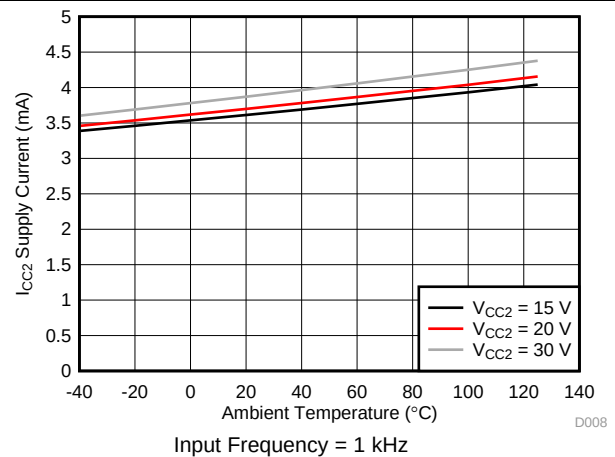


Figure 18. I_{CC2} Supply Current vs Temperature

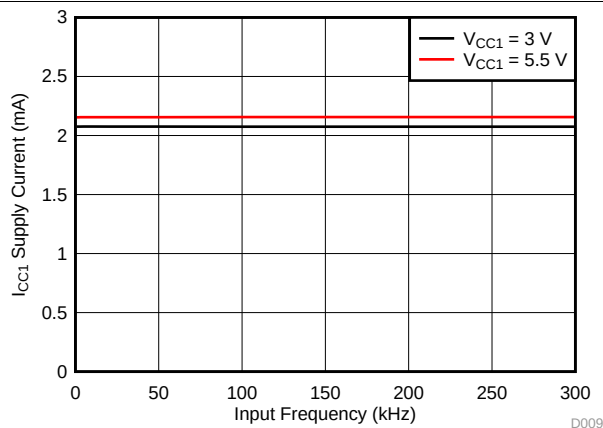


Figure 19. I_{CC1} Supply Current vs Input Frequency

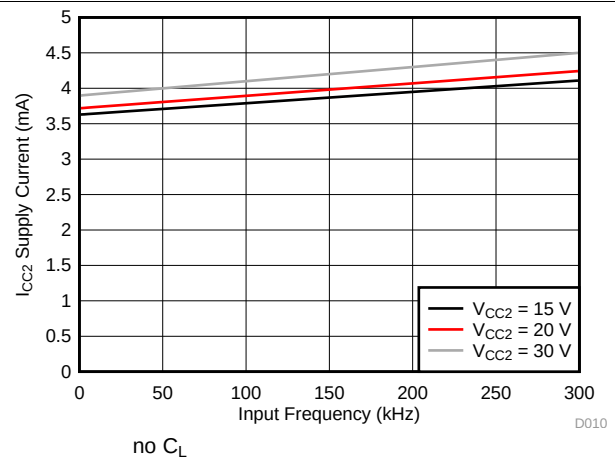
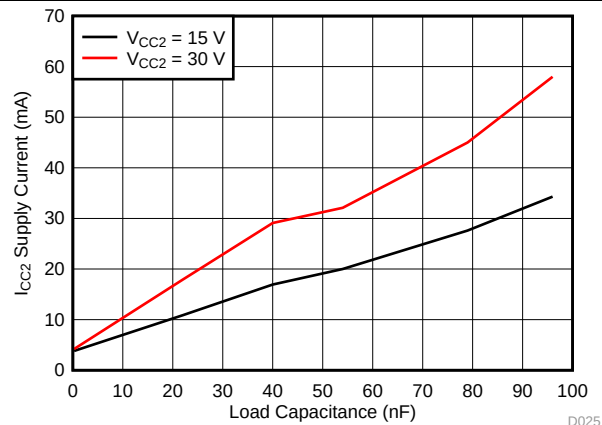


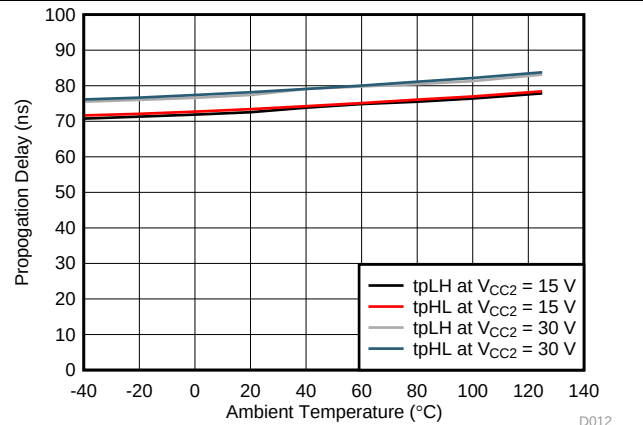
Figure 20. I_{CC2} Supply Current vs Input Frequency

Typical Characteristics (continued)



$R_G = 10\ \Omega$, 20 kHz

Figure 21. I_{CC2} Supply Current vs Load Capacitance

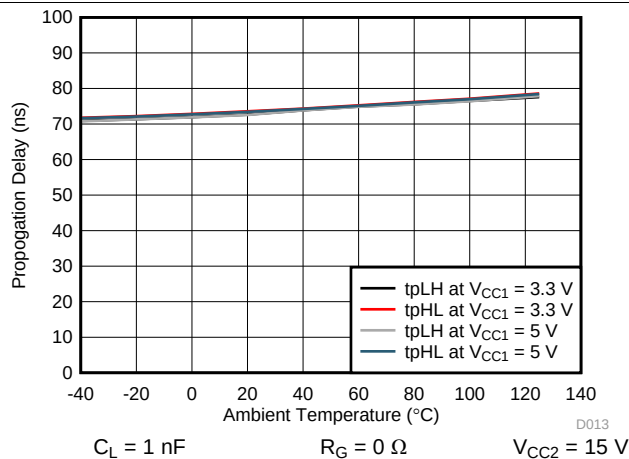


$C_L = 1\text{ nF}$

$R_G = 0\ \Omega$

$V_{CC1} = 5\text{ V}$

Figure 22. V_{CC1} Propagation Delay vs Temperature

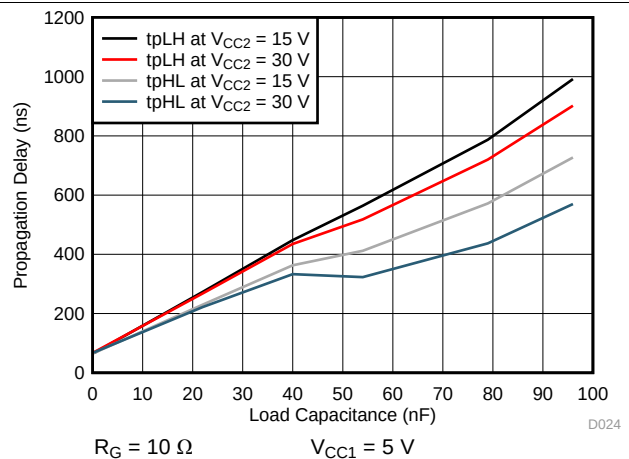


$C_L = 1\text{ nF}$

$R_G = 0\ \Omega$

$V_{CC2} = 15\text{ V}$

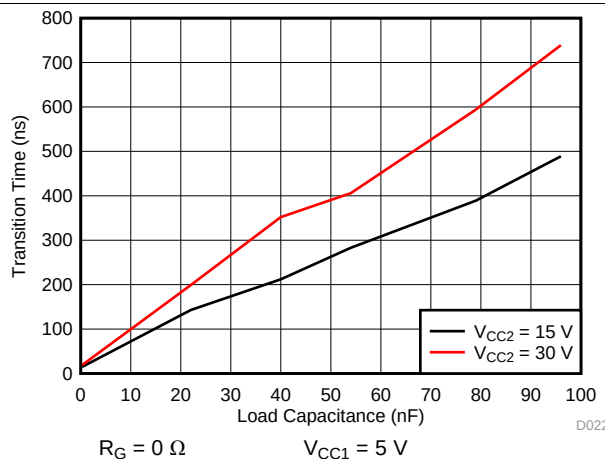
Figure 23. V_{CC2} Propagation Delay vs Temperature



$R_G = 10\ \Omega$

$V_{CC1} = 5\text{ V}$

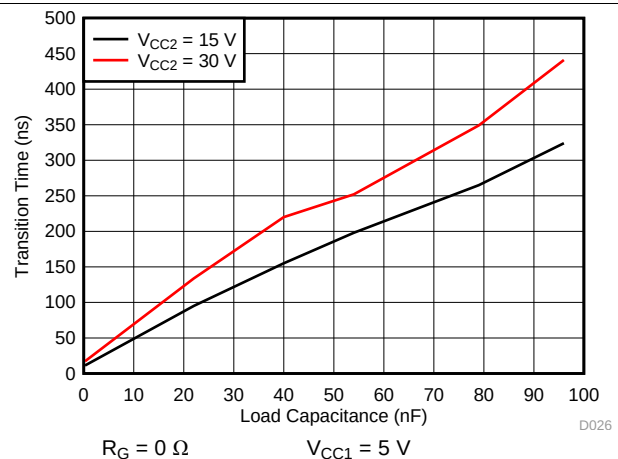
Figure 24. Propagation Delay vs Load Capacitance



$R_G = 0\ \Omega$

$V_{CC1} = 5\text{ V}$

Figure 25. t_r Rise Time vs Load Capacitance

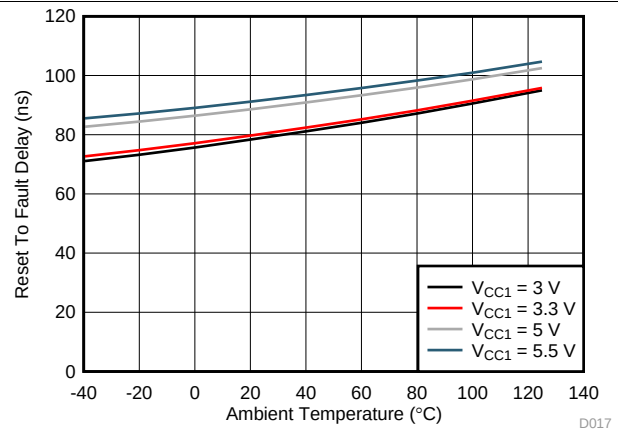
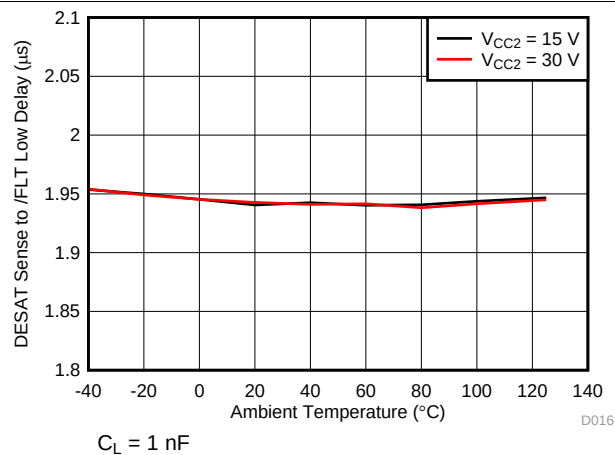
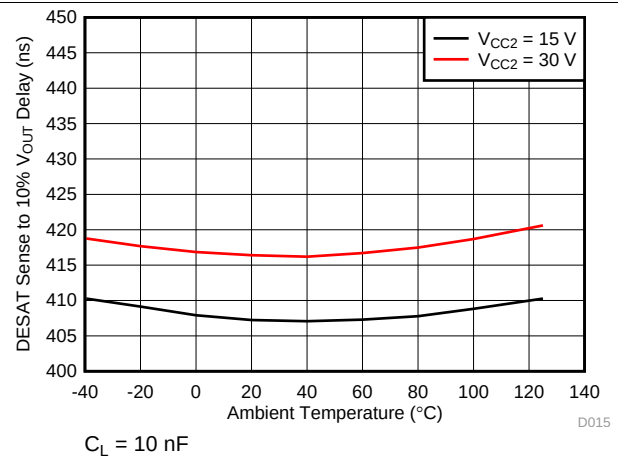
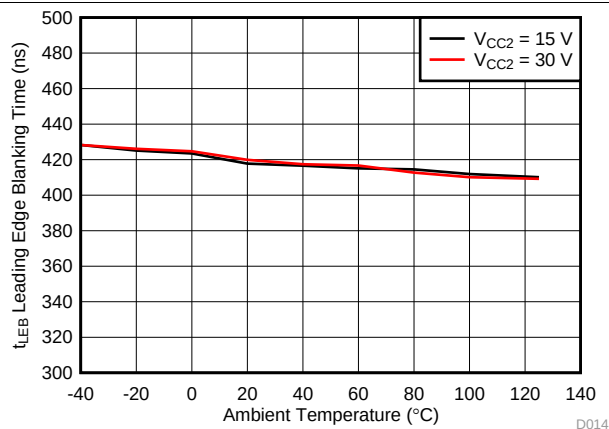
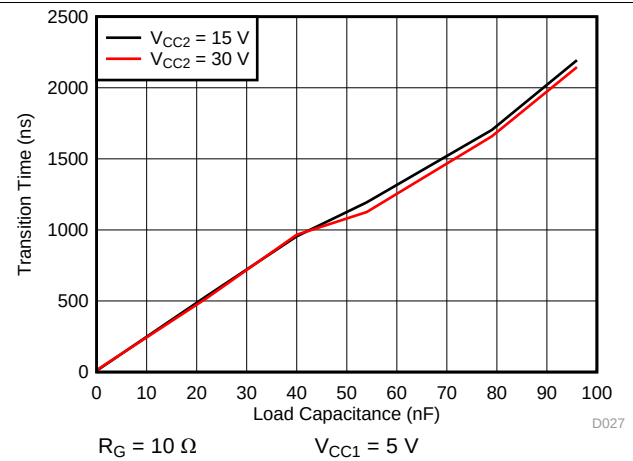
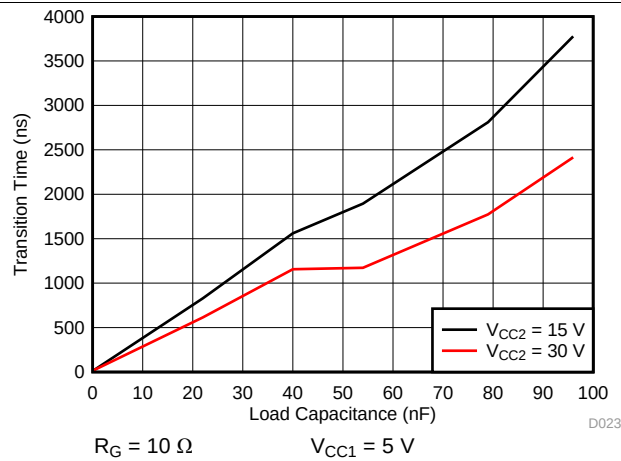


$R_G = 0\ \Omega$

$V_{CC1} = 5\text{ V}$

Figure 26. t_f Fall Time v. Load Capacitance

Typical Characteristics (continued)



Typical Characteristics (continued)

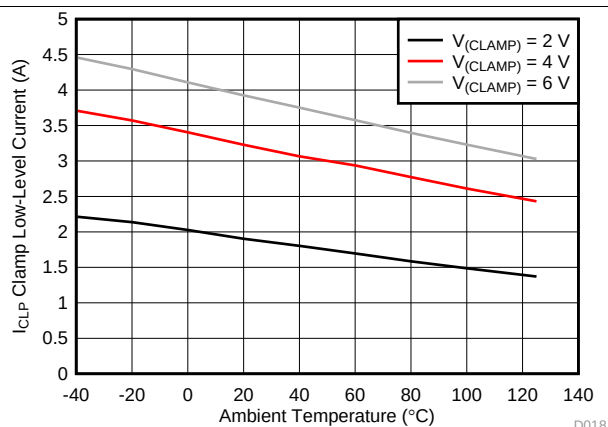


Figure 33. Miller Clamp Current vs Temperature

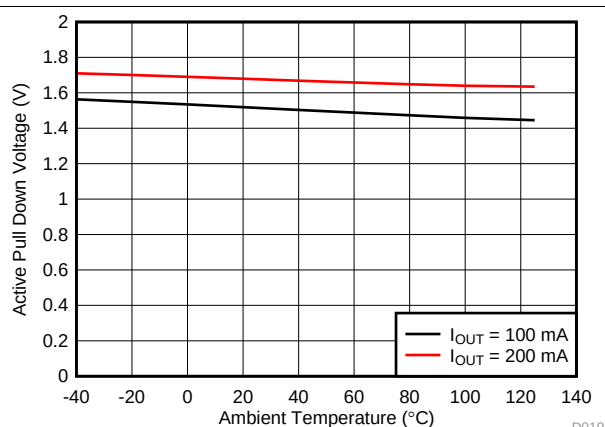


Figure 34. Active Pulldown Voltage vs Temperature

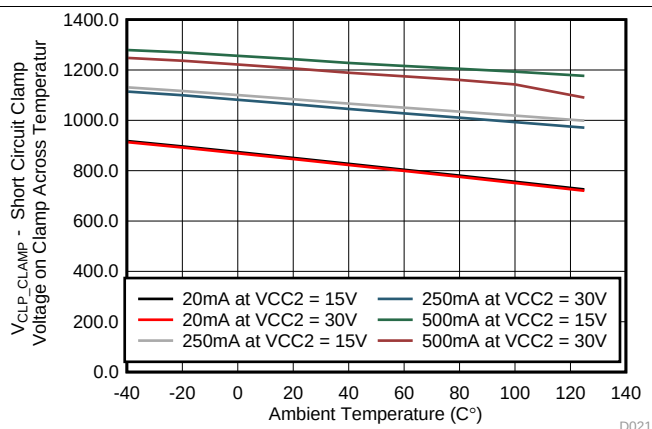


Figure 35. V_{CLP_CLAMP} - Short Circuit Clamp Voltage on Clamp Across Temperature

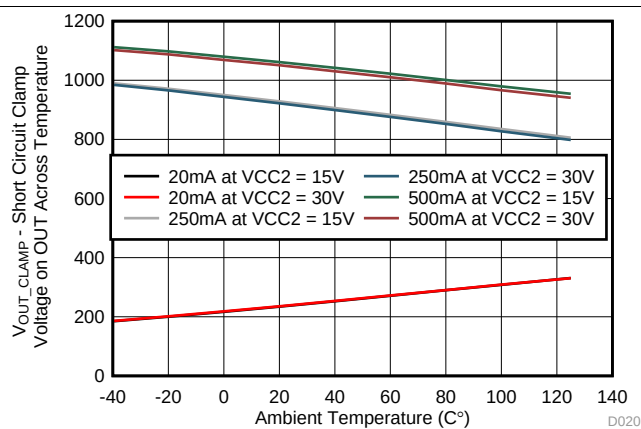


Figure 36. V_{OUT_CLAMP} - Short Circuit Clamp Voltage on OUT Across Temperature

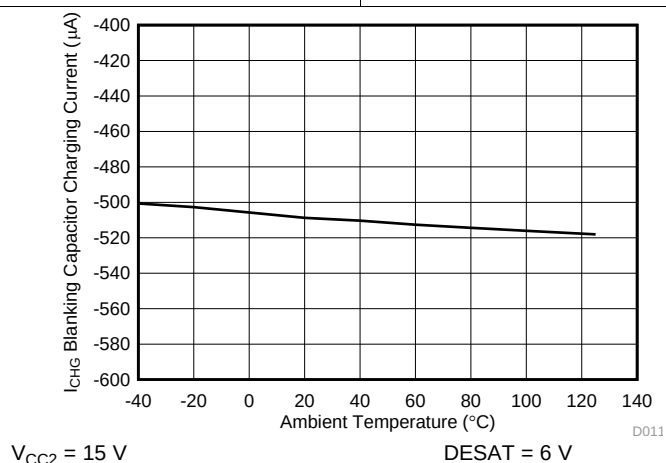


Figure 37. Blanking Capacitor Charging Current vs Temperature

8 Parameter Measurement Information

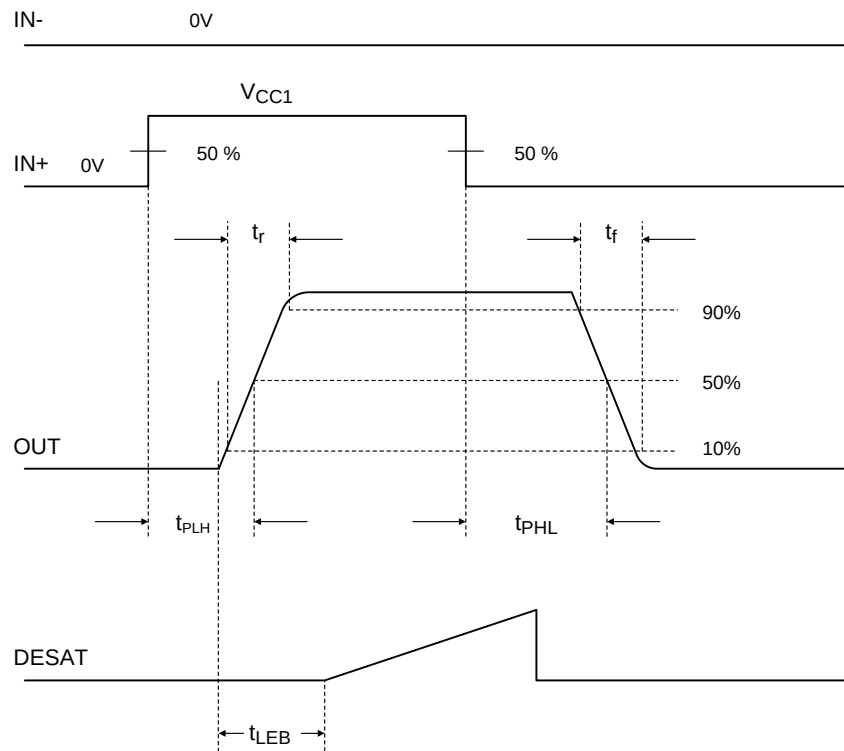


Figure 38. OUT Propagation Delay, Non-Inverting Configuration

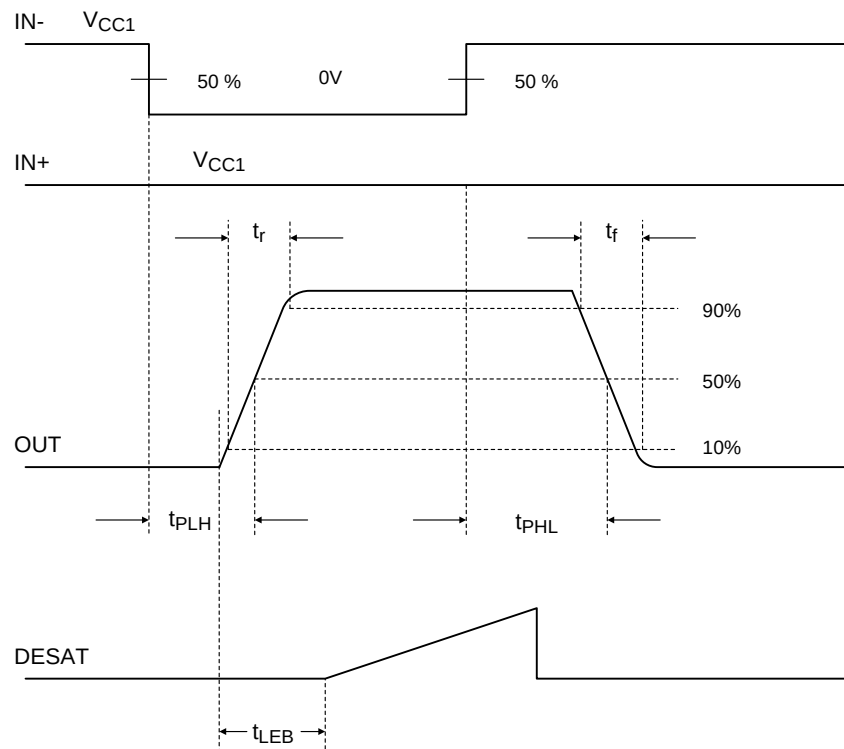


Figure 39. OUT Propagation Delay, Inverting Configuration

Parameter Measurement Information (continued)

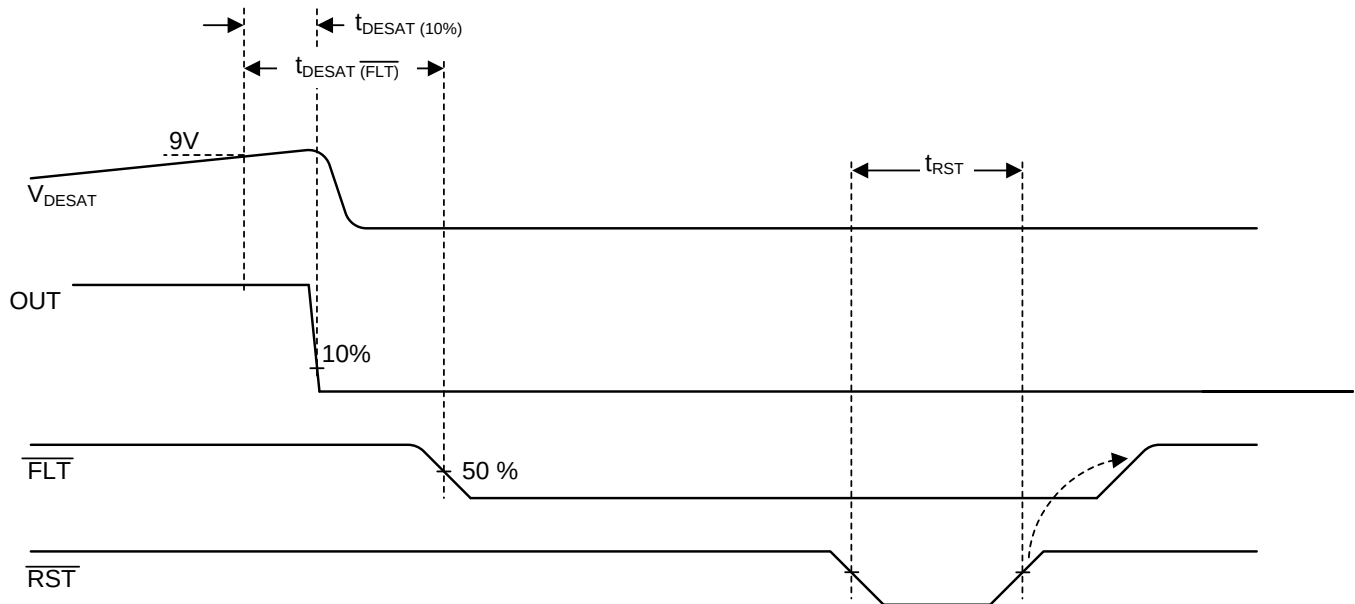
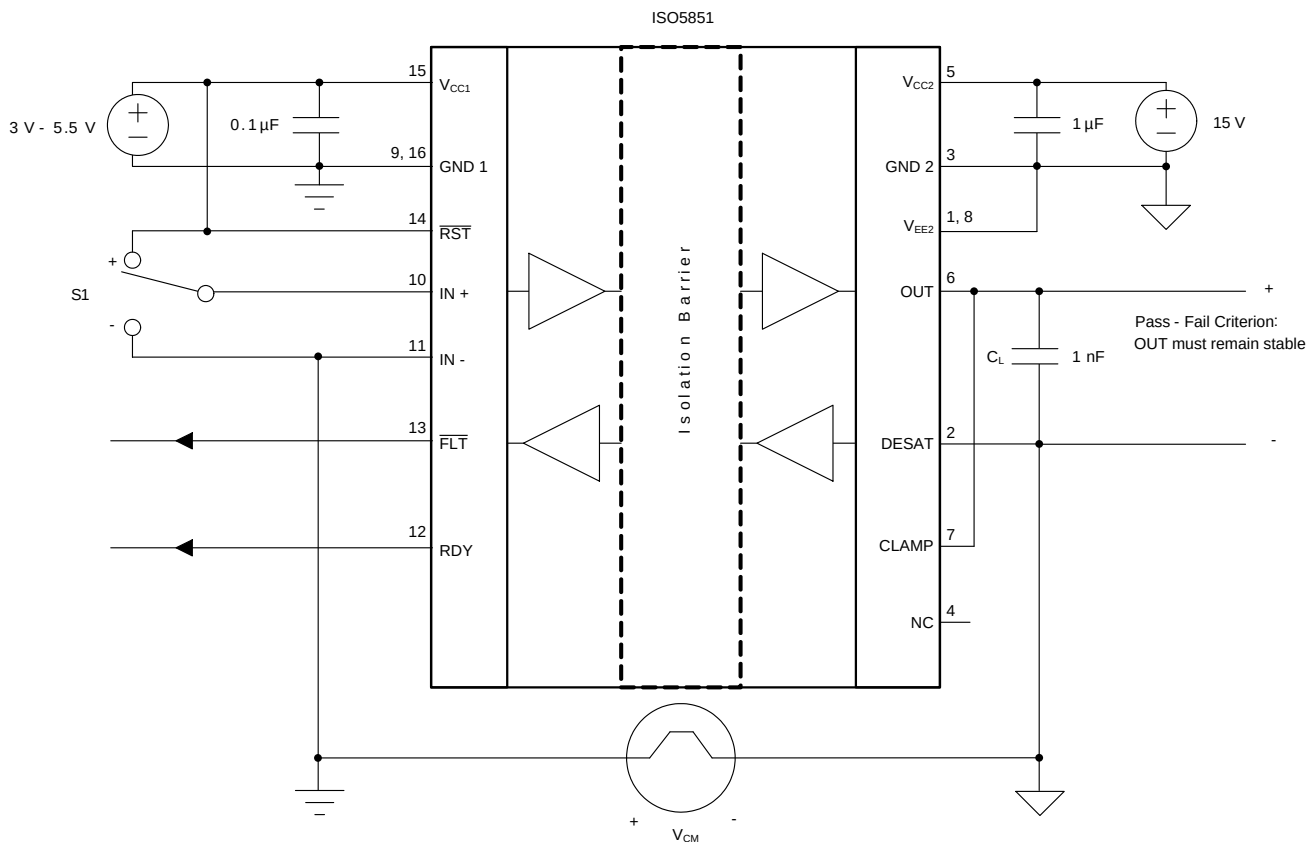


Figure 40. DESAT, OUT, $\overline{\text{FLT}}$, $\overline{\text{RST}}$ Delay



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Figure 41. Common-Mode Transient Immunity Test Circuit

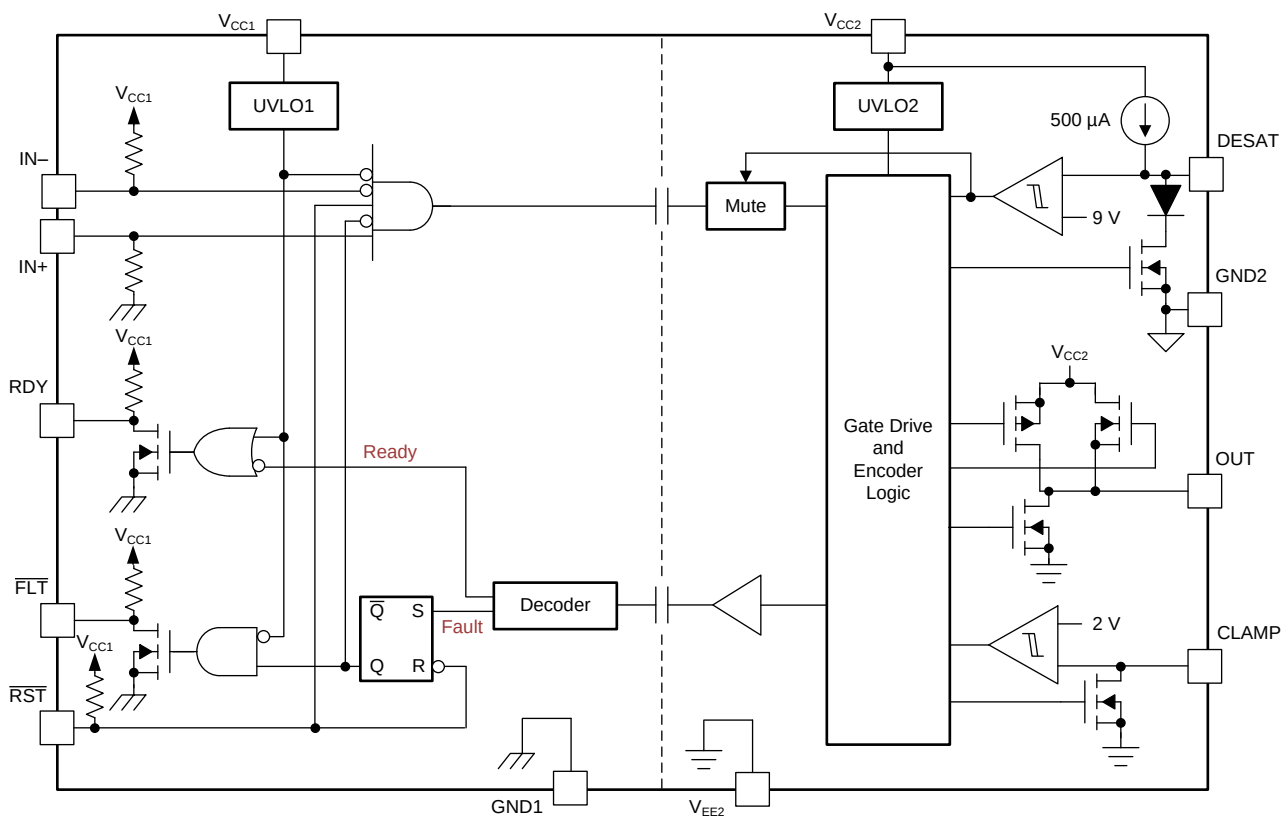
9 Detailed Description

9.1 Overview

The ISO5851 is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a capacitive, silicon dioxide (SiO_2), isolation barrier.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and RESET ($\overline{\text{RST}}$) inputs, READY (RDY) and FAULT ($\overline{\text{FLT}}$) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5851 also contains under voltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5851 also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to Miller effect, for unipolar supply operation.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Supply and Active Miller Clamp

The ISO5851 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of V_{CC2} and V_{EE2} for bipolar operation are 15 V and –8 V with respect to GND2.

For operation with unipolar supply, typically, V_{CC2} is connected to 15-V with respect to GND2, and V_{EE2} is connected to GND2. In this use case, the IGBT can turn-on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected to IGBT gate and Miller current is sunk through a low impedance CLAMP transistor.

Miller CLAMP is designed for Miller current up to 2 A. When the IGBT is turned-off and the gate voltage transitions below 2 V the CLAMP current output is activated.

9.3.2 Active Output Pulldown

The active output pulldown feature ensures that the IGBT gate OUT is clamped to V_{EE2} to ensure safe IGBT off-state when the output side is not connected to the power supply.

9.3.3 Undervoltage Lockout (UVLO) With Ready (RDY) Pin Indication Output

Undervoltage lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned-off, if the supply V_{CC1} drops below $V_{IT-(UVLO1)}$, irrespective of IN+, IN– and RST input till V_{CC1} goes above $V_{IT+(UVLO1)}$.

In similar manner, the IGBT is turned-off, if the supply V_{CC2} drops below $V_{IT-(UVLO2)}$, irrespective of IN+, IN– and RST input till V_{CC2} goes above $V_{IT+(UVLO2)}$.

Ready (RDY) pin indicates status of input and output side Under Voltage Lock-Out (UVLO) internal protection feature. If either side of device have insufficient supply (V_{CC1} or V_{CC2}), the RDY pin output goes low; otherwise, RDY pin output is high. RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

9.3.4 Fault ($\overline{FLT}$) and Reset ($\overline{RST}$)

During IGBT overload condition, to report desaturation error $\overline{FLT}$ goes low. If $\overline{RST}$ is held low for the specified duration, FLT is cleared at rising edge of RST. RST has an internal filter to reject noise and glitches. By asserting RST for at-least the specified minimum duration, device input logic can be enabled or disabled.

9.3.5 Short Circuit Clamp

Under short circuit events it is possible that currents are induced back into the gate-driver OUT and CLAMP pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUT and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

9.4 Device Functional Modes

Table 1 lists the functional modes for the ISO5851 device.

In ISO5851 OUT to follow IN+ in normal functional mode, $\overline{\text{FLT}}$ must be in high state.

Table 1. Function Table⁽¹⁾

V_{CC1}	V_{CC2}	IN+	IN–	$\overline{\text{RST}}$	RDY	OUT
PU	PD	X	X	X	Low	Low
PD	PU	X	X	X	Low	Low
PU	PU	X	X	Low	High	Low
PU	Open	X	X	X	Low	Low
PU	PU	Low	X	X	High	Low
PU	PU	X	High	X	High	Low
PU	PU	High	Low	High	High	High

(1) PU: Power Up ($V_{CC1} \geq 2.25\text{-V}$, $V_{CC2} \geq 13\text{-V}$), PD: Power Down ($V_{CC1} \leq 1.7\text{-V}$, $V_{CC2} \leq 9.5\text{-V}$), X: Irrelevant

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO5851 is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. It is intended for use in applications such as motor control, industrial inverters and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a micro controller, and are at low voltage levels such as 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 30 V (using a unipolar output supply) to 15 V (using bipolar output supply), and need high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive needs to be applied with reference to the Emitter of the IGBT (Source for MOSFET), and by construction, the emitter node in a gate drive system may swing between 0 to the DC bus voltage, that can be several hundreds of volts in magnitude.

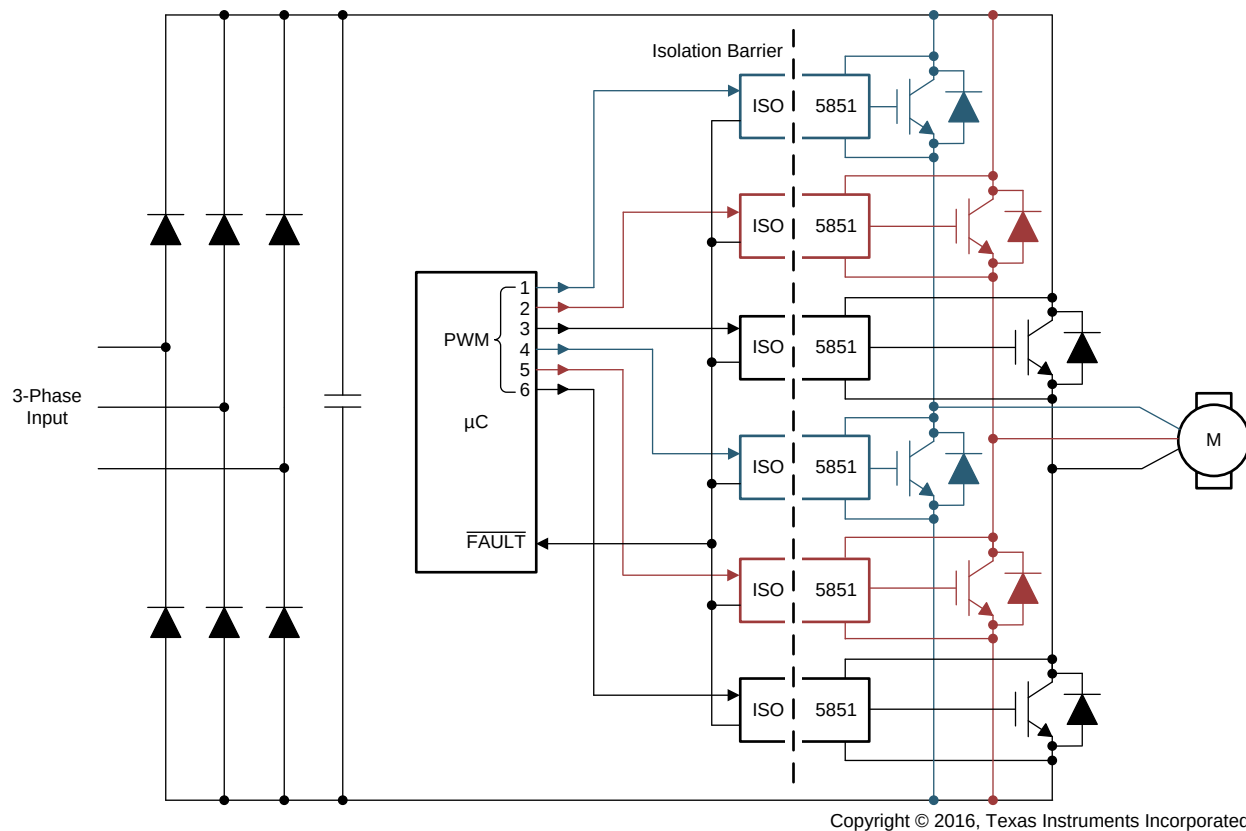
The ISO5851 is thus used to level shift the incoming 3.3-V and 5-V control signals from the microcontroller to the 30 V (using a unipolar output supply) to 15 V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

10.2 Typical Applications

[Figure 42](#) shows the typical application of a three-phase inverter using six ISO5851 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high power applications such as high-voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one ISO5851. The switches are driven on and off at high switching frequency with specific patterns that to converter dc bus voltage to three-phase AC voltages.

Typical Applications (continued)



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Figure 42. Typical Motor Drive Application

10.2.1 Design Requirements

Unlike optocoupler based gate drivers which need external current drivers and biasing circuitry to provide the input control signals, the input control to the ISO5851 is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain $\overline{FLT}$ output signal and $\overline{RST}$ input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. Table 2 shows the allowed range for Input and Output supply voltage, and the typical current output available from the gate-driver.

Table 2. Design Parameters

PARAMETER	VALUE
Input supply voltage	3 V to 5.5 V
Unipolar output supply voltage ($V_{CC2} - GND2 = V_{CC2} - V_{EE2}$)	15 V to 30 V
Bipolar output supply voltage ($V_{CC2} - V_{EE2}$)	15 V to 30 V
Bipolar output supply voltage ($GND2 - V_{EE2}$)	0 V to 15 V
Output current	2.5 A

10.2.2 Detailed Design Procedure

10.2.2.1 Recommended ISO5851 Application Circuit

The ISO5851 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications. The recommended application circuit in [Figure 43](#) shows a typical gate driver implementation with unipolar output supply and [Figure 44](#) shows a typical gate driver implementation with bipolar output supply using the ISO5851.

A 0.1- μ F bypass capacitor, recommended at input supply pin V_{CC1} and 1- μ F bypass capacitor, recommended at output supply pin V_{CC2} , provide the large transient currents necessary during a switching transition to ensure reliable operation. The 220 pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode (D_{DST}) and its 1-k Ω series resistor are external protection components. The R_G gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain $\overline{FLT}$ output and RDY output has a passive 10-k Ω pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

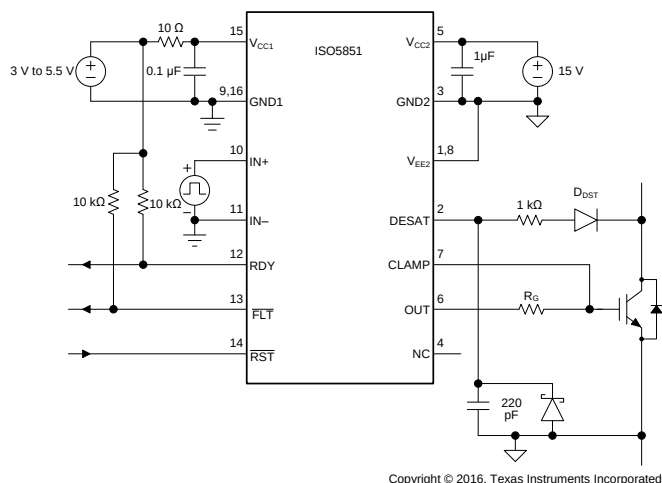


Figure 43. Unipolar Output Supply

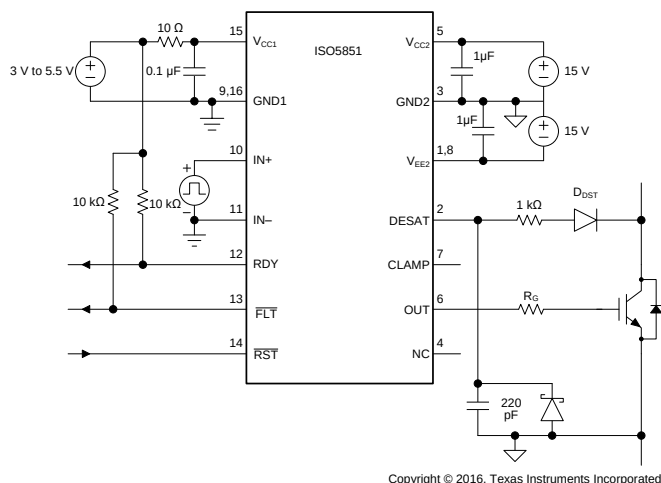
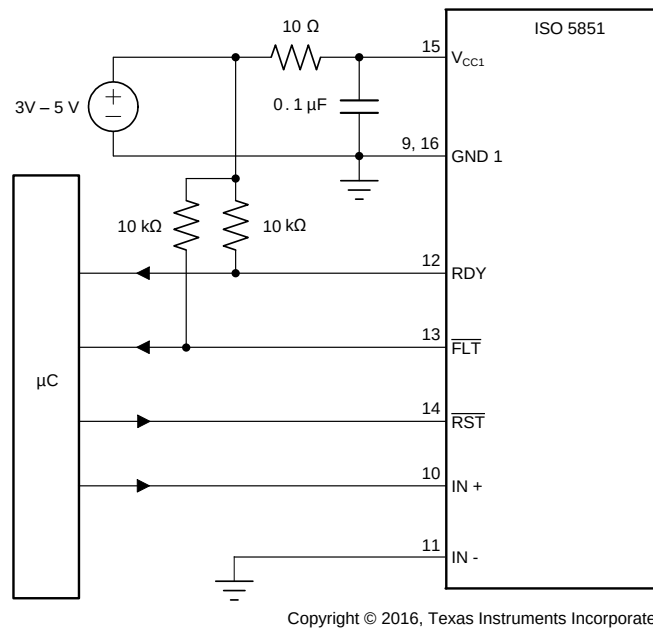


Figure 44. Bipolar Output Supply

10.2.2.2 $\overline{FLT}$ and RDY Pin Circuitry

There is 50k pullup resistor internally on $\overline{FLT}$ and RDY pins. The $\overline{FLT}$ and RDY pin is an open-drain output. A 10-k Ω pullup resistor can be used to make it faster rise and to provide logic high when $\overline{FLT}$ and RDY is inactive, as shown in Figure 45

Fast common mode transients can inject noise and glitches on $\overline{FLT}$ and RDY pins due to parasitic coupling. This is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the $\overline{FLT}$ and RDY pins.



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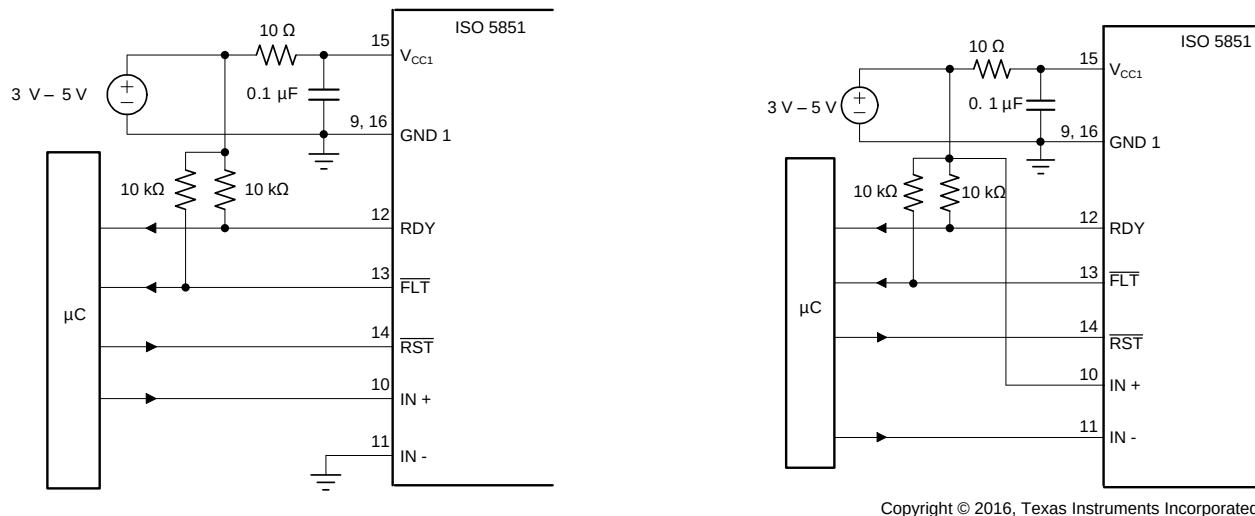
Figure 45. $\overline{FLT}$ and RDY Pin Circuitry for High CMTI

10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5851. For maximum CMTI performance, the digital control inputs, IN+ and IN–, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5851 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. There is a 20 ns glitch filter which can filter a glitch up to 20 ns on IN+ or IN–.

10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the $\overline{\text{FLT}}$ output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

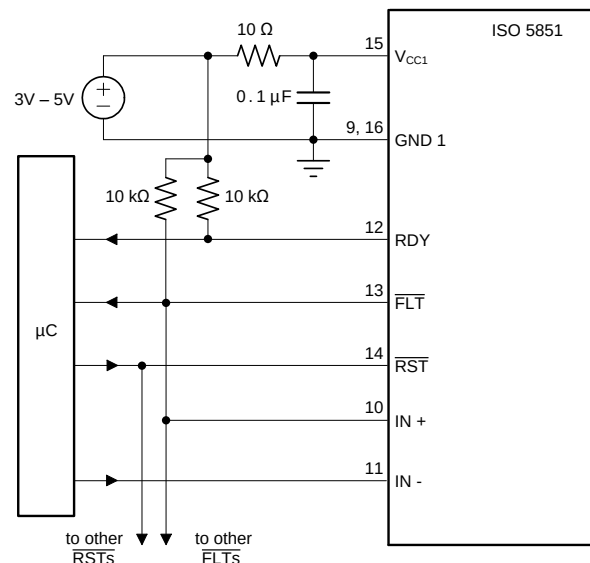


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Figure 46. Local Shutdown and Reset for Noninverting (Left) and Inverting Input Configuration (Right)

10.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5851 can be configured to shutdown automatically in the event of a fault condition by tying the $\overline{\text{FLT}}$ output to IN+. For high reliability drives, the open drain $\overline{\text{FLT}}$ outputs of multiple ISO5851 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low $\overline{\text{FLT}}$ output disables all six gate drivers simultaneously.



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Figure 47. Global Shutdown with Inverting Input Configuration

10.2.2.6 Auto-Reset

In this case, the gate control signal at IN+ is also applied to the $\overline{\text{RST}}$ input to reset the fault latch every switching cycle. Incorrect RST makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the 'gate low' state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before IN+ goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next 'on' cycle.

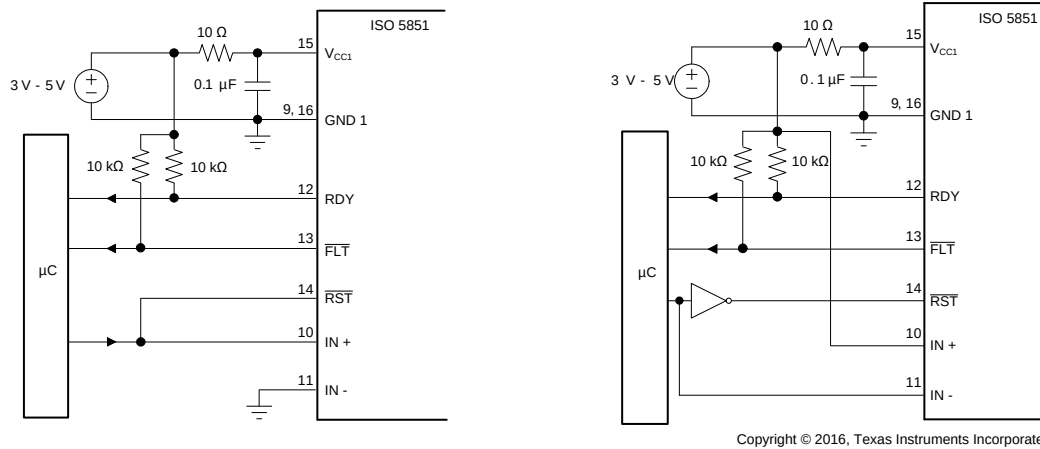


Figure 48. Auto Reset for Non-inverting and Inverting Input Configuration

10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to GND2 potential at low voltage levels.

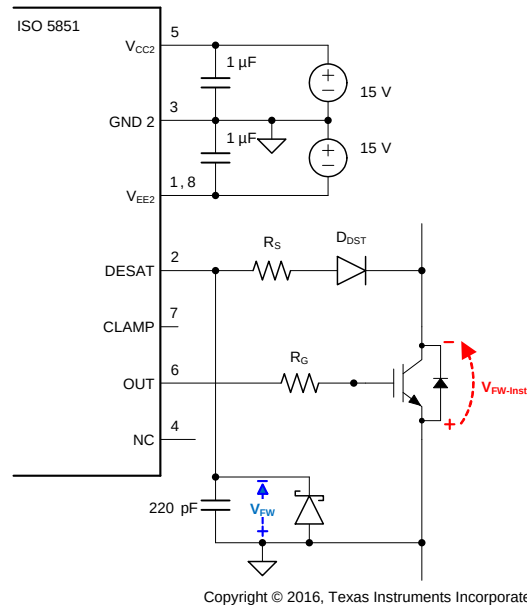


Figure 49. DESAT Pin Protection With Series Resistor and Schottky Diode

10.2.2.8 DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, $V_{(CESAT)}$, (when the IGBT is *on*) and to block high voltages (when the IGBT is *off*). During the short transition time when the IGBT is switching, there is commonly a high dV_{CE}/dt voltage ramp rate across the IGBT. This results in a charging current $I_{(CHARGE)} = C_{(D-DESAT)} \times dV_{CE}/dt$, charging the blanking capacitor. $C_{(D-DESAT)}$ is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of $1 + C_{(BLANK)} / C_{(D-DESAT)}$.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{(DESAT)}$, the V_{CE} level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: $V_{CE-FAULT(TH)} = 9\text{ V} - n \times V_F$ (where n is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

10.2.2.9 Determining the Maximum Available, Dynamic Output Power, P_{OD-max}

The ISO5851 maximum allowed total power consumption of $P_D = 251\text{ mW}$ consists of the total input power, P_{ID} , the total output power, P_{OD} , and the output power under load, P_{OL} :

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (1)$$

With:

$$P_{ID} = V_{CC1-max} \times I_{CC1-max} = 5.5\text{ V} \times 4.5\text{ mA} = 24.75\text{ mW} \quad (2)$$

and:

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{CC2-max} = (15\text{ V} - (-8\text{ V})) \times 6\text{ mA} = 138\text{ mW} \quad (3)$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251\text{ mW} - 24.75\text{ mW} - 138\text{ mW} = 88.25\text{ mW} \quad (4)$$

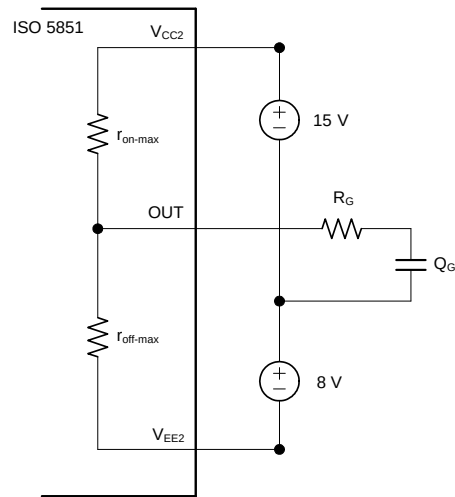
In comparison to P_{OL} , the actual dynamic output power under worst case condition, P_{OL-WC} , depends on a variety of parameters:

$$P_{OL-WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left(\frac{r_{on-max}}{r_{on-max} + R_G} + \frac{r_{off-max}}{r_{off-max} + R_G} \right)$$

where

- f_{INP} = signal frequency at the control input IN+
 - Q_G = power device gate charge
 - V_{CC2} = positive output supply with respect to GND2
 - V_{EE2} = negative output supply with respect to GND2
 - r_{on-max} = worst case output resistance in the on-state: 4Ω
 - $r_{off-max}$ = worst case output resistance in the off-state: 2.5Ω
 - R_G = gate resistor
- (5)

Once R_G is determined, [Equation 5](#) is to be used to verify whether $P_{OL-WC} < P_{OL}$. [Figure 50](#) shows a simplified output stage model for calculating P_{OL-WC} .



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Figure 50. Simplified Output Model for Calculating P_{OL-WC}

10.2.2.10 Example

This examples considers an IGBT drive with the following parameters:

$$I_{ON-PK} = 2 \text{ A}, Q_G = 650 \text{ nC}, f_{INP} = 20 \text{ kHz}, V_{CC2} = 15 \text{ V}, V_{EE2} = -8 \text{ V} \quad (6)$$

Applying the value of the gate resistor $R_G = 10 \Omega$.

Then, calculating the worst-case output power consumption as a function of R_G , using Equation 5 r_{on-max} = worst case output resistance in the on-state: 4Ω , $r_{off-max}$ = worst case output resistance in the off-state: 2.5Ω , R_G = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20 \text{ kHz} \times 650 \text{ nC} \times (15 \text{ V} - (-8 \text{ V})) \times \left(\frac{4 \Omega}{4 \Omega + 10 \Omega} + \frac{2.5 \Omega}{2.5 \Omega + 10 \Omega} \right) = 72.61 \text{ mW} \quad (7)$$

Because $P_{OL-WC} = 72.61 \text{ mW}$ is below the calculated maximum of $P_{OL} = 88.25 \text{ mW}$, the resistor value of $R_G = 10 \Omega$ is suitable for this application.

10.2.2.11 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in [Figure 51](#)) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.

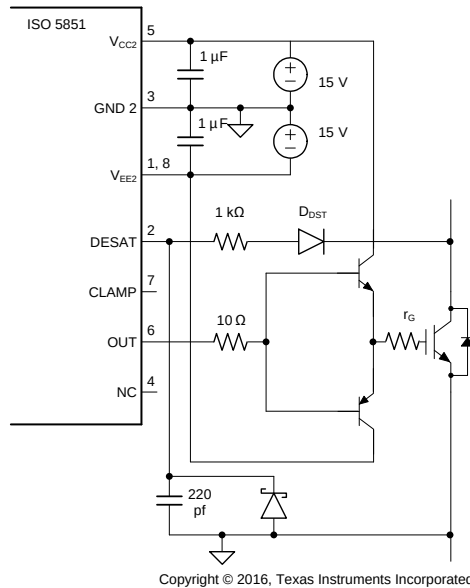


Figure 51. Current Buffer for Increased Drive Current

10.2.3 Application Curves

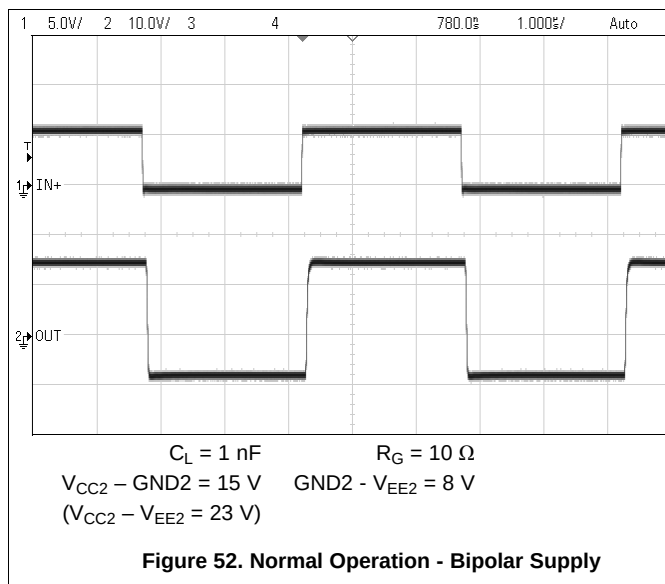


Figure 52. Normal Operation - Bipolar Supply

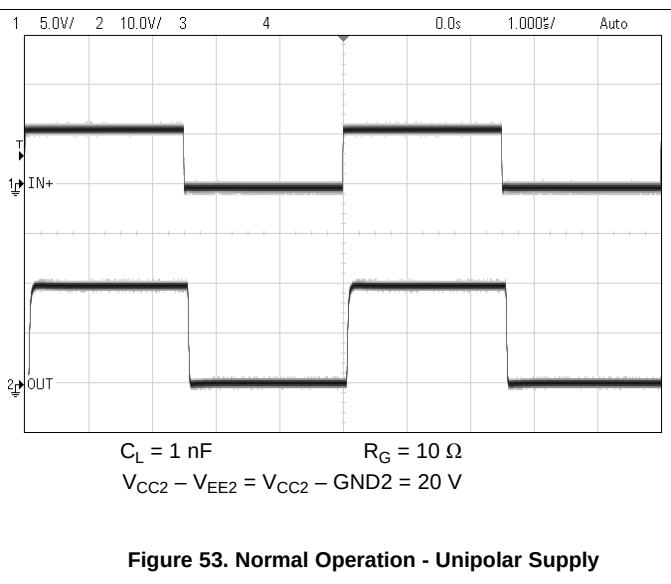


Figure 53. Normal Operation - Unipolar Supply

11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at input supply pin V_{CC1} and 1- μ F bypass capacitor is recommended at output supply pin V_{CC2} . The capacitors should be placed as close to the supply pins as possible. The recommended placement of the capacitors is 2-mm maximum from the input and output power supply pin (V_{CC1} and V_{CC2}).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 54](#)). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output OUT and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch². On the gate-driver V_{EE2} and V_{CC2} can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For detailed layout recommendations, see the [Digital Isolator Design Guide](#) (SLLA284).

12.2 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.3 Layout Example

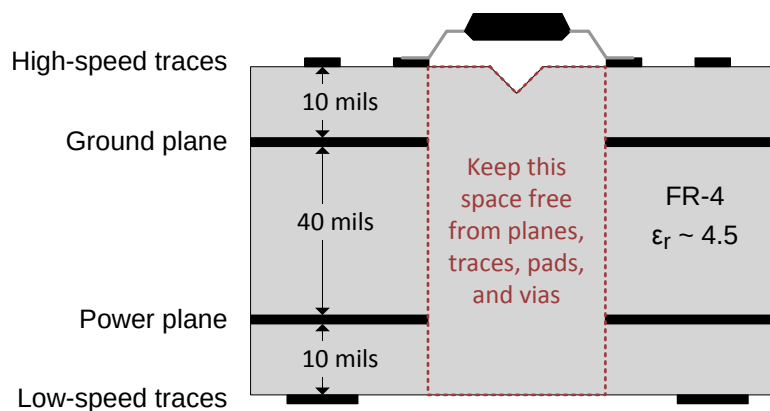


Figure 54. Recommended Layer Stack

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

相关文档如下：

- [《ISO5851 评估模块 \(EVM\) 用户指南》](#)
- [数字隔离器设计指南](#)
- [隔离相关术语](#)

13.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

13.3 社区资源

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

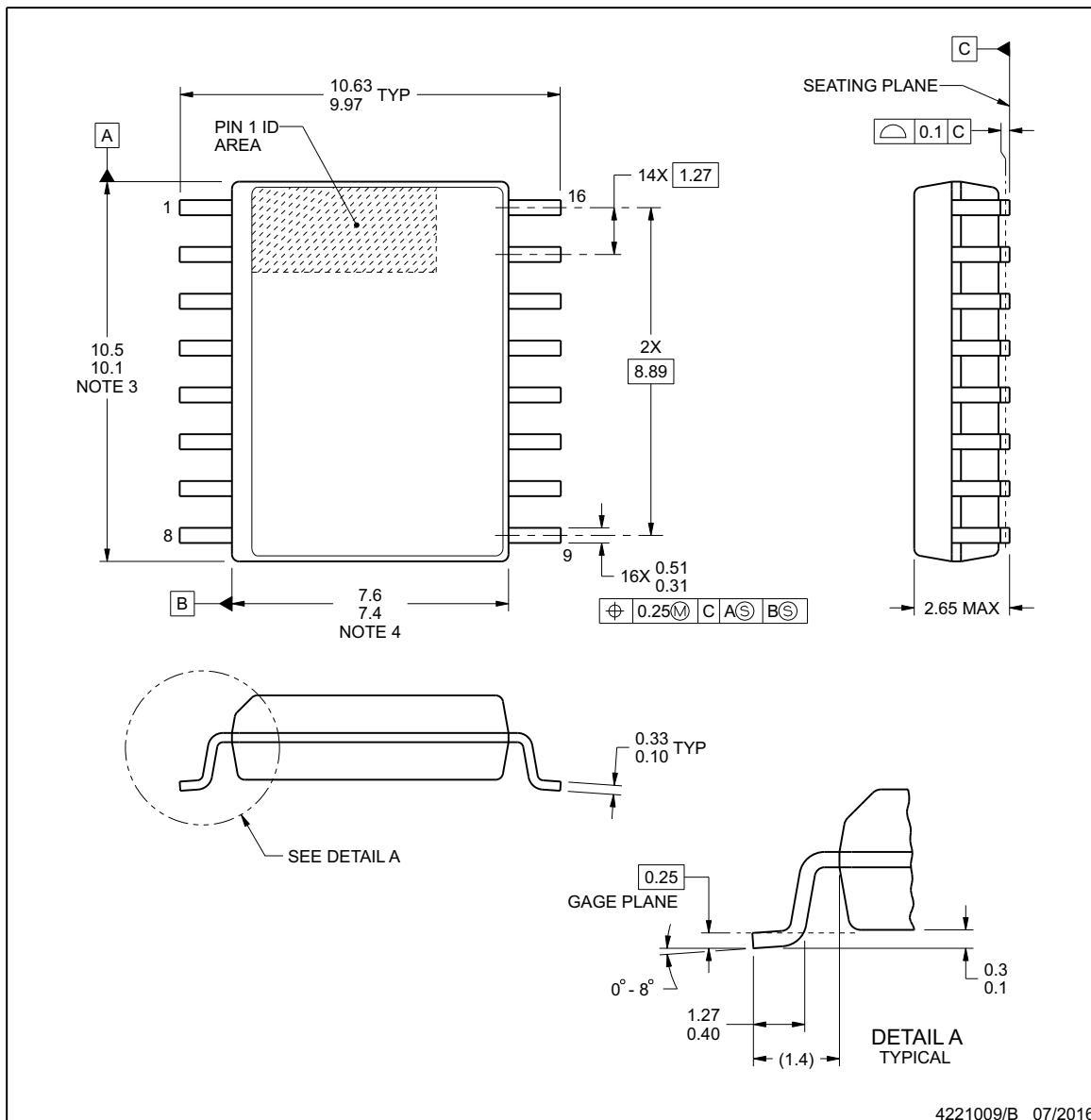
This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。


DW0016B
PACKAGE OUTLINE
SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

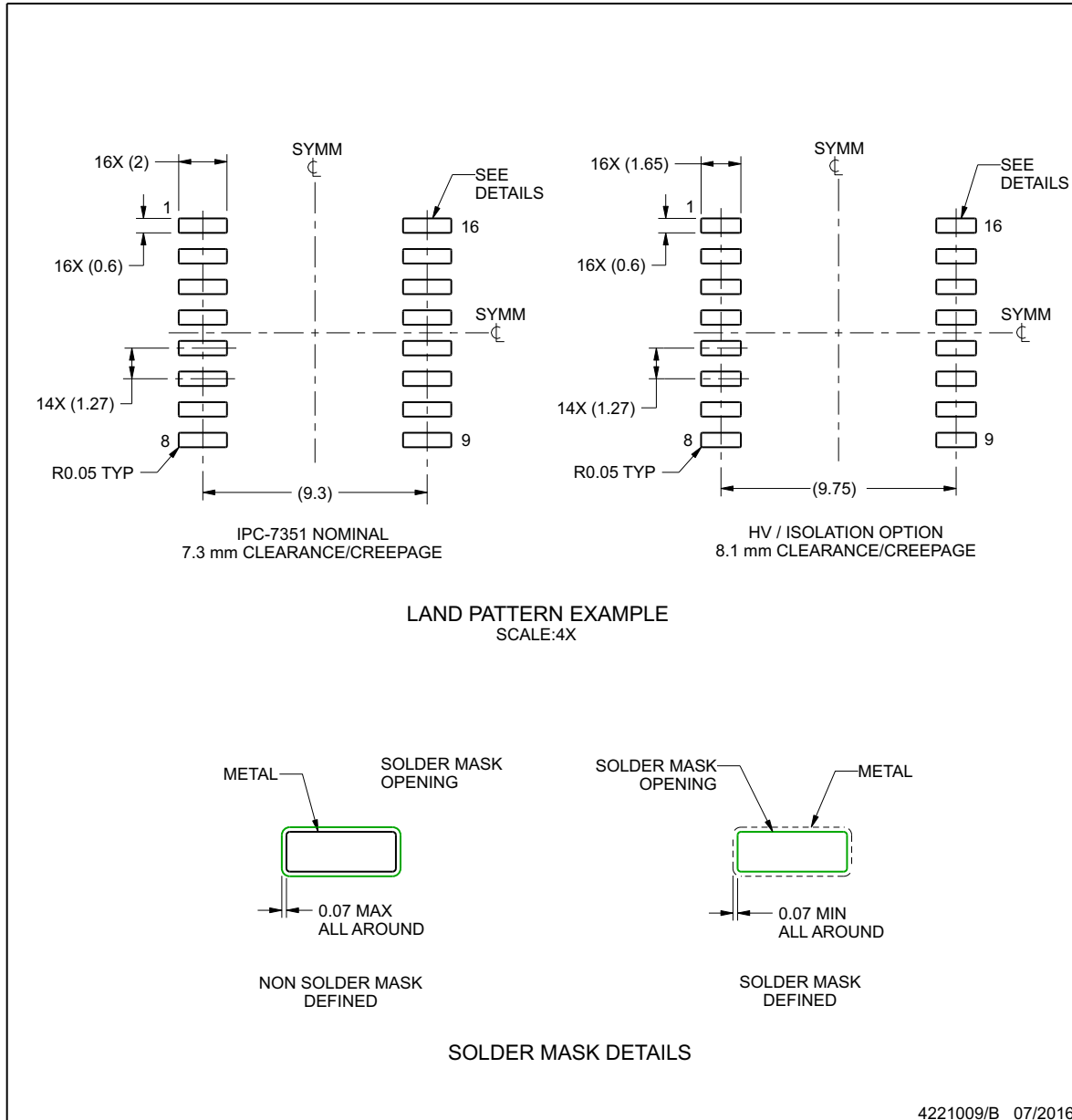
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



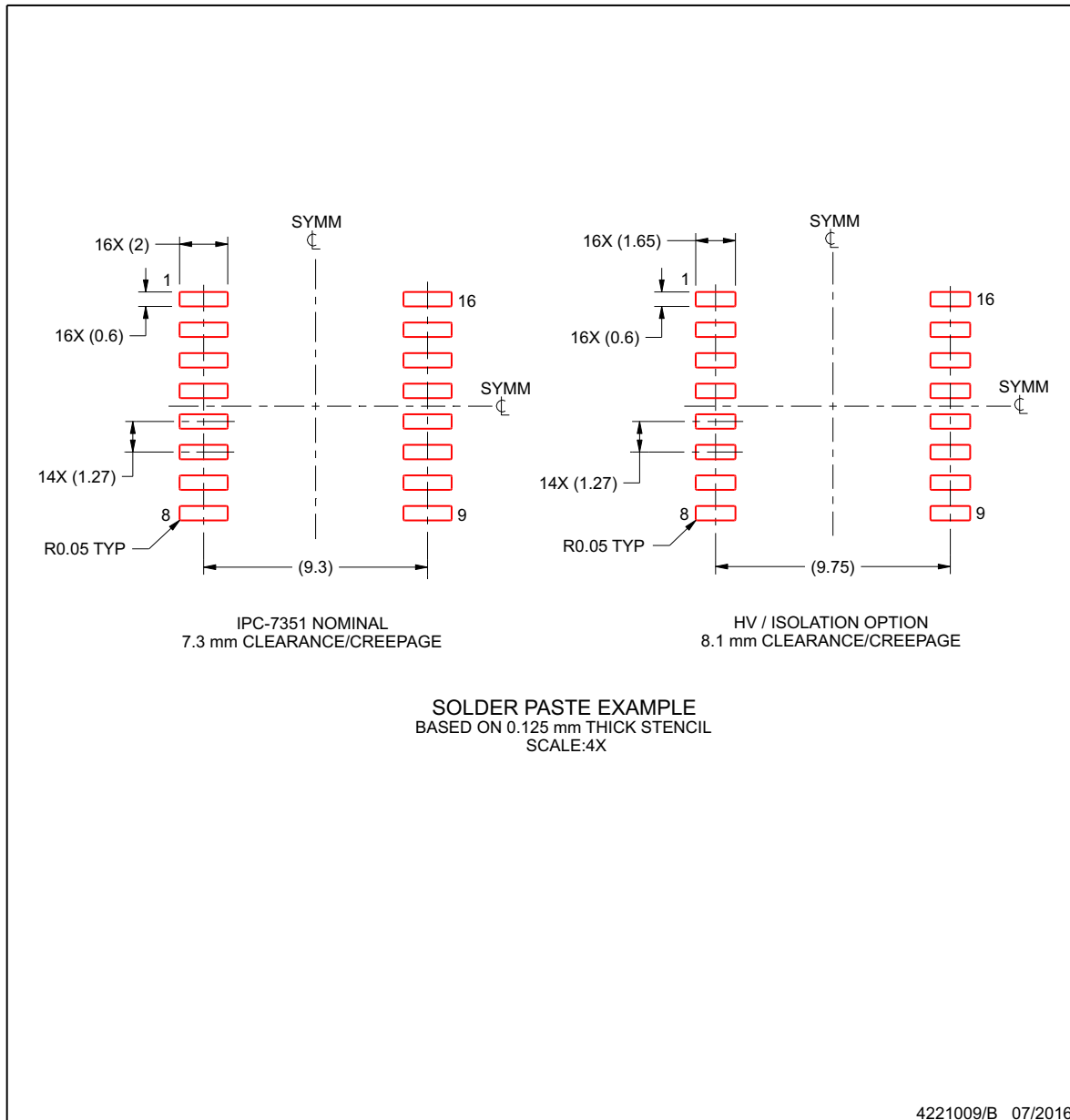
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B
SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO5851DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5851	Samples
ISO5851DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5851	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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