双路低电压 H 桥集成电路 (IC)

查询样片: **DRV8836**

特性

- 双 **H** 桥电机驱动器
  - 能够驱动两个直流电机或者一个步进电机
  - 低金属氧化物半导体场效应晶体管 **(MOSFET)** 导通电阻：
    高侧 **+** 低侧 **(HS + LS) 305 mΩ**
- 每个 **H** 桥 **1.5A** 的最大驱动电流
- 两桥并联可实现 **3A** 的驱动电流
- **2V** 至 **7V** 运行电源电压范围
- 灵活的脉宽调制 **(PWM)** 或者相位**/**使能接口
- 具有 **95nA** 最大电源电流的低功耗睡眠模式
- 专用 **SLEEPn** 输入引脚
- 极小型 **2mm x 3mm** 晶圆级小外形尺寸无引线 **(WSON)** 封装

应用范围

- 由电池供电的设备：
  - 数字单镜头反光 **(DSLR)** 镜头
  - 消费类产品
  - 玩具
  - 机器人技术
  - 摄像机
  - 医疗设备

说明

DRV8836 为摄像机、消费类产品、玩具、和其它低电压或者电池供电的运动控制类应用提供了一个集成的电机驱动器解决方案。 此器件有两个 H 桥驱动器，能够驱动两个直流电机或者一个步进电机，以及其它诸如螺线管在内的器件。 每个输出驱动器功能块包括配置为 H 桥的 N 通道功率 MOSFET 以驱动电机绕组。 一个内部电荷泵生成所需的栅极驱动电压。

DRV8836 的每个 H 桥能够提供高达 1.5A 的输出电流。 供电电压范围介于 2V 至 7V。

可选择的相位/使能和 IN/IN 接口与工业标准器件兼容。 可通过关闭所有不必要的逻辑电路来提供低功耗睡眠模式，消耗极低的电流。

内部关断功能支持过流保护、短路保护、欠压闭锁以及过温保护。

DRV8836 采用具有 PowerPAD™ 的极小型 12 引脚 WSON 封装（环保型：符合 RoHS 标准且不含 Sb/Br）。

ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
PowerPAD™ (WSON) - DSS	Reel of 3000	DRV8836DSSR	836

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: SLVSB17

DEVICE INFORMATION

Functional Block Diagram

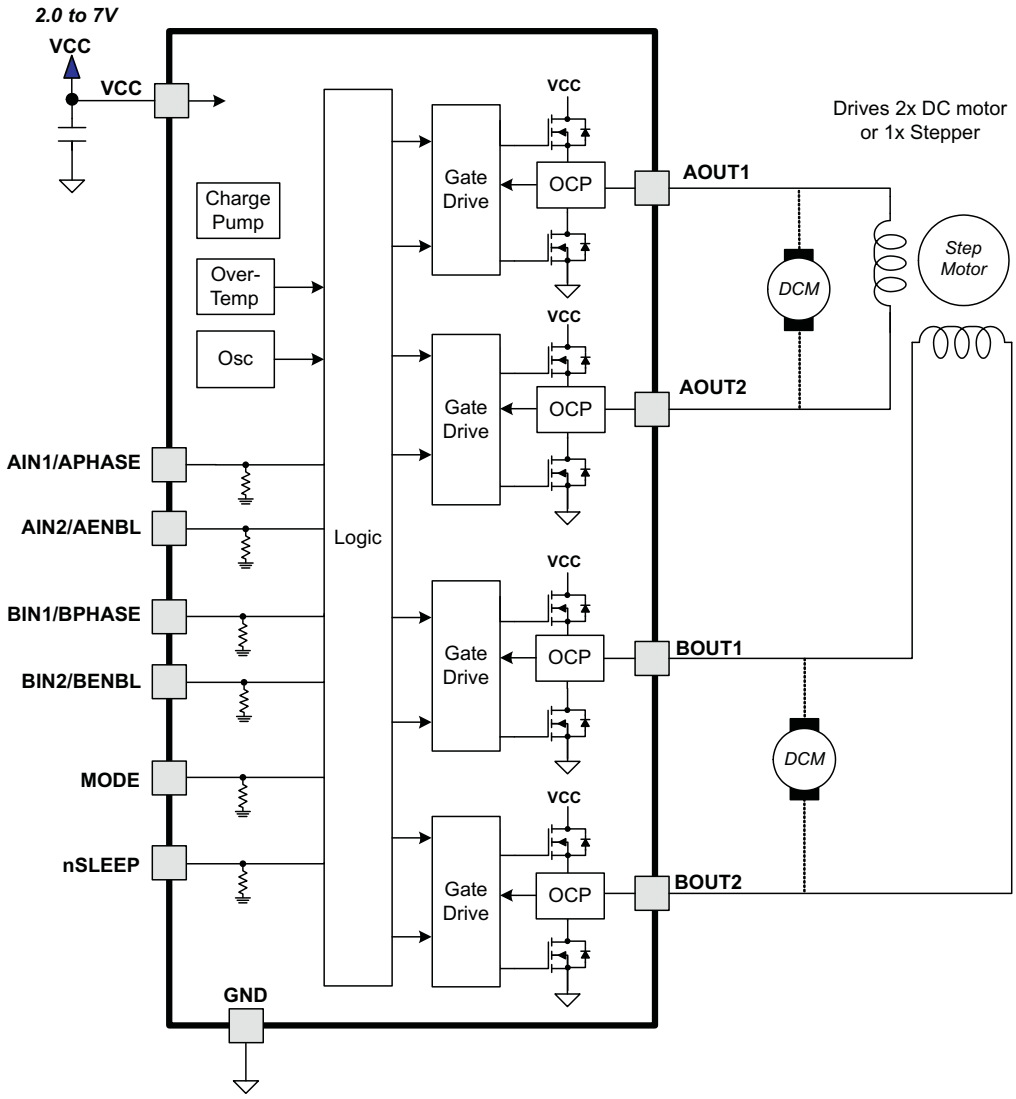

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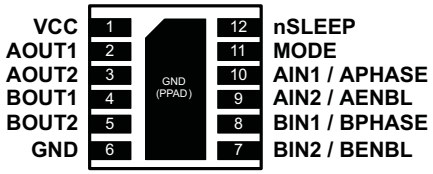
Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	6	-	Device ground	
VCC	1	-	Device and motor supply	Bypass to GND with a 0.1-μF (minimum) ceramic capacitor.
CONTROL				
nSLEEP	12	I	Sleep input	Active low places part in low-power sleep state. Internal pulldown resistor
MODE	11	I	Input mode select	Logic low selects IN/IN mode. Logic high selects PH/EN mode. Internal pulldown resistor.
AIN1/APHASE	10	I	Bridge A input 1/PHASE input	IN/IN mode: Logic high sets AOUT1 high. PH/EN mode: Sets direction of H-bridge A. Internal pulldown resistor.
AIN2/AENBL	9	I	Bridge A input 2/ENABLE input	IN/IN mode: Logic high sets AOUT2 high. PH/EN mode: Logic high enables H-bridge A. Internal pulldown resistor.
BIN1/BPHASE	8	I	Bridge B input 1/PHASE input	IN/IN mode: Logic high sets BOUT1 high. PH/EN mode: Sets direction of H-bridge B. Internal pulldown resistor.
BIN2/BENBL	7	I	Bridge B input 2/ENABLE input	IN/IN mode: Logic high sets BOUT2 high. PH/EN mode: Logic high enables H-bridge B. Internal pulldown resistor.
OUTPUT				
AOUT1	2	O	Bridge A output 1	Connect to motor winding A
AOUT2	3	O	Bridge A output 2	
BOUT1	4	O	Bridge B output 1	Connect to motor winding B
BOUT2	5	O	Bridge B output 2	

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DSS PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE	UNIT
VCC	Power supply voltage range	-0.3 to 7	V
	Digital input pin voltage range	–0.5 to VCC + 0.5	V
	Peak motor drive output current	Internally limited	A
	Continuous motor drive output current per H-bridge(3)	1.5	A
T_J	Operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

THERMAL METRIC		DRV8836 DSS 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	50.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	58	
θ_{JB}	Junction-to-board thermal resistance(3)	19.9	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(5)	20	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	6.9	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device power supply voltage range	2		7	V
I_{OUT}	H-bridge output current(1)	0		1.5	A
f_{PWM}	Externally applied PWM frequency	0		250	kHz
V_{IN}	Logic level input voltage	0		V_{CC}	V

(1) Power dissipation and thermal limits must be observed.

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VCC}	VCC operating supply current	f_{PWM} = 50 kHz, no load		1.7	2.5	mA
I_{CCQ}	VCC sleep mode supply current	nSLEEP = 0 V, all inputs 0 V		40	95	nA
		V_{CC} = 3 V, nSLEEP = 0 V, all inputs 0 V		10		
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			2	V
		V_{CC} falling			1.9	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.25 x V_{CC}	V
V_{IH}	Input high voltage		0.5 x V_{CC}			V
I_{IL}	Input low current	V_{IN} = 0	-5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS + LS FET on resistance	V_{CC} = 3 V, I_O = 800 mA, T_J = 25°C		370	420	mΩ
		V_{CC} = 5 V, I_O = 800 mA, T_J = 25°C		305	355	
I_{OFF}	Off-state leakage current				±200	nA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.6		3.5	A
t_{DEG}	Overcurrent deglitch time			1		µs
t_{OCR}	Overcurrent protection retry time			1		ms
t_{DEAD}	Output dead time			100		ns
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

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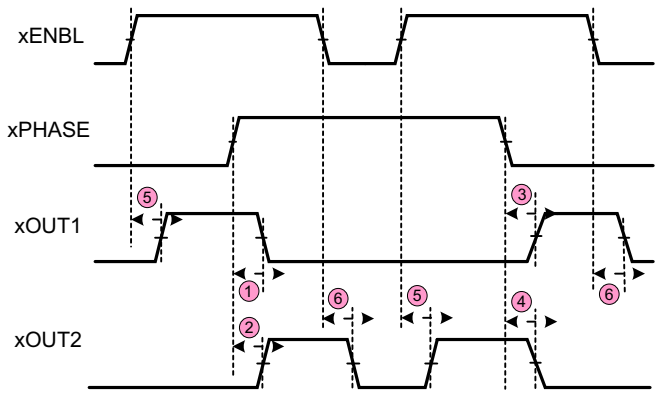
TIMING REQUIREMENTS(1)

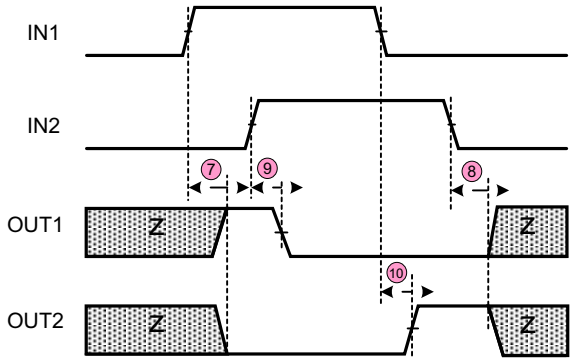
T_A = 25°C, V_{CC} = 5 V, R_L = 20 Ω

NO.	PARAMETER	CONDITIONS	MIN	MAX	UNIT
1	t_1	Delay time, xPHASE high to xOUT1 low		210	ns
2	t_2	Delay time, xPHASE high to xOUT2 high		150	ns
3	t_3	Delay time, xPHASE low to xOUT1 high		150	ns
4	t_4	Delay time, xPHASE low to xOUT2 low		210	ns
5	t_5	Delay time, xENBL high to xOUTx high		150	ns
6	t_6	Delay time, xENBL high to xOUTx low		150	ns
7	t_7	Output enable time		210	ns
8	t_8	Output disable time		210	ns
9	t_9	Delay time, xINx high to xOUTx high		125	ns
10	t_{10}	Delay time, xINx low to xOUTx low		125	ns
11	t_R	Output rise time	20	188	ns
12	t_F	Output fall time	8	30	ns

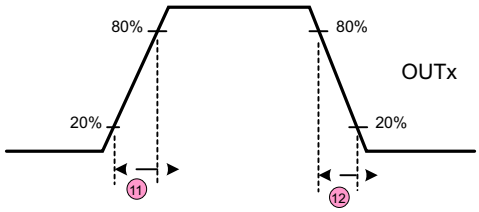
(1) Not production tested – ensured by design



PHASE/ENBL mode



IN/IN mode



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FUNCTIONAL DESCRIPTION

Bridge Control

Two control modes are available in the DRV8836: IN/IN mode, and PHASE/ENABLE mode. IN/IN mode is selected if the MODE pin is driven low or left unconnected; PHASE/ENABLE mode is selected if the MODE pin is driven to logic high. The following tables show the logic for these modes.

Table 2. IN/IN MODE

MODE	xIN1	xIN2	xOUT1	xOUT2	FUNCTION (DC MOTOR)
0	0	0	Z	Z	Coast
0	0	1	L	H	Reverse
0	1	0	H	L	Forward
0	1	1	L	L	Brake

Table 3. PHASE/ENABLE MODE

MODE	xENABLE	xPHASE	xOUT1	xOUT2	FUNCTION (DC MOTOR)
1	0	X	L	L	Brake
1	1	1	L	H	Reverse
1	1	0	H	L	Forward

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8836 will enter a low-power sleep mode. In this state all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

There is a weak pulldown resistor (approximately 100 kΩ) to ground on the input pins.

Protection Circuits

The DRV8836 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled. After approximately 1 ms, the bridge will be re-enabled automatically.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VCC rises above the UVLO threshold.

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APPLICATIONS INFORMATION

Parallel Mode

The two H-bridges in the DRV8836 can be connected in parallel for double the current of a single H-bridge. The drawing below shows the connections.

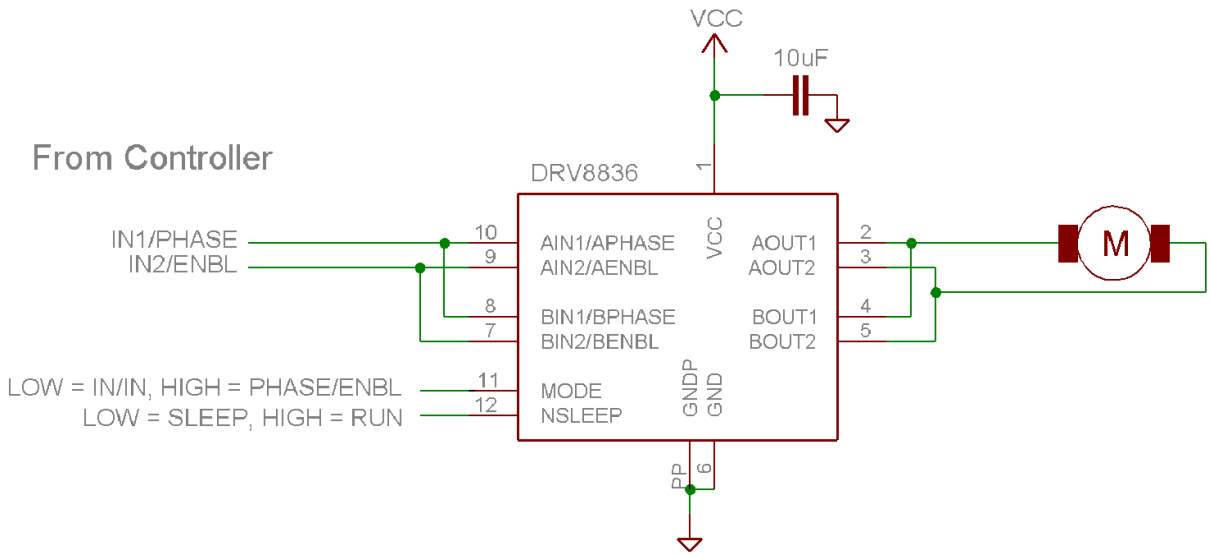

Figure 1. Parallel Mode Connections

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THERMAL INFORMATION

Thermal Protection

The DRV8836 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8836 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation when running both H-bridges can be roughly estimated by:

$$P_{TOT} = 2 \times R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

Where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 2 comes from the fact that there are two H-bridges.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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修订历史记录

Changes from Revision A (September 2013) to Revision B	Page
• Added t_{OCR} and t_{DEAD} parameters to ELECTRICAL CHARACTERISTICS	5

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8836DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	836	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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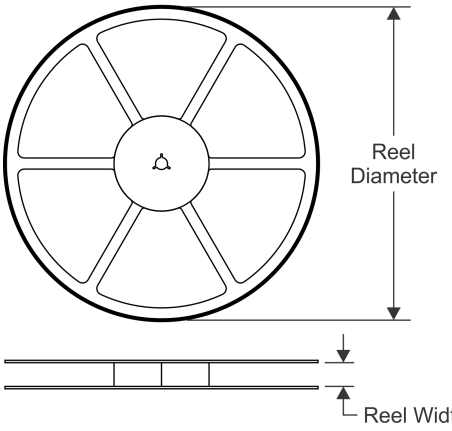
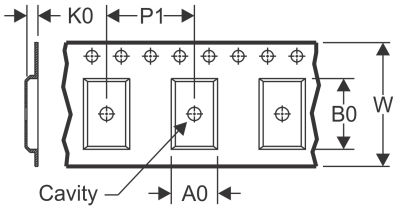
TAPE AND REEL INFORMATION

REEL DIMENSIONS

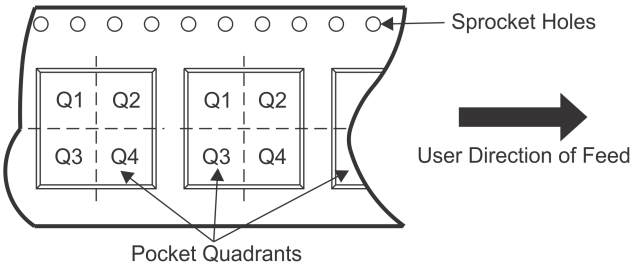


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

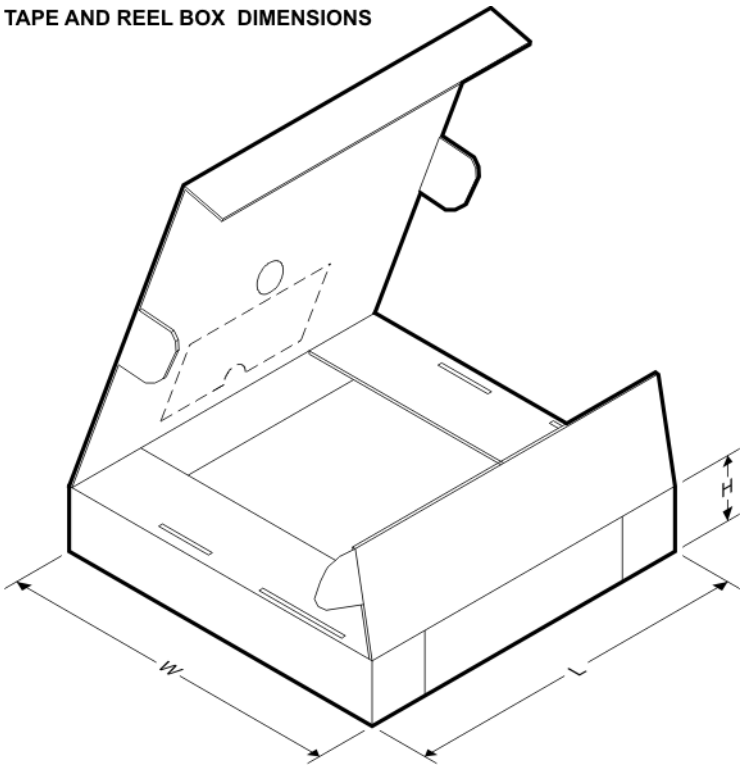
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

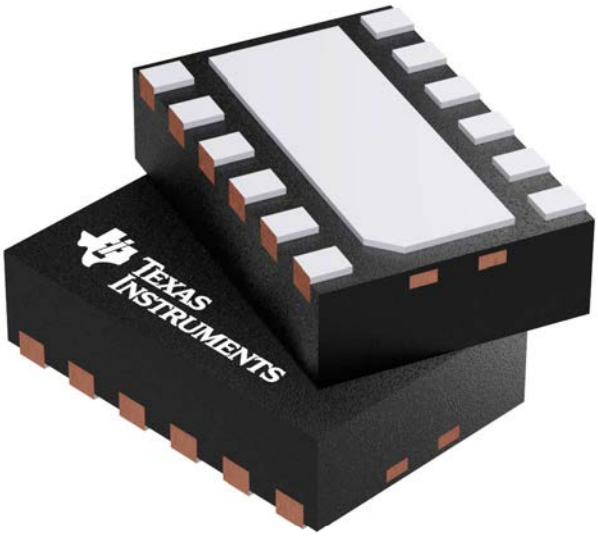
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8836DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

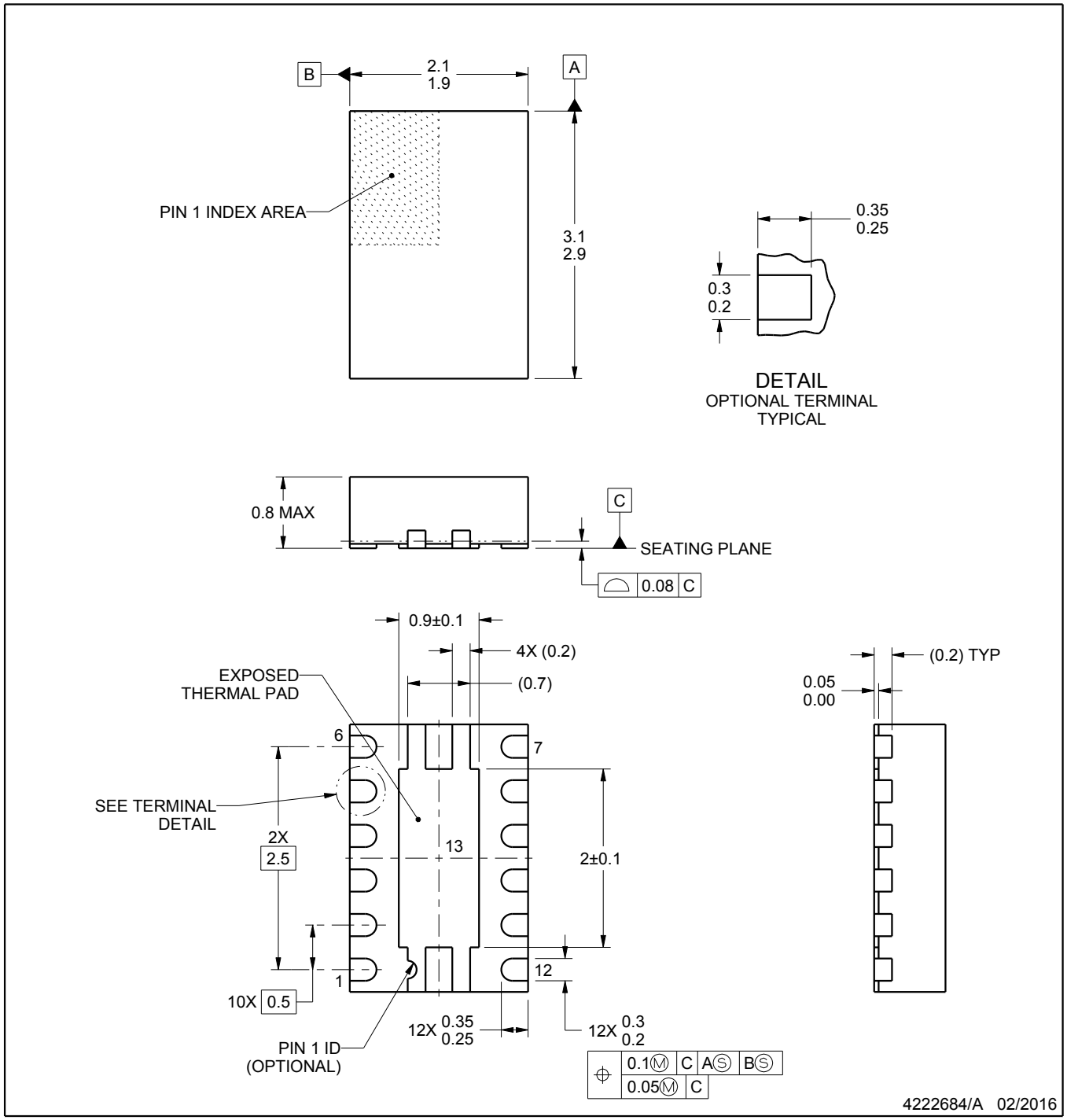


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8836DSSR	WSON	DSS	12	3000	210.0	185.0	35.0

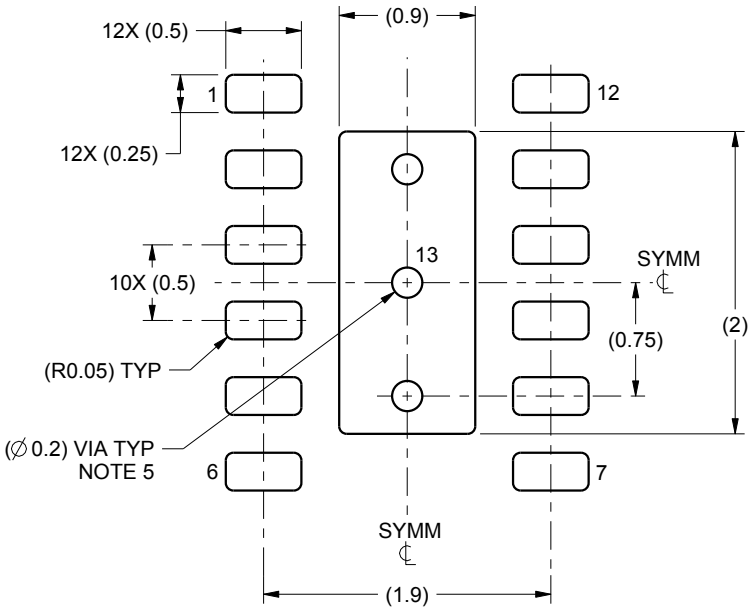


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

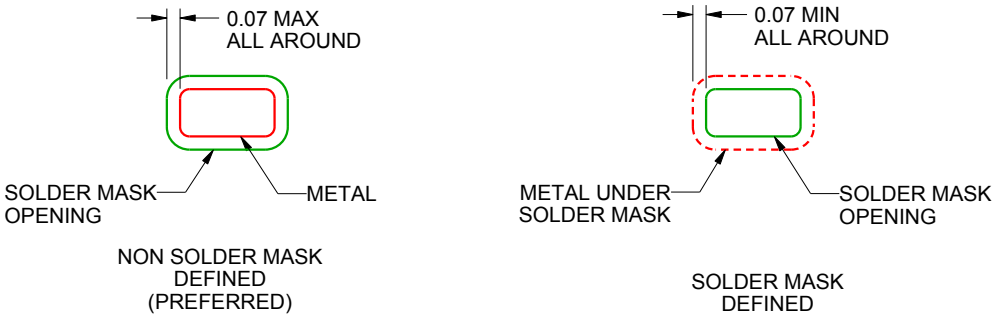


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

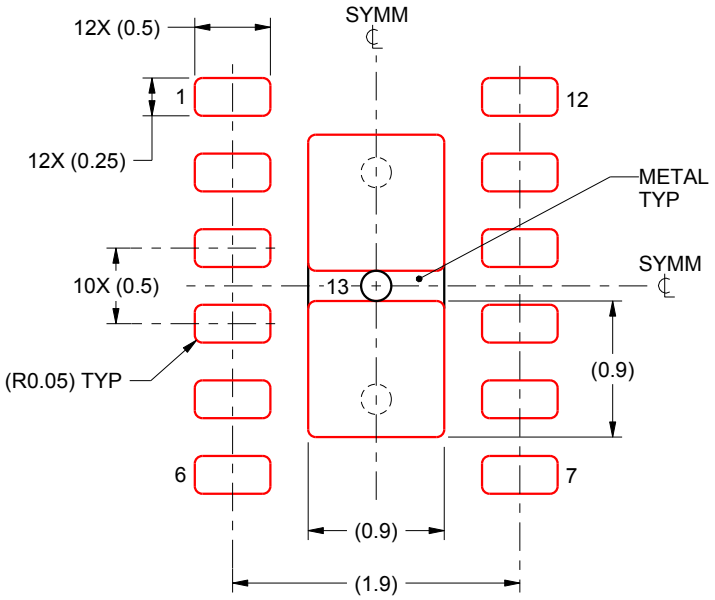


SOLDER MASK DETAILS

4222684/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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