



DRV8801A-Q1 DMOS 全桥电机驱动器

1 特性

- 符合汽车应用要求
- 低导通电阻 (0.83Ω) 输出
- 低功耗睡眠模式
- 支持 100% PWM
- 6.5 至 36V 宽电源电压范围
- 耐热增强型表面贴装封装
- 可配置过流限制
- 保护特性
 - V_{BB} 欠压闭锁 (UVLO)
 - 过流保护 (OCP)
 - 电源短路保护
 - 接地短路保护
 - 过热警告 (OTW)
 - 过热关断 (OTS)
 - 引脚 (nFAULT) 指示过流和过热故障条件

2 应用

- 汽车车身系统
- 车门锁
- 加热、通风和空调环境系统 (HVAC) 传动器
- 压电报警

3 说明

DRV8801A-Q1 器件配有 H 桥驱动器，可提供多用途电机驱动器解决方案。此器件能够驱动一个有刷直流电机或者步进电机的一个绕组，以及其它诸如螺线管等器件。一个简单的 PHASE 和 ENABLE 接口可轻松连接到控制器电路。

输出级使用配置为 H 桥的 N 通道功率 MOSFET。

DRV8801A-Q1 器件能够提供高达 $\pm 2.8A$ 的峰值输出电流，承受高达 36V 的工作电压。可通过一个内部电荷泵产生所需的栅极驱动电压。

低功耗睡眠模式可将部分内部电路关断，以实现极低的静态电流和功耗。可使用一个专用的 nSLEEP 引脚来设定这个睡眠模式。

提供的内部保护功能包括欠压闭锁、过流保护、电源短路保护、接地短路保护、过热警告和过热关断。过流（包括接地短路和电源短路）和过热故障条件由 nFAULT 引脚指示。

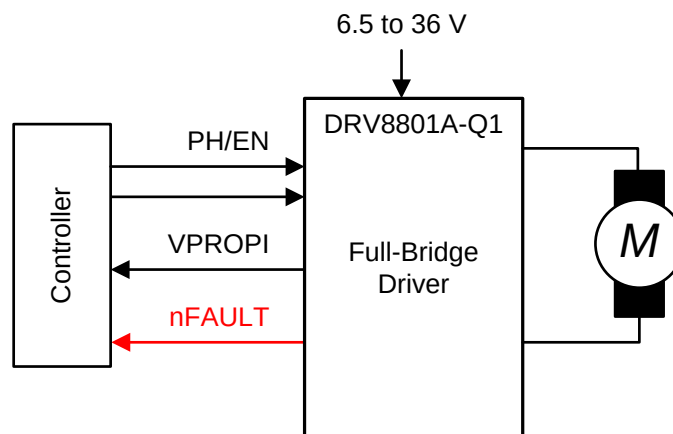
DRV8801A-Q1 器件采用 PowerPAD™ 16 引脚超薄型四方扁平无引线 (WQFN) 封装（环保型：符合 RoHS 标准且不含镉/溴）。

器件信息⁽¹⁾

部件号	封装	封装尺寸（标称值）
DRV8801A-Q1	WQFN (16)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用示意图



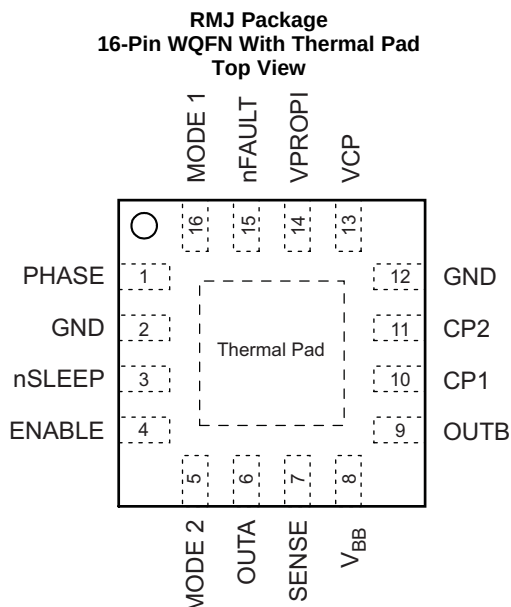
目录

1	特性	1	7.3	Feature Description	9
2	应用	1	7.4	Device Functional Modes	12
3	说明	1	8	Application and Implementation	13
4	修订历史记录	2	8.1	Application Information	13
5	Pin Configuration and Functions	3	8.2	Typical Application	13
6	Specifications	4	9	Power Supply Recommendations	15
6.1	Absolute Maximum Ratings	4	9.1	Bulk Capacitance	15
6.2	Handling Ratings	4	10	Layout	16
6.3	Recommended Operating Conditions	4	10.1	Layout Guidelines	16
6.4	Thermal Information	5	10.2	Layout Example	16
6.5	Dissipation Ratings	5	10.3	Power Dissipation	16
6.6	Electrical Characteristics	6	11	器件和文档支持	17
6.7	Typical Characteristics	7	11.1	商标	17
7	Detailed Description	8	11.2	静电放电警告	17
7.1	Overview	8	11.3	术语表	17
7.2	Functional Block Diagram	8	12	机械封装和可订购信息	17

4 修订历史记录

Changes from Original (June 2014) to Revision A	Page
• Added TYPE column to the <i>Pin Functions</i> table	3
• Updated the <i>Overcurrent Control Timing</i> image	11

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CP1	10	—	Charge-pump capacitor 1
CP2	11	—	Charge-pump capacitor 2
ENABLE	4	I	Enables OUTA and OUTB drivers
GND	2	PWR	Ground
	12		
MODE 1	16	I	Mode logic input
MODE 2	5	I	Mode 2 logic input
nFAULT	15	OD	Fault open-drain output. A logic low indicates fault a condition
nSLEEP	3	I	Logic low puts the device in a low-power sleep mode
OUTA	6	O	DMOS full-bridge output positive. H-Bridge output A
OUTB	9	O	DMOS full-bridge output negative. H-Bridge output B
PHASE	1	I	Phase logic input for direction control
SENSE	7	IO	Sense power return
V _{BB}	8	PWR	Driver supply voltage
VCP	13	—	Charge-pump reservoir capacitor pin
VPROPI	14	O	Winding current proportional voltage output
Thermal pad		—	Exposed pad for thermal dissipation; connect to GND pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Power supply voltage ⁽²⁾	V _{BB}	–0.3	40	V
Charge pump voltage	VCP, CP1, and CP2	–0.3	V _{BB} + 7	V
Digital pin voltage	PHASE, ENABLE, MODE1, MODE2, nSLEEP, nFAULT	–0.3	7	V
V _{BB} to OUTx voltage	OUTA and OUTB	–0.3	36	V
OUTx to GND voltage	OUTA and OUTB	–0.3	36	V
Sense pin voltage	SENSE	–0.5	0.5	V
H-bridge output current	OUTA, OUTB, and SENSE		2.8	A
VPROPI pin voltage	VPROPI	–0.3	3.6	V
Maximum junction temperature, T _J			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

6.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		–40	125	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	–750	750	
		Other pins	–500	500	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{BB}	Power supply voltage	6.5	36	V
V _{CC}	Logic supply voltage	0	5.5	V
f _(PWM)	Applied PWM signal (PHASE and ENABLE)	0	100	kHz
I _O	H-bridge peak output current	0	2.8	A
T _A	Ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		RMJ 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾	36.8	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance ⁽³⁾	43.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance ⁽⁴⁾	14.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	14.7	°C/W
$R_{\theta JCbott}$	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	4.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, Ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Dissipation Ratings

PACKAGE	$R_{\theta JA}$	$T_A = 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$
RMJ	36.8	3 W	27 mW/°C

6.6 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (V _{BB})							
V _{BB}	V _{BB} operating supply voltage			6.5		36	V
I _{BB}	V _{BB} operating supply current	f _{PWM} < 50 kHz		6			mA
		Charge pump on, Outputs disabled		3.2			
I _{BB(Q)}	V _{BB} sleep-mode supply current	nSLEEP = 0, T _J = 25°C				10	μA
CONTROL INPUTS (PHASE, ENABLE, MODE1, MODE2, nSLEEP)							
V _{IL}	Input logic low voltage	PHASE, ENABLE, MODE1, MODE2				0.8	V
V _{IH}	Input logic high voltage			2			
I _{IL}	Input logic low current	PHASE, ENABLE, MODE1, MODE2	V _I = 0.8 V	–20	≤ –2	20	μA
I _{IH}	Input logic high current		V _I = 2 V	< 1		20	
I _{IL}	Input logic low current	ENABLE	V _I = 0.8 V	16		40	μA
I _{IH}	Input logic high current		V _I = 2 V	40		100	
V _{IL}	Input logic low voltage	nSLEEP			0.8		V
V _{IH}	Input logic high voltage				2.7		
I _{IL}	Input logic low current		V _I = 0.8 V		< 1	10	μA
I _{IH}	Input logic high current		V _I = 2 V		27	50	
CONTROL OUTPUTS (nFAULT)							
V _{OL}	Output logic low voltage	I _O = 1 mA				0.4	V
DMOS DRIVERS (OUTA, OUTB, SENSE, VPROPI)							
r _{DS(on)}	Output ON resistance	Source driver, I _O = –2.8 A, T _J = 25°C , V _{BB} = 6.5 to 36 V		0.48			Ω
		Source driver, I _O = –2.8 A, T _J = 125°C, V _{BB} = 8 to 36 V		0.74	0.85		
		Source driver, I _O = –2.8 A, T _J = 25°C, V _{BB} = 6.5 to 8 V		0.74	0.9		
		Sink driver, I _O = 2.8 A, T _J = 125°C, V _{BB} = 6.5 to 36 V		0.35			
		Sink driver, I _O = 2.8 A, T _J = 125°C, V _{BB} = 8 to 36 V		0.52	0.7		
		Sink driver, I _O = 2.8 A, T _J = 125°C, V _{BB} = 6.5 to 8 V		0.52	0.75		
V _(TRIP)	SENSE trip voltage	R _(SENSE) between SENSE and GND		450	500	550	mV
V _f	Body diode forward voltage	Source diode, I _f = –2.8 A				1.4	V
		Sink diode, I _f = 2.8 A				1.4	
t _{pd}	Propagation delay time	Input edge to source or sink ON		600			ns
		Input edge to source or sink OFF		100			
t _{COD}	Crossover delay			500			ns
G _{D(a)}	Differential amplifier gain	V _{BB} = 8 to 36 V; SENSE = 0.1 to 0.4 V		4.8	5	5.2	V/V
		V _{BB} = 6.5 to 8 V; SENSE = 0.1 to 0.3 V		4.8		5.2	V/V
PROTECTION CIRCUITS							
V _{UV}	UVLO threshold	V _{BB} increasing		5.5		6.4	V
		V _{BB} decreasing				5.7	
I _(OCP)	Overcurrent protection trip level	V _{BB} = 8 to 36 V		3			A
		V _{BB} = 6.5 to 8 V		2.8			A
t _(DEG)	Overcurrent deglitch time			3			μs
t _(OCP)	Overcurrent retry time			1.2			ms
T _(OTW)	Thermal warning temperature	Die temperature T _J		160			°C
T _{hys(OTW)}	Thermal warning hysteresis	Die temperature T _J		15			°C
T _(OTS)	Thermal shutdown temperature	Die temperature T _J		175			°C
T _{hys(OTS)}	Thermal shutdown hysteresis	Die temperature T _J		15			°C

6.7 Typical Characteristics

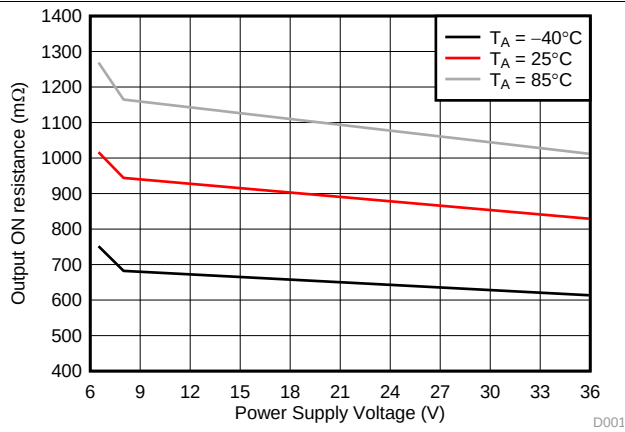


图 1. $r_{DS(on)}$ Over Voltage

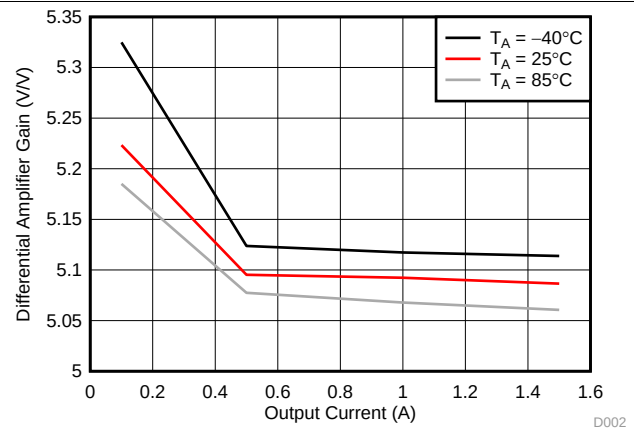


图 2. V_{PROPI} Over Output Current

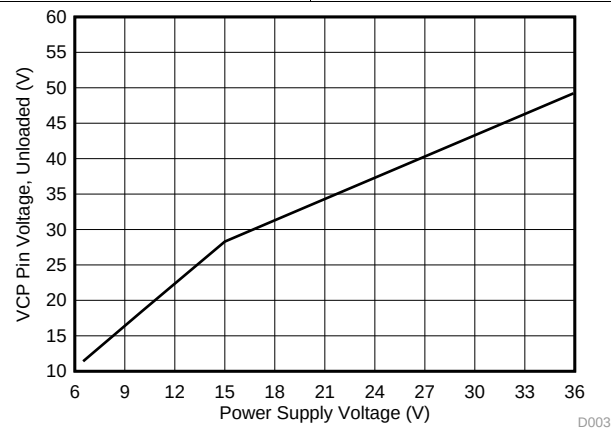


图 3. VCP Voltage vs V_{BB}

7 Detailed Description

7.1 Overview

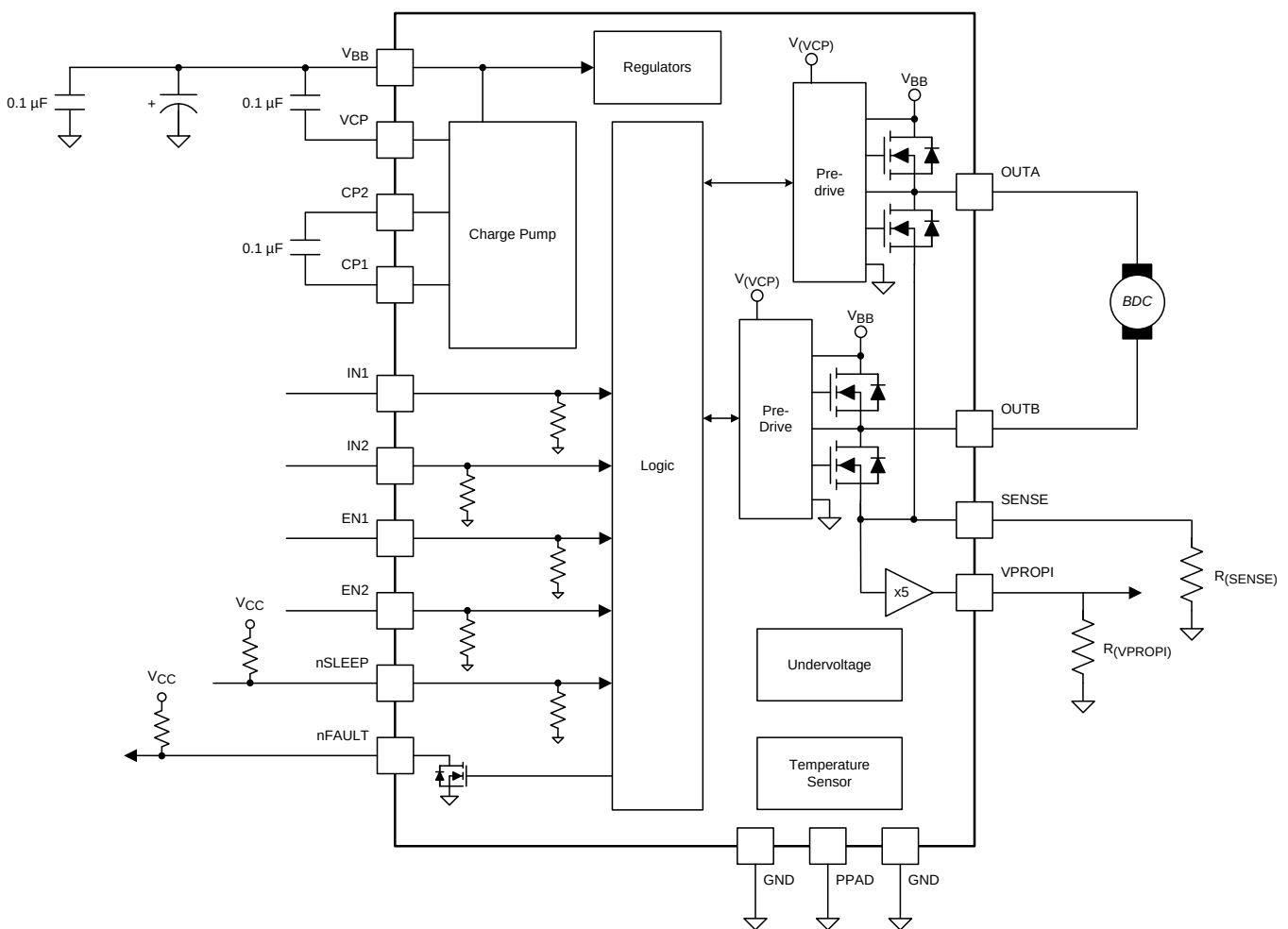
The DRV8801A-Q1 device is an integrated motor driver solutions for brushed-DC motors. The device integrates a DMOS H-bridge and current sense and protection circuitry. The device can be powered with a supply voltage between 6.5 V and 36 V, and is capable of providing an output current up to 2.8-A peak.

A simple PHASE and ENABLE interface allows control of the motor speed and direction.

A shunt amplifier output is provided for accurate current measurements by the system controller. The VPROPI pin outputs a voltage that is five-times the voltage seen at the SENSE pin.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supervisor

The control input, nSLEEP, is used to minimize power consumption when the DRV8801A-Q1 device is not in use. The nSLEEP input disables much of the internal circuitry, including the internal voltage rails and charge pump. nSLEEP is asserted logic low. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

7.3.2 Bridge Control

The following table shows the logic for the DRV8801A-Q1:

nSLEEP	PHASE	ENABLE	MODE1	MODE2	OUTA	OUTB	OPERATION
0	X	X	X	X	Z	Z	Sleep mode
1	0	1	X	X	L	H	Reverse
1	1	1	X	X	H	L	Forward
1	0	0	0	X	H	L	Fast decay
1	1	0	0	X	L	H	Fast decay
1	X	0	1	0	L	L	Low-side Slow decay
1	X	0	1	1	H	H	High-side Slow decay

To prevent reversal of current during fast-decay synchronous rectification, outputs go to the high impedance state as the current approaches 0 A.

The path of current flow for each of the states in the above logic table is shown in [图 4](#).

7.3.2.1 MODE 1

Input MODE 1 is used to toggle between fast-decay mode and slow-decay mode. A logic high puts the device in slow-decay mode.

7.3.2.2 MODE 2

MODE 2 is used to select which set of drivers (high side versus low side) is used during the slow-decay recirculation. MODE 2 is meaningful only when MODE 1 is asserted high. A logic high on MODE 2 has current recirculation through the high-side drivers. A logic low has current recirculation through the low-side drivers.

7.3.3 Fast Decay with Synchronous Rectification

This decay mode is equivalent to a phase change where the FETs opposite of the driving FETs are switched on (2 in [图 4](#)). When in fast decay, the motor current is not allowed to go negative because this would cause a change in direction. Instead, as the current approaches zero, the drivers turn off. See the [Power Dissipation](#) section for an equation to calculate power.

7.3.4 Slow Decay with Synchronous Rectification (Brake Mode)

In slow-decay mode, both low-side and high-side drivers turn on, allowing the current to circulate through the low-side and high-side body diodes of the H-bridge and the load (3 and 4 in [图 4](#)). See the [Power Dissipation](#) section for equations to calculate power for both high-side and low-side slow decay.

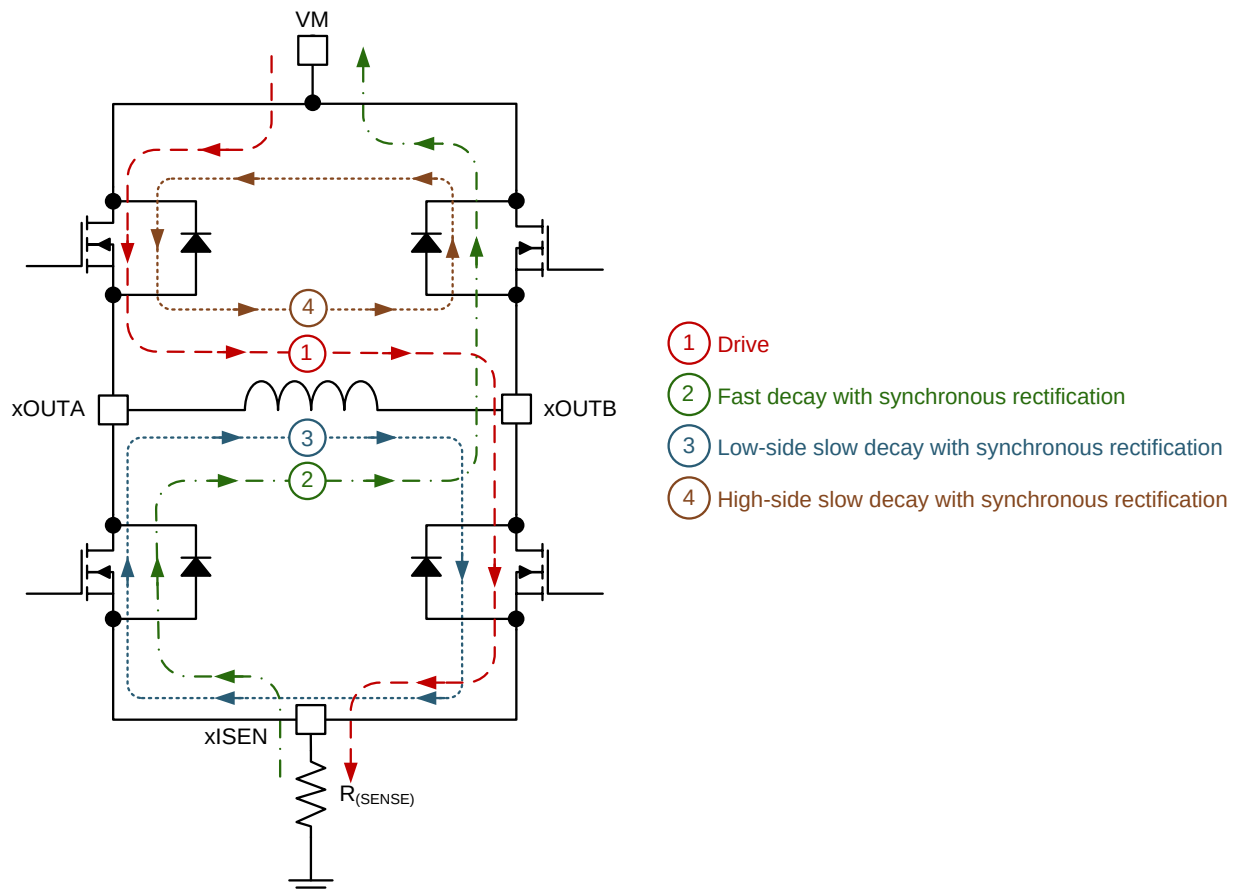


图 4. H-Bridge Operation Modes

7.3.5 Charge Pump

The charge pump is used to generate a supply above V_{BB} to drive the source-side DMOS gates. A 0.1- μF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1- μF ceramic monolithic capacitor should be connected between VCP and V_{BB} to act as a reservoir to run the high-side DMOS devices.

7.3.6 SENSE

A low-value resistor can be placed between the SENSE pin and ground for current-sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

To set a manual overcurrent trip threshold, place a resistor between the SENSE pin and GND. When the SENSE pin rises above 500 mV, the H-bridge output is disabled (hi-Z). The device automatically retries with a period of $t_{(OCP)}$.

The overcurrent trip threshold can be calculated using 公式 1.

$$I_{(trip)} = 500 \text{ mV/R} \quad (1)$$

The overcurrent trip level selected cannot be greater than $I_{(OCP)}$.

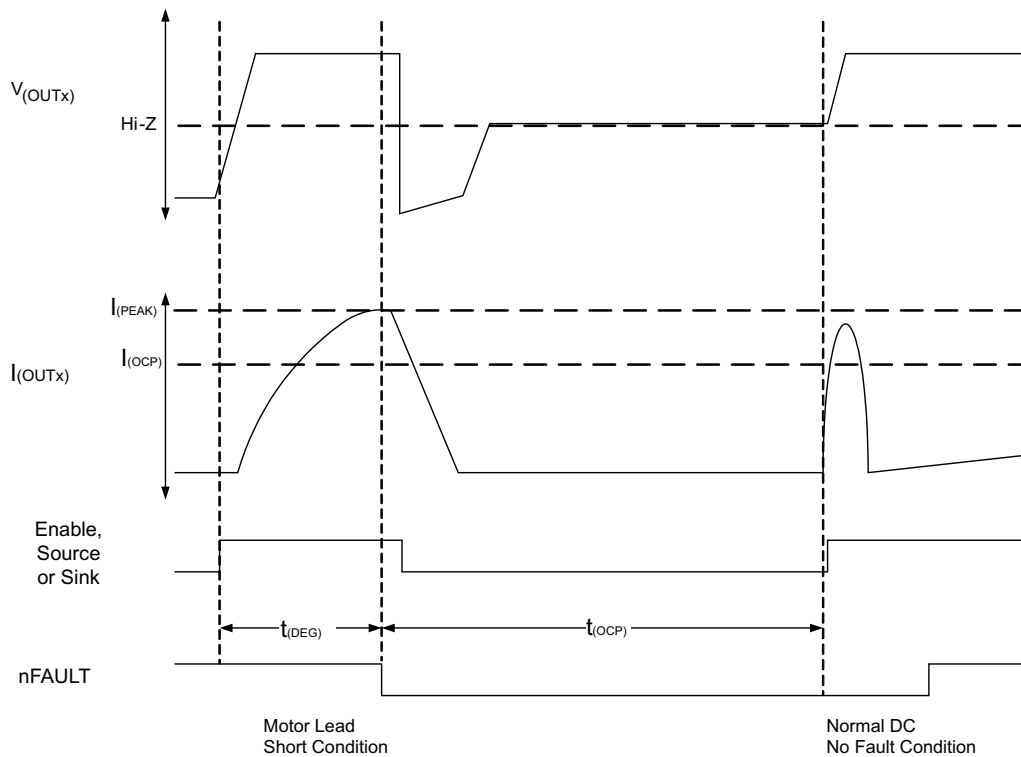


图 5. Overcurrent Control Timing

7.3.7 VPROPI

The VPROPI output is equal to approximately five times the voltage present on the SENSE pin. VPROPI is meaningful only if there is a resistor connected to the SENSE pin. If the SENSE pin is connected to ground, VPROPI measures 0 V. Also note that during slow decay (brake), VPROPI measures 0 V. VPROPI can output a maximum of 2.5 V, because at 500 mV on SENSE, the H-bridge is disabled.

7.3.8 Protection Circuits

The DRV8801A-Q1 device is fully protected against V_{BB} undervoltage, overcurrent, and overtemperature events.

7.3.8.1 V_{BB} Undervoltage Lockout (UVLO)

If at any time the voltage on the V_{BB} pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled and the charge pump is disabled. The nFAULT pin does not report the UVLO fault condition and remains hi-Z. Operation resumes when V_{BB} rises above the UVLO threshold.

7.3.8.2 Overcurrent Protection (OCP)

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, all FETs in the H-bridge are disabled, nFAULT is driven low, and a $t_{(OCP)}$ fault timer is started. After this period, $t_{(OCP)}$, the device is then allowed to follow the input commands and another turn-on is attempted (nFAULT releases during this attempt). If there is still a fault condition, the cycle repeats. If the short condition is not present after $t_{(OCP)}$ expires, normal operation resumes and nFAULT is released.

7.3.8.3 Overtemperature Warning (OTW)

If the die temperature increases past the thermal warning threshold the nFAULT pin is driven low. When the die temperature has fallen below the hysteresis level, the nFAULT pin is released. If the die temperature continues to increase, the device enters overtemperature shutdown as described in the [Overtemperature Shutdown \(OTS\)](#) section.

7.3.8.4 Overtemperature Shutdown (OTS)

If the die temperature exceeds the thermal shutdown temperature, all FETs in the H-bridge are disabled and the charge pump shuts down. The nFAULT pin remains pulled low during this fault condition. When the die temperature falls below the hysteresis threshold, operation automatically resumes.

FAULT	ERROR REPORT	H-BRIDGE	CHARGE PUMP	RECOVERY
V _{BB} undervoltage (UVLO)	No error report – nFAULT is hi-Z	Disabled	Shut Down	V _{BB} > VUVLO RISING
Overcurrent (OCP)	nFAULT pulled low	Disabled	Operating	Retry time, t _(OCP)
Overtemperature Warning (OTW)	nFAULT pulled low	Enabled	Operating	T _J < T _(OTW) – T _{hys(OTW)}
Overtemperature Shutdown (OTS)	nFAULT remains pulled low (set during OTW)	Disabled	Shut Down	T _J < T _(OTS) – T _{hys(OTS)}

7.4 Device Functional Modes

The DRV8801A-Q1 device is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled and the H-bridge FETs are disabled hi-Z. The DRV8801A-Q1 device is brought out of sleep mode automatically if nSLEEP is brought logic high.

8 Application and Implementation

8.1 Application Information

The DRV8801A-Q1 device is used in medium voltage brushed-DC motor control applications.

8.2 Typical Application

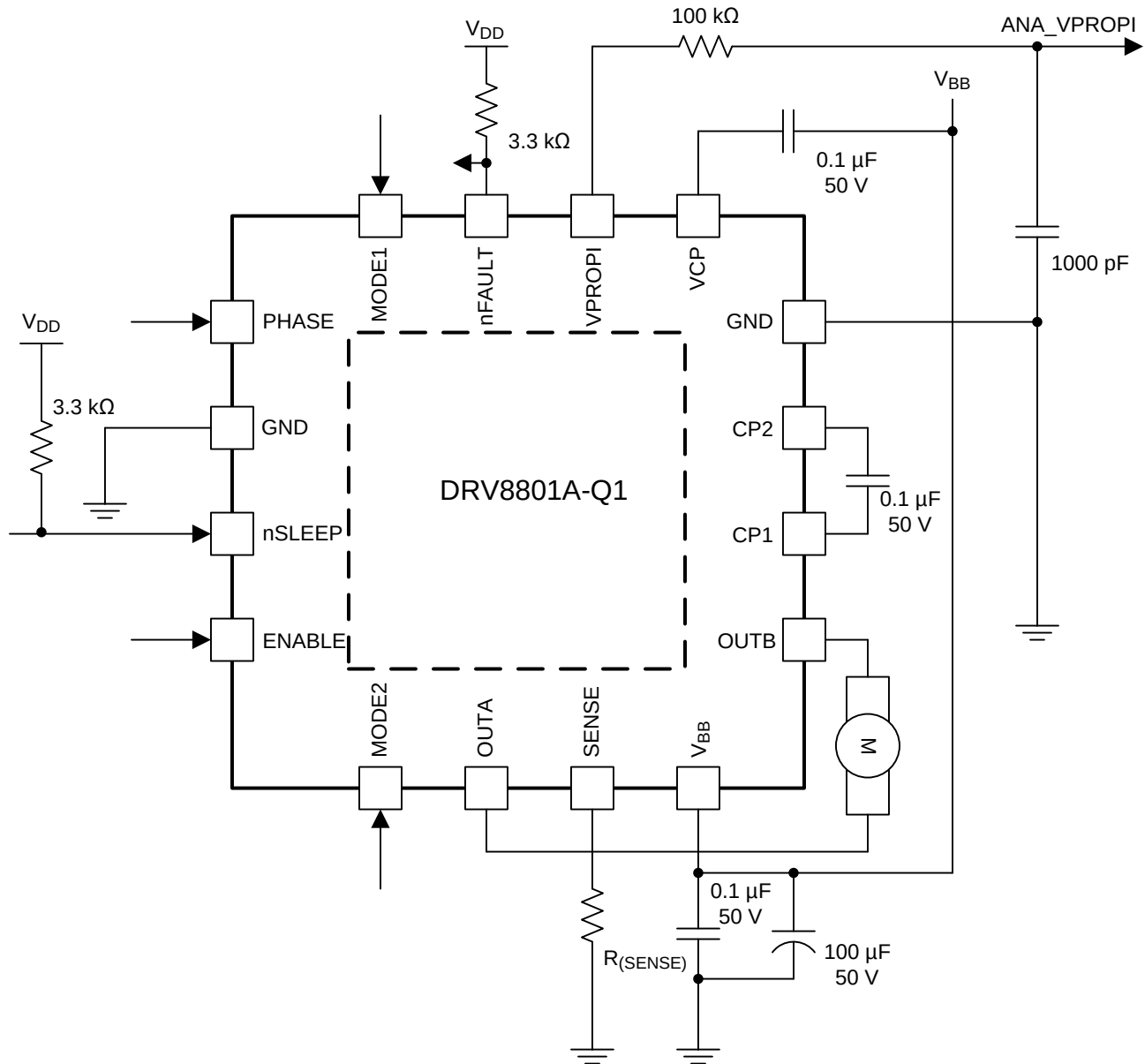


图 6. Typical Application Diagram

Typical Application (接下页)

8.2.1 Design Requirements

The example supply voltage for this design is $V_{BB} = 18\text{ V}$.

8.2.2 Detailed Design Procedure

8.2.2.1 Drive Current

This current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS driver. Power dissipation I^2R losses in one source and one sink DMOS driver, as shown in 公式 2.

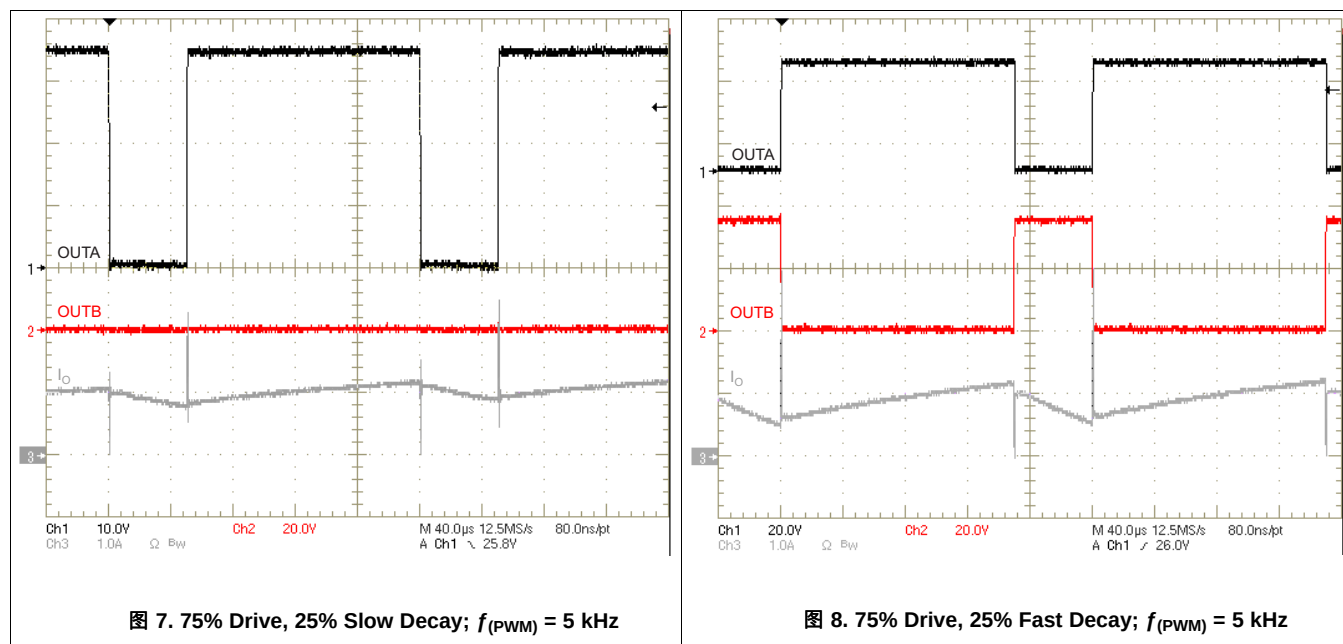
$$P_D = I^2(r_{DS(on)Source} + r_{DS(on)Sink}) \quad (2)$$

8.2.2.2 Slow-Decay SR (Brake Mode)

In slow-decay mode, both low-side sinking drivers turn on, allowing the current to circulate through the low side of the H-bridge (two sink drivers) and the load. Power dissipation I^2R losses in the two sink DMOS drivers as shown in 公式 3

$$P_D = I^2(2 \times r_{DS(on)Sink}) \quad (3)$$

8.2.3 Application Curves



9 Power Supply Recommendations

The DRV8801A-Q1 device is designed to operate from an input-voltage supply (V_{BB}) range between 6.5 V and 36 V. One 0.1- μ F ceramic capacitor rated for V_{BB} must be placed as close as possible to the V_{BB} pin. In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. This sizing is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value but system-level testing is required to determine the appropriate sized bulk capacitor.

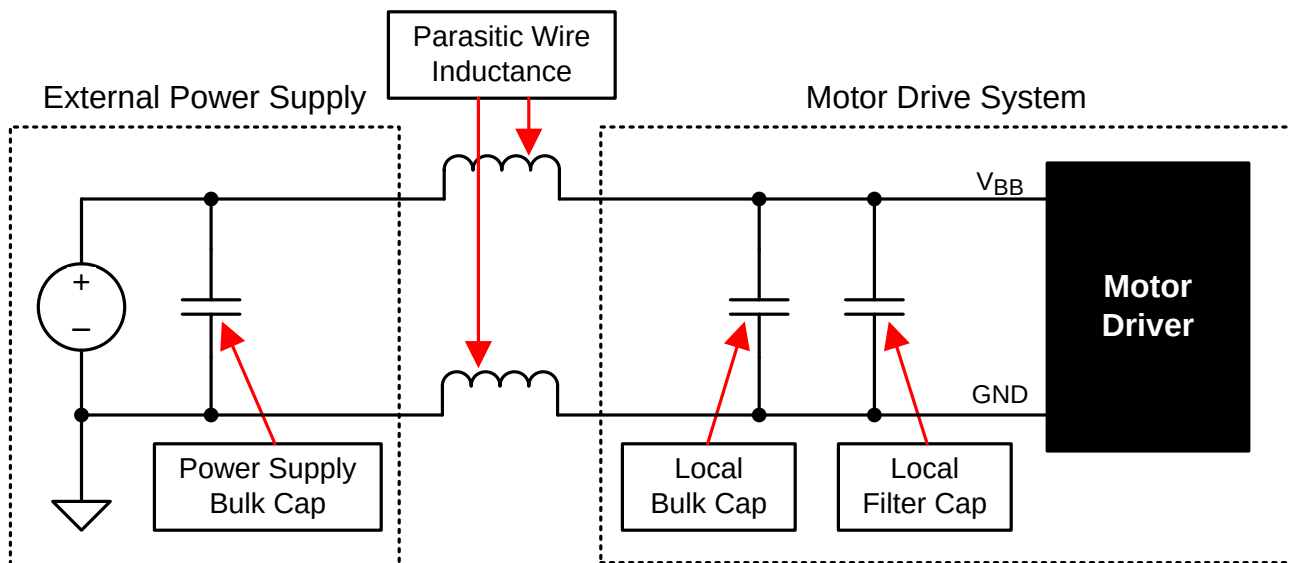


图 9. Bulk Capacitance

10 Layout

10.1 Layout Guidelines

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8801A-Q1 device must be soldered directly onto the board. On the bottom side of the DRV8801A-Q1 device is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB. For more information on this technique, see the application report, *PowerPAD™ Thermally Enhanced Package*, [SLMA002](#).

The load supply pin, V_{BB} , should be decoupled with an electrolytic capacitor (typically 100 μF) in parallel with a ceramic capacitor placed as close as possible to the device. In order to minimize lead inductance, the ceramic capacitors between the VCP and V_{BB} pins, connected to the REG pin, and the capacitors between the CP1 and CP2 pins should be as close to the pins of the device as possible.

10.2 Layout Example

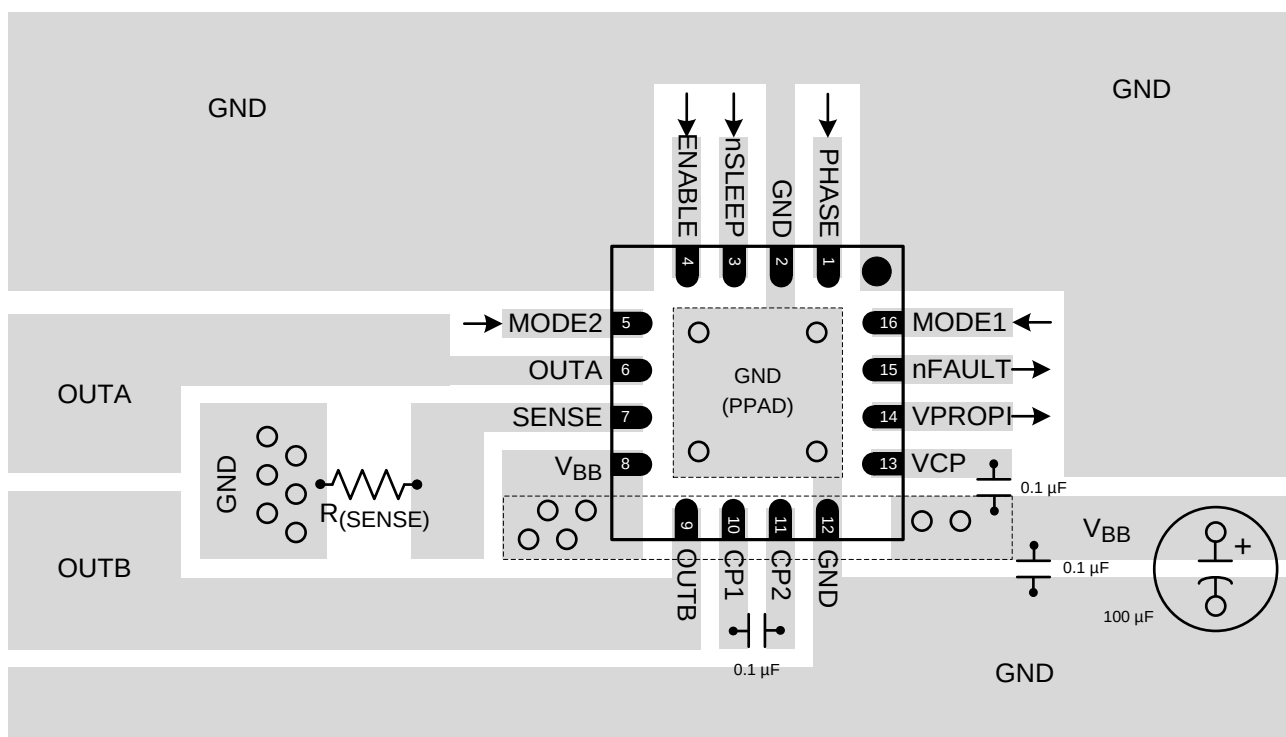


图 10. DRV8801A-Q1 Layout

10.3 Power Dissipation

First-order approximation of power dissipation in the DRV8801A-Q1 device can be calculated by examining the power dissipation in the full-bridge during each of the operation modes. The DRV8801A-Q1 device uses synchronous rectification. During the decay cycle, the body diode is shorted by the low- $r_{DS(on)}$ driver, which in turn reduces power dissipation in the full-bridge. In order to prevent shoot through (high-side and low-side drivers on the same side are ON at the same time), the DRV8801A-Q1 device implements a 500-ns typical crossover delay time. During this period, the body diode in the decay current path conducts the current until the DMOS driver turns on. High-current and high-ambient-temperature applications should take this into consideration. In addition, motor parameters and switching losses can add power dissipation that could affect critical applications.

11 器件和文档支持

11.1 商标

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用的 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2014, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8801AQRMJRQ1	ACTIVE	WQFN	RMJ	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8801 ARMJQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

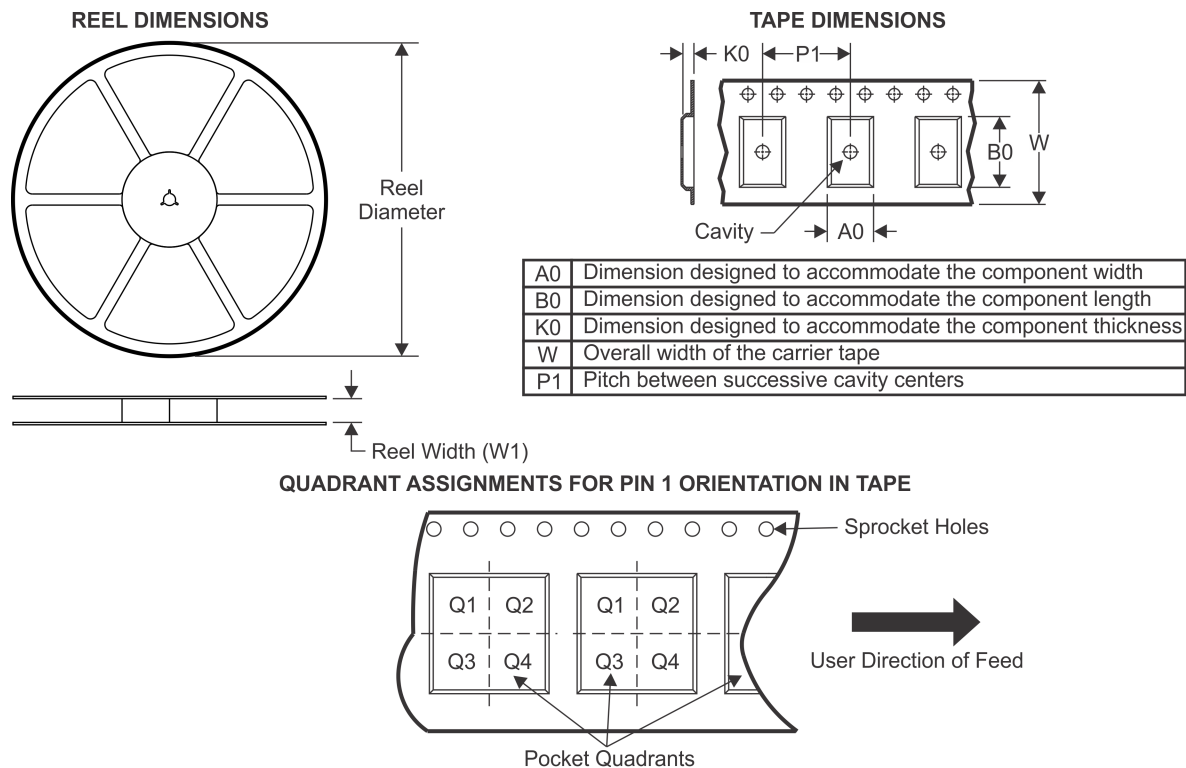
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

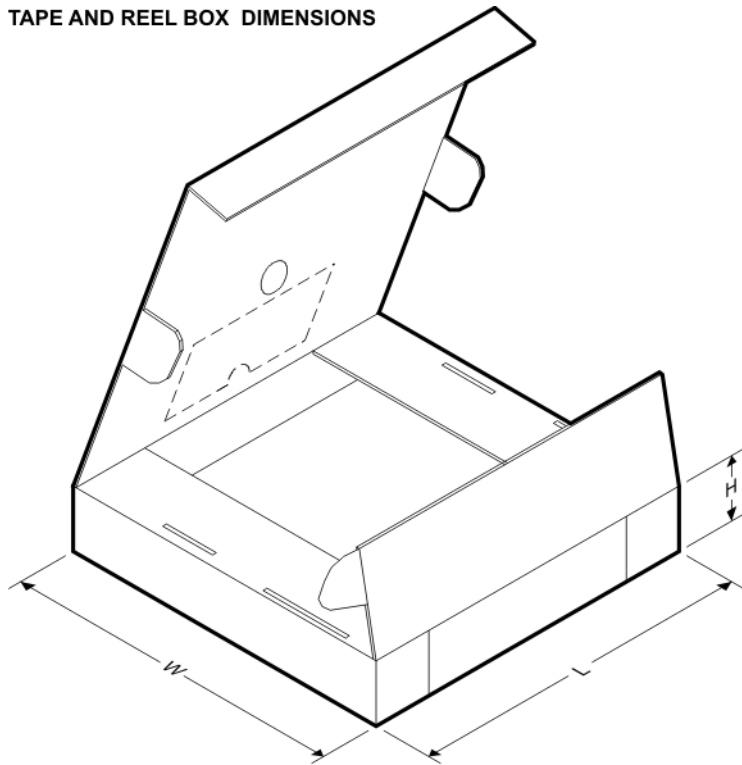
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8801AQRMJRQ1	WQFN	RMJ	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

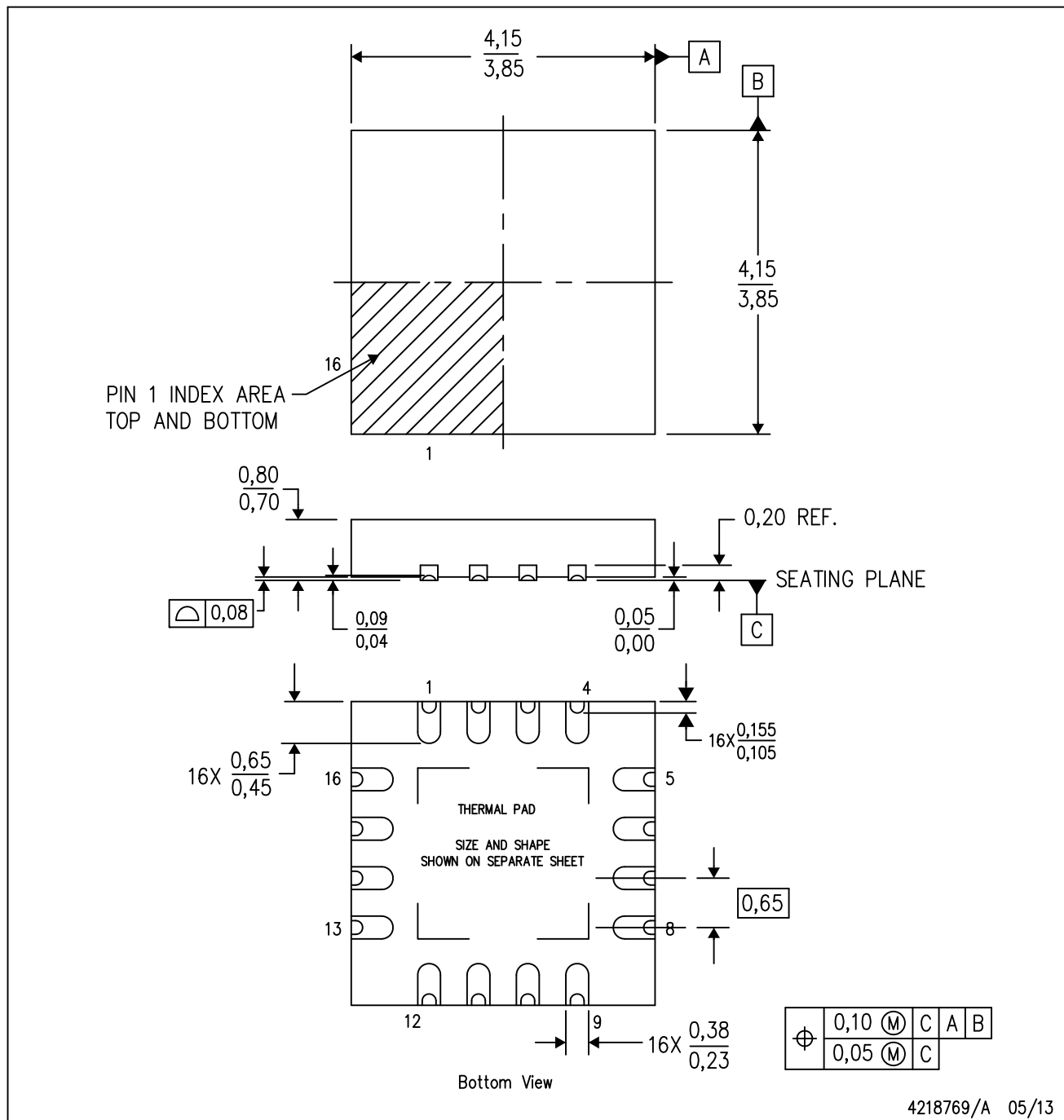


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8801AQRMJRQ1	WQFN	RMJ	16	3000	367.0	367.0	35.0

RMJ (S-PWQFN-N16)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

RMJ (S-PWQFN-N16)

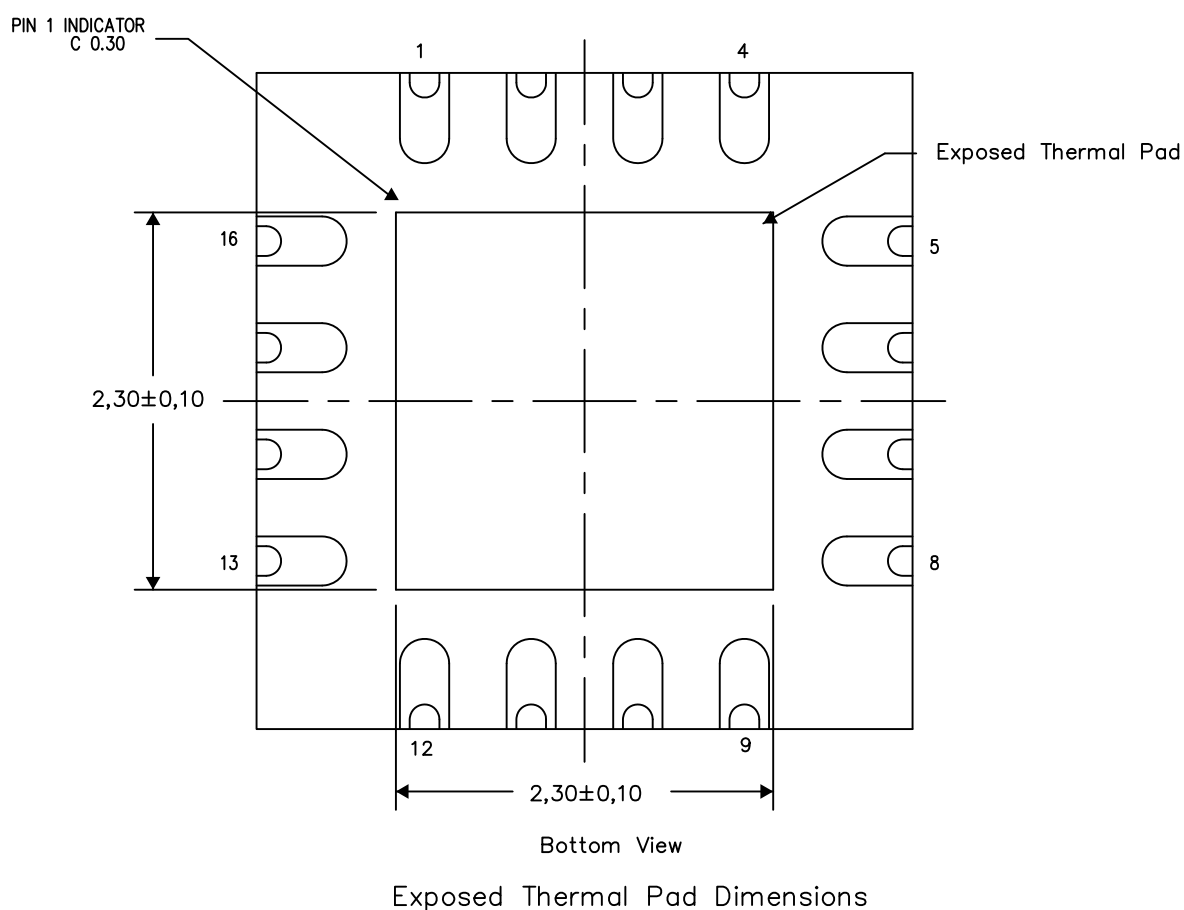
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4219300/A 07/13

NOTE: All linear dimensions are in millimeters

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司