

DUAL CHANNEL POWER DRIVER

FEATURES

- Two Independent Drivers
- 1.5 A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40 ns Rise and Fall Into 1000 pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown With Optional Latch
- Low Quiescent Current
- 5 V to 40 V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin PLCC and CLCC Package

DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices—particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5 A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both V_{IN} and V_C can independently range from 5 V to 40 V.

These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for –55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

TRUTH TABLE
(Each Channel)⁽¹⁾

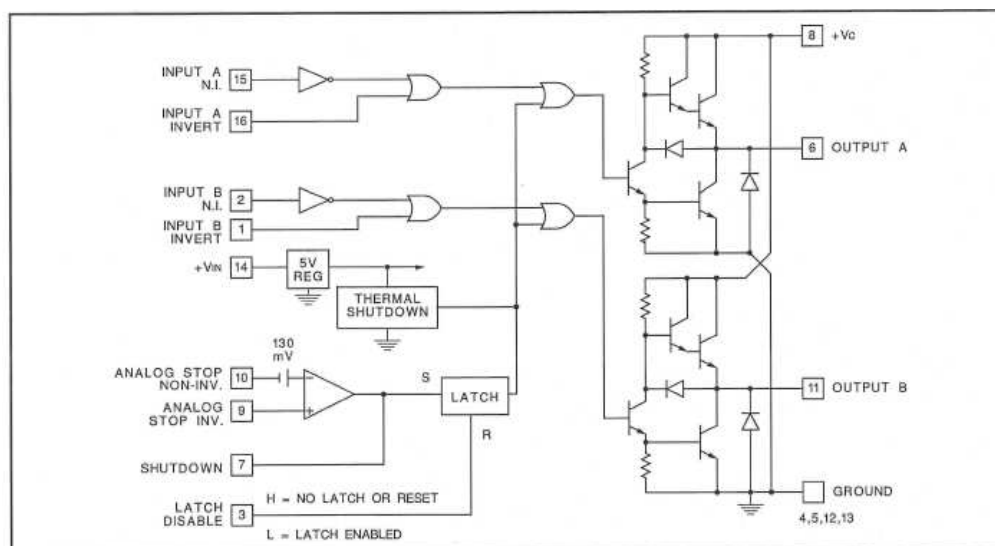
INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

(1) $\overline{OUT} = \overline{INV}$ and N.I.
 $\overline{OUT} = INV$ or N.I.

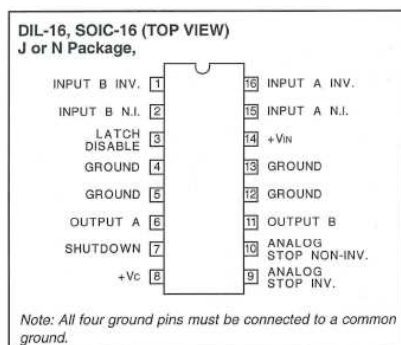
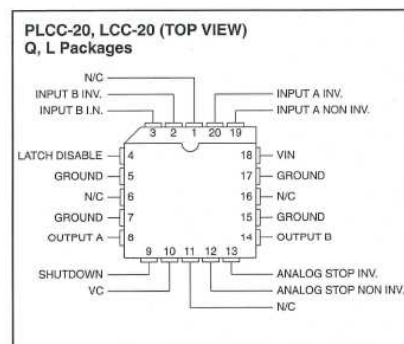


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BLOCK DIAGRAM



CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply voltage	N/J package		40	V
V_C	Collector supply voltage	N/J package		40	V
	Output current (each output, source or sink) steady-state	N/J package		±500	mA
	Peak transient	N package		±1.5	A
		J package		±1.0	
	Capacitive discharge energy	N package		20	mJ
		J package		15	
	Digital inputs ⁽¹⁾	N/J-package		5.5	V
	Analog stop inputs	N/J package		V_{IN}	
	Power dissipation at $T_A = 25^\circ\text{C}$	N package		2	W
		J package		1	
	Power dissipation at T (leads/case) = 25°C ⁽¹⁾	N package		5	W
		J package		2	
	Operating temperature range		–55	+125	$^\circ\text{C}$
	Storage temperature range		–65	+150	$^\circ\text{C}$
	Lead temperature (soldering, 10 seconds)			300	$^\circ\text{C}$

- (1) All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Digital drive can exceed 5.5 V if input current is limited to 10 mA. Consult packaging section of databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1707, -25°C to $+85^\circ\text{C}$ for the UC2707, and 0°C to $+70^\circ\text{C}$ for the UC3707; $V_{IN} = V_C = 20\text{ V}$. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} Supply current	$V_{IN} = 40\text{ V}$		12	15	mA
V_C Supply current	$V_C = 40\text{ V}$, outputs low		5.2	7.5	mA
V_C Leakage current	$V_{IN} = 0$, $V_C = 30\text{ V}$, no load		0.05	0.1	mA
Digital input low level				0.8	V
Digital input high level		2.2			V
Input current	$V_I = 0$		–0.06	–1.0	mA
Input leakage	$V_I = 5\text{ V}$		0.05	0.1	mA
$V_C - V_O$ Output high sat.	$I_O = -50\text{ mA}$			2.0	V
	$I_O = -500\text{ mA}$			2.5	
V_O Output low sat.	$I_O = -50\text{ mA}$			0.4	V
	$I_O = -500\text{ mA}$			2.5	
Analog threshold	$V_{CM} = 0$ to 15 V	100	130	160	mV
Input bias current	$V_{CM} = 0$		–10	–20	μA
Thermal shutdown			155		$^\circ\text{C}$
Shutdown threshold	Pin 7 input	0.4	1.0	2.2	V
Latch disable threshold	Pin 3 input	0.8	1.2	2.2	V

TYPICAL SWITCHING CHARACTERISTICS

$V_{IN} = V_C = 20\text{ V}$, $T_A = 25^\circ\text{C}$. Delays measured to 10% output change.

PARAMETER	TEST CONDITIONS	OUTPUT CL =			UNIT
From Inv. Input to Output		open	1.0	2.2	nF
Rise time delay		40	50	60	ns
10% to 90% rise		25	40	50	ns
Fall time delay		30	40	50	ns
90% to 10% fall		25	40	50	ns
From N.I. Input to Output					
Rise time delay		30	40	50	ns
10% to 90% rise		25	40	50	ns
Fall time delay		45	55	65	ns
90% to 10% fall		25	40	50	ns
V_C cross-conduction current spike duration	Output rise	25			ns
	Output fall	0			ns
Analog shutdown delay	Stop non-Inv. = 0 V	180			ns
	Stop Inv. = 0 to 0.5 V	180			ns
Digital shutdown delay	2 V input on Pin 7	50			ns

SIMPLIFIED INTERNAL CIRCUITRY

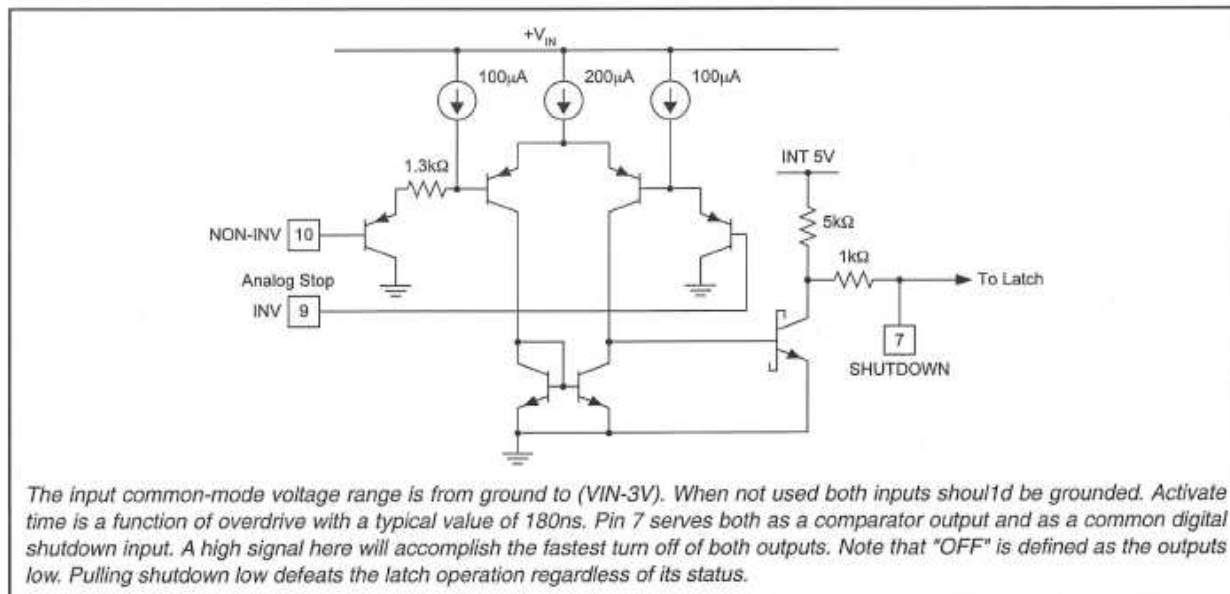


Figure 1. Typical Digital Input Gate

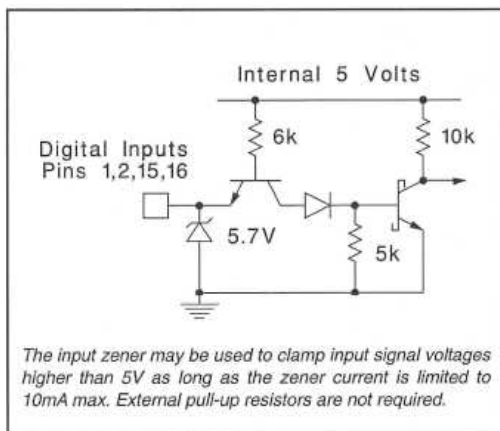


Figure 2. Typical Digital Input Gate

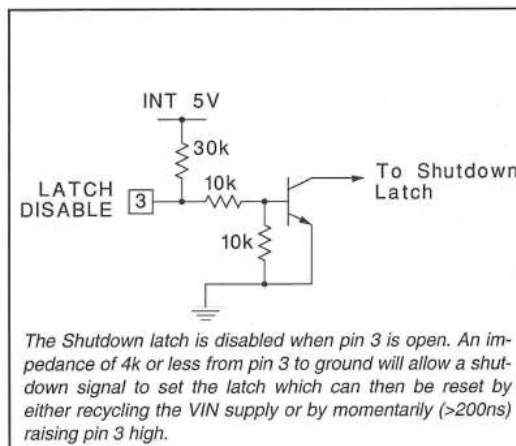
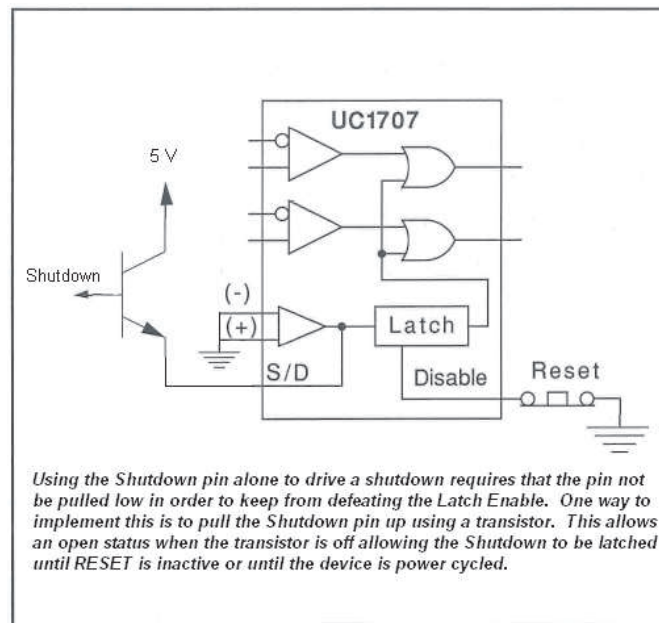


Figure 3. Latch Disable

SIMPLIFIED INTERNAL CIRCUITRY (continued)**Figure 4. Use of the Shutdown Pin****SHUTDOWN CIRCUIT DESCRIPTION**

The function of the circuitry is to be able to provide a shutdown of the device. This is defined as functionality that will drive both outputs to the low state. There are three different inputs that govern this shutdown capability.

- **Analog Stop Pins** — The differential inputs to this comparator provide a way to execute a shutdown.
- **Latch Disable Pin** — Assuming that the Shutdown pin is left open, a high on this pin disables the latching functionality of the Analog Stop shutdown. A low on this pin enables the latching functionality of the Analog Stop shutdown. If a shutdown occurs through the Analog Stop circuit while Latch Disable is high, then the outputs will go low, but will return to normal operation as soon as the Analog Stop circuit allows it. If a shutdown occurs through the Analog Stop circuit while Latch Disable is low, then the outputs will go low and remain low even if the Analog Stop circuit no longer drives the shutdown. The outputs will remain "latched" low (in shutdown) until the Latch Disable goes high and the Analog Stop circuit allows it to return from shutdown or the VIN voltage is cycled to 0V and then returned above 5V.
- **Shutdown Pin** — This pin serves two purposes.
 1. It can be used as an output of the Analog Stop circuit.
 2. It can be used as an input to force a shutdown or to force the device out of shutdown. This pin can override both the Analog Stop circuit as well as the Latch Disable Pin. When driving hard logic levels into the Shutdown pin, the Latch Disable functionality will be overridden and the Latch Disable will not function as it does when used in conjunction with the Analog Stop circuit. When the Shutdown pin is high, the outputs will be in the low state (shutdown). When the Shutdown pin is low (hard logic low) the outputs will operate normally, regardless of the state of the Latch Disable pin or the Analog Stop pins.

In order to use the Shutdown Pin with the Latch Disable functional it is necessary to use either a diode in series with the Shutdown signal or to use an open collector pull-up so that the Shutdown pin is not pulled low. This configuration will allow the Latch Disable function to work with the Shutdown pin.

SIMPLIFIED INTERNAL CIRCUITRY (continued)

UG1707 SHUTDOWN TRUTH TABLE

ANALOG STOP LOGIC	SHUTDOWN	LATCH DISABLE	PREVIOUS STATE OF OUTPUT	OUTPUT
X	0	X	X	Follows Input Logic
X	1	X	X	Low (Shutdown)
1	Open	X	X	Low (Shutdown)
0	Open	0	Shutdown	⁽¹⁾ Latched Shutdown
0	Open	0	Normal	Follows Input Logic
0	Open	1	X	Follows Input Logic

- (1) If the output was previously in Shutdown and Latch Disable was low and stays low, then even if the Analog Stop Logic is changed or the Shutdown pin is open, the outputs will remain in Shutdown.

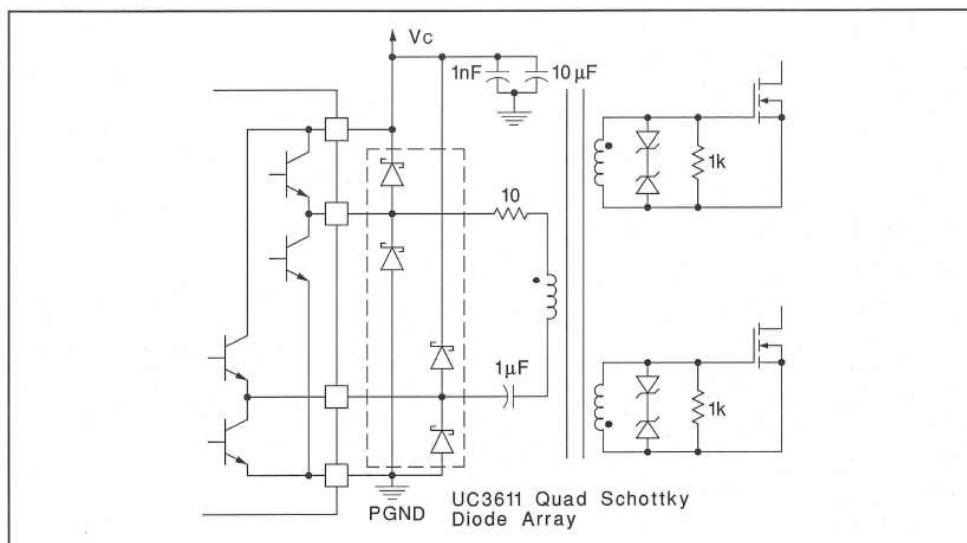


Figure 5. Transformer Coupled Push-Pull MOSFET Drive Circuit

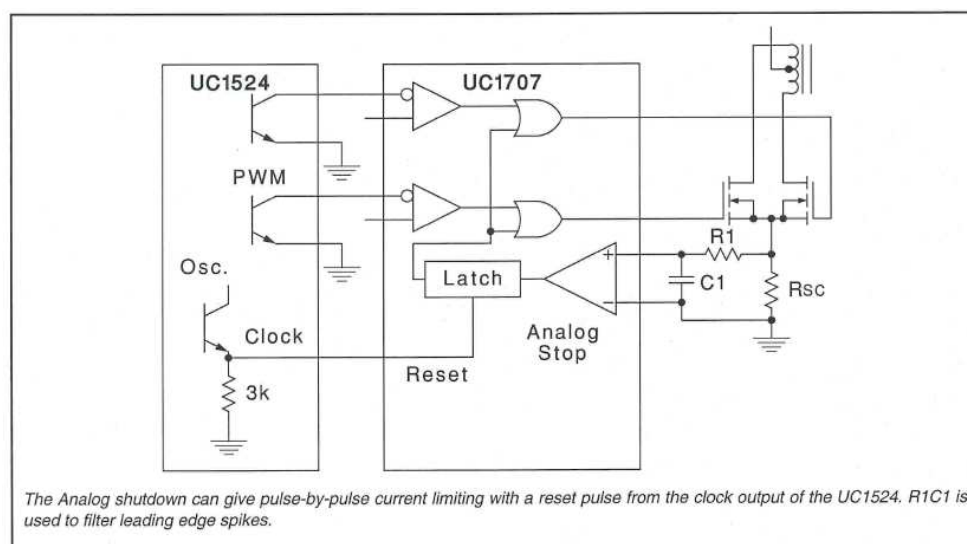


Figure 6. Current Limiting

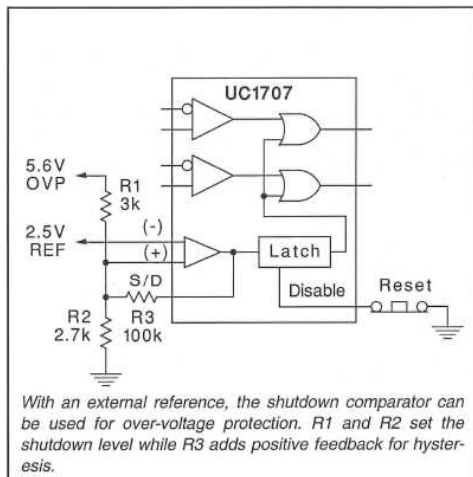


Figure 7. Over-Voltage Protection

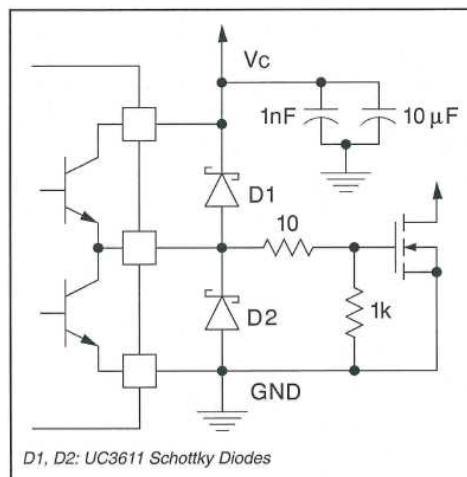


Figure 8. Power MOSFET Drive Circuit

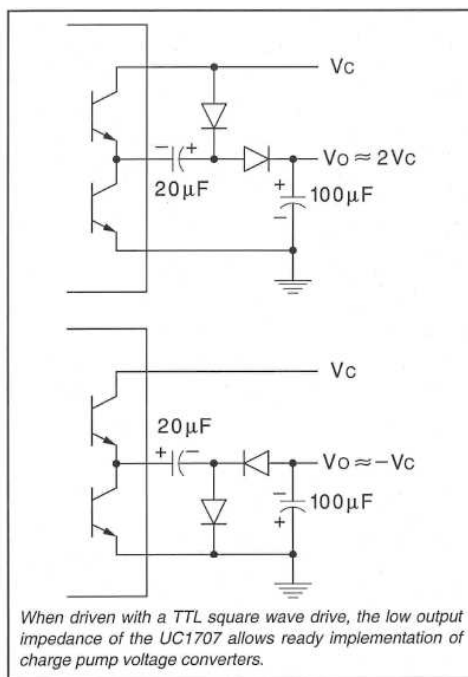


Figure 9. Charge Pump Circuits

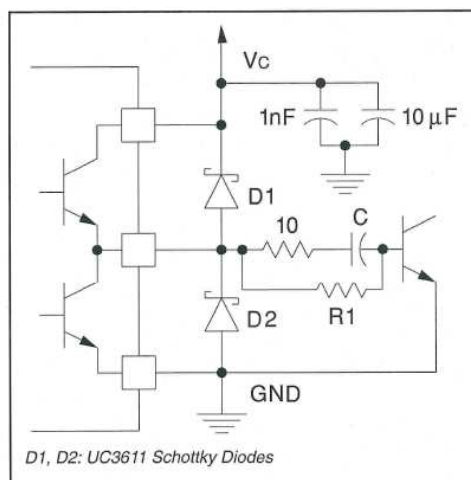


Figure 10. Power Bipolar Drive Circuit

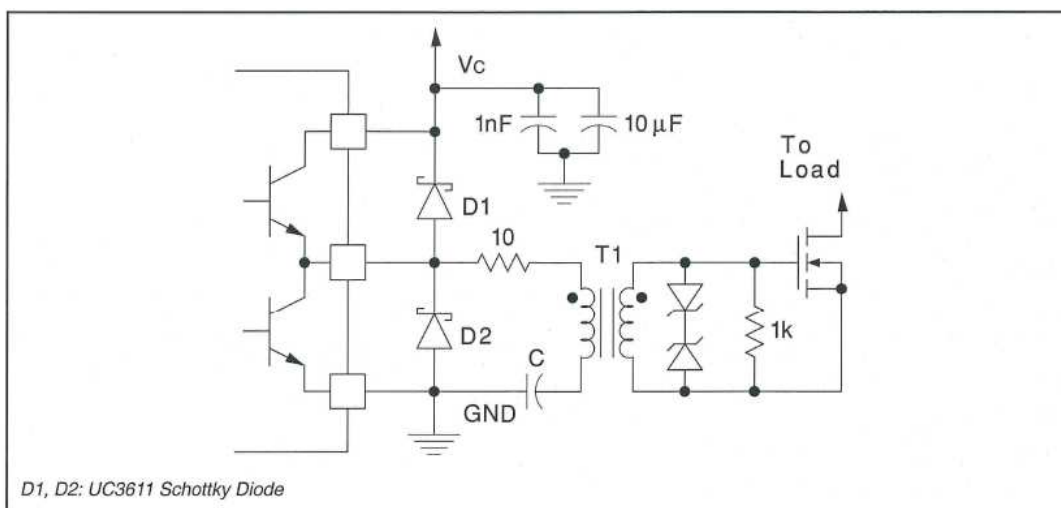


Figure 11. Transformer Coupled MOSFET Drive Circuit

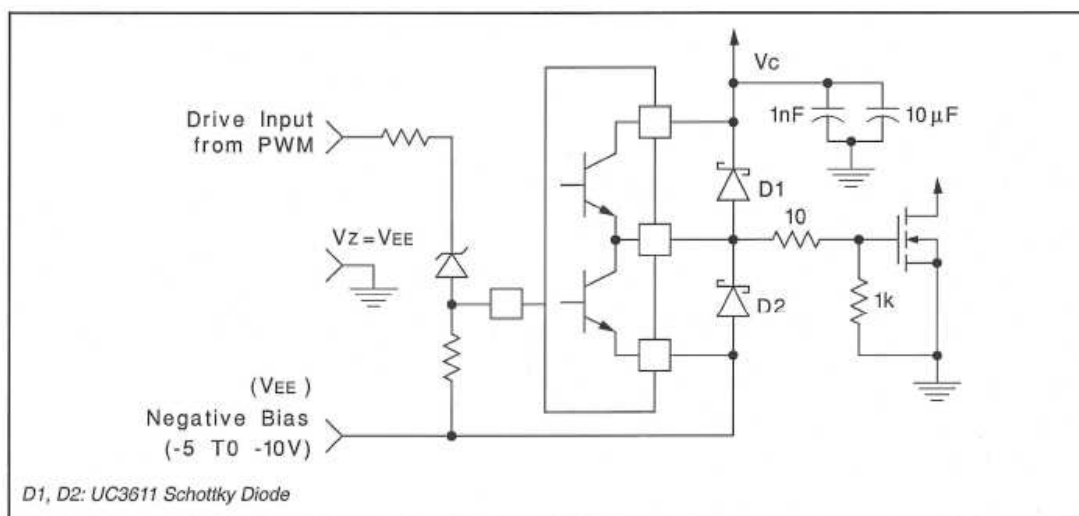


Figure 12. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Reference PWM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87619012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87619012A UC1707L/ 81032	Samples
5962-8761901EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761901EA UC1707J/80900	Samples
5962-8761901V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8761901V2A UC1707L QMLV	Samples
5962-8761901VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761901VE A UC1707JQMLV	Samples
5962-8761903V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 8761903V2A UC1707L-SP	Samples
5962-8761903VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761903VE A UC1707J-SP	Samples
5962-8761903VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761903VF A UC1707W-SP	Samples
UC1707J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1707J	Samples
UC1707J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1707J/883B	Samples
UC1707L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1707L	Samples
UC1707L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	UC1707L/ 883B	Samples
UC2707DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2707DW	Samples
UC2707DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2707DW	Samples
UC2707N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	N / A for Pkg Type	-40 to 85	UC2707N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2707NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-40 to 85	UC2707N	Samples
UC3707DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3707DW	Samples
UC3707DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3707DW	Samples
UC3707J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	0 to 70	UC3707J	Samples
UC3707N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	N / A for Pkg Type	0 to 70	UC3707N	Samples
UC3707NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	0 to 70	UC3707N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

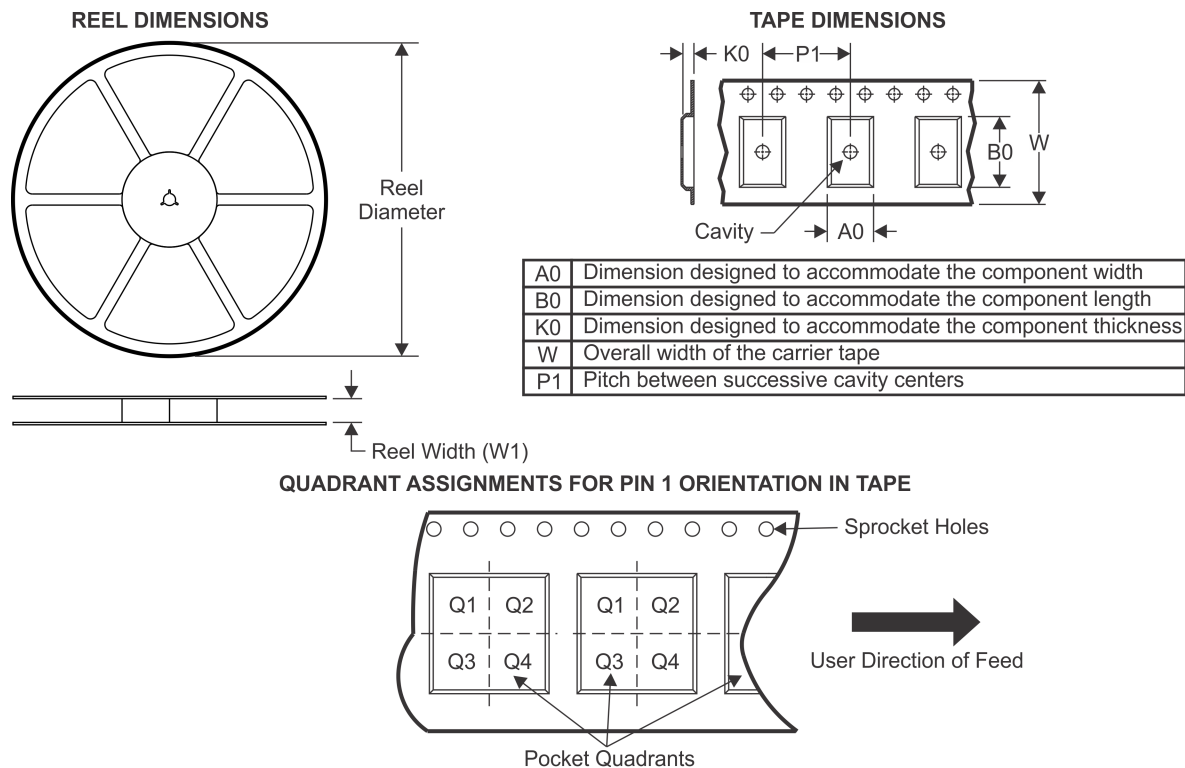
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1707, UC1707-SP, UC3707, UC3707M :

- Catalog: [UC3707](#), [UC1707](#), [UC3707M](#), [UC3707](#)
- Military: [UC1707](#)
- Space: [UC1707-SP](#)

NOTE: Qualified Version Definitions:

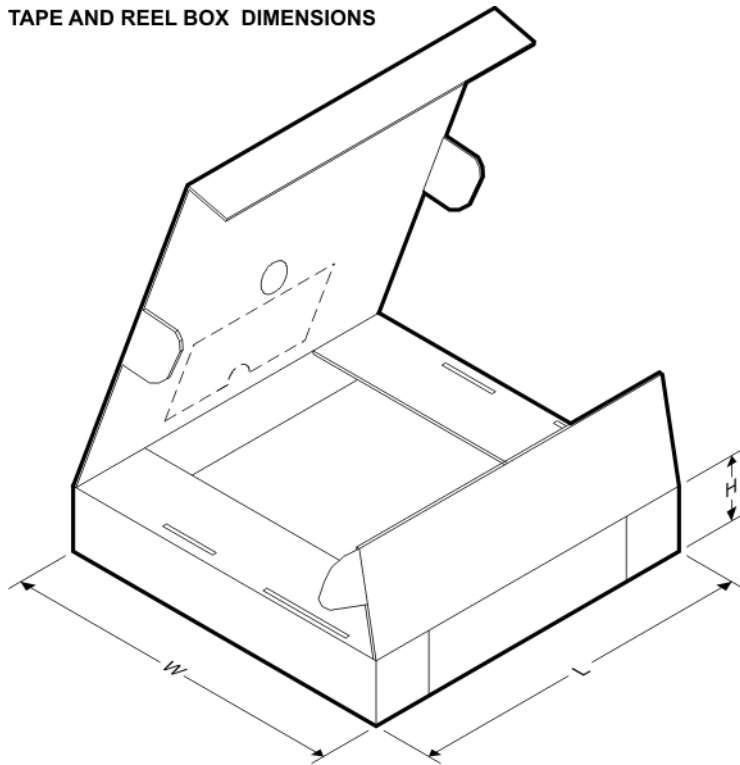
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2707DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3707DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2707DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3707DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.