# DRV8874-Q1 H-Bridge Motor Driver With Integrated Current Sense and Regulation

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
- N-channel H-bridge motor driver
  - Drives one bidirectional brushed DC motor
  - Two unidirectional brushed DC motors
  - Other resistive and inductive loads
- 4.5-V to 37-V operating supply voltage range
- Pin to pin $R_{DS(on)}$ variants
  - DRV8874-Q1: 200-mΩ (High-Side + Low-Side)
  - DRV8876-Q1: 700-mΩ (High-Side + Low-Side)
- High output current capability
  - DRV8874-Q1: 6-A Peak
  - DRV8876-Q1: 3.5-A Peak
- Integrated current sensing and regulation
- Proportional current output (IPROPI)
- Selectable current regulation (IMODE)
  - Cycle-by-cycle or fixed off time
- Selectable input control modes (PMODE)
  - PH/EN and PWM H-bridge control modes
  - Independent half-bridge control mode
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Ultra low-power sleep mode
  - <1-µA @ $V_{VM}$ = 24-V, $T_J$ = 25°C
- Spread spectrum clocking for low electromagnetic interference (EMI)
- Integrated protection features
  - Undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
  - Automatic fault recovery
  - Fault indicator pin (nFAULT)

## 2 Applications

- Brushed DC motors
- Servo motors and actuators
- HVAC damper
- Siren and piezo
- Mirror tilt and fold
- E-shifter adjust and lock

## 3 Description

The DRV887x-Q1 family of devices are flexible motor drivers for a wide variety of end applications. The devices integrate an N-channel H-bridge, charge pump regulator, current sensing and regulation, current proportional output, and protection circuitry. The charge pump improves efficiency by allowing for both high-side and low-side N-channels MOSFETs and 100% duty cycle support. The family of devices come in pin to pin, scalable $R_{DS(on)}$ options to support different loads with minimal design changes.

Integrated current sensing allows for the driver to regulate the motor current during start up and high load events. A current limit can be set with an adjustable external voltage reference. Additionally, the devices provide an output current proportional to the motor load current. This can be used to detect motor stall or change in load conditions. The integrated current sensing uses an internal current mirror architecture, removing the need for a large power shunt resistor, saving board area and reducing system cost.

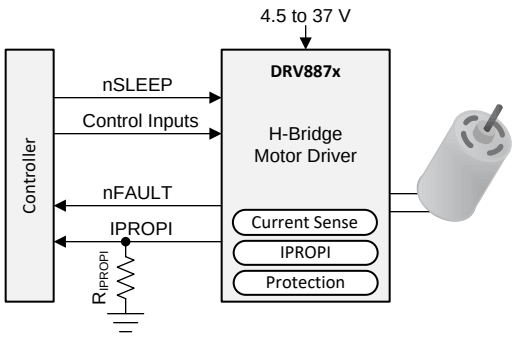
A low-power sleep mode is provided to achieve ultra-low quiescent current draw by shutting down most of the internal circuitry. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output overcurrent (OCP), and device overtemperature (TSD). Fault conditions are indicated on nFAULT.

**Device Information** (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV8874-Q1 | HTSSOP (16) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**




ADVANCE INFORMATION

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

# Table of Contents

**1 Features** ..... 1
**2 Applications** ..... 1
**3 Description** ..... 1
**4 Revision History** ..... 2
**5 Pin Configuration and Functions** ..... 3
**6 Specifications** ..... 4
6.1 Absolute Maximum Ratings ..... 4
6.2 ESD Ratings Auto ..... 4
6.3 Recommended Operating Conditions ..... 4
6.4 Thermal Information ..... 5
6.5 Electrical Characteristics ..... 5
**7 Detailed Description** ..... 8
7.1 Overview ..... 8
7.2 Functional Block Diagram ..... 8
7.3 Feature Description ..... 9
7.4 Device Functional Modes ..... 16
**8 Application and Implementation** ..... 18
8.1 Application Information ..... 18
8.2 Typical Application ..... 18
**9 Power Supply Recommendations** ..... 24
9.1 Bulk Capacitance ..... 24
**10 Layout** ..... 25
10.1 Layout Guidelines ..... 25
10.2 Layout Example ..... 25
**11 Device and Documentation Support** ..... 26
11.1 Documentation Support ..... 26
11.2 Receiving Notification of Documentation Updates 26
11.3 Community Resources ..... 26
11.4 Trademarks ..... 26
11.5 Electrostatic Discharge Caution ..... 26
11.6 Glossary ..... 26
**12 Mechanical, Packaging, and Orderable Information** ..... 27

ADVANCE INFORMATION

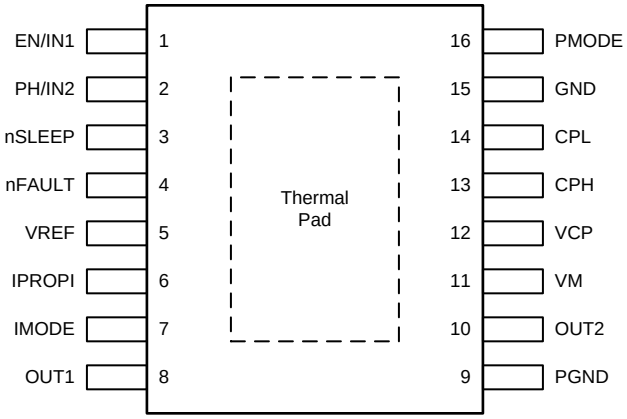
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| May 2019 | * | Initial release. |


Copyright © 2019, Texas Instruments Incorporated

# 5 Pin Configuration and Functions

**DRV8874-Q1 PWP Package**
**16-Pin HTSSOP With Exposed Thermal Pad**
**Top View**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | PWP | | |
| CPH | 13 | PWR | Charge pump switching node. Connect a X5R or X7R, 22-nF, VM-rated ceramic capacitor between the CPH and CPL pins. |
| CPL | 14 | PWR | |
| EN/IN1 | 1 | I | H-bridge control input. See Control Modes. Internal pulldown resistor. |
| GND | 15 | PWR | Device ground. Connect to system ground. |
| IMODE | 7 | I | Current regulation and overcurrent protection mode. See Current Regulation. Quad-level input. |
| IPROPI | 6 | O | Analog current output proportional to load current. See Current Sensing. |
| nFAULT | 4 | OD | Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation. See Protection Circuits. |
| nSLEEP | 3 | I | Sleep mode input. Logic high to enable device. Logic low to enter low-power sleep mode. See Device Functional Modes. Internal pulldown resistor. |
| OUT1 | 8 | O | H-bridge output. Connect to the motor or other load. |
| OUT2 | 10 | O | H-bridge output. Connect to the motor or other load. |
| PGND | 9 | PWR | Device power ground. Connect to system ground. |
| PH/IN2 | 2 | I | H-bridge control input. See Control Modes. Internal pulldown resistor. |
| PMODE | 16 | I | H-bridge control input mode. See Control Modes. Tri-level input. |
| VCP | 12 | PWR | Charge pump output. Connect a X5R or X7R, 100-nF, 16-V ceramic capacitor between the VCP and VM pins. |
| VM | 11 | PWR | 4.5-V to 37-V power supply input. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient Bulk Capacitance rated for VM. |
| VREF | 5 | I | External reference voltage input to set internal current regulation limit. See Current Regulation. |
| PAD | — | — | Thermal pad. Connect to system ground. |

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power supply pin voltage | VM | –0.3 | 40 | V |
| Voltage difference between ground pins | GND, PGND | –0.3 | 0.3 | V |
| Charge pump pin voltage | CPH, VCP | $V_{VM}$ – 0.3 | $V_{VM}$ + 7 | V |
| Charge pump low-side pin voltage | CPL | –0.3 | $V_{VM}$ + 0.3 | V |
| Logic pin voltage | EN/IN1, IMODE, nSLEEP, PH/IN2, PMODE | –0.3 | 5.75 | V |
| Open-drain output pin voltage | nFAULT | –0.3 | 5.75 | V |
| Output pin voltage | OUT1, OUT2 | –0.9 | $V_{VM}$ + 0.9 | V |
| Output pin current | OUT1, OUT2 | Internally Limited | Internally Limited | A |
| Proportional current output pin voltage | IPROPI | –0.3 | 5.75 | V |
| | | –0.3 | $V_{VM}$ + 0.3 | V |
| Reference input pin voltage | VREF | –0.3 | 5.75 | V |
| Ambient temperature, $T_A$ | | –40 | 125 | °C |
| Junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings Auto

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VM}$ | Power supply voltage | VM | 4.5 | | 37 | V |
| $V_{IN}$ | Logic input voltage | EN/IN1, MODE, nSLEEP, PH/IN2 | 0 | | 5.5 | V |
| $f_{PWM}$ | PWM frequency | EN/IN1, PH/IN2 | 0 | | 100 | kHz |
| $V_{OD}$ | Open drain pullup voltage | nFAULT | 0 | | 5.5 | V |
| $I_{OD}$ | Open drain output current | nFAULT | 0 | | 5 | mA |
| $I_{OUT}$(1) | Peak output current | OUT1, OUT2 | 0 | | 6 | A |
| $I_{IPROPI}$ | Current sense output current | IPROPI | 0 | | 3 | mA |
| $V_{VREF}$ | Current limit reference voltage | VREF | 0 | | 3.6 | V |
| $T_A$ | Operating ambient temperature | | –40 | | 125 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 150 | °C |

(1) Power dissipation and thermal limits must be observed

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

## 6.4 Thermal Information

| THERMAL METRIC | | DRV8874-Q1 PWP (HTSSOP) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 36.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 27.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 11.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 11.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.7 | °C/W |

## 6.5 Electrical Characteristics

4.5 V ≤ $V_{VM}$ ≤ 37 V, –40°C ≤ $T_J$ ≤ 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES (VCP, VM)** | | | | | | |
| $I_{VMQ}$ | VM sleep mode current | $V_{VM}$ = 13.5 V, nSLEEP = 0 V, $T_J$ = 25°C | | 0.75 | 1 | µA |
| | | nSLEEP = 0 V | | | 5 | µA |
| $I_{VM}$ | VM active mode current | $V_{VM}$ = 13.5 V, nSLEEP = 5 V, EN/IN1 = PH/IN2 = 0 V | | 3 | 7 | mA |
| $t_{WAKE}$ | Turnon time | $V_{VM}$ > $V_{UVLO}$, nSLEEP = 5 V to active | | | 1 | ms |
| $t_{SLEEP}$ | Turnoff time | nSLEEP = 0 V to sleep mode | | | 1 | ms |
| $V_{VCP}$ | Charge pump regulator voltage | VCP with respect to VM, $V_{VM}$ = 13.5 V | | 5 | | V |
| $f_{VCP}$ | Charge pump switching frequency | | | 400 | | kHz |
| **LOGIC-LEVEL INPUTS (EN/IN1, PH/IN2, nSLEEP)** | | | | | | |
| $V_{IL}$ | Input logic low voltage | $V_{VM}$ < 5 V | 0 | | 0.7 | V |
| | | $V_{VM}$ ≥ 5 V | 0 | | 0.8 | |
| $V_{IH}$ | Input logic high voltage | | 1.5 | | 5.5 | V |
| $V_{HYS}$ | Input hysteresis | | | 200 | | mV |
| | | nSLEEP | | 50 | | mV |
| $I_{IL}$ | Input logic low current | $V_I$ = 0 V | –5 | | 5 | µA |
| $I_{IH}$ | Input logic high current | $V_I$ = 5 V | | 50 | 75 | µA |
| $R_{PD}$ | Input pulldown resistance | To GND | | 100 | | kΩ |
| **TRI-LEVEL INPUTS (PMODE)** | | | | | | |
| $V_{TIL}$ | Tri-level input logic low voltage | | 0 | | 0.65 | V |
| $V_{TIZ}$ | Tri-level input Hi-Z voltage | | 0.9 | 1.1 | 1.2 | V |
| $V_{TIH}$ | Tri-level input logic high voltage | | 1.5 | | 5.5 | V |
| $I_{TIL}$ | Tri-level input logic low current | $V_I$ = 0 V | –50 | –32 | | µA |
| $I_{TIZ}$ | Tri-level input Hi-Z current | $V_I$ = 1.1 V | –5 | | 5 | µA |
| $I_{TIH}$ | Tri-level input logic high current | $V_I$ = 5 V | | 113 | 150 | µA |
| $R_{TPD}$ | Tri-level pulldown resistance | To GND | | 44 | | kΩ |
| $R_{TPU}$ | Tri-level pullup resistance | To internal 5 V | | 156 | | kΩ |
| **QUAD-LEVEL INPUTS (IMODE)** | | | | | | |
| $V_{QI2}$ | Quad-level input level 1 | Voltage to set quad-level 1 | 0 | | 0.45 | V |
| $R_{QI2}$ | Quad-level input level 2 | Resistance to GND to set quad-level 2 | 18.6 | 20 | 21.4 | kΩ |
| $R_{QI3}$ | Quad-level input level 3 | Resistance to GND to set quad-level 3 | 57.6 | 62 | 66.4 | kΩ |
| $V_{QI4}$ | Quad-level input level 4 | Voltage to set quad-level 4 | 2.5 | | 5.5 | V |
| $R_{QPD}$ | Quad-level pulldown resistance | To GND | | 136 | | kΩ |
| $R_{QPU}$ | Quad-level pullup resistance | To internal 5 V | | 68 | | kΩ |
| **OPEN-DRAIN OUTPUTS (nFAULT)** | | | | | | |

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

## Electrical Characteristics (continued)

4.5 V ≤ $V_{VM}$ ≤ 37 V, –40°C ≤ $T_J$ ≤ 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output logic low voltage | $I_{OD}$ = 5 mA | | | 0.3 | V |
| $I_{OZ}$ | Output logic high current | $V_{OD}$ = 5 V | –2 | | 2 | µA |
| **DRIVER OUTPUTS (OUT1, OUT2)** | | | | | | |
| $R_{DS(on)_HS}$ | High-side MOSFET on resistance | $V_{VM}$ = 13.5 V, $I_O$ = 2 A, $T_J$ = 25°C | | 100 | 120 | mΩ |
| | | $V_{VM}$ = 13.5 V, $I_O$ = 2 A, $T_J$ = 150°C | | 160 | 190 | mΩ |
| $R_{DS(on)_LS}$ | Low-side MOSFET on resistance | $V_{VM}$ = 13.5 V, $I_O$ = –2 A, $T_J$ = 25°C | | 100 | 120 | mΩ |
| | | $V_{VM}$ = 13.5 V, $I_O$ = –2 A, $T_J$ = 150°C | | 160 | 190 | mΩ |
| $V_{SD}$ | Body diode forward voltage | $I_{SD}$ = 1 A | | 0.9 | | V |
| $t_{RISE}$ | Output rise time | $V_{VM}$ = 13.5 V, OUTx rising 10% to 90% | | 1 | | µs |
| $t_{FALL}$ | Output fall time | $V_{VM}$ = 13.5 V, OUTx falling 90% to 10% | | 1 | | µs |
| $t_{PD}$ | Input to output propagation delay | EN/IN1, PH/IN2 to OUTx | | 1.75 | | µs |
| $t_{DEAD}$ | Output dead time | Body diode conducting | | 750 | | ns |
| **CURRENT SENSE AND REGULATION (IPROPI, VREF)** | | | | | | |
| $A_{IPROPI}$ | Current mirror scaling factor | | | 455 | | µA/A |
| $A_{ERR}$ | Current mirror scaling error | $I_{OUT}$ < 0.3 A | –15 | | 15 | mA |
| | | 0.3 A ≤ $I_{OUT}$ < 1 A | –5 | | 5 | % |
| | | 1 A ≤ $I_{OUT}$ ≤ 4 A | –3.5 | | 3.5 | |
| $t_{OFF}$ | Current regulation off time | | | 25 | | µs |
| $t_{DELAY}$ | Current sense delay time | | | 6 | | µs |
| $t_{DEG}$ | Current regulation deglitch time | | | 1.7 | | µs |
| $t_{BLK}$ | Current regulation blanking time | | | 2.7 | | µs |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{UVLO}$ | Supply undervoltage lockout (UVLO) | $V_{VM}$ rising | 4.3 | 4.45 | 4.6 | V |
| | | $V_{VM}$ falling | 4.2 | 4.35 | 4.5 | V |
| $V_{UVLO_HYS}$ | Supply UVLO hysteresis | | | 100 | | mV |
| $t_{UVLO}$ | Supply undervoltage deglitch time | | | 10 | | µs |
| $V_{CPUV}$ | Charge pump undervoltage lockout | VCP with respect to VM, $V_{VCP}$ falling | | 2.25 | | V |
| $I_{OCP}$ (1) | Overcurrent protection trip point | | 6 | 9 | | A |
| $t_{OCP}$ | Overcurrent protection deglitch time | | | 3 | | µs |
| $t_{RETRY}$ | Overcurrent protection retry time | | | 2 | | ms |
| $T_{TSD}$ | Thermal shutdown temperature | | 160 | 175 | 190 | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | 20 | | °C |

(1) On the "P" prototype version samples, the output short circuit current should be limited to less than 20 A.

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

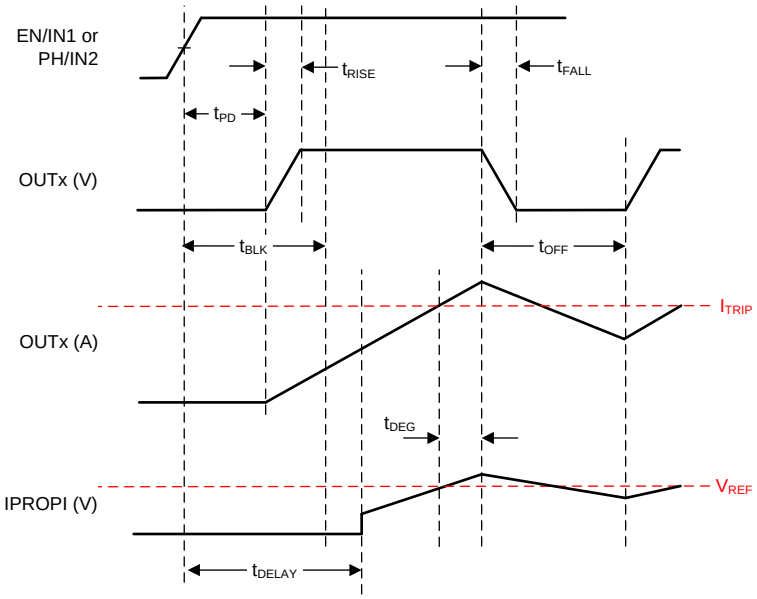



**Figure 1. Timing Parameter Diagram**

ADVANCE INFORMATION

# 7 Detailed Description

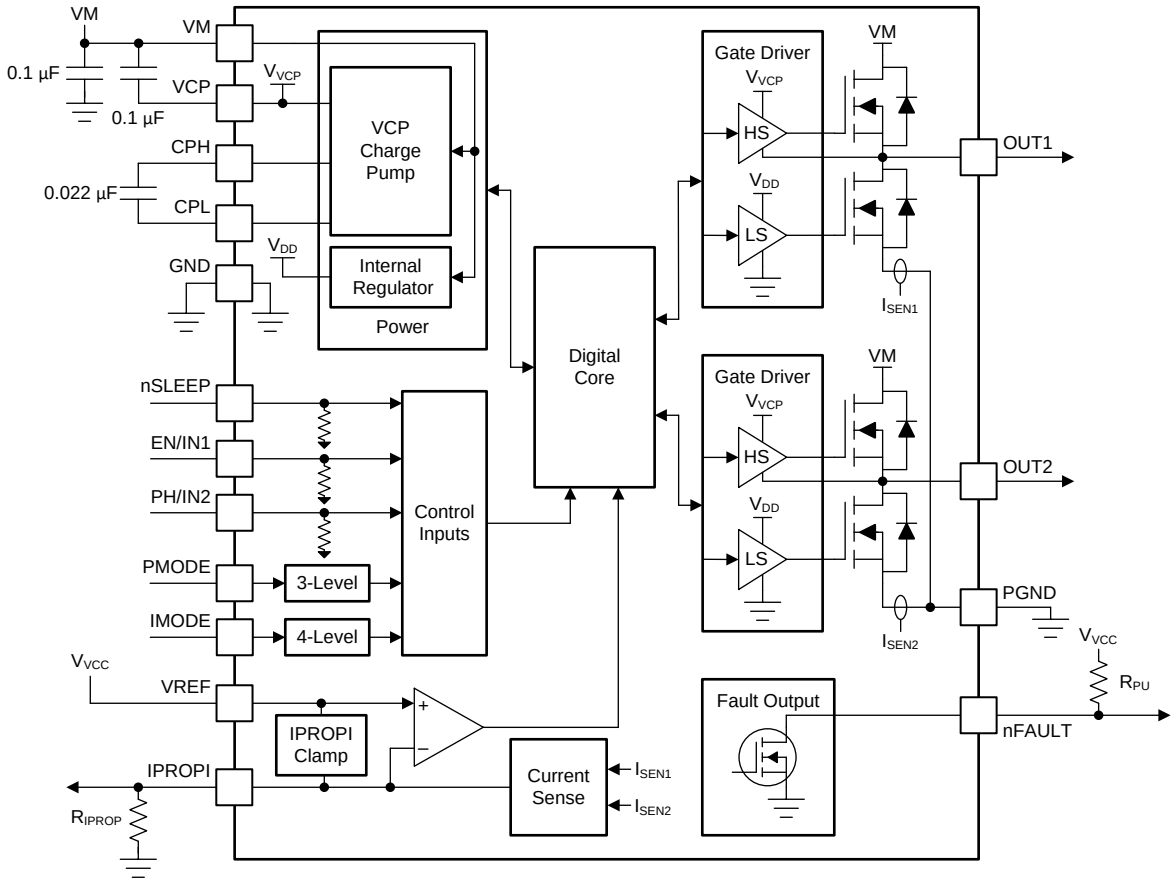
## 7.1 Overview

The DRV887x-Q1 family of devices are brushed DC motor drivers that operate from 4.5 to 37-V supporting a wide range of output load currents for various types of motors and loads. The devices integrate an H-bridge output power stage that can be operated in different control modes set be the PMODE pin setting. This allows for driving a single bidirectional brushed DC motor, two unidirectional brushed DC motors, or other output load configurations. The devices integrate a charge pump regulator to support more efficient high-side N-channel MOSFETs and 100% duty cycle operation. The devices operate off a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The nSLEEP pin provides an ultra low power mode to minimize current draw during system inactivity.

The DRV887x-Q1 family of device also integrate output current sensing using current mirrors on the low-side power MOSFETs. A proportional current is then sent out on the IPROPI pin and can be converted to a proportional voltage using an external resistor ($R_{IPROPI}$). The integrated current sensing allows the DRV887x-Q1 devices to limit the output current with a fixed off-time PWM chopping scheme and provide load information to the external controller to detect change in load or stall conditions. The integrated current sensing out performs traditional external shunt resistor sensing by providing current information even during the off-time slow decay recirculating period and removing the need for an external power shunt resistor. The off-time PWM current regulation level can be configured during motor operation through the VREF pin to limit the load current accordingly to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin.

## 7.2 Functional Block Diagram




ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 External Components

Table 1 lists the recommended external components for the device.

**Table 1. Recommended External Components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| $C_{VM1}$ | VM | GND | 0.1-µF, low ESR ceramic capacitor, VM-rated. |
| $C_{VM1}$ | VM | GND | Bulk Capacitance, VM-rated. |
| $C_{VCP}$ | VCP | VM | X5R or X7R, 100-nF, 16-V ceramic capacitor |
| $C_{FLY}$ | CPH | CPL | X5R or X7R, 22-nF, VM-rated ceramic capacitor |
| $R_{IMODE}$ | IMODE | GND | See Current Regulation. |
| $R_{PMODE}$ | PMODE | GND | See Control Modes. |
| $R_{nFAULT}$ | VCC | nFAULT | Pullup resistor, $I_{OD} \leq$ 5-mA |
| $R_{IPROPI}$ | IPROPI | GND | See Current Sensing. |

### 7.3.2 Control Modes

The DRV887x-Q1 family of devices provide three modes to support different control schemes with the EN/IN1 and PH/IN2 pins. The control mode is selected through the PMODE pin with either logic low, logic high, or setting the pin Hi-Z as shown in Table 2. The PMODE pin state is latched when the device is enabled through the nSLEEP pin. The PMODE state can be changed by taking the nSLEEP pin logic low, waiting the $t_{SLEEP}$ time, changing the PMODE pin input, and then enabling the device by taking the nSLEEP pin back logic high.

**Table 2. PMODE Functions**

| PMODE STATE | CONTROL MODE |
|---|---|
| PMODE = Logic Low | PH/EN |
| PMODE = Logic High | PWM |
| PMODE = Hi-Z | Independent Half-Bridge |

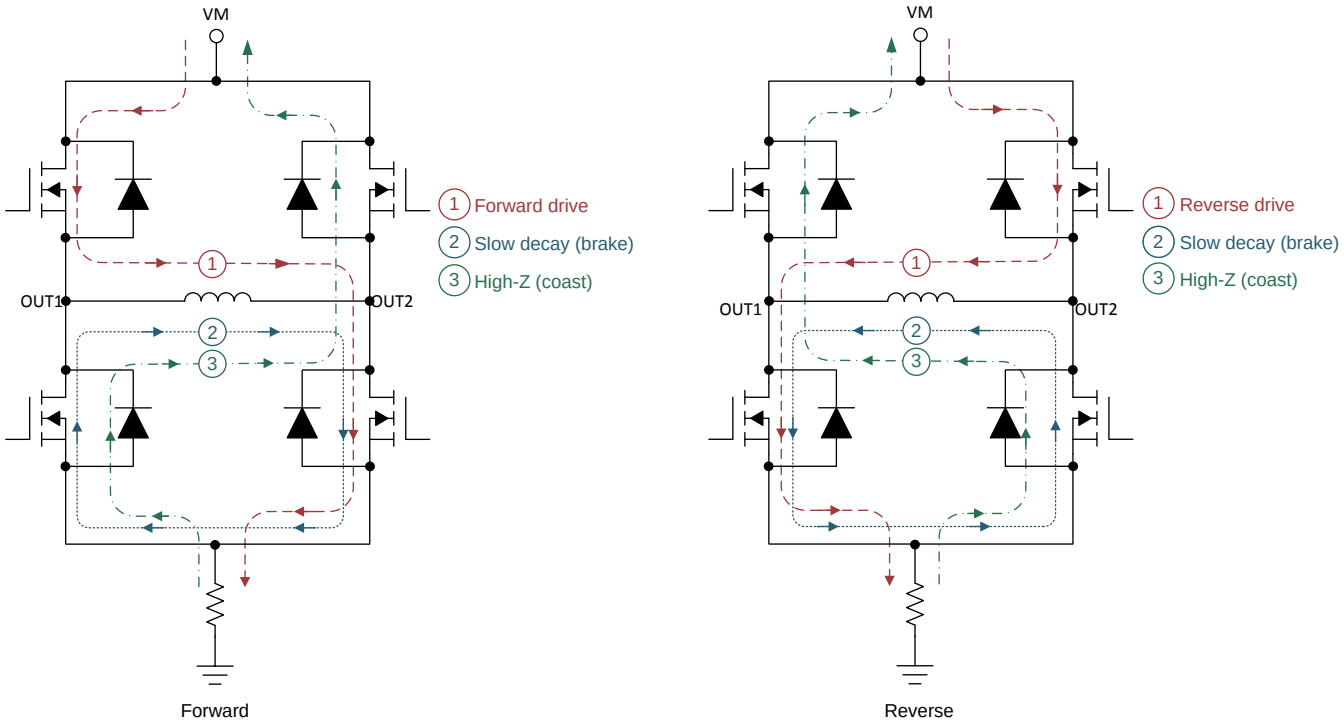



**Figure 2. H-Bridge States**

ADVANCE INFORMATION

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied with no issues. By default, the EN/IN1 and PH/IN2 pins have an internal pulldown resistor to ensure the outputs are Hi-Z if no inputs are present.

The sections below show the truth table for each control mode. Note that these tables do not take into account the internal current regulation feature. Additionally, the DRV887x-Q1 family of device automatically handles the dead-time generation when switching between the high-side and low-side MOSFET of a half-bridge.

Figure 2 describes the naming and configuration for the various H-bridge states.

#### 7.3.2.1 PH/EN Control Mode (PMODE = Logic Low)

When the PMODE pin is logic low on power up, the device is latched into PH/EN mode. PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. The truth table for PH/EN mode is shown in Table 3.

**Table 3. PH/EN Control Mode**

| nSLEEP | EN | PH | OUT1 | OUT2 | DESCRIPTION |
|---|---|---|---|---|---|
| 0 | X | X | Hi-Z | Hi-Z | Sleep, (H-Bridge Hi-Z) |
| 1 | 0 | X | L | L | Brake, (Low-Side Slow Decay) |
| 1 | 1 | 0 | L | H | Reverse (OUT2 → OUT1) |
| 1 | 1 | 1 | H | L | Forward (OUT1 → OUT2) |

#### 7.3.2.2 PWM Control Mode (PMODE = Logic High)

When the PMODE pin is logic high on power up, the device is latched into PWM mode. PWM mode allows for the H-bridge to enter the Hi-Z state without taking the nSLEEP pin logic low. The truth table for PWM mode is shown in Table 4.

**Table 4. PWM Control Mode**

| nSLEEP | IN1 | IN2 | OUT1 | OUT2 | DESCRIPTION |
|---|---|---|---|---|---|
| 0 | X | X | Hi-Z | Hi-Z | Sleep, (H-Bridge Hi-Z) |
| 1 | 0 | 0 | Hi-Z | Hi-Z | Coast, (H-Bridge Hi-Z) |
| 1 | 0 | 1 | L | H | Reverse (OUT2 → OUT1) |
| 1 | 1 | 0 | H | L | Forward (OUT1 → OUT2) |
| 1 | 1 | 1 | L | L | Brake, (Low-Side Slow Decay) |

#### 7.3.2.3 Independent Half-Bridge Control Mode (PMODE = Hi-Z)

When the PMODE pin is Hi-Z on power up, the device is latched into independent half-bridge control mode. This mode allows for each half-bridge to be directly controlled in order to support high-side slow decay or driving two independent loads. The truth table for independent half-bridge mode is shown in Table 5.

In independent half-bridge control mode, current sensing and feedback are still available, but the internal current regulation is disabled since each half-bridge is operating independently. Additionally, if both low-side MOSFETs are conducting current at the same time, the IPROPI scaled output will be the sum of the currents. See Current Sense and Regulation for more information.

**Table 5. Independent Half-Bridge Control Mode**

| nSLEEP | INx | OUTx | DESCRIPTION |
|---|---|---|---|
| 0 | X | Hi-Z | Sleep, (H-Bridge Hi-Z) |
| 1 | 0 | L | OUTx Low-Side On |
| 1 | 1 | H | OUTx High-Side On |

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

### 7.3.3 Current Sense and Regulation

The DRV887x-Q1 family of devices integrate current sensing, regulation, and feedback. These features allow for the device to sense the output current without an external sense resistor or sense circuitry reducing system size, cost, and complexity. This also allows for the devices to limit the output current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through a current proportional output.

#### *7.3.3.1 Current Sensing*

The IPROPI pin outputs an analog current proportional to the current flowing through the low-side power MOSFETs in the H-bridge scaled by $A_{IPROPI}$. The IPROPI output current can be calculated by Equation 1.

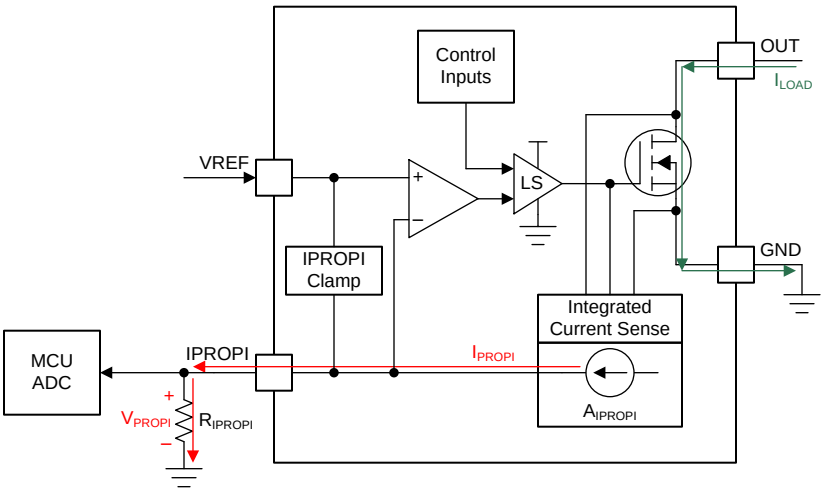
$$I_{PROPI}\ (\mu A) = (I_{LS1} + I_{LS2})\ (A) \times A_{IPROPI}\ (\mu A/A) \quad (1)$$

The current is measured by an internal current mirror architecture that removes the needs for an external power sense resistor. Additionally, the current mirror architecture allows for the motor winding current to be sensed in both the drive and brake low-side slow-decay periods allowing for continuous current monitoring in typical bidirectional brushed DC motor applications. In coast mode, the current is freewheeling and cannot be sensed, but the current can be sampled by briefly reenabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again. In the case of independent PWM mode and both low-side MOSFETs are carrying current, the IPROPI output will be the sum of the two low-side MOSFET currents.

The IPROPI pin should be connected to an external resistor ($R_{IPROPI}$) to ground in order to generate a proportional voltage ($V_{IPROPI}$) on the IPROPI pin with the $I_{IPROPI}$ analog current output. This allows for the load current to be measured as the voltage drop across the $R_{IPROPI}$ resistor with a standard analog to digital converter (ADC). The $R_{IPROPI}$ resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. Additionally, the DRV887x-Q1 devices implements an internal IPROPI voltage clamp circuit to limit $V_{IPROPI}$ with respect to $V_{VREF}$ on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events.

The corresponding IPROPI voltage to the output current can be calculated by Equation 2.

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \quad (2)$$




Copyright © 2017, Texas Instruments Incorporated

**Figure 3. Integrated Current Sensing**

The IPROPI output bandwidth is limited by the sense delay time ($t_{DELAY}$) of the DRV887x-Q1 internal current sensing circuit. This time is the delay from the low-side MOSFET enable command to the IPROPI output being ready. If the device is alternating between drive and slow-decay (brake) in an H-bridge PWM pattern then the low-side MOSFET sensing the current is continuously on and the sense delay time has no impact to the IPROPI output.

ADVANCE INFORMATION

### 7.3.3.2 Current Regulation

The DRV887x-Q1 family of devices integrate current regulation using either a fixed off-time or cycle-by-cycle PWM current chopping scheme. The current chopping scheme is selectable through the IMODE quad-level input. This allows the devices to limit the output current in case of motor stall, high torque, or other high current load events.

The IMODE level can be set by leaving the pin floating (Hi-Z), connecting the pin to GND, or connecting a resistor between IMODE and GND. The IMODE pin state is latched when the device is enabled through the nSLEEP pin. The IMODE state can be changed by taking the nSLEEP pin logic low, waiting the $t_{SLEEP}$ time, changing the IMODE pin input, and then enabling the device by taking the nSLEEP pin back logic high. The IMODE input is also used to select the device response to an overcurrent event. See more details in the Protection Circuits section.

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND (if current feedback isn't required) or if current feedback is required, setting $V_{VREF}$ and $R_{IPROPI}$ such that $V_{IPROPI}$ never reaches the $V_{VREF}$ threshold. In independent half-bridge control mode (PMODE = Hi-Z), the internal current regulation is automatically disabled since the outputs are operating independently and the current sense and regulation is shared between half-bridges.

**Table 6. IMODE Functions**

| IMODE STATE | | IMODE FUNCTION | | nFAULT Response |
|---|---|---|---|---|
| | | Current Chopping Mode | Overcurrent Response | |
| Quad-Level 1 | $R_{IMODE}$ = GND | Fixed Off-Time | Automatic Retry | Overcurrent Only |
| Quad-Level 2 | $R_{IMODE}$ = 20kΩ to GND | Cycle-By-Cycle | Automatic Retry | Current Chopping and Overcurrent |
| Quad-Level 3 | $R_{IMODE}$ = 62kΩ to GND | Cycle-By-Cycle | Outputs Latched Off | Current Chopping and Overcurrent |
| Quad-Level 4 | $R_{IMODE}$ = Hi-Z | Fixed Off-Time | Outputs Latched Off | Overcurrent Only |

The current chopping threshold ($I_{TRIP}$) is set through a combination of the VREF voltage ($V_{VREF}$) and IPROPI output resistor ($R_{IPROPI}$). This is done by comparing the voltage drop across the external $R_{IPROPI}$ resistor to $V_{VREF}$ with an internal comparator.

$$I_{TRIP}\ (A) \times A_{IPROPI}\ (\mu A/A) = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, if $V_{VREF}$ = 2.5 V, $R_{IPROPI}$ = 1500 Ω, and $A_{IPROPI}$ = 1000 μA/A, then $I_{TRIP}$ will be approximately 1.67 A

When the $I_{TRIP}$ threshold is exceeded, the outputs will enter a current chopping mode according to the IMODE setting. The $I_{TRIP}$ comparator has both a blanking time ($t_{BLK}$) and a deglitch time ($t_{DEG}$). The internal blanking time helps to prevent voltage and current transients during output switching from effecting the current regulation. The internal deglitch time ensure that transient conditions do not prematurely trigger the current regulation.

#### 7.3.3.2.1 Fixed Off-Time Current Chopping

In the fixed off-time mode, the H-bridge enters a brake, low-side slow decay (both low-side MOSFETs ON) for $t_{OFF}$ duration after $I_{OUT}$ exceeds $I_{TRIP}$. After $t_{OFF}$ the outputs are re-enabled according to the control inputs unless $I_{OUT}$ is still greater than $I_{TRIP}$. If $I_{OUT}$ is still greater than $I_{TRIP}$, the H-bridge will enter another period of brake, low-side slow decay for $t_{OFF}$. The fixed off-time mode allows for a simple current chopping scheme without involvement from the external controller. This is shown in Figure 4. Fixed off-time mode will support 100% duty cycle current regulation since the H-bridge automatically enables after the $t_{OFF}$ period and does not require a new control input edge on the EN/IN1 or PH/IN2 pins to reset the outputs.

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

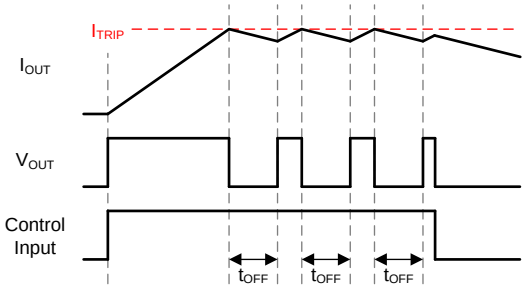



**Figure 4. Off-Time Current-Regulation**

#### 7.3.3.2.2 Cycle-By-Cycle Current Chopping

In cycle-by-cycle mode, the H-bridge enters a brake, low-side slow decay (both low-side MOSFETs ON) after $I_{OUT}$ exceeds $I_{TRIP}$ until the next control input edge on the EN/IN1 or PH/IN2 pins. This allows for additional control of the current chopping scheme by the external controller. This is shown in Figure 5. Cycle-by-cycle mode will not support 100% duty cycle current regulation as a new control input edge is required to reset the outputs after the brake, low-side slow decay state has been entered.

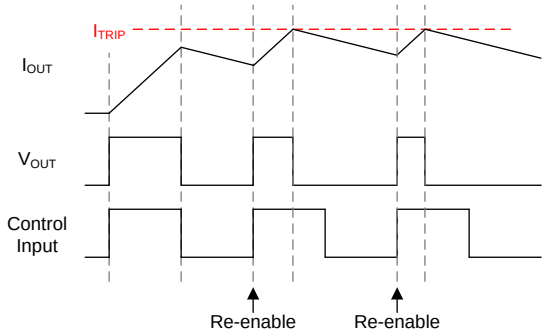



**Figure 5. Cycle-By-Cycle Current Regulation**

In cycle-by-cycle mode, the device will also indicates whenever the H-bridge has entered internal current chopping by pulling the nFAULT pin low. This can be used to determine when the device outputs will differ from the control inputs or the load has reached the $I_{TRIP}$ threshold. This is shown in Figure 6. nFAULT will be released whenever the next control input edge is received by the device and the outputs are reset.

ADVANCE INFORMATION

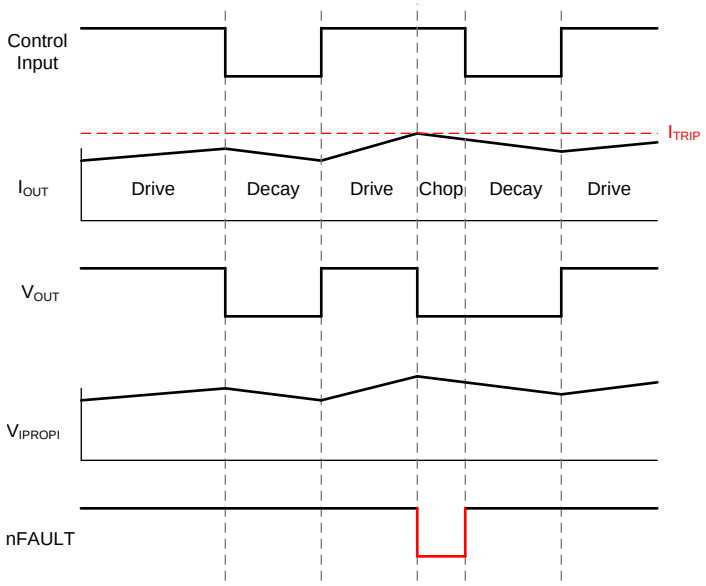



**Figure 6. Cycle-By-Cycle Current Regulation**

No device functionality is affected when the nFAULT pin is pulled low for the current chopping indicator. The nFAULT pin is only used as an indicator and the device will continue normal operation. To distinguish from a device fault (outlined in the Protection Circuits section) from the current chopping indicator, the nFAULT pin can be compared with the control inputs. The current chopping indicator can only assert when the control inputs are commanding a forward or reverse drive state (Figure 2). If the nFAULT pin is pulled low and the control inputs are commanding the high-Z or slow-decay states, then a device fault has occurred.

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

### 7.3.4 Protection Circuits

The DRV887x-Q1 family of devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

#### *7.3.4.1 VM Supply Undervoltage Lockout (UVLO)*

If at any time the supply voltage on the VM pin falls below the undervoltage lockout threshold voltage ($V_{UVLO}$), all MOSFETs in the H-bridge will be disabled and the nFAULT pin driven low. The charge pump is disabled in this condition. Normal operation will resume when the undervoltage condition is removed and VM rises above the $V_{UVLO}$ threshold.

#### *7.3.4.2 VCP Charge Pump Undervoltage Lockout (CPUV)*

If at any time the charge pump voltage on the VCP pin falls below the undervoltage lockout threshold voltage ($V_{CPUV}$), all MOSFETs in the H-bridge will be disabled and the nFAULT pin driven low. Normal operation will resume when the undervoltage condition is removed and VCP rises above the $V_{CPUV}$ threshold.

#### *7.3.4.3 OUT Overcurrent Protection (OCP)*

An analog current limit circuit on each MOSFETs limits the peak current out of the device even in hard short circuit events.

If the output current exceeds the overcurrent threshold, $I_{OCP}$, for longer than $t_{OCP}$, all MOSFETs in the H-bridge will be disabled and the nFAULT pin driven low. The overcurrent response can be configured through the IMODE pin as shown in Table 6.

In automatic retry mode, the MOSFETs will be disabled and nFAULT pin driven low for a duration of $t_{RETRY}$. After $t_{RETRY}$, the MOSFETs are re-enabled according to the state of the EN/IN1 and PH/IN2 pins. If the overcurrent condition is still present, the cycle repeats; otherwise normal device operation resumes.

In latched off mode, the MOSFETs will remain disabled and nFAULT pin driven low until the device is reset through either the nSLEEP pin or by removing the VM power supply.

In Independent Half-Bridge Control Mode (PMODE = Hi-Z), the OCP behavior is slightly modified. If an overcurrent event is detected, only the corresponding half-bridge will be disabled and the nFAULT pin driven low. The other half-bridge will continue normal operation. This allows for the device to manage independent fault events when driving independent loads. If an overcurrent event is detected in both half-bridges, both half-bridges will be disabled and the nFAULT pin driven low. In automatic retry mode, both half-bridges share the same overcurrent retry timer. If an overcurrent event occurs first in one half-bridge and then later in the secondary half-bridge, but before $t_{RETRY}$ has expired, the retry timer for the first half-bridge will be reset to $t_{RETRY}$ and both half-bridges will enable again after the retry timer expires.

#### *7.3.4.4 Thermal Shutdown (TSD)*

If the die temperature exceeds the overtemperature limit $T_{TSD}$, all MOSFET in the H-bridge will be disabled and the nFAULT pin driven low. Normal operation will resume when the overtemperature condition is removed and the die temperature drops below the $T_{TSD}$ threshold.

#### *7.3.4.5 Fault Condition Summary*

**Table 7. Fault Condition Summary**

| FAULT | CONDITION | REPORT | H-BRIDGE | RECOVERY |
|---|---|---|---|---|
| $I_{TRIP}$ Indicator | CBC Mode & $I_{OUT} > I_{TRIP}$ | nFAULT | Active Low-Side Slow Decay | Control Input Edge |
| VM Undervoltage Lockout (UVLO) | VM < $V_{UVLO}$ | nFAULT | Disabled | VM > $V_{UVLO}$ |
| VCP Undervoltage Lockout (CPUV) | VCP < $V_{CPUV}$ | nFAULT | Disabled | VCP > $V_{CPUV}$ |
| Overcurrent (OCP) | $I_{OUT} > I_{OCP}$ | nFAULT | Disabled | $t_{RETRY}$ or Reset (Set by IMODE) |
| Thermal Shutdown (TSD) | $T_J > T_{TSD}$ | nFAULT | Disabled | $T_J < T_{TSD} – T_{HYS}$ |

ADVANCE INFORMATION

### 7.3.5 Pin Diagrams

#### 7.3.5.1 Logic-Level Inputs

Figure 7 shows the input structure for the logic-level input pins EN/IN1, PH/IN2, and nSLEEP.

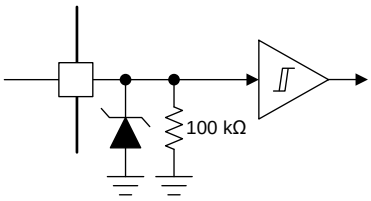



**Figure 7. Logic-Level Input**

#### 7.3.5.2 Tri-Level Inputs

Figure 8 shows the input structure for the tri-level input pin PMODE.

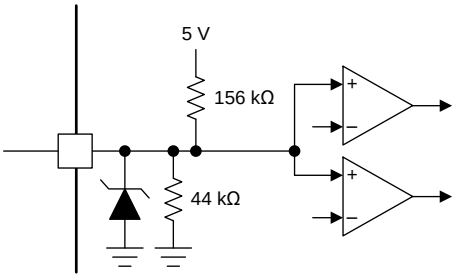



**Figure 8. PMODE Tri-Level Input**

#### 7.3.5.3 Quad-Level Inputs

Figure 9 shows the input structure for the quad-level input pin IMODE.

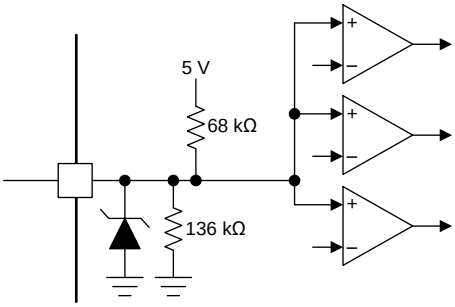



**Figure 9. Quad-Level Input**

## 7.4 Device Functional Modes

The DRV887x-Q1 family of devices have several different modes of operation depending on the system inputs.

### 7.4.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold $V_{UVLO}$, the nSLEEP pin is logic high, and $t_{WAKE}$ has elapsed, the device enters its active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs. The input control mode (PMODE) and current control modes (IMODE) will be latched when the device enters active mode.

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

## Device Functional Modes (continued)

### 7.4.2 Low-Power Sleep Mode

The DRV887x-Q1 family of devices support a low power mode to reduce current consumption from the VM pin when the driver is not active. This mode is entered by setting the nSLEEP pin logic low and waiting for $t_{SLEEP}$ to elapse. In sleep mode, the H-bridge, charge pump, internal 5-V regulator, and internal logic are disabled. The device relies on a weak pulldown to ensure all of the internal MOSFETs remain disabled. The device will not respond to any inputs besides nSLEEP while in low-power sleep mode.

### 7.4.3 Fault Mode

The DRV887x-Q1 family of devices enter a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in Table 7 and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

ADVANCE INFORMATION

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DRV887x-Q1 family of devices can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, and actuators. The device can also be utilized to drive many common passive loads such as LEDs, resistive elements, relays, etc. The application examples below will highlight how to use the device in bidirectional current control applications requiring an H-bridge driver and dual unidirectional current control applications requiring two half-bridge drivers.

## 8.2 Typical Application

### 8.2.1 Primary Application

In the primary application example, the device is configured to drive a bidirectional current through an external load (such as a brushed DC motor) using an H-bridge configuration. The H-bridge polarity and duty cycle are controlled with a PWM and IO resource from the external controller to the EN/IN1 and PH/IN2 pins. The device is configured for the PH/EN control mode by tying the PMODE pin to GND. The current limit threshold ($I_{TRIP}$) is generated with an external resistor divider from the control logic supply voltage ($V_{CC}$). The device is configured for the fixed off-time current regulation scheme by tying the IMODE pin to GND. The load current is monitored with an ADC from the controller to detect the voltage across $R_{IPROPI}$.

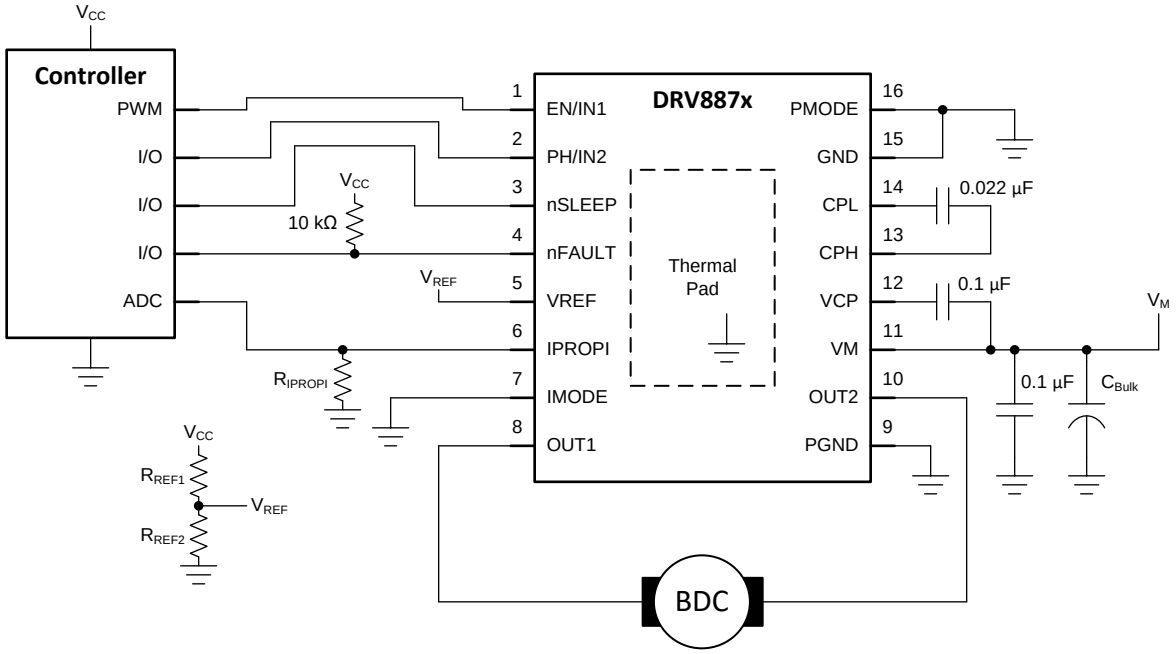



**Figure 10. Typical Application Schematic**

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

## Typical Application (continued)

### 8.2.1.1 Design Requirements

**Table 8. Design Parameters**

| REFERENCE | DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|---|
| $V_M$ | Motor and driver supply voltage | 13.5 V |
| $V_{CC}$ | Controller supply voltage | 3.3 V |
| $I_{RMS}$ | Output RMS current | 0.5 A |
| $f_{PWM}$ | Switching frequency | 20 kHz |
| $I_{TRIP}$ | Current regulation trip point | 1 A |
| $A_{IPROPI}$ | Current sense scaling factor | 1000 µA/A |
| $R_{IPROPI}$ | IPROPI external resistor | 2.5 kΩ |
| $V_{REF}$ | Current regulation reference voltage | 2.5 V |
| $V_{ADC}$ | Controller ADC reference voltage | 2.5 V |
| $R_{REF1}$ | VREF external resistor | 16 kΩ |
| $R_{REF2}$ | VREF external resistor | 50 kΩ |
| $T_A$ | PCB ambient temperature | –20 to 85 °C |
| $T_J$ | Device max junction temperature | 150 °C |
| $R_{\theta JA}$ | Device junction to ambient thermal resistance | 35 °C/W |

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Current Sense and Regulation

The DRV887x-Q1 family of devices provide integrated regulation and sensing out the output current.

The current sense feedback is configured by scaling the $R_{IPROPI}$ resistor to properly sense the scaled down output current from IPROPI within the dynamic voltage range of the controller ADC. An example of this is shown.

$$R_{IPROPI} <= V_{ADC} / (I_{TRIP} \times A_{IPROPI}) \quad (4)$$

$$R_{IPROPI} = 2.5\ k\Omega <= 2.5\ V / (1\ A \times 1000\ \mu A/A) \quad (5)$$

If $V_{ADC}$ = 2.5 V, $I_{TRIP}$ = 1 A, and $A_{IPROPI}$ = 1000 µA/A then to maximize the dynamic IPROPI voltage range an $R_{IPROPI}$ of approximately 2.5 kΩ should be selected.

The accuracy tolerance of $R_{IPROPI}$ can be selected based on the application requirements. 10%, 5%, 1%, 0.1% are all valid tolerance values. The typical recommendation is 1% for best tradeoff between performance and cost.

The output current regulation trip point ($I_{TRIP}$) is configured with a combination of $V_{REF}$ and $R_{IPROPI}$. Since $R_{IPROPI}$ was previously calculated and $A_{IPROPI}$ is a constant, all the remains is to calculate $V_{REF}$.

$$V_{REF} = R_{IPROPI} \times (I_{TRIP} \times A_{IPROPI}) \quad (6)$$

$$V_{REF} = 2.5\ V = 2.5\ k\Omega \times (1\ A \times 1000\ \mu A/A) \quad (7)$$

If $R_{IPROPI}$ = 2.5 kΩ, $I_{TRIP}$ = 1 A, and $A_{IPROPI}$ = 1000 µA/A then $V_{REF}$ should be set to 2.5 V.

$V_{REF}$ can be generated with a simple resistor divider ($R_{REF1}$ and $R_{REF2}$) from the controller supply voltage. The resistor sizing can be achieved by selecting a value for $R_{REF1}$ and calculating the required value for $R_{REF2}$.

#### 8.2.1.2.2 Power Dissipation and Output Current Capability

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation for the device is composed of three main components. These are the quiescent supply current dissipation, the power MOSFET switching losses. and the power MOSFET $R_{DS(on)}$ (conduction) losses. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (8)$$

$P_{VM}$ can be calculated from the nominal supply voltage ($V_M$) and the $I_{VM}$ active mode current specification.

ADVANCE INFORMATION

$$P_{VM} = V_M \times I_{VM} \quad (9)$$

$$P_{VM} = 0.054\ W = 13.5\ V \times 4\ mA \quad (10)$$

$P_{SW}$ can be calculated from the nominal supply voltage ($V_M$), average output current ($I_{RMS}$), switching frequency ($f_{PWM}$) and the device output rise ($t_{RISE}$) and fall ($t_{FALL}$) time specifications.

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} \quad (11)$$

$$P_{SW_RISE} = 0.5 \times V_M \times I_{RMS} \times t_{RISE} \times f_{PWM} \quad (12)$$

$$P_{SW_FALL} = 0.5 \times V_M \times I_{RMS} \times t_{FALL} \times f_{PWM} \quad (13)$$

$$P_{SW_RISE} = 0.0675\ W = 0.5 \times 13.5\ V \times 0.5\ A \times 1\ \mu s \times 20\ kHz \quad (14)$$

$$P_{SW_FALL} = 0.0675\ W = 0.5 \times 13.5\ V \times 0.5\ A \times 1\ \mu s \times 20\ kHz \quad (15)$$

$$P_{SW} = 0.135\ W = 0.0675\ W + 0.0675\ W \quad (16)$$

$P_{RDS}$ can be calculated from the device $R_{DS(on)}$ and average output current ($I_{RMS}$)

$$P_{RDS} = I_{RMS}^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (17)$$

It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(on)}$ with temperature can be found in the Typical Characteristics curves. Assuming a device temperature of 85 °C it can be expected that $R_{DS(on)}$ will see an increases of ~1.25 based on the normalized temperature data.

$$P_{RDS} = 0.219\ W = 0.5\ A^2 \times (350\ m\Omega \times 1.25 + 350\ m\Omega \times 1.25) \quad (18)$$

By adding together the different power dissipation components it can be verified that the expected power dissipation and device junction temperature is within design targets.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (19)$$

$$P_{TOT} = 0.408\ W = 0.054\ W + 0.135\ W + 0.219\ W \quad (20)$$

The device junction temperature can be calculated with the $P_{TOT}$, device ambient temperature ($T_A$), and package thermal resistance ($R_{\theta JA}$). The value for $R_{\theta JA}$ is heavily dependent on the PCB design and copper heat sinking around the device.

$$T_J = (P_{TOT} \times R_{\theta JA}) + T_A \quad (21)$$

$$T_J = 99°C = (0.408\ W \times 35\ °C/W) + 85°C \quad (22)$$

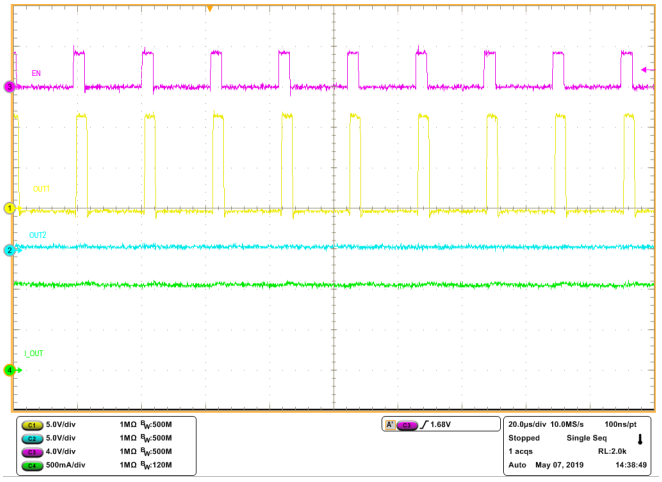
It should be ensured that the device junction temperature is within the specified operating region. Other methods exist for verifying the device junction temperature depending on the measurements available.

Additional information on motor driver current ratings and power dissipation can be found in and Related Documentation.

ADVANCE INFORMATION

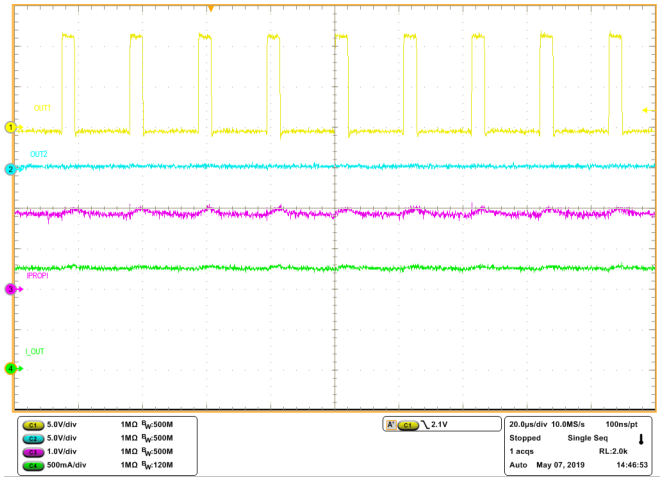

Copyright © 2019, Texas Instruments Incorporated

### 8.2.1.3 Application Curves



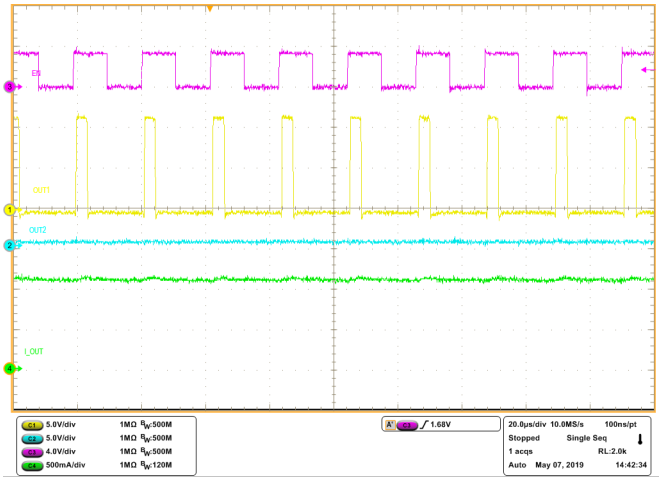

Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan 4 = IOUT

**Figure 11. Driver PWM Operation (PH/EN)**



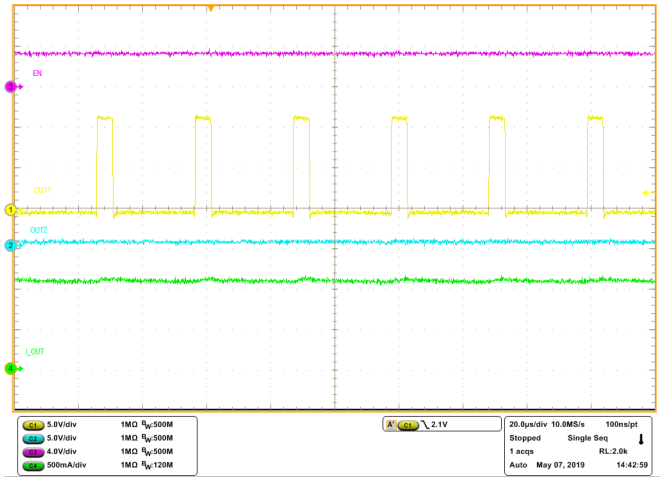

Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = IPROPI
Chan 4 = IOUT

**Figure 12. Driver PWM Operation With Current Feedback**




Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan 4 = IOUT

**Figure 13. Driver PWM Operation With Current Chopping**




Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan 4 = IOUT

**Figure 14. Driver Full On Operation With Current Chopping**

ADVANCE INFORMATION

## 8.2.2 Alternative Application

In the alternative application example, the device is configured to drive a unidirectional current through two external loads (such as two brushed DC motors) using a dual half-bridge configuration. The duty cycle of each half-bridge is controlled with a PWM resource from the external controller to the EN/IN1 and PH/IN2 pins. The device is configured for the independent half-bridge control mode by leaving the PMODE pin floating. Since the current regulation scheme is disabled in the independent half-bridge control mode, the VREF pin is tied to $V_{CC}$. The combined load current is monitored with an ADC from the controller to detect the voltage across $R_{IPROPI}$.

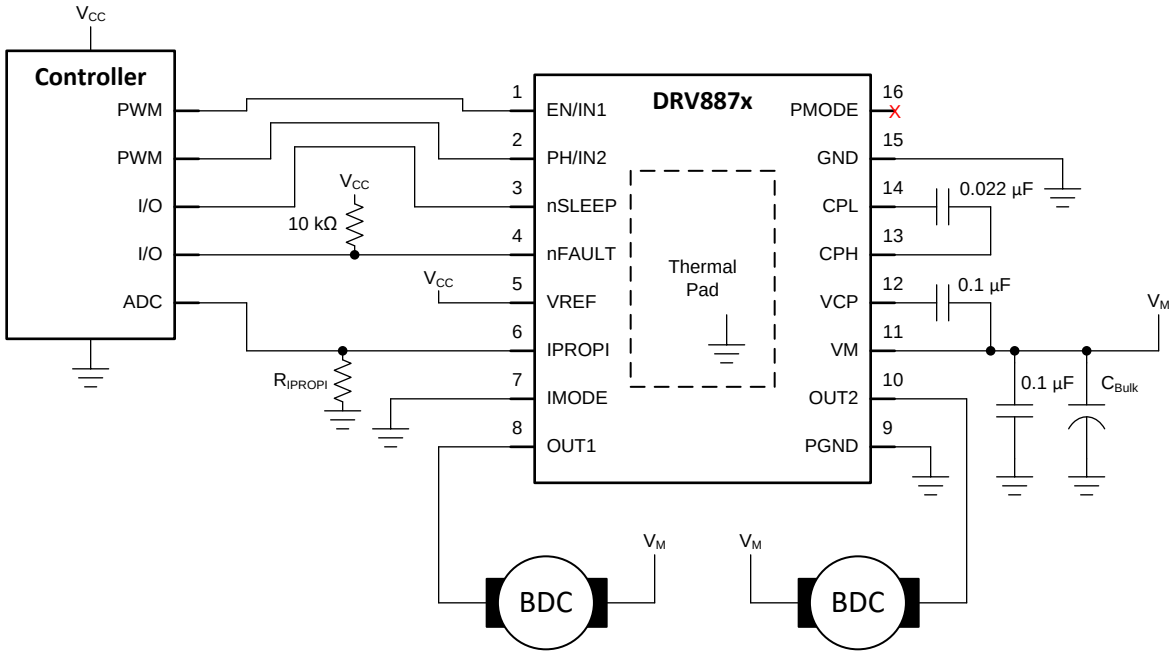



**Figure 15. Typical Application Schematic**

### 8.2.2.1 Design Requirements

**Table 9. Design Parameters**

| REFERENCE | DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|---|
| $V_M$ | Motor and driver supply voltage | 13.5 V |
| $V_{CC}$ | Controller supply voltage | 3.3 V |
| $I_{RMS1}$ | Output 1 RMS current | 0.5 A |
| $I_{PEAK1}$ | Output 1 peak current | 1 A |
| $I_{RMS2}$ | Output 2 RMS current | 0.25 A |
| $I_{PEAK2}$ | Output 2 peak current | 0.5 A |
| $f_{PWM}$ | Switching frequency | 20 kHz |
| $A_{IPROPI}$ | Current sense scaling factor | 1000 µA/A |
| $R_{IPROPI}$ | IPROPI external resistor | 2.5 kΩ |
| $V_{ADC}$ | Controller ADC reference voltage | 3.3 V |
| $T_A$ | PCB ambient temperature | –20 to 85 °C |
| $T_J$ | Device max junction temperature | 150 °C |
| $R_{\theta JA}$ | Device junction to ambient thermal resistance | 35 °C/W |

### 8.2.2.2 Detailed Design Procedure

You can refer to the Primary Application Detailed Design Procedure section for a detailed design procedure example. The majority of the design concepts apply to the alternative application example. A few changes to the procedure are outlined below.

#### 8.2.2.2.1 Current Sense and Regulation

In the alternative application for two half-bridge loads, the IPROPI output will be the combination of the two outputs currents. The current sense feedback resistor $R_{IPROPI}$ should be scaled appropriately to stay within the dynamic voltage range of the controller ADC. An example of this is shown

$$R_{IPROPI} <= V_{ADC} / ((I_{PEAK1} + I_{PEAK2}) \times A_{IPROPI}) \quad (23)$$

$$R_{IPROPI} = 2.2\ k\Omega <= 3.3\ V / ((1\ A + 0.5\ A) \times 1000\ \mu A/A) \quad (24)$$

ADVANCE INFORMATION

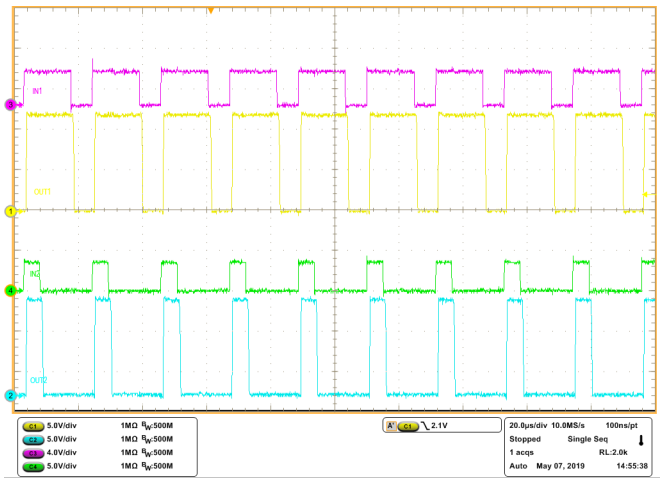

Copyright © 2019, Texas Instruments Incorporated

If $V_{ADC}$ = 3.3 V, $I_{PEAK1}$ = 1 A, $I_{PEAK2}$ = 0.5 A, and $A_{IPROPI}$ = 1000 µA/A then to maximize the dynamic IPROPI voltage range an $R_{IPROPI}$ of approximately 2.2 kΩ should be selected.

The accuracy tolerance of $R_{IPROPI}$ can be selected based on the application requirements. 10%, 5%, 1%, 0.1% are all valid tolerance values. The typical recommendation is 1% for best tradeoff between performance and cost.

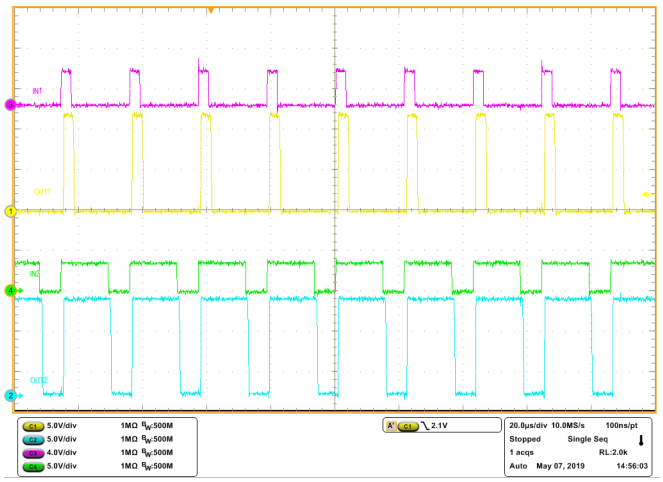
In independent half-bridge mode, the internal current regulation of the device is disabled. $V_{REF}$ can be set directly to the supply reference for the controller ADC.

### *8.2.2.3 Application Curves*




Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan. 4 = PH/IN2

**Figure 16. Independent Half-Bridge PWM Operation**




Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan. 4 = PH/IN2

**Figure 17. Independent Half-Bridge PWM Operation**

ADVANCE INFORMATION

# 9 Power Supply Recommendations

## 9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local bulk capacitance needed depends on a variety of factors, including:

- The highest current required by the motor or load
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple of the system
- The motor braking method (if applicable)

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended minimum value, but system level testing is required to determine the appropriately sized bulk capacitor.

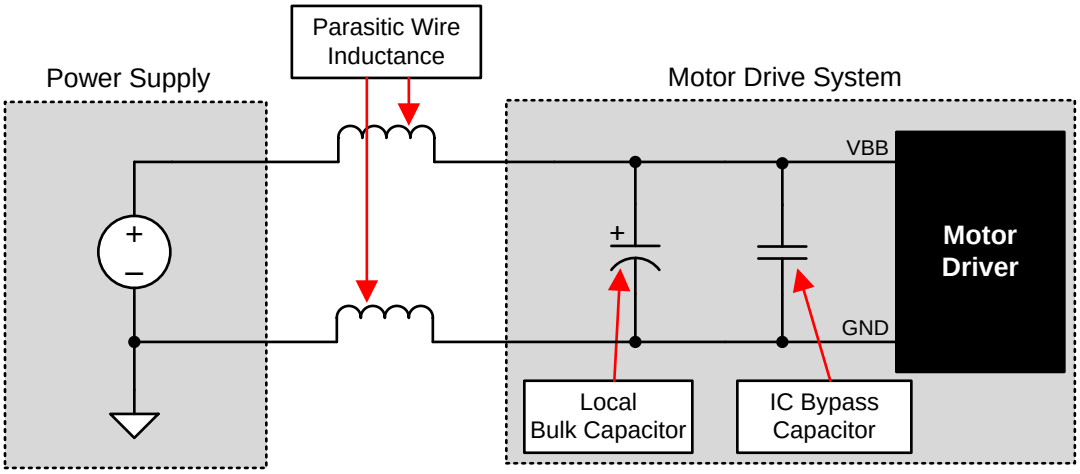



**Figure 18. System Supply Parasitics Example**

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

# 10 Layout

## 10.1 Layout Guidelines

Since the DRV887x-Q1 family of devices are integrated power MOSFETs device capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor, the VCP to VM charge pump storage capacitor, and the charge pump flying capacitor. X5R and X7R types are recommended.
- The VM power supply and VCP, CPH, CPL charge pump capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and PGND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- PGND and GND should connect together directly on the PCB ground plane. They are not intended to be isolated from each other.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

## 10.2 Layout Example

### 10.2.1 HTSSOP Layout Example

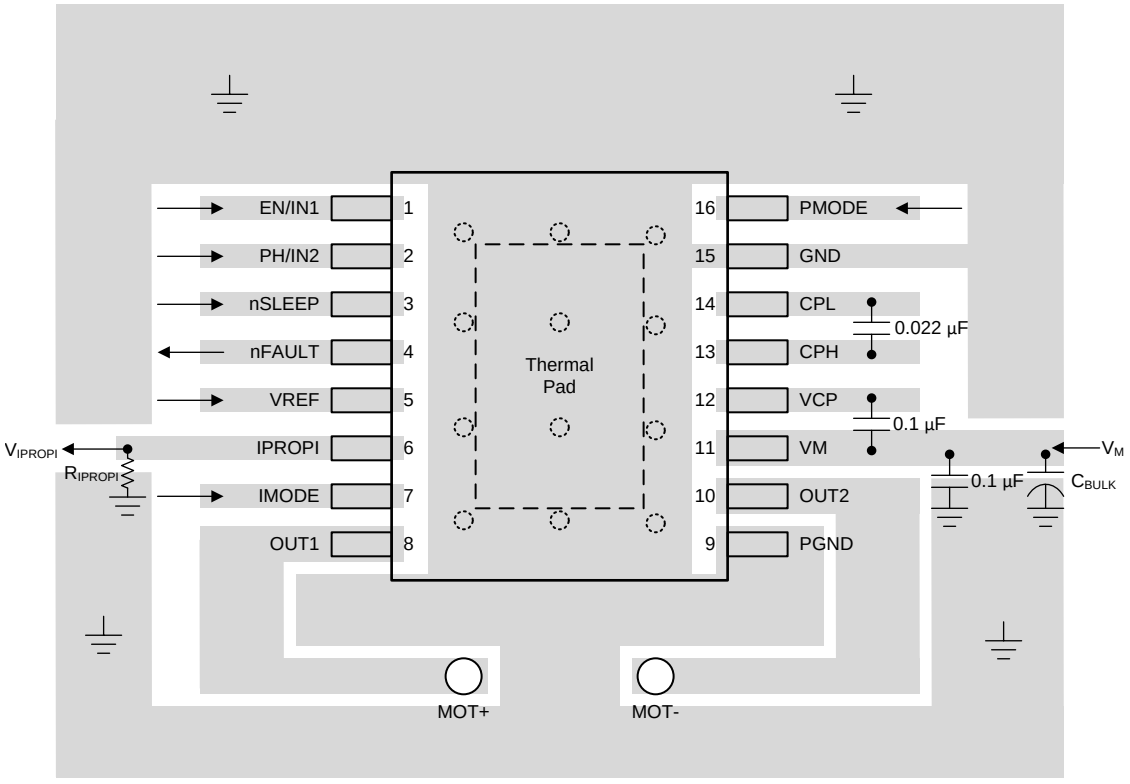



**Figure 19. HTSSOP (PWP) Example Layout**

ADVANCE INFORMATION

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION


Copyright © 2019, Texas Instruments Incorporated

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8874QPWPRQ1 | PREVIEW | HTSSOP | PWP | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |
| PDRV8874QPWPRQ1 | ACTIVE | HTSSOP | PWP | 16 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF DRV8874-Q1 :**

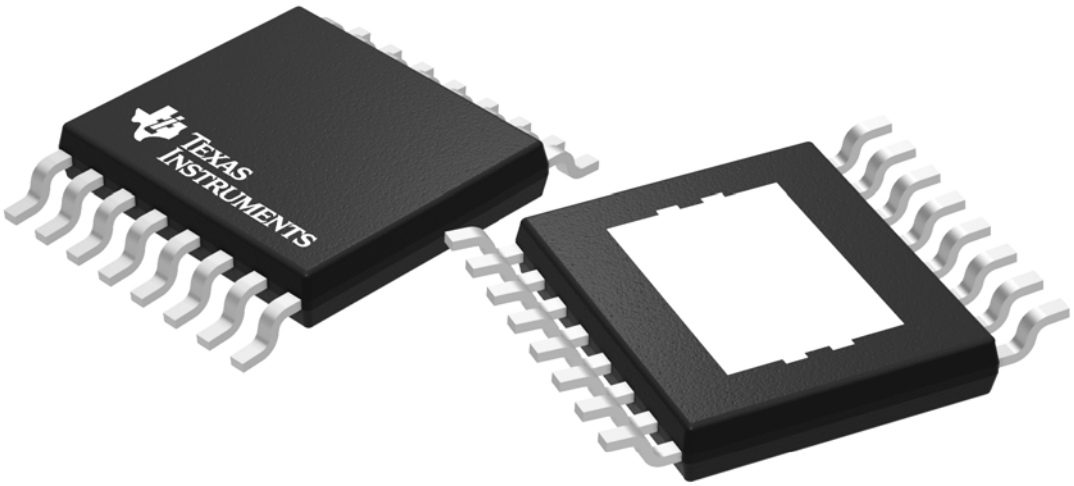
- Catalog: DRV8874

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

# PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated