DRV8876N H-Bridge Motor Driver

1 Features

- N-channel H-bridge motor driver
  - Drives one bidirectional brushed DC motor
  - Two unidirectional brushed DC motors
  - Other resistive and inductive loads
- 4.5-V to 37-V operating supply voltage range
- High output current capability: 3.5-A Peak
- Selectable input control modes (PMODE)
  - PH/EN and PWM H-bridge control modes
  - Independent half-bridge control mode
- Supports 1.8-V, 3.3-V, and 5-V logic inputs
- Ultra low-power sleep mode
  - <1-µA @ V_{VM} = 24-V, T_J = 25°C
- Spread spectrum clocking for low electromagnetic interference (EMI)
- Integrated protection features
  - Undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
    - Automatic retry or outputs latched off (IMODE)
  - Thermal shutdown (TSD)
  - Automatic fault recovery
  - Fault indicator pin (nFAULT)

2 Applications

- Brushed DC motors
- Major and small home appliances
- Vacuum, humanoid, and toy robotics
- Printers and scanners
- Smart meters
- ATMs, currency counters, and EPOS
- Servo motors and actuators

3 Description

The DRV887x family of devices are flexible motor drivers for a wide variety of applications. The devices integrate an N-channel H-bridge, charge pump regulator, and protection circuitry. The charge pump improves efficiency by allowing for both high-side and low-side N-channels MOSFETs and 100% duty cycle support. The family of devices come in pin-to-pin, scalable $R_{DS(on)}$ options to support different loads with minimal design changes.

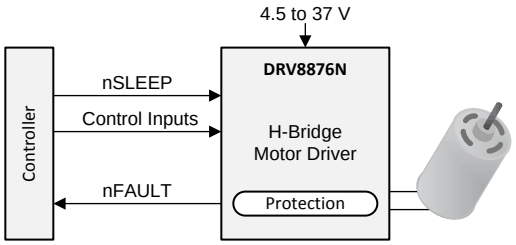
A low-power sleep mode is provided to achieve ultra-low quiescent current draw by shutting down most of the internal circuitry. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output overcurrent (OCP), and device overtemperature (TSD). Fault conditions are indicated on nFAULT.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8876N	HTSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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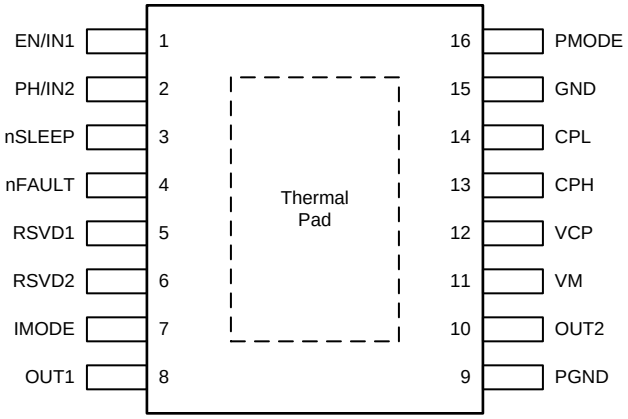
4 Revision History

DATE	REVISION	NOTES
August 2019	*	Initial release.

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5 Pin Configuration and Functions

DRV8876N PWP Package
16-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	PWP		
CPH	13	PWR	Charge pump switching node. Connect a X5R or X7R, 22-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	14	PWR	
EN/IN1	1	I	H-bridge control input. See Control Modes. Internal pulldown resistor.
GND	15	PWR	Device ground. Connect to system ground.
IMODE	7	I	Overcurrent protection mode. See OUTx Overcurrent Protection (OCP). Quad-level input.
nFAULT	4	OD	Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation. See Protection Circuits.
nSLEEP	3	I	Sleep mode input. Logic high to enable device. Logic low to enter low-power sleep mode. See Device Functional Modes. Internal pulldown resistor.
OUT1	8	O	H-bridge output. Connect to the motor or other load.
OUT2	10	O	H-bridge output. Connect to the motor or other load.
PGND	9	PWR	Device power ground. Connect to system ground.
PH/IN2	2	I	H-bridge control input. See Control Modes. Internal pulldown resistor.
PMODE	16	I	H-bridge control input mode. See Control Modes. Tri-level input.
RSVD1	5	I	Reserved pin. Connect to a voltage greater than 1 V. Recommend connecting this pin to the system logic supply rail or to nSLEEP.
RSVD2	6	O	Reserved pin. Connect to system ground.
VCP	12	PWR	Charge pump output. Connect a X5R or X7R, 100-nF, 16-V ceramic capacitor between the VCP and VM pins.
VM	11	PWR	4.5-V to 37-V power supply input. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient Bulk Capacitance rated for VM.
PAD	—	—	Thermal pad. Connect to system ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	–0.3	40	V
Voltage difference between ground pins	GND, PGND	–0.3	0.3	V
Charge pump pin voltage	CPH, VCP	V_{VM} – 0.3	V_{VM} + 7	V
Charge pump low-side pin voltage	CPL	–0.3	V_{VM} + 0.3	V
Logic pin voltage	EN/IN1, IMODE, nSLEEP, PH/IN2, PMODE	–0.3	5.75	V
Open-drain output pin voltage	nFAULT	–0.3	5.75	V
Output pin voltage	OUT1, OUT2	–0.9	V_{VM} + 0.9	V
Output pin current	OUT1, OUT2	Internally Limited	Internally Limited	A
Reserved pin voltage	RSVD1, RSVD2	–0.3	5.75	V
		–0.3	V_{VM} + 0.3	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	4.5		37	V
V_{IN}	Logic input voltage	EN/IN1, MODE, nSLEEP, PH/IN2	0		5.5	V
f_{PWM}	PWM frequency	EN/IN1, PH/IN2	0		100	kHz
V_{OD}	Open drain pullup voltage	nFAULT	0		5.5	V
I_{OD}	Open drain output current	nFAULT	0		5	mA
I_{OUT}(1)	Peak output current	OUT1, OUT2	0		3.5	A
V_{RSVD1}	RSVD1 reserved pin voltage	RSVD1	0		5.5	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

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6.4 Thermal Information

THERMAL METRIC(1)		DRV8876N PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

4.5 V ≤ V_{VM} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCP, VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 24 V, nSLEEP = 0 V, T_J = 25°C		0.75	1	µA
		nSLEEP = 0 V			5	µA
I_{VM}	VM active mode current	V_{VM} = 24 V, nSLEEP = 5 V, EN/IN1 = PH/IN2 = 0 V		3	7	mA
t_{WAKE}	Turnon time	V_{VM} > V_{UVLO}, nSLEEP = 5 V to active			1	ms
t_{SLEEP}	Turnoff time	nSLEEP = 0 V to sleep mode			1	ms
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM, V_{VM} = 24 V		5		V
f_{VCP}	Charge pump switching frequency			400		kHz
LOGIC-LEVEL INPUTS (EN/IN1, PH/IN2, nSLEEP)						
V_{IL}	Input logic low voltage	V_{VM} < 5 V	0		0.7	V
		V_{VM} ≥ 5 V	0		0.8	
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input hysteresis			200		mV
		nSLEEP		50		mV
I_{IL}	Input logic low current	V_I = 0 V	–5		5	µA
I_{IH}	Input logic high current	V_I = 5 V		50	75	µA
R_{PD}	Input pulldown resistance	To GND		100		kΩ
TRI-LEVEL INPUTS (PMODE)						
V_{TIL}	Tri-level input logic low voltage		0		0.65	V
V_{TIZ}	Tri-level input Hi-Z voltage		0.9	1.1	1.2	V
V_{TIH}	Tri-level input logic high voltage		1.5		5.5	V
I_{TIL}	Tri-level input logic low current	V_I = 0 V	–50	–32		µA
I_{TIZ}	Tri-level input Hi-Z current	V_I = 1.1 V	–5		5	µA
I_{TIH}	Tri-level input logic high current	V_I = 5 V		113	150	µA
R_{TPD}	Tri-level pulldown resistance	To GND		44		kΩ
R_{TPU}	Tri-level pullup resistance	To internal 5 V		156		kΩ
QUAD-LEVEL INPUTS (IMODE)						
V_{QI2}	Quad-level input level 1	Voltage to set quad-level 1	0		0.45	V
R_{QI2}	Quad-level input level 2	Resistance to GND to set quad-level 2	18.6	20	21.4	kΩ
R_{QI3}	Quad-level input level 3	Resistance to GND to set quad-level 3	57.6	62	66.4	kΩ
V_{QI4}	Quad-level input level 4	Voltage to set quad-level 4	2.5		5.5	V
R_{QPD}	Quad-level pulldown resistance	To GND		136		kΩ
R_{QPU}	Quad-level pullup resistance	To internal 5 V		68		kΩ

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Electrical Characteristics (continued)

4.5 V ≤ V_{VM} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.3	V
I_{OZ}	Output logic high current	V_{OD} = 5 V	–2		2	µA
DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(on)_HS}$	High-side MOSFET on resistance	V_{VM} = 24 V, I_O = 1 A, T_J = 25°C		350	420	mΩ
$R_{DS(on)_LS}$	Low-side MOSFET on resistance	V_{VM} = 24 V, I_O = –1 A, T_J = 25°C		350	420	mΩ
V_{SD}	Body diode forward voltage	I_{SD} = 1 A		0.9		V
t_{RISE}	Output rise time	V_{VM} = 24 V, OUTx rising 10% to 90%		150		ns
t_{FALL}	Output fall time	V_{VM} = 24 V, OUTx falling 90% to 10%		150		ns
t_{PD}	Input to output propagation delay	EN/IN1, PH/IN2 to OUTx		650		ns
t_{DEAD}	Output dead time	Body diode conducting		300		ns
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	V_{VM} rising	4.3	4.45	4.6	V
		V_{VM} falling	4.2	4.35	4.5	V
V_{UVLO_HYS}	Supply UVLO hysteresis			100		mV
t_{UVLO}	Supply undervoltage deglitch time			10		µs
V_{CPUV}	Charge pump undervoltage lockout	VCP with respect to VM, V_{VCP} falling		2.25		V
I_{OCP}	Overcurrent protection trip point		3.5	5.5		A
t_{OCP}	Overcurrent protection deglitch time			3		µs
t_{RETRY}	Overcurrent protection retry time			2		ms
T_{TSD}	Thermal shutdown temperature		160	175	190	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C

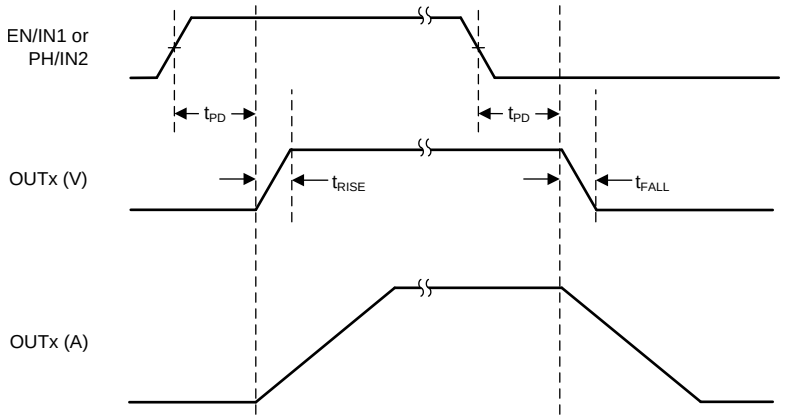


Figure 1. Timing Parameter Diagram

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6.6 Typical Characteristics

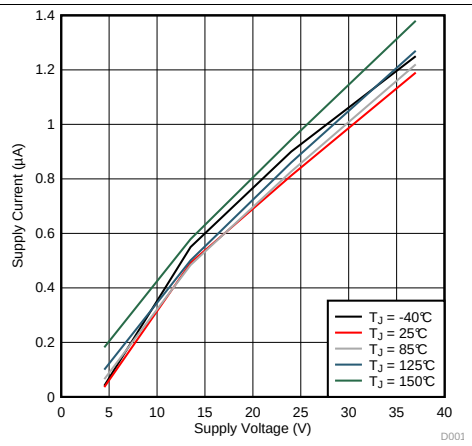


Figure 2. Sleep Current (I_{VMQ}) vs. Supply Voltage (V_{VM})

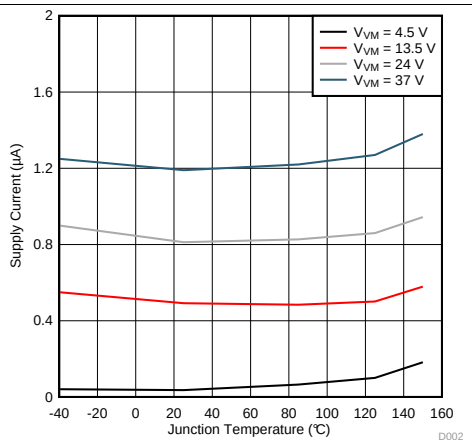


Figure 3. Sleep Current (I_{VMQ}) vs. Junction Temperature

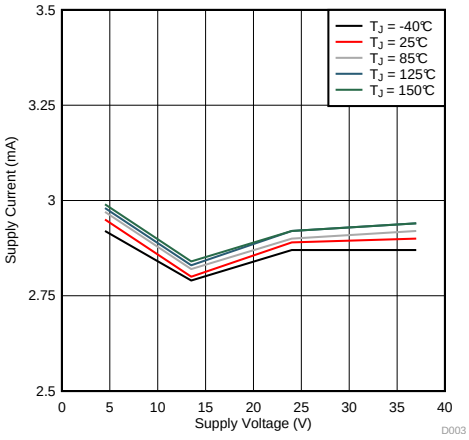


Figure 4. Active Current (I_{VM}) vs. Supply Voltage (V_{VM})

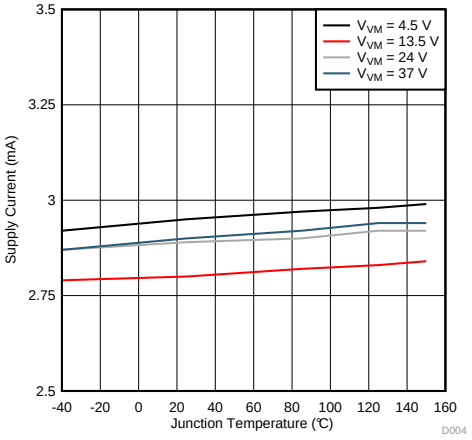


Figure 5. Active Current (I_{VM}) vs. Junction Temperature

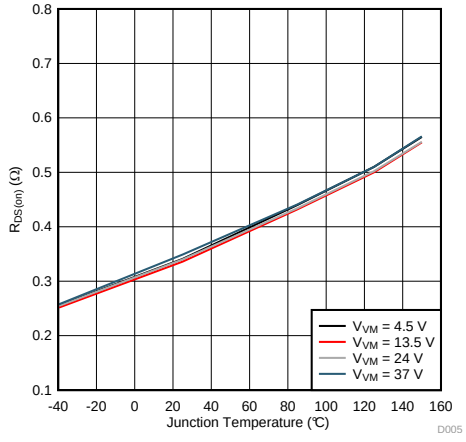


Figure 6. Low-Side $R_{DS(on)}$ vs. Junction Temperature

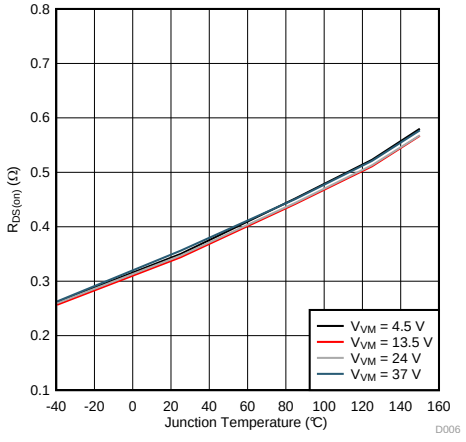


Figure 7. High-Side $R_{DS(on)}$ vs. Junction Temperature

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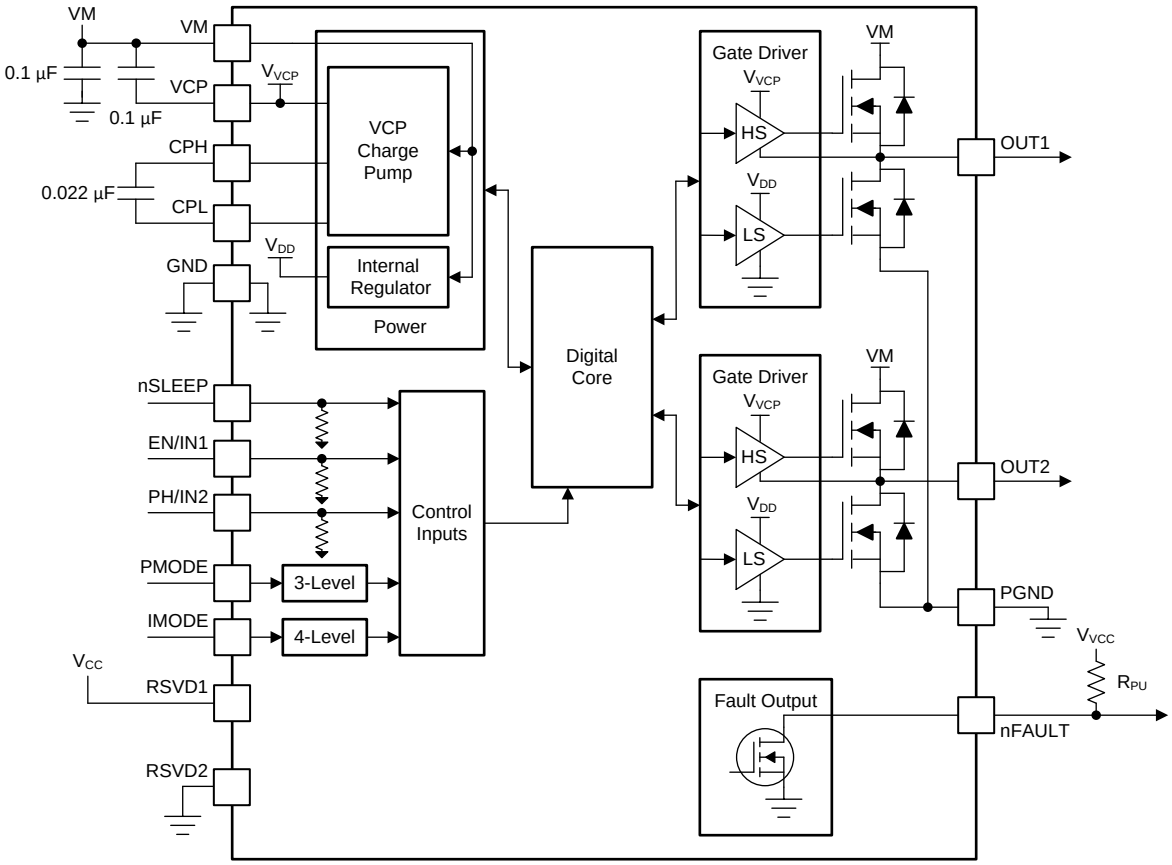
7 Detailed Description

7.1 Overview

The DRV887x family of devices are brushed DC motor drivers that operate from 4.5 to 37-V supporting a wide range of output load currents for various types of motors and loads. The devices integrate an H-bridge output power stage that can be operated in different control modes set be the PMODE pin setting. This allows for driving a single bidirectional brushed DC motor, two unidirectional brushed DC motors, or other output load configurations. The devices integrate a charge pump regulator to support more efficient high-side N-channel MOSFETs and 100% duty cycle operation. The devices operate from a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The nSLEEP pin provides an ultra-low power mode to minimize current draw during system inactivity.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 External Components

Table 1 lists the recommended external components for the device.

Table 1. Recommended External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF, low ESR ceramic capacitor, VM-rated.
C_{VM1}	VM	GND	Bulk Capacitance, VM-rated.
C_{VCP}	VCP	VM	X5R or X7R, 100-nF, 16-V ceramic capacitor
C_{FLY}	CPH	CPL	X5R or X7R, 22-nF, VM-rated ceramic capacitor
R_{IMODE}	IMODE	GND	See OUTx Overcurrent Protection (OCP).
R_{PMODE}	PMODE	GND	See Control Modes.
R_{nFAULT}	VCC	nFAULT	Pullup resistor, I_{OD} ≤ 5-mA

7.3.2 Control Modes

The DRV887x family of devices provide three modes to support different control schemes with the EN/IN1 and PH/IN2 pins. The control mode is selected through the PMODE pin with either logic low, logic high, or setting the pin Hi-Z as shown in Table 2. The PMODE pin state is latched when the device is enabled through the nSLEEP pin. The PMODE state can be changed by taking the nSLEEP pin logic low, waiting the t_{SLEEP} time, changing the PMODE pin input, and then enabling the device by taking the nSLEEP pin back logic high.

Table 2. PMODE Functions

PMODE STATE	CONTROL MODE
PMODE = Logic Low	PH/EN
PMODE = Logic High	PWM
PMODE = Hi-Z	Independent Half-Bridge

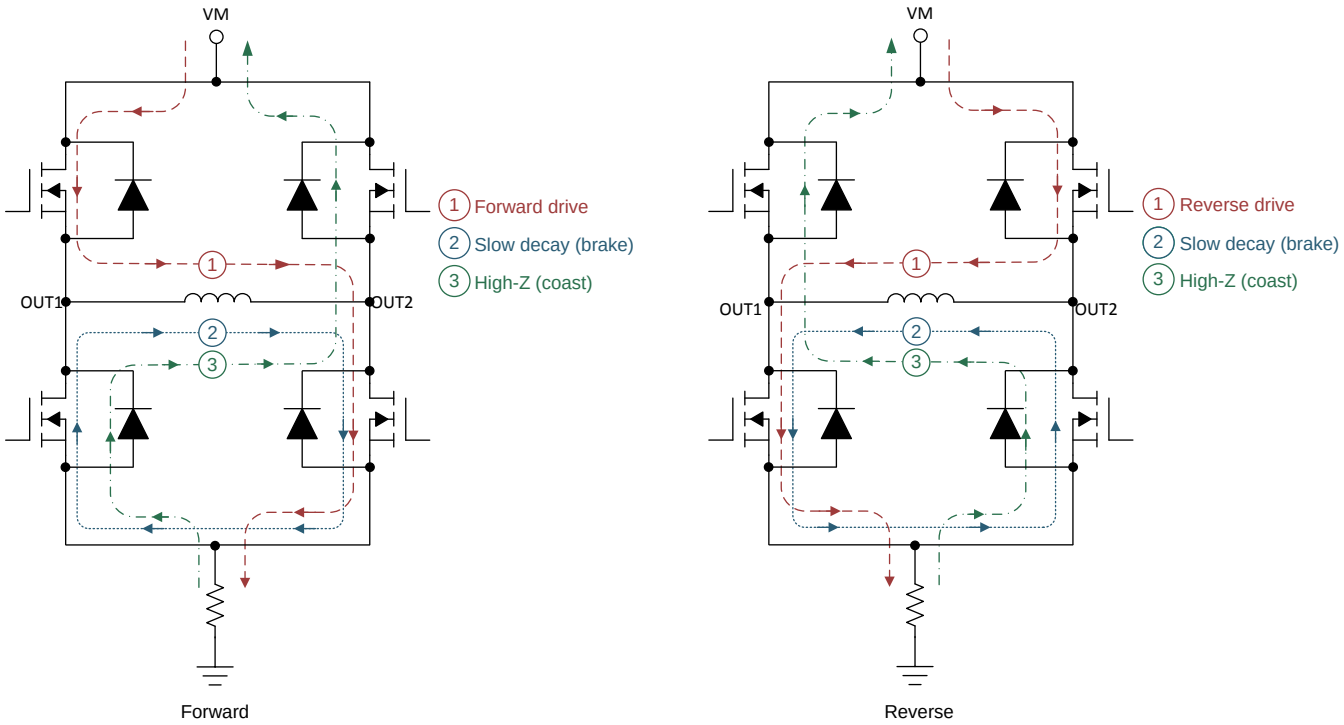


Figure 8. H-Bridge States

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied with no issues. By default, the EN/IN1 and PH/IN2 pins have an internal pulldown resistor to ensure the outputs are Hi-Z if no inputs are present.

The sections below show the truth table for each control mode. Additionally, the DRV887x family of devices automatically handles the dead-time generation when switching between the high-side and low-side MOSFET of a half-bridge.

Figure 8 describes the naming and configuration for the various H-bridge states.

7.3.2.1 PH/EN Control Mode (PMODE = Logic Low)

When the PMODE pin is logic low on power up, the device is latched into PH/EN mode. PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. The truth table for PH/EN mode is shown in Table 3.

Table 3. PH/EN Control Mode

nSLEEP	EN	PH	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep, (H-Bridge Hi-Z)
1	0	X	L	L	Brake, (Low-Side Slow Decay)
1	1	0	L	H	Reverse (OUT2 → OUT1)
1	1	1	H	L	Forward (OUT1 → OUT2)

7.3.2.2 PWM Control Mode (PMODE = Logic High)

When the PMODE pin is logic high on power up, the device is latched into PWM mode. PWM mode allows for the H-bridge to enter the Hi-Z state without taking the nSLEEP pin logic low. The truth table for PWM mode is shown in Table 4.

Table 4. PWM Control Mode

nSLEEP	IN1	IN2	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep, (H-Bridge Hi-Z)
1	0	0	Hi-Z	Hi-Z	Coast, (H-Bridge Hi-Z)
1	0	1	L	H	Reverse (OUT2 → OUT1)
1	1	0	H	L	Forward (OUT1 → OUT2)
1	1	1	L	L	Brake, (Low-Side Slow Decay)

7.3.2.3 Independent Half-Bridge Control Mode (PMODE = Hi-Z)

When the PMODE pin is Hi-Z on power up, the device is latched into independent half-bridge control mode. This mode allows for each half-bridge to be directly controlled in order to support high-side slow decay or driving two independent loads. The truth table for independent half-bridge mode is shown in Table 5.

Table 5. Independent Half-Bridge Control Mode

nSLEEP	INx	OUTx	DESCRIPTION
0	X	Hi-Z	Sleep, (H-Bridge Hi-Z)
1	0	L	OUTx Low-Side On
1	1	H	OUTx High-Side On

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7.3.3 Protection Circuits

The DRV887x family of devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.3.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the supply voltage on the VM pin falls below the undervoltage lockout threshold voltage (V_{UVLO}), all MOSFETs in the H-bridge will be disabled and the nFAULT pin driven low. The charge pump is disabled in this condition. Normal operation will resume when the undervoltage condition is removed and VM rises above the V_{UVLO} threshold.

7.3.3.2 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the charge pump voltage on the VCP pin falls below the undervoltage lockout threshold voltage (V_{CPUV}), all MOSFETs in the H-bridge will be disabled and the nFAULT pin driven low. Normal operation will resume when the undervoltage condition is removed and VCP rises above the V_{CPUV} threshold.

7.3.3.3 OUTx Overcurrent Protection (OCP)

An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events.

If the output current exceeds the overcurrent threshold, I_{OCP}, for longer than t_{OCP}, all MOSFETs in the H-bridge will be disabled and the nFAULT pin driven low. The overcurrent response can be configured through the IMODE pin as shown in Table 6.

Table 6. IMODE Functions

IMODE STATE	Overcurrent Response
R_{IMODE} = GND	Automatic Retry
R_{IMODE} = Hi-Z	Outputs Latched Off

In automatic retry mode, the MOSFETs will be disabled and nFAULT pin driven low for a duration of t_{RETRY}. After t_{RETRY}, the MOSFETs are re-enabled according to the state of the EN/IN1 and PH/IN2 pins. If the overcurrent condition is still present, the cycle repeats; otherwise normal device operation resumes.

In latched off mode, the MOSFETs will remain disabled and nFAULT pin driven low until the device is reset through either the nSLEEP pin or by removing the VM power supply.

In Independent Half-Bridge Control Mode (PMODE = Hi-Z), the OCP behavior is slightly modified. If an overcurrent event is detected, only the corresponding half-bridge will be disabled and the nFAULT pin driven low. The other half-bridge will continue normal operation. This allows for the device to manage independent fault events when driving independent loads. If an overcurrent event is detected in both half-bridges, both half-bridges will be disabled and the nFAULT pin driven low. In automatic retry mode, both half-bridges share the same overcurrent retry timer. If an overcurrent event occurs first in one half-bridge and then later in the secondary half-bridge, but before t_{RETRY} has expired, the retry timer for the first half-bridge will be reset to t_{RETRY} and both half-bridges will enable again after the retry timer expires.

7.3.3.4 Thermal Shutdown (TSD)

If the die temperature exceeds the overtemperature limit T_{TSD}, all MOSFET in the H-bridge will be disabled and the nFAULT pin driven low. Normal operation will resume when the overtemperature condition is removed and the die temperature drops below the T_{TSD} threshold.

7.3.3.5 Fault Condition Summary

Table 7. Fault Condition Summary

FAULT	CONDITION	REPORT	H-BRIDGE	RECOVERY
VM Undervoltage Lockout (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	VM > V_{UVLO}
VCP Undervoltage Lockout (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	VCP > V_{CPUV}

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Table 7. Fault Condition Summary (continued)

FAULT	CONDITION	REPORT	H-BRIDGE	RECOVERY
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	nFAULT	Disabled	t_{RETRY} or Reset (Set by IMODE)
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	nFAULT	Disabled	$T_J < T_{TSD} – T_{HYS}$

7.3.4 Pin Diagrams

7.3.4.1 Logic-Level Inputs

Figure 9 shows the input structure for the logic-level input pins EN/IN1, PH/IN2, and nSLEEP.

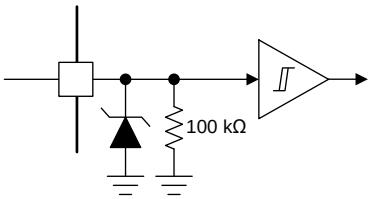


Figure 9. Logic-Level Input

7.3.4.2 Tri-Level Inputs

Figure 10 shows the input structure for the tri-level input pin PMODE.

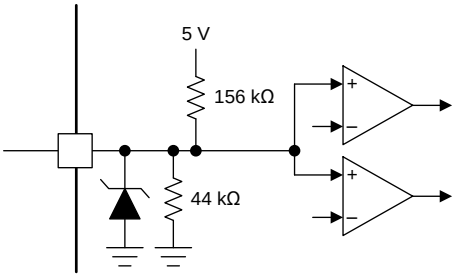


Figure 10. PMODE Tri-Level Input

7.3.4.3 Quad-Level Inputs

Figure 11 shows the input structure for the quad-level input pin IMODE. For DRV8876N, this pin should be connected to ground or left floating as described by Table 6.

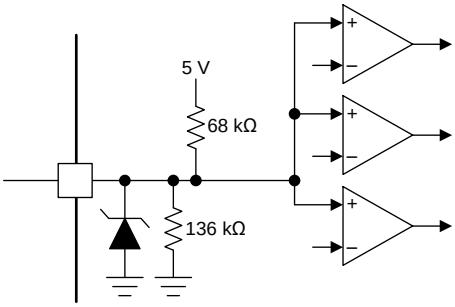


Figure 11. Quad-Level Input

7.4 Device Functional Modes

The DRV887x family of devices have several different modes of operation depending on the system inputs.

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Device Functional Modes (continued)

7.4.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the nSLEEP pin is logic high, and t_{WAKE} has elapsed, the device enters its active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs. The input control mode (PMODE) and OCP modes (IMODE) will be latched when the device enters active mode.

7.4.2 Low-Power Sleep Mode

The DRV887x family of devices support a low power mode to reduce current consumption from the VM pin when the driver is not active. This mode is entered by setting the nSLEEP pin logic low and waiting for t_{SLEEP} to elapse. In sleep mode, the H-bridge, charge pump, internal 5-V regulator, and internal logic are disabled. The device relies on a weak pulldown to ensure all of the internal MOSFETs remain disabled. The device will not respond to any inputs besides nSLEEP while in low-power sleep mode.

7.4.3 Fault Mode

The DRV887x family of devices enter a fault mode when a fault is encountered. This is utilized to protect the device and the output load. The device behavior in the fault mode is described in Table 7 and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV887x family of devices can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, and actuators. The device can also be utilized to drive many common passive loads such as LEDs, resistive elements, relays, etc. The application examples below will highlight how to use the device in bidirectional current control applications requiring an H-bridge driver and dual unidirectional current control applications requiring two half-bridge drivers.

8.2 Typical Application

8.2.1 Primary Application

In the primary application example, the device is configured to drive a bidirectional current through an external load (such as a brushed DC motor) using an H-bridge configuration. The H-bridge polarity and duty cycle are controlled with a PWM and IO resource from the external controller to the EN/IN1 and PH/IN2 pins. The device is configured for the PH/EN control mode by tying the PMODE pin to GND.

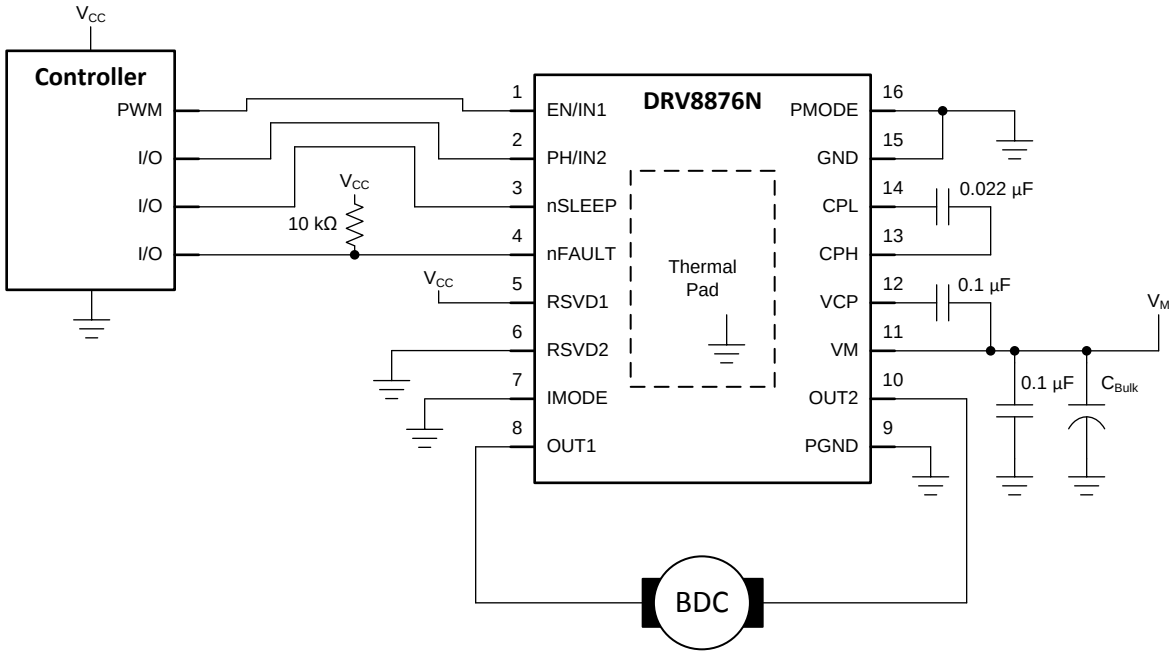


Figure 12. Typical Application Schematic

8.2.1.1 Design Requirements

Table 8. Design Parameters

REFERENCE	DESIGN PARAMETER	EXAMPLE VALUE
V_M	Motor and driver supply voltage	24 V
V_{CC}	Controller supply voltage	3.3 V
I_{RMS}	Output RMS current	0.5 A

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Typical Application (continued)

Table 8. Design Parameters (continued)

REFERENCE	DESIGN PARAMETER	EXAMPLE VALUE
f_{PWM}	Switching frequency	20 kHz
T_A	PCB ambient temperature	–20 to 85 °C
T_J	Device max junction temperature	150 °C
$R_{\theta JA}$	Device junction to ambient thermal resistance	35 °C/W

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Power Dissipation and Output Current Capability

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation for the device is composed of three main components. These are the quiescent supply current dissipation, the power MOSFET switching losses. and the power MOSFET $R_{DS(on)}$ (conduction) losses. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (1)$$

P_{VM} can be calculated from the nominal supply voltage (V_M) and the I_{VM} active mode current specification.

$$P_{VM} = V_M \times I_{VM} \quad (2)$$

$$P_{VM} = 0.096\ W = 24\ V \times 4\ mA \quad (3)$$

P_{SW} can be calculated from the nominal supply voltage (V_M), average output current (I_{RMS}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} \quad (4)$$

$$P_{SW_RISE} = 0.5 \times V_M \times I_{RMS} \times t_{RISE} \times f_{PWM} \quad (5)$$

$$P_{SW_FALL} = 0.5 \times V_M \times I_{RMS} \times t_{FALL} \times f_{PWM} \quad (6)$$

$$P_{SW_RISE} = 0.018\ W = 0.5 \times 24\ V \times 0.5\ A \times 150\ ns \times 20\ kHz \quad (7)$$

$$P_{SW_FALL} = 0.018\ W = 0.5 \times 24\ V \times 0.5\ A \times 150\ ns \times 20\ kHz \quad (8)$$

$$P_{SW} = 0.036\ W = 0.018\ W + 0.018\ W \quad (9)$$

P_{RDS} can be calculated from the device $R_{DS(on)}$ and average output current (I_{RMS})

$$P_{RDS} = I_{RMS}^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (10)$$

It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(on)}$ with temperature can be found in the Typical Characteristics curves. Assuming a device temperature of 85 °C it can be expected that $R_{DS(on)}$ will see an increases of ~1.25 based on the normalized temperature data.

$$P_{RDS} = 0.219\ W = 0.5\ A^2 \times (350\ m\Omega \times 1.25 + 350\ m\Omega \times 1.25) \quad (11)$$

By adding together the different power dissipation components it can be verified that the expected power dissipation and device junction temperature is within design targets.

$$P_{TOT} = P_{VM} + P_{SW} + P_{RDS} \quad (12)$$

$$P_{TOT} = 0.351\ W = 0.096\ W + 0.036\ W + 0.219\ W \quad (13)$$

The device junction temperature can be calculated with the P_{TOT}, device ambient temperature (T_A), and package thermal resistance ($R_{\theta JA}$). The value for $R_{\theta JA}$ is heavily dependent on the PCB design and copper heat sinking around the device.

$$T_J = (P_{TOT} \times R_{\theta JA}) + T_A \quad (14)$$

$$T_J = 97°C = (0.351\ W \times 35\ °C/W) + 85°C \quad (15)$$

It should be ensured that the device junction temperature is within the specified operating region. Other methods exist for verifying the device junction temperature depending on the measurements available.

Additional information on motor driver current ratings and power dissipation can be found in Thermal Performance and Related Documentation.

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8.2.1.2.2 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria:

- 2-layer PCB, standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness.
  - Top layer: HTSSOP package footprint and copper plane heatsink.
  - Bottom layer: signal layer with small copper pad underneath and thermally connected through vias. Bottom layer thermal pad is the same size as the package (5 mm x 4.4 mm). Bottom pad size remains constant as top copper plane is varied. Thermal vias are only present under the thermal pad (grid pattern with 1.2mm spacing).
- 4-layer PCB, standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness.
  - Top layer: HTSSOP package footprint and copper plane heatsink. Inner planes were kept at 1-oz.
  - Mid layer 1: GND plane thermally connected to pad through vias.
  - Mid layer 2: power plane, no thermal connection.
  - Bottom layer: signal layer with small copper pad underneath and thermally connected through via stitching from the TOP and internal GND planes. Bottom layer thermal pad is the same size as the package (5 mm x 4.4 mm). Bottom pad size remains constant as top copper plane is varied. Thermal vias are only present under the thermal pad (grid pattern with 1.2mm spacing).

Figure 13 shows an example of the simulated board. Table 9 shows the dimensions of the board that were varied for each simulation.

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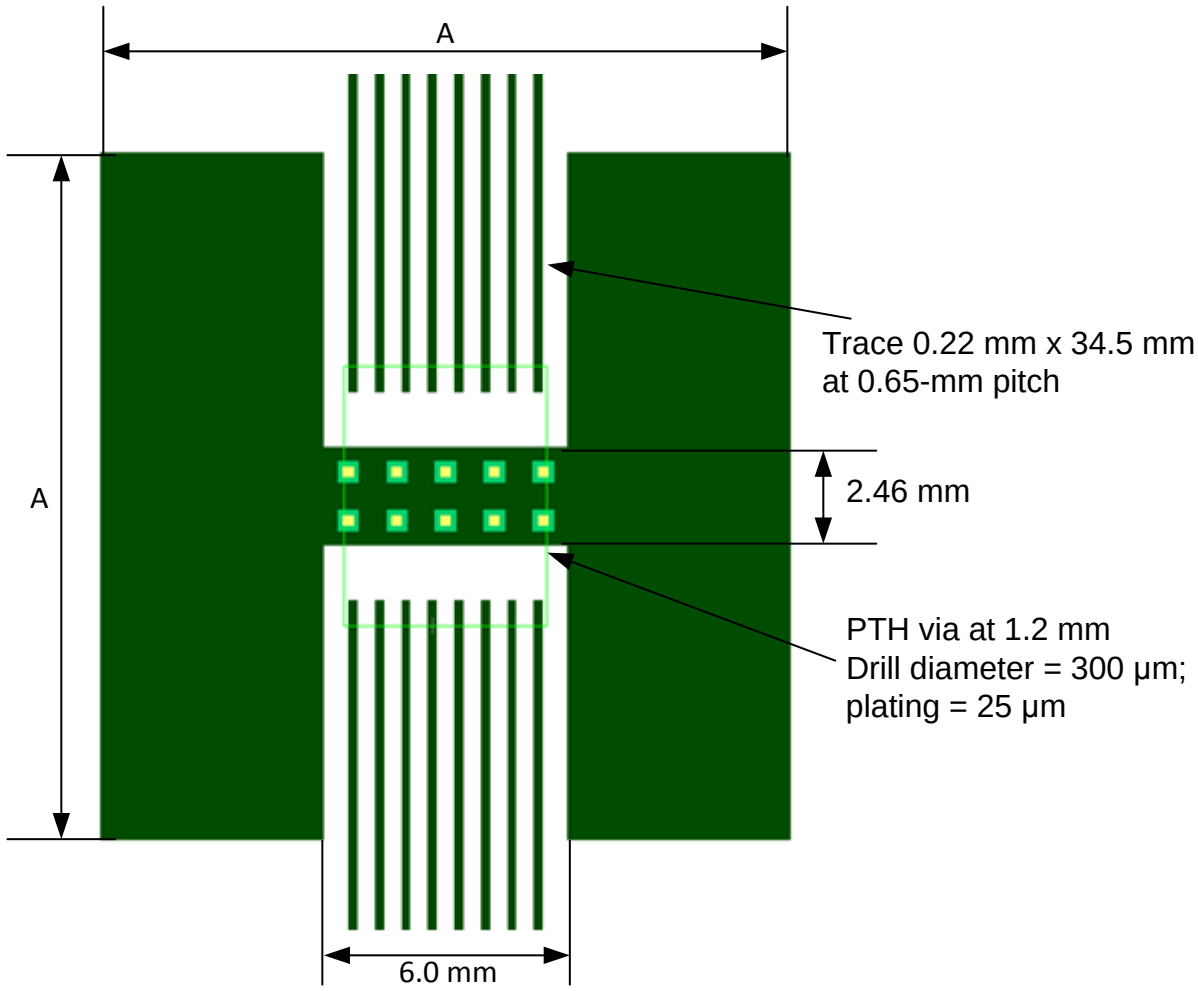


Figure 13. PCB model (4-layer PCB shown, 2-layer PCB has no vias)

Table 9. Dimension A for 16-pin PWP package

Cu area (mm^2)	Dimension A
2	17.0
4	22.8
8	31.0
16	42.8
32	59.5
48	72.2

8.2.1.2.2.1 Steady-State Thermal Performance

"Steady-state conditions" assume that the motor driver operates with a constant RMS current over a long period of time. Figure 14, Figure 15, Figure 16, and Figure 17 show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

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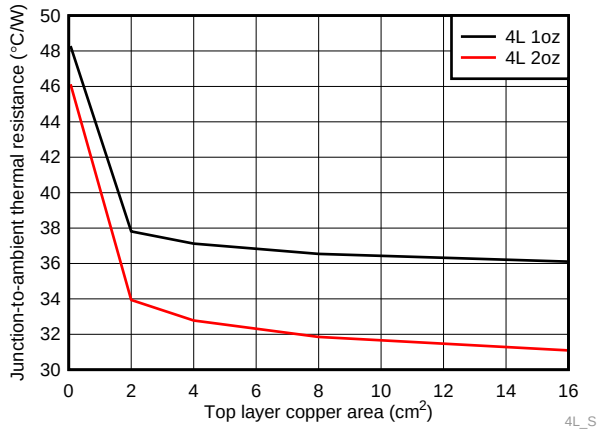


Figure 14. HTSSOP, 4-layer PCB junction-to-ambient thermal resistance vs copper area

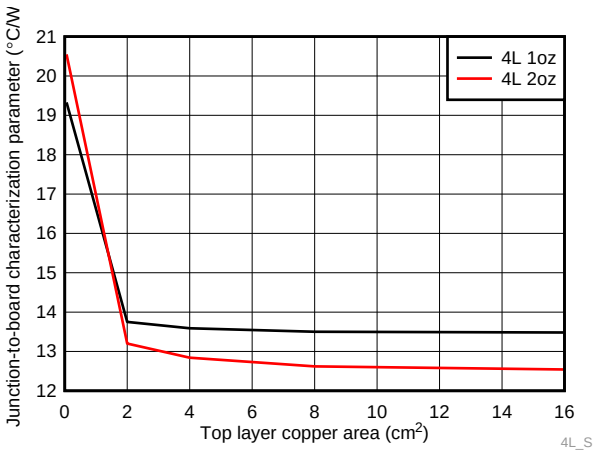


Figure 15. HTSSOP, 4-layer PCB junction-to-board characterization parameter vs copper area

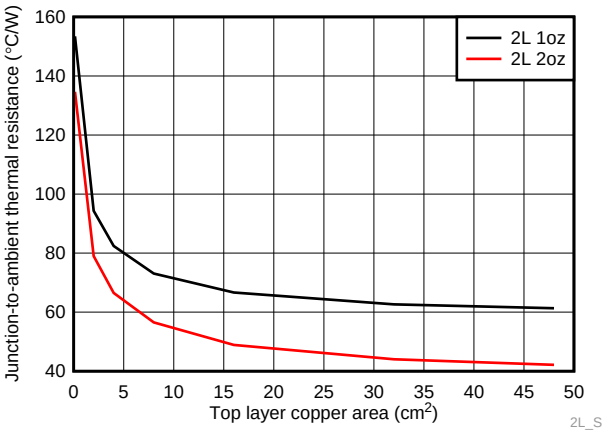


Figure 16. HTSSOP, 2-layer PCB junction-to-ambient thermal resistance vs copper area

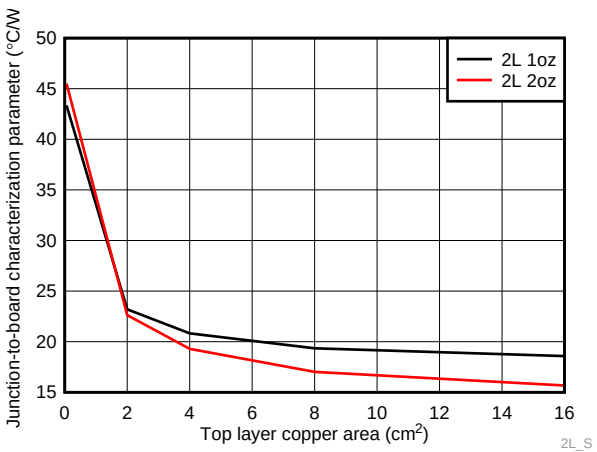


Figure 17. HTSSOP, 2-layer PCB junction-to-board characterization parameter vs copper area

8.2.1.2.2.2 Transient Thermal Performance

The motor drive device may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include

- Motor start-up when the rotor is not yet spinning at full speed.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the device goes into and out of overcurrent protection.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance. In transient cases, thermal impedance ($Z_{\theta JA}$) denotes the junction-to-ambient thermal performance. and show the simulated thermal impedances for 1-oz and 2-oz copper layouts. In these graphs, the solid lines indicate the 2-layer board, and the dashed lines indicate the 4-layer board. These graphs indicate better thermal performance with short current pulses. For short periods of time, the device package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and again depending on copper area as the duration of the drive pulse increases. Very long pulses can be considered steady-state performance.

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8.2.1.3 Application Curves

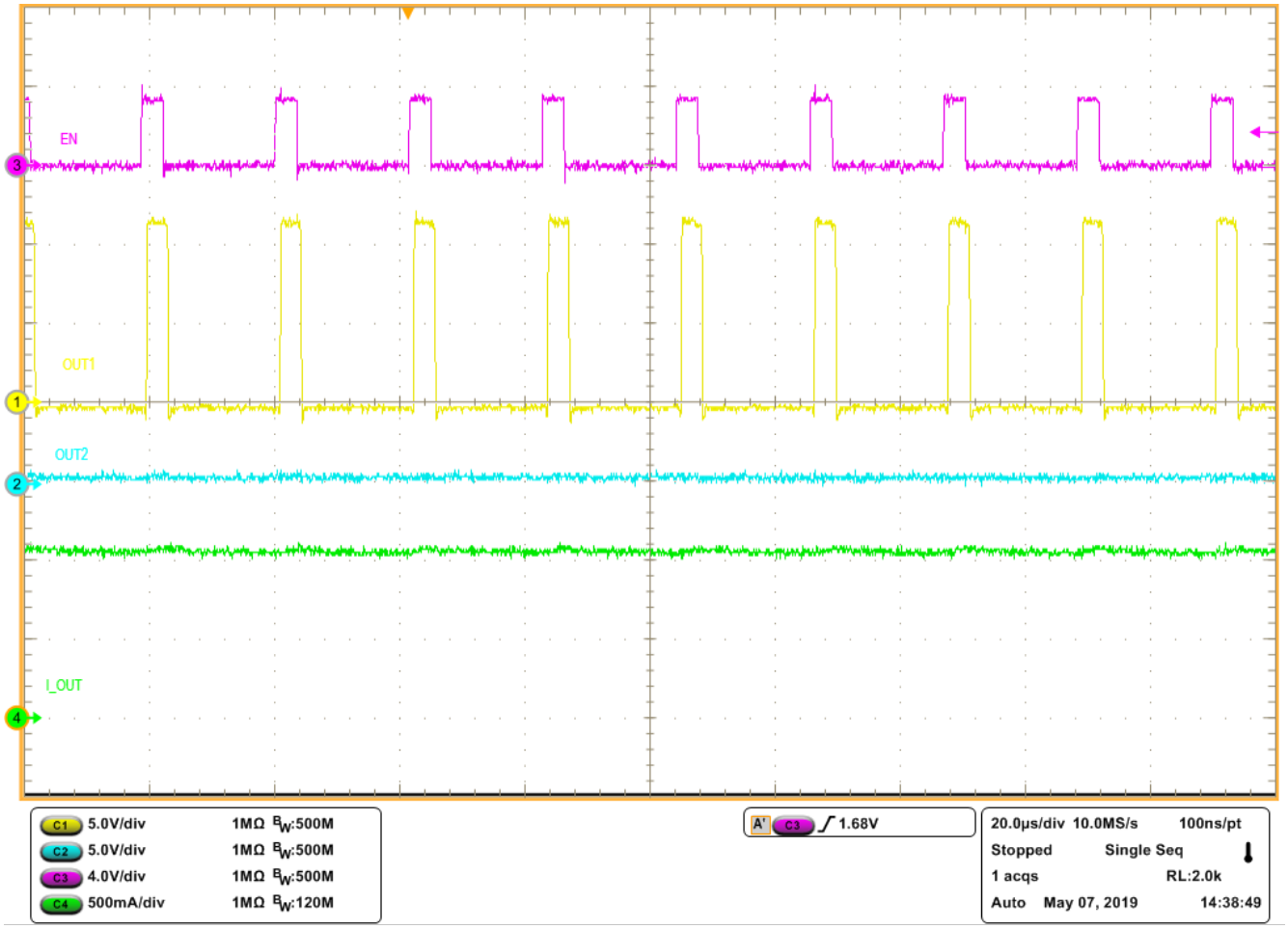


Figure 18. Driver PWM Operation (PH/EN)

8.2.2 Alternative Application

In the alternative application example, the device is configured to drive a unidirectional current through two external loads (such as two brushed DC motors) using a dual half-bridge configuration. The duty cycle of each half-bridge is controlled with a PWM resource from the external controller to the EN/IN1 and PH/IN2 pins. The device is configured for the independent half-bridge control mode by leaving the PMODE pin floating.

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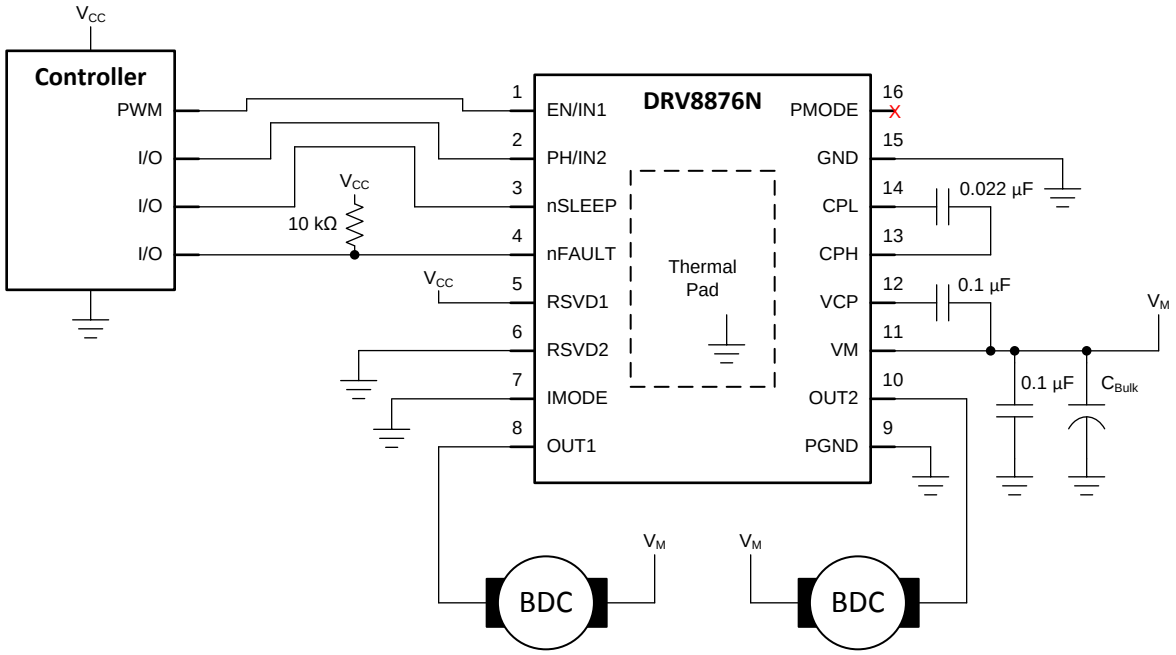


Figure 19. Typical Application Schematic

8.2.2.1 Design Requirements

Table 10. Design Parameters

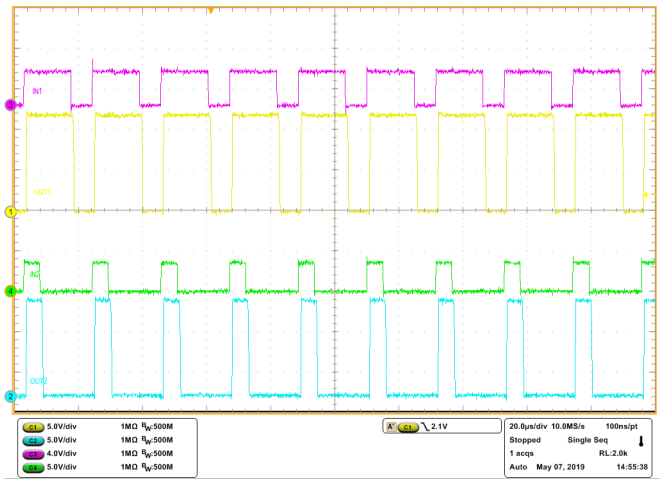
REFERENCE	DESIGN PARAMETER	EXAMPLE VALUE
V_M	Motor and driver supply voltage	24 V
V_{CC}	Controller supply voltage	3.3 V
I_{RMS1}	Output 1 RMS current	0.5 A
I_{PEAK1}	Output 1 peak current	1 A
I_{RMS2}	Output 2 RMS current	0.25 A
I_{PEAK2}	Output 2 peak current	0.5 A
f_{PWM}	Switching frequency	20 kHz
T_A	PCB ambient temperature	–20 to 85 °C
T_J	Device max junction temperature	150 °C
$R_{\theta JA}$	Device junction to ambient thermal resistance	35 °C/W

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8.2.2.2 Detailed Design Procedure

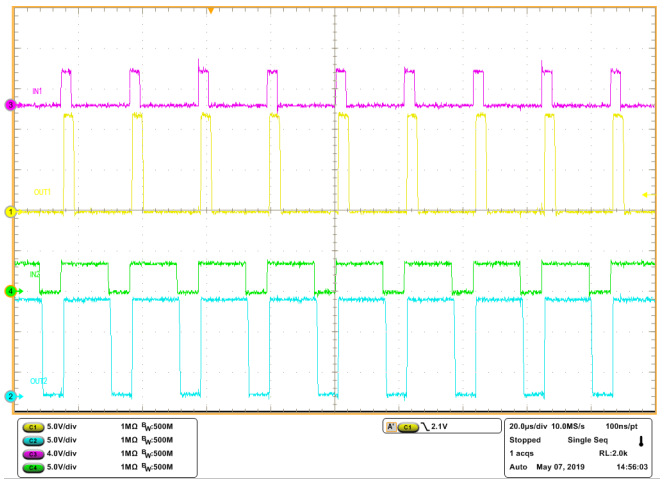
Refer to the Primary Application Detailed Design Procedure section for a detailed design procedure example. The majority of the design concepts apply to the alternative application example.

8.2.2.3 Application Curves



Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan. 4 = PH/IN2

Figure 20. Independent Half-Bridge PWM Operation



Chan. 1 = OUT1 Chan. 2 = OUT2 Chan. 3 = EN/IN1
Chan. 4 = PH/IN2

Figure 21. Independent Half-Bridge PWM Operation

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9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local bulk capacitance needed depends on a variety of factors, including:

- The highest current required by the motor or load
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple of the system
- The motor braking method (if applicable)

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended minimum value, but system level testing is required to determine the appropriately sized bulk capacitor.

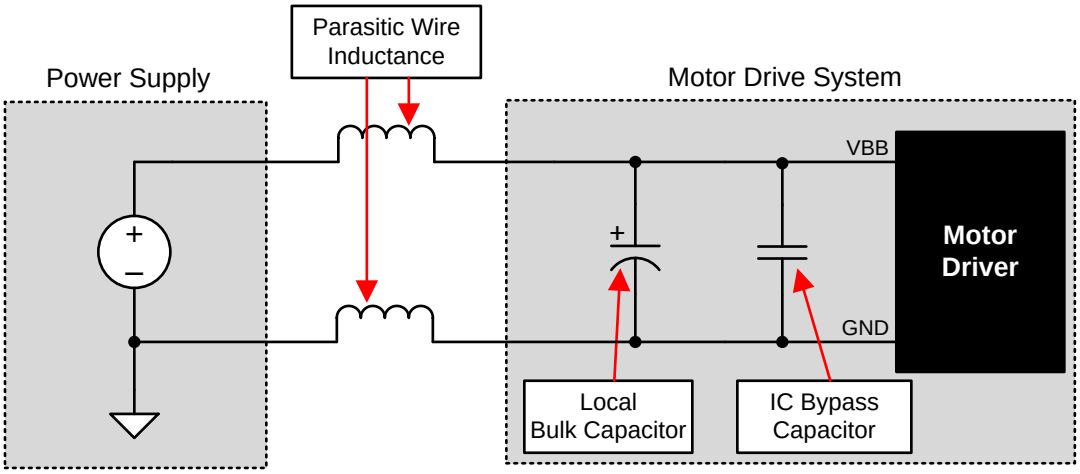


Figure 22. System Supply Parasitics Example

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10 Layout

10.1 Layout Guidelines

Since the DRV887x family of devices are integrated power MOSFETs device capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below.

- Low ESR ceramic capacitors should be utilized for the VM to GND bypass capacitor, the VCP to VM charge pump storage capacitor, and the charge pump flying capacitor. X5R and X7R types are recommended.
- The VM power supply and VCP, CPH, CPL charge pump capacitors should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and PGND carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- PGND and GND should connect together directly on the PCB ground plane. They are not intended to be isolated from each other.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- A recommended land pattern for the thermal vias is provided in the package drawing section.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

10.2 Layout Example

10.2.1 HTSSOP Layout Example

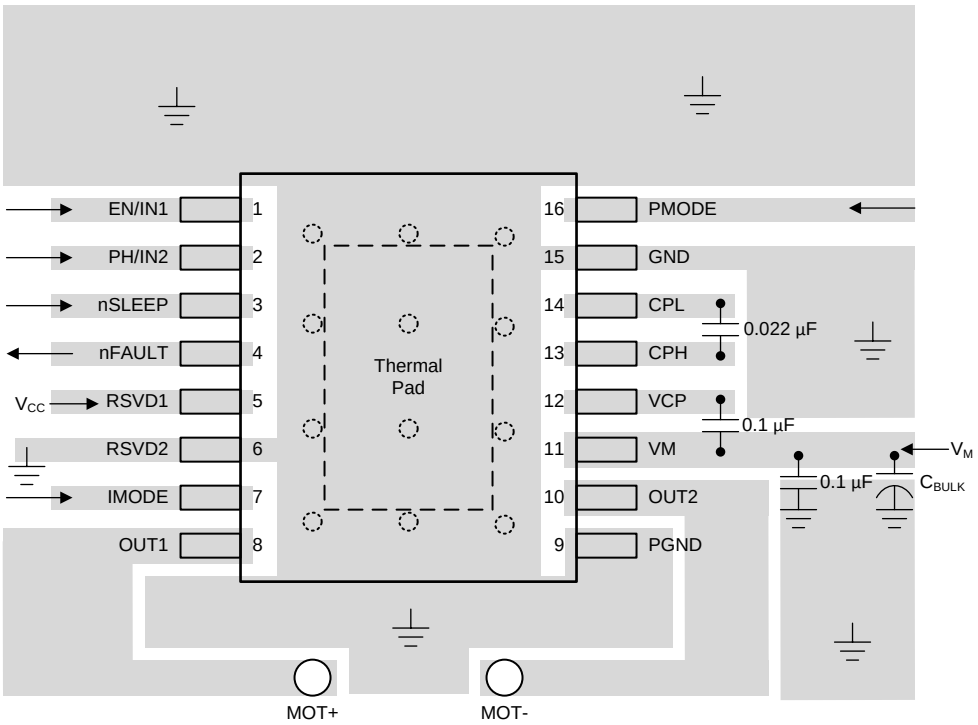


Figure 23. HTSSOP (PWP) Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8876NPWPR	ACTIVE	HTSSOP	PWP	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	8876N	Samples
DRV8876NPWPT	ACTIVE	HTSSOP	PWP	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	8876N	Samples
DRV8876NRGTR	PREVIEW	VQFN	RGT	16	3000	TBD	Call TI	Call TI	-40 to 125		
DRV8876NRGTT	PREVIEW	VQFN	RGT	16	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

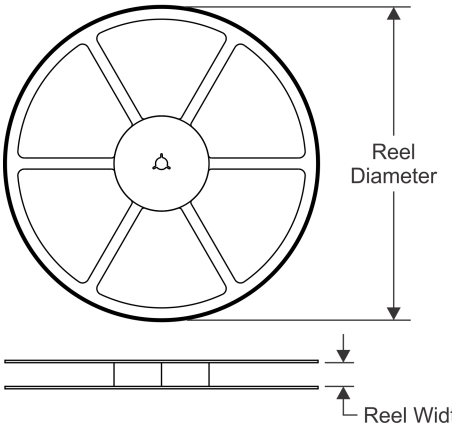
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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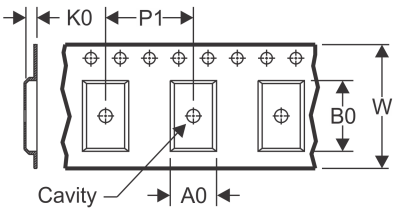
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

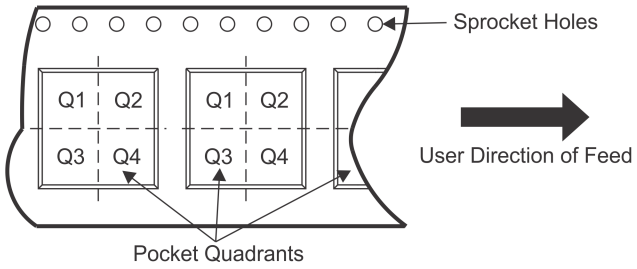


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

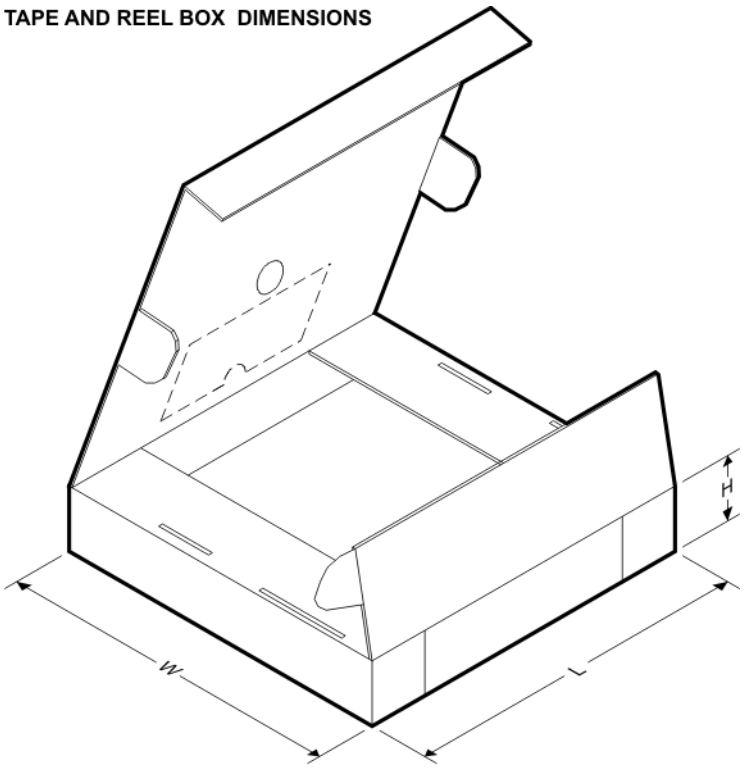
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8876NPWPR	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8876NPWPT	HTSSOP	PWP	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

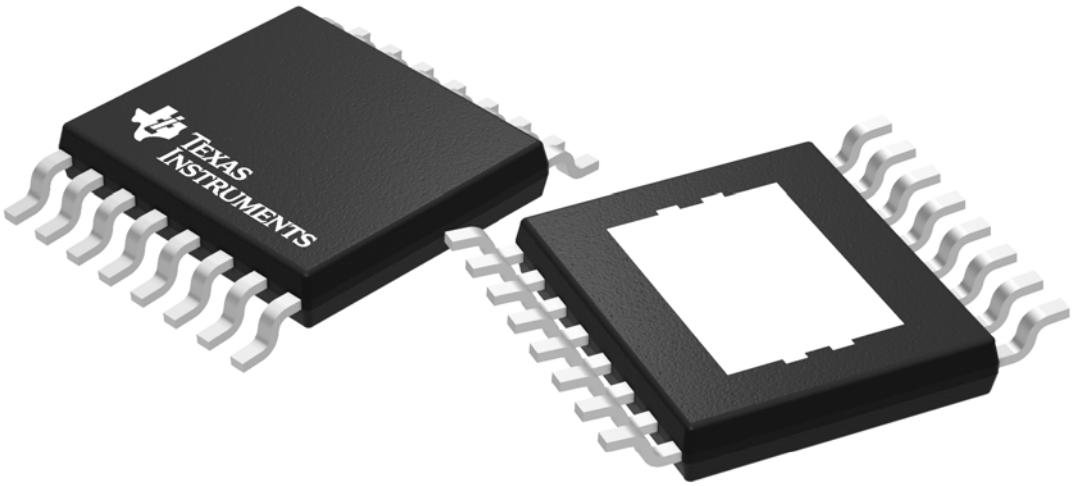


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8876NPWPR	HTSSOP	PWP	16	3000	350.0	350.0	43.0
DRV8876NPWPT	HTSSOP	PWP	16	250	210.0	185.0	35.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

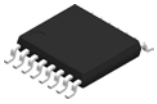
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

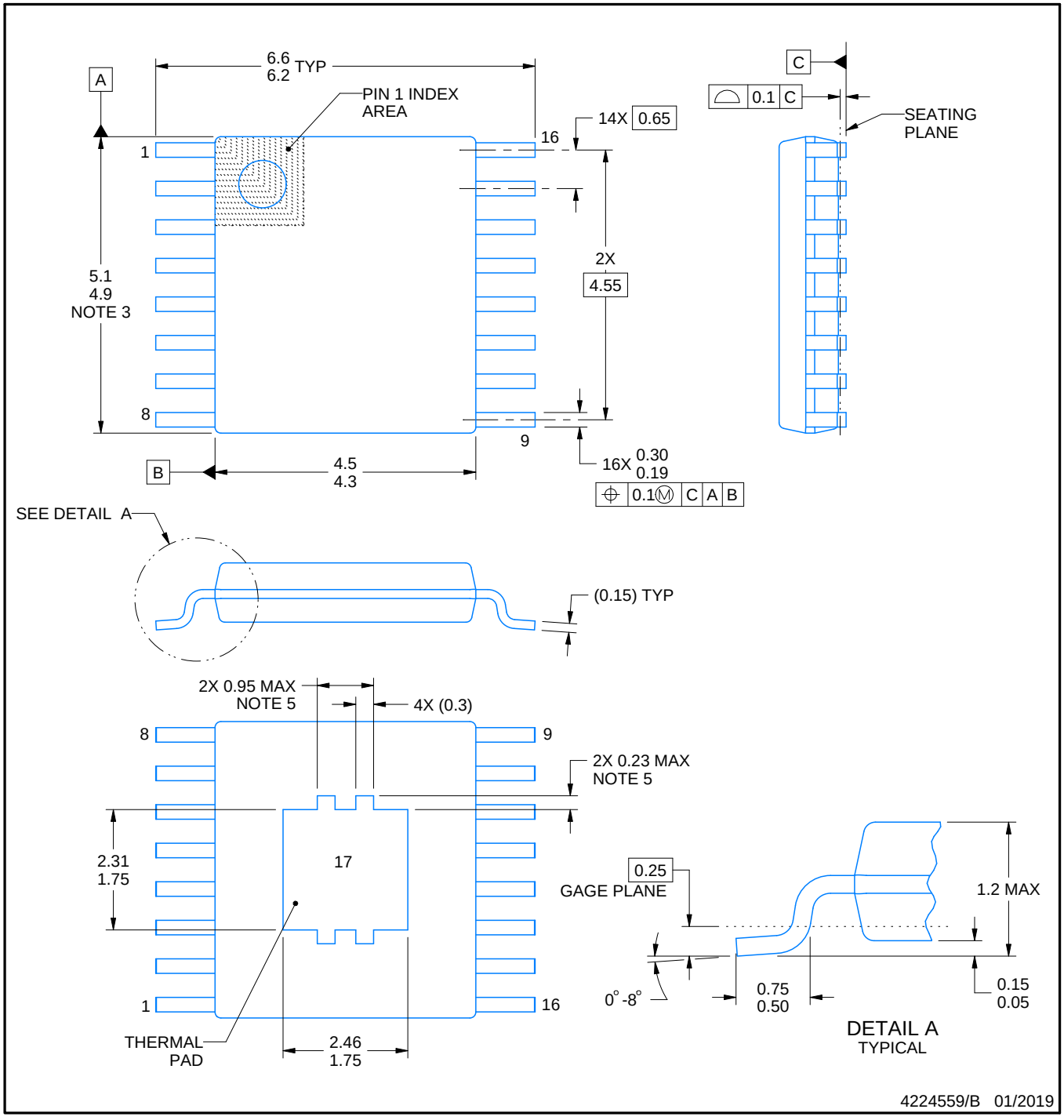
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

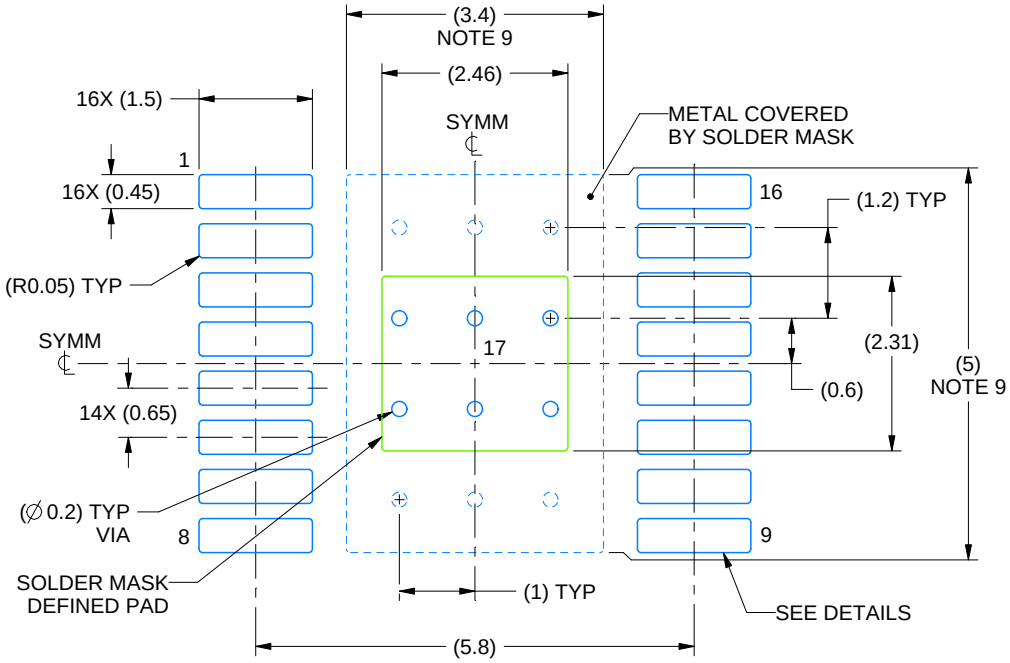
SMALL OUTLINE PACKAGE



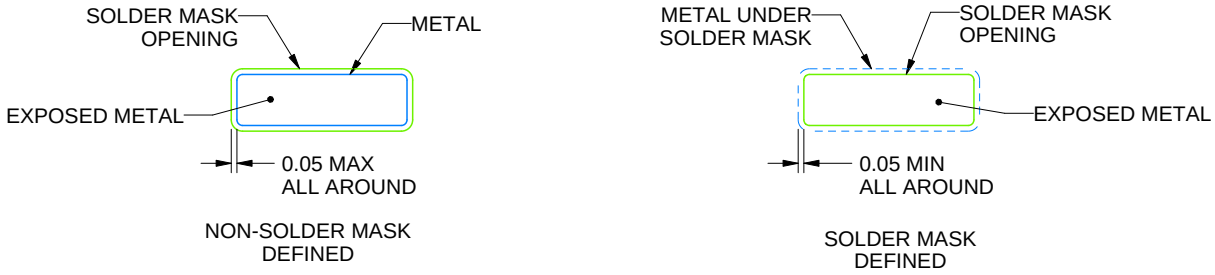
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

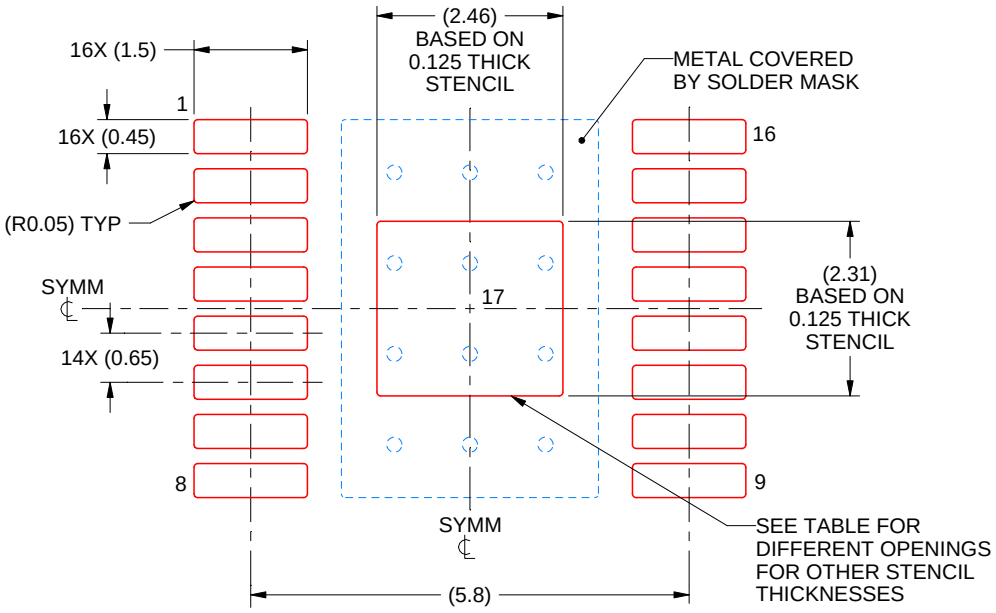


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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