TMP821 Two-Phase Half-Wave Motor Predriver

1 Features

- Built-In Lock Detection and Rotational Speed Sensing Mechanisms
- Compact 8-Pin Package Reduces Number of External Components Required
- Automatic Restart When Motor Lock Is Undone
- Hall Amplifier Inputs Have Hysteresis

2 Applications

Small Server Fans

3 Description

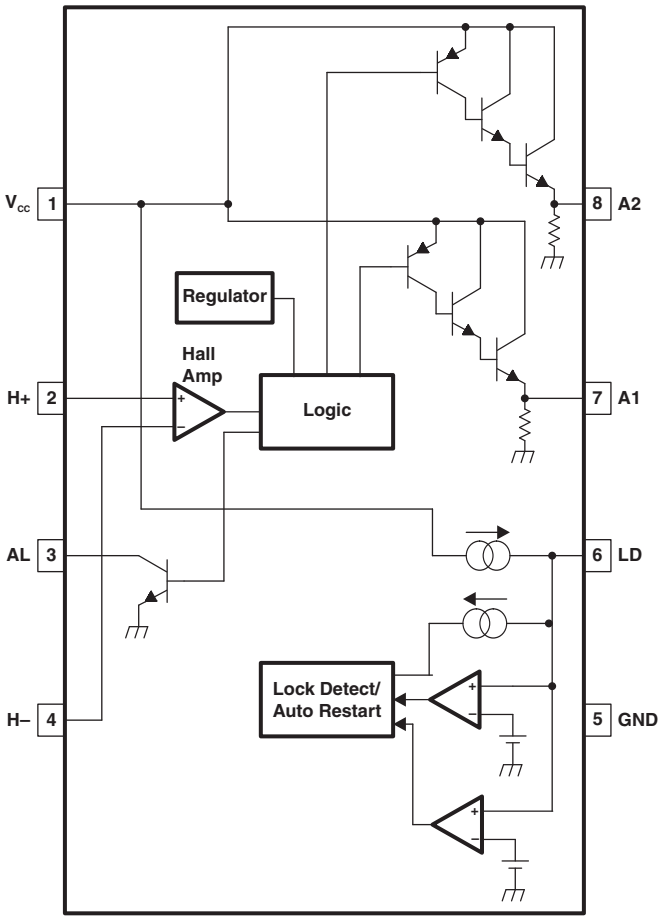
The TMP821 device is a two-phase half-wave motor predriver that is suited for fan motors, which has winding in push-pull configuration. It uses differential hall effect sensors for commutation signals for two of the switches in power circuit. The device has a very small pin count, making it very simple to use.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP821	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

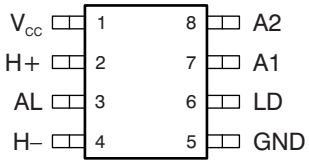
Changes from Original (January 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	7	O	Driver output
A2	8	O	Driver output
AL	3	O	Speed indication
GND	5	Power GND	Ground
H+	2	I	Positive Hall input
H–	4	I	Negative Hall input
LD	6	I	Timing capacitor
VCC	1	Power Supply	Power input (4 V to 28 V)

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		30	V
V_{AL}	Output voltage (AL)		30	V
I_{OUT}	Continuous output current (A1, A2)		70	mA
I_{AL}	Continuous output current (AL)		8	mA
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	28	V
V_H	Hall amplifier input voltage	1	V_{CC} – 0.5	V
T_A	Operating free-air temperature	–40	100	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP821 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	97	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	58.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	57.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Package thermal impedance is calculated in accordance with JESD 51-7.

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6.5 Electrical Characteristics

V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Hall amplifier input voltage hysteresis			±3		±15	mV
V_{AL}	Lock alarm signal low-level output voltage	AL	I_{AL} = 5 mA			0.5	V
I_{AL}	Lock alarm signal low-level output current	AL	V_{AL} = 2 V	8			mA
I_{LDC}	Lock Detection capacitor charge current	LD	V_{LD} = 1.5 V	2	3.45	5.25	µA
I_{LDD}	Lock Detection capacitor discharge current	LD	V_{LD} = 1.5 V	0.35	0.8	1.45	µA
r_{CD}	Lock Detection capacitor charge and discharge current ratio	LD	$r_{CD} = I_{LDC}/I_{LDD}$	3	4.5	8	
V_{LDCL}	Lock Detection capacitor clamp voltage	LD		2.2	2.6	3	V
V_{LDCP}	Lock Detection capacitor comparator voltage	LD		0.4	0.6	0.8	V
V_{7H}	High-level output voltage	A1	I_{OH} = –10 mA	10	10.5		V
V_{8H}	High-level output voltage	A2	I_{OH} = –10 mA	10	10.5		V
I_{CC}	Supply current		Output off		3.2	5	mA

6.6 Typical Characteristics

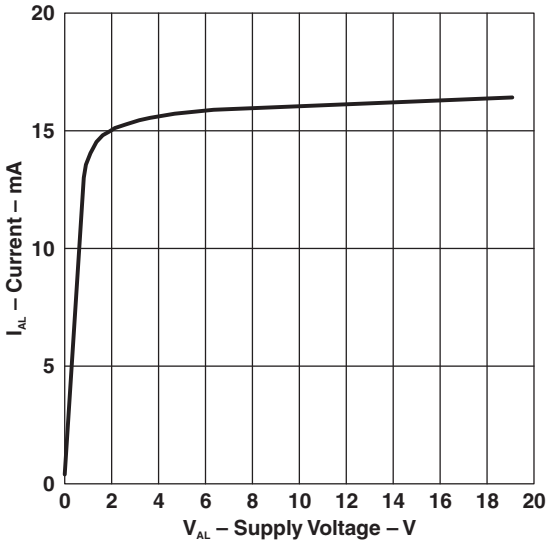


Figure 1. AL Current Consumption vs AL Supply Voltage (V_{CC} = 12 V)

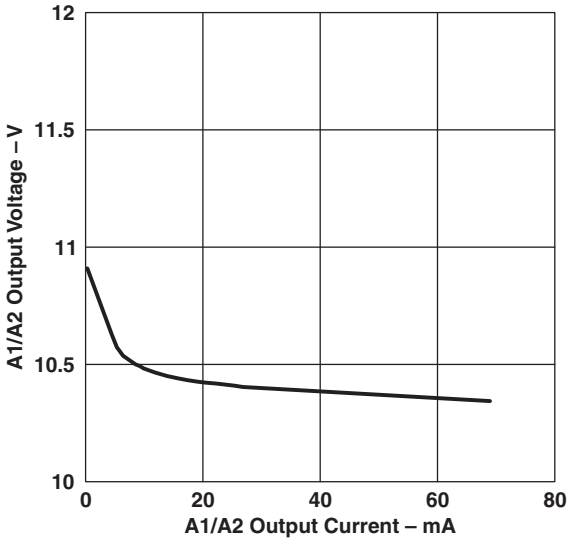


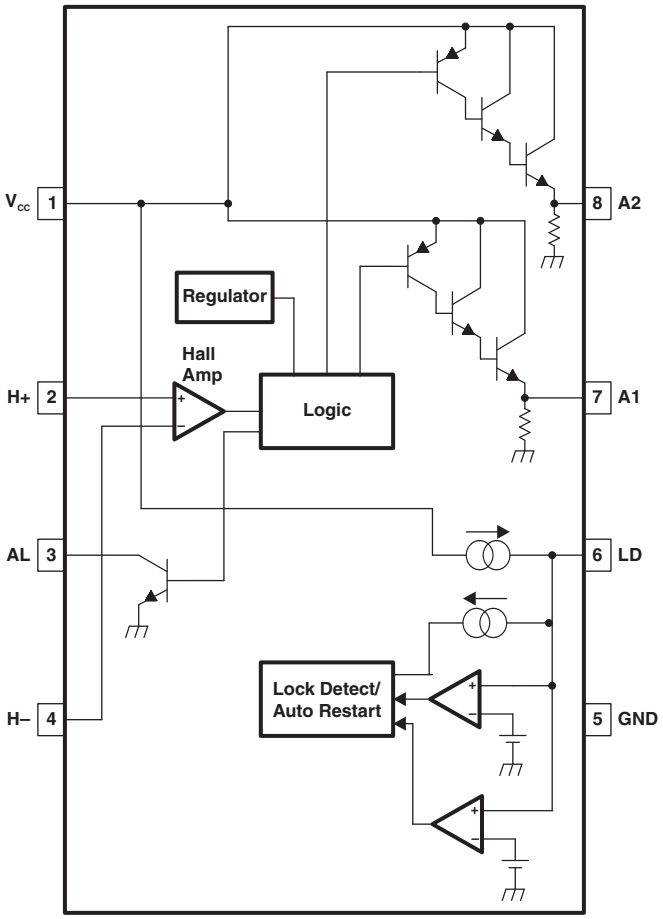
Figure 2. A1/A2 Output Voltage vs A1/A2 Output Current

7 Detailed Description

7.1 Overview

The TMP821 device is a two phase half wave motor predriver suited for small fan applications. The two switches are controlled from the logic generated from differential hall sensors connected to the device. The drive logic operates in push-pull configuration. The TMP821 device is a very small package with minimum external components required, making the design very simple and easy. Speed information is available on a pin. The lock detect feature is also part of the features provided by the device whose timing is configured by connecting an external capacitor.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Lock Detection

The TMP821 device comes with the built-in lock detect feature. If it's not able to rotate the rotor for a specific amount of time, the Lock Detection disables the drive and retries after some time. The timings are dependant on the capacitor connected at LD Pin.

When a motor lock is detected, the TMP821 device automatically shuts down its output current. When the motor lock is removed, the TMP821 device automatically restarts. Motor lock is detected when the Hall signal stops switching, as shown in Figure 3.

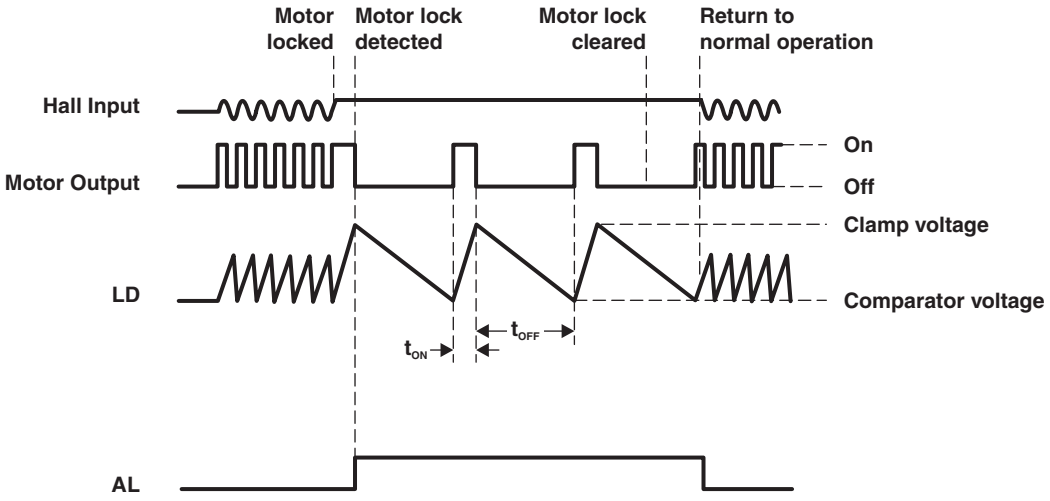


Figure 3. Motor Lock Diagram

t_{ON} and t_{OFF} are determined by the capacitor connected to LD:

$$t_{ON} = (C_{LD} \times (V_{LD_CLAMP} - V_{LD_COMP}) / I_{LD_CHARGE} \text{ (seconds)} \quad (1)$$

$$t_{OFF} = (C_{LD} \times (V_{LD_CLAMP} - V_{LD_COMP}) / I_{LD_DISCHARGE} \text{ (seconds)}$$

where

- C_{LD} = capacitance of the external capacitor on LD
- V_{LD_CLAMP} = LD clamp voltage
- V_{LD_COMP} = LD comparator voltage
- I_{LD_CHARGE} = LD charge current
- $I_{LD_DISCHARGE}$ = LD discharge current (2)

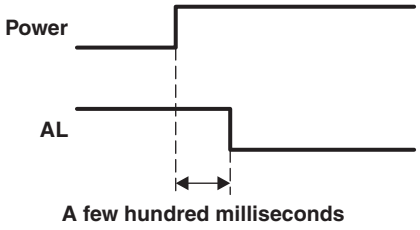


Figure 4. Power-on to AL Delay

7.3.2 Speed Sensing

The TMP821 device gives the speed information on the pin AL. This pin may remain high for few hundred milliseconds at the start-up. Once the motor attains some speed, the frequency can be observed at this pin.

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Feature Description (continued)

NOTE

After power is supplied to the device, the Lock Detection pin (AL) may remain high for a few hundred milliseconds (see Figure 4).

7.4 Device Functional Modes

7.4.1 Lock Detection Pin

When rotor is locked, the drive is enabled until the voltage at LD pin reaches a higher threshold. Once the voltage reaches a higher threshold, the drive is disabled until the LD capacitor discharges to a lower threshold.

7.4.2 Run

If the motor is unlocked and hall sensor inputs and drive signals are connected properly, the motor starts spinning.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP821 device needs very few external components for the features described in *Feature Description*. The device needs a 1-µF or more capacitor connected at VCC. The Lock Detection capacitor decides the hiccup time.

8.2 Typical Application

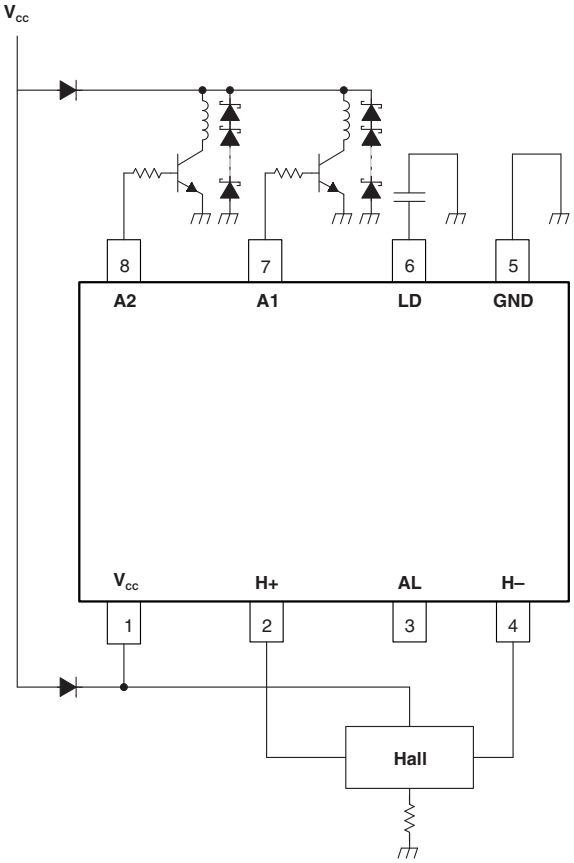


Figure 5. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the following parameters:

- Test setup input voltage: 12-V DC source
- VCC capacitor: 1 µF or more
- H Bridge top side: P-channel FETs
- H Bridge bottom side: N-channel FETs

Typical Application (continued)

8.2.2 Detailed Design Procedure

Pins:

- Connect hall sensor differential inputs to IN+ and IN–.
- Connect LD to Lock Detection capacitor.
- Connect drive outputs to the gates of the H bridge switches.
- Pull up on FG.

Power Supply:

- Make sure the power supply is set with sufficient current limit at the decided motor voltage (12 V and 1 A are shown in *Application Curves*).

Build the circuit with recommended connections at the pins.

Test the motor circuit with hardware connected to it.

8.2.3 Application Curves

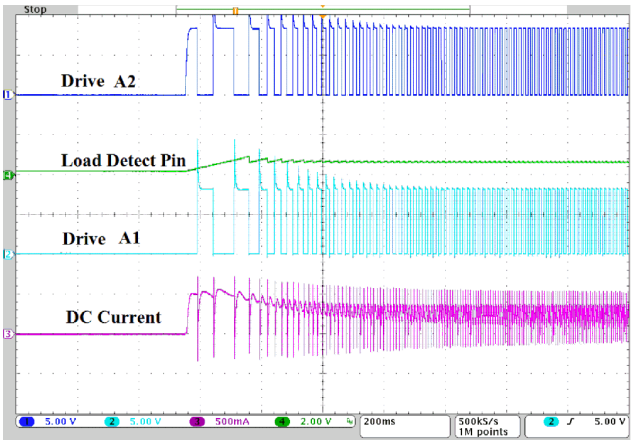


Figure 6. Start-up at 12 V (Soft Start)

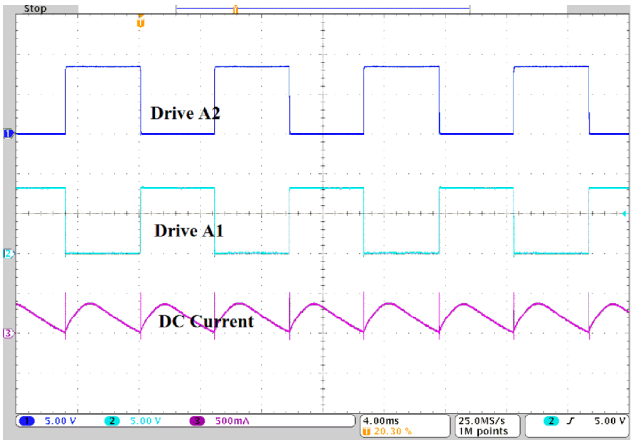


Figure 7. Motor Outputs and DC Current

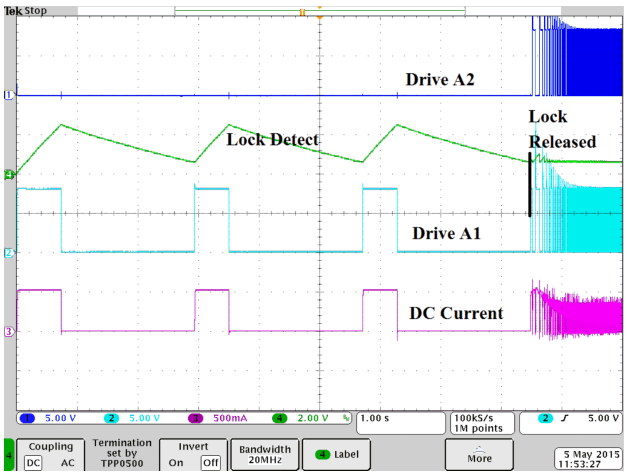


Figure 8. Lock Detection and Retries

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9 Power Supply Recommendations

Connect a bulk capacitor of 1 µF or greater to VDD and GND. The maximum voltage applied must be less than 30 V.

10 Layout

10.1 Layout Guidelines

A bulk capacitor at the VDD and GND LD capacitor can be connected near the device as shown in Figure 9.

10.2 Layout Example

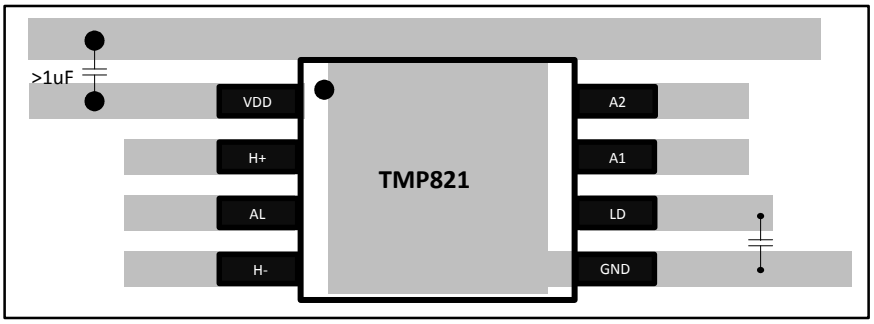


Figure 9. Recommended Layout Example

10.3 Power Dissipation

Figure 10 shows allowable power dissipation versus ambient temperature.

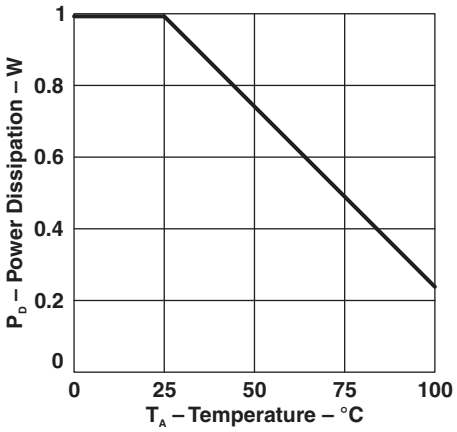


Figure 10. Power Dissipation

Use Equation 3 to calculate total power consumption.

$$P_{total} = P_{C1} + P_{C2} + P_{C3}$$

where

- P_{C1} = circuit power dissipation
- $P_{C1} = V_{CC} \times I_{CC}$
- P_{C2} = output power dissipation
- $P_{C2} = (V_{CC} – V_{OH}) \times I_O$
- V_{OH} = A1 and A2 high-level voltage
- P_{C2} can be reduced by increasing the external output transistor's hFE rank to reduce the I_O consumption.

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Power Dissipation (continued)

- P_{C3} = AL power dissipation
- $P_{C3} = V_{AL_LOW} \times I_{AL}$ (3)

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11 Device and Documentation Support

11.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP821DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TMP821	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

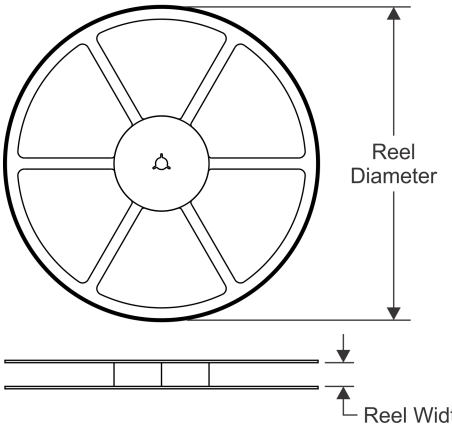
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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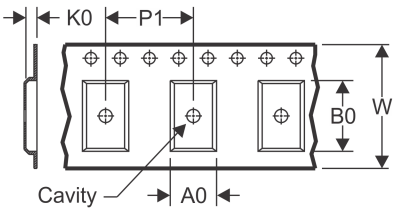
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

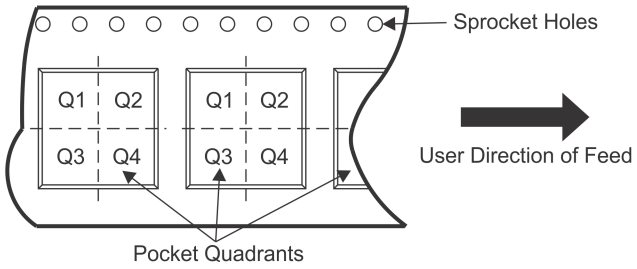


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

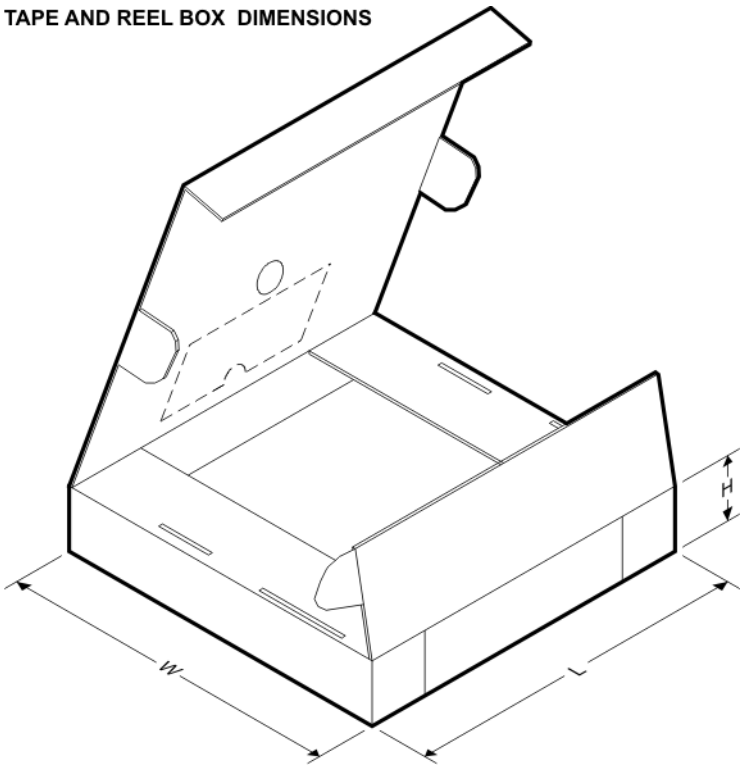
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

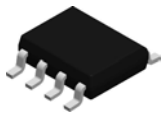
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP821DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP821DR	SOIC	D	8	2500	367.0	367.0	35.0

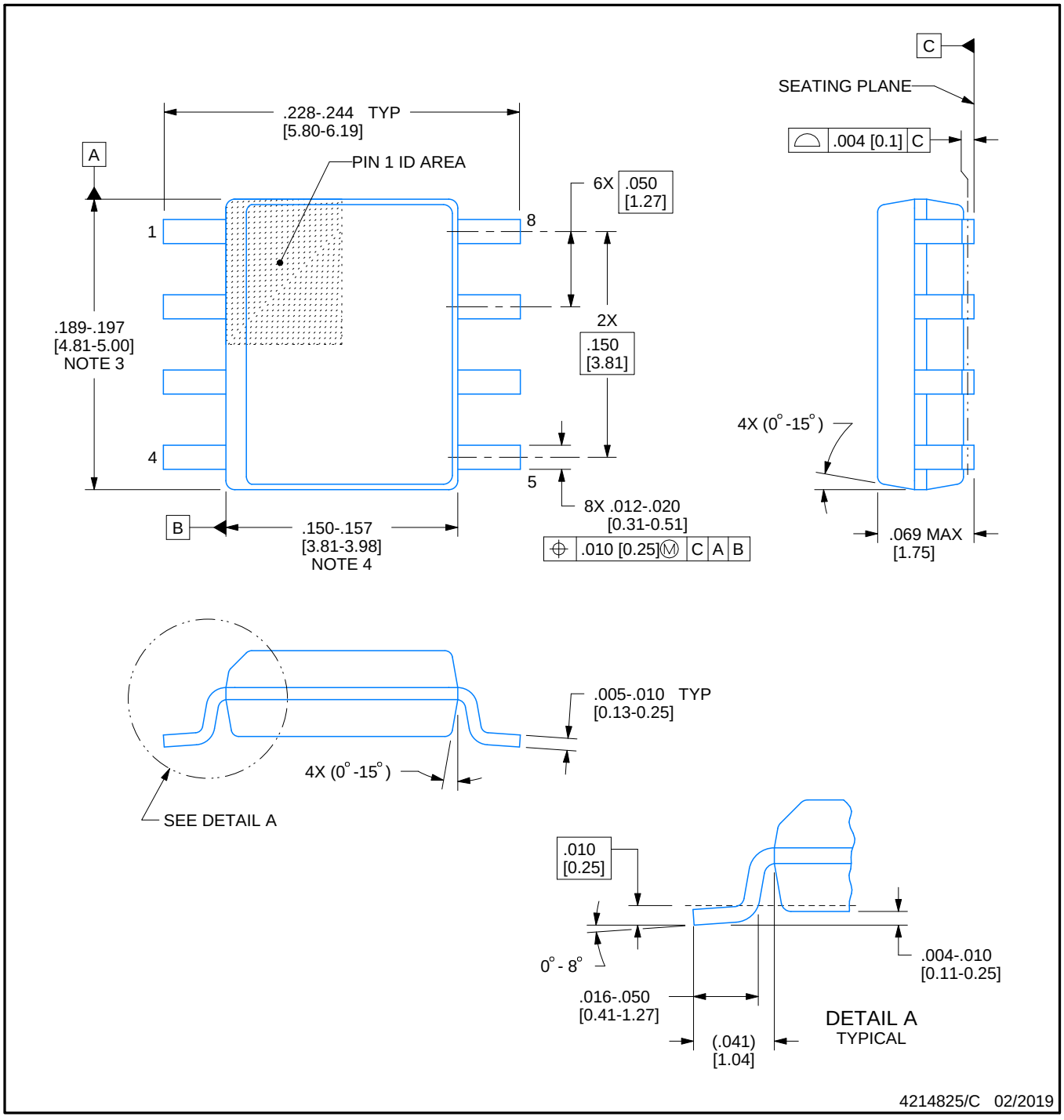


PACKAGE OUTLINE

D0008A

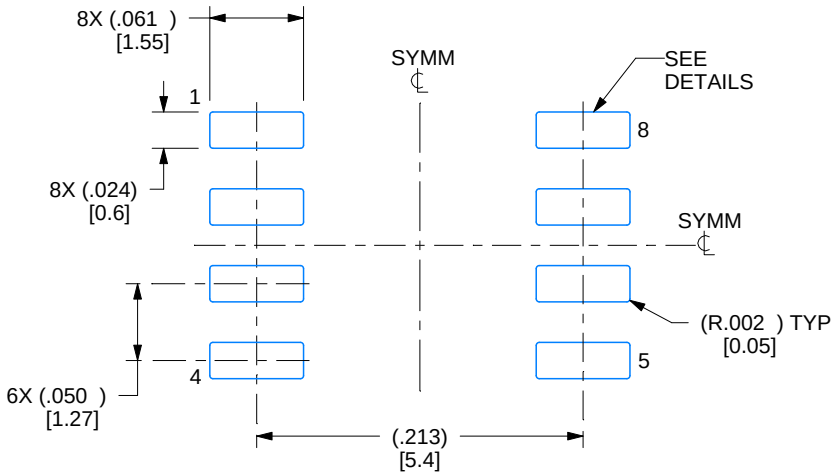
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

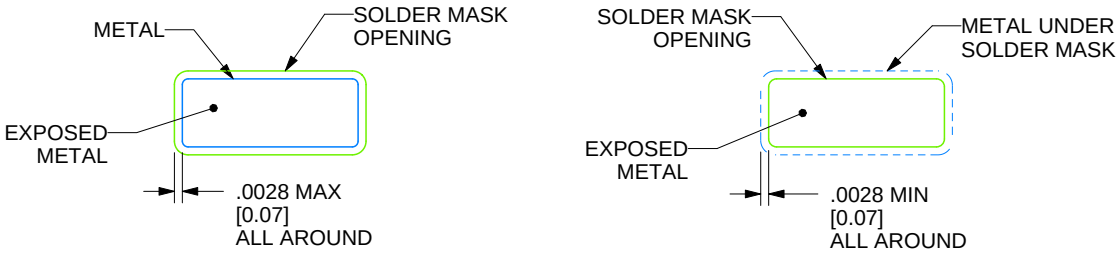


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

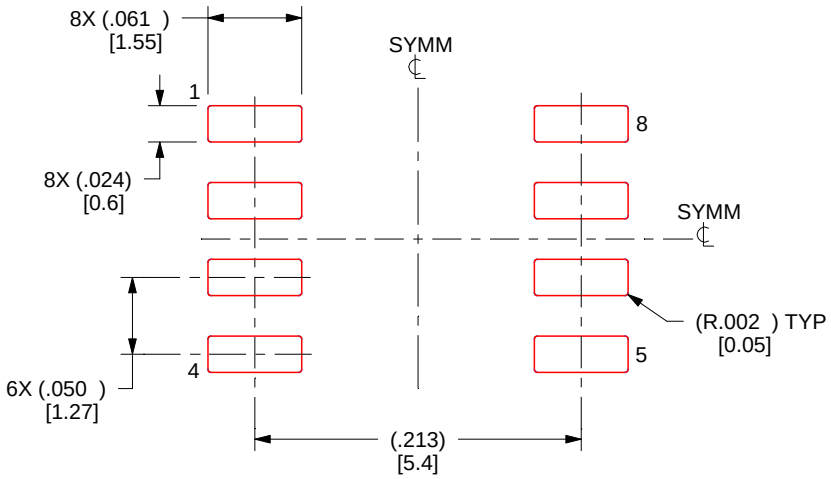
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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