TEXAS INSTRUMENTS

DRV8303

ZHCSBP4C – SEPTEMBER 2013 – REVISED DECEMBER 2016

具有两个电流分流放大器的 DRV8303 三相栅极驱动器

1 特性

- 6V 至 60V 工作电源电压范围
- 1.7A 拉电流和 2.3A 灌电流栅极驱动电流能力
- 具有用于降低 EMI 的转换率控制
- 支持 100% 占空比的自举栅极驱动器
- 6 种或 3 种脉宽调制 (PWM) 输入模式
- 具有可调节增益和偏移的双集成电流分流放大器
- 支持 3.3V 和 5V 接口
- 串行外设接口 (SPI)
- DRV8303 中的 特性：
  - 可编程死区控制 (DTC)
  - 可编程过流保护 (OCP)
  - PVDD 和 GVDD 欠压锁定 (UVLO)
  - GVDD 过压锁定 (OVLO)
  - 过热警告/关断 (OTW/OTS)
  - 通过 nFAULT、nOCTW 和 SPI 寄存器进行报告

2 应用

- 三相无刷直流 (BLDC) 电机和永磁同步电机 (PMSM)
- CPAP 和泵
- 电动自行车
- 电动工具
- 机器人和遥控 (RC) 玩具
- 工业自动化

3 说明

DRV8303 是一款适用于三相电机驱动应用的栅极驱动器 IC。该器件提供三个半桥驱动器，每个驱动器能够驱动两个 N 通道 MOSFET。该器件最高支持 1.7A 拉电流和 2.3A 峰值电流。DRV8303 可在 6V 至 60V 的宽电源范围内，在单一电源供电下运行。它采用自举栅极驱动器架构和涓流充电电路来支持 100% 占空比。DRV8303 在切换高侧或低侧 MOSFET 时使用自动握手机制，以防止发生电流击穿。高侧和低侧 MOSFET 的集成 VDS 感测用于防止外部功率级出现过流现象。

DRV8303 具有两个针对电流进行精确测量的分流放大器。这两个放大器支持双向电流感测，可提供高达 3V 的可调节输出失调电压。

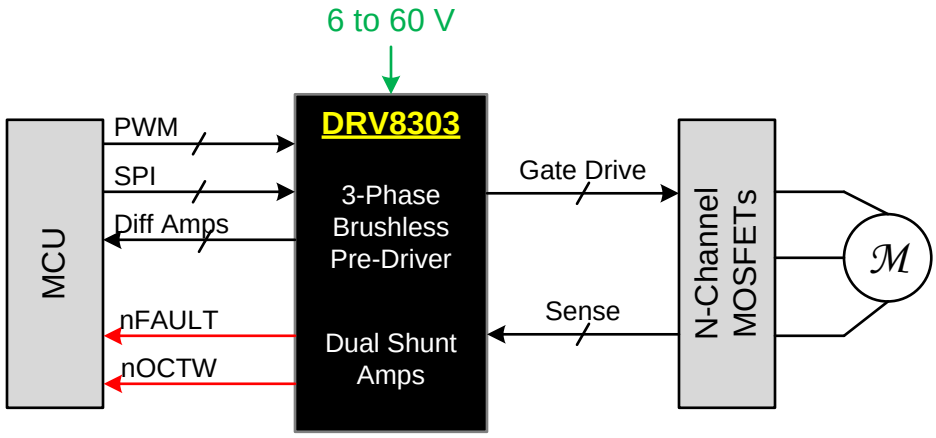
串行外设接口 (SPI) 提供详细的故障报告和灵活的参数设置，例如电流分流放大器的增益选项和栅极驱动器的转换率控制。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV8303	TSSOP (48)	12.50mm x 6.10mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (November 2015) to Revision C **Page**

- Added the maximum voltage difference and maximum voltage parameters for the BST_X, GH_X, SL_X, and SH_X pins in the *Absolute Maximum Ratings* table ... 5
- 已添加 *文档支持* 和*接收文档更新通知* 部分 ... 29

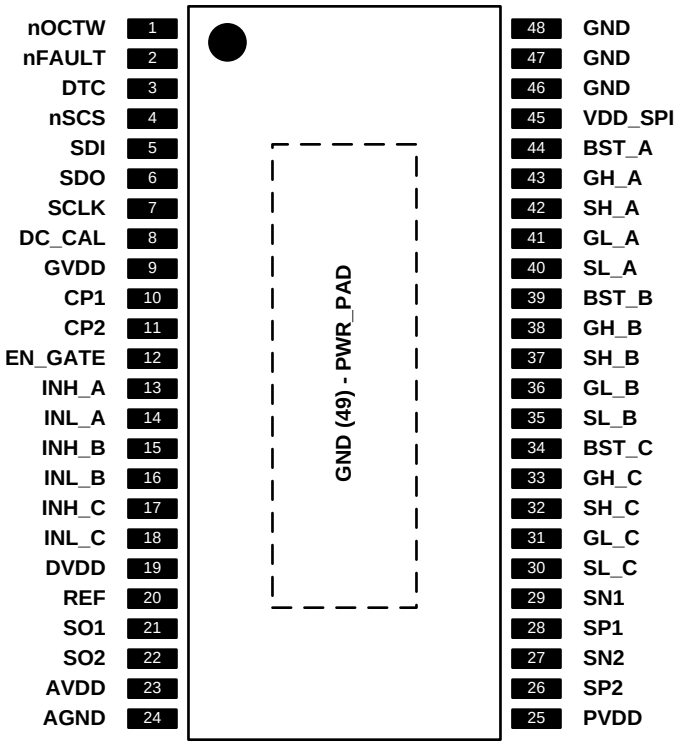
Changes from Revision A (October 2013) to Revision B **Page**

- 已添加 *ESD 额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 更新了标题 ... 1
- V_{PVDD} absolute max voltage rating reduced from 70 V to 65 V ... 5
- Clarification made on how the OCP status bits report in *Overcurrent Protection (OCP) and Reporting* ... 15
- Update to PVDD undervoltage protection in *Undervoltage Protection (UVLO)* describing specific transient brownout issue. ... 16
- Update to EN_GATE pin functional description in *EN_GATE* clarifying proper EN_GATE reset pulse lengths. ... 17
- Added gate driver power-up sequencing errata ... 22

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5 Pin Configuration and Functions

DCA Package
48-Pin TSSOP Pad Down
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	nOCTW	O	Overcurrent and overtemperature warning indicator. This output is open drain with external pullup resistor required. Programmable output mode through SPI registers.
2	nFAULT	O	Fault report indicator. This output is open drain with external pullup resistor required.
3	DTC	I	Dead-time adjustment with external resistor to GND
4	nSCS	I	SPI chip select
5	SDI	I	SPI input
6	SDO	O	SPI output
7	SCLK	I	SPI clock signal
8	DC_CAL	I	When DC_CAL is high, device shorts inputs of shunt amplifiers and disconnects loads. DC offset calibration can be done through external microcontroller.
9	GVDD	P	Internal gate driver voltage regulator. GVDD cap should connect to GND
10	CP1	P	Charge pump pin 1, ceramic cap should be used between CP1 and CP2
11	CP2	P	Charge pump pin 2, ceramic cap should be used between CP1 and CP2
12	EN_GATE	I	Enable gate driver and current shunt amplifiers.
13	INH_A	I	PWM Input signal (high side), half-bridge A
14	INL_A	I	PWM Input signal (low side), half-bridge A
15	INH_B	I	PWM Input signal (high side), half-bridge B
16	INL_B	I	PWM Input signal (low side), half-bridge B
17	INH_C	I	PWM Input signal (high side), half-bridge C
18	INL_C	I	PWM Input signal (low side), half-bridge C

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
19	DVDD	P	Internal 3.3-V supply voltage. DVDD cap should connect to AGND. This is an output, but not specified to drive external circuitry.
20	REF	I	Reference voltage to set output of shunt amplifiers with a bias voltage which equals to half of the voltage set on this pin. Connect to ADC reference in microcontroller.
21	SO1	O	Output of current amplifier 1
22	SO2	O	Output of current amplifier 2
23	AVDD	P	Internal 6-V supply voltage, AVDD capacitor should always be installed and connected to AGND. This is an output, but not specified to drive external circuitry.
24	AGND	P	Analog ground pin
25	PVDD	P	Power supply pin for gate driver, current shunt amplifier, and SPI communication. PVDD cap should connect to GND
26	SP2	I	Input of current amplifier 2 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best common mode rejection.
27	SN2	I	Input of current amplifier 2 (connecting to negative input of amplifier).
28	SP1	I	Input of current amplifier 1 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best common mode rejection.
29	SN1	I	Input of current amplifier 1 (connecting to negative input of amplifier).
30	SL_C	I	Low-Side MOSFET source connection, half-bridge C. Low-side V_{DS} measured between this pin and SH_C.
31	GL_C	O	Gate drive output for Low-Side MOSFET, half-bridge C
32	SH_C	I	High-Side MOSFET source connection, half-bridge C. High-side V_{DS} measured between this pin and PVDD.
33	GH_C	O	Gate drive output for High-Side MOSFET, half-bridge C
34	BST_C	P	Bootstrap capacitor pin for half-bridge C
35	SL_B	I	Low-Side MOSFET source connection, half-bridge B. Low-side V_{DS} measured between this pin and SH_B.
36	GL_B	O	Gate drive output for Low-Side MOSFET, half-bridge B
37	SH_B	I	High-Side MOSFET source connection, half-bridge B. High-side V_{DS} measured between this pin and PVDD.
38	GH_B	O	Gate drive output for High-Side MOSFET, half-bridge B
39	BST_B	P	Bootstrap cap pin for half-bridge B
40	SL_A	I	Low-Side MOSFET source connection, half-bridge A. Low-side V_{DS} measured between this pin and SH_A.
41	GL_A	O	Gate drive output for Low-Side MOSFET, half-bridge A
42	SH_A	I	High-Side MOSFET source connection, half-bridge A. High-side V_{DS} measured between this pin and PVDD.
43	GH_A	O	Gate drive output for High-Side MOSFET, half-bridge A
44	BST_A	P	Bootstrap capacitor pin for half-bridge A
45	VDD_SPI	I	SPI supply pin to support 3.3V or 5V logic. Connect to either 3.3V or 5V.
469	GND	O	GND pin. The exposed power pad must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.
47			
48			
49	GND (PWR_PAD)		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{PVDD}	Supply voltage	Relative to PGND	–0.3	65	V
	Maximum supply-voltage ramp rate	Voltage rising up to $PVDD_{MAX}$		1	V/µs
V_{PGND}	Maximum voltage between PGND and GND		–0.3	0.3	V
V_{OPA_IN}	Voltage for SPx and SNx pins		–0.6	0.6	V
V_{LOGIC}	Input voltage for logic and digital pins (INH_A, INL_A, INH_B, INL_B, INH_C, INL_C, EN_GATE, SCLK, SDI, SCS, DC_CAL)		–0.3	7	V
V_{GVDD}	Maximum voltage for GVDD pin			13.2	V
V_{AVDD}	Maximum voltage for AVDD pin			8	V
V_{DVDD}	Maximum voltage for DVDD pin			3.6	V
V_{VDD_SPI}	Maximum voltage for VDD_SPI pin			7	V
V_{SDO}	Maximum voltage for SDO pin			V_{DD_SPI} +0.3	V
V_{REF}	Maximum reference voltage for current amplifier			7	V
V_{BST_MAX}	Maximum voltage for BST_X Pin		–0.3	80	V
V_{BST_DIFF}	Maximum voltage difference for (BST_X-SH_X) and (BST_X-GH_X)		–0.3	14.5	V
V_{GH_MAX}	Maximum voltage for GH_X pin		–0.3	80	V
V_{GH_DIF}	Maximum voltage difference for (GH_X-SH_X)		–0.3	14.5	V
V_{GL_MAX}	Maximum voltage for GL_X pin		–0.3	13.2	V
V_{GL_DIF}	Maximum voltage difference for (GL_X-SL_X)		–0.3	13.2	V
V_{SH_MAX}	Maximum voltage for SH_X pin		–2	PVDD + 2	V
V_{SL_MAX}	Maximum voltage for SL_X pin		–0.6	0.6	V
I_{IN_MAX}	Maximum current for all digital and analog inputs (INH_A, INL_A, INH_B, INL_B, INH_C, INL_C, SCLK, SCS, SDI, EN_GATE, DC_CAL, DTC)		–1	1	mA
I_{SINK_MAX}	Maximum sinking current for open-drain pins (nFAULT and nOCTW pins)			7	mA
I_{REF}	Maximum current for REF pin		100		µA
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

			MIN	NOM	MAX	UNIT
V_{PVDD}	DC supply voltage PVDD for normal operation	Relative to PGND	6		60	V
I_{DIN_EN}	Input current of digital pins when EN_GATE is high				100	µA
I_{DIN_DIS}	Input current of digital pins when EN_GATE is low				1	µA
C_{O_OPA}	Maximum output capacitance on outputs of shunt amplifier				20	pF
R_{DTC}	Dead time control resistor. Time range is 50 ns (–GND) to 500 ns (150 kΩ) with a linear approximation.		0		150	kΩ
I_{FAULT}	nFAULT pin sink current. Open drain	V = 0.4 V			2	mA
I_{OCTW}	nOCTW pin sink current. Open drain	V = 0.4 V			2	mA
V_{REF}	External voltage reference voltage for current shunt amplifiers		2		6	V
f_{gate}	Operating switching frequency of gate driver	$Q_{g(TOT)}$ = 25 nC or total 30-mA gate drive average current			200	kHz
I_{gate}	Total average gate drive current				30	mA
T_A	Ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV8303 DCA (TSSOP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

PVDD = 6 V to 60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT PINS: INH_X, INL_X, SCS, SDI, SCLK, EN_GATE, DC_CAL						
V_{IH}	High input threshold		2			V
V_{IL}	Low input threshold				0.8	V
RPULL_DOWN – INTERNAL PULLDOWN RESISTOR FOR GATE DRIVER INPUTS						
R_{EN_GATE}	Internal pulldown resistor for EN_GATE			100		kΩ
R_{INH_X}	Internal pulldown resistor for high side PWMs (INH_A, INH_B, and INH_C)	EN_GATE high		100		kΩ
R_{INH_X}	Internal pulldown resistor for low side PWMs (INL_A, INL_B, and INL_C)	EN_GATE high		100		kΩ
R_{SCS}	Internal pulldown resistor for nSCS	EN_GATE high		100		kΩ
R_{SDI}	Internal pulldown resistor for SDI	EN_GATE high		100		kΩ
R_{DC_CAL}	Internal pulldown resistor for DC_CAL	EN_GATE high		100		kΩ
R_{SCLK}	Internal pulldown resistor for SCLK	EN_GATE high		100		kΩ
OUTPUT PINS: nFAULT AND nOCTW						
V_{OL}	Low-output threshold	I_O = 2 mA			0.4	V
V_{OH}	High-output threshold	External 47-kΩ pullup resistor connected to 3-5.5 V	2.4			V

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Electrical Characteristics (continued)

PVDD = 6 V to 60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	Leakage current on open drain pins when logic high (nFAULT and nOCTW)				1	µA
GATE DRIVE OUTPUT: GH_A, GH_B, GH_C, GL_A, GL_B, GL_C						
V_{GX_NORM}	Gate driver Vgs voltage	PVDD = 8V to 60 V, I_{gate} = 30 mA, C_{CP} = 22 nF	9.5		11.5	V
		PVDD = 8 V to 60 V, I_{gate} = 30 mA, C_{CP} = 220 nF	9.5		11.5	
V_{GX_MIN}	Gate driver Vgs voltage	PVDD = 6 V to 8 V, I_{gate} = 15 mA, C_{CP} = 22 nF	8.8			V
		PVDD = 6 V to 8 V, I_{gate} = 30 mA, C_{CP} = 220 nF	8.3			
I_{oso1}	Maximum source current setting 1, peak	Vgs of FET equals to 2 V. REG 0x02		1.7		A
I_{osi1}	Maximum sink current setting 1, peak	Vgs of FET equals to 8 V. REG 0x02		2.3		A
I_{oso2}	Source current setting 2, peak	Vgs of FET equals to 2 V. REG 0x02		0.7		A
I_{osi2}	Sink current setting 2, peak	Vgs of FET equals to 8 V. REG 0x02		1		A
I_{oso3}	Source current setting 3, peak	Vgs of FET equals to 2 V. REG 0x02		0.25		A
I_{osi3}	Sink current setting 3, peak	Vgs of FET equals to 8 V. REG 0x02		0.5		A
R_{gate_off}	Gate output impedance during standby mode when EN_GATE low (pins GH_x, GL_x)		1.6		2.4	kΩ
SUPPLY CURRENTS						
I_{PVDD_STB}	PVDD supply current, standby	EN_GATE is low. PVDD = 8 V		20	50	µA
I_{PVDD_OP}	PVDD supply current, operating	EN_GATE is high, no load on gate drive output, switching at 10 kHz, 100-nC gate charge		15		mA
I_{PVDD_HIZ}	PVDD supply current, Hi-Z	EN_GATE is high, gate not switching	2	5	10	mA
INTERNAL REGULATOR VOLTAGE						
A_{VDD}	AVDD voltage	PVDD = 8 V to 60 V	6	6.5	7	V
		PVDD = 6 V to 8 V	5.5		6	
D_{VDD}	DVDD voltage		3	3.3	3.6	V
VOLTAGE PROTECTION						
V_{PVDD_UV}	Undervoltage protection limit, PVDD				6	V
V_{GVDD_UV}	Undervoltage protection limit, GVDD				7.5	V
V_{GVDD_OV}	Overvoltage protection limit, GVDD			16		V
CURRENT PROTECTION, (VDS SENSING)						
V_{DS_OC}	Drain-source voltage protection limit	PVDD = 8 V to 60 V	0.125		2.4	V
		PVDD = 6 V to 8 V(1)	0.125		1.491	
T_{OC}	OC sensing response time			1.5		µs
T_{OC_PULSE}	nOCTW pin reporting pulse stretch length for OC event			64		µs
TEMPERATURE PROTECTION						
OTW_CLR	Junction temperature for resetting over temperature warning			115		°C
OTW_SET/ OTSD_CLR	Junction temperature for over temperature warning and resetting over temperature shut down			130		°C
OTSD_SET	Junction temperature for over temperature shut down		150			°C

(1) Reduced A_{VDD} voltage range results in limitations on settings for overcurrent protection. See Table 12.

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6.6 Current Shunt Amplifier Characteristics

Over operating free-air temperature range.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G1	Gain option 1	Tc = –40°C to 125°C	9.5	10	10.5	V/V
G2	Gain option 2	Tc = –40°C to 125°C	18	20	21	V/V
G3	Gain Option 3	Tc = –40°C to 125°C	38	40	42	V/V
G4	Gain Option 4	Tc = –40°C to 125°C	75	80	85	V/V
Tsettling	Settling time to 1%	Tc = 0 to 60°C, G = 10, Vstep = 2 V		300		ns
Tsettling	Settling time to 1%	Tc = 0 to 60°C, G = 20, Vstep = 2 V		600		ns
Tsettling	Settling time to 1%	Tc = 0 to 60°C, G = 40, Vstep = 2 V		1.2		µs
Tsettling	Settling time to 1%	Tc = 0 to 60°C, G = 80, Vstep = 2 V		2.4		µs
Vswing	Output swing linear range		0.3		5.7	V
	Slew Rate	G = 10		10		V/µs
DC_offset	Offset error RTI	G = 10 with input shorted			4	mV
Drift_offset	Offset drift RTI			10		µV/C
Ibias	Input bias current				100	µA
Vin_com	Common input mode range		–0.15		0.15	V
Vin_dif	Differential input range		–0.3		0.3	V
Vo_bias	Output bias	With zero input current, V_{REF} up to 6 V	–0.5%	0.5×Vref	0.5%	V
CMRR_OV	Overall CMRR with gain resistor mismatch	CMRR at DC, gain = 10	70	85		dB

6.7 SPI Characteristics (Slave Mode Only)

			MIN	NOM	MAX	UNIT
t_{SPI_READY}	SPI ready after EN_GATE transitions to HIGH	PVDD > 6 V		5	10	ms
t_{CLK}	Minimum SPI clock period		100			ns
t_{CLKH}	Clock high time	See Figure 1	40			ns
t_{CLKL}	Clock low time	See Figure 1	40			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{HD_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time, CLK high to SDO valid	C_L = 20 pF			20	ns
t_{HD_SDO}	SDO output data hold time	See Figure 1	40			ns
t_{SU_SCS}	SCS setup time	See Figure 1	50			ns
t_{HD_SCS}	SCS hold time		50			ns
t_{HI_SCS}	SCS minimum high time before SCS active low		40			ns
t_{ACC}	SCS access time, SCS low to SDO out of high impedance			10		ns
t_{DIS}	SCS disable time, SCS high to SDO high impedance			10		ns

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6.8 Gate Timing and Protection Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING, OUTPUT PINS						
$t_{pd,lf-O}$	Positive input falling to GH_x falling	C_L = 1 nF, 50% to 50%		45		ns
$t_{pd,lr-O}$	Positive input rising to GL_x falling	C_L = 1 nF, 50% to 50%		45		ns
t_{d_min}	Minimum dead time after hand shaking (1)				50	ns
t_{dtp}	Dead time	With R_{DTC} set to different values	50		500	ns
t_{GDr}	Rise time, gate drive output	C_L = 1 nF, 10% to 90%		25		ns
t_{GDF}	Fall time, gate drive output	C_L = 1 nF, 90% to 10%		25		ns
t_{ON_MIN}	Minimum on pulse	Not including handshake communication. Hi-Z to on state, output of gate driver			50	ns
t_{pd_match}	Propagation delay matching between high side and low side				5	ns
t_{dt_match}	Deadtime matching				5	ns
TIMING, PROTECTION AND CONTROL						
$t_{pd,R_GATE-OP}$	Start-up time, from EN_GATE active high to device ready for normal operation	PVDD is up before start up, all charge pump caps and regulator capacitors as in the *Recommended Operating Conditions*		5	10	ms
$t_{pd,R_GATE-Quick}$	If EN_GATE goes from high to low and back to high state within quick reset time, it will only reset all faults and gate driver without powering down charge pump, current amp, and related internal voltage regulators.	Maximum low pulse time			10	µs
$t_{pd,E-L}$	Delay, error event to all gates low			200		ns
$t_{pd,E-FAULT}$	Delay, error event to $\overline{FAULT}$ low			200		ns

(1) Dead time programming definition: Adjustable delay from GH_x falling edge to GL_X rising edge, and GL_X falling edge to GH_X rising edge. This is a minimum dead-time insertion. It is not added to the value set by the microcontroller externally.

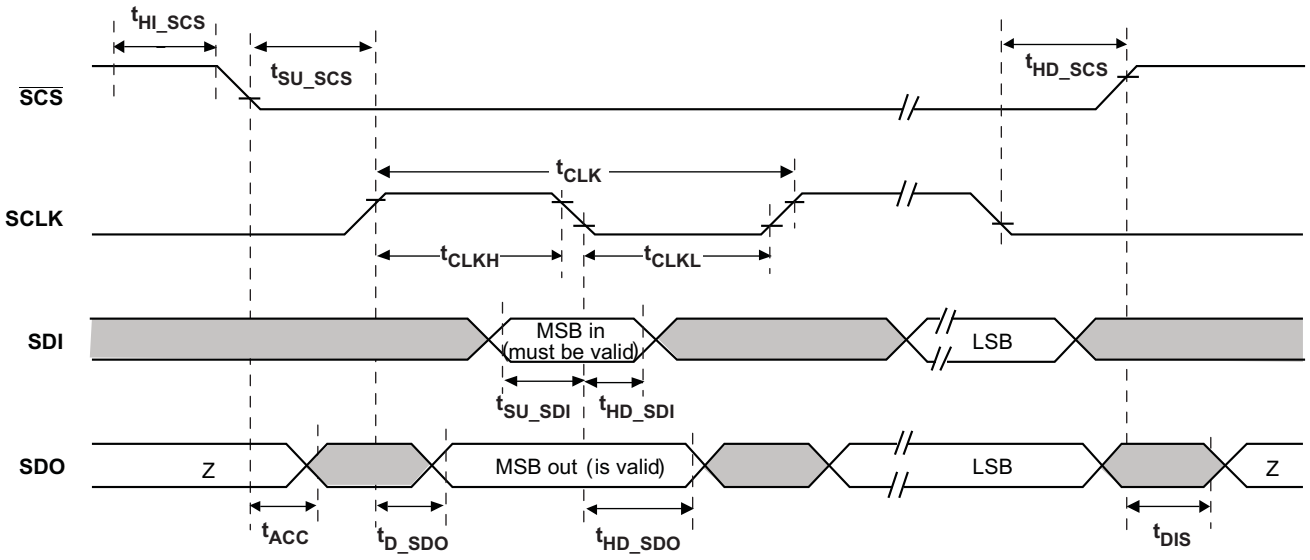


Figure 1. SPI Slave Mode Timing Definition

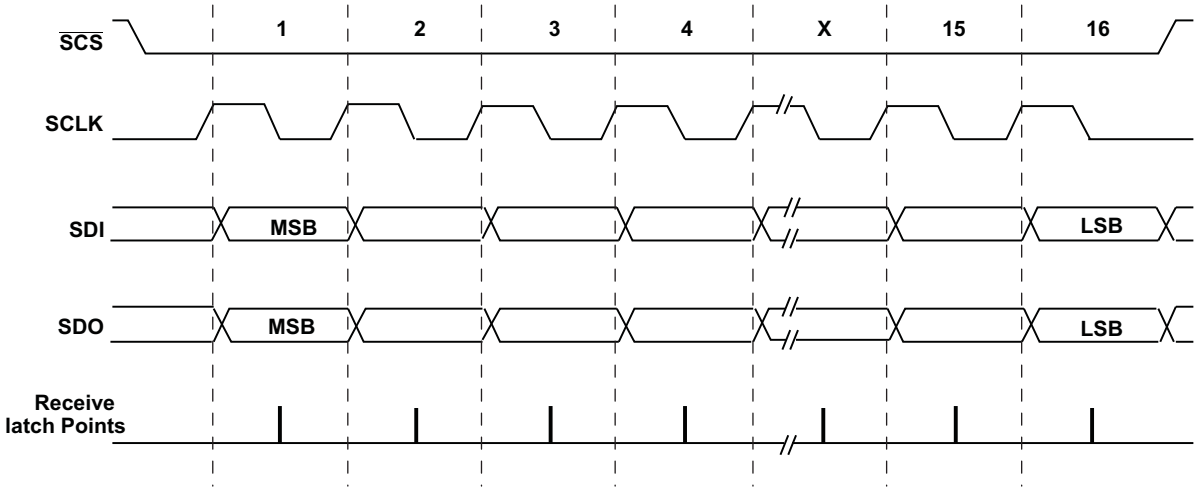
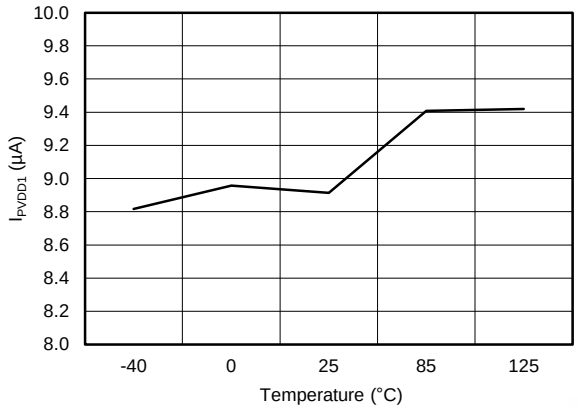


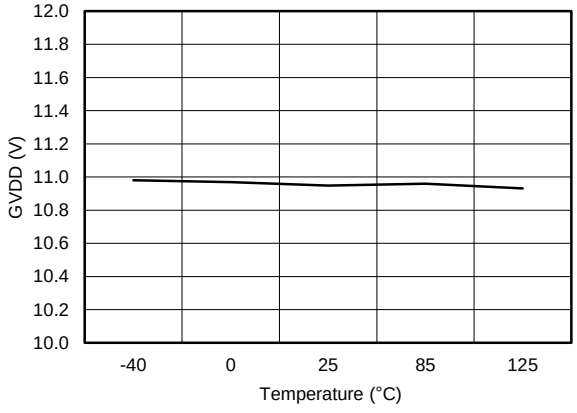
Figure 2. SPI Slave Mode Timing Diagram

6.9 Typical Characteristics



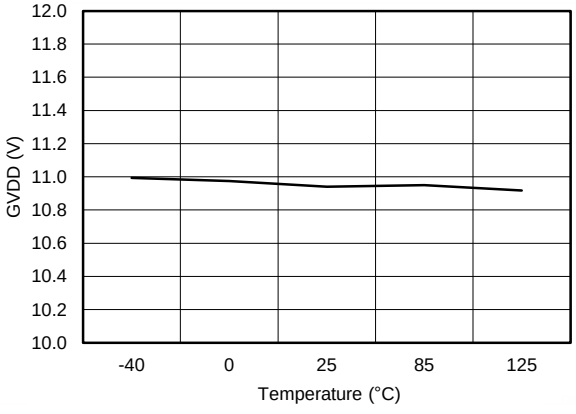
PVDD = 8 V EN_GATE = LOW

Figure 3. I_{PVDD1} vs Temperature



PVDD = 8 V EN_GATE = HIGH

Figure 4. GVDD vs Temperature



PVDD = 60 V EN_GATE = HIGH

Figure 5. GVDD vs Temperature

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7 Detailed Description

7.1 Overview

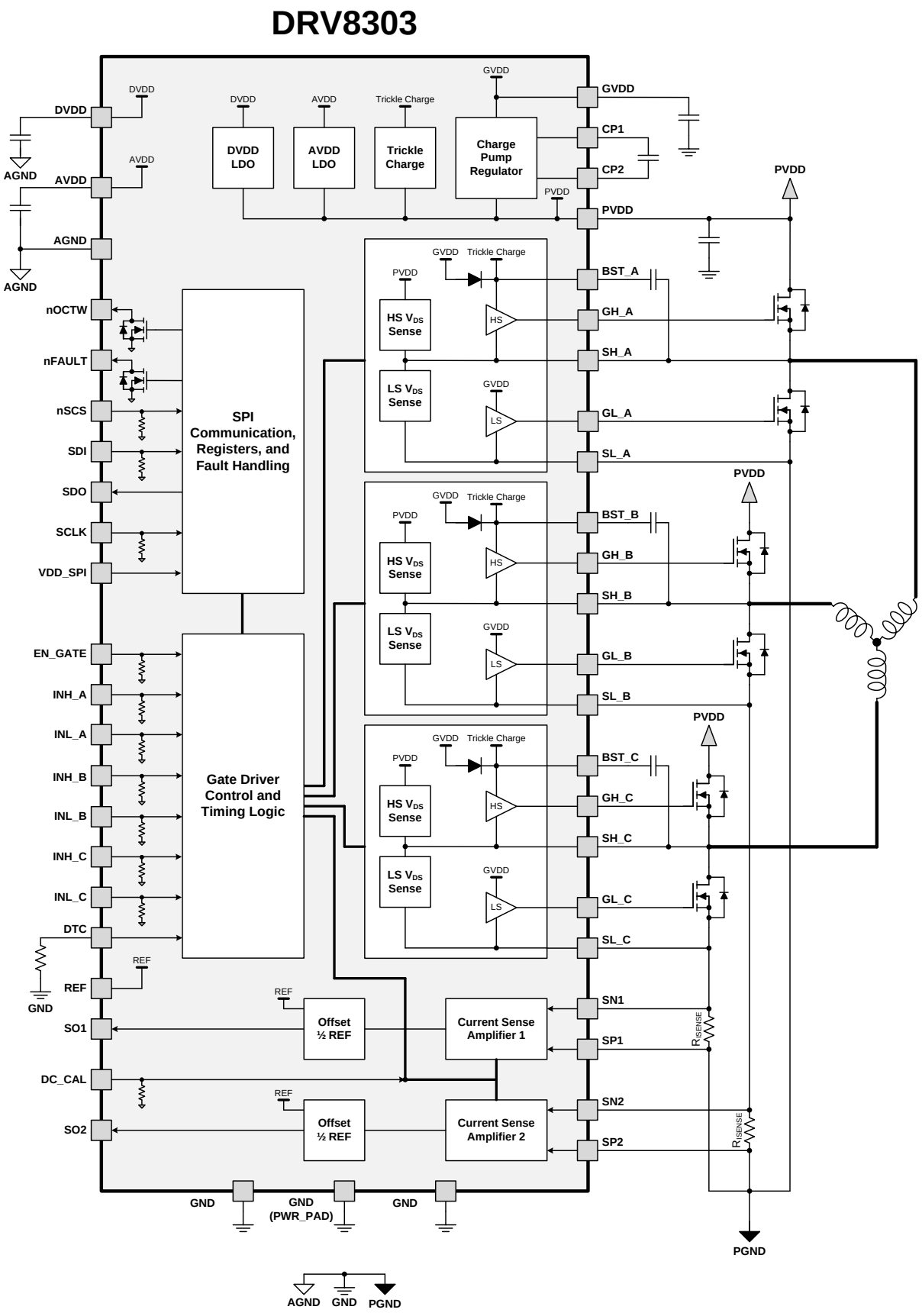
The DRV8303 is a 6-V to 60-V, gate driver IC for three-phase motor drive applications. This device reduces external component count by integrating three half-bridge drivers and two current shunt amplifiers. The DRV8303 provides overcurrent, over-temperature, and undervoltage protection. Fault conditions are indicated through the nFAULT and nOCTW pins in addition to the SPI registers.

Adjustable dead time control and peak gate drive current allows for finely tuning the switching of the external MOSFETs. Internal hand shaking is used to prevent through current.

V_{DS} sensing of the external MOSFETs allows for the DRV8303 to detect overcurrent conditions and respond appropriately. Individual MOSFET overcurrent conditions are reported through the SPI status registers.

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7.2 Functional Block Diagram



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7.3 Feature Description

The following sections describe the DRV8303 features.

7.3.1 Three-Phase Gate Driver

The half-bridge drivers use a bootstrap configuration with a trickle charge pump to support 100% duty cycle operation. Each half-bridge is configured to drive two N-channel MOSFETs, one for the high-side and one for the low-side. The half-bridge drivers can be used in combination to drive a 3-phase motor or separately to drive various other loads.

The peak gate drive current and internal dead times are adjustable to accommodate a variety of external MOSFETs and applications. The peak gate drive current is set through a register setting and the dead time is adjusted with an external resistor on the DTC pin. Shorting the DTC pin to ground will provide the minimum dead time (50 ns). There is an internal hand shake between the high side and low side MOSFETs during switching transitions to prevent current shoot through.

The three-phase gate driver can provide up to 30 mA of average gate drive current. This will support switching frequencies up to 200 kHz when the MOSFET Q_g = 25 nC.

Each MOSFET gate driver has a VDS sensing circuit for overcurrent protection. The sense circuit measures the voltage from the drain to the source of the external MOSFETs while the MOSFET is enabled. This voltage is compared against the programmed trip point to determine if an overcurrent event has occurred. The high-side sense is between the PVDD1 and SH_X pins. The low-side sense is between the SH_X and SL_X pins. Ensuring a differential, low impedance connection to the external MOSFETs for these lines will help provide accurate VDS sensing.

The DRV8303 allows for both 6-PWM and 3-PWM control through a register setting.

Table 1. 6-PWM Mode

INL_X	INH_X	GL_X	GH_X
0	0	L	L
0	1	L	H
1	0	H	L
1	1	L	L

Table 2. 3-PWM Mode

INL_X	INH_X	GL_X	GH_X
X	0	H	L
X	1	L	H

Table 3. Gate Driver External Components

NAME	PIN 1	PIN 2	RECOMMENDED
R_{nOCTW}	nOCTW	V_{CC} (1)	≥10 kΩ
R_{nFAULT}	nFAULT	V_{CC} (1)	≥10 kΩ
R_{DTC}	DTC	GND (PowerPAD)	0 to 150 kΩ (50 ns to 500 ns)
C_{GVDD}	GVDD	GND (PowerPAD)	2.2-µF (20%) ceramic, ≥ 16 V
C_{CP}	CP1	CP2	0.022-µF (20%) ceramic, rated for PVDD
C_{DVDD}	DVDD	AGND	1-µF (20%) ceramic, ≥ 6.3 V
C_{AVDD}	AVDD	AGND	1-µF (20%) ceramic, ≥ 10 V
C_{PVDD}	PVDD	GND (PowerPAD)	≥4.7-µF (20%) ceramic, rated for PVDD
C_{BST_X}	BST_X	SH_X	0.1-µF (20%) ceramic, ≥ 16 V

(1) V_{CC} is the logic supply to the MCU

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7.3.2 Current Shunt Amplifiers

The DRV8303 includes two high performance current shunt amplifiers to accurate low-side, inline current measurement.

The current shunt amplifiers have 4 programmable GAIN settings through the SPI registers. These are 10, 20, 40, and 80 V/V.

They provide output offset up to 3 V to support bidirectional current sensing. The offset is set to half the voltage on the reference pin (REF).

To minimize DC offset and drift over temperature a calibration method is provided through either the DC_CAL pin or SPI register. When DC calibration is enabled, the device will short the input of the current shunt amplifier and disconnect the load. DC calibration can be done at any time, even during MOSFET switching, because the load is disconnected. For the best results, perform the DC calibration during the switching OFF period, when no load is present, to reduce the potential noise impact to the amplifier.

Use Equation 1 to calculate the output of the current shunt amplifier.

$$V_O = \frac{V_{REF}}{2} - G \times (SN_X - SP_X) \quad (1)$$

where

- V_{REF} is the reference voltage (REF pin)
- G is the gain of the amplifier (10, 20, 40, or 80 V/V)
- SNX and SPx are the inputs of channel x. SPx should connect to the ground side of the sense resistor for the nest common mode rejection.

Figure 6 shows the simplified block diagram for the current shunt amplifier.

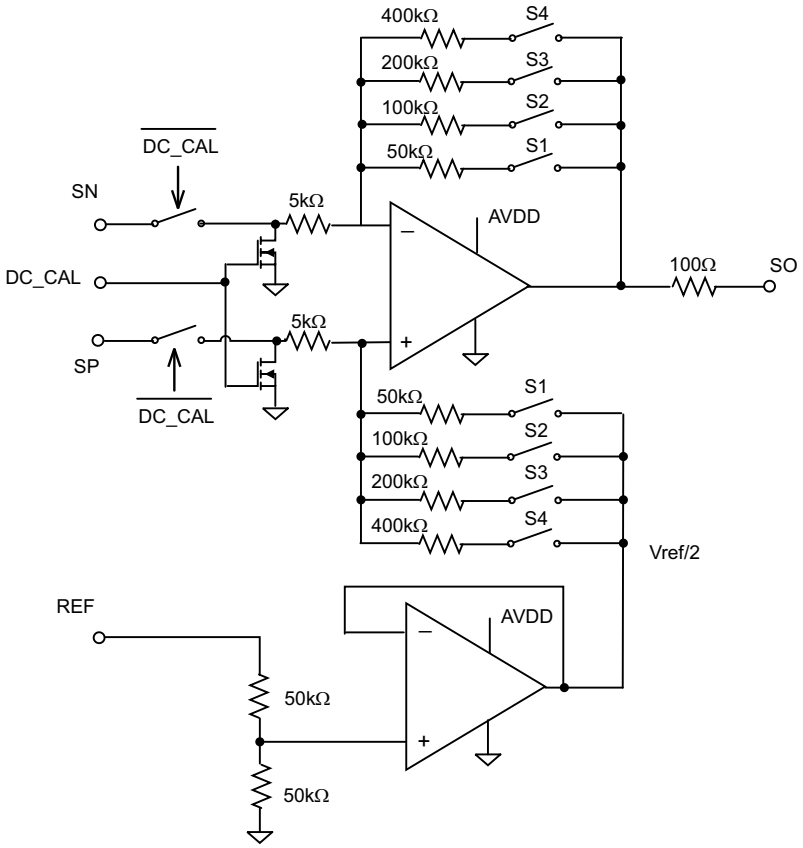


Figure 6. Current Shunt Amplifier Simplified Block Diagram

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7.3.3 Protection Features

The DRV8303 provides a broad range of protection features and fault condition reporting. The DRV8303 has undervoltage and over-temperature protection for the IC. It also has overcurrent and undervoltage protection for the MOSFET power stage. In fault shut down conditions all gate driver outputs will be held low to ensure the external MOSFETs are in a high impedance state.

7.3.3.1 Power Stage Protection

The DRV8303 provides over-current and undervoltage protection for the MOSFET power stage. During fault shut down conditions, all gate driver outputs will be kept low to ensure external FETs at high impedance state.

7.3.3.2 Overcurrent Protection (OCP) and Reporting

To protect the power stage from damage due to excessive currents, VDS sensing circuitry is implemented in the DRV8303. Based on the $R_{DS(on)}$ of the external MOSFETs and the maximum allowed IDS, a voltage threshold can be determined to trigger the overcurrent protection features when exceeded. The voltage threshold is programmed through the SPI registers. Overcurrent protection should be used as a protection scheme only; it is not intended as a precise current regulation scheme. There can be up to a 20% tolerance across channels for the VDS trip point.

$$V_{DS} = I_{DS} \times R_{DS(ON)} \quad (2)$$

The V_{DS} sense circuit measures the voltage from the drain to the source of the external MOSFET while the MOSFET is enabled. The high-side sense is between the PVDD and SH_X pins. The low-side sense is between the SH_X and SL_X pins. Ensuring a differential, low impedance connection to the external MOSFETs for these lines will help provide accurate V_{DS} sensing .

There are four different overcurrent modes (OC_MODE) that can be set through the SPI registers. The OC status bits operate in latched mode. When an overcurrent condition occurs the corresponding OC status bit will latch in the DRV8303 registers until the fault is reset.

1. **Current Limit Mode:** In current limit mode the device uses current limiting instead of device shutdown during an overcurrent event. In this mode the device reports overcurrent events through the nOCTW pin. The nOCTW pin will be held low for a maximum 64-µs period (internal timer) or until the next PWM cycle. If another overcurrent event is triggered from another MOSFET, during a previous overcurrent event, the reporting will continue for another 64-µs period (internal timer will restart) or until both PWM signals cycle. The associated status bit will be asserted for the MOSFET in which the overcurrent was detected. There are two current control settings in current limit mode. These are set by one bit in the SPI registers. The default mode is cycle by cycle (CBC).
   - **Cycle-By-Cycle Mode (CBC)**: In CBC mode, the MOSFET on which overcurrent has been detected on will shut off until the next PWM cycle.
   - **Off-Time Control Mode**: In Off-Time mode, the MOSFET in which overcurrent has been detected is disabled for a 64-µs period (set by internal timer). If overcurrent is detected in another MOSFET, the timer will be reset for another 64-µs period and both MOSFETs will be disabled for the duration. During this period, normal operation can be restored for a specific MOSFET with a corresponding PWM cycle.
2. **OC Latch Shut Down Mode**: When an overcurrent event occurs, both the high-side and low-side MOSFETs will be disabled in the corresponding half-bridge. The nFAULT pin, nFAULT status bit, and OC status bit for the MOSFET in which the overcurrent was detected will latch until the fault is reset through the GATE_RESET bit or a quick EN_GATE reset pulse.
3. **Report Only Mode**: No protective action will be taken in this mode when an overcurrent event occurs. The overcurrent event will be reported through the nOCTW pin (64-µs pulse) and SPI status register. The external MCU should take action based on its own control algorithm.
4. **OC Disable Mode**: The device will ignore and not report all overcurrent detections.

7.3.3.3 Undervoltage Protection (UVLO)

To protect the power output stage during start-up, shutdown, and other possible undervoltage conditions, the DRV8303 provides undervoltage protection by driving the gate drive outputs (GH_X, GL_X) low whenever PVDD or GVDD are below their undervoltage thresholds (PVDD_UV/GVDD_UV). This will put the external MOSFETs in a high impedance state. When the device is in PVDD_UV it will not respond to SPI commands and the SPI registers will revert to their default settings.

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A specific PVDD undervoltage transient brownout from 13 to 15 µs can cause the DRV8303 to become unresponsive to external inputs until a full power cycle. The transient condition consists of having PVDD greater than the PVDD_UV level and then PVDD dropping below the PVDD_UV level for a specific period of 13 to 15 µs. Transients shorter or longer than 13 to 15 µs will not affect the normal operation of the undervoltage protection. Additional bulk capacitance can be added to PVDD to reduce undervoltage transients.

7.3.3.4 Overvoltage Protection (GVDD_OV)

The device will shut down both the gate driver and charge pump if the GVDD voltage exceeds the GVDD_OV threshold to prevent potential issues related to the GVDD pin or the charge pump (for example, short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a reset transition on the EN_GATE pin.

7.3.3.5 Overtemperature Protection

A two-level over-temperature detection circuit is implemented:

- Level 1: overtemperature warning (OTW)
  OTW is reported through nOCTW pin (over-current-temperature warning) for default setting. OCTW pin can be set to report OTW or OCW only through SPI command. See SPI Register section.
- Level 2: overtemperature (OT) latched shut down of gate driver and charge pump (OTSD_GATE)
  Fault will be reported to nFAULT pin. This is a latched shut down, so gate driver will not be recovered automatically even OT condition is not present anymore. An EN_GATE reset through pin or SPI (RESET_GATE) is required to recover gate driver to normal operation after temperature goes below a preset value, t_{OTSD_CLR}.

SPI operation is still available and register settings will be remaining in the device during OTSD operation as long as PVDD is still within defined operation range.

7.3.3.6 Fault and Protection Handling

The nFAULT pin indicates an error event with shut down has occurred such as over-current, over-temperature, overvoltage, or undervoltage. Note that nFAULT is an open-drain signal. nFAULT will go high when gate driver is ready for PWM signal (internal EN_GATE goes high) during start up.

The nOCTW pin indicates overcurrent event and over temperature event that not necessary related to shut down.

Table 4 summarizes all protection features and their reporting structure:

Table 4. Fault and Warning Reporting and Handling

EVENT	ACTION	LATCH	REPORTING ON nFAULT PIN	REPORTING ON nOCTW PIN	REPORTING IN SPI STATUS REGISTER
PVDD undervoltage	External FETs HiZ; Weak pulldown of all gate driver output	N	Y	N	Y
DVDD undervoltage	External FETs HiZ; Weak pulldown of all gate driver output; When recovering, reset all status registers	N	Y	N	N
GVDD undervoltage	External FETs HiZ; Weak pulldown of all gate driver output	N	Y	N	Y
GVDD overvoltage	External FETs HiZ; Weak pulldown of all gate driver output Shut down the charge pump Won't recover and reset through SPI reset command or quick EN_GATE toggling	Y	Y	N	Y
OTW	None	N	N	Y (in default setting)	Y

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Table 4. Fault and Warning Reporting and Handling (continued)

EVENT	ACTION	LATCH	REPORTING ON nFAULT PIN	REPORTING ON nOCTW PIN	REPORTING IN SPI STATUS REGISTER
OTSD_GATE	Gate driver latched shut down. Weak pulldown of all gate driver output to force external FETs HiZ Shut down the charge pump	Y	Y	Y	Y
External FET overload – current limit mode	External FETs current Limiting (only OC detected FET)	N	N	Y	Y, indicates which phase has OC
External FET overload – Latch mode	Weak pulldown of gate driver output and PWM logic “0” of LS and HS in the same phase. External FETs HiZ	Y	Y	Y	Y
External FET overload – reporting only mode	Reporting only	N	N	Y	Y, indicates which phase has OC

7.3.4 Start-Up and Shutdown Sequence Control

During power up, all gate drive outputs are held low. Normal operation of gate driver and current shunt amplifiers can be initiated by toggling EN_GATE from a low state to a high state. If no errors are present, the DRV8303 is ready to accept PWM inputs. Gate driver always has control of the power FETs even in gate disable mode as long as PVDD is within functional region.

There is an internal diode from SDO to VDD_SPI, so VDD_SPI is required to be powered to the same power level as other SPI devices (if there is any SDO signal from other devices) all the time. VDD_SPI supply should be powered up first before any signal appears at SDO pin and powered down after completing all communications at SDO pin.

7.4 Device Functional Modes

7.4.1 EN_GATE

EN_GATE low is used to put gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low power consumption mode to save energy. SPI communication is not supported during this state. Device will put the MOSFET output stage to high impedance mode as long as PVDD is still present.

When EN_GATE pin goes to high, it will go through a power-up sequence, and enable gate driver, current amplifiers, charge pump, internal regulator, and so forth, and reset all latched faults related to gate driver block. It will also reset status registers in SPI table. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present.

When EN_GATE goes from high to low, it will shut down gate driver block immediately, so gate output can put external FETs in high impedance mode. It will then wait for 10us before completely shutting down the rest of the blocks. A quick fault reset mode can be done by toggling EN_GATE pin for a very short period (less than 10 µs). This will prevent device to shut down other function blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery. SPI will still function with such a quick EN_GATE reset mode.

The other way to reset all the faults is to use SPI command (RESET_GATE), which will only reset gate driver block and all the SPI status registers without shutting down other function blocks.

One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset or SPI command reset does not work with GVDD_OV fault. A complete EN_GATE with low level holding longer than 10µS is required to reset GVDD_OV fault. TI highly recommends inspecting the system and board when GVDD_OV occurs.

7.4.2 DTC

Dead time can be programmed through DTC pin. A resistor should be connected from DTC to ground to control the dead time. Dead time control range is from 50 ns to 500 ns. Short DTC pin to ground will provide minimum dead time (50 ns). Resistor range is 0 kΩ to 150 kΩ. Dead time is linearly set over this resistor range.

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Device Functional Modes (continued)

Current shoot through prevention protection will be enabled in the device all time independent of dead time setting and input mode setting.

7.4.3 VDD_SPI

VDD_SPI is the power supply to power SDO pin. It must be connected to the same power supply (3.3V or 5V) that MCU uses for its SPI operation.

During power up or down transient, VDD_SPI pin could be zero voltage shortly. During this period, no SDO signal should be present at SDO pin from any other devices in the system because it causes a parasitic diode in the DRV8303 conducting from SDO to VDD_SPI pin as a short. This should be considered and prevented from system power sequence design.

7.4.4 DC_CAL

When DC_CAL is enabled, device will short inputs of shunt amplifier and disconnect from the load, so external microcontroller can do a DC offset calibration. DC offset calibration can be also done with SPI command. If using SPI exclusively for DC calibration, the DC_CAL pin can connected to GND.

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7.5 Programming

7.5.1 SPI Communication

7.5.1.1 SPI

The DRV8303 SPI operates as a slave. The SPI input (SDI) data format consists of a 16 bit word with 1 read/write bit, 4 address bits, and 11 data bits. The SPI output (SDO) data format consists of a 16 bit word with 1 frame fault bit, 4 address bits, and 11 data bits. When a frame is not valid, frame fault bit will set to 1 and the remaining bits will shift out as 0.

A valid frame must meet following conditions:

- Clock must be low when nSCS goes low.
- Should have 16 full clock cycles.
- Clock must be low when nSCS goes high.

When nSCS is asserted high, any signals at the SCLK and SDI pins are ignored and SDO is forced into a high impedance state. When nSCS transitions from HIGH to LOW, SDO is enabled and the SDO response word loads into the shift register based on the previous SPI input word.

The SCLK pin must be low when nSCS transitions low. While nSCS is low, at each rising edge of the clock the response word is serially shifted out on the SDO pin with the MSB shifted out first.

While SCS is low, at each falling edge of the clock the new input word is sampled on the SDI pin. The SPI input word is decoded to determine the register address and access type (read or write). The MSB will be shifted in first. Any amount of time may pass between bits, as long as nSCS stays active low. This allows two 8-bit words to be used. If the input word sent to SDI is less than 16 bits or more than 16 bits, it is considered a frame error. If it is a write command, the data will be ignored. The fault bit in the next SDO response word will then report 1. After the 16th clock cycle or when nSCS transitions from LOW to HIGH, the SDI shift register data is transferred into a latch where the input word is decoded.

For a READ command (Nth cycle) sent to SDI, SDO will respond with the data at the specified address in the next cycle. (N+1)

For a WRITE command (Nth cycle) sent to SDI, SDO will respond with the data in Status Register 1 (0x00) in the next cycle (N+1). This feature is intended to maximize SPI communication efficiency when having multiple write commands.

7.5.1.2 SPI Format

The SDI input data word is 16 bits long and consists of:

- 1 read/write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

The SDO output data word is 16 bits long and consists of:

- 1 fault frame bit F [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

The SDO output word (Nth cycle) is in response to the previous SDI input word (N-1 cycle).

Therefore each SPI Query/Response pair requires two full 16 bit shift cycles to complete.

Table 5. SPI Input Data Control Word Format

	R/W	ADDRESS				DATA										
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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Table 6. SPI Output Data Response Word Format

	R/W	DATA														
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	F0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

7.6 Register Maps

7.6.1 Read / Write Bit

The MSB bit of the SDI input word (W0) is a read/write bit. When W0 = 0, the input word is a write command. When W0 = 1, input word is a read command.

7.6.2 Address Bits

Table 7. Register Address

REGISTER TYPE	ADDRESS [A3..A0]				REGISTER NAME	DESCRIPTION	READ AND WRITE ACCESS
Status Register	0	0	0	0	Status Register 1	Status register for device faults	R
	0	0	0	1	Status Register 2	Status register for device faults and ID	R
Control Register	0	0	1	0	Control Register 1		R/W
	0	0	1	1	Control Register 2		R/W

7.6.3 SPI Data Bits

7.6.3.1 Status Registers

Table 8. Status Register 1 (Address: 0x00) (all default values are zero)

ADDRESS	REGISTER NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Status Register 1	FAULT	GVDD_UV	PVDD_UV	OTSD	OTW	FETHA_OC	FETLA_OC	FETHB_OC	FETLB_OC	FETHC_OC	FETLC_OC

Table 9. Status Register 2 (Address: 0x01) (all default values are zero)

ADDRESS	REGISTER NAME	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	Status Register 2				GVDD_OV				Device ID [3]	Device ID [2]	Device ID [1]	Device ID [0]

7.6.3.2 Control Registers

Table 10. Control Register 1 for Gate Driver Control (Address: 0x02)(1)

ADDRESS	NAME	DESCRIPTION	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x02	GATE_CURRENT	Gate drive peak current 1.7 A										0(1)	0(1)
		Gate drive peak current 0.7 A										0	1
		Gate drive peak current 0.25 A										1	0
		Reserved										1	1
	GATE_RESET	Normal mode									0(1)		
		Reset gate driver latched faults (reverts to 0)									1		
	PWM_MODE	6 PWM inputs (see Table 1)								0(1)			
		3 PWM inputs (see Table 2)								1			
	OCP_MODE	Current limit						0(1)	0(1)				
		OC latch shut down						0	1				
		Report only						1	0				
		OC disabled						1	1				
	OC_ADJ_SET	See OC_ADJ_SET table	X	X	X	X	X						

(1) Default value

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Table 11. Control Register 2 for Current Shunt Amplifiers and Misc Control (Address: 0x03)(1)

ADDRESS	NAME	DESCRIPTION	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x03	OCTW_MODE	Report both OT and OC at nOCTW pin										0(1)	0(1)
		Report OT only										0	1
		Report OC only										1	0
		Report OC only (reserved)										1	1
	GAIN	Gain of shunt amplifier: 10 V/V								0(1)	0(1)		
		Gain of shunt amplifier: 20 V/V								0	1		
		Gain of shunt amplifier: 40 V/V								1	0		
		Gain of shunt amplifier: 80 V/V								1	1		
	DC_CAL_CH1	Shunt amplifier 1 connects to load through input pins							0(1)				
		Shunt amplifier 1 shorts input pins and disconnects from load for external calibration							1				
	DC_CAL_CH2	Shunt amplifier 2 connects to load through input pins						0(1)					
		Shunt amplifier 2 shorts input pins and disconnects from load for external calibration						1					
	OC_TOFF	Cycle by cycle					0(1)						
		Off-time control					1						
	Reserved												

(1) Default value

7.6.3.3 Overcurrent Adjustment

Table 12. OC_ADJ_SET Table

Control Bit (D6–D10) (0xH)	0	1	2	3	4	5	6	7
Vds (V)	0.060	0.068	0.076	0.086	0.097	0.109	0.123	0.138
Control Bit (D6–D10) (0xH)	8	9	10	11	12	13	14	15
Vds (V)	0.155	0.175	0.197	0.222	0.250	0.282	0.317	0.358
Control Bit (D6–D10) (0xH)	**16**	17	18	19	20	21	22	23
Vds (V)	0.403	0.454	0.511	0.576	0.648	0.730	0.822	0.926
Code Number (0xH)	24	25	26	27	28	29	30	31
Vds (V)	1.043	1.175	1.324	1.491	1.679(1)	1.892(1)	2.131(1)	2.400(1)

(1) Do not use settings 28, 29, 30, 31 for V_{DS} sensing if the IC is expected to operate in the 6-V to 8-V range.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8303 is a gate driver designed to drive a 3-phase BLDC motor in combination with external power MOSFETs. The device provides a high level of integration with three half-bridge gate drivers, two current shunt amplifier, and overcurrent protection.

8.1.1 Gate Driver Power-Up Sequencing Errata

The DRV8301 gate drivers may not correctly power up if a voltage greater than 8.5 V is present on any SH_X pin when EN_GATE is brought logic high (device enabled) after PVDD power is applied (PVDD1 > PVDD_UV). This sequence should be avoided by ensuring the voltage levels on the SH_X pins are less than 8.5 V when the DRV8301 is enabled through EN_GATE.

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8.2 Typical Application

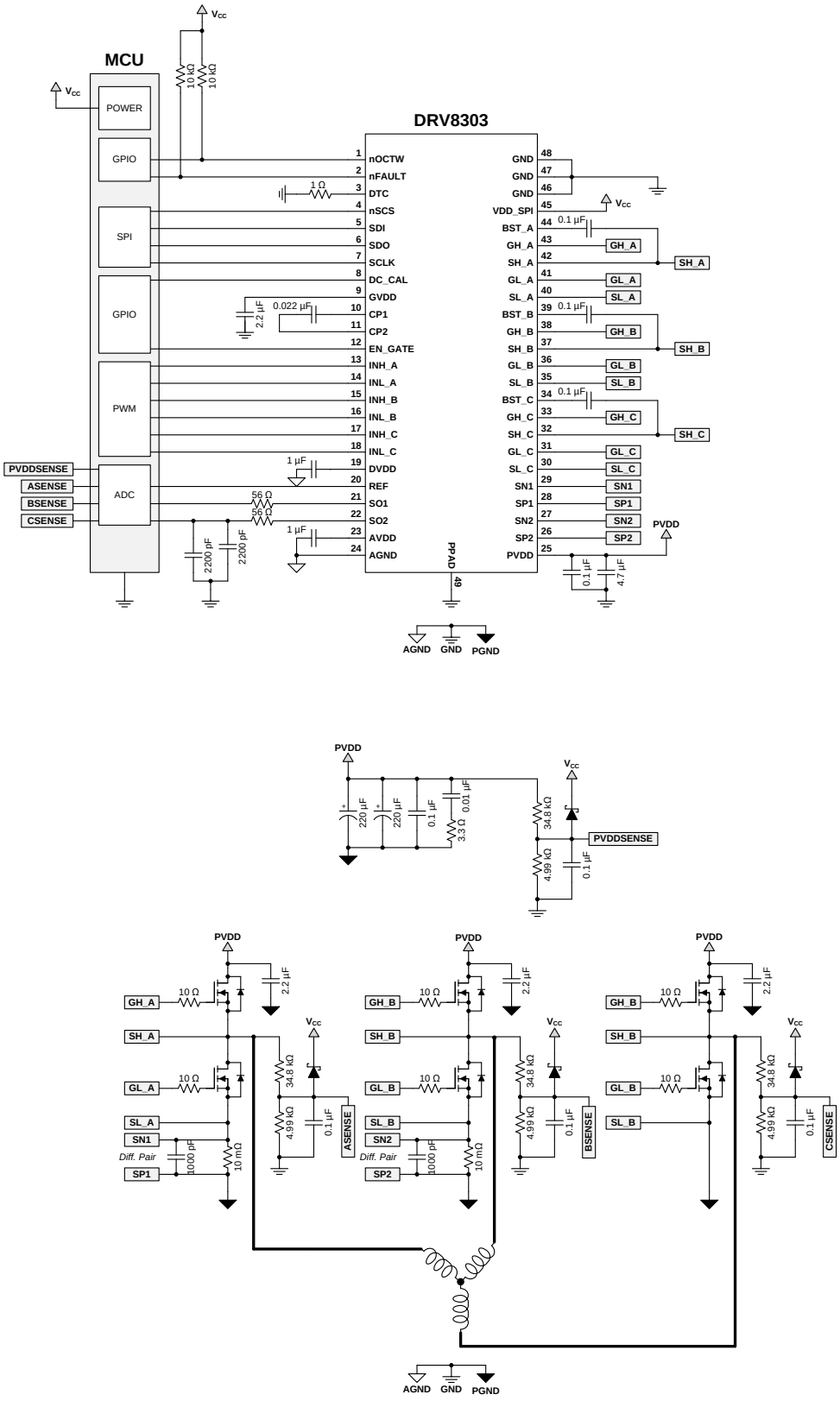


Figure 7. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 13 lists the design parameters for this example.

Table 13. Design Parameters

DESIGN PARAMETER	REFERENCE	VALUE
Supply voltage	PVDD	24 V
Motor winding resistance	M_R	0.5 Ω
Motor winding inductance	M_L	0.28 mH
Motor poles	M_P	16 poles
Motor rated RPM	M_{RPM}	4000 RPM
Target full-scale current	I_{MAX}	14 A
Sense resistor	R_{SENSE}	0.01 Ω
MOSFET Q_g	Q_g	29 nC
MOSFET RDS(on)	$R_{DS(on)}$	4.7 mΩ
VDS trip level	OC_ADJ_SET	0.123 V
Switching frequency	f_{SW}	45 kHz
Series gate resistance	R_{GATE}	10 Ω
Amplifier reference	V_{REF}	3.3 V
Amplifier gain	Gain	10 V/V

8.2.2 Detailed Design Procedure

8.2.2.1 Gate Drive Average Current Load

The gate drive supply (GVDD) of the DRV8303 can deliver up to 30 mA (RMS) of current to the external power MOSFETs. Use Equation 3 to determine the approximate RMS load on the gate drive supply:

$$\text{Gate Drive RMS Current} = \text{MOSFET } Q_g \times \text{Number of Switching MOSFETs} \times \text{Switching Frequency} \quad (3)$$

Example:

$$7.83 \text{ mA} = 29 \text{ nC} \times 6 \times 45 \text{ kHz} \quad (4)$$

This is a rough approximation only.

8.2.2.2 Overcurrent Protection Setup

The DRV8303 provides overcurrent protection for the external power MOSFETs through the use of V_{DS} monitors for both the high side and low side MOSFETs. These are intended for protecting the MOSFET in overcurrent conditions and not for precise current regulation.

The overcurrent protection works by monitoring the V_{DS} voltage of the external MOSFET and comparing it against the OC_ADJ_SET register value. If the V_{DS} exceeds the OC_ADJ_SET value the DRV8303 takes action according to the OC_MODE register.

$$\text{Overcurrent Trip} = \text{OC_ADJ_SET} / \text{MOSFET } R_{DS(on)} \quad (5)$$

Example:

$$26.17 \text{ A} = 0.123 \text{ V} / 4.7 \text{ m}\Omega \quad (6)$$

MOSFET $R_{DS(on)}$ changes with temperature and this will affect the overcurrent trip level.

8.2.2.3 Sense Amplifier Setup

The DRV8303 provides two bidirectional low-side current shunt amplifiers. These can be used to sense a sum of the three half-bridges, two of the half-bridges individually, or in conjunction with an additional shunt amplifier to sense all three half-bridges individually.

1. Determine the peak current that the motor will demand (I_{MAX}). This will be dependent on the motor parameters and your specific application. $I_{(MAX)}$ in this example is 14 A.
2. Determine the available voltage range for the current shunt amplifier. This will be ± half of the amplifier

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reference voltage (V_{REF}). In this case the available range is ±1.65 V.

3. Determine the sense resistor value and amplifier gain settings. There are common tradeoffs for both the sense resistor value and amplifier gain. The larger the sense resistor value, the better the resolution of the half-bridge current. This comes at the cost of additional power dissipated from the sense resistor. A larger gain value will allow you to decrease the sense resistor, but at the cost of increased noise in the output signal. This example uses a 0.01-Ω sense resistor and the minimum gain setting of the DRV8303 (10 V/V). These values allow the current shunt amplifiers to measure ±16.5 A (some additional margin on the 14-A requirement).

8.2.3 Application Curves

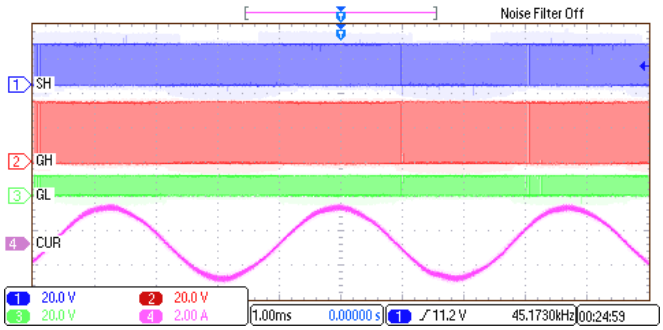


Figure 8. Motor Spinning 2000 RPM

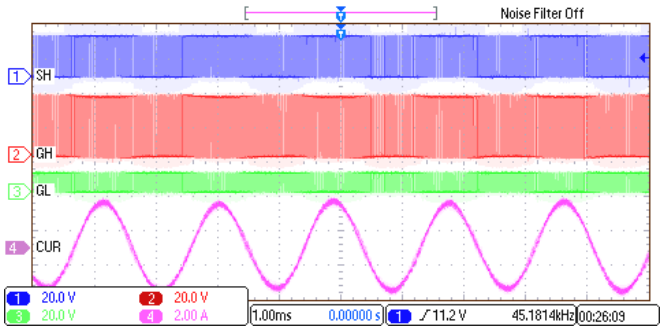


Figure 9. Motor Spinning 4000 RPM

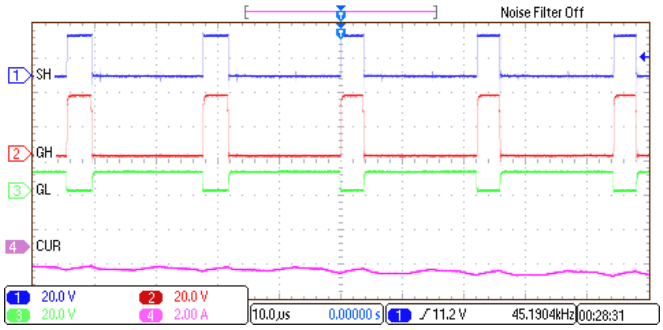


Figure 10. Gate Drive 20% Duty Cycle

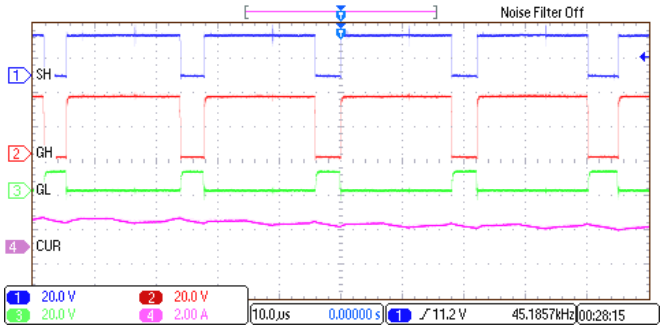


Figure 11. Gate Drive 80% Duty Cycle

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9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and its ability to source or sink current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

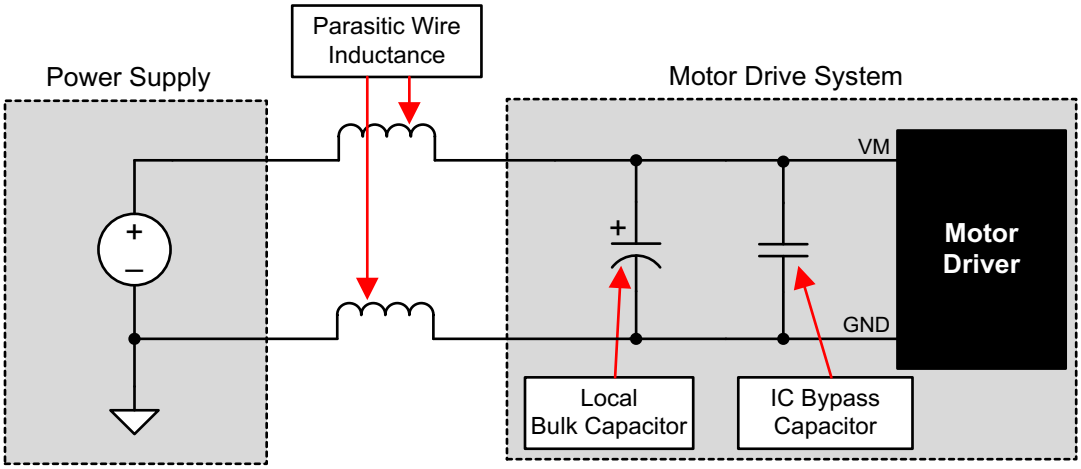


Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

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10 Layout

10.1 Layout Guidelines

Use these layout recommendations when designing a PCB for the DRV8303.

- The DRV8303 makes an electrical connection to GND through the PowerPAD. Always check to ensure that the PowerPAD has been properly soldered (see *PowerPAD™ Thermally Enhanced Package*).
- PVDD bypass capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD).
- GVDD bypass capacitor should be placed close its corresponding pin with a low impedance path to device GND (PowerPAD).
- AVDD and DVDD bypass capacitors should be placed close to their corresponding pins with a low impedance path to the AGND pin. It is preferable to make this connection on the same layer.
- AGND should be tied to device GND (PowerPAD) through a low impedance trace/copper fill.
- Add stitching vias to reduce the impedance of the GND path from the top to bottom side.
- Try to clear the space around and underneath the DRV8303 to allow for better heat spreading from the PowerPAD.

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10.2 Layout Example

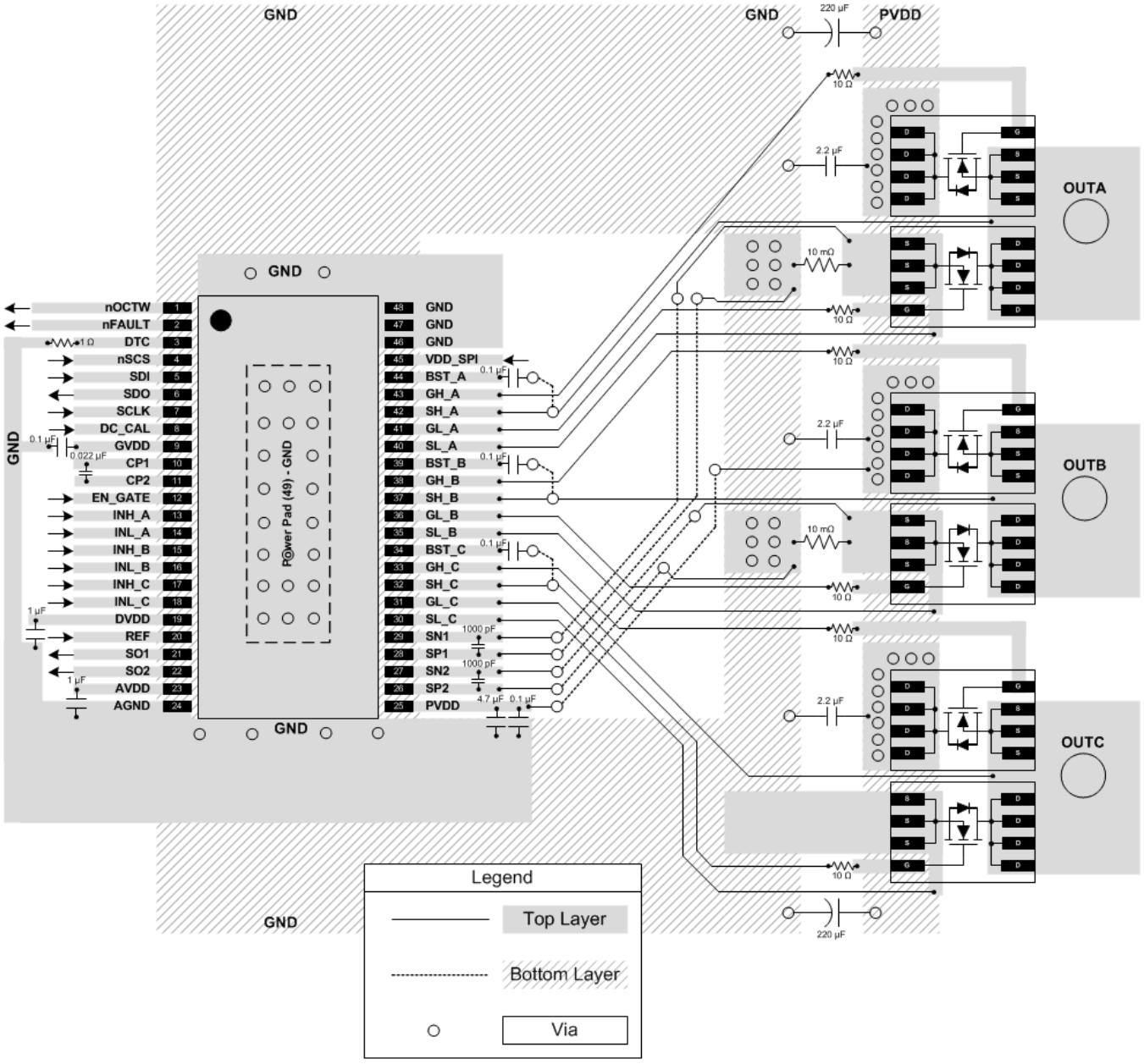


Figure 13. Layout Recommendation

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《DRV8303EVM 用户指南》*
- *《PowerPAD™ 散热增强型封装》*
- *《采用 MSP430 且配有传感器的三相 BLDC 电机控制》*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8303DCA	ACTIVE	HTSSOP	DCA	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8303	Samples
DRV8303DCAR	ACTIVE	HTSSOP	DCA	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8303	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

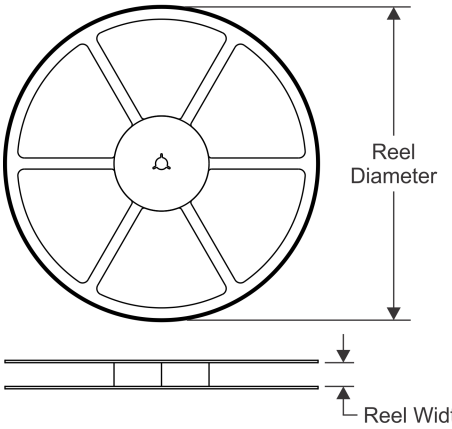
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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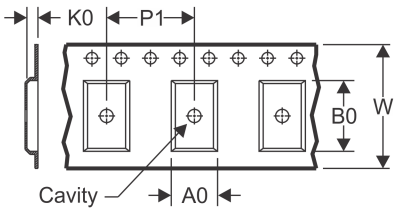
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

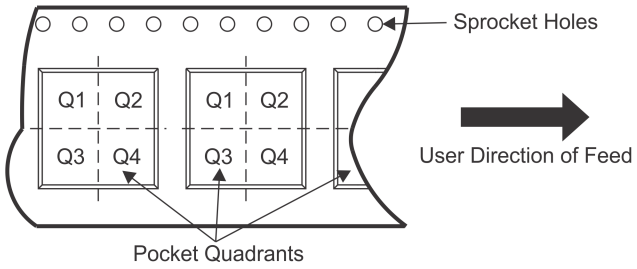


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

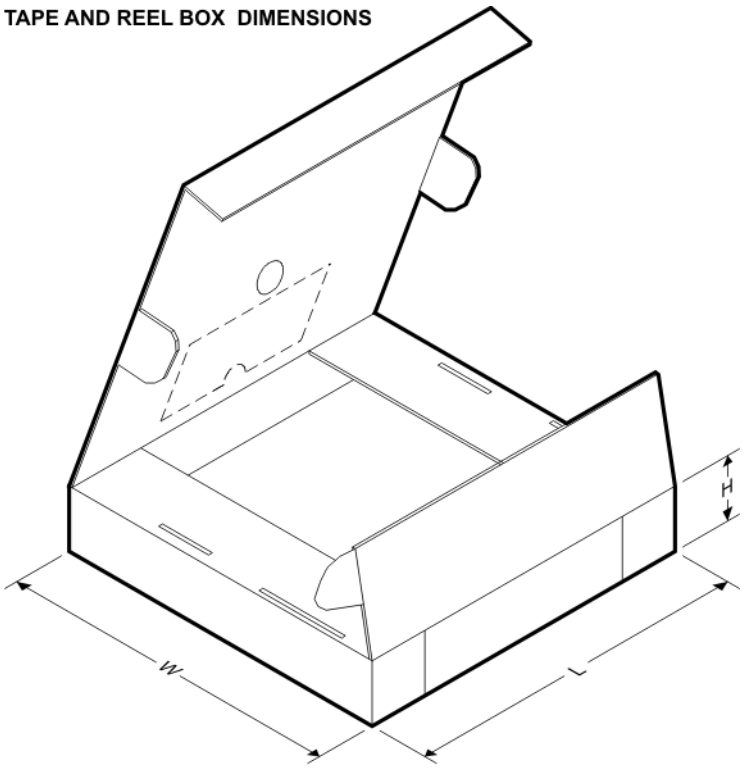
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8303DCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

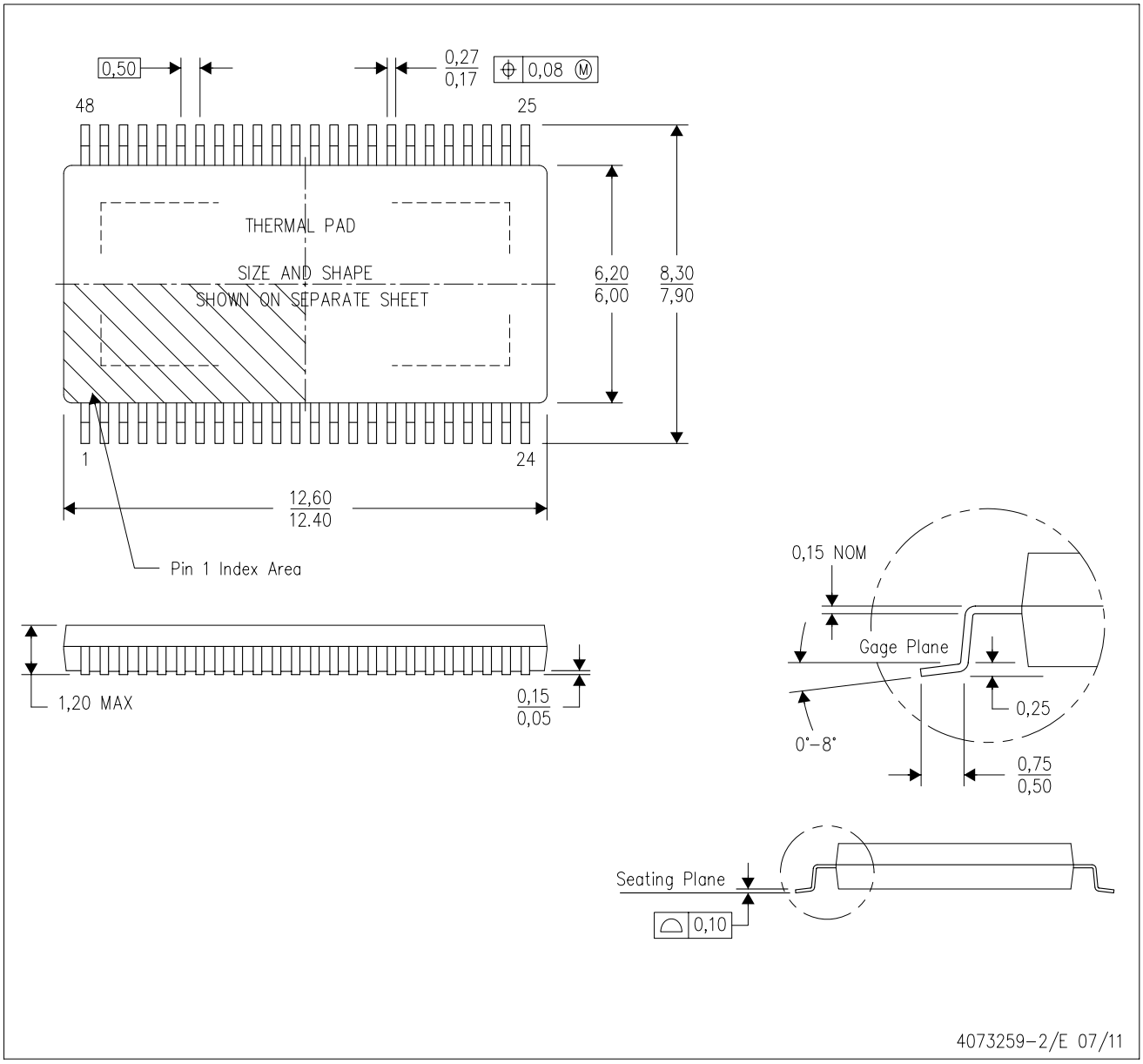
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8303DCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

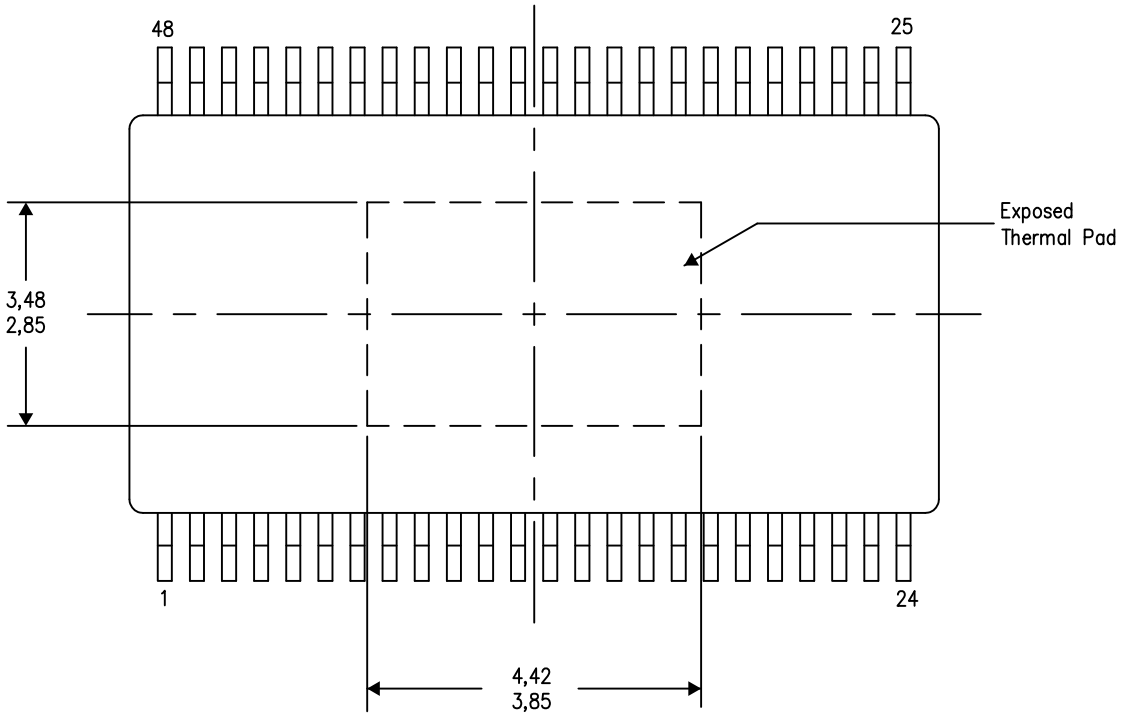
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

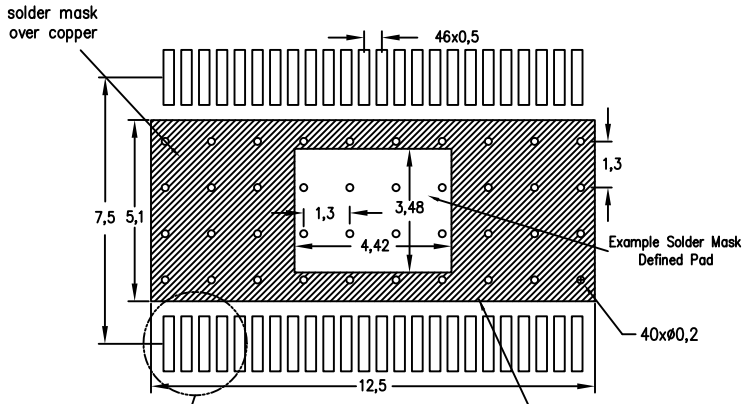
4206320–3/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

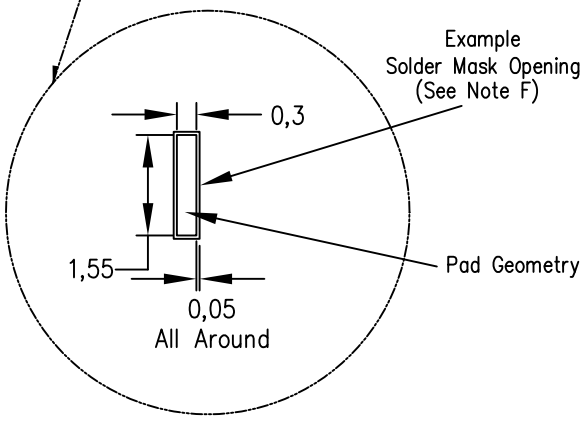
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

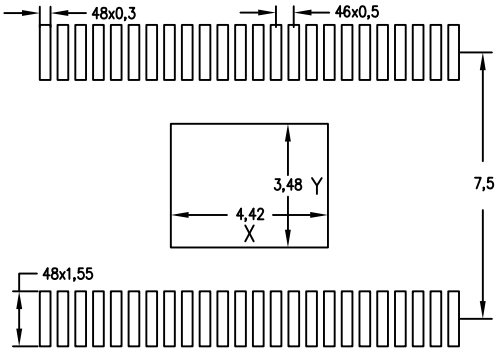


Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.98	3.92
0.127mm	4.42	3.48
0.152mm	4.04	3.18
0.178mm	3.73	2.94

4208546–2/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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