DRV1097512V 三相无传感器 BLDC 电机驱动器

1 特性

- 输入电压范围：6.5 至 18 V
- 总驱动器 H + L $r_{DS(on)}$：250mΩ
- 驱动电流：1.5A 持续绕组电流（峰值 2A）
- 无传感器专有反电动势 (BEMF) 控制方案
- 连续正弦 180° 换向
- 无需外部感应电阻
- 用户可通过添加外部感应电阻以灵活监视为电机提供的功率
- 灵活的用户接口选项：
  - I^2C 接口：访问命令和反馈寄存器
  - 专用的 SPEED 引脚：接受模拟或 PWM 输入
  - 专用的 FG 引脚：提供 TACH 反馈
  - 可通过 EEPROM 定制旋转曲线
  - 使用 DIR 引脚进行正向/反向控制
- 集成了降压稳压器，可高效地为内部和外部电路提供电压 (5V 或 3.3V)
- 待机版本 (DRV10975) 电源电流为 4.5mA
- 睡眠版本 (DRV10975Z) 电源电流为 80μA
- 过流保护
- 锁定检测
- 电压浪涌保护
- 欠压闭锁 (UVLO) 保护
- 热关断保护
- 耐热增强型 24 引脚散热薄型小外形尺寸 (HTSSOP)

2 应用

- 设备风扇
- 制热、通风与空调控制 (HVAC)

3 说明

DRV10975 器件是一款具有集成功率 MOSFET 的三相无传感器电机驱动器，可提供高达 1.5A 的持续驱动电流。该器件专为成本敏感型、低噪声、低外部组件数量应用而设计。

DRV10975 器件采用专有无传感器控制方案来提供持续正弦驱动，可大幅降低换向过程中通常会产生的纯音。该器件的接口设计简单而灵活。可直接通过 PWM、模拟、或 I^2C 输入控制电机。可通过 FG 引脚或 I^2C 提供电机速度反馈。

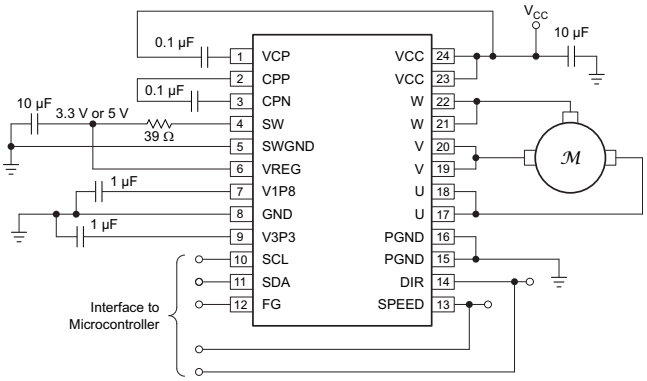
DRV10975 器件 采用了 一个集成降压稳压器，可高效地将电源电压降至 5V 或 3.3V，从而为内外部电路供电。该器件提供睡眠模式和待机模式两种型号，可在电机停止运转时实现节能。待机模式 (4.5mA) 型号会使稳压器保持运行，而休眠模式 (80μA) 型号会使稳压器停止工作。在使用稳压器为外部微控制器供电的 应用中使用待机模式型号。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV10975	HTSSOP (24)	7.80mm × 6.40mm
	VQFN (24)	5.00mm × 4.00mm
DRV10975Z	散热薄型小外形尺寸封装 (HTSSOP) (24)	7.80mm × 6.40mm
	VQFN (24)	5.00mm × 4.00mm

(1) 要了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

应用原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (March 2018) to Revision E — **Page**

- 删除了*器件信息* 表中两个器件的 VFQN 封装的“预告信息” ... 1
- Deleted the ADVANCE INFORMATION notation from the pinout drawing of the RHF package ... 5
- Deleted the ADVANCE INFORMATION table note from the *Pin Functions* table ... 5
- Changed ESD rating for RHF (VQFN) to match PWP (HTSSOP) package ... 6
- Deleted "Advance Info." from the RHF (VQFN) column of the *Thermal Information* table ... 7
- Changed time taken to drive motor after exiting from sleep mode from microseconds to milliseconds ... 9
- Changed text from BRKDontThr[2:0] to BRKDoneThr[2:0] to match actual register name ... 23
- Changed the caption for 图 42 ... 51
- Added a layout diagram for the VQFN package ... 52

Changes from Revision C (February 2018) to Revision D — **Page**

- 在*器件信息* 表中添加了新的封装 ... 1
- Added pin configuration diagram for RHF package ... 5
- Added pin number information for RHF package to the *Pin Functions* table ... 5
- Added ESD ratings for the RHF (VQFN) package ... 6
- Added a column to the *Thermal Information* table for the RHF package ... 7
- Added timing information for entering and exiting sleep mode and standby mode ... 9

Changes from Revision B (December 2017) to Revision C — **Page**

- Added BEMF COMPARATOR hysteresis specification ... 10
- Updated *Start the Motor Under Different Initial Conditions* figure ... 21
- Changed the default value for register address 0x27 from 0xFC to 0xF4 in the *Default EEPROM Value* table ... 43
- Deleted the "TI recommends..." sentence from the description for address 0x27, bit 3 ... 46

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- 已添加 constraints to recommended external inductor 49

Changes from Revision A (March 2017) to Revision B **Page**

- *在特性中指定驱动电流为持续绕组电流* 1
- Changed the $r_{DS(on)}$ maximum value from 1 Ω to 0.4 Ω and added typical value in the *Electrical Characteristics* table 8
- Added the internal SPEED pin pulldown resistance to ground parameter to the *Electrical Characteristics* table 9
- Changed the *Step-Down Regulator* section 14
- Updated the *Motor Phase Resistance* section 17
- 已删除 the *Inductive AVS Function* section 37
- Changed the default value for register address 0x29 from 0xB7 to 0xB8 in the *Default EEPROM Value* table 43
- 已添加 application information for the sleep mode device 48

Changes from Original (January 2015) to Revision A **Page**

- 已添加 在产品说明书标题和*器件信息* 表中添加了 DRV10975Z 部件号 1
- Corrected the link to the *DRV10983 and DRV10975 Tuning Guide* 17
- Added text to the *PWM Output* section 37
- Changed 图 36 38
- Changed "FGOLSet[1:0]" to "FGOLsel[1:0]" in *Register Map* address 0x2B 42
- Changed Supply Voltage regiser description 44
- Added recommended minimum dead time to SysOpt7 register 47
- Added *External Components* table 49
- Changed the link to the *DRV10983 and DRV10975 Tuning Guide* 49
- Changed the layout example 51

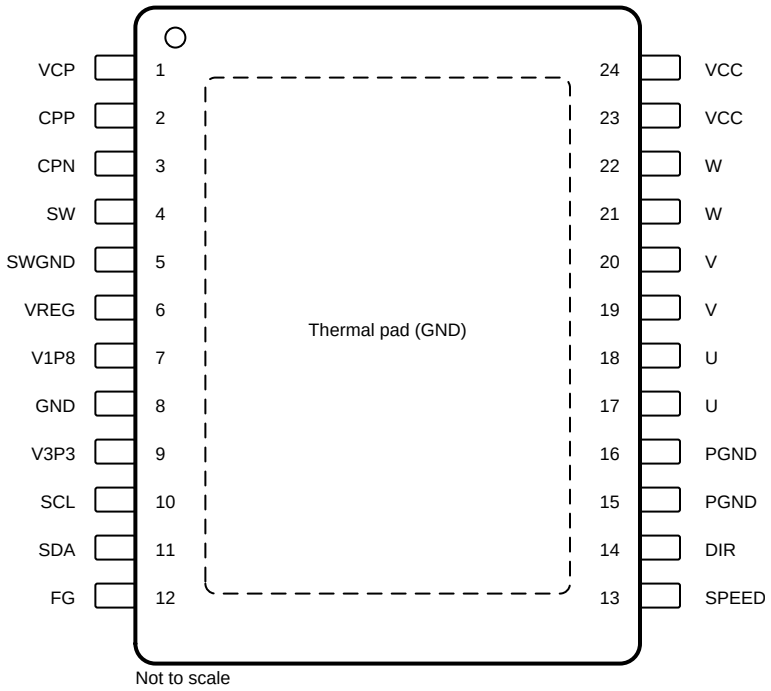
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5 说明 （续）

用户可通过 I²C 接口对寄存器中的特定电机参数进行重新编程并可对 EEPROM 进行编程，以帮助优化既定应用的性能。DRV10975 器件采用带有外露散热焊盘的高效散热型 HTSSOP 24 引脚封装。额定工作温度为 –40°C 至 125°C。

6 Pin Configuration and Functions

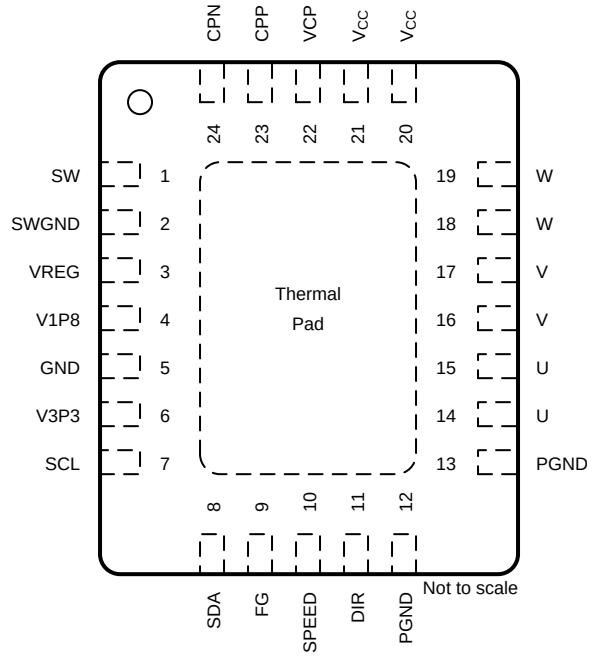
PWP PowerPAD™ Package
24-Pin HTSSOP With Exposed Thermal Pad
Top View



Not to scale

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RHF Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	HTSSOP	VQFN		
CPN	3	24	P	Charge pump pin 1, use a ceramic capacitor between CPN and CPP.
CPP	2	23	P	Charge pump pin 2, use a ceramic capacitor between CPN and CPP.
DIR	14	11	I	Direction
FG	12	9	O	FG signal output
GND	8	5	—	Digital and analog ground
PGND	15, 16	12, 13	P	Power ground
SCL	10	7	I	I^2C clock signal
SDA	11	8	I/O	I^2C data signal
SPEED	13	10	I	Speed control signal for PWM or analog input speed command
SW	4	1	O	Step-down regulator switching node output
SWGND	5	2	P	Step-down regulator ground
U	17, 18	14, 15	O	Motor U phase
V	19, 20	16, 17	O	Motor V phase
V1P8	7	4	P	Internal 1.8-V digital core voltage. V1P8 capacitor must connect to GND. This is an output, but not specified to drive external loads.
V3P3	9	6	P	Internal 3.3-V supply voltage. V3P3 capacitor must connect to GND. This is an output and may drive external loads not to exceed I_{V3P3_MAX}.
V_{CC}	23, 24	20, 21	P	Device power supply
VCP	1	22	P	Charge pump output
VREG	6	3	P	Step-down regulator output and feedback point
W	21, 22	18, 19	O	Motor W phase

(1) I = Input, O = Output, I/O = Input/output, P = Power

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Pin Functions (continued)

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	HTSSOP	VQFN		
Thermal pad (GND)	—	—	—	The exposed thermal pad must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2)	VCC	–0.3	23	V
	SPEED	–0.3	4	
	GND	–0.3	0.3	
	SCL, SDA	–0.3	4	
	DIR	–0.3	4	
Output voltage(2)	U, V, W	–1	23	V
	SW	–1	23	
	VREG	–0.3	7	
	FG	–0.3	4	
	VCP	–0.3	$V_{(VCC)}$ + 6	
	CPN	–0.3	23	
	CPP	–0.3	$V_{(VCC)}$ + 6	
	V3P3	–0.3	4	
	V1P8	–0.3	2.5	
Maximum junction temperature, T_{J_MAX}		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	VCC	6.5	12	18	V
Voltage	U, V, W	–0.7		19	V
	SCL, SDA, FG, SPEED, DIR	–0.1	3.3	3.6	
	PGND, GND	–0.1		0.1	
Current	Step-down regulator output current (buck mode)			100	mA
	Step-down regulator output current (linear mode)			0	
	V3P3 LDO output current			5	
Operating junction temperature, T_J		–40		125	°C

7.4 Thermal Information

THERMAL METRIC		DRV10975, DRV10975Z		UNIT
		RHF (VQFN)	PWP (HTSSOP)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.9	36.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.6	17.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	14.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.4	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	1.1	°C/W

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7.5 Electrical Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (DRV10975)						
I_{Vcc}	Supply current	T_A = 25°C; sleepDis = 1; SPEED = 0 V; $V_{(VCC)}$ = 12 V; buck regulator		5	7	mA
		T_A = 25°C; sleepDis = 1; SPEED = 0 V; $V_{(VCC)}$ = 12 V; linear regulator		11		
$I_{VccSTBY}$	Standby current	T_A = 25°C; SPEED = 0 V; $V_{(VCC)}$ = 12 V; standby mode device; buck regulator		4.5	6	mA
		T_A = 25°C; SPEED = 0 V; $V_{(VCC)}$ = 12 V; standby mode device; linear regulator		9		
SUPPLY CURRENT (DRV10975Z)						
I_{Vcc}	Supply current	T_A = 25°C; sleepDis = 1; SPEED = 0 V; Vcc = 12 V; buck regulator		5	7	mA
		T_A = 25°C; sleepDis = 1; SPEED = 0 V; Vcc = 12 V; linear regulator		11		
$I_{VccSLEEP}$	Sleep current	T_A = 25°C; SPEED = 0 V; $V_{(VCC)}$ = 12 V; sleep mode device		80	150	µA
UVLO						
V_{UVLO_R}	UVLO threshold voltage	Rise threshold, T_A = 25°C	5.2	5.6	6.5	V
V_{UVLO_F}	UVLO threshold voltage	Fall threshold, T_A = 25°C	5	5.5	5.8	V
V_{UVLO_HYS}	UVLO threshold voltage hysteresis	T_A = 25°C	100	200	400	mV
LDO OUTPUT						
V3P3		$V_{(VCC)}$ = 12 V, T_A = 25°C, VregSel = 0, 5-mA load	3	3.3	3.6	V
		$V_{(VCC)}$ = 12 V, T_A = 25°C, VregSel = 1, $V_{(VREG)}$ < 3.3 V, 5-mA load	$V_{(VREG)}$ – 0.3	$V_{(VREG)}$ – 0.1	$V_{(VREG)}$	
		$V_{(VCC)}$ = 12 V, T_A = 25°C, VregSel = 1, $V_{(VREG)}$ ≥ 3.3 V, 5-mA load	3	3.3	3.6	
I_{V3P3_MAX}	Maximum load from V3P3	$V_{(VCC)}$ = 12 V, T_A = 25°C		5		mA
V1P8		$V_{(VCC)}$ = 12 V, T_A = 25°C, VregSel = 0	1.6	1.78	2	V
		$V_{(VCC)}$ = 12 V, T_A = 25°C, VregSel = 1	1.6	1.78	2	
STEP-DOWN REGULATOR						
V_{REG}	Regulator output voltage	T_A = 25˚C; VregSel = 0, L_{SW} = 47 µH, C_{SW} = 10 µF, I_{load} = 50 mA	4.5	5	5.5	V
		T_A = 25˚C; VregSel = 1, L_{SW} = 47 µH, C_{SW} = 10 µF, I_{load} = 50 mA	3.06	3.4	3.6	
V_{REG_L}	Regulator output voltage (linear mode)	T_A = 25°C, VregSel = 0, R_{SW} = 39 Ω, C_{SW} = 10 µF		5		V
		T_A = 25°C, VregSel = 1, R_{SW} = 39 Ω, C_{SW} = 10 µF		3.4		
I_{REG_MAX}	Maximum load from V_{REG}	T_A = 25°C, L_{SW} = 47 µH, C_{SW} = 10 µF		100		mA
INTEGRATED MOSFET						
$r_{DS(on)}$	Series resistance (H + L)	T_A = 25˚C; $V_{(VCC)}$ = 12 V; $V_{(VCP)}$ = 17 V; Iout = 1 A		0.25	0.4	Ω
SPEED – ANALOG MODE						
V_{AN/A_FS}	Analog full-speed voltage			$V_{(V3P3)}$ × 0.9		V
V_{AN/A_ZS}	Analog zero-speed voltage			100		mV
t_{SAM}	Analog speed sample period			320		µs
V_{AN/A_RES}	Analog voltage resolution			5.8		mV
SPEED – PWM DIGITAL MODE						
V_{DIG_IH}	PWM input high voltage		2.2			V

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Electrical Characteristics (continued)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG_IL}	PWM input low voltage				0.6	V
f_{PWM}	PWM input frequency		1		100	kHz
STANDBY MODE (DRV10975)						
V_{EN_SB}	Analog voltage-to-enter standby mode	SpdCtrlMd = 0 (analog mode)	30			mV
V_{EX_SB}	Analog voltage-to-exit standby	SpdCtrlMd = 0 (analog mode)		120		mV
$t_{EX_SB_ANA}$	Time-to-exit from standby mode	SpdCtrlMd = 0 (analog mode) SPEED > V_{EX_SB}		700		ms
$t_{EX_SB_DR_ANA}$	Time taken to drive motor after exiting from standby mode	SpdCtrlMd = 0 (analog mode) SPEED > V_{EX_SB}; ISDen = 0; BrkDoneThr[2:0] = 0		1		µs
$t_{EX_SB_PWM}$	Time-to-exit from standby mode	SpdCtrlMd = 1 (PWM mode) SPEED > V_{DIG_IH}		1		µs
$t_{EX_SB_DR_PWM}$	Time taken to drive motor after exiting from standby mode	SpdCtrlMd = 1 (PWM mode) SPEED > V_{DIG_IH}; ISDen = 0; BrkDoneThr[2:0] = 0		55		ms
$t_{EN_SB_ANA}$	Time-to-enter standby mode	SpdCtrlMd = 0 (analog mode) SPEED < V_{EN_SB}; AvSIndEn = 0		5		ms
$t_{EN_SB_PWM}$	Time-to-enter standby mode	SpdCtrlMd = 1 (PMW mode) SPEED < V_{DIG_IL}; AvSIndEn = 0		60		ms
SLEEP MODE (DRV10975Z)						
V_{EN_SL}	Analog voltage-to-enter sleep	SpdCtrlMd = 0 (analog mode)	30			mV
V_{EX_SL}	Analog voltage-to-exit sleep	SpdCtrlMd = 0 (analog mode)	2.2	3.3		V
$t_{EX_SL_ANA}$	Time-to-exit from sleep mode	SpdCtrlMd = 0 (analog mode) SPEED > V_{EX_SL}		1		µs
$t_{EX_SL_DR_ANA}$	Time taken to drive motor after exiting from sleep mode	SpdCtrlMd = 0 (analog mode) SPEED > V_{EX_SL}; ISDen = 0; BrkDoneThr[2:0] = 0		350		ms
$t_{EX_SL_PWM}$	Time-to-exit from sleep mode	SpdCtrlMd = 1 (PWM mode) SPEED > V_{DIG_IH}		1		µs
$t_{EX_SL_DR_PWM}$	Time taken to drive motor after exiting from sleep mode	SpdCtrlMd = 1 (PWM mode) SPEED > V_{DIG_IH}; ISDen = 0; BrkDoneThr[2:0] = 0		350		ms
$t_{EN_SL_ANA}$	Time-to-enter sleep mode	SpdCtrlMd = 0 (analog mode) SPEED < V_{EN_SL}; AvSIndEn = 0		5.2		ms
$t_{EN_SL_PWM}$	Time-to-enter sleep mode	SpdCtrlMd = 1 (PMW mode) SPEED < V_{DIG_IL}; AvSIndEn = 0		58		ms
$R_{PD_SPEED_SL}$	Internal SPEED pin pulldown resistance to ground	V_{SPEED} = 0 (sleep mode)	55			kΩ
DIGITAL I/O (DIR INPUT AND FG OUTPUT)						
V_{DIR_H}	Input high		2.2			V
V_{DIR_L}	Input low				0.6	V
I_{FG_SINK}	Output sink current	Vout = 0.3 V	5			mA
I^2C SERIAL INTERFACE						
V_{I2C_H}	Input high		2.2			V
V_{I2C_L}	Input low				0.6	V
LOCK DETECTION RELEASE TIME						
t_{LOCK_OFF}	Lock release time			5		s
t_{LCK_ETR}	Lock enter time			0.3		s
OVERCURRENT PROTECTION						

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Electrical Characteristics (continued)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OC_limit}	Overcurrent protection	T_A = 25°C; phase to phase	2	4		A
THERMAL SHUTDOWN						
T_{SDN}	Shutdown temperature threshold	Shutdown temperature		150		°C
T_{SDN_HYS}	Shutdown temperature threshold	Hysteresis		10		°C
BEMF COMPARATOR						
$BEMF_{HYS}$	BEMF comparator hysteresis	bemfHsyEn = 1		50		mV

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7.6 Typical Characteristics

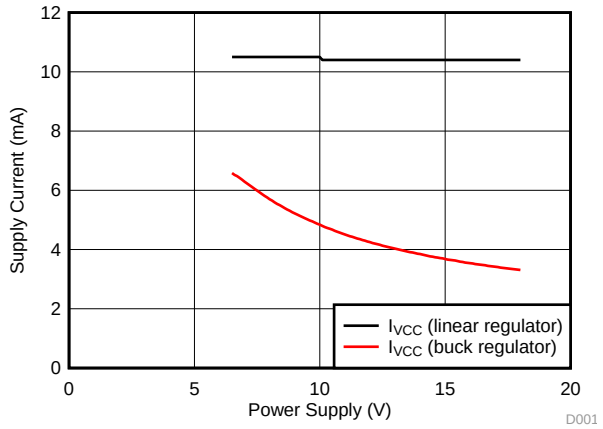


图 1. Supply Current vs Power Supply

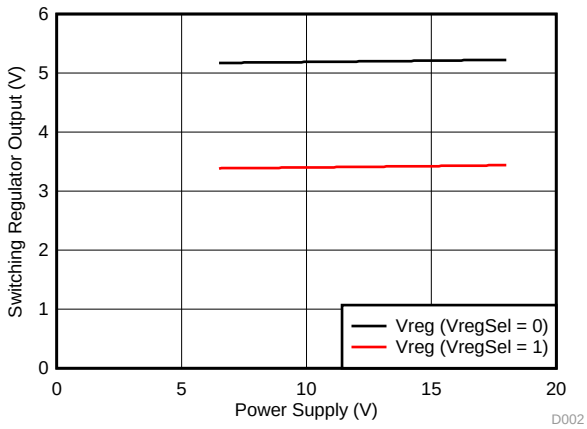


图 2. Step-down Regulator Output vs Power Supply

8 Detailed Description

8.1 Overview

The DRV10975 is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive current capability up to 1.5 A continuous. The device is specifically designed for low-noise, low external component count, 12-V motor drive applications. The device is configurable through a simple I^2C interface to accommodate different motor parameters and spin-up profiles for different customer applications.

A 180° sensorless control scheme provides continuous sinusoidal output voltages to the motor phases to enable ultra-quiet motor operation by keeping the electrically induced torque ripple small.

The DRV10975 features extensive protection and fault detect mechanisms to ensure reliable operation. Voltage surge protection prevents the input Vcc capacitor from overcharging, which is typical during motor deceleration. The devices provides overcurrent protection without the need for an external current sense resistor. Rotor lock detect is available through several methods. These methods can be configured with register settings to ensure reliable operation. The device provides additional protection for undervoltage lockout (UVLO) and for thermal shutdown.

The commutation control algorithm continuously measures the motor phase current and periodically measures the VCC supply voltage. The device uses this information for BEMF estimation, and the information is also provided through the I^2C register interface for debug and diagnostic use in the system, if desired.

A buck step-down regulator efficiently steps down the supply voltage. The output of this regulator provides power for the internal circuits and can also be used to provide power for an external circuit such as a microcontroller. If providing power for an external circuit is not necessary (and to reduce system cost), configure the buck step-down regulator as a linear regulator by replacing the inductor with resistor.

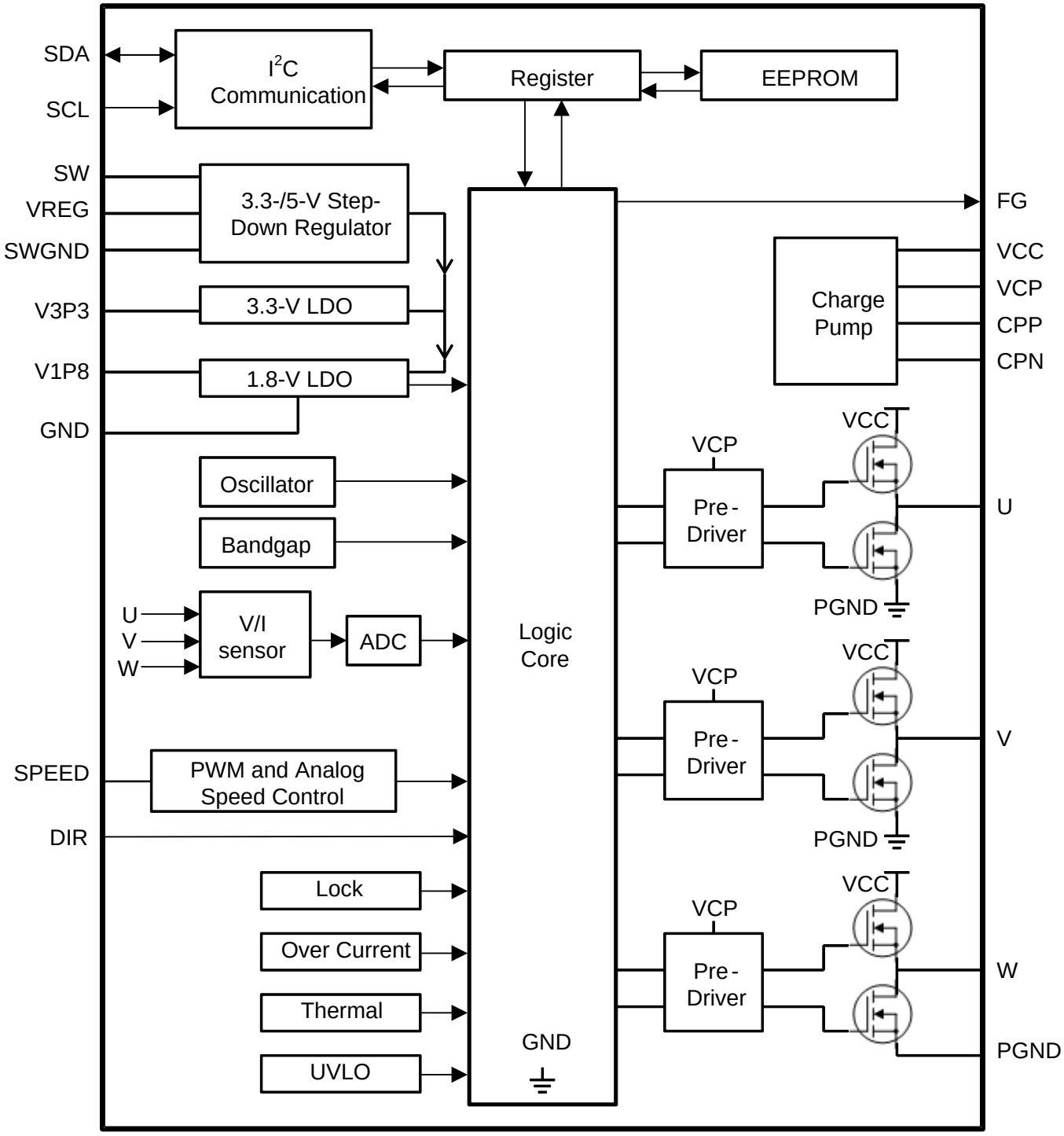
TI designed the interfacing to the DRV10975 to be flexible. In addition to the I^2C interface, the system can use the discrete FG pin, DIR pin, and SPEED pin. SPEED is the speed command input pin. It controls the output voltage amplitude. DIR is the direction control input pin. FG is the speed indicator output, which shows the frequency of the motor commutation.

EEPROM is integrated in the DRV10975 as memory for the motor parameter and operation settings. EEPROM data transfers to the register after power on and exit from sleep mode.

The DRV10975 device can also operate in register mode. If the system includes a microcontroller communicating through the I^2C interface, the device can dynamically update the motor parameter and operation settings by writing to the registers. In this configuration, the EEPROM data is bypassed by the register settings.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Regulators

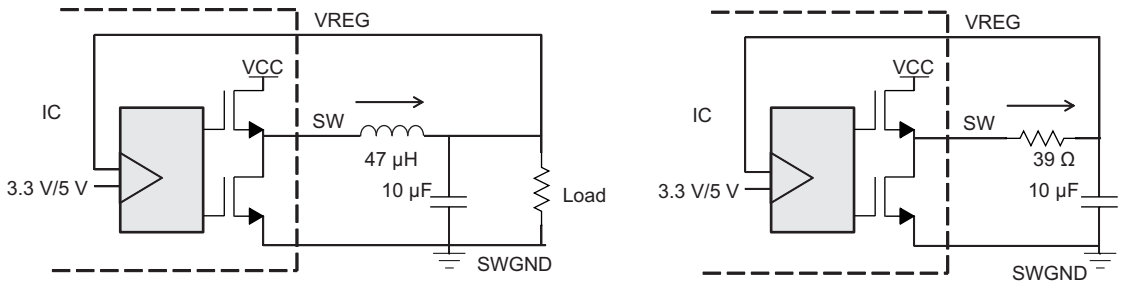
8.3.1.1 Step-Down Regulator

The DRV10975 includes a hysteretic step-down voltage regulator that can be operated as either a switching buck regulator using an external inductor or as a linear regulator using an external resistor (see 图 3). The best efficiency is achieved when the step-down regulator is in buck mode. However, the DRV10975Z device (sleep mode version) only operates with the step-down regulator in linear mode and with a Zener diode as described in the *Typical Application* section. The regulator output voltage can be configured by register bit VregSel. When VregSel = 0, the regulator output voltage is 5 V, and when VregSel = 1, the regulator output voltage is 3.3 V. When the regulated voltage drops by the hysteresis level, the high-side FET turns on to increase the regulated voltage back to the target of 3.3 V or 5 V. The switching frequency of the hysteretic regulator is not constant and changes with the load.

If the step-down regulator is configured in buck mode, see I_{REG_MAX} in the *Electrical Characteristics* to determine the amount of current provided for external load. If the step-down regulator is configured as linear mode, it is used for the device internal circuit only.

注

The DRV10975Z step-down regulator only operates in linear mode (using an external resistor) and with a Zener diode as described in the *Typical Application* section. The DRV10975Z device does not support buck mode (using an external inductor) as shown in 图 3.



Step-Down Regulator With External Inductor (Buck Mode)

Step-Down Regulator With External Resistor (Linear Mode)

图 3. Step-Down Regulator Configurations

8.3.1.2 3.3-V and 1.8-V LDO

The DRV10975 includes a 3.3-V LDO and an 1.8-V LDO. The 1.8-V LDO is for internal circuit only. The 3.3-V LDO is mainly for internal circuits, but can also drive external loads not to exceed I_{V3P3_MAX} listed in the *Electrical Characteristics*. For example, it can work as a pullup voltage for the FG, DIR, SDA, and SCL interface.

Both V1P8 and V3P3 capacitor must be connected to GND.

8.3.2 Protection Circuits

8.3.2.1 Thermal Shutdown

The DRV10975 has a built-in thermal shutdown function, which shuts down the device when junction temperature is more than T_{SDN} °C and recovers operating conditions when junction temperature falls to $T_{SDN} - T_{SDN_HYS}$°C.

The OverTemp status bit (address 0x10 bit 7) is set during thermal shutdown.

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Feature Description (接下页)

8.3.2.2 Undervoltage Lockout (UVLO)

The DRV10975 has a built-in UVLO function block. The hysteresis of UVLO threshold is $V_{UVLO-HYS}$. The device is locked out when VCC is down to V_{UVLO_F} and woke up at V_{UVLO_R}.

8.3.2.3 Overcurrent Protection (OCP)

The overcurrent protection function acts to protect the device if the current, as measured from the FETs, exceeds the $I_{OC-limit}$ threshold. It protects the device in the short-circuit condition if by accident a phase shorts to GND, or to another phase; the DRV10975 places the output drivers into a high-impedance state and maintains this condition until the overcurrent is no longer present. The OverCurr status bit (address 0x10 bit 5) is set.

The DRV10975 also provides acceleration current limit and lock detection current limit functions to protect the device and motor (see *Current Limit* and *Lock Detect and Fault Handling*).

8.3.2.4 Lock

When the motor is blocked or stopped by an external force, the lock protection is triggered, and the device stops driving the motor immediately. After the lock release time t_{LOCK_OFF}, the DRV10975 resumes driving the motor again. If the lock condition is still present, it enters the next lock protection cycle until the lock condition is removed. With this lock protection, the motor and device does not get overheated or damaged due to the motor being locked (see *Lock Detect and Fault Handling*).

During lock condition, the MtrLck Status bit (address 0x10, bit 4) is set. To further diagnose, check the register FaultCode.

8.3.3 Motor Speed Control

The DRV10975 offers four methods for indirectly controlling the speed of the motor by adjusting the output voltage amplitude. This can be accomplished by varying the supply voltage (V_{CC}) or by controlling the Speed Command. The Speed Command can be controlled in one of three ways. The user can set the Speed Command on the SPEED pin by adjusting either the PWM input (SPEED pin configured for PWM mode) or the analog input (SPEED pin configured for analog mode), or by writing the Speed Command directly through the I^2C serial port to SpdCtrl[8:0]. The Speed Command is used to determine the PWM duty cycle output (PWM_DCO) (see 图 4).

The Speed Command may not always be equal to the PWM_DCO because DRV10975 has implemented the AVS function (see *AVS Function*), the acceleration current limit function (see *Acceleration Current Limit*), and the closed loop accelerate function (see *Closed Loop Accelerate*) to optimize the control performance. These functions can limit the PWM_DCO, which affects the output amplitude.

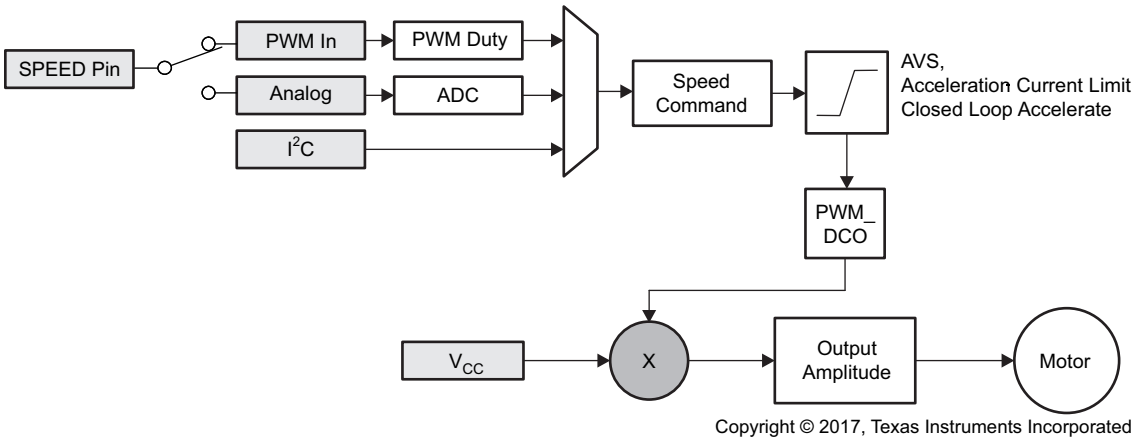


图 4. Multiplexing the Speed Command to the Output Amplitude Applied to the Motor

The output voltage amplitude applied to the motor is accomplished through sine wave modulation so that the phase-to-phase voltage is sinusoidal.

Feature Description (接下页)

When any phase is measured with respect to ground, the waveform is sinusoidally coupled with third-order harmonics. This encoding technique permits one phase to be held at ground while the other two phases are pulse-width modulated. 图 5 and 图 6 show the sinusoidal encoding technique used in the DRV10975.

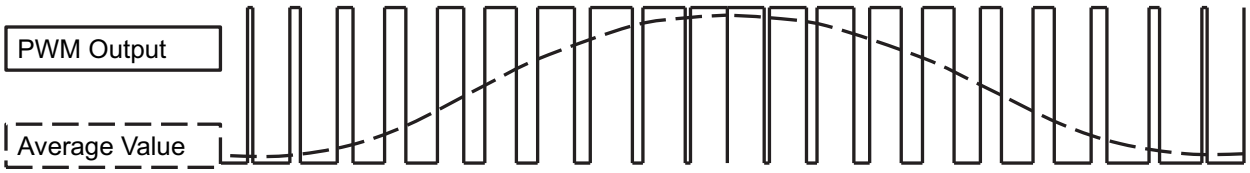
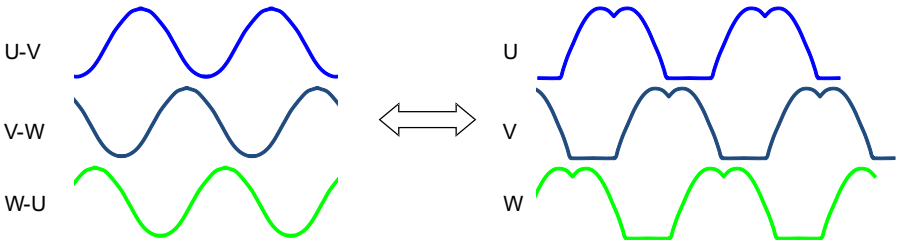


图 5. PWM Output and the Average Value



Sinusoidal voltage from phase to phase

Sinusoidal voltage with third order harmonics from phase to GND

图 6. Representing Sinusoidal Voltages With Third-Order Harmonic Output

The output amplitude is determined by the magnitude of V_{CC} and the PWM duty cycle output (PWM_DCO). The PWM_DCO represents the peak duty cycle that is applied in one electrical cycle. The maximum amplitude is reached when PWM_DCO is at 100%. The peak output amplitude is V_{CC}. When the PWM_DCO is at 50%, the peak amplitude is V_{CC} / 2 (see 图 7).

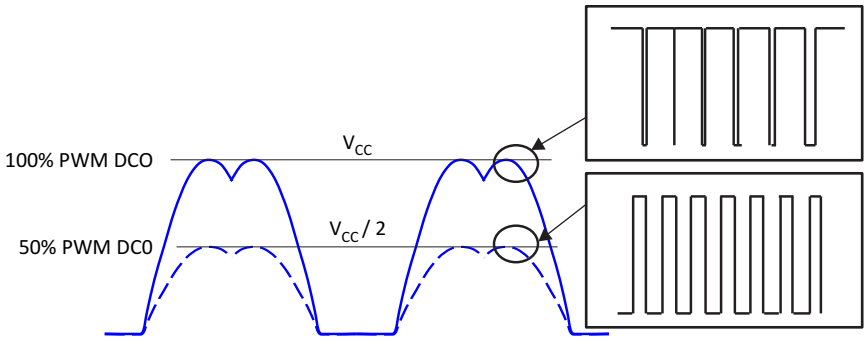


图 7. Output Voltage Amplitude Adjustment

8.3.4 Sleep or Standby Condition

The DRV10975 is available in either a sleep mode or standby mode version. The DRV10975 enters either sleep or standby to conserve energy. When the device enters either sleep or standby, the motor stops driving. The step-down regulator is disabled in the sleep mode version to conserve more energy. The I^2C interface is disabled and any register data not stored in EEPROM will be reset. The step-down regulator remains active in the standby mode version. The register data is maintained, and the I^2C interface remains active.

Setting sleepDis = 1 prevents the device from entering into the sleep or standby condition. If the device has already entered into sleep or standby condition, setting sleepDis = 1 will not take it out of the sleep or standby condition. During a sleep or standby condition, the Slp_Stdby status bit (address 0x10, bit 6) will be set.

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Feature Description (接下页)

For different speed command modes, 表 1 shows the timing and command to enter the sleep or standby condition.

表 1. Conditions to Enter or Exit Sleep or Standby Condition

SPEED COMMAND MODE	ENTER STANDBY CONDITION	ENTER SLEEP CONDITION	EXIT FROM STANDBY CONDITION	EXIT FROM SLEEP CONDITION
Analog	SPEED pin voltage < V_{EN_SB} for $t_{EN_SB_ANA}$	SPEED pin voltage < V_{EN_SL} for $t_{EN_SL_ANA}$	SPEED pin voltage > V_{EX_SB} for $t_{EX_SB_ANA}$	SPEED pin voltage > V_{EX_SL} for $t_{EX_SL_ANA}$
PWM	SPEED pin low (V < V_{DIG_IL}) for $t_{EN_SB_PWM}$	SPEED pin low (V < V_{DIG_IL}) for $t_{EN_SL_PWM}$	SPEED pin high (V > V_{DIG_IH}) for $t_{EX_SB_PWM}$	SPEED pin high (V > V_{DIG_IH}) for $t_{EX_SL_PWM}$
I^2C	SpdCtrl[8:0] is programmed as 0 for $t_{EN_SB_PWM}$	SpdCtrl[8:0] is programmed as 0 for $t_{EN_SL_PWM}$	SpdCtrl[8:0] is programmed as non-zero for $t_{EX_SB_PWM}$	SPEED pin high (V > V_{DIG_IH}) for $t_{EX_SL_PWM}$(PWM mode) or SPEED pin voltage > V_{EX_SL} for $t_{EX_SL_ANA}$ (Analog mode)

Note that using the analog speed command, a higher voltage is required to exit from the sleep condition than the standby condition. The I^2C speed command cannot take the device out of the sleep condition because I^2C communication is disabled during the sleep condition.

8.3.5 Non-Volatile Memory

The DRV10975 has 96-bits of EEPROM data, which are used to program the motor parameters as described in the *I^2C Serial Interface*.

The procedure for programming the EEPROM is as follows. TI recommends to perform the EEPROM programming without the motor spinning, power cycle after the EEPROM write, and read back the EEPROM to verify the programming is successful.

1. Set SIdata = 1.
2. Write the desired motor parameters into the corresponding registers (address 0x20:0x2B) (see *I^2C Serial Interface*).
3. Write 1011 0110 (0xB6) to enProgKey in the DevCtrl register.
4. Ensure that V_{CC} is at or above 22 V.
5. Write eeWrite = 1 in EECtrl register to start the EEPROM programming.

The programming time is about 24 ms, and eeWrite bit is reset to 0 when programming is done.

8.4 Device Functional Modes

This section includes the logic required to be able to reliably start and drive the motor. It describes the processes used in the logic core and provides the information needed to effectively configure the parameters to work over a wide range of applications.

8.4.1 Motor Parameters

For the motor parameter measurement, see the *DRV10983 and DRV10975 Tuning Guide*.

The motor phase resistance and the BEMF constant (Kt) are two important parameters used to characterize a BLDC motor. The DRV10975 requires these parameters to be configured in the register. The motor phase resistance is programmed by writing the values for Rm[6:0] in the MotorParam1 register. The BEMF constant is programmed by writing the values for Kt[6:0] in the MotorParam2 register.

8.4.1.1 Motor Phase Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap, R_{PH_CT} (see 图 8).

Device Functional Modes (接下页)

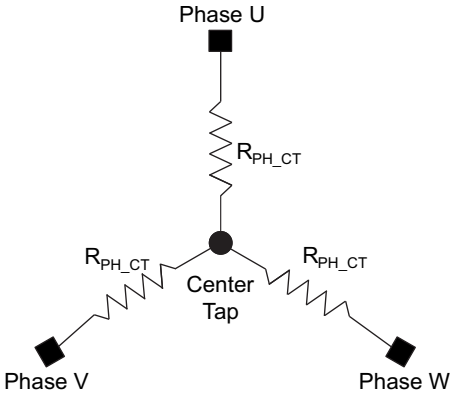


图 8. Wye-Connected Motor Phase Resistance

For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration, which is represented as R_Y. $R_{PH_CT} = R_Y$ (see 图 9).

For both the delta-connected motor and the wye-connected motor, calculating the equivalent R_{PH_CT} is easy by measuring the resistance between two phase terminals (R_{PH_PH}), and then dividing this value by two as shown in 公式 1.

$$R_{PH_CT} = ½R_{PH_PH} \quad (1)$$

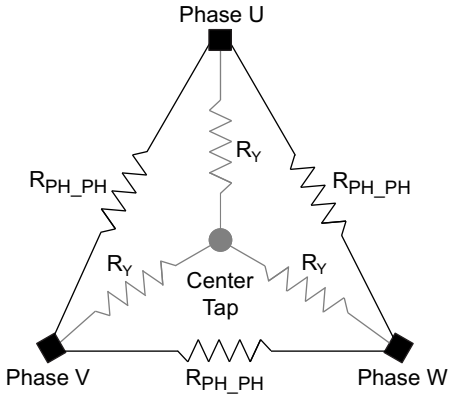


图 9. Delta-Connected Motor and the Equivalent Wye Connections

The motor phase resistance (R_{PH_CT}) must be converted to a 7-bit digital register value Rm[6:0] to program the motor phase resistance value. The digital register value can be determined as follows:

1. Convert the motor phase resistance (R_{PH_CT}) to a digital value where the LSB is weighted to represent 7.35 mΩ: Rmdig = R_{PH_CT} / 0.00735.
2. Encode the digital value such that Rmdig = Rm[3:0] << Rm[6:4].

The maximum resistor value, R_{PH_CT}, that can be programmed for the DRV10975 is 14.1 Ω, which represents Rmdig = 1920 and an encoded Rm[6:0] value of 0x7Fh. The minimum resistor the DRV10975 supports is 0.0294 Ω, R_{PH_CT}, which represents Rmdig = 4.

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Device Functional Modes (接下页)

For convenience, the encoded value for Rm[6:0] can also be obtained from 表 2.

表 2. Motor Phase Resistance Look-Up Table

R_{PH_CT} (Ω)	RM[6:0]	HEX	R_{PH_CT} (Ω)	RM[6:0]	HEX	R_{PH_CT} (Ω)	RM[6:0]	HEX
0	000 0000	00	0.235	010 1000	28	1.88	101 1000	58
0.0073	000 0001	01	0.264	010 1001	29	2.11	101 1001	59
0.0147	000 0010	02	0.294	010 1010	2A	2.35	101 1010	5A
0.0220	000 0011	03	0.323	010 1011	2B	2.58	101 1011	5B
0.0294	000 0100	04	0.352	010 1100	2C	2.82	101 1100	5C
0.0367	000 0101	05	0.382	010 1101	2D	3.05	101 1101	5D
0.0441	000 0110	06	0.411	010 1110	2E	3.29	101 1110	5E
0.0514	000 0111	07	0.441	010 1111	2F	3.52	101 1111	5F
0.0588	000 1000	08	0.47	011 1000	38	3.76	110 1000	68
0.0661	000 1001	09	0.529	011 1001	39	4.23	110 1001	69
0.0735	000 1010	0A	0.588	011 1010	3A	4.7	110 1010	6A
0.0808	000 1011	0B	0.646	011 1011	3B	5.17	110 1011	6B
0.0882	000 1100	0C	0.705	011 1100	3C	5.64	110 1100	6C
0.0955	000 1101	0D	0.764	011 1101	3D	6.11	110 1101	6D
0.102	000 1110	0E	0.823	011 1110	3E	6.58	110 1110	6E
0.110	000 1111	0F	0.882	011 1111	3F	7.05	110 1111	6F
0.117	001 1000	18	0.94	100 1000	48	7.52	111 1000	78
0.132	001 1001	19	1.05	100 1001	49	8.46	111 1001	79
0.147	001 1010	1A	1.17	100 1010	4A	9.4	111 1010	7A
0.161	001 1011	1B	1.29	100 1011	4B	10.3	111 1011	7B
0.176	001 1100	1C	1.41	100 1100	4C	11.2	111 1100	7C
0.191	001 1101	1D	1.52	100 1101	4D	12.2	111 1101	7D
0.205	001 1110	1E	1.64	100 1110	4E	13.1	111 1110	7E
0.22	001 1111	1F	1.76	100 1111	4F	14.1	111 1111	7F

8.4.1.2 BEMF Constant

The BEMF constant, Kt[6:0] describes the motors phase-to-phase BEMF voltage as a function of the motor velocity.

The measured BEMF constant (Kt) needs to be converted to a 7-bit digital register value Kt[6:0] to program the BEMF constant value. The digital register value can be determined as follows:

1. Convert the measured Kt to a weighted digital value: $Kt_{ph_dig} = 1442 \times Kt$
2. Encode the digital value such that $Kt_{ph_dig} = Kt[3:0] << Kt[4:6]$.

The maximum Kt that can be programmed is 1330 mV/Hz. This represents a digital value of 1920 and an encoded Kt[6:0] value of 0x7Fh. The minimum Kt that can be programmed is 0.7 mV/Hz, which represents a digital value of 1 and an encoded Kt[6:0] value of 0x01h.

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For convenience, the encoded value of Kt[6:0] may also be obtained from 表 3.

表 3. BEMF Constant Look-Up Table

Kt (mV/Hz)	Kt[6:0]	HEX	Kt (mV/Hz)	Kt [6:0]	HEX	Kt (mV/Hz)	Kt [6:0]	HEX
0	000 0000	00	22.3	010 1000	28	178	101 1000	58
0.7	000 0001	01	25.1	010 1001	29	200	101 1001	59
1.39	000 0010	02	27.8	010 1010	2A	223	101 1010	5A
2.09	000 0011	03	30.6	010 1011	2B	245	101 1011	5B
2.78	000 0100	04	33.4	010 1100	2C	267	101 1100	5C
3.48	000 0101	05	36.2	010 1101	2D	290	101 1101	5D
4.18	000 0110	06	39	010 1110	2E	312	101 1110	5E
4.88	000 0111	07	41.8	010 1111	2F	334	101 1111	5F
5.57	000 1000	08	44.6	011 1000	38	356	110 1000	68
6.27	000 1001	09	50.2	011 1001	39	401	110 1001	69
6.97	000 1010	0A	55.7	011 1010	3A	446	110 1010	6A
7.66	000 1011	0B	61.3	011 1011	3B	490	110 1011	6B
8.36	000 1100	0C	66.9	011 1100	3C	535	110 1100	6C
9.06	000 1101	0D	72.5	011 1101	3D	580	110 1101	6D
9.76	000 1110	0E	78	011 1110	3E	624	110 1110	6E
10.4	000 1111	0F	83.6	011 1111	3F	669	110 1111	6F
11.1	001 1000	18	89.2	100 1000	48	713	111 1000	78
12.5	001 1001	19	100	100 1001	49	803	111 1001	79
13.9	001 1010	1A	111	100 1010	4A	892	111 1010	7A
15.3	001 1011	1B	122	100 1011	4B	981	111 1011	7B
16.7	001 1100	1C	133	100 1100	4C	1070	111 1100	7C
18.1	001 1101	1D	145	100 1101	4D	1160	111 1101	7D
19.5	001 1110	1E	156	100 1110	4E	1240	111 1110	7E
20.9	001 1111	1F	167	100 1111	4F	1330	111 1111	7F

8.4.2 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when the DRV10975 attempts to begin the start-up process. The motor may be stationary, or spinning in the forward or reverse directions. The DRV10975 includes a number of features to allow for reliable motor start under all of these conditions. 图 10 shows the motor start-up flow for each of the three initial motor states.

8.4.2.1 Case 1 – Motor Is Stationary

If the motor is stationary, the commutation logic must be initialized to be in phase with the position of the motor. The DRV10975 provides for two options to initialize the commutation logic to the motor position. Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors. The Align and Go technique forces the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase. The following sections explain how to configure these techniques for use in the designer's system.

8.4.2.2 Case 2 – Motor Is Spinning in the Forward Direction

If the motor is spinning forward with enough velocity, the DRV10975 may be configured to go directly into closed loop. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition.

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8.4.2.3 Case 3 – Motor Is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction, the DRV10975 provides several methods to convert it back to forward direction.

One method, reverse drive, allows the motor to be driven so that it accelerates through zero velocity. The motor achieves the shortest possible spin-up time in systems where the motor is spinning in the reverse direction.

If this feature is not selected, then the DRV10975 may be configured to either wait for the motor to stop spinning or brake the motor. After the motor has stopped spinning, the motor start-up sequence proceeds as it would for a motor which is stationary.

Take care when using the feature reverse drive or brake to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

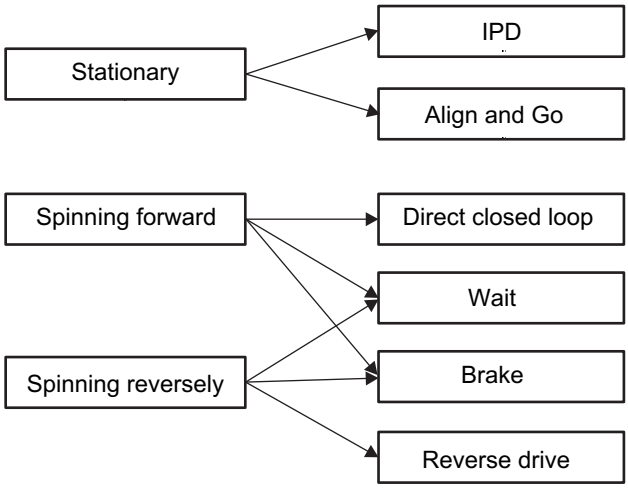


图 10. Start the Motor Under Different Initial Conditions

8.4.3 Motor Start Sequence

图 11 shows the motor start sequence implemented in the DRV10975.

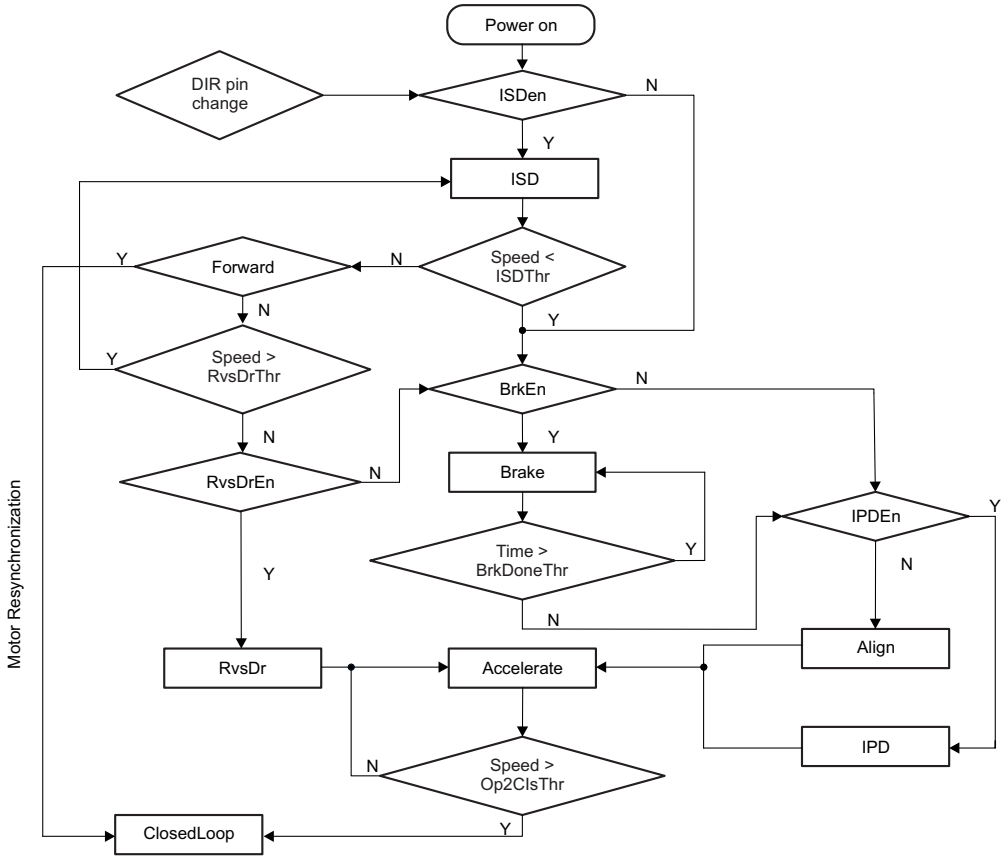


图 11. Motor Starting-Up Flow

Power-On State This is the initial power-on state of the motor start sequencer (MSS). The MSS starts in this state on initial power-up or whenever the DRV10975 comes out of either standby or sleep modes.

ISDen Judgment After power on, the DRV10975 MSS enters the ISDen Judgment where it checks to see if the Initial Speed Detect (ISD) function is enabled (ISDen = 1). If ISD is disabled, the MSS proceeds directly to the BrkEn Judgment. If ISD is enabled, the motor start sequence advances to the ISD state.

ISD State The MSS determines the initial condition of the motor (see *ISD*).

Speed<ISDThr Judgment If the motor speed is lower than the threshold defined by ISDThr[1:0], then the motor is considered to be stationary and the MSS proceeds to the BrkEn judgment. If the speed is greater than the threshold defined by ISDThr[1:0], the start sequence proceeds to the Forward judgment.

Forward Judgment The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the DRV10975 executes the resynchronization (see *Motor Resynchronization*) process by transitioning directly into the ClosedLoop state. If the motor is spinning in the reverse direction, the MSS proceeds to the Speed>RvsDrThr.

Speed>RvsDrThr Judgment The motor start sequencer checks to see if the reverse speed is greater than the threshold defined by RvsDrThr[2:0]. If it is, then the MSS returns to the ISD state to allow the motor to decelerate. This prevents the DRV10975 from attempting to reverse drive or brake a motor that is spinning too quickly. If the reverse speed of the motor is less than the threshold defined by RvsDrThr[2:0], then the MSS advances to the RvsDrEn judgment.

RvsDrEn Judgment The MSS checks to see if the reverse drive function is enabled (RvsDrEn = 1). If it is, the MSS transitions into the RvsDr state. If the reverse drive function is not enabled, the MSS

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advances to the BrkEn judgment.

RvsDr State The DRV10975 drives the motor in the forward direction to force it to rapidly decelerate (see *Reverse Drive*). When it reaches zero velocity, the MSS transitions to the Accelerate state.

BrkEn Judgment The MSS checks to determine whether the brake function is enabled (BrkDoneThr[2:0] ≠ 000). If the brake function is enabled, the MSS advances to the Brake state.

Brake State The device performs the brake function (see *Motor Brake*).

Time>BrkDoneThr Judgment The MSS applies brake for time configured by BRKDoneThr[2:0]. After brake state, the MSS advances to the IPDEn judgment.

IPDEn Judgment The MSS checks to see if IPD has been enabled (IPDCurrThr[3:0] ≠ 0000). If the IPD is enabled, the MSS transitions to the IPD state. Otherwise, it transitions to the align state.

Align State The DRV10975 performs align function (see *Align*). After the align completes, the MSS transitions to the Accelerate state.

IPD State The DRV10975 performs the IPD function. The IPD function is described in *Initial Position Detect (IPD)* . After the IPD completes, the MSS transitions to the Accelerate state.

Accelerate State The DRV10975 accelerates the motor according to the setting StAccel and StAccel2. After applying the accelerate settings, the MSS advances to the Speed > Op2ClsThr judgment.

Speed>Op2ClsThr Judgment The motor accelerates until the drive rate exceeds the threshold configured by the Op2ClsThr[4:0] settings. When this threshold is reached, the DRV10975 enters into the ClosedLoop state.

ClosedLoop State In this state, the DRV10975 drives the motor based on feedback from the commutation control algorithm.

DIR Pin Change Judgment If DIR pin get changed during any of above states, DRV10975 stops driving the motor and restarts from the beginning.

8.4.3.1 ISD

The ISD function is used to identify the initial condition of the motor. If the function is disabled, the DRV10975 does not perform the initial speed detect function and treats the motor as if it is stationary.

Phase-to-phase comparators are used to detect the zero crossings of the BEMF voltage of the motor while it is coasting (motor phase outputs are in high-impedance state). 图 12 shows the configuration of the comparators.

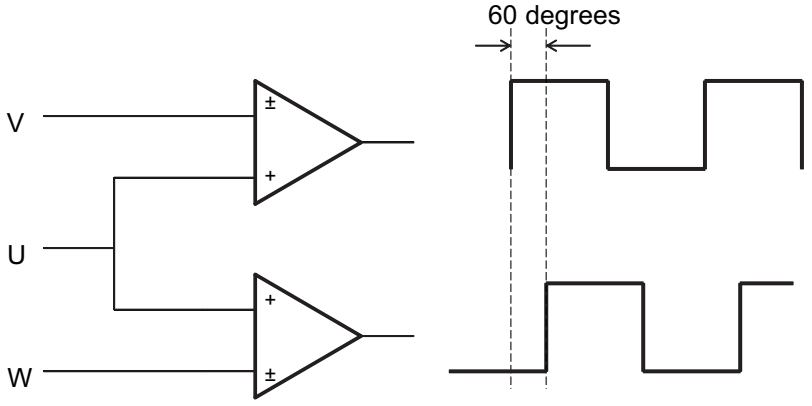


图 12. Initial Speed Detect Function

If the UW comparator output is lagging the UV comparator by 60°, the motor is spinning forward. If the UW comparator output is leading the UV comparator by 60°, the motor is spinning in reverse.

The motor speed is determined by measuring the time between two rising edges of either of the comparators.

If neither of the comparator outputs toggle for a given amount of time, the condition is defined as stationary. The amount of time can be programmed by setting the register bits ISDThr[1:0].

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8.4.3.2 Motor Resynchronization

The resynchronize function works when the ISD function is enabled and determines that the initial state of the motor is spinning in the forward direction. The speed and position information measured during ISD are used to initialize the drive state of the DRV10975, which can transition directly into the closed loop running state without needing to stop the motor.

8.4.3.3 Reverse Drive

The ISD function measures the initial speed and the initial position; the DRV10975 reverse drive function acts to reverse accelerate the motor through zero speed and to continue accelerating until the closed loop threshold is reached (see 图 13). If the reverse speed is greater than the threshold configured in RvsDrThr[1:0], then the DRV10975 waits until the motor coasts to a speed that is less than the threshold before driving the motor to reverse accelerate.

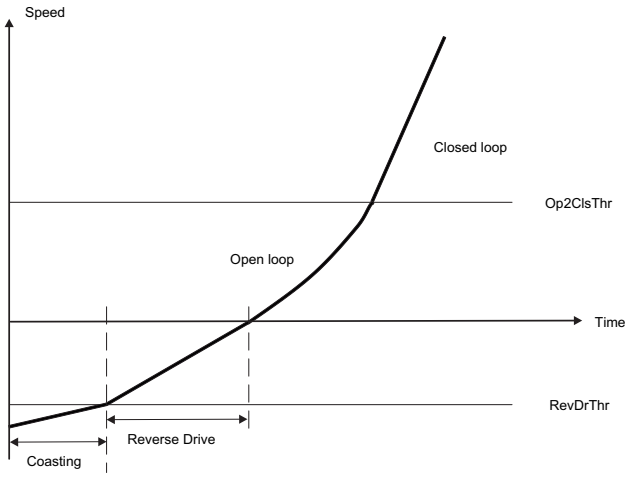


图 13. Reverse Drive Function

Reverse drive is suitable for applications where the load condition is light at low speed and relatively constant and where the reverse speed is low (that is, a fan motor with little friction). For other load conditions, the motor brake function provides a method for helping force a motor which is spinning in the reverse direction to stop spinning before a normal start-up sequence.

8.4.3.4 Motor Brake

The motor brake function can be used to stop the spinning motor before attempting to start the motor. The brake is applied by turning on all three of the low-side driver FETs.

If the motor is spinning at a speed that is greater than the braking threshold (configured by BrkDoneThr[2:0]), then dynamic braking acts to stop the spinning (whether forward or reverse). After the motor is stopped (that is, the motor speed is less than the BrkDoneThr[2:0]), the motor position is unknown. To proceed with restarting in the correct direction, the IPD or Align and Go algorithm needs to be implemented. The motor start sequence is the same as it would be for a motor starting in the stationary condition.

The motor brake function can be disabled. The motor skips the brake state and attempts to spin the motor as if it were stationary. If this happens while the motor is spinning in either direction, the start-up sequence may not be successful.

8.4.3.5 Motor Initialization

8.4.3.5.1 Align

The DRV10975 aligns a motor by injecting dc current through a particular phase pattern which is current flowing into phase V, flowing out from phase W for a certain time (configured by AlignTime[2:0]). The current magnitude is determined by OpenLCurr[1:0]. The motor should be aligned at the known position.

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The time of align affects the start-up timing (see *Start-Up Timing*). A bigger inertial motor requires longer align time.

8.4.3.5.2 Initial Position Detect (IPD)

The inductive sense method is used to determine the initial position of the motor when IPD is enabled. IPD is enabled by selecting IPDCurrThr[3:0] to any value other than 0000.

IPD can be used in applications where reverse rotation of the motor is unacceptable. Because IPD does not need to wait for the motor to align with the commutation, it can allow for a faster motor start sequence. IPD works well when the inductance of the motor varies as a function of position. Because it works by pulsing current to the motor, it can generate acoustics which must be taken into account when determining the best start method for a particular application.

8.4.3.5.2.1 IPD Operation

The IPD operates by sequentially applying voltage across two of the three motor phases according to the following sequence: VW WV UV VU WU UW (see 图 14). When the current reaches the threshold configured in IPDCurrThr[3:0], the voltage across the motor is stopped. The DRV10975 measures the time it takes from when the voltage is applied until the current threshold is reached. The time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

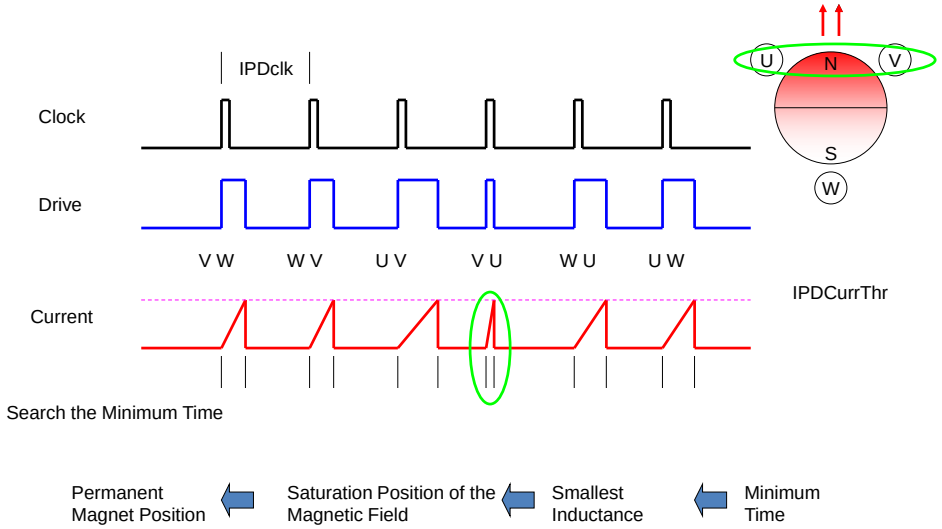


图 14. IPD Function

8.4.3.5.2.2 IPD Release Mode

Two options are available for stopping the voltage applied to the motor when the current threshold is reached. If IPDRlsMd = 0, the recirculate mode is selected. The low-side (S6) MOSFET remains on to allow the current to recirculate between the MOSFET (S6) and body diode (S2) (see 图 15). If IPDRlsMd = 1, the high-impedance (Hi-Z) mode is selected. Both the high-side (S1) and low-side (S6) MOSFETs are turned off and the current flies back across the body diodes into the power supply (see 图 16).

The high-impedance mode has a faster settle-down time, but could result in a surge on V_{CC}. Manage this with appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_{CC} and GND. If the voltage surge cannot be contained and if it is unacceptable for the application, then select the recirculate mode. When selecting the recirculate mode, select the IPDClk[1:0] bits to give the current in the motor windings enough time to decay to 0.

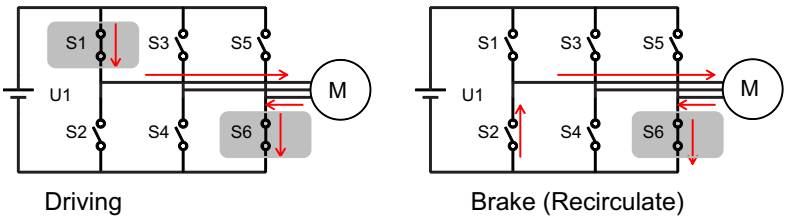


图 15. IPD Release Mode 0

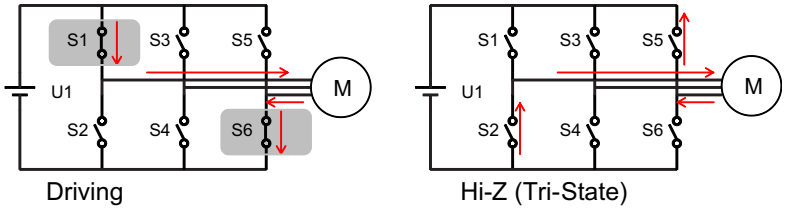


图 16. IPD Release Mode 1

8.4.3.5.2.3 IPD Advance Angle

After the initial position is detected, the DRV10975 begins driving the motor at an angle specified by IPDAdvcAgl[1:0].

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPDAdvcAgl[1:0] to allow for smooth acceleration in the application (see 图 17).

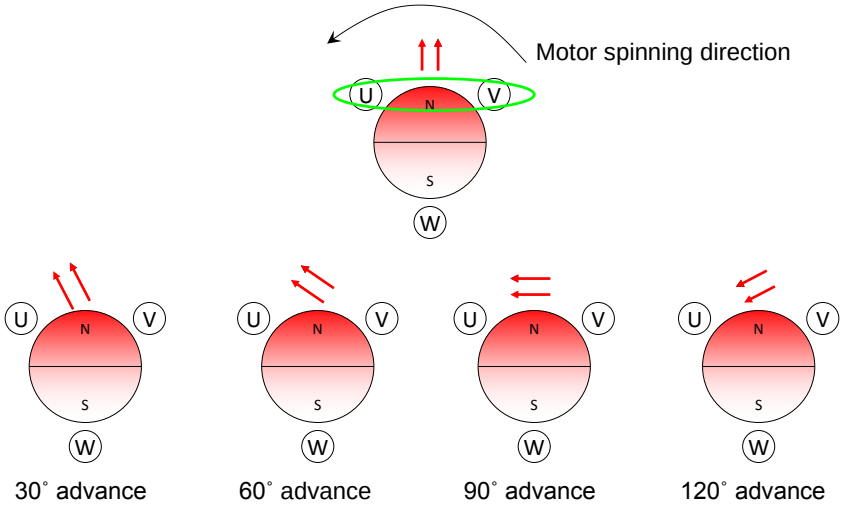


图 17. IPD Advance Angle

8.4.3.5.3 Motor Start

After it is determined that the motor is stationary and after completing the motor initialization with either align or IPD, the DRV10975 begins to accelerate the motor. This acceleration is accomplished by applying a voltage determined by the open loop current setting (OpenLCurr[1:0]) to the appropriate drive state and by increasing the rate of commutation without regard to the real position of the motor (referred to as open loop operation). The function of the open loop operation is to drive the motor to a minimum speed so that the motor generates sufficient BEMF to allow the commutation control logic to accurately drive the motor.

表 4 lists the configuration options that can be set in register to optimize the initial motor acceleration stage for different applications.

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表 4. Configuration Options for Controlling Open Loop Motor Start

Description	Reg Name	ConfigBits	Min Value	Max Value
Open to closed loop threshold	SysOpt4	Op2ClsThr[4:0]	0.8 Hz	204.8 Hz
Align time	SysOpt4	AlignTime[2:0]	40 ms	5.3 s
First order accelerate	SysOpt3	StAccel[2:0]	0.3 Hz/s	76 Hz/s
Second order accelerate	SysOpt3	StAccel2[2:0]	0.22 Hz/s2	57 Hz/s2
Open loop current setting	SysOpt2	OpenLCurr[1:0]	200 mA	1.6 A
Open loop current ramping	SysOpt2	OpLCurrRt[2:0]	0.23 V_{CC}/s	6 V_{CC}/s

8.4.3.6 Start-Up Timing

Start-up timing is determined by the align and accelerate time. The align time can be set by AlignTime[2:0], as described in *Register Definition* . The accelerate time is defined by the open-to-closed loop threshold Op2ClsThr[4:0] along with the first order StAccel[2:0](A1) and second order StAccel2[2:0](A2) acceleration coefficient. 图 18 shows the motor start-up process.

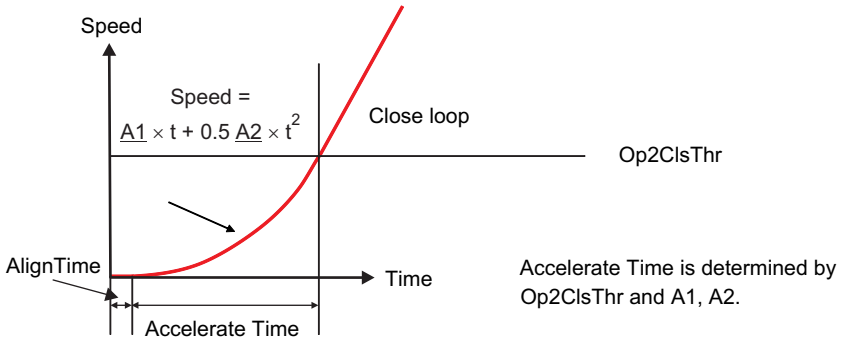


图 18. Motor Start-Up Process

Select the first order and second order acceleration coefficient to allow the motor to reliably accelerate from zero velocity up to the closed loop threshold in the shortest time possible. Using a slow acceleration coefficient during the first order accelerate stage can help improve reliability in applications where it is difficult to accurately initialize the motor with either align or IPD.

Select the open-to-closed loop threshold to allow the motor to accelerate to a speed that generates sufficient BEMF for closed loop control. This is determined by the velocity constant of the motor based on the relationship described in 公式 2.

$$BEMF = Kt \times speed\ (Hz) \quad (2)$$

8.4.4 Start-Up Current Setting

The start-up current setting is to control the peak start-up during open loop. During open loop operation, it is desirable to control the magnitude of drive current applied to the motor. This is helpful in controlling and optimizing the rate of acceleration. The limit takes effect during reverse drive, align, and acceleration.

The start current is set by programming the OpenLCurr[1:0] bits. The current should be selected to allow the motor to reliably accelerate to the handoff threshold. Heavier loads may require a higher current setting, but it should be noted that the rate of acceleration will be limited by the acceleration rate (StAccel[2:0], StAccel2[2:0]). If the motor is started with more current than necessary to reliably reach the handoff threshold, it results in higher power consumption.

The start current is controlled based on the relationship shown in 公式 3 and 图 19. The duty cycle applied to the motor is derived from the calculated value for U_{Limit} and the magnitude of the supply voltage, V_{CC}, as well as the drive state of the motor.

$$U_{Limit} = I_{Limit} \times Rm + Speed\,(Hz) \times Kt$$

where

- I_{Limit} is configured by OpenLCurr[1:0]

- Rm is configured by Rm[6:0]
- Speed is variable based open-loop acceleration profile of the motor
- Kt is configured by Kt[6:0] (3)

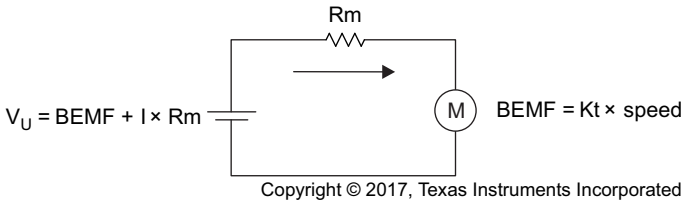


图 19. Motor Start-Up Current

8.4.4.1 Start-Up Current Ramp-Up

A fast change in the applied drive current may result in a sudden change in the driving torque. In some applications, this could result in acoustic noise. To avoid this, the DRV10975 allows the option of limiting the rate at which the current is applied to the motor. OpLCurrRt[2:0] sets the maximum voltage ramp up rate that will be applied to the motor. The waveforms in 图 20 show how this feature can be used to gradually ramp the current applied to the motor.



Start driving with fast current ramp

Start driving with slow current ramp

图 20. Motor Startup Current Ramp

8.4.5 Closed Loop

In closed loop operation, the DRV10975 continuously samples the current in the U phase of the motor and uses this information to estimate the BEMF voltage that is present. The drive state of the motor is controlled based on the estimated BEMF voltage.

8.4.5.1 Half Cycle Control and Full Cycle Control

The estimated BEMF used to control the drive state of the motor has two zero-crosses every electrical cycle. The DRV10975 can be configured to update the drive state either once every electrical cycle or twice for every electrical cycle. When AdjMode is programmed to 1, half cycle adjustment is applied. The control logic is triggered at both rising edge and falling edge. When AdjMode is programmed to 0, full cycle adjustment is applied. The control logic is triggered only at the rising edge (see 图 21).

Half cycle adjustment provides a faster response when compared with full cycle adjustment. Use half cycle adjustment whenever the application requires operation over large dynamic loading conditions. Use the full cycle adjustment for low current (<1 A) applications because it offers more tolerance for current measurement offset errors.

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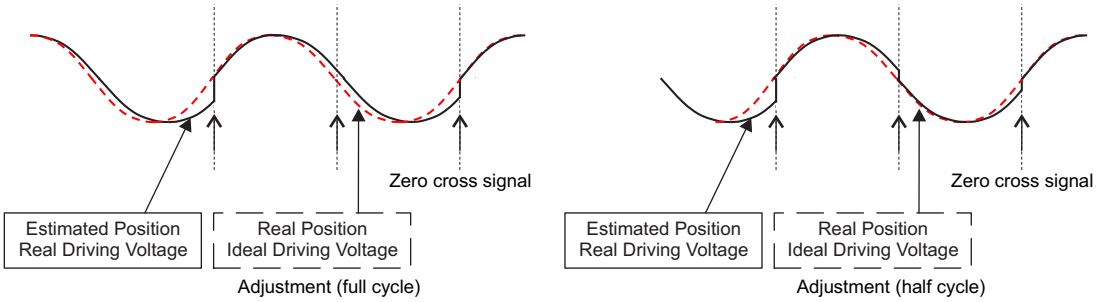


图 21. Closed Loop Control Commutation Adjustment Mode

8.4.5.2 Analog Mode Speed Control

The SPEED input pin can be configured to operate as an analog input (SpdCtrlMd = 0).

When configured for analog mode, the voltage range on the SPEED pin can be varied from 0 to V3P3. If SPEED > V_{ANA_FS}, the speed command is maximum. If V_{ANA_ZS} ≤ SPEED < V_{ANA_FS} the speed command changes linearly according to the magnitude of the voltage applied at the SPEED pin. If SPEED < V_{ANA_ZS} the speed command is to stop the motor. 图 22 shows the speed command when operating in analog mode.

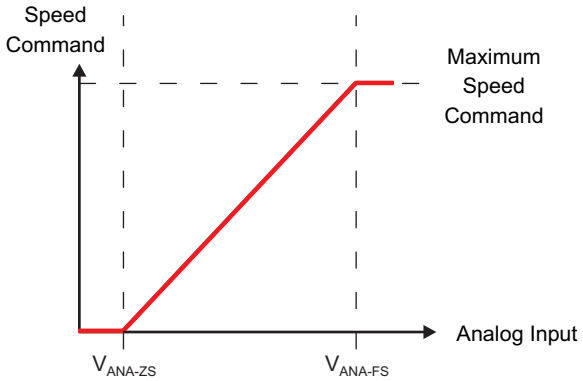


图 22. Analog Mode Speed Command

8.4.5.3 Digital PWM Input Mode Speed Control

If SpdCtrlMd = 1, the SPEED input pin is configured to operate as a PWM-encoded digital input. The PWM duty cycle applied to the SPEED pin can be varied from 0 to 100%. The speed command is proportional to the PWM input duty cycle. The speed command stops the motor when the PWM input keeps at 0 for $t_{EN_SL_PWM}$ (see 图 23).

The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM}. This is the frequency the device can accept to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phase. The PWM output frequency can be configured to be either 25 kHz when the DoubleFreq bit is set to 0 or to 50 kHz when DoubleFreq bit is set to 1.

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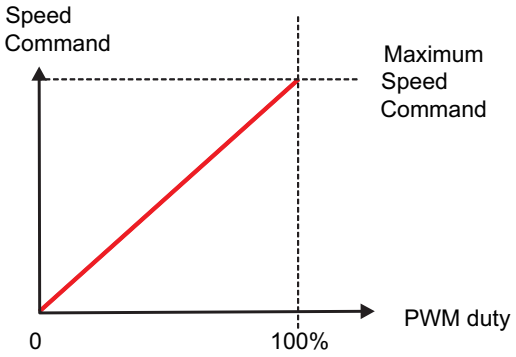


图 23. PWM Mode Speed Command

8.4.5.4 I²C Mode Speed Control

The DRV10975 can also command the speed through the I²C serial interface. To enable this feature, the OverRide bit is set to 1. When the DRV10975 is configured to operate in I²C mode, it ignores the signal applied to the SPEED pin.

The speed command can be set by writing the SpdCtrl[8] and SpdCtrl[7:0] bits. The 9-bit SpdCtrl [8:0] located in the SpeedCtrl1 and SpeedCntrl2 registers are used to set the peak amplitude voltage applied to the motor. The maximum speed command is set when SpdCtrl [8:0] is set to 0x1FF (511).

When SpdCtrl [8] is written to the SpeedCtrl2 register, the data is stored, but the output is not changed. When SpdCtrl [7:0] is written to the SpeedCtrl1 register, the speed command is updated (see 图 24).

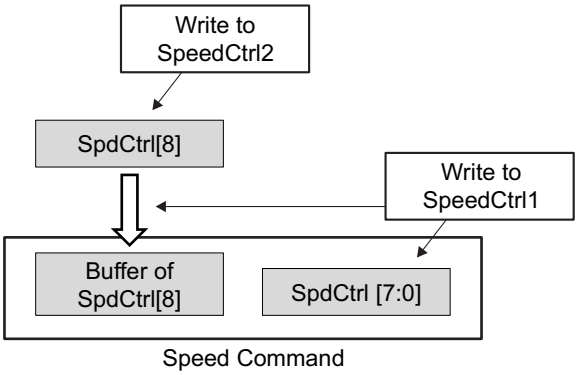


图 24. I²C Mode Speed Control

8.4.5.5 Closed Loop Accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the DRV10975 provides the option of limiting the maximum rate at which the speed command changes. ClsLpAccel[2:0] can be programmed to set the maximum rate at which the speed command changes (shown in 图 25).

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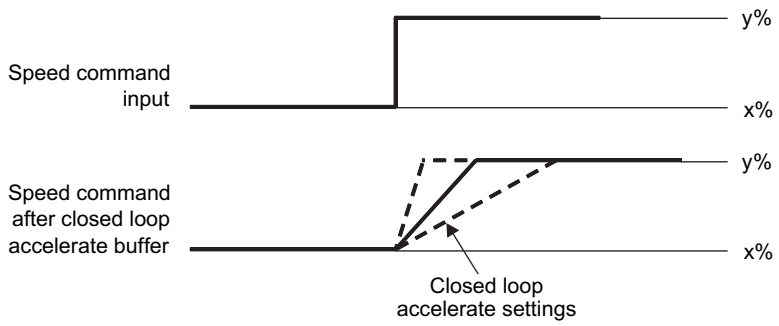


图 25. Closed-Loop Accelerate

8.4.5.6 Control Coefficient

The DRV10975 continuously measures the motor current and uses this information to control the drive state of the motor when operating in closed loop mode. In applications where noise makes it difficult to control the commutation optimally, the CtrlCoef[1:0] can be used to attenuate the feedback used for closed loop control. The loop will be less reactive to the noise on the feedback and provide for a smoother output.

8.4.5.7 Commutation Control Advance Angle

To achieve the best efficiency, it is often desirable to control the drive state of the motor so that the phase current of the motor is aligned with the BEMF voltage of the motor.

To align the phase current of the motor with the BEMF voltage of the motor, consider the inductive effect of the motor. The voltage applied to the motor should be applied in advance of the BEMF voltage of the motor (see 图 26). The DRV10975 provides configuration bits for controlling the time (t_{adv}) between the driving voltage and BEMF.

For motors with salient pole structures, aligning the motor BEMF voltage with the motor current may not achieve the best efficiency. In these applications, the timing advance should be adjusted accordingly. Accomplish this by operating the system at constant speed and load conditions and by adjusting the t_{adv} until the minimum current is achieved.

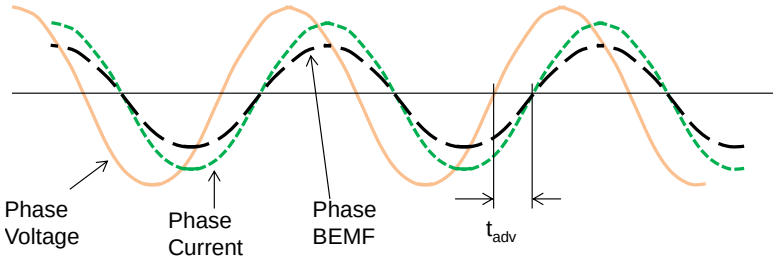


图 26. Advance Time (t_{adv}) Definition

The DRV10975 has two options for adjusting the motor commutate advance time. When CtrlAdvMd = 0, mode 0 is selected. When CtrlAdvMd = 1, mode 1 is selected.

Mode 0: t_{adv} is maintained to be a fixed time relative to the estimated BEMF zero cross as determined by 公式 4.

$$t_{adv} = t_{SETTING} \quad (4)$$

Mode 1: t_{adv} is maintained to be a variable time relative to the estimated BEMF zero cross as determined by 公式 5.

$$t_{adv} = t_{SETTING} \times (U\text{-}BEMF)/U. \quad (5)$$

where

- U is the phase voltage amplitude
- BEMF is phase BEMF amplitude

$t_{SETTING}$ (in µs) is determined by the configuration of the TCtrlAdv [6:4] and TCtrlAdv [3:0] bits as defined in 公式 6. For convenience, the available $t_{SETTING}$ values are provided in 表 5.

$$t_{SETTING} = 2.5\ \mu s \times [TCtrlAdv[3:0]] << TCtrlAdv[6:4] \quad (6)$$

表 5. Configuring Commutation Advance Timing by Adjusting $t_{SETTING}$

$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX	$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX	$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX
0	000 0000	00	80	010 1000	28	640	101 1000	58
2.5	000 0001	01	90	010 1001	29	720	101 1001	59
5	000 0010	02	100	010 1010	2A	800	101 1010	5A
7.5	000 0011	03	110	010 1011	2B	880	101 1011	5B
10	000 0100	04	120	010 1100	2C	960	101 1100	5C
12.5	000 0101	05	130	010 1101	2D	1040	101 1101	5D
15	000 0110	06	140	010 1110	2E	1120	101 1110	5E
17.5	000 0111	07	150	010 1111	2F	1200	101 1111	5F
20	000 1000	08	160	011 1000	38	1280	110 1000	68
22.5	000 1001	09	180	011 1001	39	1440	110 1001	69
25	000 1010	0A	200	011 1010	3A	1600	110 1010	6A
27.5	000 1011	0B	220	011 1011	3B	1760	110 1011	6B
30	000 1100	0C	240	011 1100	3C	1920	110 1100	6C
32.5	000 1101	0D	260	011 1101	3D	2080	110 1101	6D
35	000 1110	0E	280	011 1110	3E	2240	110 1110	6E
37.5	000 1111	0F	300	011 1111	3F	2400	110 1111	6F
40	001 1000	18	320	100 1000	48	2560	111 1000	78
45	001 1001	19	360	100 1001	49	2880	111 1001	79
50	001 1010	1A	400	100 1010	4A	3200	111 1010	7A
55	001 1011	1B	440	100 1011	4B	3520	111 1011	7B
60	001 1100	1C	480	100 1100	4C	3840	111 1100	7C
65	001 1101	1D	520	100 1101	4D	4160	111 1101	7D
70	001 1110	1E	560	100 1110	4E	4480	111 1110	7E
75	001 1111	1F	600	100 1111	4F	4800	111 1111	7F

8.4.6 Current Limit

The DRV10975 has several current limit modes to help ensure optimal control of the motor and to ensure safe operation. The various current limit modes are listed in 表 6. Acceleration current limit is used to provide a means of controlling the amount of current delivered to the motor. This is useful when the system needs to limit the amount of current pulled from the power supply during motor start-up. The lock detection current limit is a configurable threshold that can be used to limit the current applied to the motor. Overcurrent protection is used to protect the device; therefore, it cannot be disabled or configured to a different threshold. The current limit modes are described in the following sections.

表 6. DRV10975 Current Limit Modes

Current Limit Mode	Situation	Action	Fault Diagnose
Acceleration current limit	Motor start	Limit the output voltage amplitude	No fault
Lock detection current limit	Motor locked	Stop driving the motor and enter lock state	Mechanical rotation error
Overcurrent protection (OCP)	Short circuit	Stop driving and recover when OC signal disappeared	Circuit connection

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8.4.6.1 Acceleration Current Limit

The acceleration current limit limits the voltage applied to the motor to prevent the current from exceeding the programmed threshold. The acceleration current limit threshold is configured by writing the SWiLimitThr[3:0] bits to select I_{LIMIT}. The acceleration current limit does not use a direct measurement of current. It uses the programmed motor phase resistance, R_{PH_CT}, and programmed BEMF constant, Kt, to limit the voltage applied to the motor, U, as shown in 图 27 and 公式 7.

When the acceleration current limit is active, it does not stop the motor from spinning nor does it trigger a fault. The acceleration current limit function is only available in closed loop control.

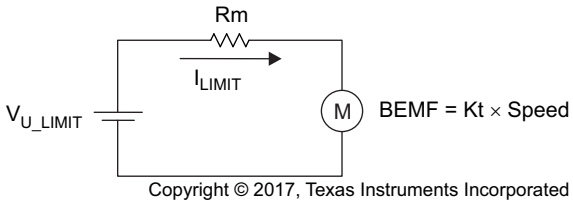


图 27. Acceleration Current Limit

$$U_{LIMIT} = I_{LIMIT} \times R_{PH_CT} + Speed \times Kt \quad (7)$$

8.4.7 Lock Detect and Fault Handling

The DRV10975 provides several options for determining if the motor becomes locked as a result of some external torque. Five lock detect schemes work together to ensure the lock condition is detected quickly and reliably. 图 28 shows the logic which integrates the various lock detect schemes. When a lock condition is detected, the DRV10975 device takes action to prevent continuously driving the motor in order to prevent damage to the system or the motor.

In addition to detecting if there is a locked motor condition, the DRV10975 also identifies and takes action if there is no motor connected to the system.

Each of the five lock-detect schemes and the no motor detection can be disabled by respective register bits LockEn[5:0].

When a lock condition is detected, the MtrLck in the Status register is set. The FaultCode register provides an indication of which of the six different conditions was detected on Lock5 to Lock0. These bits are reset when the motor restarts. The bits in the FaultCode register are set even if the lock detect scheme is disabled.

The DRV10975 reacts to either locked rotor or no motor connected conditions by putting the output drivers into a high-impedance state. To prevent the energy in the motor from pumping the supply voltage, the DRV10975 incorporates an anti-voltage-surge (AVS) process whenever the output stages transition into the high-impedance state. The AVS function is described in *AVS Function*. After entering the high-impedance state as a result of a fault condition, the system tries to restart after t_{LOCK_OFF}.

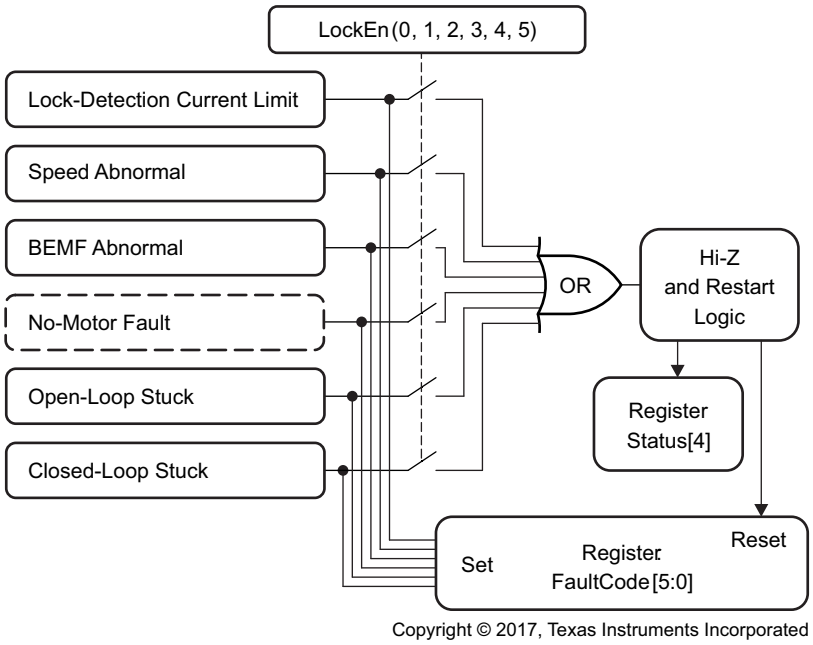


图 28. Lock Detect and Fault Diagnose

8.4.7.1 Lock0: Lock Detection Current Limit Triggered

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. This is often tripped in the event of a sudden locked rotor condition. The DRV10975 continuously monitors the current in the low-side drivers as shown in 图 29. If the current goes higher than the threshold configured by the HWiLimitThr[2:0] bits, then the DRV10975 stops driving the motor by placing the output phases into a high-impedance state. The MtrLck bit is set and a lock condition is reported. It retries after t_{LOCK_OFF}.

Set the lock detection current limit to a higher value than the acceleration current limit.

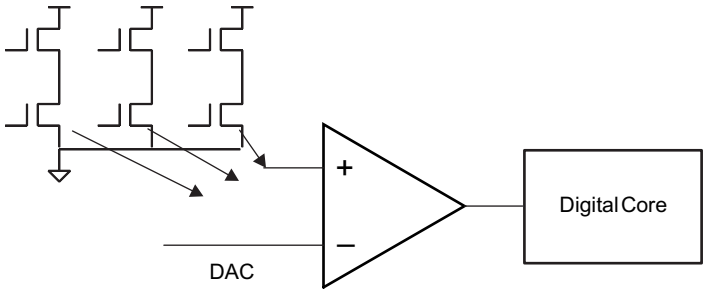
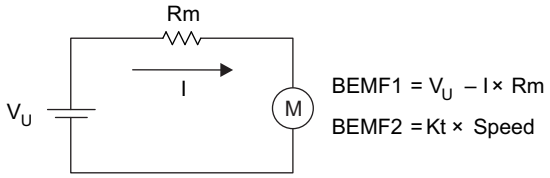


图 29. Lock Detection Current Limit

8.4.7.2 Lock1: Abnormal Speed

If motor is operating normally, the motor BEMF should always be less than output amplitude. The DRV10975 uses two methods of monitoring the BEMF in the system. The U phase current is monitored to maintain an estimate of BEMF based on the setting for Rm[6:0]. In addition, the BEMF is estimated based on the operation speed of the motor and the setting for Kt[6:0]. 图 30 shows the method for using this information to detect a lock condition. If motor BEMF is much higher than output amplitude for a certain period of time, t_{LCK_ETR}, it means the estimated speed is wrong, and the motor has gotten out of phase.

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图 30. Lock Detection 1

8.4.7.3 Lock2: Abnormal Kt

For any given motor, the integrated value of BEMF during half of an electrical cycle is constant. It is determined by BEMF constant (Kt) (see 图 31). It is true regardless of whether the motor is running fast or slow. This constant value is continuously monitored by calculation and used as criteria to determine the motor lock condition. It is referred to as Ktc.

Based on the Kt value programmed, create a range from Kt_low to Kt_high, if the Ktc goes beyond the range for a certain period of time, t_{LCK_ETR}, lock is detected. Kt_low and Kt_high are determined by KtLckThr[1:0] (see 图 32).

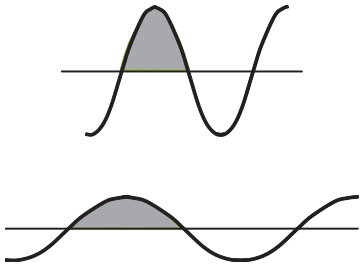


图 31. BEMF Integration

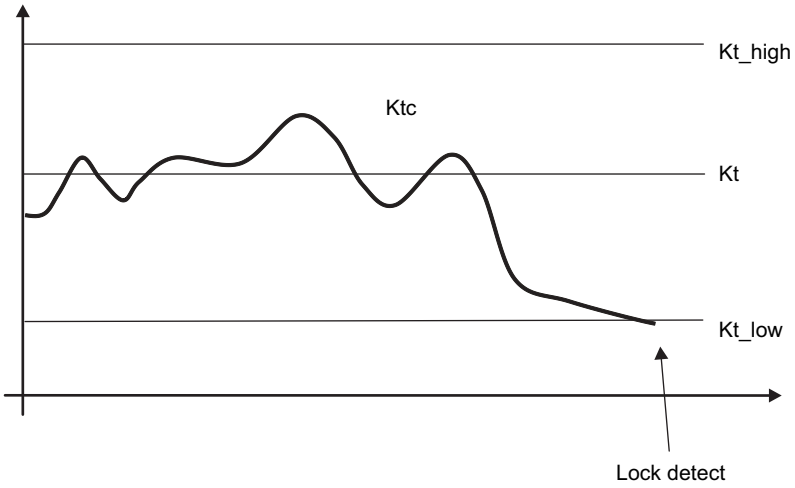


图 32. Abnormal Kt Lock Detect

8.4.7.4 Lock3 (Fault3): No Motor Fault

The phase U current is checked after transitioning from open loop to closed loop. If phase U current is not greater than 140 mA then the motor is not connected as shown in 图 33. This condition is treated and reported as a fault.

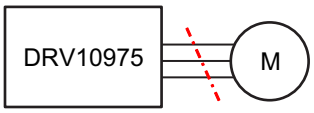


图 33. No Motor Error

8.4.7.5 Lock4: Open Loop Motor Stuck Lock

Lock4 is used to detect locked motor conditions while the motor start sequence is in open loop.

For a successful startup, motor speed should equal to open to closed loop handoff threshold when the motor is transitioning into closed loop. However, if the motor is locked, the motor speed is not able to match the open loop drive rate.

If the motor BEMF is not detected for one electrical cycle after the open loop drive rate exceeds the threshold, then the open loop was unsuccessful as a result of a locked rotor condition.

8.4.7.6 Lock5: Closed Loop Motor Stuck Lock

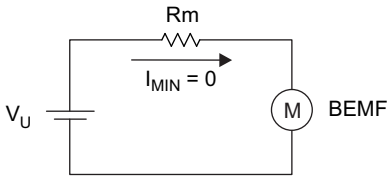
If the motor suddenly becomes locked, motor speed and Ktc are not able to be refreshed because motor BEMF zero cross may not appear after the lock. In this condition, lock can also be detected by the following scheme: if the current commutation period is 2× longer than the previous period.

8.4.8 AVS Function

When a motor is driven, energy is transferred from the power supply into it. Some of this energy is stored in the form of inductive energy or as mechanical energy. The DRV10975 includes circuits to prevent this energy from being returned to the power supply which could result in pumping up the V_{CC} voltage. This function is referred to as the AVS and acts to protect the DRV10975 as well as other circuits that share the same V_{CC} connection. Two forms of AVS protection are used to prevent both the mechanical energy or the inductive energy from being returned to the supply. Each of these modes can be independently disabled through the register configuration bits AVSMEn and AVSIndEn.

8.4.8.1 Mechanical AVS Function

If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_{CC} voltage surges. The mechanical AVS function works to prevent this from happening. The DRV10975 buffers the speed command value and limits the resulting output voltage, U_{MIN}, so that it is not less than the BEMF voltage of the motor. The BEMF voltage in the mechanical AVS function is determined using the programmed value for the Kt of the motor (Kt[6:0]) along with the speed. 图 34 shows the criteria used by the mechanical AVS function.



V_{U_MIN} = BEMF + I_{MIN} × Rm = BEMF

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图 34. Mechanical AVS

The mechanical AVS function can operate in one of two modes, which can be configured by the register bit AVSMMd:

AVSMMd = 0 – AVS mode is always active to prevent the applied voltage from being less than the BEMF voltage.

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AVSMMd = 1 – AVS mode becomes active when V_{CC} reaches 24 V. The motor acts as a generator and returns energy into the power supply until V_{CC} reaches 24 V. This mode can be used to enable faster deceleration of the motor in applications where returning energy to the power supply is allowed.

8.4.9 PWM Output

The DRV10975 has 16 options for PWM dead time which can be used to configure the time between one of the bridge FETs turning off and the complementary FET turning on. Deadtime[3:0] can be used to configure dead times between 40 ns and 640 ns. Take care that the dead time is long enough to prevent the bridge FETs from shooting through. The recommend minimum dead time is 400 ns for 24-V VCC and 360 ns for 12-V VCC.

The DRV10975 offers two options for PWM switching frequency. When the configuration bit DoubleFreq is set to 0, the output PWM frequency will be 25 kHz and when DoubleFreq is set to 1, the output PWM frequency will be 50 kHz.

8.4.10 FG Customized Configuration

The DRV10975 provides information about the motor speed through the frequency generate (FG) pin. FG also provides information about the driving state of the DRV10975.

8.4.10.1 FG Output Frequency

The FG output frequency can be configured by FGcycle[1:0]. The default FG toggles once every electrical cycle (FGcycle = 00). Many applications configure the FG output so that it provides two pulses for every mechanical rotation of the motor. The configuration bits provided in DRV10975 can accomplish this for 4-pole, 6-pole, 8-pole, and 12-pole motors, as shown in 图 35.

图 35 shows the DRV10975 has been configured to provide FG pulses once every electrical cycle (4 pole), twice every three electrical cycle (6 pole), once every two electrical cycles (8 pole), and once every three electrical cycles (12 pole).

Note that when it is set to 2 FG pulses every three electrical cycles, the FG output is not 50% duty cycle. Motor speed is able to be measured by monitoring the rising edge of the FG output.

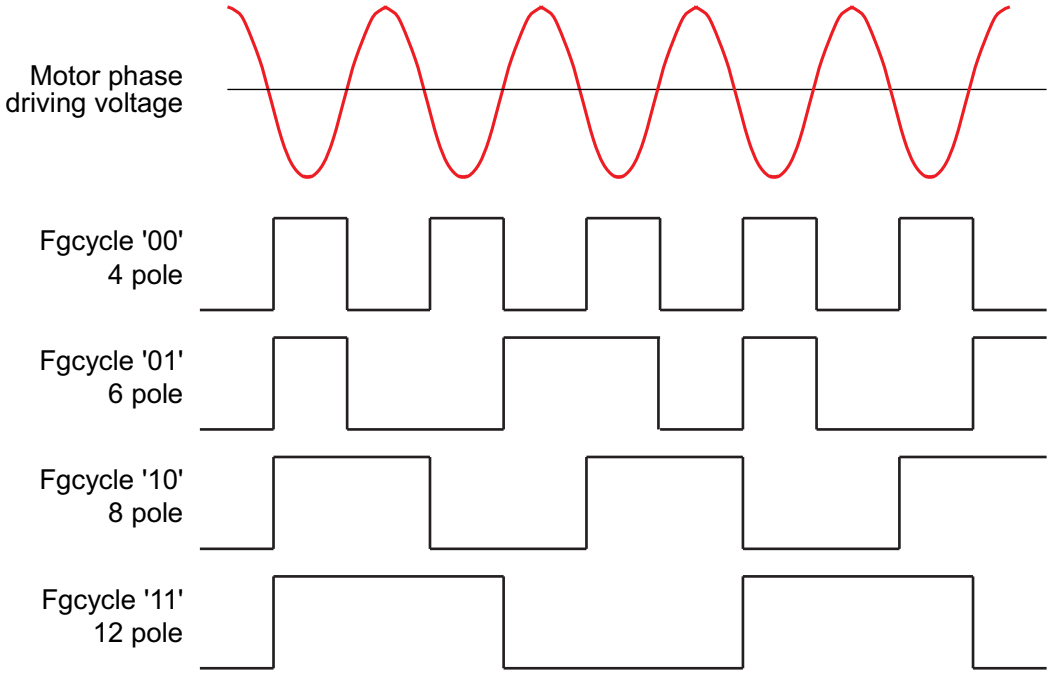


图 35. FG Frequency Divider

8.4.10.2 FG Open-Loop and Lock Behavior

Note that the FG output reflects the driving state of the motor. During normal closed loop behavior, the driving state and the actual state of the motor are synchronized. During open loop acceleration, however, this may not reflect the actual motor speed. During a locked motor condition, the FG output is driven high.

The DRV10975 provides three options for controlling the FG output during open loop as shown in 图 36. The selection of these options is determined by the FGOLsel[1:0] setting.

- Option0: Open loop output FG based on driving frequency
- Option1: Open loop no FG output (keep high)
- Option2: FG output based on driving frequency at the first power-on start-up, and no FG output (keep high) for any subsequent restarts

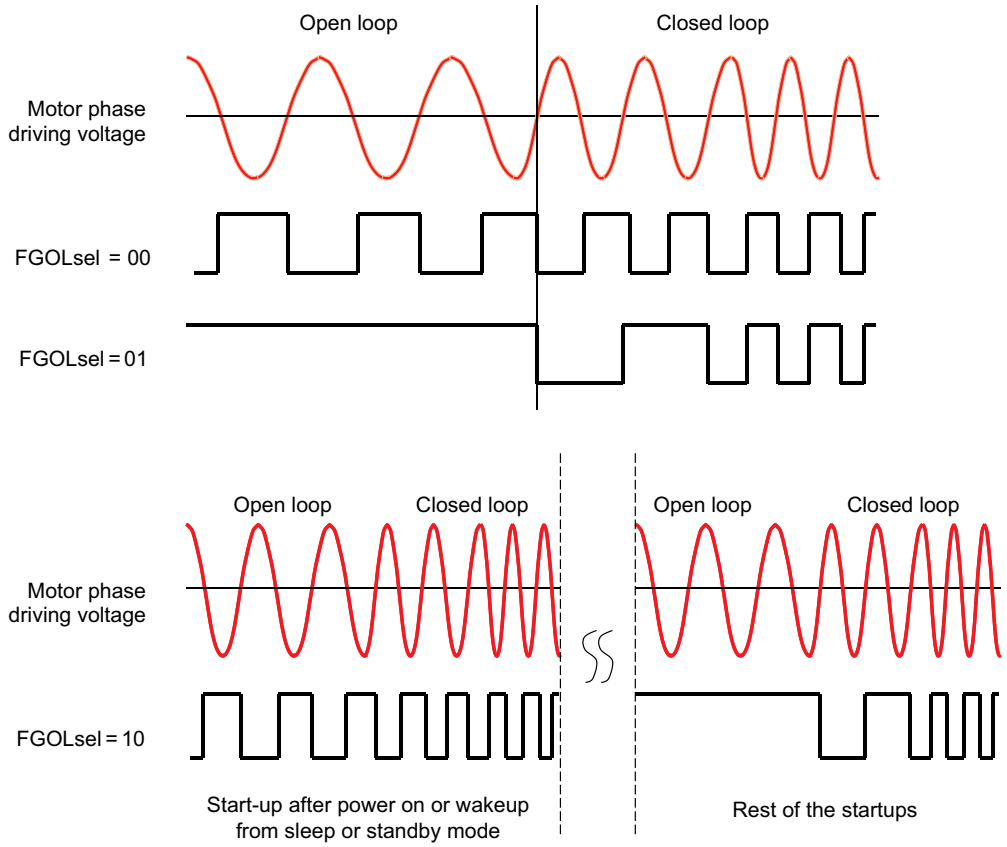


图 36. FG Behavior During Open Loop

8.4.11 Diagnostics and Visibility

The DRV10975 offers extensive visibility into the motor system operation conditions stored in internal registers. This information can be monitored through the I^2C interface. Information can be monitored relating to the device status, motor speed, supply voltage, speed command, motor phase voltage amplitude, fault status, and others. The data is updated on the fly.

8.4.11.1 Motor Status Readback

The motor status register provides information on overtemperature (OverTemp), sleep or standby state (Slp_Stdby), over current (OverCurr), and locked rotor (MtrLck).

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8.4.11.2 Motor Speed Readback

The motor operation speed is automatically updated in register MotorSpeed1 and MotorSpeed2 while the motor is spinning. MotorSpeed1 contains the 8 most significant bits and MotorSpeed2 contains the 8 least significant bits. The value is determined by the period for calculated BEMF zero crossings on phase U. The electrical speed of the motor is denoted as *Velocity (Hz)* and is calculated as shown in 公式 8.

Velocity (Hz) = {MotorSpeed1:MotorSpeed2} / 10 (8)

As an example consider the following:

MotorSpeed1 = 0x01;

MotorSpeed2 = 0xFF;

Velocity = 512 (0x01FF) / 10 = 51 Hz

For a 4-pole motor, this translates to: $51 \frac{\text{ecycles}}{\text{second}} \times \frac{1}{2} \frac{\text{mechcycle}}{\text{ecycle}} \times 60 \frac{\text{second}}{\text{minute}} = 1530 \text{ RPM}$

8.4.11.2.1 Two-Byte Register Readback

Several of the registers such as MotorSpeed report data that is contained in two registers.

To make sure that the data does not change between the reading of the first and second register reads, the DRV10975 implements a special scheme to synchronize the reading of MSB and LSB data. To ensure valid data is read when reading a two register value, use the following sequence.

1. Read the MSB.
2. Read the LSB.

图 37 shows the two-register readback circuit. When the MSB is read, the controller takes a snapshot of the LSB. The LSB data is stored in one extra register byte, which is shown as MotorSpeedBuffer[7:0]. When the LSB is read, the value of MotorSpeedBuffer[7:0] is sent.

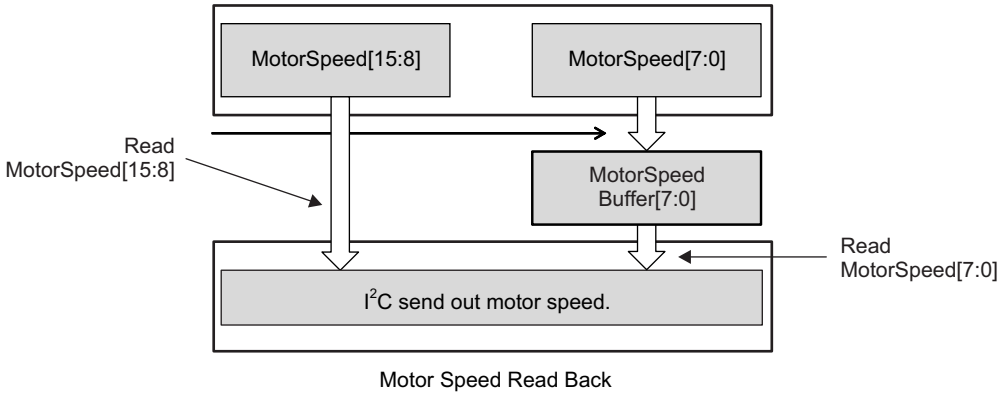


图 37. Two-Byte Register Readback

8.4.11.3 Motor Electrical Period Readback

The motor operation electrical period is automatically updated in register MotorPeriod1 and MotorPeriod2 while the motor is spinning. MotorPeriod1 is the MSB and MotorPeriod2 is the LSB. The electrical period is measured as the time between calculated BEMF zero crossings for phase U. The electrical period of the motor is denoted as d as t_{ELE_PERIOD} (µs) and is calculated as shown in 公式 9.

t_{ELE_PERIOD} (µs) = {MotorPeriod1:MotorPeriod2} × 10 (9)

As an example consider the following:

MotorPeriod1 = 0x01;

MotorPeriod2 = 0xFF;

t_{ELE_PERIOD} = 512 (0x01FF) × 10 = 5120 µs

The motor electrical period and motor speed satisfies the condition of 公式 10.

t_{ELE_PERIOD} (s) × Velocity (Hz) = 1 (10)

8.4.11.4 BEMF Constant Readback

For any given motor, the integrated value of BEMF during half of an electronic cycle will be constant, Ktc (see *Lock2: Abnormal Kt*).

The integration of the motor BEMF is processed periodically (updated every electrical cycle) while the motor is spinning. The result is stored in register MotorKt1 and MotorKt2.

The relationship is shown in 公式 11.

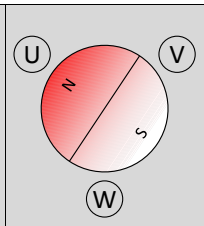
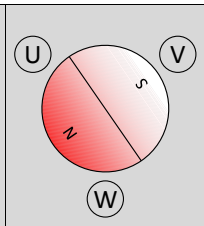
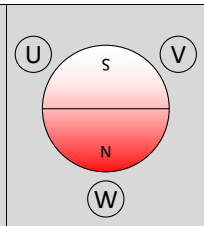
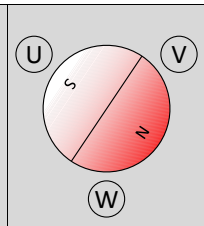
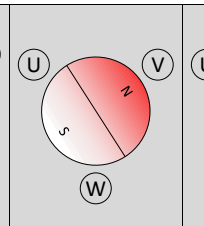
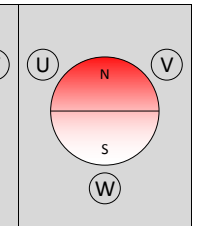
Ktc (V/Hz)= {MotorKt1:MotorKt2} / 2 /1442 (11)

8.4.11.5 Motor Estimated Position by IPD

After inductive sense is executed the rotor position is detected within 60 electrical degrees of resolution. The position is stored in register IPDPosition.

The value stored in IPD Position corresponds to one of the six motor positions plus the IPD Advance Angle as shown in 表 7. For more about information about IPD, see *Initial Position Detect (IPD)*.

表 7. IPD Position Readback

						
Rotor position (°)	0	60	120	180	240	300
Data1	0	43	85	128	171	213
IPD Advance Angle	30	60	90	120		
Data2	22	44	63	85		
Register date	(Data1 + Data2) mod (256)					

8.4.11.6 Supply Voltage Readback

The power supply is monitored periodically during motor operation. This information is available in register SupplyVoltage. The power supply voltage is recorded as shown in 公式 12.

$V_{POWERSUPPLY}$ (V) = Supply Voltage × 22.8 V / 256 (12)

8.4.11.7 Speed Command Readback

The DRV10975 converts the various types of speed command into a speed command value (SpeedCmd) as shown in 图 38. By reading SpeedCmd, the user can observe PWM input duty (PWM digital mode), analog voltage (analog mode), or I^2C data (I^2C mode). This value is calculated as shown in 公式 13.

公式 13 shows how the speed command as a percentage can be calculated and set in SpeedCmd.

$Duty_{SPEED}$ (%) = SpeedCmd × 100% / 255

where

- $Duty_{SPEED}$ = Speed command as a percentage
- SpeedCmd = Register value (13)

8.4.11.8 Speed Command Buffer Readback

If acceleration current limit and AVS are enabled, the PWM duty cycle output (read back at spdCmdBuffer) may not always match the input command (read back at SpeedCmd) shown in 图 38. See *AVS Function* and *Current Limit*.

By reading the value of spdCmdBuffer, the user can observe buffered speed command (output PWM duty cycle) to the motor.

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公式 14 shows how the buffered speed is calculated.

$$Duty_{OUTPUT}\ (\%) = spdCmdBuffer \times 100\% / 255 \quad (14)$$

where

- $Duty_{OUTPUT}$ = The maximum duty cycle of the output PWM, which represents the output amplitude in percentage.
- spdCmdBuffer = Register value

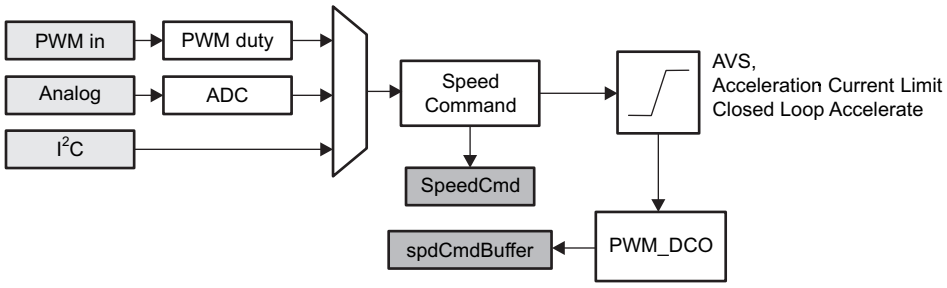


图 38. SpeedCmd and spdCmdBuffer Register

8.4.11.9 Fault Diagnostics

See *Lock Detect and Fault Handling*.

8.5 Register Maps

8.5.1 I²C Serial Interface

The DRV10975 provides an I²C slave interface with slave address 101 0010. TI recommends a pullup resistor 4.7 kΩ to 3.3 V for I²C interface port SCL and SDA.

Four read/write registers (0x00:0x03) are used to set motor speed and control device registers and EEPROM. Device operation status can be read back through 12 read-only registers (0x10:0x1E). Another 12 EEPROM registers (0x20:0x2B) can be accessed to program motor parameters and optimize the spin-up profile for the application.

8.5.2 Register Map

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
SpeedCtrl1 (1)	0x00	SpdCtrl[7:0]							
SpeedCtrl2 (1)	0x01	OverRide							SpdCtrl[8]
DevCtrl (1)	0x02	enProgKey[7:0]							
EECtrl (1)	0x03	sleepDis	SIdata	eeRefresh	eeWrite				
Status (2)	0x10	OverTemp	Slp_Stdby	OverCurr	MtrLck				
MotorSpeed1 (2)	0x11	MotorSpeed[15:8]							
MotorSpeed2 (2)	0x12	MotorSpeed[7:0]							
MotorPeriod1 (2)	0x13	MotorPeriod[15:8]							
MotorPeriod2 (2)	0x14	MotorPeriod[7:0]							
MotorKt1 (2)	0x15	MotorKt[15:8]							
MotorKt2 (2)	0x16	MotorKt[7:0]							
IPDPosition (2)	0x19	IPDPosition[7:0]							
SupplyVoltage (2)	0x1A	SupplyVoltage [7:0]							
SpeedCmd (2)	0x1B	SpeedCmd [7:0]							
spdCmdBuffer (2)	0x1C	spdCmdBuffer[7:0]							
FaultCode (2)	0x1E			Lock5	Lock4	Fault3	Lock2	Lock1	Lock0
MotorParam1 (3)	0x20	DoubleFreq	Rm[6:0]						
MotorParam2 (3)	0x21	AdjMode	Kt[6:0]						
MotorParam3 (3)	0x22	CtrlAdvMd	TCtrlAdv[6:0]						
SysOpt1 (3)	0x23	ISDThr[1:0]		IPDAdvcAgl[1:0]		ISDen	RvsDrEn	RvsDrThr[1:0]	
SysOpt2 (3)	0x24	OpenLCurr[1:0]		OpLCurrRt[2:0]			BrkDoneThr[2:0]		
SysOpt3 (3)	0x25	CtrlCoef[1:0]		StAccel2[2:0]			StAccel[2:0]		
SysOpt4 (3)	0x26	Op2ClsThr[4:0]					AlignTime[2:0]		
SysOpt5 (3)	0x27	LockEn[3:0]				AVSIndEn	AVSMEn	AVSMMd	IPDRlsMd
SysOpt6 (3)	0x28	SWiLimitThr[3:0]				HWiLimitThr[2:0]			
SysOpt7 (3)	0x29	LockEn5	ClsLpAccel[2:0]			Deadtime[3:0]			
SysOpt8 (3)	0x2A	IPDCurrThr[3:0]				LockEn4	VregSel	IPDClk[1:0]	
SysOpt9 (3)	0x2B	FGOLsel[1:0]		FGcycle[1:0]		KtLckThr[1:0]		SpdCtrlMd	CLoopDis

(1) R/W
(2) Read only
(3) EEPROM

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表 8. Default EEPROM Value

Address	Default Value
0x20	0x4A
0x21	0x4E
0x22	0x2A
0x23	0x00
0x24	0x98
0x25	0xE4
0x26	0x7A
0x27	0xF4
0x28	0x69
0x29	0xB8
0x2A	0xAD
0x2B	0x0C

8.5.3 Register Definition

表 9. Register Description

Register			Data	Description
Name	Address	Bits		
SpeedCtrl1 (1)	0x00	7:0	SpdCtrl[7:0]	8 LSB of a 9-bit value used for the motor speed. If OverRide = 1, the user can directly control the motor speed by writing to the register through I^2C.
SpeedCtrl2 (1)	0x01	7	OverRide	Use to control the SpdCtrl [8:0] bits. If OverRide = 1, the user can write the speed command through I^2C.
		6:1	N/A	N/A
		0	SpdCtrl [8]	MSB of a 9-bit value used for the motor speed. If OverRide = 1, user can directly control the motor speed by writing to the register through I^2C. The MSB should be written first. Digital takes a snapshot of the MSB when LSB is written.
DevCtrl (1)	0x02	7:0	enProgKey[7:0]	8-bit byte use to enable programming in the EEPROM. To program the EEPROM, enProgKey = 1011 0110 (0xB6), followed immediately by eeWrite = 1. Otherwise, enProgKey value is reset.
EECtrl (1)	0x03	7	sleepDis	Set to 1 to disable entering into sleep or standby mode.
		6	SIdata	Set to 1 to enable the writing to the configuration registers.
		5	eeRefresh	Copy EEPROM data to register.
		4	eeWrite	Bit used to program (write) to the EEPROM.
		3:0	N/A	N/A
Status (2)	0x10	7	OverTemp	Bit to indicate device temperature is over its limits.
		6	Slp_Stdby	Bit to indicate that device went into sleep or standby mode.
		5	OverCurr	Bit to indicate that an overcurrent event happened. This is a sticky bit, once written, it stays high even if overcurrent signal goes low. This bit is cleared on Read.
		4	MtrLck	Bit to indicate that the motor is locked.
		3	N/A	N/A
		2	N/A	N/A
		1	N/A	N/A
		0	N/A	N/A
Motor Speed1 (2)	0x11	7:0	MotorSpeed [15:8]	16-bit value indicating the motor speed. Always read the MotorSpeed1 first. Velocity (Hz) = {MotorSpeed1:MotorSpeed2} / 10 For example: MotorSpeed1 = 0x01, MotorSpeed2 = 0xFF, Motor Speed = 0x01FF (511) / 10 = 51 Hz
Motor Speed2 (2)	0x12	7:0	MotorSpeed [7:0]	

(1) R/W
(2) Read only

表 9. Register Description (接下页)

Register			Data	Description
Name	Address	Bits		
Motor Period1 (2)	0x13	7:0	MotorPeriod [15:8]	16-bit value indicating the motor period. Always read the MotorPeriod1 first. t_{ELE_PERIOD} (µs) = {MotorPeriod1:MotorPeriod2} × 10 For example: MotorPeriod1 = 0x01, MotorPeriod2 = 0xFF, Motor Period = 0x01FF (511) × 10 = 5.1 ms
Motor Period2 (2)	0x14	7:0	MotorPeriod [7:0]	
MotorKt1 (2)	0x15	7:0	MotorKt[15:8]	16-bit value indicating the motor measured velocity constant. Always read the MotorKt1 first. Ktc (V/Hz)= {MotorKt1:MotorKt2} / 2 /1090 {MotorKt1:MotorKt2} corresponding to 2 × Ktph_dig
MotorKt2 (2)	0x16	7:0	MotorKt[7:0]	
IPDPosition (2)	0x19	7:0	IPDPosition [7:0]	8-bit value indicating the estimated motor position during IPD plus the IPD advance angle (see 表 7)
Supply Voltage (2)	0x1A	7:0	SupplyVoltage [7:0]	8-bit value indicating the supply voltage $V_{POWERSUPPLY}$ (V) = SupplyVoltage[7:0] × 22.8 V / 256 For example, SupplyVoltage[7:0] = 0x87, $V_{POWERSUPPLY}$ (V) = 0x87 (135) × 22.8 / 256 = 12 V
SpeedCmd (2)	0x1B	7:0	SpeedCmd[7:0]	8-bit value indicating the speed command based on analog or PWMin or I^2C. FF indicates 100% speed command.
spdCmd Buffer (2)	0x1C	7:0	spdCmdBuffer [8:1]	8-bit value indicating the speed command after buffer output. FF indicates 100% speed command.
FaultCode (2)	0x1E	7:6	N/A	N/A
		5	Lock5	Stuck in closed loop
		4	Lock4	Stuck in open loop
		3	Fault3	No motor
		2	Lock2	Kt abnormal
		1	Lock1	Speed abnormal
		0	Lock0	Lock detection current limit
Motor Param1 (3)	0x20	7	DoubleFreq	0 = Set driver output frequency to 25 kHz 1 = Set driver output frequency to 50 kHz
		6:0	Rm[6:0]	Rm[6:4] : Number of the Shift bits of the motor phase resistance Rm[3:0] : Significant value of the motor phase resistance Rmdig = R_(ph_ct) / 0.00735 Rmdig = Rm[3:0] ≪ Rm[6:4] See *Motor Phase Resistance* and 表 2
Motor Param2 (3)	0x21	7	AdjMode	Closed loop adjustment mode setting 0 = Full cycle adjustment 1 = Half cycle adjustment
		6:0	Kt[6:0]	Kt[6:4] = Number of the Shift bits of BEMF constant Kt[3:0] = Significant value of the BEMF constant 〖Kt〗_(ph_dig) = 1442× 〖Kt〗_ph 〖Kt〗_(ph_dig) = Kt[3:0] ≪ Kt[4:6] See *BEMF Constant* and 表 3 .
Motor Param3 (3)	0x22	7	CtrlAdvMd	Motor commutate control advance 0 = Fixed time 1 = Variable time relative to the motor speed and V_{CC}
		6:0	Tdelay[6:0]	t_{delay} [6:4] = Number of the Shift bits of LRTIME t_{delay} [3:0] = Significant value of LRTIME $t_{SETTING}$ = 2.5 µs × {TCtrlAdv[3:0] << TCtrlAdv[6:4]}

(3) EEPROM

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表 9. Register Description (接下页)

Register			Data	Description
Name	Address	Bits		
SysOpt1 (3)	0x23	7:6	ISDThr[1:0]	ISD stationary judgment threshold 00 = 6 Hz (80 ms, no zero cross) 01 = 3 Hz (160 ms, no zero cross) 10 = 1.6 Hz (320 ms, no zero cross) 11 = 0.8 Hz (640 ms, no zero cross)
		5:4	IPDAdvcAgl [1:0]	Advancing angle after inductive sense 00 = 30° 01 = 60° 10 = 90° 11 = 120°
		3	ISDen	0 = Initial speed detect (ISD) disable 1 = ISD enable
		2	RvsDrEn	0 = Reverse drive disable 1 = Reverse drive enable
		1:0	RvsDrThr[1:0]	The threshold where device starts to process reverse drive (RvsDr) or brake. 00 = 6.3 Hz 01 = 13 Hz 10 = 26 Hz 11 = 51 Hz
SysOpt2 (3)	0x24	7:6	OpenLCurr[1:0]	Open loop current setting. 00 = 0.2 A 01 = 0.4 A 10 = 0.8 A 11 = 1.6 A
		5:3	OpLCurrRt:[2:0]	Open-loop current ramp-up rate setting 000 = 6 V_{CC}/s 001 = 3 V_{CC}/s 010 = 1.5 V_{CC}/s 011 = 0.7 V_{CC}/s 100 = 0.34 V_{CC}/s 101 = 0.16 V_{CC}/s 110 = 0.07 V_{CC}/s 111 = 0.023 V_{CC}/s
		2:0	BrkDoneThr [2:0]	Braking mode setting 000 = No brake (BrkEn = 0) 001 = 2.7 s 010 = 1.3 s 011 = 0.67 s 100 = 0.33 s 101 = 0.16 s 110 = 0.08 s 111 = 0.04 s

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表 9. Register Description (接下页)

Register			Data	Description
Name	Address	Bits		
SysOpt3 (3)	0x25	7:6	CtrlCoef[1:0]	Control coefficient 00 = 0.25 01 = 0.5 10 = 0.75 11 = 1
		5:3	StAccel2[2:0]	Open loop start-up accelerate (second order) 000 = 57 Hz/s^2 001 = 29 Hz/s^2 010 = 14 Hz/s^2 011 = 6.9 Hz/s^2 100 = 3.3 Hz/s^2 101 = 1.6 Hz/s^2 110 = 0.66 Hz/s^2 111 = 0.22 Hz/s^2
		2:0	StAccel[2:0]	Open loop start-up accelerate (first order) 000 = 76 Hz/s 001 = 38 Hz/s 010 = 19 Hz/s 011 = 9.2 Hz/s 100 = 4.5 Hz/s 101 = 2.1 Hz/s 110 = 0.9 Hz/s 111 = 0.3 Hz/s
SysOpt4 (3)	0x26	7:3	Op2ClsThr[4:0]	Open to closed loop threshold 0xxxx = Range 0: n × 0.8 Hz 00000 = N/A 00001 = 0.8 Hz 00111 = 5.6 Hz 01111 = 12 Hz 1xxxx = Range 1: (n + 1) × 12.8 Hz 10000 = 12.8 Hz 10001 = 25.6 Hz 10111 = 192 Hz 11111 = 204.8 Hz
		2:0	AlignTime[2:0]	Align time. 000 = 5.3 s 001 = 2.7 s 010 = 1.3 s 011 = 0.67 s 100 = 0.33 s 101 = 0.16 s 110 = 0.08 s 111 = 0.04 s
SysOpt5 (3)	0x27	7	FaultEn3 (LockEn[3])	No motor fault. Enabled when high
		6	LockEn[2]	Abnormal Kt. Enabled when high
		5	LockEn[1]	Abnormal speed. Enabled when high
		4	LockEn[0]	Lock detection current limit. Enabled when high
		3	AVSIndEn	Inductive AVS enable. Enabled when high.
		2	AVSMEn	Mechanical AVS enable. Enabled when high
		1	AVSMMd	Mechanical AVS mode 0 = AVS to V_{CC} 1 = AVS to 24 V
		0	IPDRlsMd	IPD release mode 0 = Brake when inductive release 1 = Hi-z when inductive release

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表 9. Register Description (接下页)

Register			Data	Description
Name	Address	Bits		
SysOpt6[3]	0x28	7:4	SWiLimitThr [3:0]	Acceleration current limit threshold 0000 = No acceleration current limit 0001 = 0.2-A current limit xxxx = n × 0.2 A current limit
		3:1	HWiLimitThr [2:0]	Lock detection current limit threshold (n + 1) × 0.4 A
		0	N/A	N/A
SysOpt7[3]	0x29	7	LockEn[5]	Stuck in closed loop (no zero cross detected). Enabled when high
		6:4	ClsLpAccel[2:0]	Closed loop accelerate 000 = Inf fast 001 = 48 V_{CC}/s 010 = 48 V_{CC}/s 011 = 0.77 V_{CC}/s 100 = 0.37 V_{CC}/s 101 = 0.19 V_{CC}/s 110 = 0.091 V_{CC}/s 111 = 0.045 V_{CC}/s
		3:0	Deadtime[3:0]	Dead time between HS and LS gate drive for motor phases 0000 = 40 ns xxxx = (n + 1) × 40 ns. Recommended minimum dead time is 400 ns for 24-V VCC and 360 ns for 12-V VCC.
SysOpt8[3]	0x2A	7:4	IPDCurrThr[3:0]	IPD (inductive sense) current threshold 0000 = No IPD function. Align and Go 0001 = 0.4-A current threshold. xxxx = 0.2 A × (n + 1) current threshold.
		3	LockEn[4]	Open loop stuck (no zero cross detected). Enabled when high
		2	VregSel	Buck regulator voltage select 0: Vreg = 5 V 1: Vreg = 3.3 V
		1:0	IPDClk[1:0]	Inductive sense clock 00 = 12 Hz; 01 = 24 Hz; 10 = 47 Hz; 11 = 95 Hz
SysOpt9[3]	0x2B	7:6	FGOLsel[1:0]	FG open loop output select 00 = FG outputs in both open loop and closed loop 01 = FG outputs only in closed loop 10 = FG outputs closed loop and the first open loop 11 = Reserved
		5:4	FGcycle[1:0]	FG cycle select 00 = 1 pulse output per electrical cycle 01 = 2 pulses output per 3 electrical cycles 10 = 1 pulse output per 2 electrical cycles 11 = 1 pulse output per 3 electrical cycles
		3:2	KtLckThr[1:0]	Abnormal Kt lock detect threshold 00 = Kt_high = 3/2Kt. Kt_low = 3/4Kt 01 = Kt_high = 2Kt. Kt_low = 3/4Kt 10 = Kt_high = 3/2Kt. Kt_low = 1/2Kt 11 = Kt_high = 2Kt. Kt_low = 1/2Kt
		1	SpdCtrlMd	Speed input mode 0 = Analog input expected at SPEED pin 1 = PWM input expected at SPEED pin
		0	CLoopDis	0 = Transfer to closed loop at Op2ClsThr speed 1 = No transfer to closed loop. Keep in open loop

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV10975 is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high reliability, flexible and simple solution for appliance fan, pump, and HVAC applications. The following design in 图 39 shows a common application of the DRV10975. For the DRV10975Z sleep mode device, a Zener diode must be placed in parallel with the 10-µF V_{REG} capacitor as shown in 图 39. The Zener diode must meet the requirements listed in 表 11

9.2 Typical Application

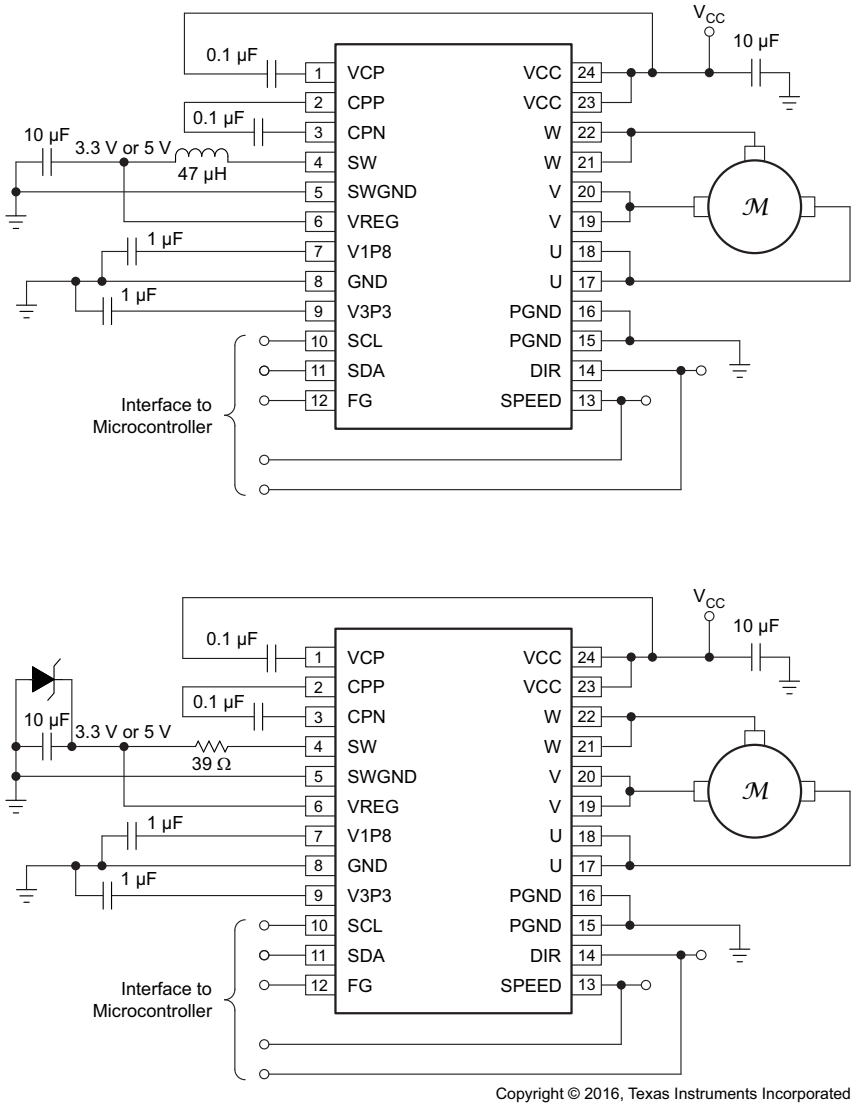


图 39. Typical Application Schematics for DRV10975 (Top Image) and DRV10975Z (Bottom Image)

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Typical Application (接下页)

9.2.1 Design Requirements

表 10 provides design input parameters and motor parameters for system design.

表 10. Recommended Application Range

		MIN	TYP	MAX	UNIT
Motor voltage		6.5	12	18	V
BEMF constant	Phase to phase, measured while motor is coasting	0.001		1.4	V/Hz
Motor phase resistance	1 phase, measured ph-ph and divide by 2	0.3		12	Ω
Motor electrical constant	1 phase; inductance divided by resistance, measured ph-ph is equal to 1 ph	100		5000	µs
Operating closed loop speed	Electrical frequency	1		1000	Hz
Operating current	PGND, GND	0.1		1.5	A
Absolute maximum current	During start-up or lock condition			2	A

表 11. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VCC}	V_{CC}	GND	10-µF ceramic capacitor rated for V_{CC}
C_{VCP}	VCP	V_{CC}	0.1-µF ceramic capacitor rated for 10 V
C_{CP}	CPP	CPN	0.1-µF ceramic capacitor rated for V_{CC} × 2
$L_{SW-VREG}$	SW	VREG	47-µH ferrite inductor with 1.15-A current rating, 1.15-A saturation current, and < 1 Ω DC resistance (buck mode)
$R_{SW-VREG}$	SW	VREG	39-Ω series resistor rated for ¼ W (linear mode)
C_{VREG}	VREG	GND	10-µF ceramic capacitor rated for 10 V
C_{V1P8}	V1P8	GND	1-µF ceramic capacitor rated for 5 V
C_{V3P3}	V3P3	GND	1-µF ceramic capacitor rated for 5 V
R_{SCL}	SCL	V3P3	4.75-kΩ pullup to V3P3
R_{SDA}	SDA	V3P3	4.75-kΩ pullup to V3P3
R_{FG}	FG	V3P3	4.75-kΩ pullup to V3P3
D_{Zener} (For 3.3-V Vreg mode)	GND	VREG	Only for DRV10975Z, Zener Voltage (Vz) = 4 V (±5%). Peak Power > 2.5 W, Leakage Current <100 µA
D_{Zener} (For 5-V Vreg mode)	GND	VREG	Only for DRV10975Z, Zener Voltage(Vz) = 6 V (±5%). Peak Power > 2.5 W, Leakage Current <100 µA

9.2.2 Detailed Design Procedure

1. See the *Design Requirements* section and make sure your system meets the recommended application range.
2. See the *DRV10983 and DRV10975 Tuning Guide* and measure the motor parameters.
3. See the *DRV10983 and DRV10975 Tuning Guide*. Configure the parameters using DRV10975 GUI, and optimize the motor operation. The *Tuning Guide* takes the user through all the configurations step by step, including: start-up operation, closed-loop operation, current control, initial positioning, lock detection, and anti-voltage surge.
4. See the *Programming Guide for the DRV10983* and Non-Volatile Memory section for burning tuned settings into EEPROM.
5. Build your hardware based on *Layout Guidelines*.
6. Connect the device into system and validate your system solution.

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9.2.3 Application Curves

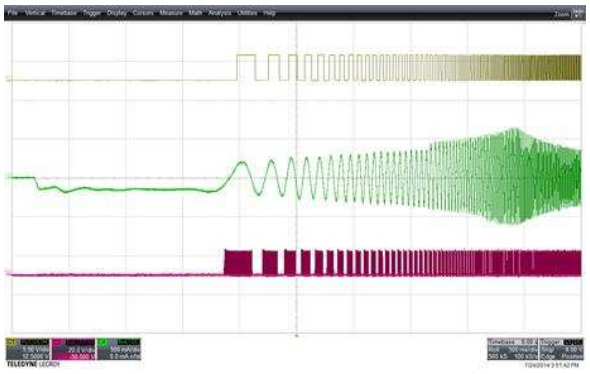


图 40. DRV10975 Start-Up Waveform

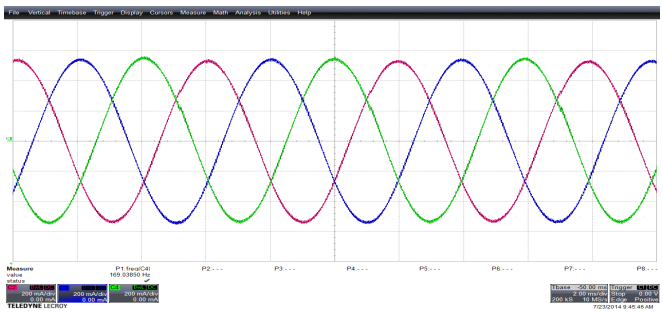


图 41. DRV10975 Operation Current Waveform

10 Power Supply Recommendations

The DRV10975 is designed to operate from an input voltage supply, $V_{(VCC)}$, range between 6.5 V and 18 V. The user must place a 10-µF ceramic capacitor rated for V_{CC} as close as possible to the V_{CC} and GND pins.

If the power supply ripple is more than 200 mV, in addition to the local decoupling capacitors, a bulk capacitance is required and must be sized according to the application requirements. If the bulk capacitance is implemented in the application, the user can reduce the value of the local ceramic capacitor to 1 µF.

11 Layout

11.1 Layout Guidelines

- Place V_{CC}, GND, U, V, and W pins with thick traces because high current passes through these traces.
- Place the 10-µF capacitor between V_{CC} and GND, and as close to the V_{CC} and GND pins as possible.
- Place the capacitor between CPP and CPN, and as close to the CPP and CPN pins as possible.
- Connect the GND, PGND, and SWGND under the thermal pad.
- Keep the thermal pad connection as large as possible, both on the bottom side and top side. It should be one piece of copper without any gaps.

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11.2 Layout Example

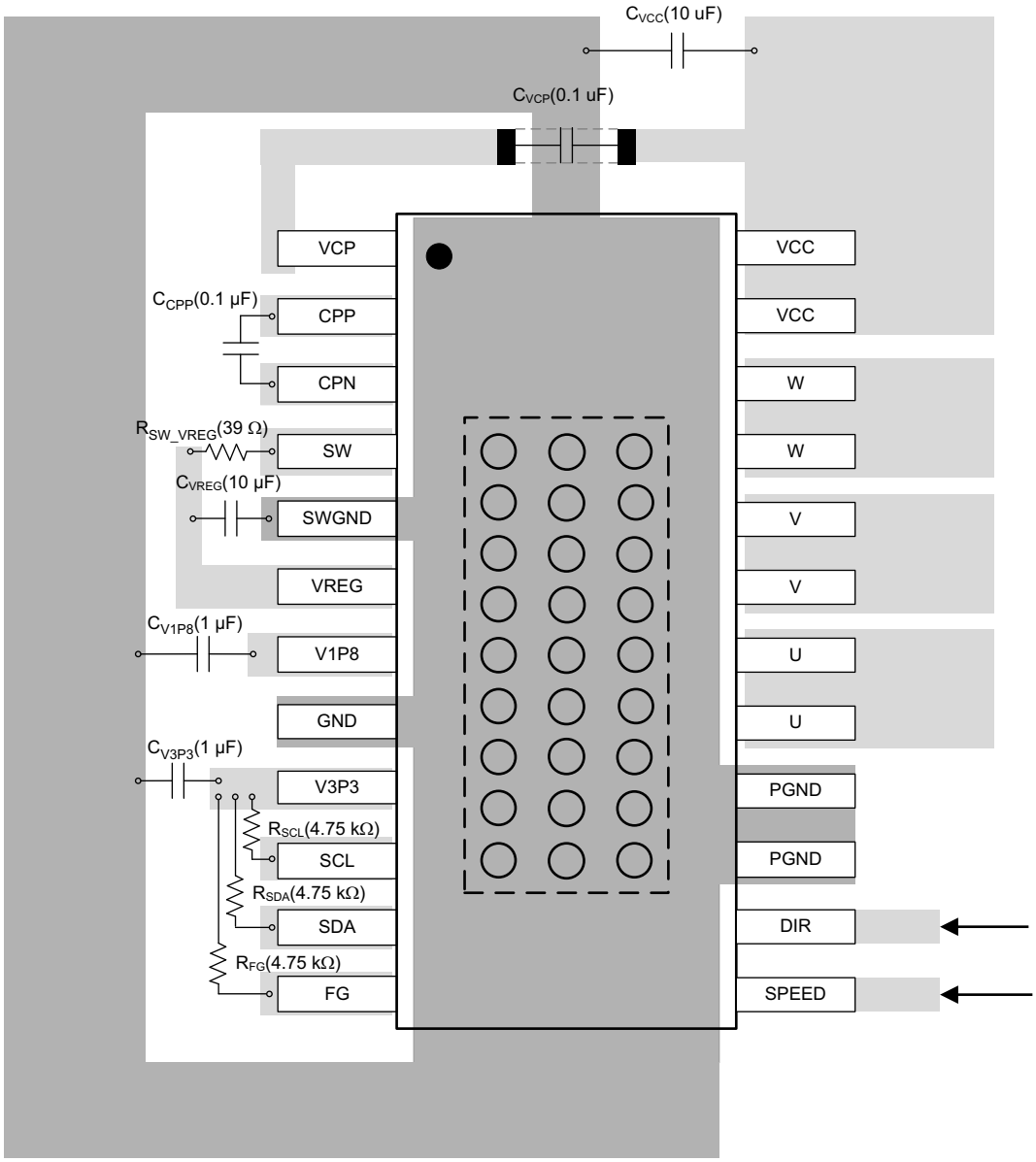


图 42. Example Layout Diagram for HTSSOP Package

Layout Example (接下页)

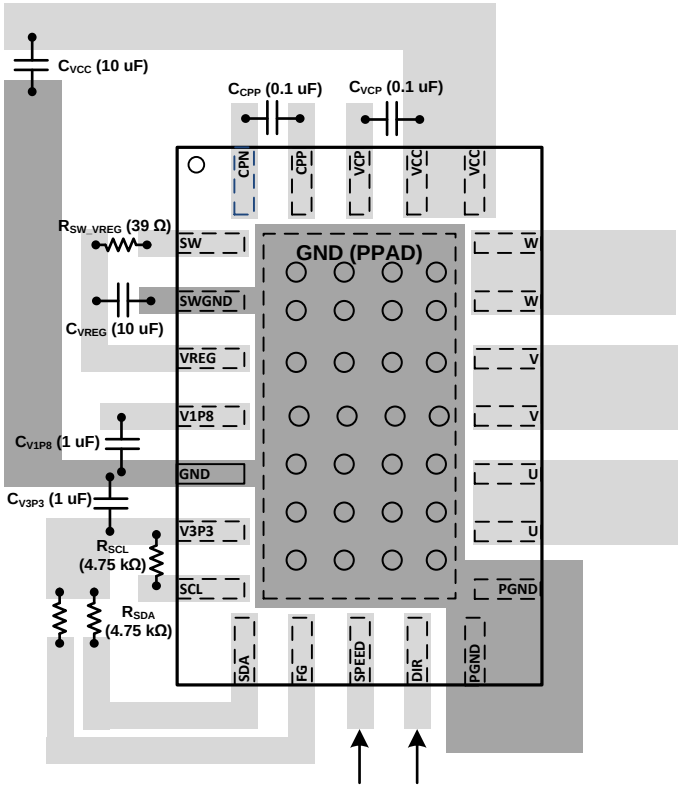


图 43. Example Layout Diagram for VQFN Package

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12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

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12.2 文档支持

12.2.1 相关文档

如需相关文档，请参阅：

- 德州仪器 (TI)，*DRV10983 和 DRV10975 评估模块用户指南*
- 德州仪器 (TI)，*DRV10983 和 DRV10975调优指南*
- 德州仪器 (TI)，*如何设计高效散热型集成 BLDC 电机驱动 PCB 应用报告*
- 德州仪器 (TI)，*DRV10983 编程指南*

12.3 商标

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12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航面板。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV10975PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10975	Samples
DRV10975PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10975	Samples
DRV10975RHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 10975	Samples
DRV10975ZPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10975Z	Samples
DRV10975ZPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10975Z	Samples
DRV10975ZRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV 10975Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

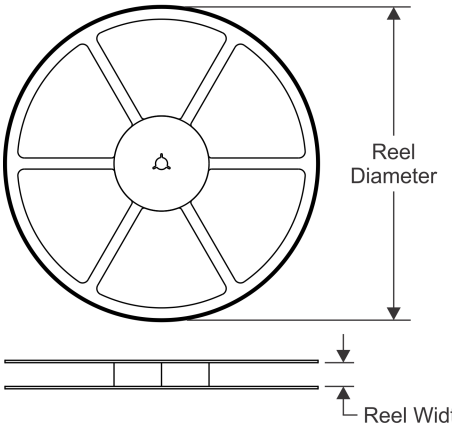
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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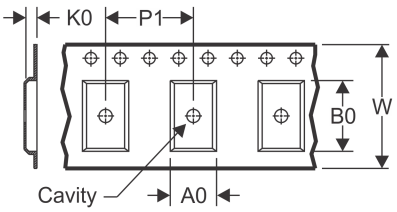
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

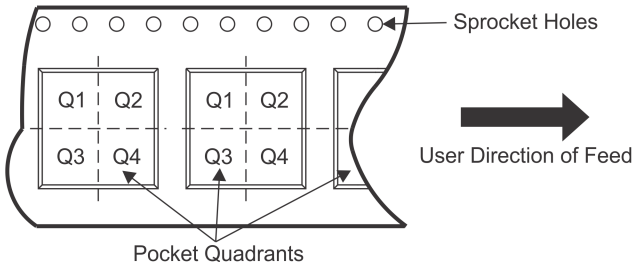


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

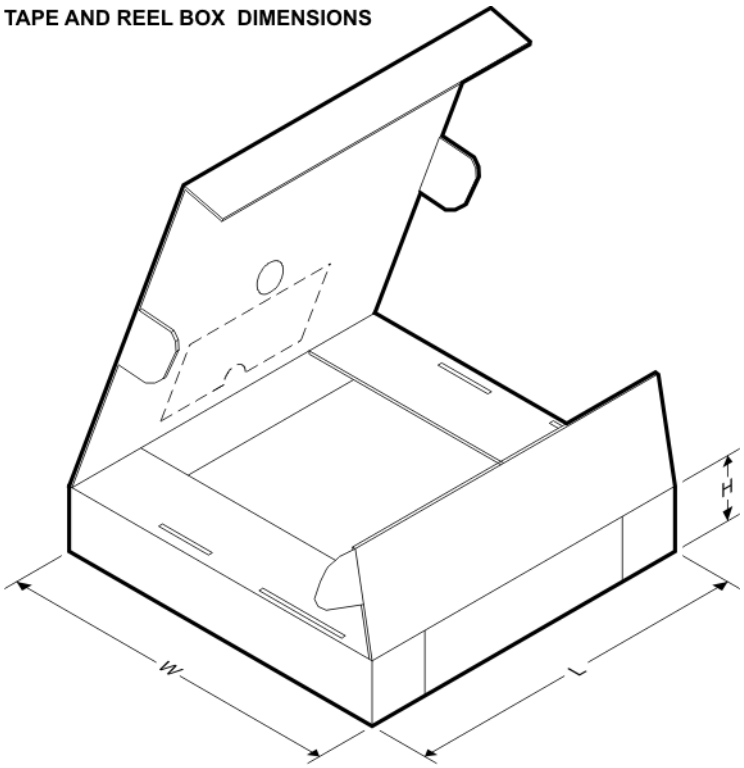
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV10975PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV10975RHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
DRV10975ZPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV10975ZRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV10975PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DRV10975RHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
DRV10975ZPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DRV10975ZRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

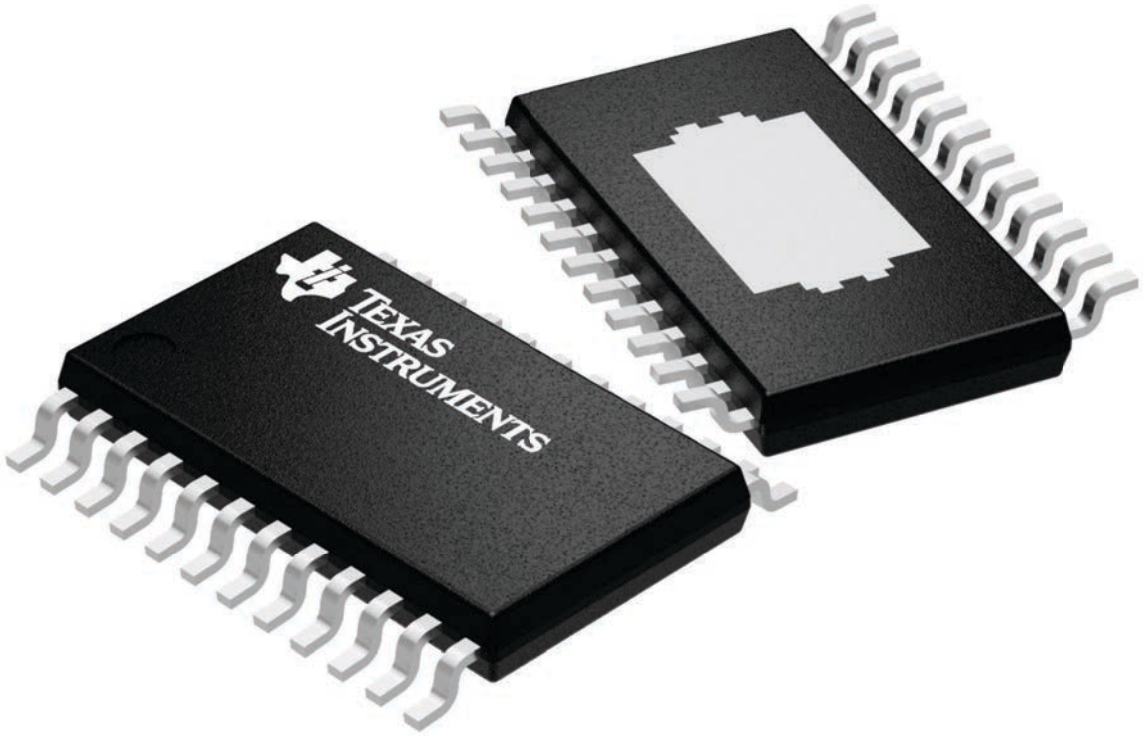
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

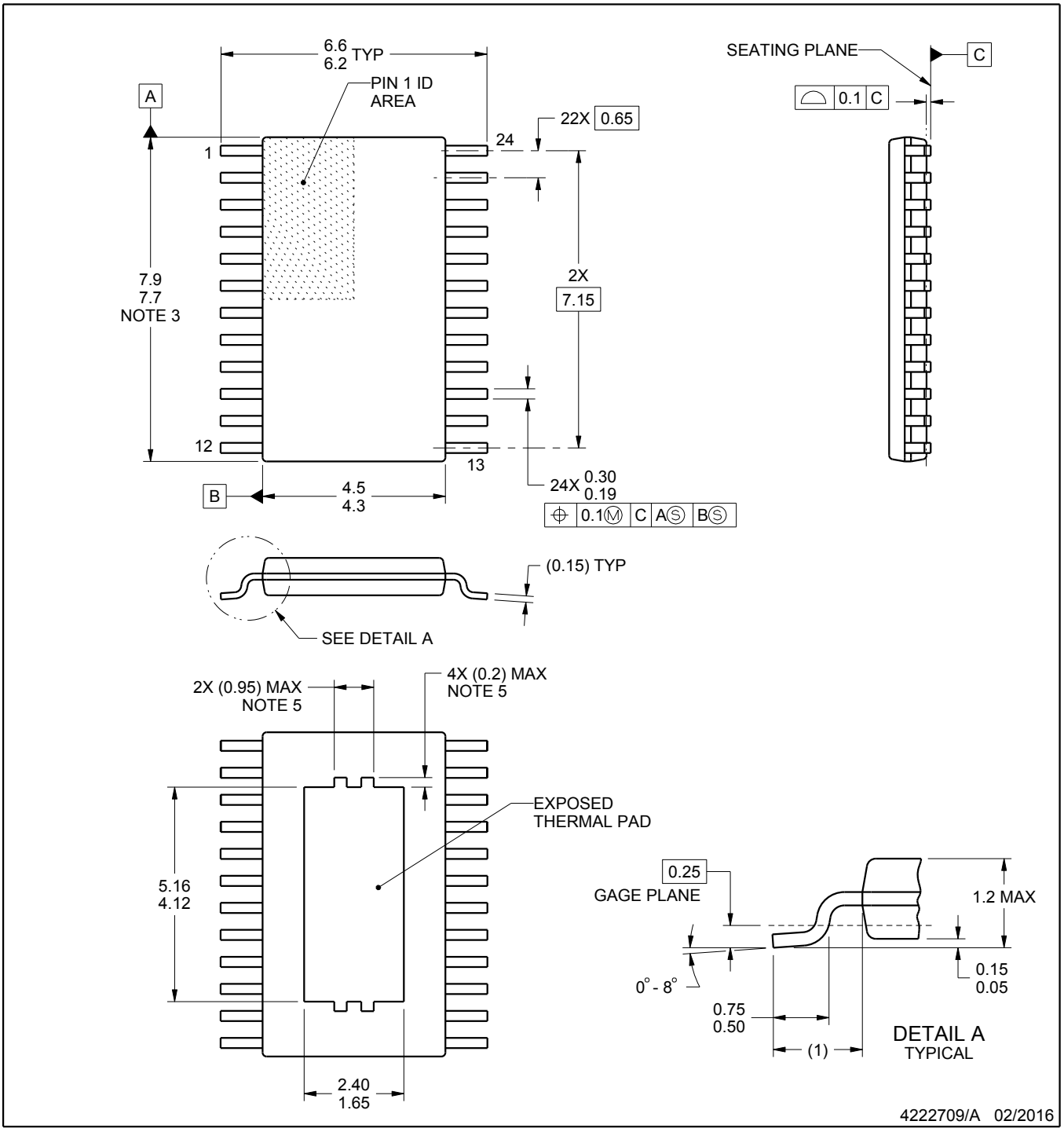


PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

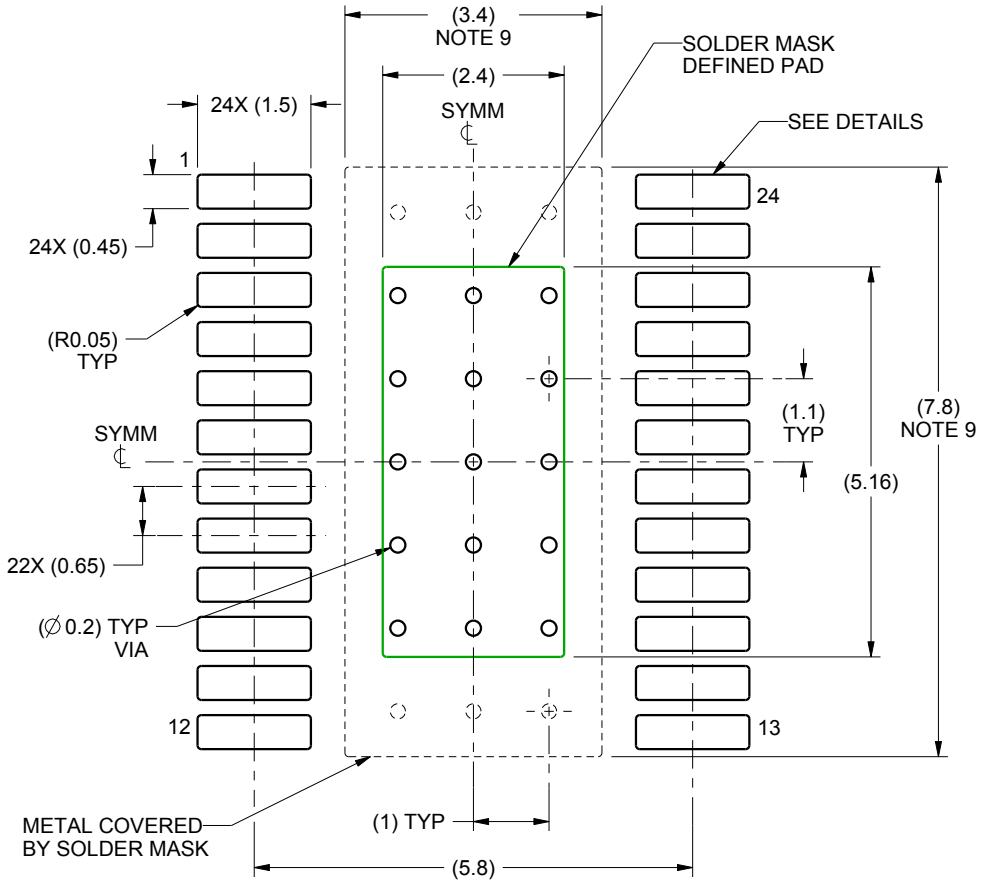
PLASTIC SMALL OUTLINE



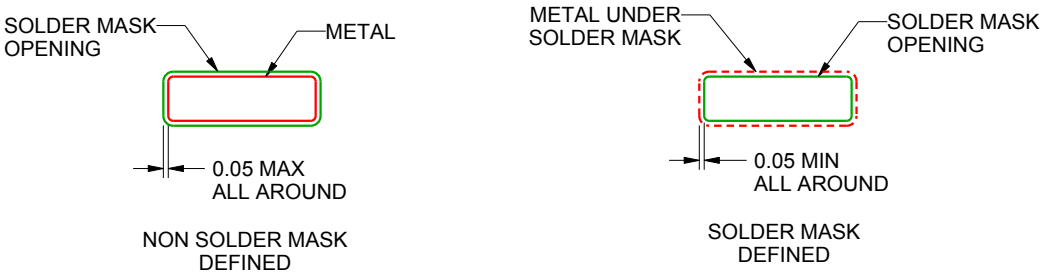
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

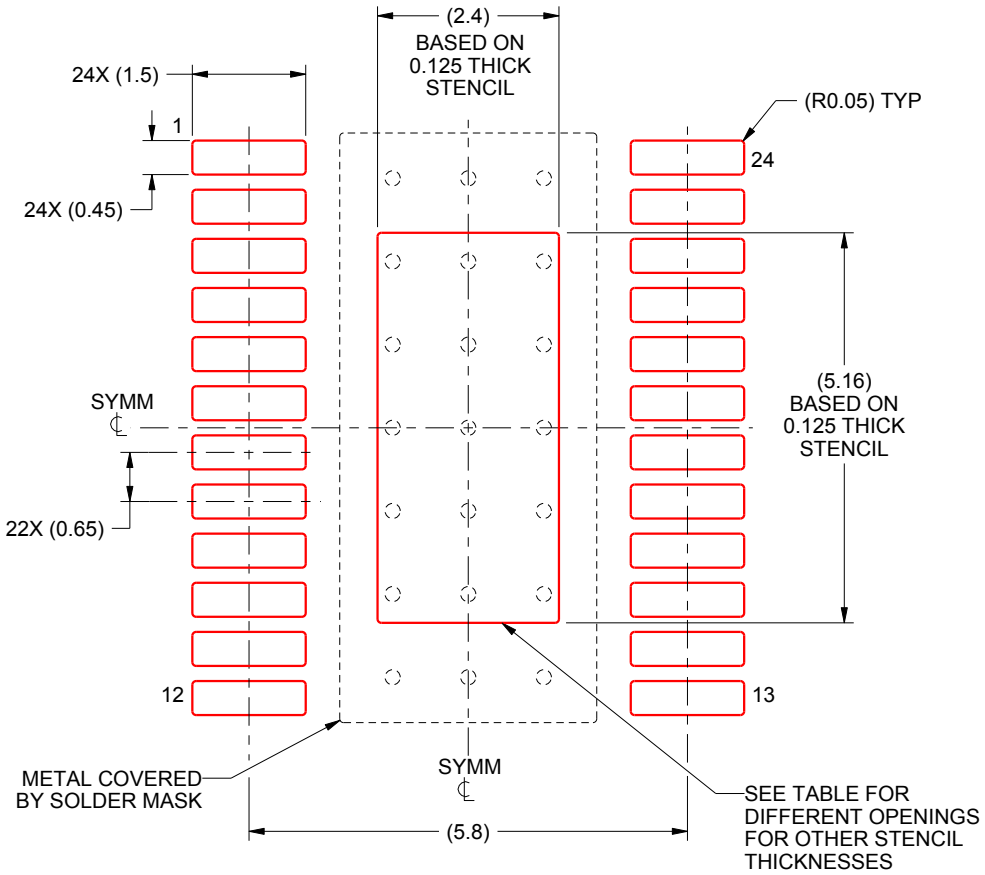


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

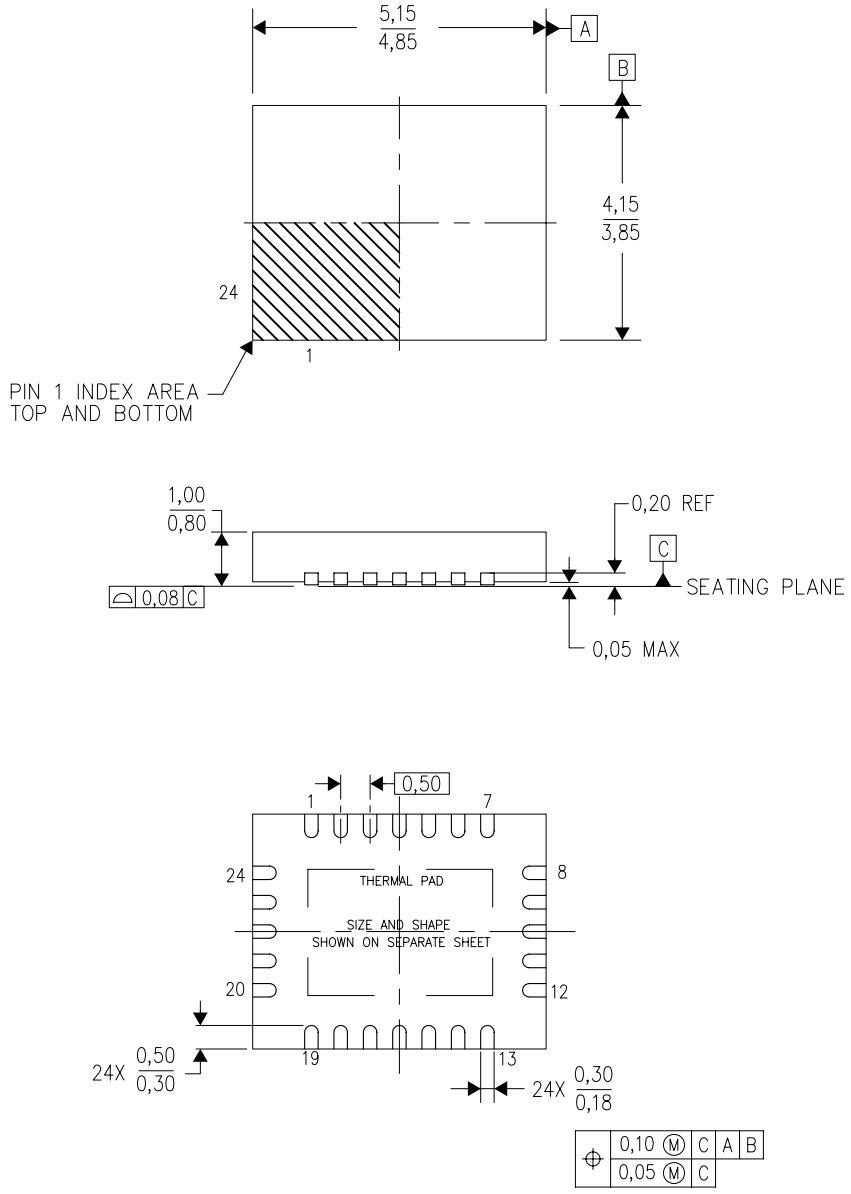
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

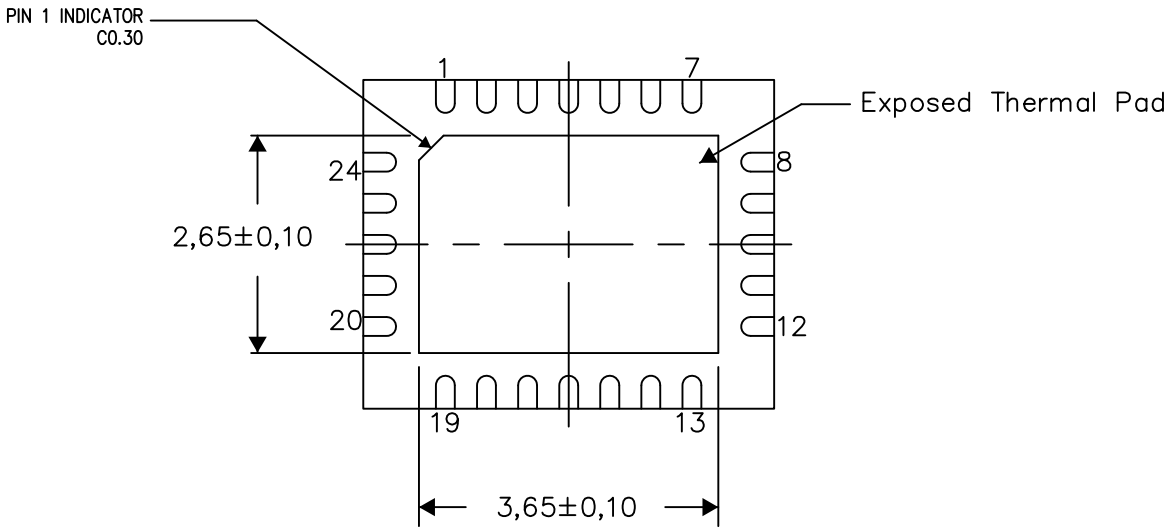
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



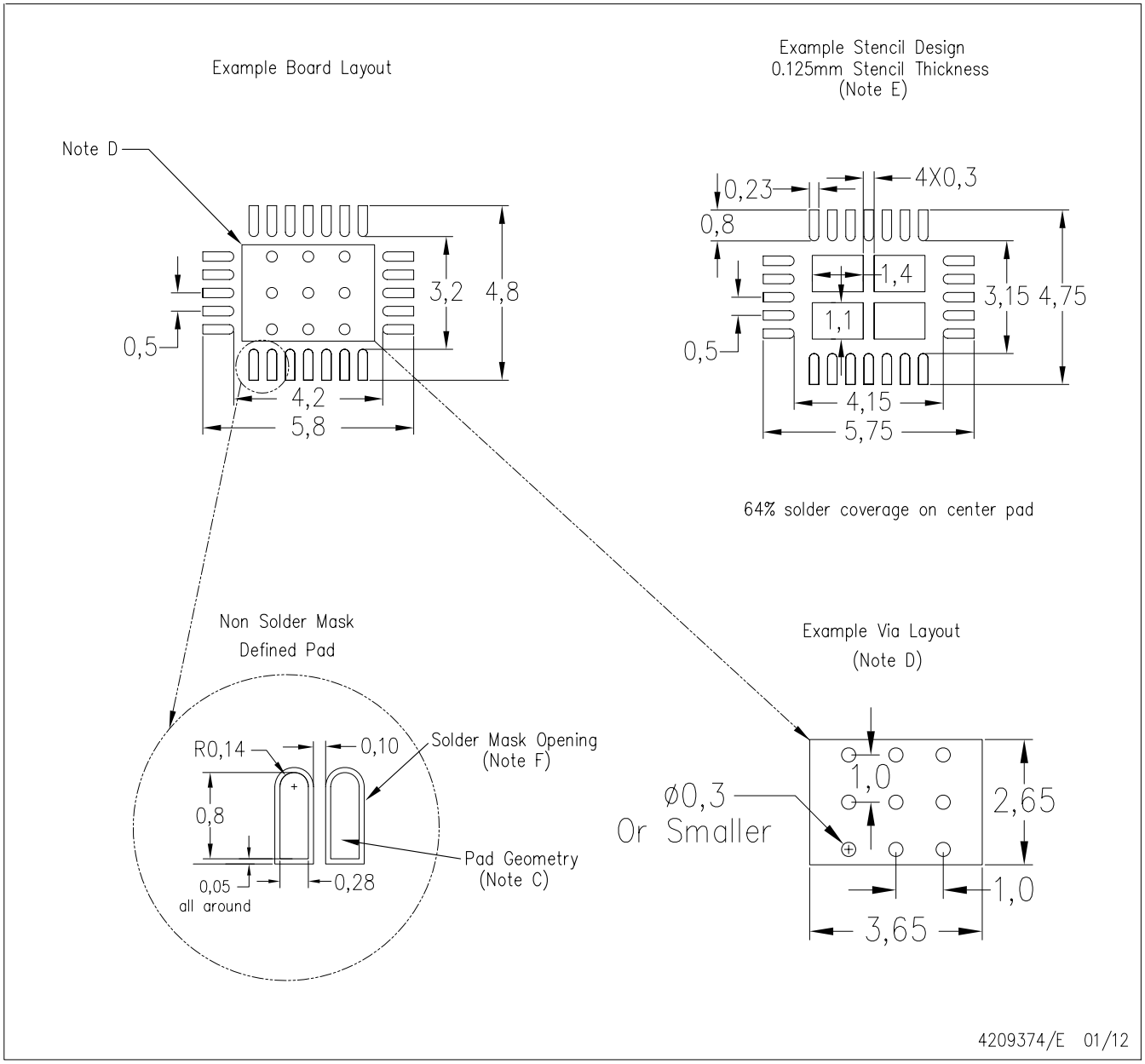
Bottom View

Exposed Thermal Pad Dimensions

4206360–3/K 02/14

NOTE: All linear dimensions are in millimeters

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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