UCC2751x 单通道、高速、低侧栅极驱动器（具有 4A 峰值拉电流和 4A 峰值灌电流）

1 特性

- 低成本栅极驱动器器件提供 NPN 和 PNP 离散解决方案的高品质替代产品
- 4A 峰值拉电流和 4A 峰值灌电流对称驱动
- 短暂传播延迟（典型值 13ns）
- 短暂上升和下降时间（典型值分别为 9ns 和 7ns）
- 4.5V 至 18V 单电源范围
- VDD 欠压闭锁 (UVLO) 期间输出保持低电平（确保上电和掉电时无毛刺脉冲运行）
- 晶体管逻辑 (TTL) 和互补金属氧化物半导体 (CMOS) 兼容输入逻辑阈值（与电源电压无关）
- 针对高抗扰度的滞后逻辑阈值
- 双输入设计（可选择反相（IN- 引脚）或非反相（IN+ 引脚）驱动器配置）
  - 未使用的输入引脚可用于使能或禁用功能
- 当输入引脚悬空时，输出保持在低电平
- 输入引脚绝对最大电压电平不受 VDD 引脚偏置电源电压的限制
- -40°C 至 140°C 的运行温度范围
- 5 引脚 DBV (SOT-23) 和 6 引脚 DRS（3mm x 3mm 带有外露散热焊盘的晶圆级小外形无引线 (WSON)）封装选项

2 应用

- 开关模式电源
- 直流-直流转换器
- 针对数字电源控制器的伴随栅极驱动器器件
- 太阳能、电机控制、不间断电源 (UPS)
- 用于新上市的宽带隙电源器件（例如 GaN）的栅极驱动器

3 说明

UCC27516 和 UCC27517 单通道高速低侧栅极驱动器器件可有效驱动金属氧化物半导体场效应晶体管 (MOSFET) 和绝缘栅双极型晶体管 (IGBT) 电源开关。UCC27516 和 UCC27517 采用的设计方案可最大程度减少击穿电流，从而为电容负载提供较高的峰值拉/灌电流脉冲，同时提供轨到轨驱动能力以及超短的传播延迟（典型值为 13ns）。

当 VDD = 12V 时，UCC27516 和 UCC27517 可提供峰值为 4A 的灌/拉（对称驱动）电流驱动能力。

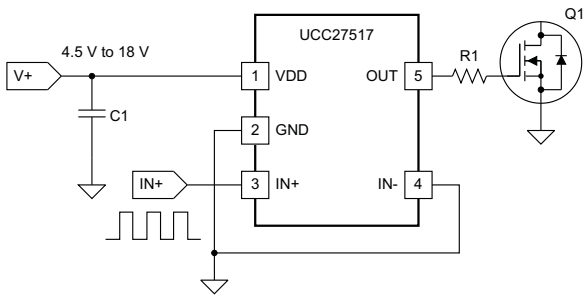
器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC27516	SON (6)	3.00mm × 3.00mm
UCC27517	SOT-23 (5)	2.90mm x 1.60mm

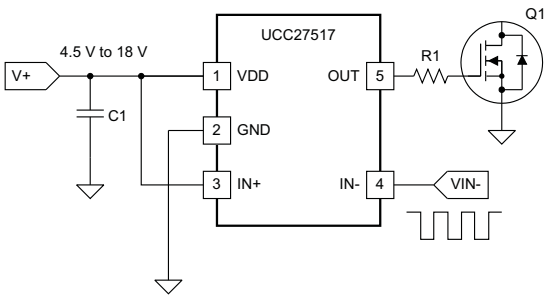
(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图

Non-Inverting Input



Inverting Input



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (May 2013) to Revision D — **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision B (June 2012) to Revision C — **Page**

- 已添加 0.5 to beginning of P_{SW} equation in *Power Dissipation* section ... 25

Changes from Revision A (March 2012) to Revision B — **Page**

- 已添加 UCC27516 器件。 ... 1
- Added GND, ground definition. ... 4
- Added DC and repetitive pulse rates to OUT voltage. ... 5
- Added note 5. ... 5
- Changed Human Body Model max value from 2000 V to 400V. ... 5
- Changed Charged Device Model max value from 500 V to 100 V. ... 5
- 已添加 UCC27516 block diagram. ... 13
- 已添加 PCB layout bullet. ... 22
- 已添加 Thermal Information description. ... 23

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5 说明 （续）

UCC27516 和 UCC27517 具有 4.5V 至 18V 的宽 VDD 范围，以及 –40°C 至 140°C 的宽温度范围。VDD 引脚上的内部欠压闭锁 (UVLO) 电路可在超出 VDD 运行范围时使输出保持低电平。此器件能够在低电压（例如低于 5V）下运行，并且拥有同类产品中较好的开关特性，因此非常适用于驱动诸如 GaN 功率半导体器件等新上市的宽带隙电源开关器件。

UCC27516 和 UCC27517 特有双输入设计，同一器件可灵活实现反相（IN- 引脚）和非反相（IN+ 引脚）配置。IN+ 引脚和 IN- 引脚中的任何一个都可用于控制此驱动器输出的状态。未使用的输入引脚可被用于启用和禁用功能。出于安全考虑，输入引脚上的内部上拉和下拉电阻器在输入引脚处于悬空状态时，确保输出被保持在低电平。因此，未使用的输入引脚不能保留在悬空状态而必须被适当的偏置，以确保驱动器输出被使能用于正常运行。

UCC27516 和 UCC27517 器件的输入引脚阈值是基于 TTL 和 COMS 兼容低压逻辑电路的，此逻辑电路是固定的且与 VDD 电源电压无关。高低阈值间的宽滞后提供了出色的抗扰度。

6 Device Comparison Table

The UCC2751x family of gate-driver products (Table 1) represent TI's latest generation of single-channel low-side high-speed gate-driver devices featuring high-source/sink current capability, industry best-in-class switching characteristics and a host of other features (表 2), all of which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits.

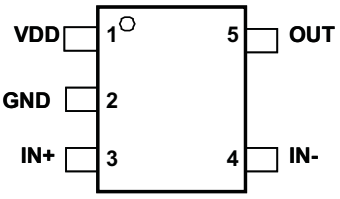
Table 1. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27516DRS	3 mm × 3 mm WSON, 6 pin	4-A/8-A (Symmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27511DBV	SOT-23, 6 pin		
UCC27516DRS	3 mm × 3 mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV	SOT-23, 5 pin		
UCC27518DBV	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV	SOT-23, 5 pin		

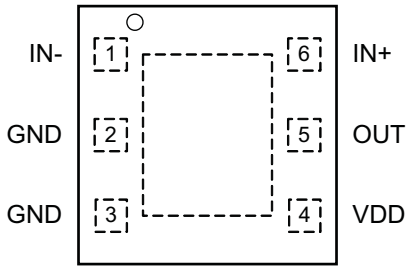
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7 Pin Configuration and Functions

5-Pin
UCC27517 DBV Package
Top View



6-Pin
UCC27516 DRS
Top View



Pin Functions – UCC27516

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN–	I	Inverting Input: When the driver is used in noninverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating.
2, 3	GND	—	Ground: All signals referenced to this pin. TI recommends to connect pin 2 and pin 3 on PCB as close to the device as possible.
4	VDD	I	Bias supply input.
5	OUT	I	Sourcing/Sinking Current Output of Driver
6	IN+	O	Noninverting Input: When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating.

Pin Functions – UCC27517

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD	I	Bias supply input.
2	GND	—	Ground. All signals reference to this pin. For the UCC27516, TI recommends to connect pin 2 and pin 3 on PCB as close to the device as possible.
3	IN+	I	Noninverting input. When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating
4	IN–	I	Inverting input. When the driver is used in noninverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating
5	OUT	O	Sourcing/Sinking current output of driver.

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8 Specifications

8.1 Absolute Maximum Ratings (1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	20	V
OUT voltage	DC	–0.3	VDD + 0.3	V
	Repetitive pulse less than 200 ns (4)	–2	VDD + 0.3	V
Output continuous current	I_{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 µs)	I_{OUT_pulsed}(source/sink)		4	
IN+, IN- (5)		–0.3	20	V
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.
(4) Values are verified by characterization on bench.
(5) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	–40		140	°C
Input voltage, IN+ and IN-	0		18	V

8.4 Thermal Information

THERMAL METRIC (1)		UCC27516 WSON 6 PINS	UCC27517 SOT-23 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.6	217.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100.1	85.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.6	44.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.7	43.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	23.7	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

VDD = 12 V, $T_A = T_J$ = –40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified pin.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN+ = VDD, IN- = GND	40	100	160	µA
			IN+ = IN- = GND or IN+ = IN- = VDD	25	75	145	
			IN+ = GND, IN- = VDD	20	60	115	
UNDERVOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.91	4.20	4.5	V
		T_A = –40°C to 140°C		3.70	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.2	0.3	0.5	
INPUTS (IN+, IN-)							
V_{IN_H}	Input signal high threshold	Output high for IN+ pin, Output low for IN- pin			2.2	2.4	V
V_{IN_L}	Input signal low threshold	Output low for IN+ pin, Output high for IN- pin		1.0	1.2		
V_{IN_HYS}	Input signal hysteresis				1.0		
SOURCE/SINK CURRENT							
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			±4		A
OUTPUTS (OUT)							
V_{DD}- V_{OH}	High output voltage	VDD = 12 V I_{OUT} = –10 mA			50	90	mV
		VDD = 4.5 V I_{OUT} = –10 mA			60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUT} = 10 mA			5	10	
		VDD = 4.5 V I_{OUT} = 10 mA			6	12	
R_{OH}	Output pullup resistance(2)	VDD = 12 V I_{OUT} = –10 mA			5.0	7.5	Ω
		VDD = 4.5 V I_{OUT} = –10 mA			5.0	11.0	
R_{OL}	Output pulldown resistance	VDD = 12 V I_{OUT} = 10 mA			0.5	1.0	
		VDD = 4.5 V I_{OUT} = 10 mA			0.6	1.2	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pullup structure of the UCC27516 and UCC27517's output stage.

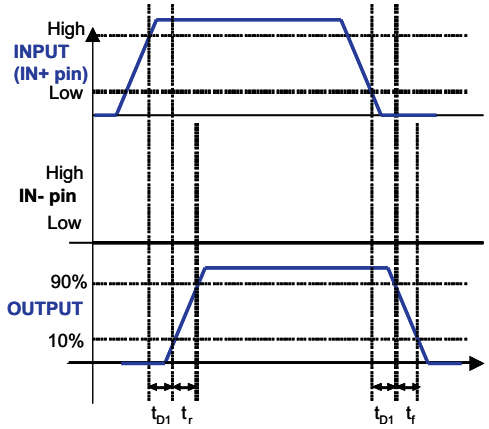
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8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

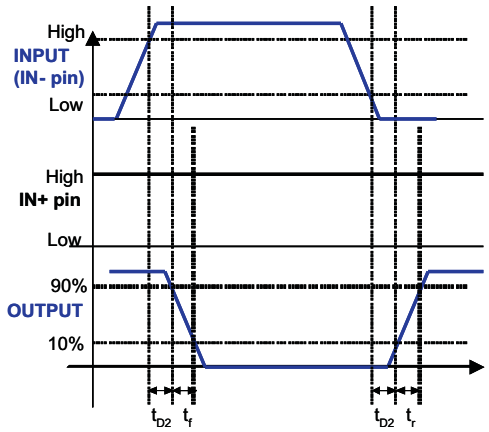
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time(1)	VDD = 12 V C_{LOAD} = 1.8 nF		8	12	ns
		VDD = 4.5 V C_{LOAD} = 1.8 nF		16	22	
t_F	Fall time(1)	VDD = 12 V C_{LOAD} = 1.8 nF		7	11	
		VDD=4.5V C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(1)	VDD = 12 V 5-V input pulse C_{LOAD} = 1.8 nF	4	13	23	
		VDD = 4.5 V 5-V input pulse C_{LOAD} = 1.8 nF	4	15	26	
t_{D2}	IN- to output propagation delay(1)	VDD = 12 V C_{LOAD} = 1.8 nF	4	13	23	
		VDD = 4.5 V C_{LOAD} = 1.8 nF	4	19	30	

(1) See timing diagrams in 图 1, 图 2, 图 3, and 图 4.



(PWM Input to IN+ Pin (IN– Pin Tied to GND))

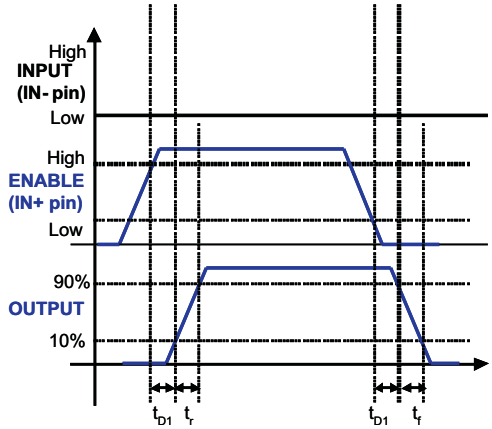
图 1. Noninverting Configuration



(PWM Input to IN- Pin (IN+ Pin Tied to VDD))

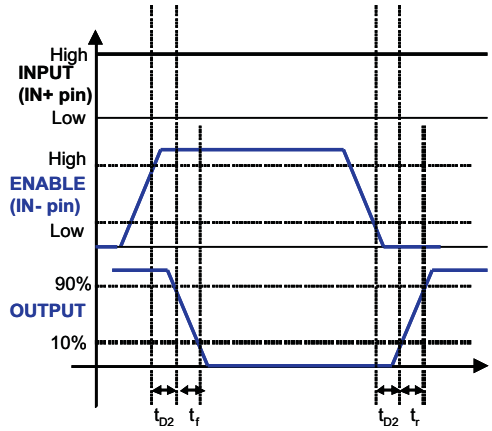
图 2. Inverting Configuration

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(Enable and Disable Signal Applied to IN+ Pin, PWM Input to IN- Pin)

图 3. Enable and Disable Function Using IN+ Pin



(Enable and Disable Signal Applied to IN- Pin, PWM Input to IN+ Pin)

图 4. Enable and Disable Function Using IN- Pin

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8.7 Typical Characteristics

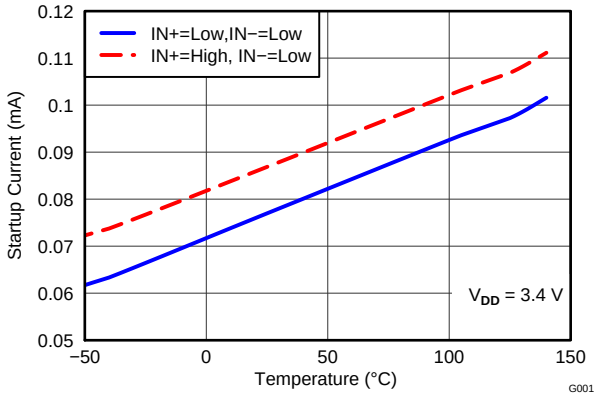


图 5. Startup Current vs Temperature

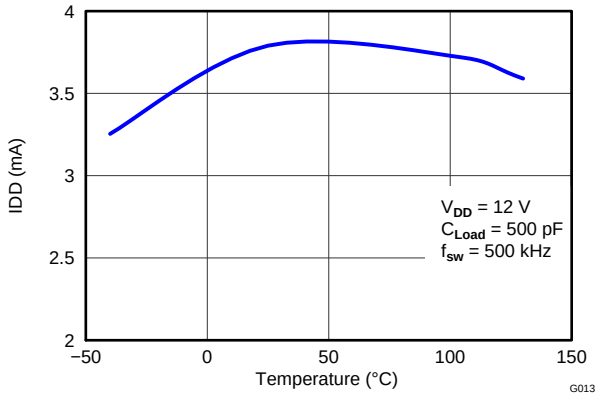


图 6. Operating Supply Current vs Temperature (Output Switching)

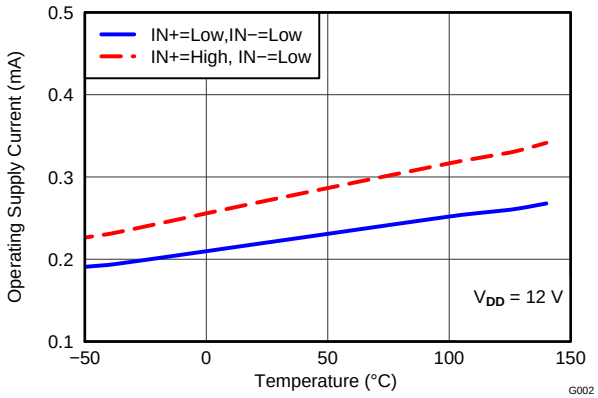


图 7. Supply Current vs Temperature (Output In DC On/Off Condition)

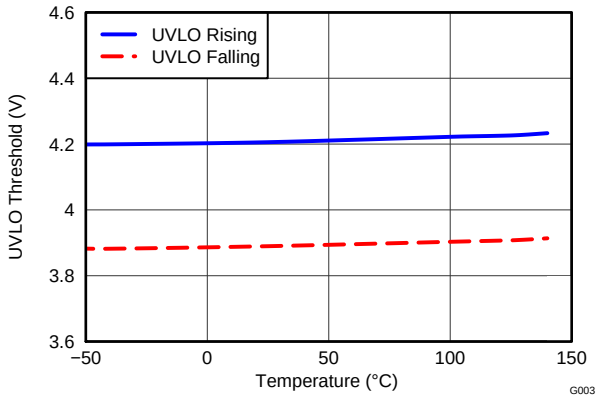


图 8. UVLO Threshold Voltage vs Temperature

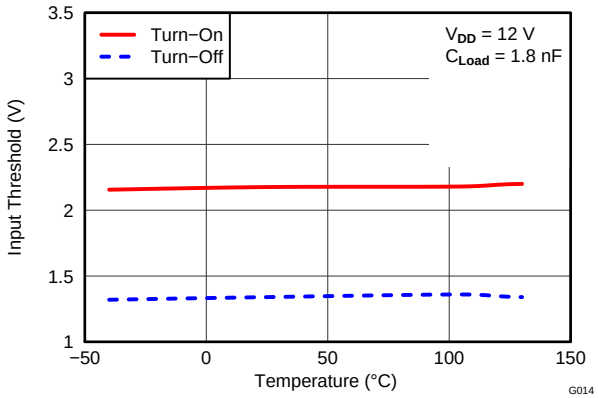


图 9. Input Threshold vs Temperature

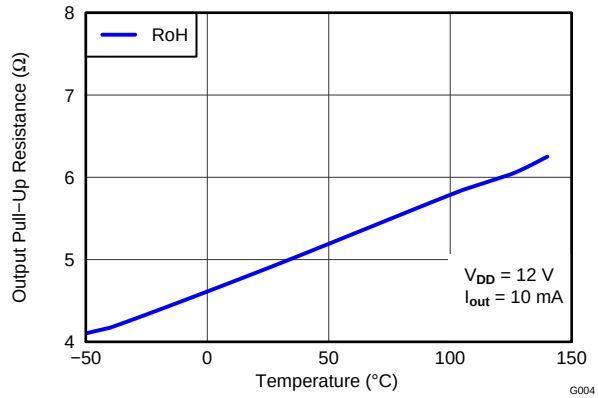


图 10. Output Pullup Resistance vs Temperature

Typical Characteristics (接下页)

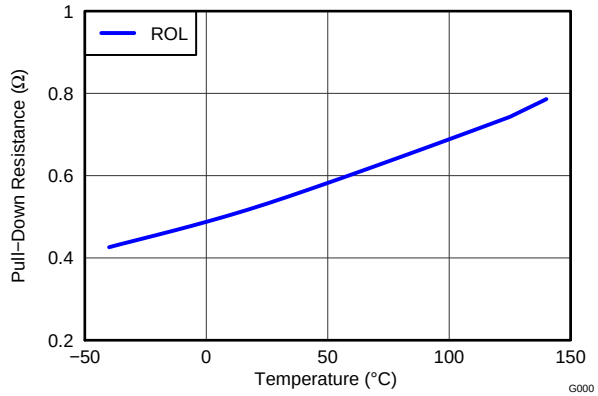


图 11. Output Pulldown Resistance vs Temperature

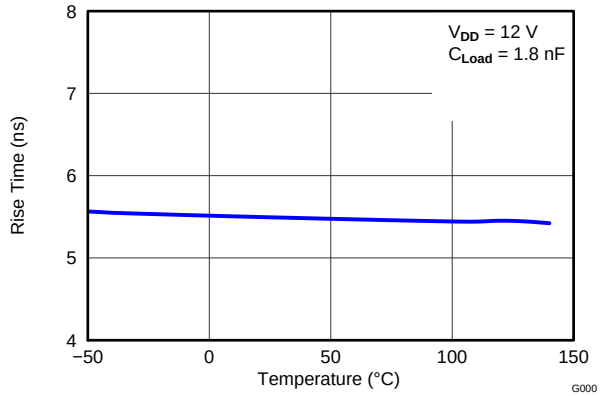


图 12. Rise Time vs Temperature

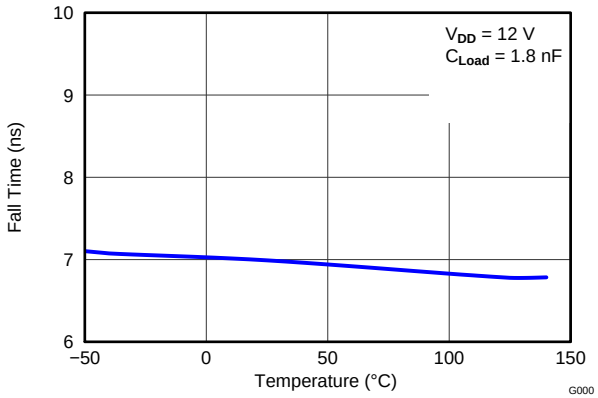


图 13. Fall Time vs Temperature

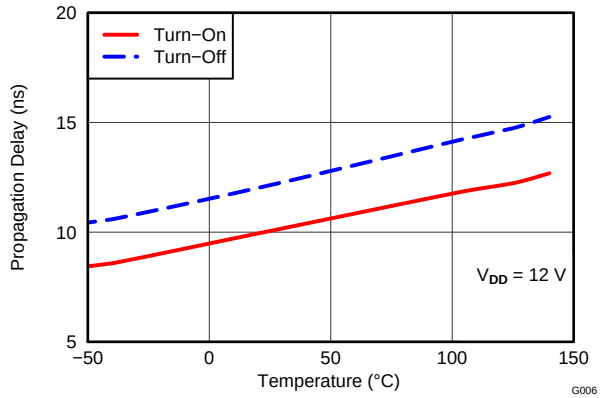


图 14. Input To Output Propagation Delay vs Temperature

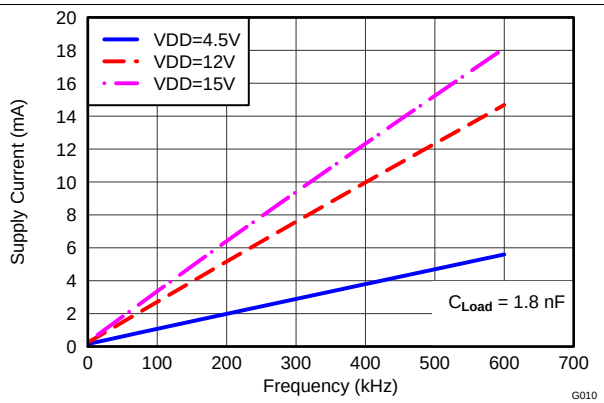


图 15. Operating Supply Current vs Frequency

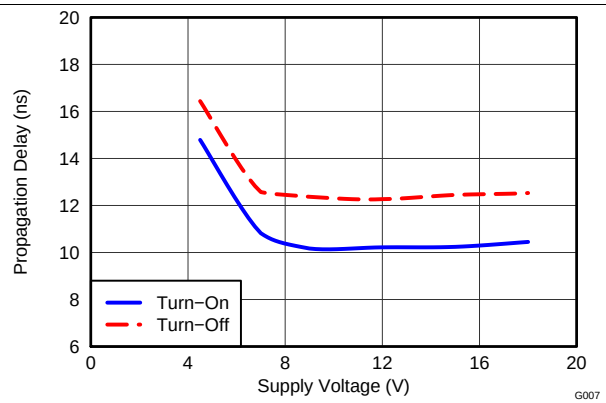


图 16. Propagation Delays vs Supply Voltage

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Typical Characteristics (接下页)

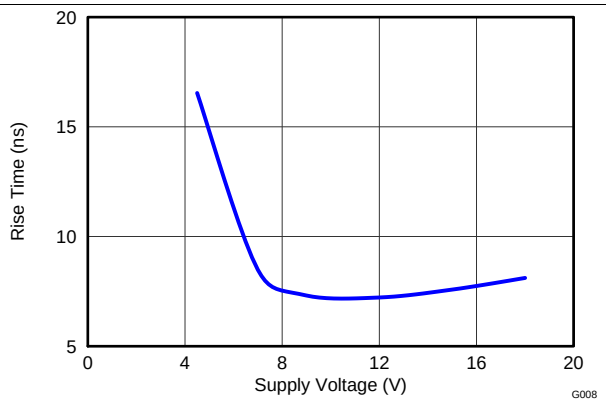


图 17. Rise Time vs Supply Voltage

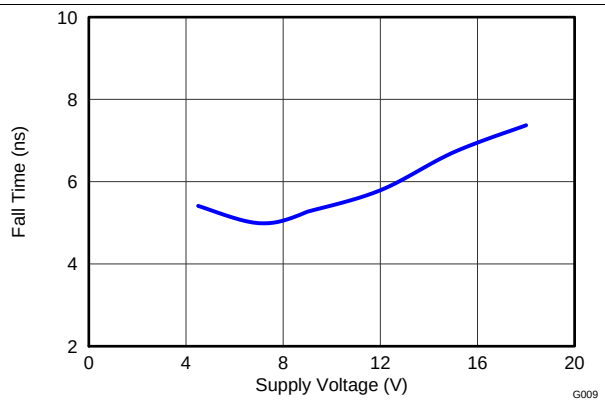


图 18. Fall Time vs Supply Voltage

9 Detailed Description

9.1 Overview

The UCC2751x single-channel, high-speed, low-side gate-driver device can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC2751x device can source and sink high peak-current pulses into capacitive loads, offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical). The UCC2751x device provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability. The UCC27511 device is designed to operate over a wide V_{DD} range of 4.5 to 18 V, and a wide temperature range of –40°C to 140°C.

Internal UVLO circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in-class switching characteristics, is suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The UCC2751x device features a dual-input design which offers flexibility of implementing both inverting (IN– pin) and noninverting (IN+ pin) configuration with the same device. Either the IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For system robustness, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation. The input pin threshold of the device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

表 2. UCC2751x Family of Features and Benefits

FEATURE	BENEFIT
High Source/Sink Current Capability 4 A/8 A (Asymmetrical) – UCC27511/2 4 A/4 A (Symmetrical) – UCC2751x	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low-pulse transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design Low VDD operation ensures compatibility with emerging wide-bandgap power devices such as GaN
Expanded Operating Temperature range of -40°C to 140°C (See *Electrical Characteristics* table)	
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable glitch-free operation at power up and power down
Outputs held low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Ability of input pins (and enable pin in UCC27518/9) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Split output structure in UCC27511 (OUTH, OUTL)	Allows independent optimization of turnon and turnoff speeds
Strong sink current (8 A) and low pulldown impedance (0.375 Ω) in UCC27511/2	High immunity to C x dV/dt Miller turnon events
CMOS/TTL compatible input threshold logic with wide hysteresis in UCC27511/2/6/7	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
CMOS input threshold logic in UCC27518/9 (VIN_H – 70% VDD, VIN_L – 30% VDD)	Well suited for slow input-voltage signals, with flexibility to program delay circuits (RCD)

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9.2 Functional Block Diagrams

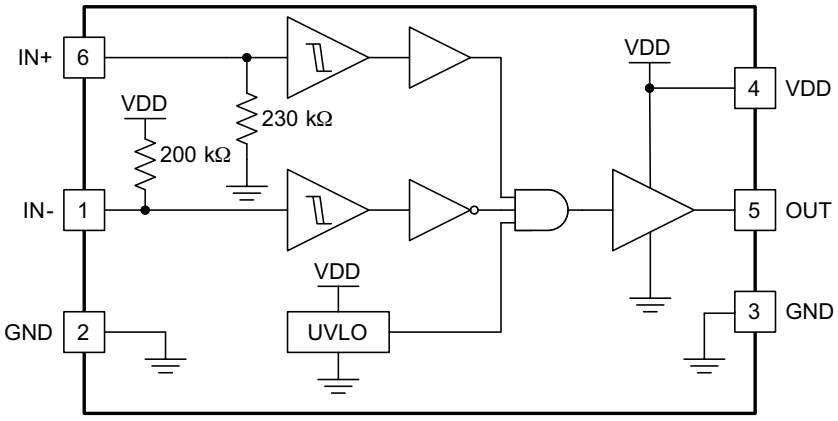


图 19. UCC27516 Functional Block Diagram

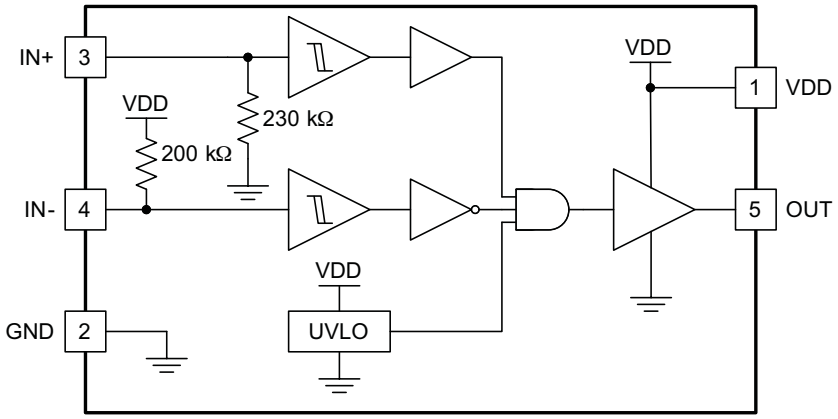


图 20. UCC27517 Functional Block Diagram

9.3 Feature Description

9.3.1 VDD and Undervoltage Lockout

The UCC2751x devices have internal UVLO protection feature on the VDD-pin supply-circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage is less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD}-supply voltages have noise from the power supply and also when there are droops in the VDD-bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide-bandgap power-semiconductor devices.

For example, at power up, the UCC2751x driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the noninverting operation (PWM signal applied to IN+ pin) shown below, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) shown below the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high-state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached.

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Feature Description (接下页)

Because the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-μF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 μF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

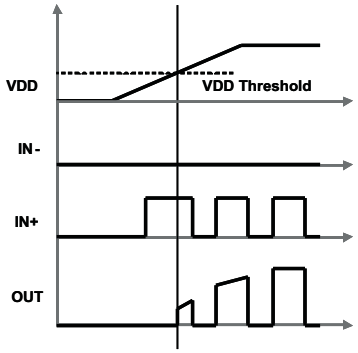


图 21. Power Up (Noninverting Drive)

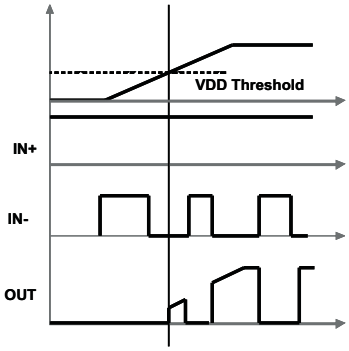


图 22. Power Up (Inverting Drive)

9.3.2 Operating Supply Current

The UCC2751x features very low quiescent I_{DD} currents. The typical operating-supply current in Undervoltage-Lockout (UVLO) state and fully-on state (under static and switching conditions) are summarized in 图 5, 图 6, and 图 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, see 图 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pullup resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pullup resistors (refer to *Functional Block Diagrams* for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the IDD current as a function of switching frequency at different VDD bias voltages under 1.8-nF switching load is provided in 图 15. The strikingly-linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to the high-speed characteristics of I_{OUT}.

9.3.3 Input Stage

The input pins of the UCC27516 and UCC27517 devices are based on a TTL/CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typ high threshold = 2.2 V and typ low threshold = 1.2 V, the logic-level thresholds can be conveniently driven with PWM-control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (typ 1 V) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input-pin threshold-voltage levels which eases system-design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD-pullup resistors on all the inverting inputs (IN- pin) or GND-pulldown resistors on all the noninverting input pins (IN+ pin), (refer to *Functional Block Diagrams*).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a noninverting input pin (IN+) or an inverting input pin (IN-). The state of the output pin is dependent on the bias on both the IN+ and IN- pins. Refer to the input/output logic truth table (表 3) and the Typical Application Diagrams, (图 24 and 图 25), for additional clarification.

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Feature Description (接下页)

Once an input pin has been chosen for PWM drive, the other input pin (the *unused* input pin) must be properly biased in order to enable the output. As mentioned earlier, the *unused* input pin cannot remain in a floating condition because, whenever any input pin is left in a floating condition, the output is disabled for safety purposes. Alternatively, the *unused* input pin can effectively be used to implement an enable and disable function, as explained below.

- To drive the device in a noninverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the *unused* input pin, IN-, must be biased low (eg. tied to GND) in order to enable the output.
  - Alternately, the IN- pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN- is biased high and OUT is enabled when IN- is biased low.
- To drive the device in an inverting configuration, apply the PWM-control input signal to IN- pin. In this case, the *unused* input pin, IN+, must be biased high (eg. tied to VDD) in order to enable the output.
  - Alternately, the IN+ pin can be used to implement the enable/disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.
- Finally, note that the output pin is driven into a high state *only* when IN+ pin is biased high and IN- input is biased low.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly-varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitics causes ground bounce. Because the device features just one GND pin, which may be referenced to the power ground, the differential voltage between input pins and GND is modified and triggers an unintended change of output state. Because of fast 13-ns propagation delay, high-frequency oscillations ultimately occur, which increases power dissipation and poses risk of damage.
- 1-V input-threshold hysteresis boosts noise immunity compared to most other industry-standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between input pin and ground very close to the driver device is necessary. This helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate-driver device package and transferring the gate driver into the external resistor.

9.3.4 Enable Function

As mentioned earlier, an enable/disable function is easily implemented in the UCC27516 and UCC27517 using the *unused* input pin. When IN+ is pulled down to GND or IN- is pulled down to VDD, the output is disabled. Thus IN+ pin is used like an enable pin that is based on active-high logic, while IN- can be used like an enable pin that is based on active-low logic.

9.3.5 Output Stage

The UCC27516 and UCC27517 devices can deliver 4-A source, 4-A sink (symmetrical drive) at VDD = 12 V. The output stage of the UCC27516 and UCC27517 devices are illustrated in 图 23. The UCC27516 and UCC27517 devices features a unique architecture on the output stage which delivers the highest peak-source current when most needed during the Miller-plateau region of the power-switch turnon transition (when the power-switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device delivers a brief boost in the peak-sourcing current enabling fast turnon.

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Feature Description (接下页)

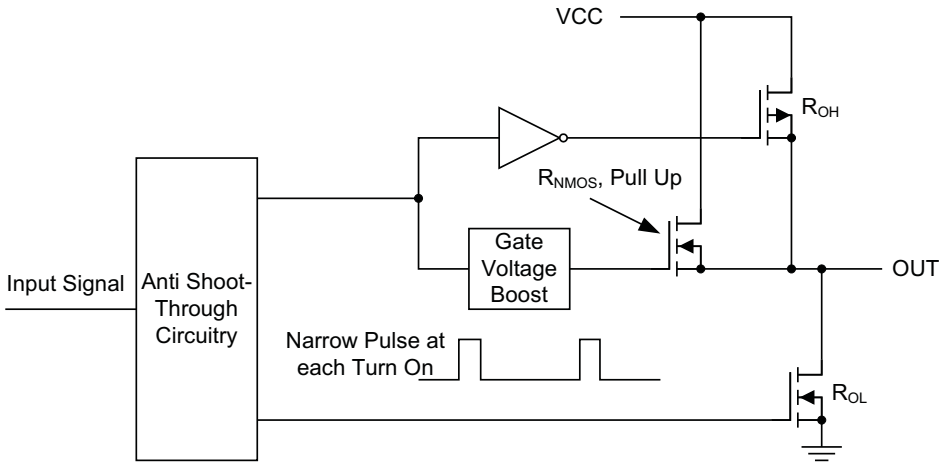


图 23. UCC2751x Gate Driver Output Structure

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and is representative of the on-resistance of the P-Channel device only, because the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In the UCC27516 and UCC27517, the effective resistance of the hybrid pullup structure is approximately $1.4 \times R_{OL}$.

The driver-output voltage swings between VDD and GND providing rail-to-rail operation because of the MOS output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

9.3.6 Low Propagation Delays

The UCC27516 and UCC27517 driver devices feature best-in-class input-to-output propagation delay of 13 ns (typ) at VDD = 12 V. This promises the lowest level of pulse-transmission distortion available from industry-standard gate-driver devices for high-frequency switching applications. As seen in 图 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

9.4 Device Functional Modes

表 3. Device Logic Table

IN+ PIN	IN- PIN	OUT PIN
L	L	L
L	H	L
H	L	H
H	H	L
x(1)	Any	L
Any	x(1)	L

(1) x = Floating Condition

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10 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

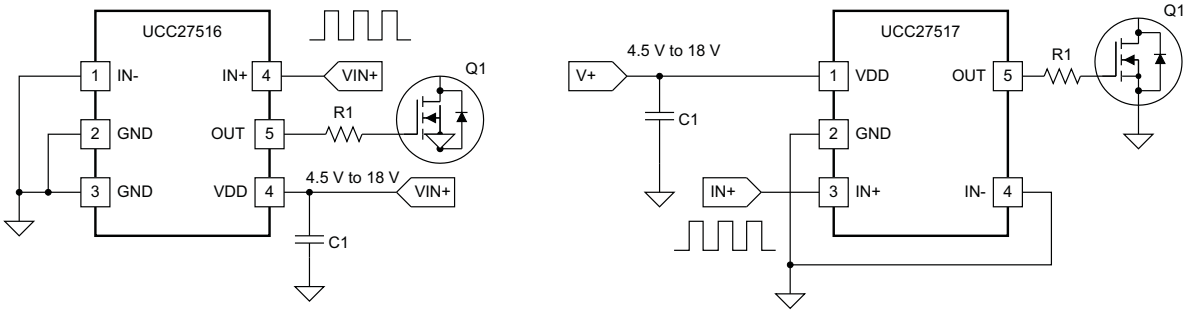
High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when there are times that the PWM controller cannot directly drive the gates of the switching devices. With advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Because traditional buffer-drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter-follower configurations, lack level-shifting capability, the circuits prove inadequate with digital power. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate-charge power losses into itself. Finally, emerging wide-bandgap power-device technologies, such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate-drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction with a simplified system design.

10.2 Typical Application

The UCC27516 and UCC27517 devices can be used in non-inverting and inverting driver configurations.

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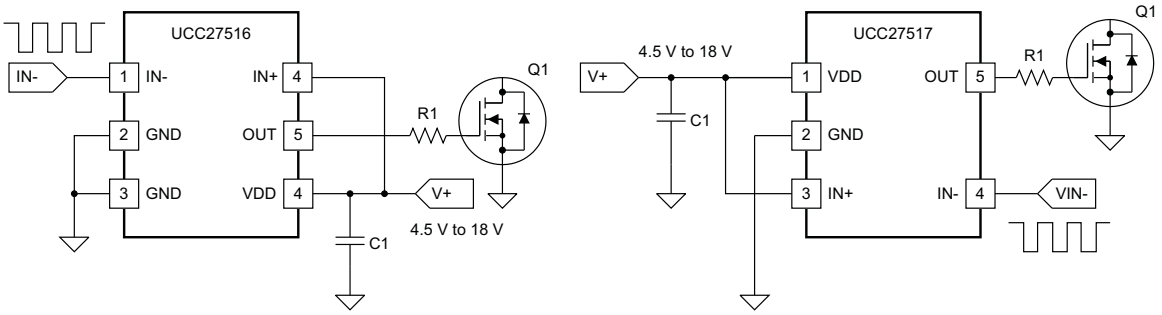
The UCC27516 features two ground pins, pin 2 and pin 3. TI recommends tying both pins together using PCB trace as close as possible to the device.



(IN- Is Grounded to the Enable Output)

图 24. Using Noninverting Input

Typical Application (接下页)



(IN+ Is Tied to VDD Enable Output)

图 25. Using Inverting Input

10.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type.

表 4. Design Parameters

Design Parameter	Example Value
Input-to-Output Logic	Non-Inverting
Input Threshold Type	Logic Level
VDD Bias Supply Voltage	10 V (Minimum), 13 V (Nominal), 15 V (Peak)
Peak Source and Sink Currents	Minimum 3 A Source, Minimum 3 A Sink
Enable and Disable Function	Yes, Needed
Propagation Delay	Maximum 40 ns or less

10.2.2 Detailed Design Procedure

10.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. The UCC27516 and UCC27517 devices can be configured in either an inverting or noninverting input-to-output configuration, using the IN– or IN+ pins, respectively. To configure the device for use in inverting mode, tie the IN+ pin to V_{DD} and apply the input signal to the IN– pin. For the non inverting configuration, tie the IN– pin to GND and apply the input signal to the IN+ pin.

10.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller used with the gate driver device. The UCC27516 and UCC27517 devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers, as well as higher-voltage input signals from analog controllers. See *Electrical Characteristics* for the actual input threshold voltage levels and hysteresis specifications for the UCC27516 and UCC27517 devices.

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10.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27516 and UCC27517 devices can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10 V, 12 V), IGBTs (VGE = 15 V, 18 V), and wide-band gap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

10.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible, to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20V/ns or higher, under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20 ns or less.

When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to the power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, VGS(TH). To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27516 and UCC27517 gate driver is capable of providing 4-A peak sourcing current, which exceeds the design requirement and has the capability to meet the switching speed needed.

The 2.4x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET, along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver.

To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ $\times I_{PEAK}$ × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical).

If the parasitic trace inductance limits the dI/dt, then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

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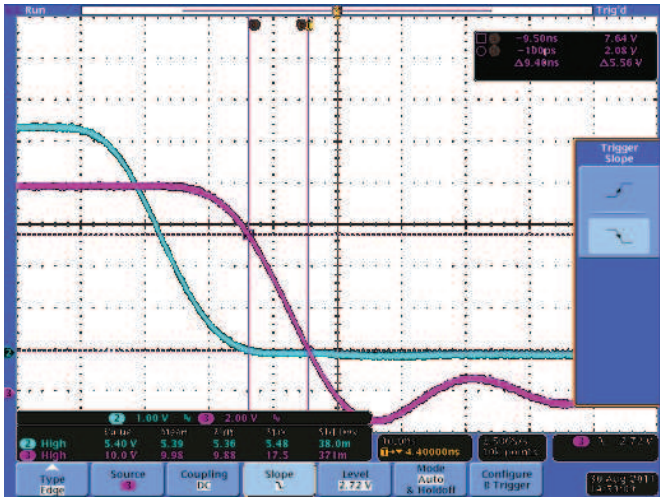
10.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver, without involving the input signal. A pin offering an enable and disable function achieves this requirement. The UCC27516 and UCC27517 devices offer two input pins, IN+ and IN–, both of which control the state of the output as listed in 表 3. Based on whether an inverting or non inverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other unused input pin can be used for the enable and disable functionality. If the design does not require an enable function, the unused input pin can be tied to either the V_{DD} pin (in case IN+ is the unused pin), or GND (in case IN– is unused pin) to ensure it does not affect the output status.

10.2.2.6 Propagation Delay

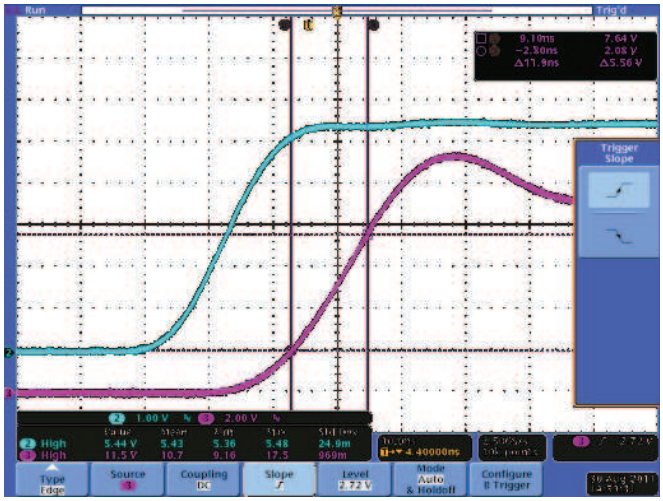
The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used, and the acceptable level of pulse distortion to the system. The UCC27516 and UCC27517 devices feature industry best-in-class 13-ns (typical) propagation delays, which ensure very little pulse distortion and allow operation at very high-frequencies. See *Switching Characteristics* for the propagation and switching characteristics of the UCC27516 and UCC27517 devices.

10.2.3 Application Curves



V_{DD} = 10 V $C_{(LOAD)}$ = 1 nF

图 26. Typical Turnon Waveform



V_{DD} = 10 V $C_{(LOAD)}$ = 1 nF

图 27. Typical Turnoff Waveform

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11 Power Supply Recommendations

The bias supply voltage range for which the UCC27516 and UCC27517 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal UVLO protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device, to avoid triggering a device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Keep in mind that the charge for source current pulses delivered by the OUT pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the V_{DD} pin. Therefore, ensure that local bypass capacitors are provided between the V_{DD} and GND pins, and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. TI recommends using 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device, and another surface-mount capacitor of few microfarads added in parallel.

12 Layout

12.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27516 and UCC27517 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of the power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A/4-A peak current is at VDD = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch or the ground of PWM controller at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

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Layout Guidelines (接下页)

- In noisy environments, tying the unused input pin of UCC27516 and UCC27517 to VDD (in case of IN+) or GND (in case of IN–) using short traces to ensure that the output is enabled and to prevent noise from causing malfunction in the output is necessary.
- The UCC27516 device offers two ground pins, pin 2 and pin 3. Shorting the two pins together using the PCB trace is extremely important. The shortest trace should be located as close as possible to the device.

12.2 Layout Example

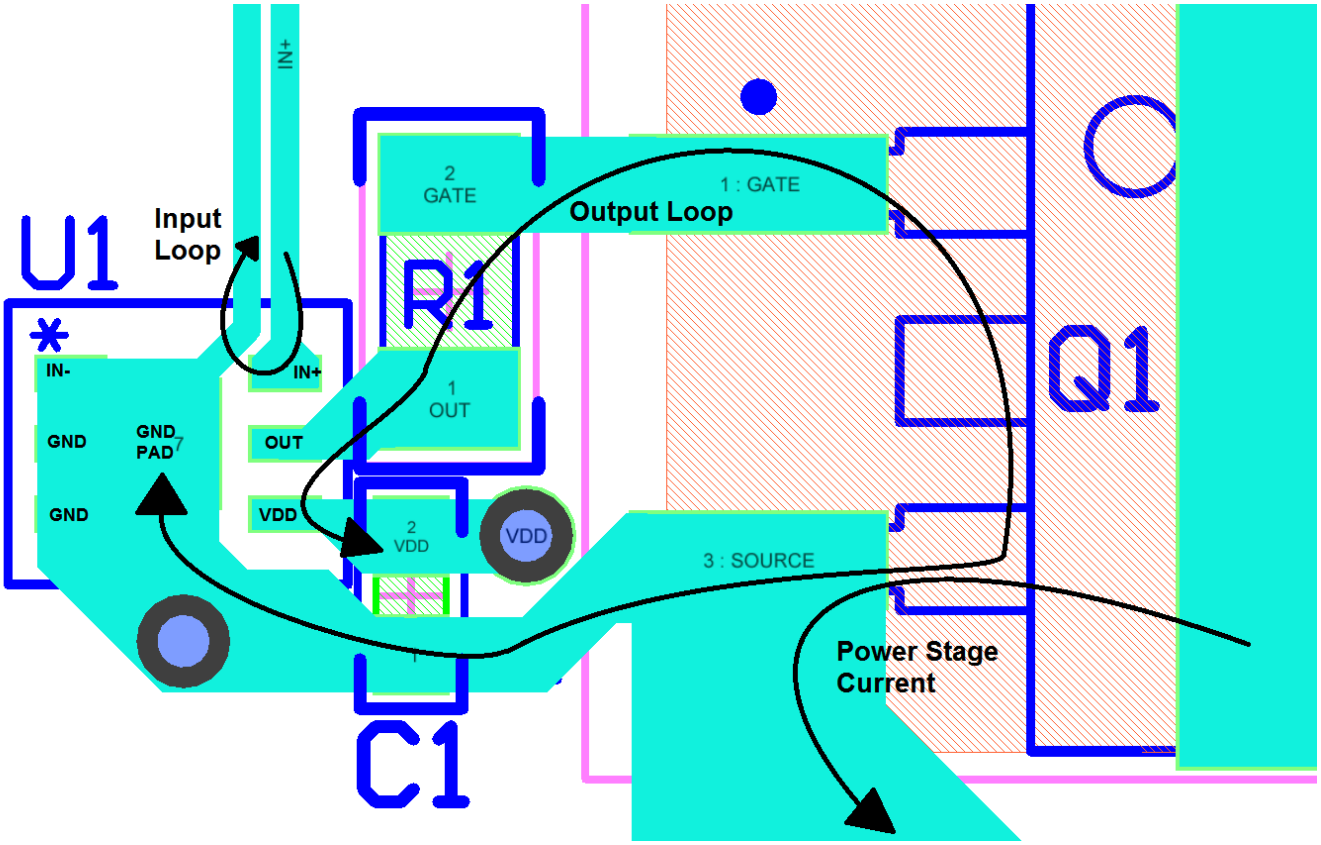


图 28. UCC27516DRS in Noninverting Configuration

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Layout Example (接下页)

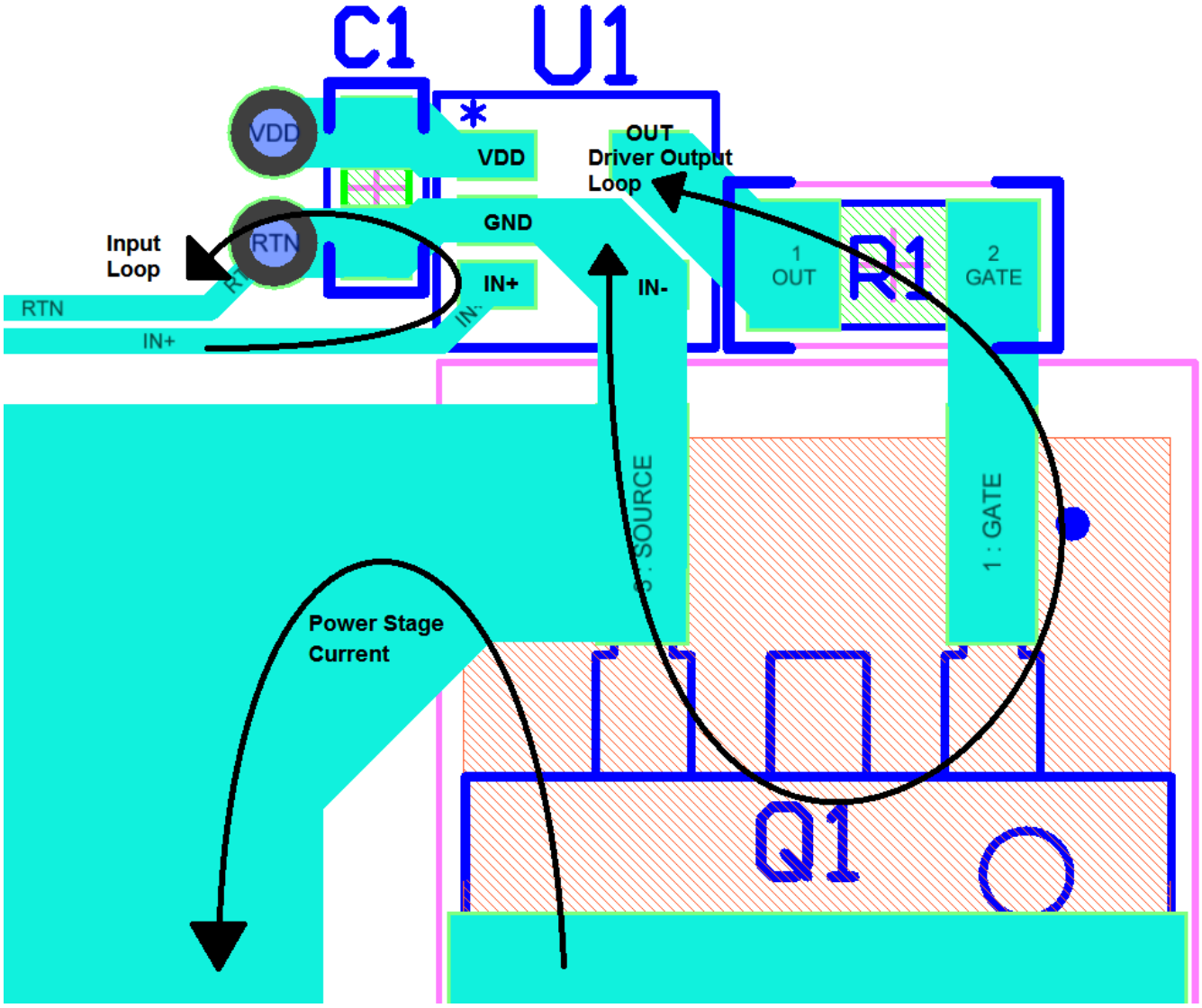


图 29. UCC27517DBV in Noninverting Configuration

12.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in *Thermal Information*. For detailed information regarding the thermal information table, refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

The UCC27516 and UCC27517 devices are offered in SOT-23, 5-pin package (DBV) and 3 mm × 3 mm, WSON 6-pin package with exposed thermal pad (DRS), respectively. The *Thermal Information* table summarizes the thermal performance metrics related to the two packages. $R_{\theta JA}$ metric should be used for comparison of power dissipation between different packages. Under identical power dissipation conditions, the DRS package will maintain a lower die temperature than the DBV. The ψ_{JT} and ψ_{JB} metrics should be used when estimating the die temperature during actual application measurements.

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Thermal Considerations (接下页)

The DRS is a better thermal package overall because of the exposed thermal pad and ability to sink heat to the PCB better than the DBV. The thermal pad in DRS package provides designers with an ability to create an excellent heat removal subsystem from the vicinity of the device, thus helping to maintain a lower junction temperature. This pad should be soldered to the copper on the printed circuit board directly underneath the device package. Then a printed circuit board designed with thermal lands and thermal vias completes a very efficient heat removal subsystem. In such a design, the heat is extracted from the semiconductor junction through the thermal pad, which is then efficiently conducted away from the location of the device on the PCB through the thermal network. This extraction helps to maintain a lower board temperature near the vicinity of the device leading to an overall lower device-junction temperature.

In comparison, for the DBV package, heat removal occurs primarily through the leads of the device and the PCB traces connected to the leads.

Note that the exposed pad in DRS package is not directly connected to any leads of the package. However, the DRS package is electrically and thermally connected to the substrate of the device which is the ground of the device. TI recommends to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

12.4 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 公式 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through etc). The UCC27516 and UCC27517 features very low quiescent currents (less than 1 mA, refer 图 7) and contains internal logic to eliminate any shoot-through in the output-driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external-gate resistors.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly easy. The energy that must be transferred from the bias supply to charge the capacitor is given by 公式 2.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

Where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

(2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by 公式 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency

(3)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD}$ x V_{DD}, to provide 公式 4 for power:

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Power Dissipation (接下页)

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or turned off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in 公式 5.

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \quad (5)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pullup structure) = 1.4 x R_{OL}

13 器件和文档支持

13.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 5. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
UCC27516	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC27517	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 商标

All trademarks are the property of their respective owners.

13.3 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27516DRSR	ACTIVE	SON	DRS	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27516	Samples
UCC27516DRST	ACTIVE	SON	DRS	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27516	Samples
UCC27517DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 140	7517	Samples
UCC27517DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 140	7517	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

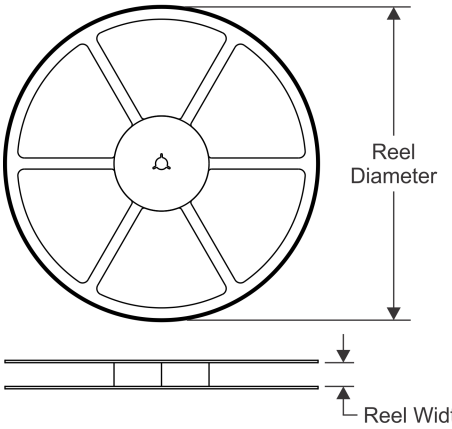
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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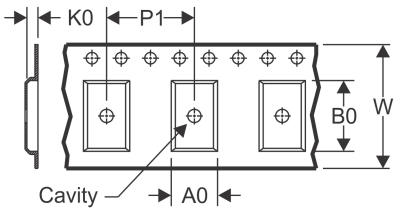
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

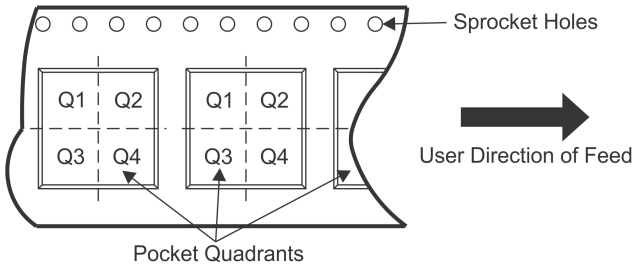


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

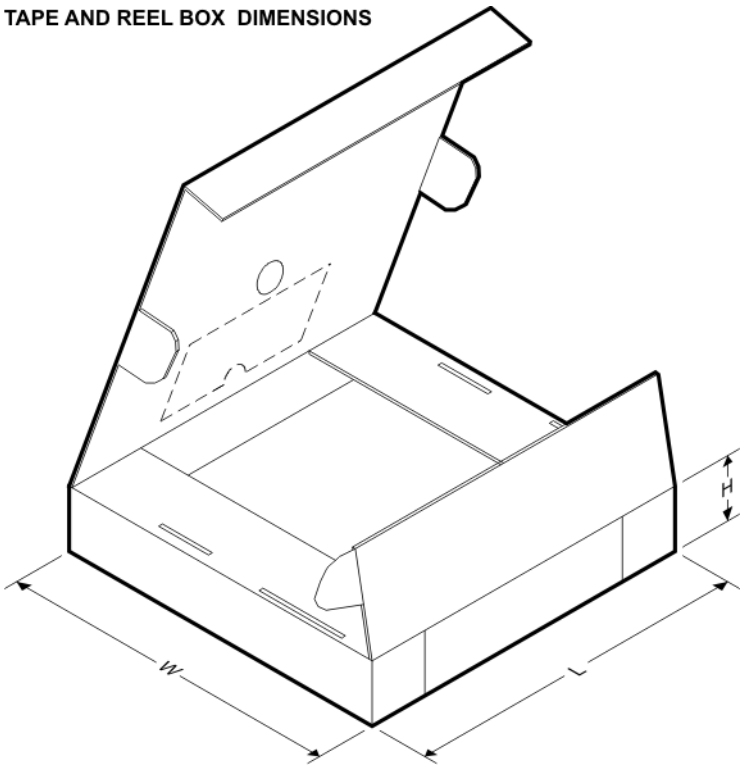
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27516DRSR	SON	DRS	6	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27516DRST	SON	DRS	6	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27517DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27517DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27517DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

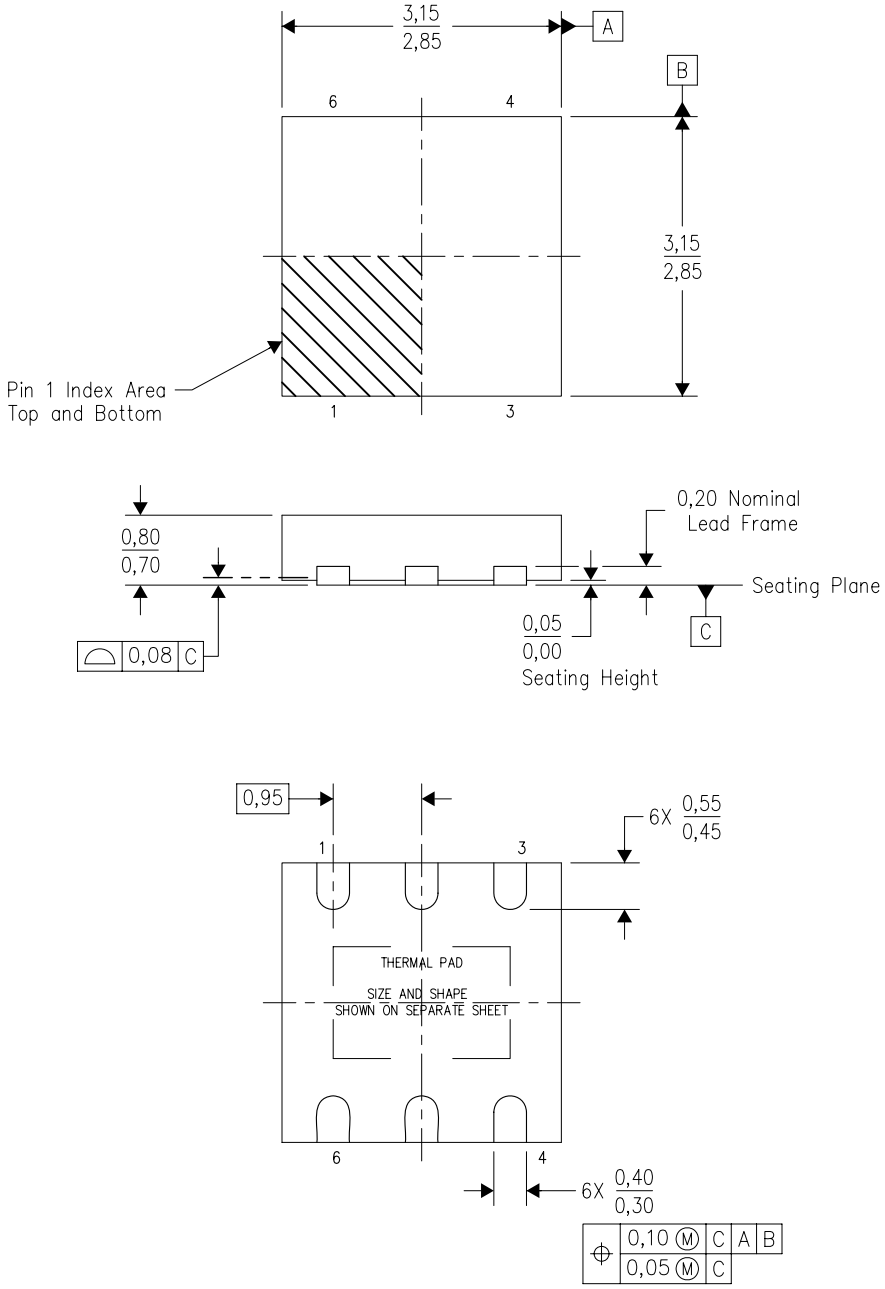
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27516DRSR	SON	DRS	6	3000	367.0	367.0	35.0
UCC27516DRST	SON	DRS	6	250	210.0	185.0	35.0
UCC27517DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
UCC27517DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
UCC27517DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206219/F 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

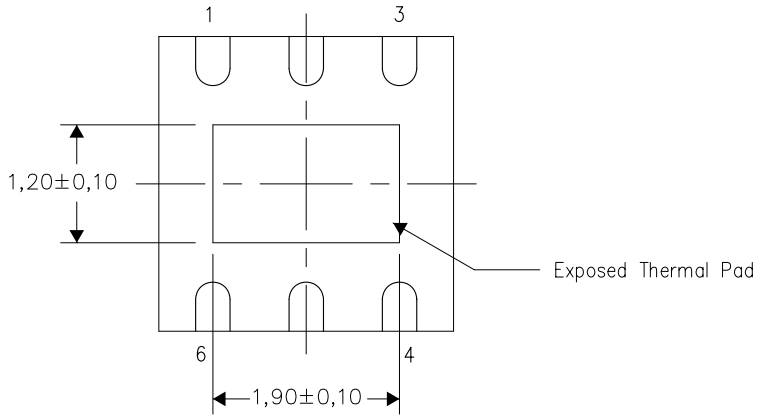
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



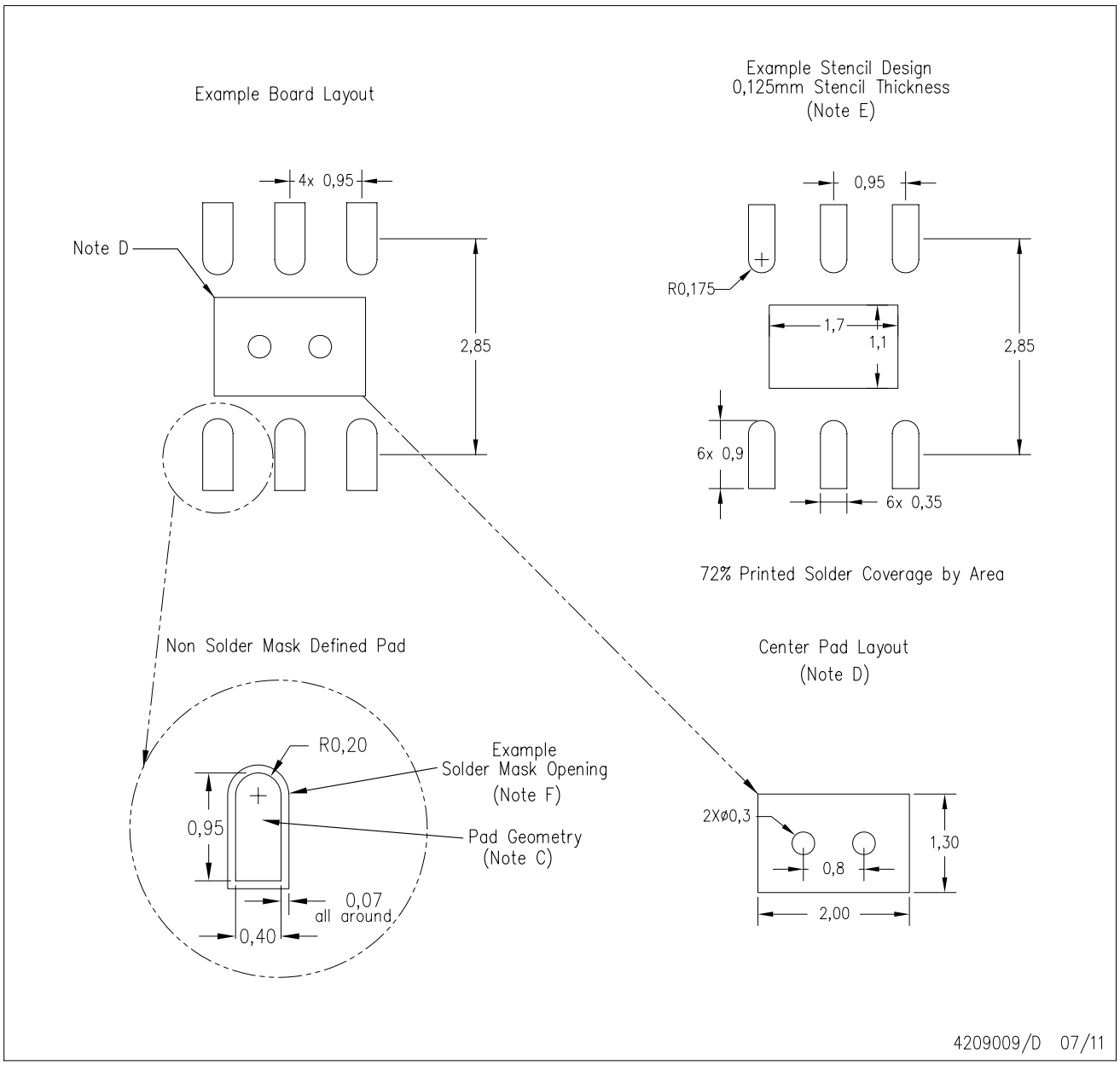
Bottom View

Exposed Thermal Pad Dimensions

4207663/E 07/11

NOTE: All linear dimensions are in millimeters

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



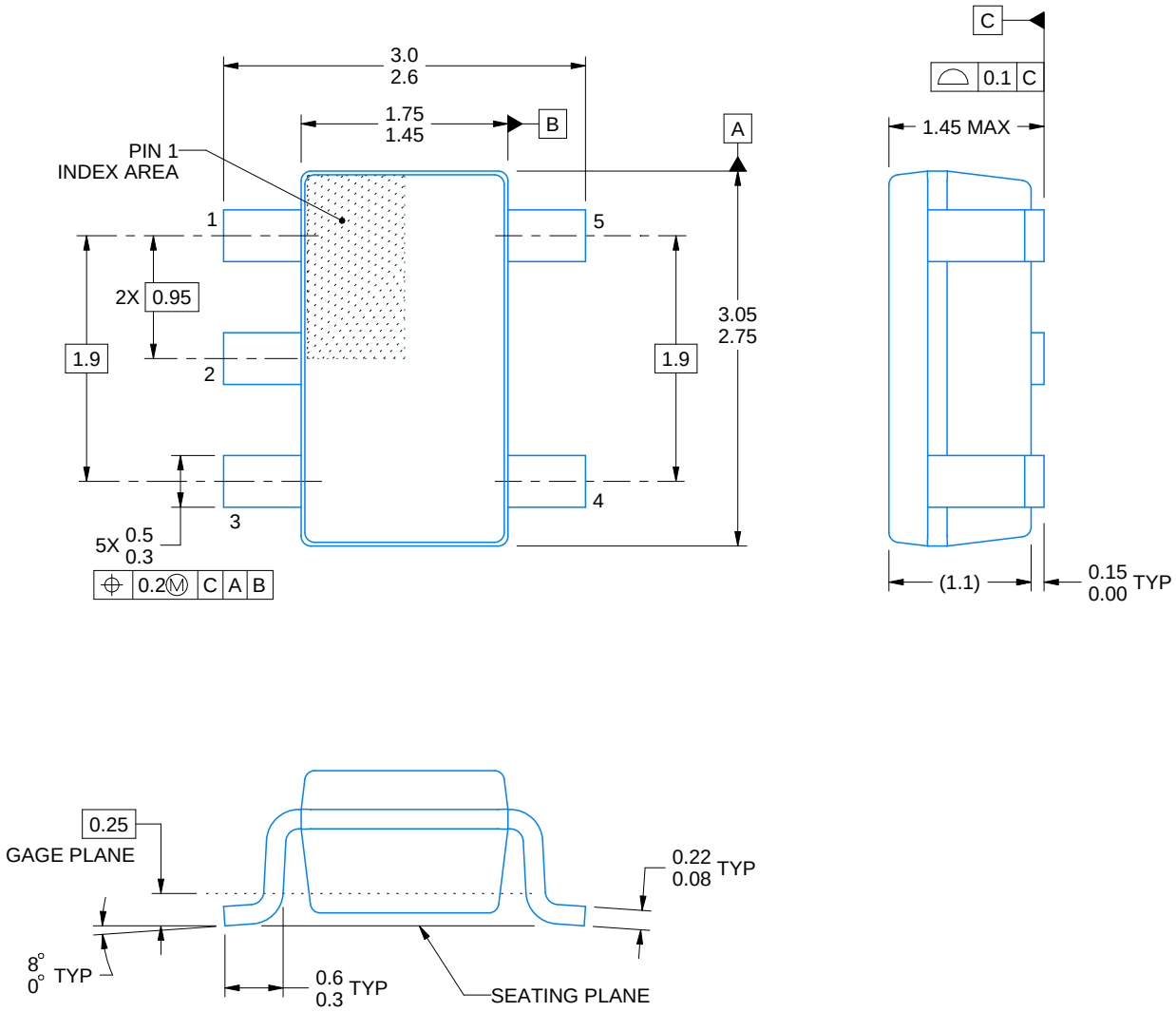
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

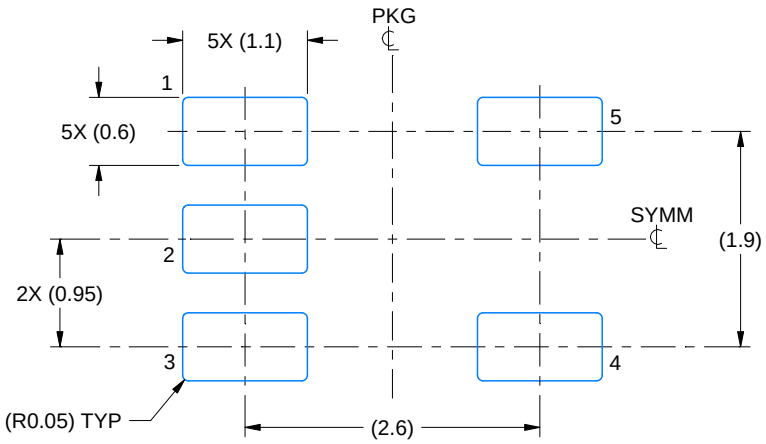
SMALL OUTLINE TRANSISTOR



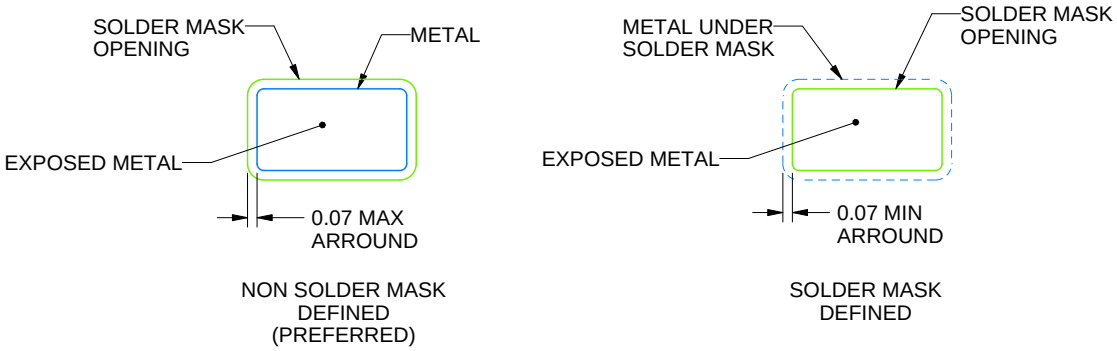
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

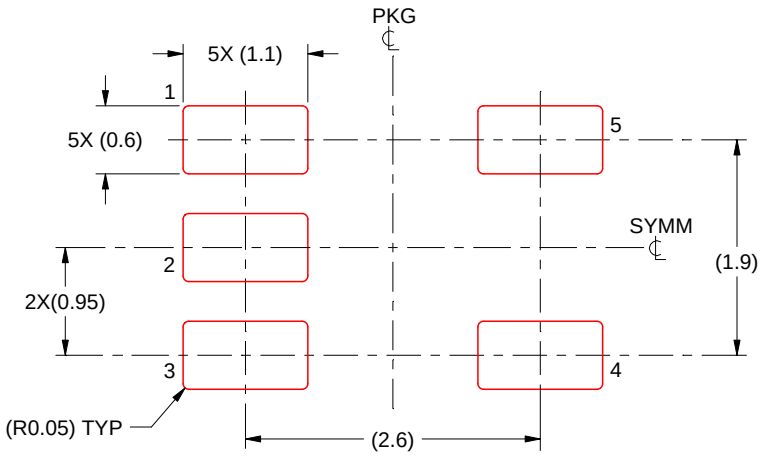


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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