LM5134 具有 PILOT 输出的单路 7.6A 峰值电流低侧栅极驱动器

1 特性

- 主输出具有 7.6A/4.5A 的峰值灌电流/拉电流驱动能力
- PILOT 输出具有 820mA/660mA 的峰值灌电流/拉电流驱动能力
- 4V 至 12.6V 单电源
- 反相和非反相输入之间的延迟时间匹配
- TTL/CMOS 逻辑输入
- 高达 14V 的逻辑输入（与 VDD 电压无关）
- –40°C 至 125°C 的结温范围

2 应用

- 电机驱动器
- 固态功率控制器
- 功率因数校正转换器

3 说明

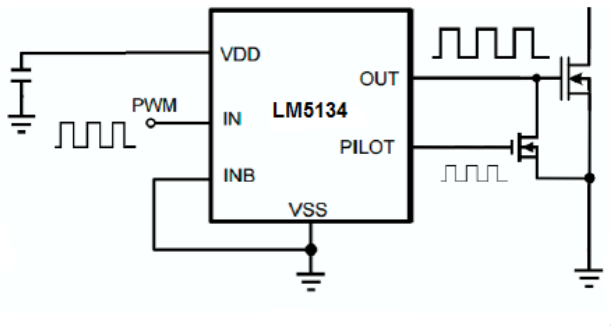
LM5134 是一款高速单路低侧驱动器，具备 7.6A/4.5A 的峰值灌电流/拉电流驱动能力。LM5134 具有反相和非反相输入，为用户控制场效应晶体管 (FET) 提供了更大的灵活性。LM5134 具有 1 个主输出 (OUT) 和 1 个额外的栅极驱动输出 (PILOT)。PILOT 引脚逻辑与 OUT 引脚互补，并且可用于驱动位于主功率 FET 附近的较小 MOSFET。该配置可最大限度减少关断环路，并进一步降低寄生电感。这对于驱动高速 FET 或多个并联的 FET 特别有用。LM5134 提供 6 引脚 SOT-23 封装以及带外露焊盘的 6 引脚 WSON 封装，第二种封装有助于提升散热性能。

器件信息(1)

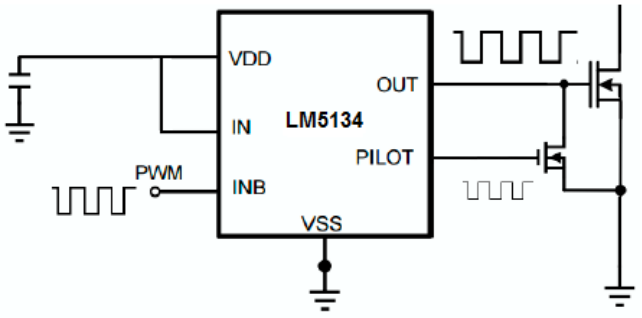
器件型号	封装	封装尺寸（标称值）
LM5134	SOT-23 (6)	2.90mm x 1.60mm
	WSON (6)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

非反相输入



反相输入



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (April 2013) to Revision C **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

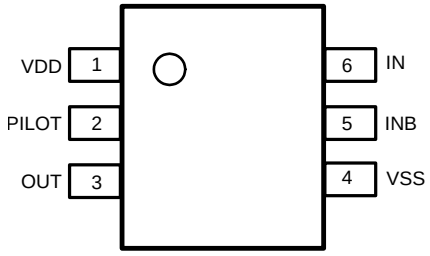
Changes from Revision A (April 2013) to Revision B **Page**

- Changed layout of National Data Sheet to TI format ... 18

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5 Pin Configuration and Functions

DBV Package, NGG Package
6-Pin SOT-23, 6-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.			
VDD	1	—	Gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close as possible to the IC.
PILOT	2	O	Gate drive output for an external turnoff FET	Connect to the gate of a small turnoff MOSFET with a short, low inductance path. The turnoff FET provides a local turnoff path.
OUT	3	O	Gate drive output for the power FET	Connect to the gate of the power FET with a short, low inductance path. A gate resistor can be used to eliminate potential gate oscillations.
VSS	4	—	Ground	All signals are referenced to this ground.
INB	5	I	Inverting logic input	Connect to VSS when not used.
IN	6	I	Non-inverting logic input	Connect to VDD when not used.
EP	EP	—	Exposed Pad	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PC board, and that ground plane extend out from beneath the IC to help dissipate heat.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage	VDD to VSS	−0.3	14	V
	IN, INB to VSS	−0.3	14	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Gate drive supply, VDD	4		12.6	V
Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM5134		UNIT
		DBV (SOT-23)	NGG (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.9	51	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21	25.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.5	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = 25°C, VDD = 12 V, unless otherwise specified. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.[1].

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
VDD	VDD operating voltage	T_J = –40°C to +125°C		4		12.6	V
UVLO	VDD undervoltage lockout	VDD rising	T_J = 25°C		3.6		V
			T_J = –40°C to +125°C	3.25		4	
	VDD undervoltage lockout hysteresis				0.36		V
	VDD undervoltage lockout to main output delay time	VDD rising			500		ns
I_{DD}	VDD quiescent current	IN = INB = VDD	T_J = 25°C		0.8		mA
			T_J = –40°C to +125°C			2	
OUTPUT							
R_{ON-DW} (SOT23-6)	Main output resistance – pulling down	VDD = 10 V, I_{OUT} = –100 mA	T_J = 25°C		0.15		Ω
			T_J = –40°C to +125°C			0.45	
		VDD = 4.5 V, I_{OUT} = –100 mA	T_J = 25°C		0.2		Ω
			T_J = –40°C to +125°C			0.5	
R_{ON-DW} (WSON)	Main output resistance – pulling down	VDD = 10 V, I_{OUT} = –100 mA	T_J = 25°C		0.2		Ω
			T_J = –40°C to +125°C			0.5	
		VDD = 4.5 V, I_{OUT} = –100 mA	T_J = 25°C		0.25		Ω
			T_J = –40°C to +125°C			0.55	
	Power-off pulldown resistance	VDD = 0 V, I_{OUT} = –10 mA			1.5	10	Ω
	Power-off pulldown clamp voltage	VDD = 0 V, I_{OUT} = –10 mA			0.7	1	V
	Peak sink current	C_L = 10,000 pF			7.6		A

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

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Electrical Characteristics (continued)

T_J = 25°C, VDD = 12 V, unless otherwise specified. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{ON-UP} (SOT23-6)	Main output resistance - pulling up	VDD = 10 V, I_{OUT} = 50 mA	T_J = 25°C		0.7		Ω
			T_J = –40°C to +125°C			1.3	
		VDD = 4.5 V, I_{OUT} = 50 mA	T_J = 25°C		1		Ω
			T_J = –40°C to +125°C			1.9	
R_{ON-UP} (WSON)	Main output resistance - pulling up	VDD = 10 V, I_{OUT} = 50 mA	T_J = 25°C		0.75		Ω
			T_J = –40°C to +125°C			1.2	
		VDD = 4.5 V, I_{OUT} = 50 mA	T_J = 25°C		1.14		Ω
			T_J = –40°C to +125°C			1.85	
	Peak source current	C_L = 10,000 pF			4.5		A
PILOT							
R_{ONP-DW}	PILOT output resistance – pulling down	VDD = 10 V, I_{OUT} = –100 mA	T_J = 25°C		3.7		Ω
			T_J = –40°C to +125°C			9	
		VDD = 4.5 V, I_{OUT} = –100 mA	T_J = 25°C		4.7		Ω
			T_J = –40°C to +125°C			12	
	Peak sink current	C_L = 330 pF			820		mA
R_{ONP-UP}	PILOT output resistance – pulling up	VDD = 10 V, I_{OUT} = 50 mA	T_J = 25°C		6		Ω
			T_J = –40°C to +125°C			11	
		VDD = 4.5 V, I_{OUT} = 50 mA	T_J = 25°C		10.7		Ω
			T_J = –40°C to +125°C			20	
	Peak source current	C_L = 330 pF			660		mA
LOGIC INPUT							
V_{IH}	Logic 1 input voltage	LM5134A, T_J = –40°C to +125°C		0.67 × VDD			V
		LM5134B, T_J = –40°C to +125°C		2.4			
V_{IL}	Logic 0 input voltage	LM5134A, T_J = –40°C to +125°C				0.33 × VDD	V
		LM5134B, T_J = –40°C to +125°C				0.8	
V_{HYS}	Logic-input hysteresis	LM5134A			0.9		V
		LM5134B			0.68		
	Logic-input current	INB = VDD or 0	T_J = 25°C		0.001		µA
			T_J = –40°C to +125°C			10	
THERMAL RESISTANCE							
θ_{JA}	Junction to ambient	SOT23-6			90		°C/W
		WSON-6			60		°C/W

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FOR VDD = +10 V							
t_R	OUT rise time	C_L = 1000 pF			3		ns
		C_L = 5000 pF			10		
		C_L = 10,000 pF			20		
t_F	OUT fall time	C_L = 1000 pF			2		ns
		C_L = 5000 pF			4.7		
		C_L = 10,000 pF			7.2		
t_{D-ON}	OUT turnon propagation delay	C_L = 1000 pF	T_J = 25°C		17		ns
			T_J = –40°C to +125°C			40	
t_{D-OFF}	OUT turnoff propagation delay	C_L = 1000 pF	T_J = 25°C		12		ns
			T_J = –40°C to +125°C			25	
	Main output break-before-make time				2.5		ns
t_{PR}	PILOT rise time	C_L = 330 pF			5.3		ns
t_{PF}	PILOT fall time	C_L = 330 pF			3.9		ns
t_{PD-ON}	OUT turnoff to PILOT turnon propagation delay	C_L = 330 pF			4.2		ns
t_{PD-OFF}	PILOT turnoff to OUT turnon propagation delay	C_L = 330 pF			6.4		ns
FOR VDD = +4.5 V							
t_R	Rise time	C_L = 1000 pF			5		ns
		C_L = 5000 pF			14		
		C_L = 10,000 pF			24		
t_F	Fall time	C_L = 1000 pF			2.3		ns
		C_L = 5000 pF			5.4		
		C_L = 10,00 0pF			7.2		
t_{D-ON}	OUT turnon propagation delay	C_L = 1000 pF	T_J = 25°C		26		ns
			T_J = –40°C to +125°C			50	
t_{D-OFF}	OUT turnoff propagation delay	C_L = 1000 pF	T_J = 25°C		20		ns
			T_J = –40°C to +125°C			45	
	Main output break-before-make time				4.2		ns
t_{PR}	PILOT rise time	C_L = 330 pF			9.6		ns
t_{Pf}	PILOT fall time	C_L = 330 pF			3.7		ns
t_{PD-ON}	OUT turnoff to PILOT turnon propagation delay	C_L = 330 pF			7.5		ns
t_{PD-OFF}	PILOT turnoff to OUT turnon propagation delay	C_L = 330 pF			11.8		ns

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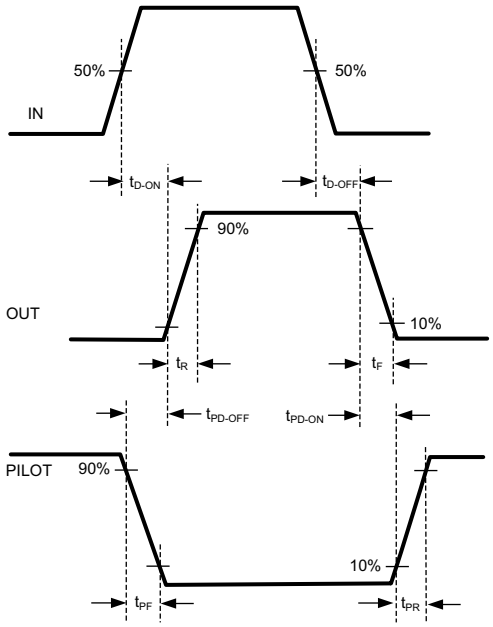


Figure 1. Timing Diagram — Noninverting Input

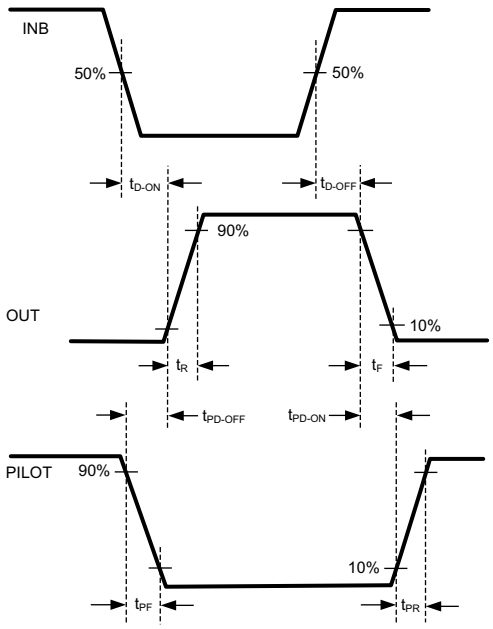


Figure 2. Timing Diagram — Inverting Input

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6.7 Typical Characteristics

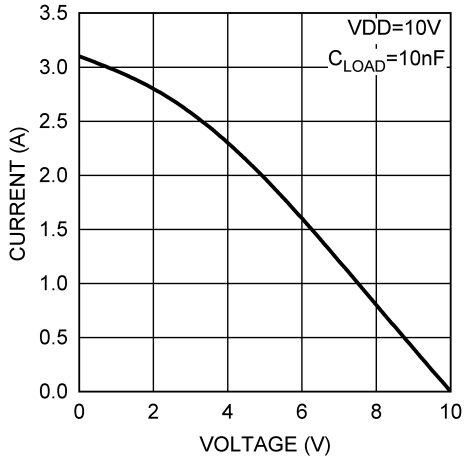


Figure 3. OUT Source Current vs OUT Voltage

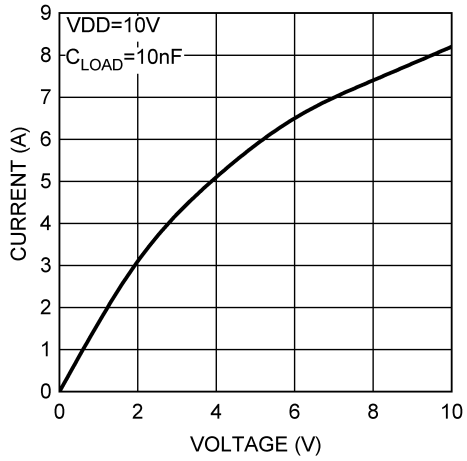


Figure 4. OUT Sink Current vs OUT Voltage

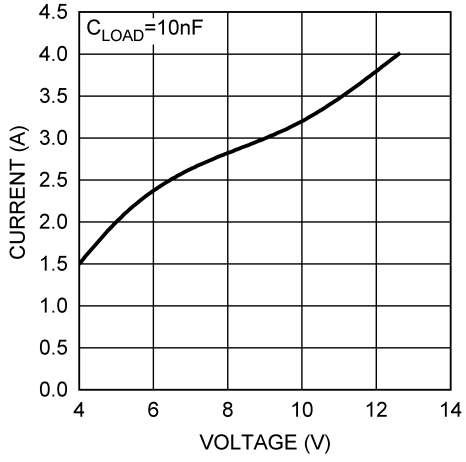


Figure 5. OUT Peak Source Current vs VDD Voltage

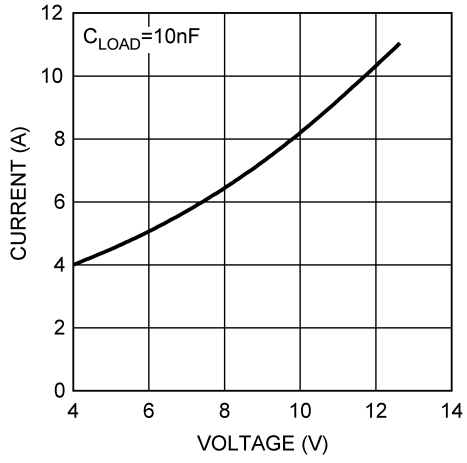


Figure 6. OUT Peak Sink Current vs VDD Voltage

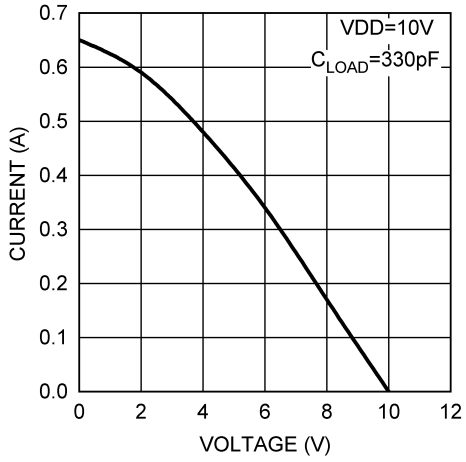


Figure 7. PILOT Source Current vs PILOT Voltage

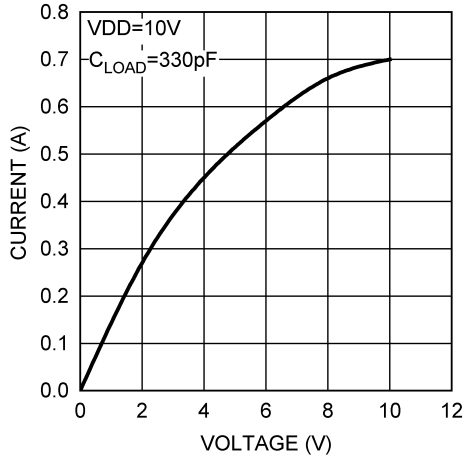


Figure 8. PILOT Sink Current vs PILOT Voltage

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Typical Characteristics (continued)

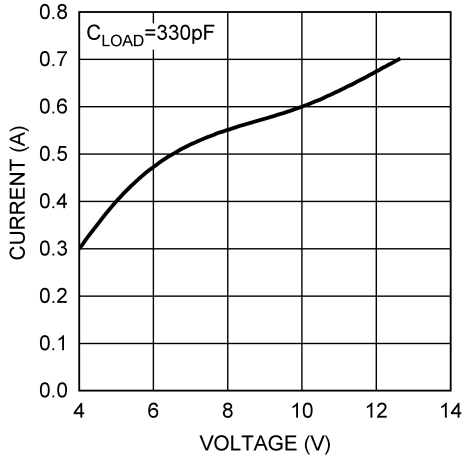


Figure 9. PILOT Peak Source Current vs VDD Voltage

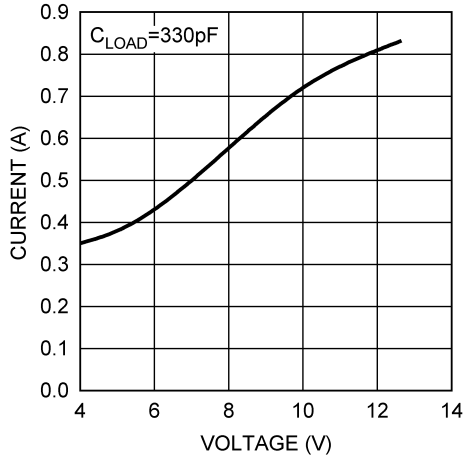


Figure 10. PILOT Peak Sink Current vs VDD Voltage

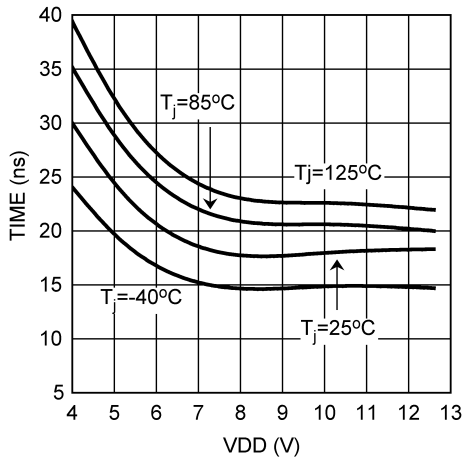


Figure 11. OUT Turnon Propagation Delay vs VDD

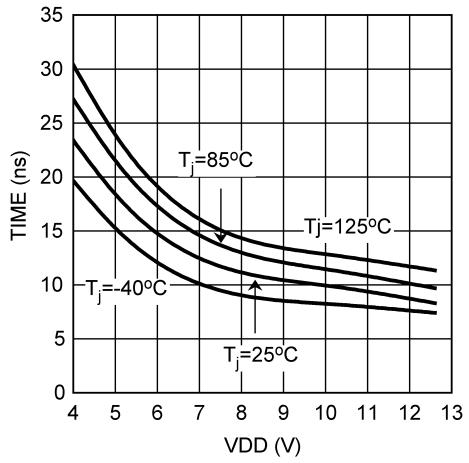


Figure 12. OUT Turnoff Propagation Delay vs VDD

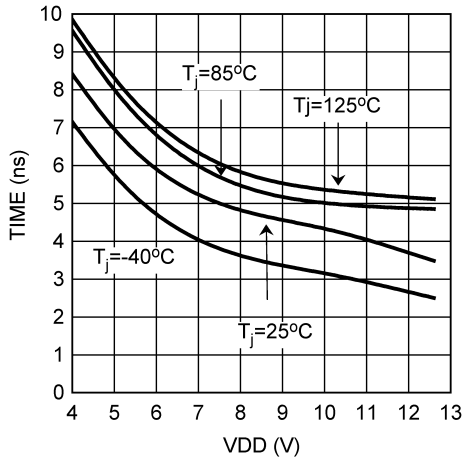


Figure 13. OUT Turnoff to PILOT Turnon Propagation Delay vs VDD

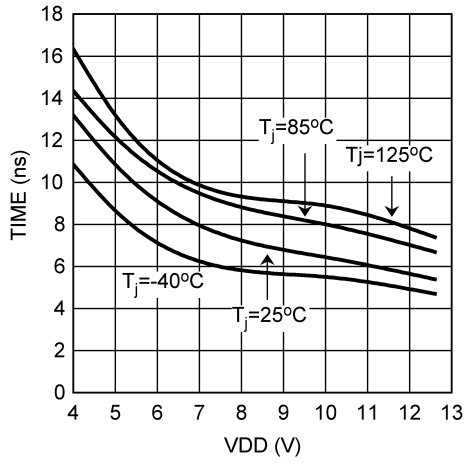


Figure 14. PILOT Turnoff to OUT Turnon Propagation Delay vs VDD

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Typical Characteristics (continued)

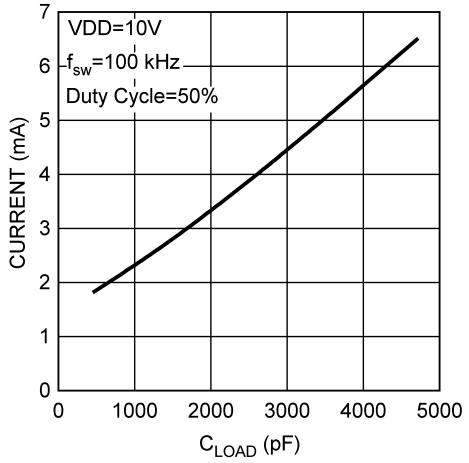


Figure 15. Supply Current vs OUT Capacitive Load

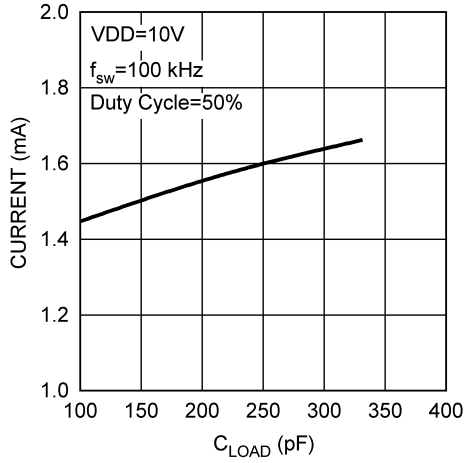


Figure 16. Supply Current vs PILOT Capacitive Load

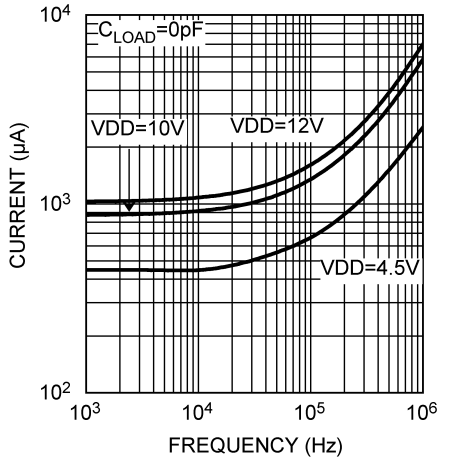


Figure 17. Supply Current vs Frequency

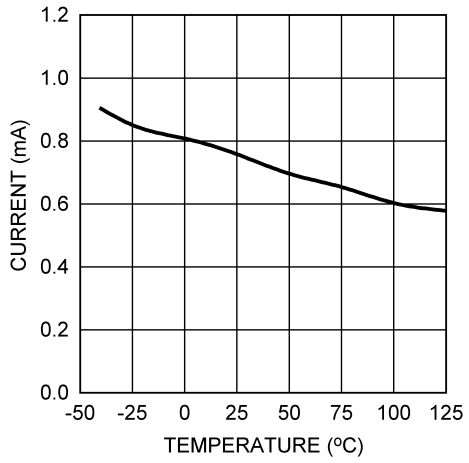


Figure 18. Quiescent Current vs Temperature

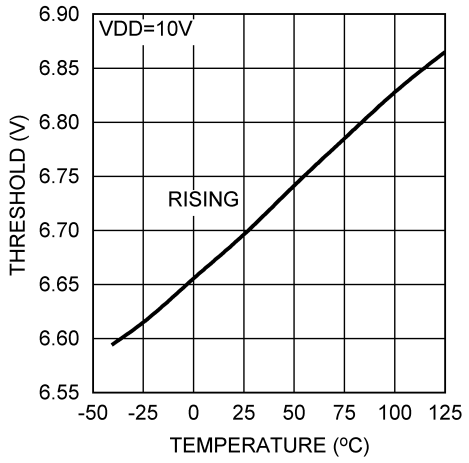


Figure 19. LM5134A Input Threshold vs Temperature

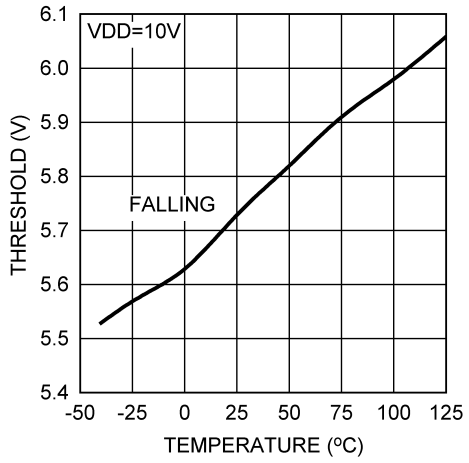


Figure 20. LM5134A Input Threshold vs Temperature

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Typical Characteristics (continued)

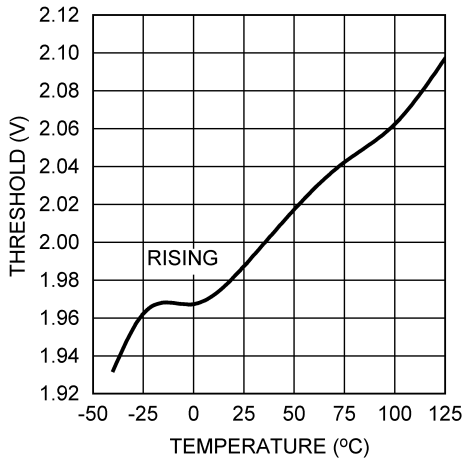


Figure 21. LM5134B Input Threshold vs Temperature

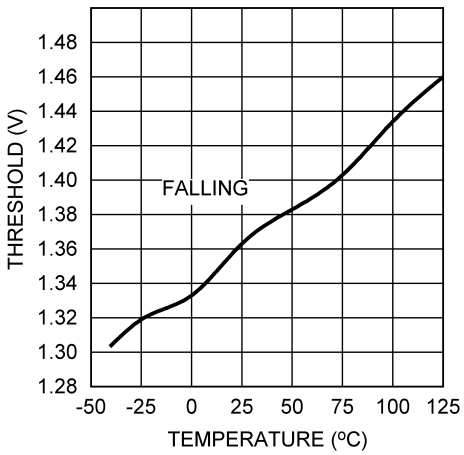


Figure 22. LM5134B Input Threshold vs Temperature

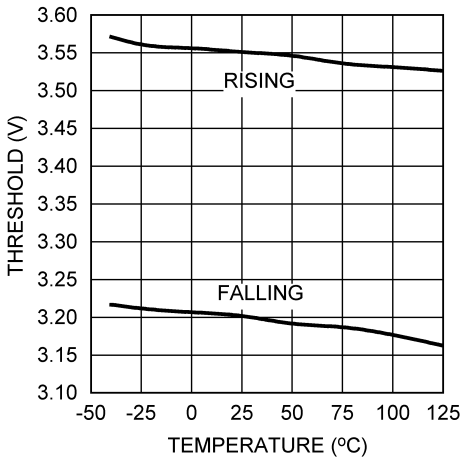


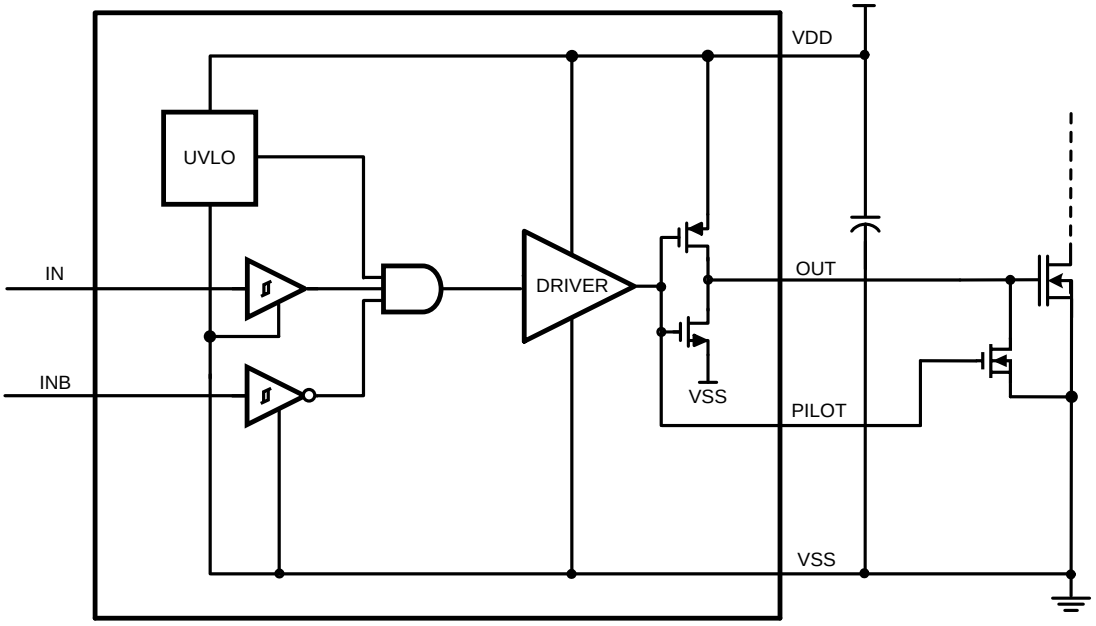
Figure 23. UVLO Threshold vs Temperature

7 Detailed Description

7.1 Overview

The LM5134 is a single low-side gate driver with one main output, OUT, and a complementary output PILOT. The OUT pin has high 7.6-A and 4.5-A peak sink and source current and can be used to drive large power MOSFETs or multiple MOSFETs in parallel. The PILOT pin has 820-mA and 660-mA peak sink and source current, and is intended to drive an external turnoff MOSFET, as shown in *Functional Block Diagram*. The external turnoff FET can be placed close to the power MOSFETs to minimize the loop inductance, and therefore helps eliminate stray inductance induced oscillations or undesired turnon. This feature also provides the flexibility to adjust turnon and turnoff speed independently.

7.2 Functional Block Diagram



7.3 Feature Description

When using the external turnoff switch, it is important to prevent the potential shoot-through between the external turnoff switch and the LM5134 internal pullup switch. The propagation delay, T_{PD-ON} and T_{PD-OFF}, has been implemented in the LM5134 between the PILOT and the OUT pins, as depicted in the timing diagram. The turnon delay T_{PD-ON} is designed to be shorter than the turnoff delay T_{PD-OFF} because the rising time of the external turnoff switch can attribute to the additional delay time. It is also desirable to minimize T_{PD-ON} to favor the fast turnoff of the power MOSFET.

The LM5134 offers both inverting and noninverting inputs to satisfy requirements for inverting and non-inverting gate drive signals in a single device type. Inputs of the LM5134 are TTL and CMOS Logic compatible and can withstand input voltages up to 14 V regardless of the VDD voltage. This allows inputs of the LM5134 to be connected directly to most PWM controllers.

The LM5134 includes an Undervoltage Lockout (UVLO) circuit. When the VDD voltage is below the UVLO threshold voltage, the IN and INB inputs are ignored, and if there is sufficient VDD voltage, the OUT is pulled low. In addition, the LM5134 has an internal PNP transistor in parallel with the output NMOS. Under the UVLO condition, the PNP transistor will be on and clamp the OUT voltage below 1 V. This feature ensures the OUT remains low even with insufficient VDD voltage.

7.4 Device Functional Modes

Table 1 lists the logic options for the device and Table 2 lists the device truth table.

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Table 1. Input/Output Options

BASE PART NUMBER	LOGIC INPUT
LM5134A	CMOS
LM5134B	TTL

Table 2. Truth Table

IN	INB	OUT	PILOT
L	L	L	H
L	H	L	H
H	L	H	L
H	H	L	H

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when there are times that the PWM controller cannot directly drive the gates of the switching devices. With advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Because traditional buffer-drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter-follower configurations, lack level-shifting capability, the circuits prove inadequate with digital power.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers can also perform other tasks, such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, and reducing power dissipation and thermal stress in controllers by moving gate-charge power losses into itself.

Finally, emerging wide-bandgap power-device technologies, such as GaN based switches capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays, and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction with a simplified system design.

8.2 Typical Application

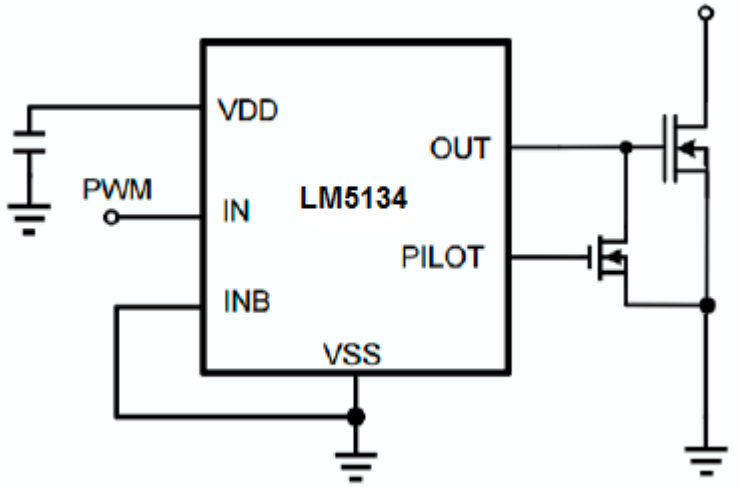


Figure 24. Application Schematic

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Typical Application (continued)

8.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must first be evaluated to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type.

Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
Input-to-output logic	Noninverting
Input threshold type	Logic level
V_{DD} bias supply voltage	10 V (minimum), 113 V (nominal), 15 V (peak)
Peak source and sink currents	Minimum 1.65-A source, minimum 1.65-A sink
Enable and disable function	Yes, required
Propagation delay	Maximum 40 ns or less

8.2.2 Detailed Design Procedure

8.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET when the input signal is in high state is preferred, then the noninverting configuration must be selected. If turning off the power MOSFET when the input signal is in high state is preferred, the inverting configuration must be chosen. The LM5134 device can be configured in either an inverting or noninverting input-to-output configuration, using the IN– or IN+ pins, respectively. To configure the device for use in inverting mode, tie the IN+ pin to VDD and apply the input signal to the IN– pin. For the noninverting configuration, tie the IN– pin to GND and apply the input signal to the IN+ pin.

8.2.2.2 Input Threshold Type

The type of controller used determines the input voltage threshold of the gate driver device. The LM5134B device features a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers, as well as higher-voltage input signals from analog controllers.

The LM5134A device features higher voltage thresholds for greater noise immunity, and controllers with higher drive voltages.

See *Electrical Characteristics* for the actual input threshold voltage levels and hysteresis specifications for the LM5134 device.

8.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage applied to the VDD pin of the device should never exceed the values listed in *Recommended Operating Conditions*. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With an operating range from 4 V to 12 V, the LM5134 device can be used to drive a variety of power switches, such as Si MOSFETs (for example,
VGS = 4.5 V, 10 V, 12 V), BJTs, and wide-band gap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

8.2.2.4 Peak Source and Sink Currents

Generally, to minimize switching power losses, the switching speed of the power switch during turnon and turnoff should be as fast as possible. However, very fast transitions on the Drain node voltage can lead to unwanted emissions for EMI, and the turnon speed is often deliberately slowed down by placing a series resistor between the Drive output and MOSFET gate to reduce these emissions.

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The speed at which the drain node rises during turnoff is typically dictated by the current in the inductor at turnoff, and thus is not dependent on the turnoff current of the drive circuit. However, depending on the amount of current flowing through the drain to gate capacitance of the MOSFET as the drain voltage rises and the impedance to ground of the drive circuit, it is possible for the gate voltage to exceed the threshold voltage of the FET and turn the FET back on, known as a false turnon.

For these reasons, turn the FET off as fast as possible. The LM5134 allows the flexibility of different turnon and turnoff speeds, and avoids false turnon by providing a pilot output to drive a small pulldown MosFET, which can be placed close to the main FET and reduces the impedance from gate to ground on turnoff.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a dV/dt of 20 V/ns or higher, under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC converter application. This type of application is an inductive hard-switching application, and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to V DS(on) in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to the power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, VGS(TH). To achieve the targeted dV/dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The LM5134 gate driver is capable of providing 4.5-A peak sourcing current, which exceeds the design requirement and has the capability to meet the switching speed needed. The 2.7x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET, along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations.

However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I PEAK × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt, then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I PEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

The LM5134 is capable of driving a small FET local to the Gate of the main MOSFET to reduce the impact of this parasitic inductance and achieve the high dV/dt required on turnoff. The nominal gate voltage plateau of the SPP20N60C3 is given as 5.5 V. Thus to achieve the required sink current of 1.65 A would require an Rds_on of 3.3 Ω for the pilot FET. Lower on resistance gives further margin in the turnoff speed as described above, and reduces the potential for false turnon.

8.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver, without involving the input signal. A pin offering an enable and disable function achieves this requirement. The LM5134 device offers two input pins, IN+ and IN – , both of which control the state of the output as listed in Table 2. Based on whether an inverting or noninverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other unused input pin can be used for the enable and disable functionality. If the design does not require an enable function, the unused input pin can be tied to either the VDD pin (in case IN+ is the unused pin), or GND (in case IN – is unused pin) to ensure it does not affect the output status.

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8.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used, and the acceptable level of pulse distortion to the system. The LM5134 device features industry best-in-class 17-ns (typical) propagation delays, which ensure very little pulse distortion and allow operation at very high frequencies. See *Electrical Characteristics* for the propagation and switching characteristics of the LM5134 device.

8.2.2.7 PILOT MOSFET Selection

In general, a small-sized 20-V MOSFET with logic level gates can be used as the external turnoff switch. To achieve a fast switching speed and avoid the potential shoot-through, select a MOSFET with the total gate charge less than 3 nC. Verify that no shoot-through occurs for the entire operating temperature range. In addition, a small Rds(on) is preferred to obtain the strong sink current capability. The power losses of the PILOT MOSFET can be estimated in Equation 1.

$$P_g = 1/2 \times Q_{go} \times VDD \times F_{SW} \quad (1)$$

where

- Q_{go} is the total input gate charge of the power MOSFET

8.2.3 Application Curves

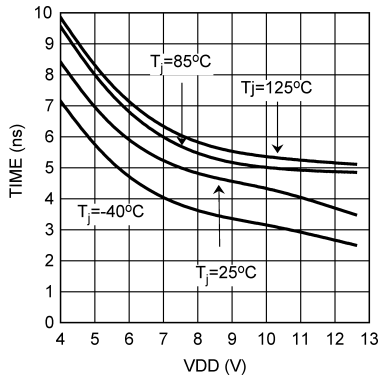


Figure 25. OUT Turnoff to PILOT Turnon Propagation Delay vs VDD

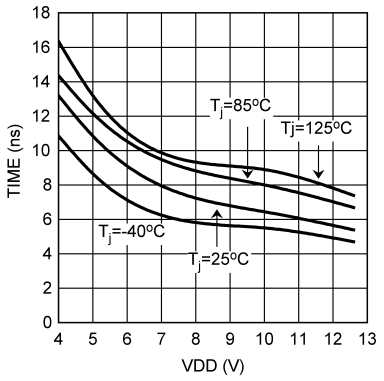


Figure 26. PILOT Turnoff to OUT Turnon Propagation Delay vs VDD

9 Power Supply Recommendations

A low ESR/ESL ceramic capacitor must be connected close to the IC, between VDD and VSS pins to support the high peak current being drawn from VDD during turnon of the FETs. Place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

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10 Layout

10.1 Layout Guidelines

Attention must be given to board layout when using LM5134. Some important considerations include:

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate.
2. To reduce the loop inductance, the driver should be placed as close as possible to the FETs. The gate trace to and from the FETs are recommended to be placed closely side by side, or directly on top of one another.
3. The parasitic source inductance, along with the gate capacitor and the driver pulldown path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.

10.2 Layout Example

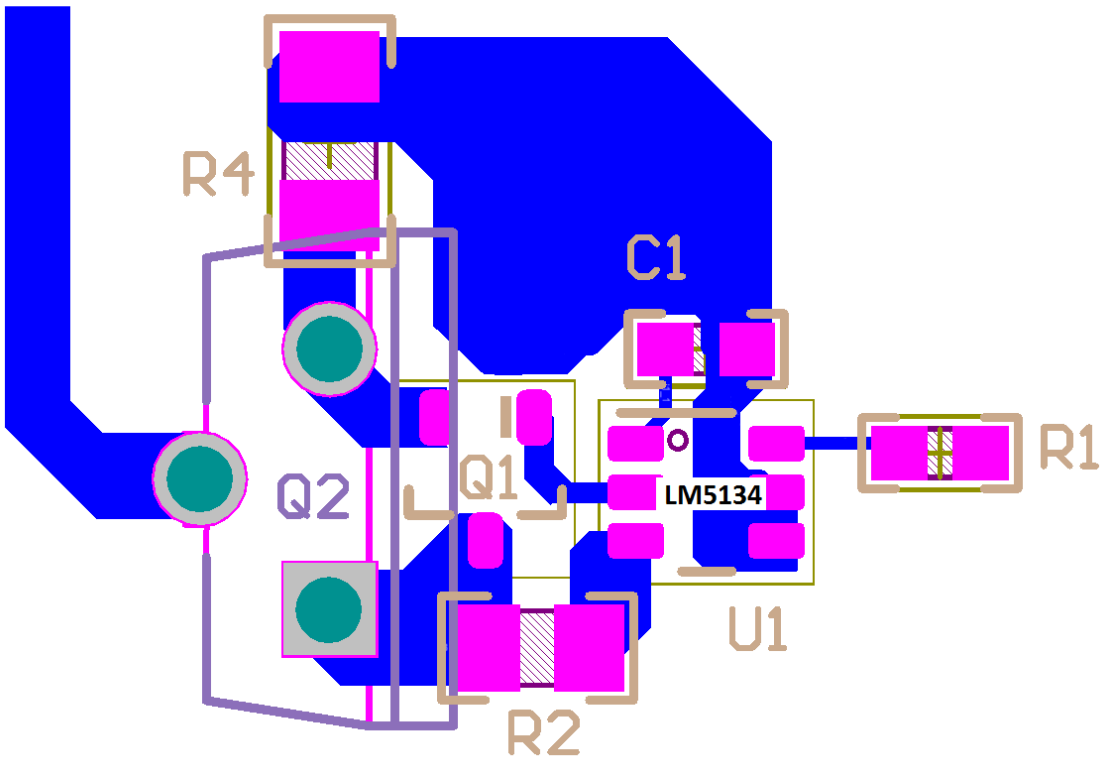


Figure 27. LM5134 Layout Example

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10.3 Power Dissipation

It is important to keep the power consumption of the driver below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the LM5134 is the sum of the gate charge losses and the losses in the driver due to the internal CMOS stages used to buffer the output as well as the power losses associated with the quiescent current.

The gate charge losses include the power MOSFET gate charge losses as well as the PILOT FET gate charge losses and can be calculated as follows:

$$P_g = (Q_{go} + Q_{gp}) \times VDD \times F_{SW} \quad (2)$$

Or

$$P_g = (C_o + C_p) \times VDD^2 \times F_{SW}$$

where

- F_{sw} is switching frequency
- Q_{go} is the total input gate charge of the power MOSFET
- Q_{gp} is the total input gate charge of the PILOT MOSFET (3)

C_o and C_p are the load capacitance at OUT and PILOT outputs respectively. It should be noted that due to the use of an external turnoff switch, part of the gate charge losses are dissipated in the external turnoff switch. Therefore, the actual gate charge losses dissipated in the LM5134 is less than predicted by the above expressions. However, they are a good conservative design estimate.

The power dissipation associated with the internal circuit operation of the driver can be estimated with the characterization curves of the LM5134. For a given ambient temperature, the maximum allowable power losses of the IC can be defined using Equation 4.

$$P = (T_J - T_A) / \theta_{JA}$$

where

- P is the total power dissipation of the driver (4)

11 器件和文档支持

11.1 社区资源

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11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5134AMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SK7A	Samples
LM5134AMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SK7A	Samples
LM5134ASD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5134A	Samples
LM5134ASDX/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5134A	Samples
LM5134BMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SK7B	Samples
LM5134BMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	SK7B	Samples
LM5134BSD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5134B	Samples
LM5134BSDX/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5134B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

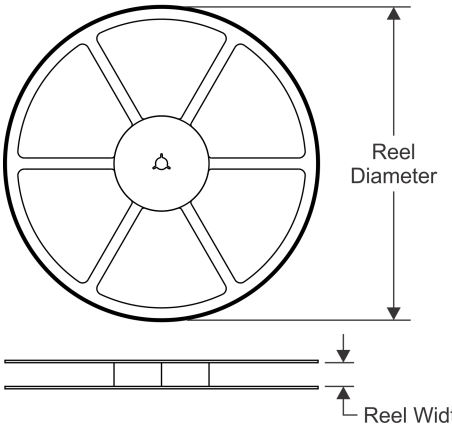
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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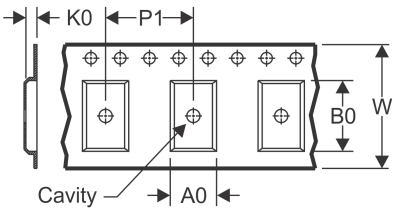
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

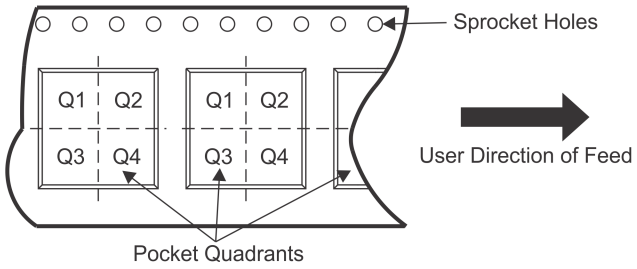


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

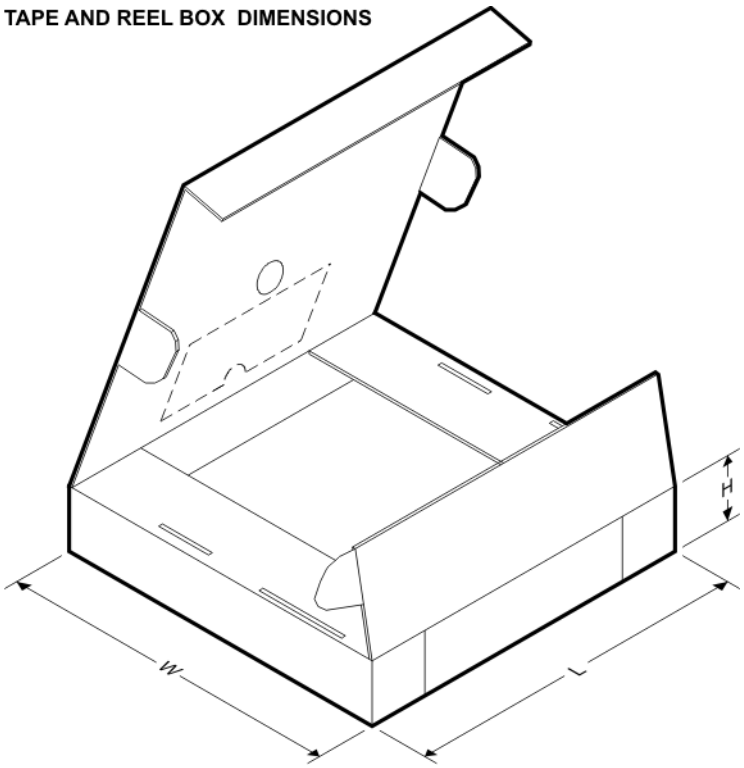
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5134AMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134AMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134ASD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5134ASDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5134BMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134BMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5134BSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM5134BSDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

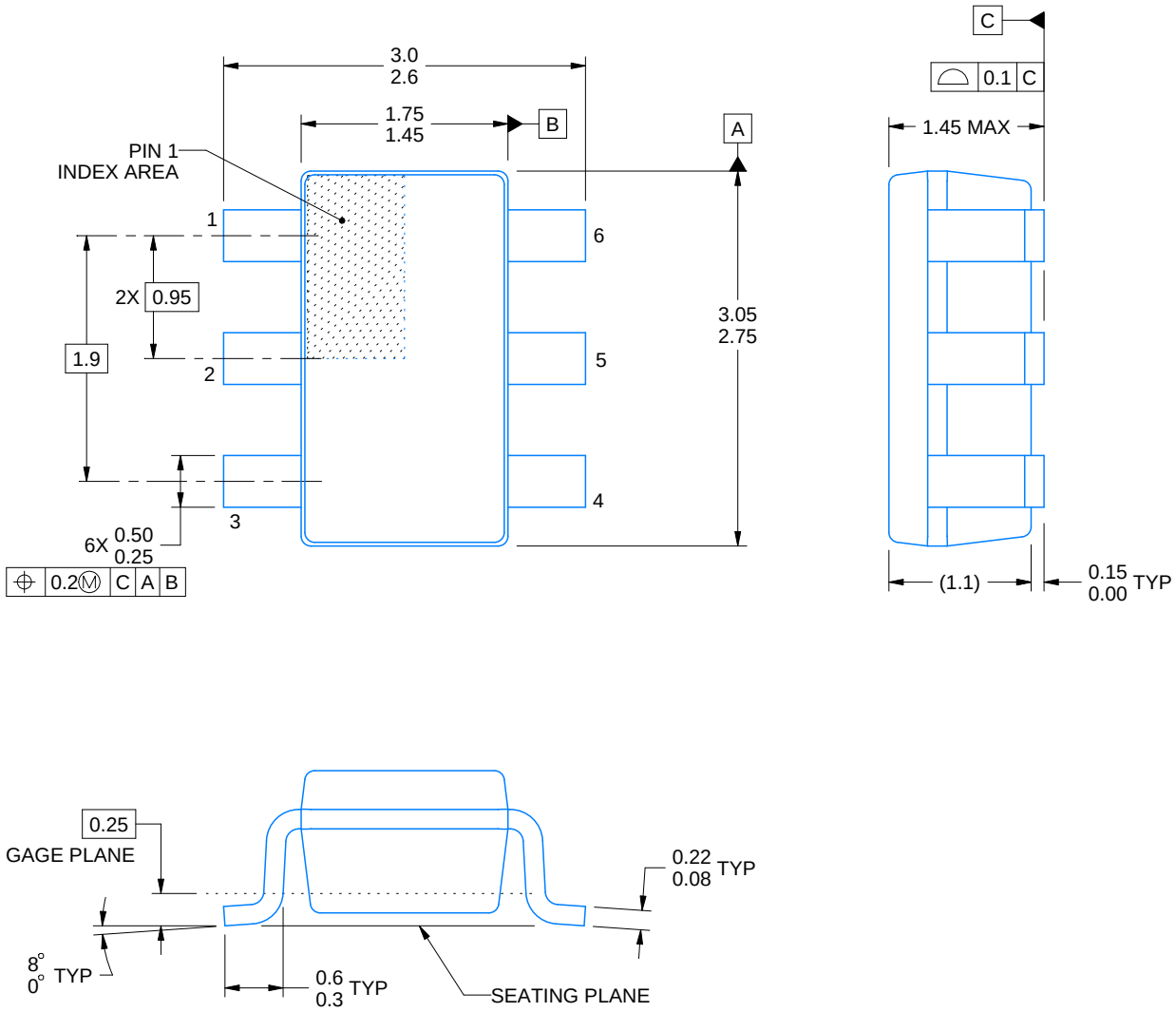
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5134AMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5134AMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5134ASD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM5134ASDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LM5134BMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LM5134BMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LM5134BSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LM5134BSDX/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

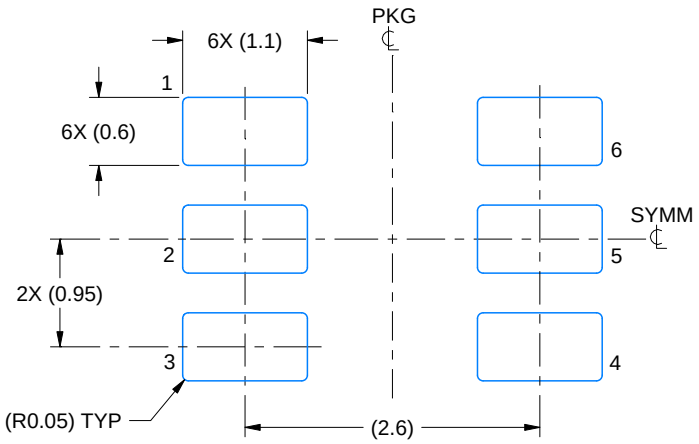
SMALL OUTLINE TRANSISTOR



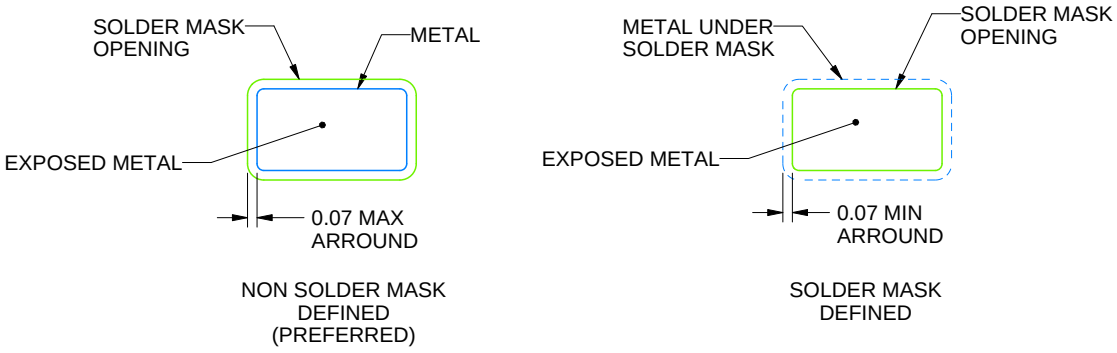
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

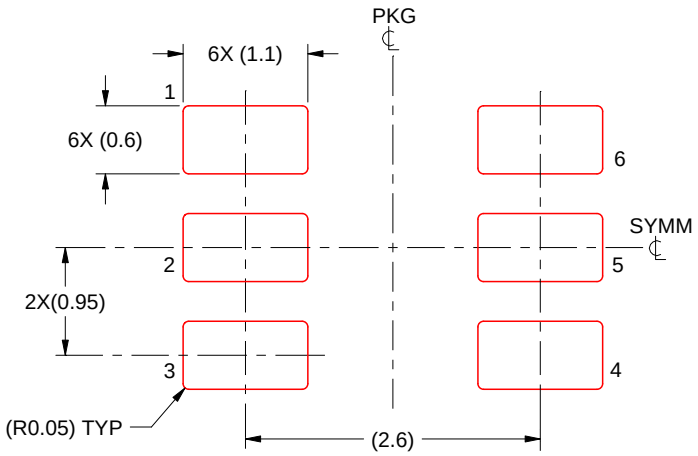


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



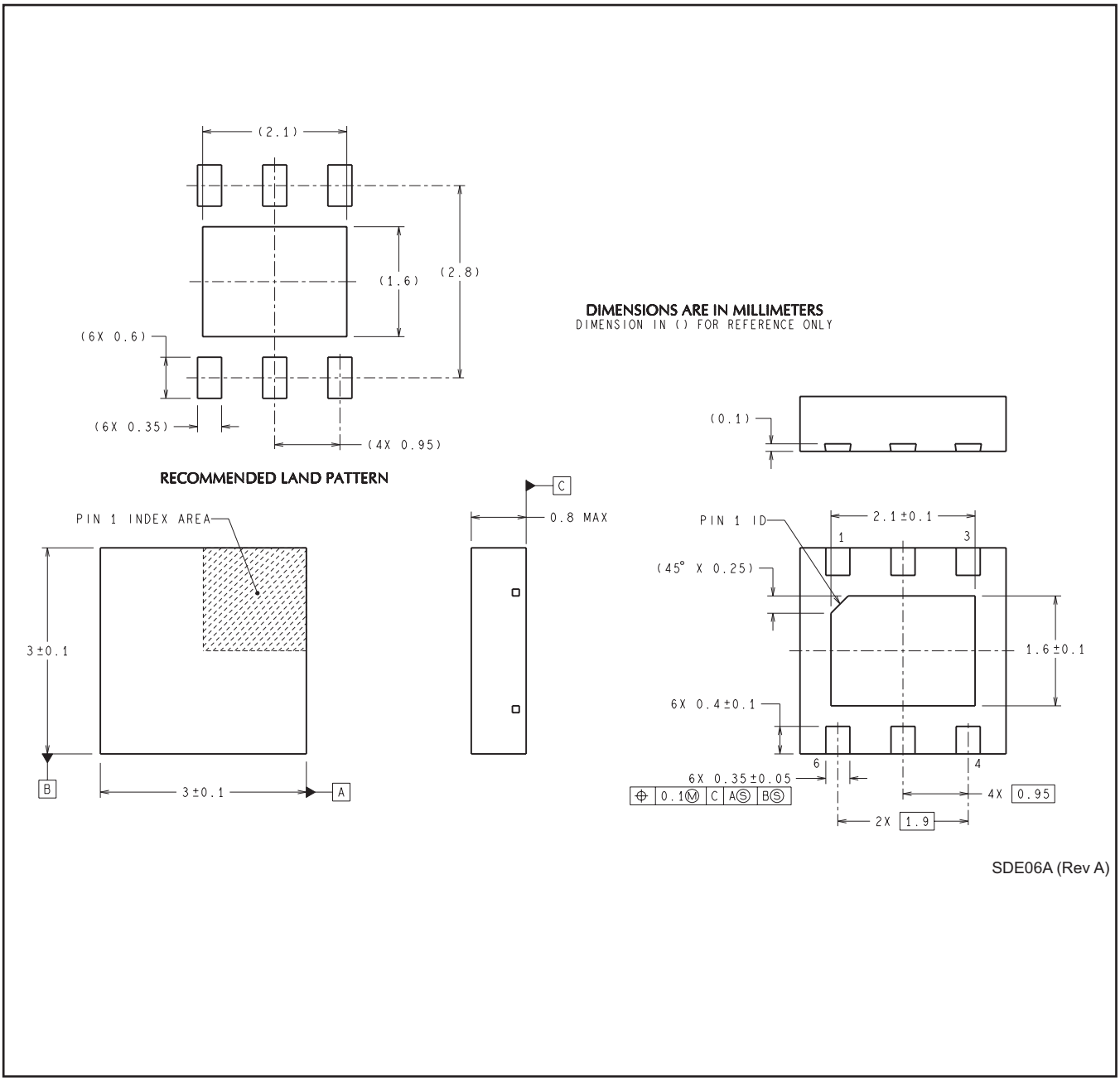
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NGG0006A



SDE06A (Rev A)

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