2.5A 和 5A，35V最大值VDD 场效应晶体管 (FET) 和绝缘栅双极晶体管 (IGBT) 单栅极驱动器

查询样品: UCC27532

特性

- 低成本栅极驱动器（为驱动 **FET** 和 **IGBT** 的最佳解决方案）
- 离散晶体管对驱动的出色替代产品（提供与控制器的简便对接）
- **CMOS** 兼容输入逻辑阀值（在 **VDD** 大于 **18V** 是变为固定值）
- 分离输出可实现独立接通和关闭调整
- 由固定 **TTL** 兼容阀值启用
- **18V VDD** 时的高 **2.5A** 源电流和 **5A** 灌峰值驱动电流
- 从 **10V** 到高达 **35V** 的宽 **VDD** 范围
- 能够耐受比接地最多低 **5V** 的直流 **(DC)** 电压的输入引脚
- 当输入悬空或 **VDD** 欠压闭锁 **(UVLO)** 期间，输出保持低电平
- 快速传播延迟（典型值 **17ns**）
- 快速上升和下降时间（**1800pF** 负载时的典型值分别为 **15ns** 和 **7ns**）
- 欠压闭锁 **(UVLO)**
- 被用作高侧或低侧驱动器（如果采用适当的偏置和信号隔离设计）
- 低成本、节省空间的 **6** 引脚 **DBV**（小外形尺寸晶体管 **(SOT)-23**）封装
- 运行温度范围 **-40°C** 至 **140°C**

应用范围

- 开关模式电源
- 直流 **(DC)** 到 **DC** 转换器
- 太阳能逆变器、电机控制、不间断电源 **(UPS)**
- 混合动力车 **(HEV)** 和电动车辆 **(EV)** 充电器
- 家用电器
- 可再生能源功率转换
- **SiC FET** 转换器

说明

UCC27532 是一款单通道、高速、栅极驱动器，此驱动器可借助于高达 2.5A 源电流和 5A 灌电流（非对称驱动）来有效驱动 MOSFET 和 IGBT 电源开关。 强劲的非对称驱动中的吸收能力提升了抗寄生米勒 (Miller) 接通效应的能力。 UCC27532 器件还特有一个分离输出配置，在此配置中栅极驱动电流从 OUTH 引脚拉出并从 OUTL 引脚被灌入。 这个独特的引脚安排使得用户能够分别在 OUTH 和 OUTL 引脚上采样独立的接通和关闭电阻器并且能很轻易地控制开关的转换率。

此驱动器具有轨到轨驱动能力和典型值为 17ns 的极小传播延迟。

UCC27532DBV 具有 CMOS 输入阀值，此阀值在 VDD 低于或等于 18V 时介于比 VDD 高 55% 的电压值与比 VDD 低 45% 的电压值范围内。当 VDD 高于 18V 时，输入阀值保持在其最大水平上。

此驱动器具有支持固定 TTL 兼容阀值的 EN 引脚。 EN 被内部上拉；将 EN 下拉为低电平禁用驱动器，而将其保持打开可提供正常运行。 EN 引脚可被用作一个额外输入，其性能与 IN 引脚一样。

将驱动器的输入引脚保持开状态将把输出保持为低电平。 驱动器的逻辑运行方式被显示在应用图、时序图和输入与输出逻辑真值表中。

VDD 引脚上的内部电路提供一个欠压闭锁功能，此功能在 VDD 电源电压处于运行范围内之前将输出保持为低电平。

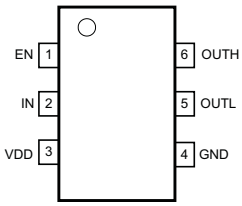
UCC27532 驱动器采用 6 引脚标准 SOT-23 (DBV) 封装。 此器件具有 -40°C 至 140°C 的宽运行温度范围。

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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UCC27532DBV（顶视图）



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PART NUMBER	PACKAGE(2)	PEAK CURRENT (SOURCE AND SINK)	INPUT THRESHOLD LOGIC	OPERATING TEMPERATURE RANGE T_A
UCC27532DBV	SOT-23, 6-PIN	2.5 A and 5 A	CMOS-(dependent on VDD bias voltage)	-40°C to +140°C

(1) DBV package uses Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) For the most up-to-date packaging information see the TI web site.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range,	VDD	-0.3	35	V
Continuous	OUTH, OUTL	-0.3	VDD +0.3	
Pulse	OUTH, OUTL (200 ns)	-2	VDD +0.3	
Continuous IN, EN		-5	27	V
Pulse IN, EN (1.5 µs)		-6.5	27	
Human body model, HBM (ESD)(5)			4000	
Charged device model, CDM (ESD)			1000	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

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THERMAL INFORMATION

THERMAL METRIC(1)		UCC27532 DBV 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	178.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	109.7	
θ_{JB}	Junction-to-board thermal resistance(4)	28.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	27.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Operating junction temperature range	-40		140	°C
Input voltage, IN	-5		25	V
Enable, EN	-5		25	

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ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = -40°C to 140°C, IN switching from 0 V to VDD, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together. Typical condition specifications are at 25°C.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Bias Currents						
I_{DDoff}	Startup Current, VDD = 7.0	IN, EN = VDD	100	240	350	µA
		IN, EN = GND	100	250	350	
Under Voltage Lockout (UVLO)						
V_{ON}	Supply start threshold		8.0	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	
V_{DD_H}	Supply voltage hysteresis			0.7		
Input (IN)						
V_{IN_H}	Input signal high threshold	Output high	8.8	9.4	10	V
V_{IN_L}	Input signal low threshold	Output low	6.7	7.3	7.9	
V_{IN_HYS}	Input signal hysteresis			2.1		
Enable (EN)						
V_{EN_H}	Enable signal high threshold	Output high	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output low	0.8	1.0	1.2	
V_{EN_HYS}	Enable signal hysteresis			0.9		
Outputs (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)(13) (1)	C_{LOAD} = 0.22 µF, f = 1 kHz		-2.5/+5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = -10 mA	VDD -0.2	VDD - 0.12	VDD - 0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	
R_{OH}	OUTH, pull-up resistance (15) (2)	T_A = 25°C, I_{OUT} = -10 mA	11	12	12.5	Ω
		T_A = -40°C to 140°C, I_{OUT} = -10 mA	7	12	20	
R_{OL}	OUTL, pull-down resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	
		T_A = -40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	
Switching Time (1)(3)						
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		
t_{D1}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, IN = 0 V to VDD		17	26	
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, IN = VDD to 0 V		17	26	

(1) Ensured by design and tested during characterization. Not production tested.
(2) Output pull-up resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure. The effective dynamic pull-up resistance is 3 x R_{OL}.
(3) See Figure 1.

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Timing Diagram

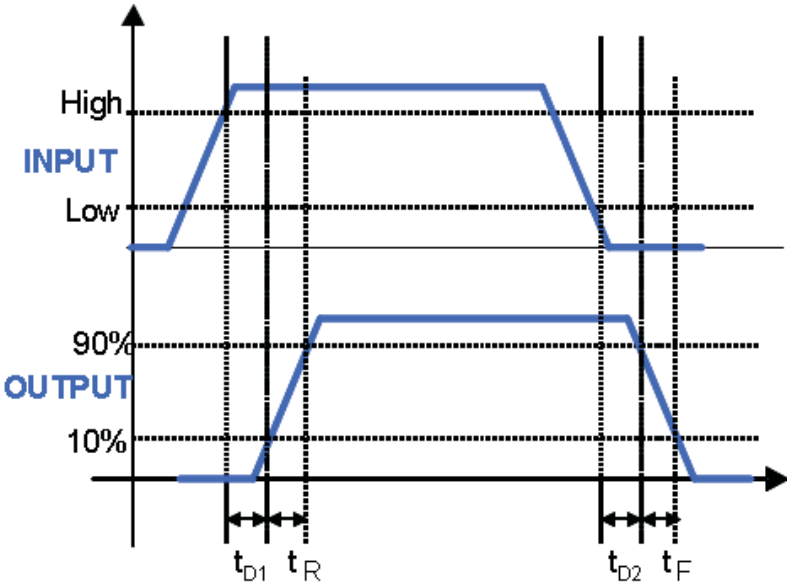
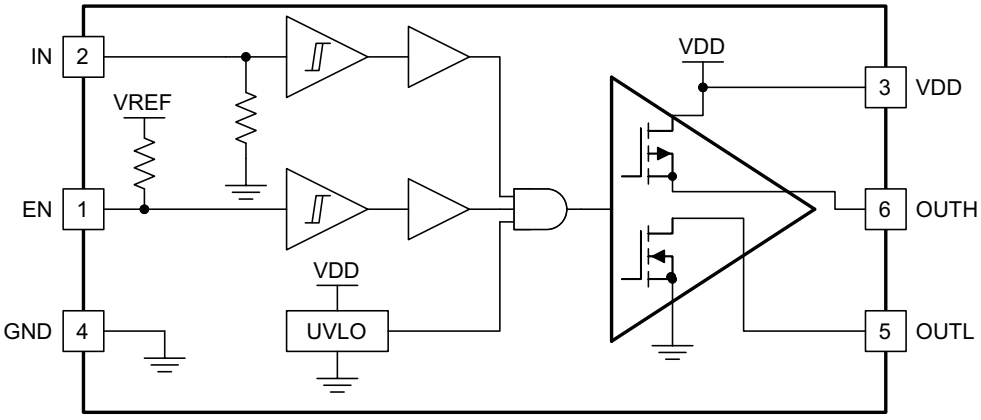


Figure 1. (OUTH tied to OUTL)(Input = IN, Output = OUT (EN = VDD), or Input = EN, Output = OUT (IN = VDD)

DEVICE INFORMATION

Block Diagram

(EN Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, In Pull-Down Resistance to GND = 230 kΩ)



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DEVICE INFORMATION

Typical Application Diagrams

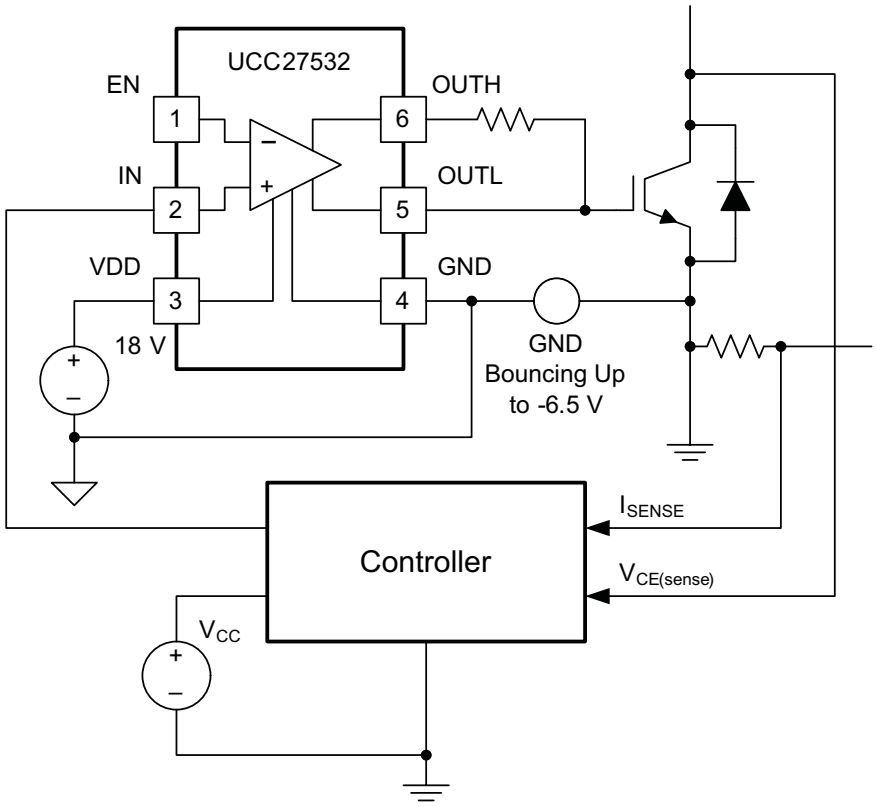


Figure 2. Driving IGBT Without Negative Bias

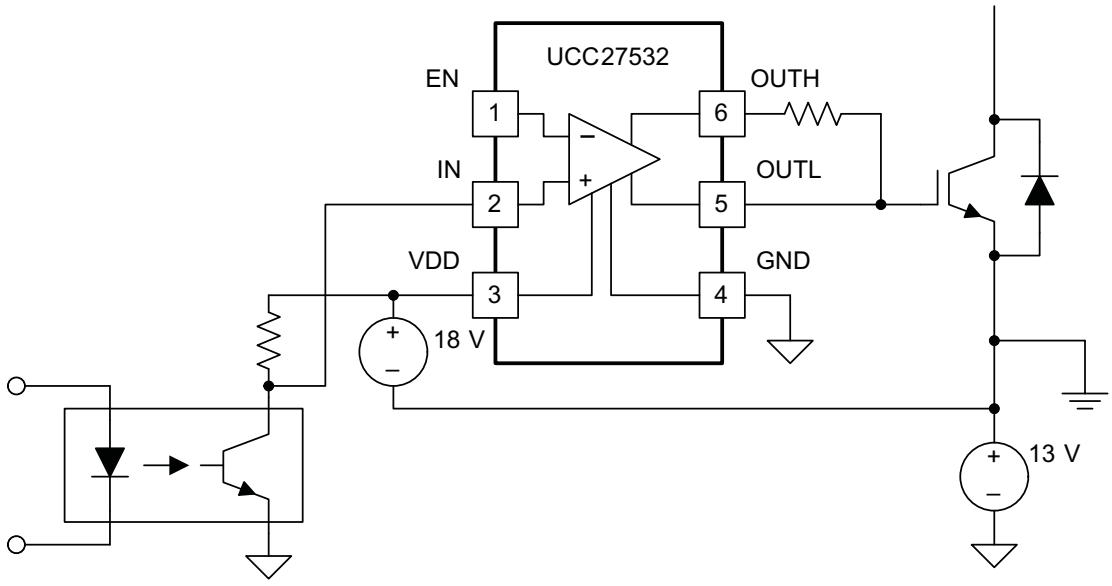


Figure 3. Driving IGBT With 13-V Negative Turn-Off Bias

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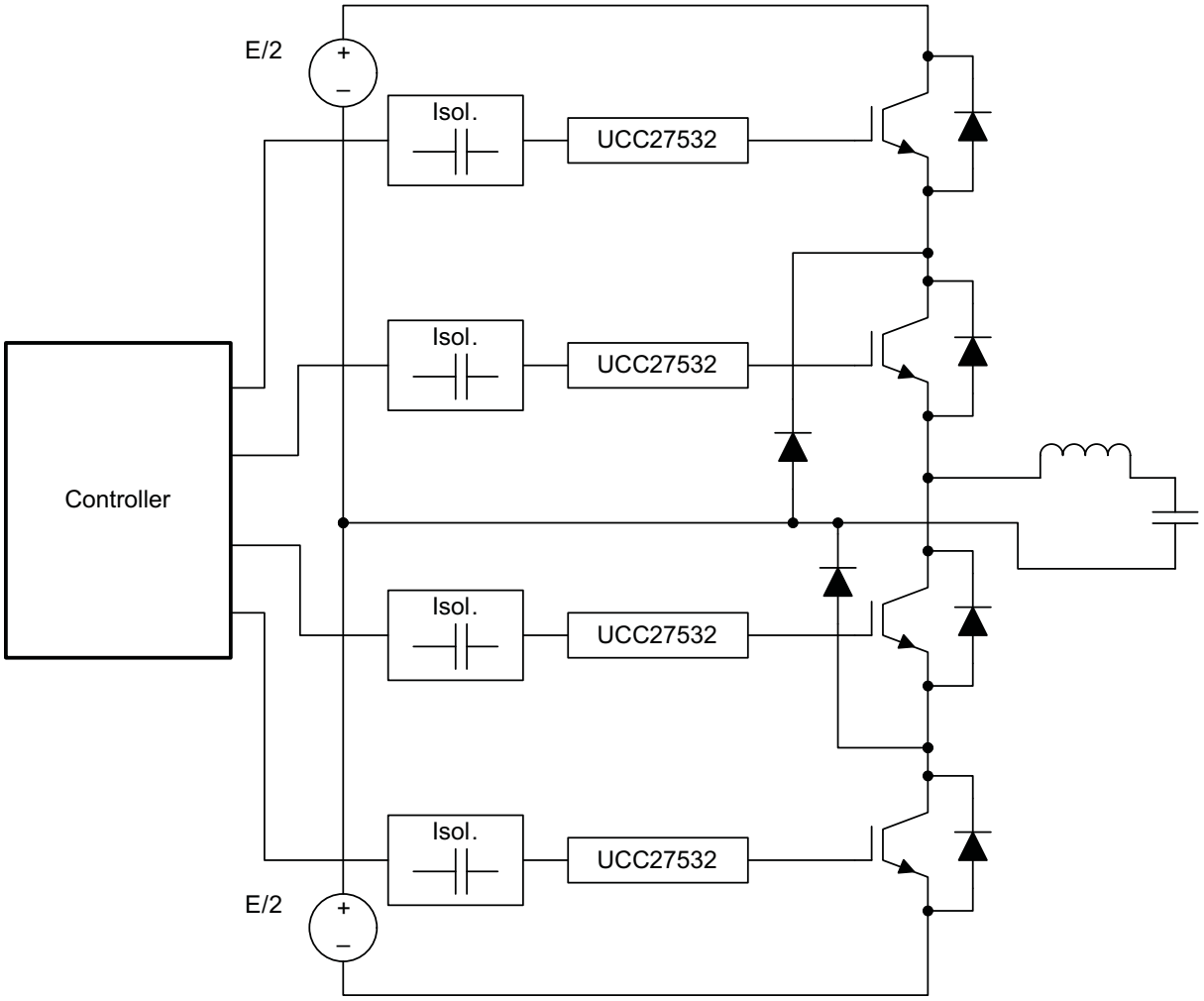
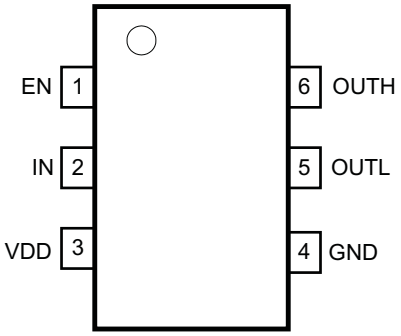


Figure 4. Using UCC27532 Drivers in an Inverter

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DEVICE INFORMATION

SOT-23, 6-Pin (DBV) Package (top view)



TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
1	EN	I	Enable (Pull EN to GND in order to disable output, pull it high or leave open to enable output).
2	IN	I	Driver non-inverting input (CMOS threshold for UCC27532DBV).
3	VDD	I	Bias supply input.
4	GND	-	Ground (all signals are referenced to this node).
5	OUTL	O	5-A sink current output of driver.
6	OUTH	O	2.5-A source current output of driver.

INPUT/OUTPUT LOGIC TRUTH TABLE

IN PIN	EN PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H

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TYPICAL CHARACTERISTICS

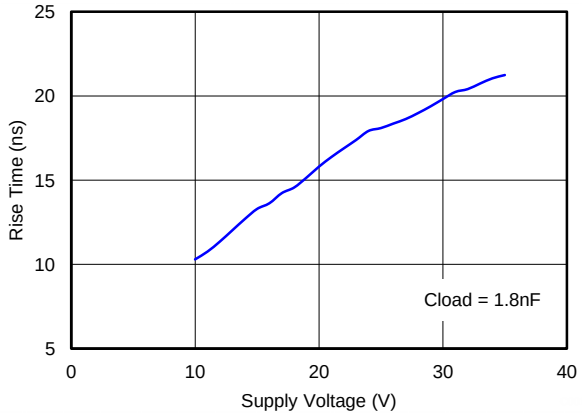


Figure 5. Rise Time vs. Supply Voltage

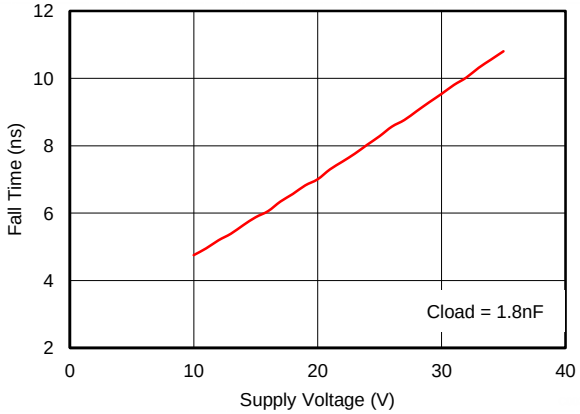


Figure 6. Fall Time vs. Supply Voltage

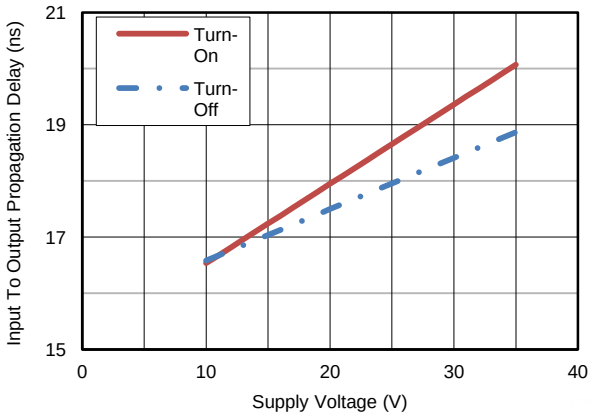


Figure 7. Propagation Delay vs. Supply Voltage

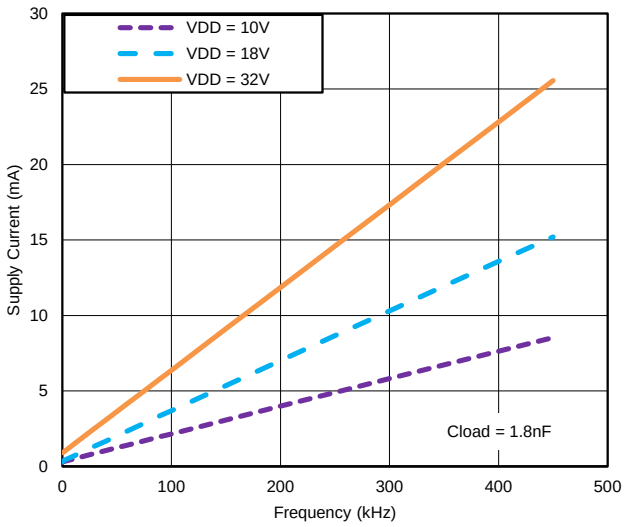


Figure 8. Operating Supply Current vs. Frequency

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TYPICAL CHARACTERISTICS (continued)

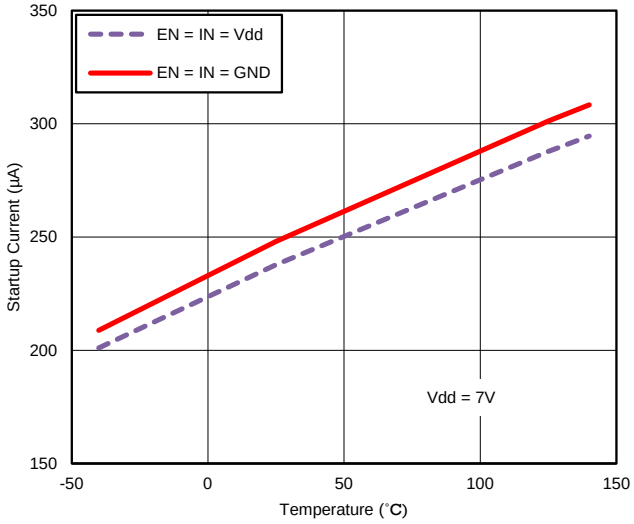


Figure 9. Start-Up Current vs. Temperature

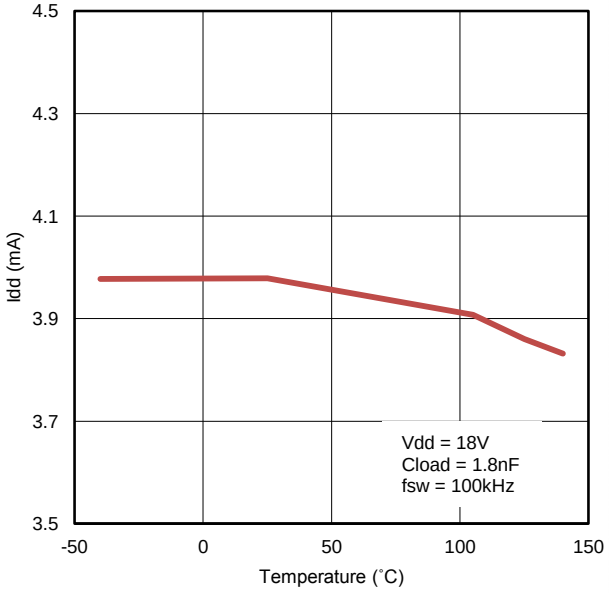


Figure 10. Operating Supply Current vs. Temperature (output switching)

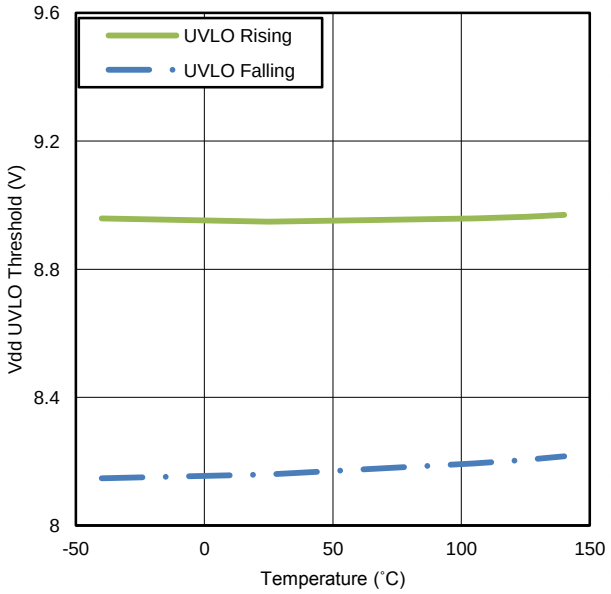


Figure 11. UVLO Threshold Voltage vs. Temperature

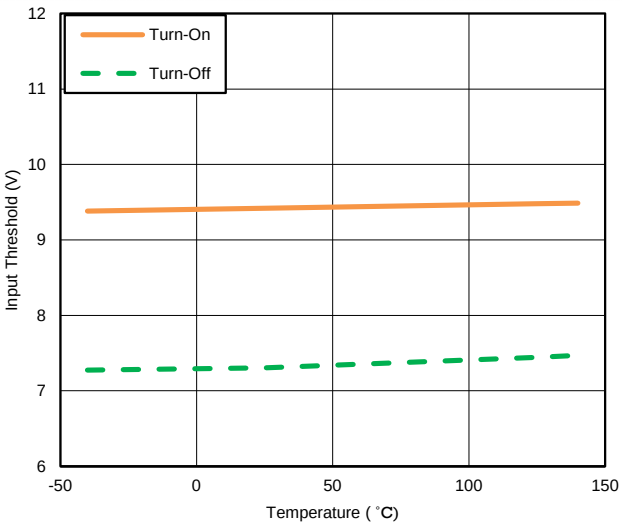


Figure 12. Input Threshold vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

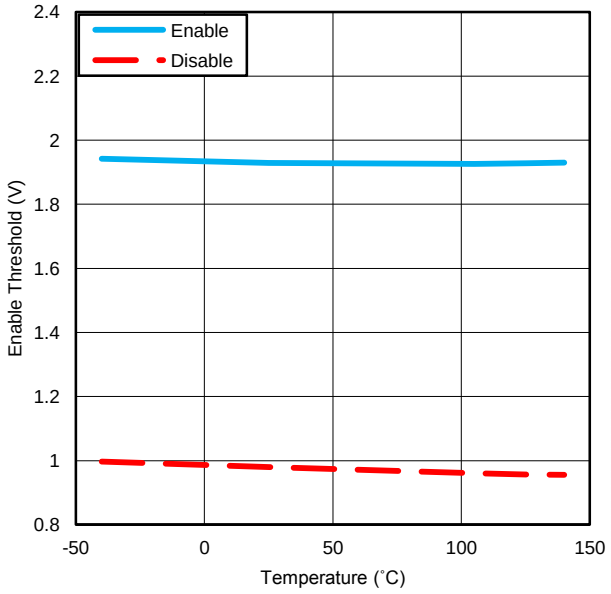


Figure 13. Enable Threshold vs. Temperature

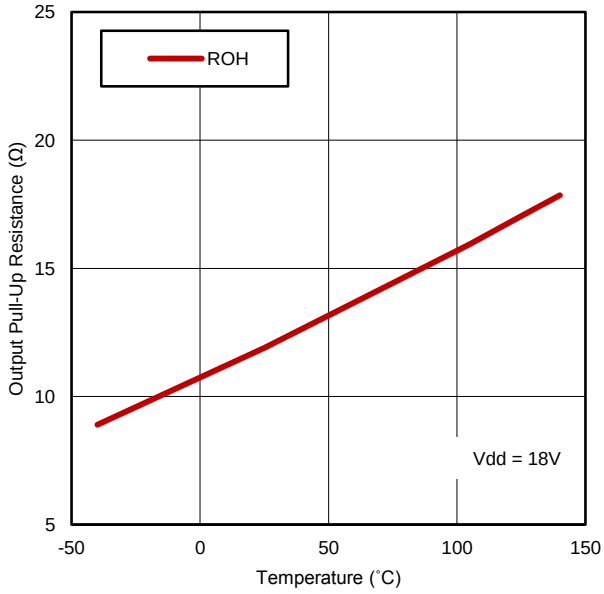


Figure 14. Output Pull-Up Resistance vs. Temperature

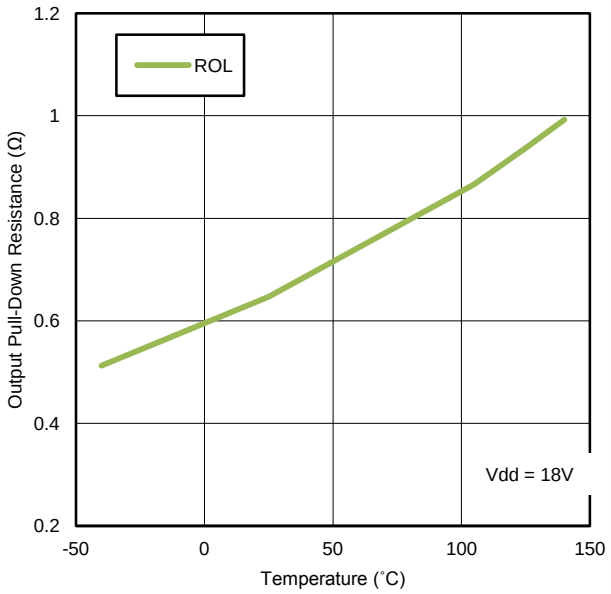


Figure 15. Output Pull-Down Resistance vs. Temperature

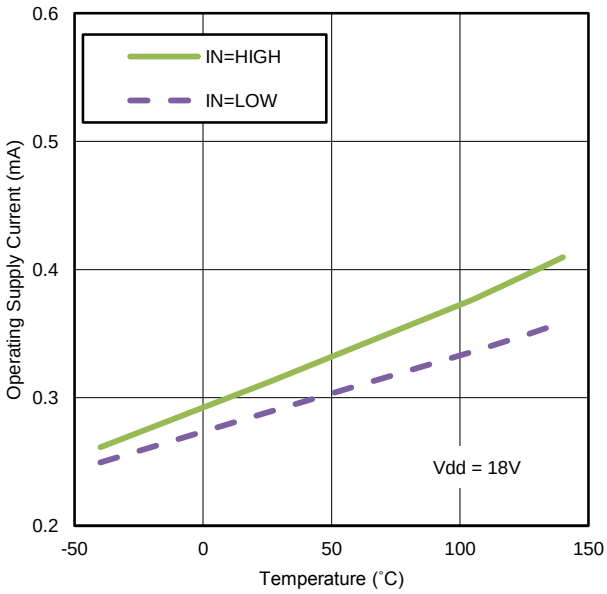


Figure 16. Operating Supply Current vs. Temperature (output in DC on/off condition)

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TYPICAL CHARACTERISTICS (continued)

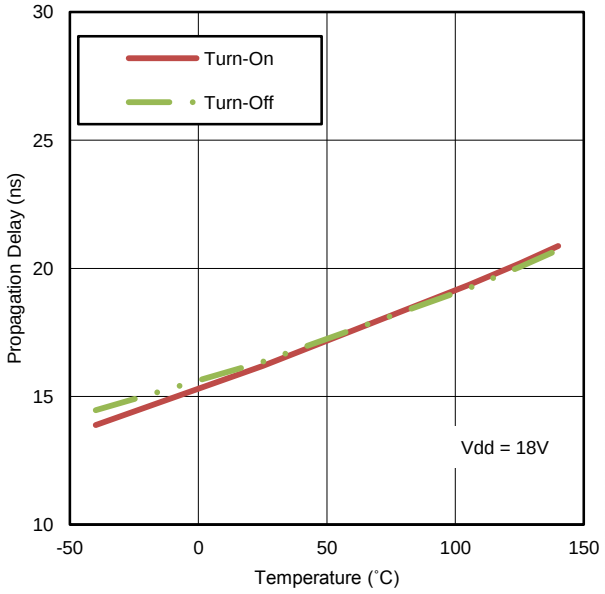


Figure 17. Input-to-Output Propagation Delay vs. Temperature

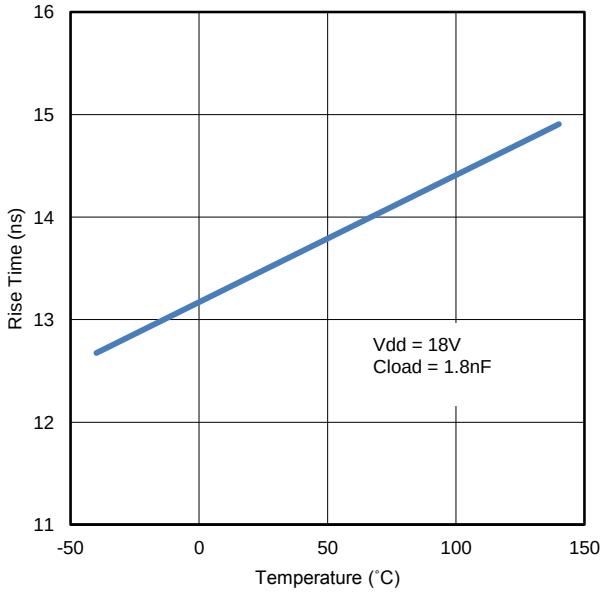


Figure 18. Rise Time vs. Temperature

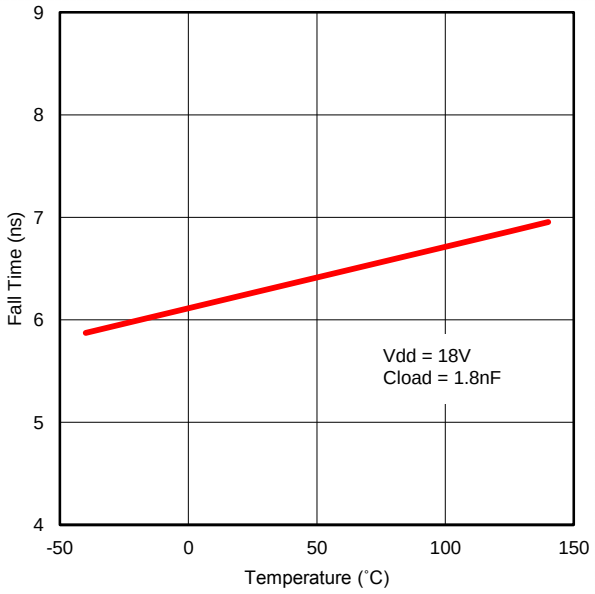


Figure 19. Fall Time vs. Temperature

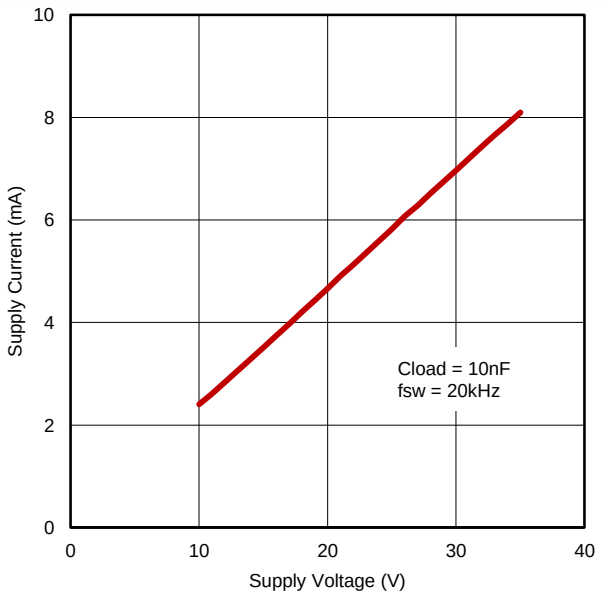


Figure 20. Operating Supply Current vs. Supply Voltage (output switching)

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TYPICAL CHARACTERISTICS (continued)

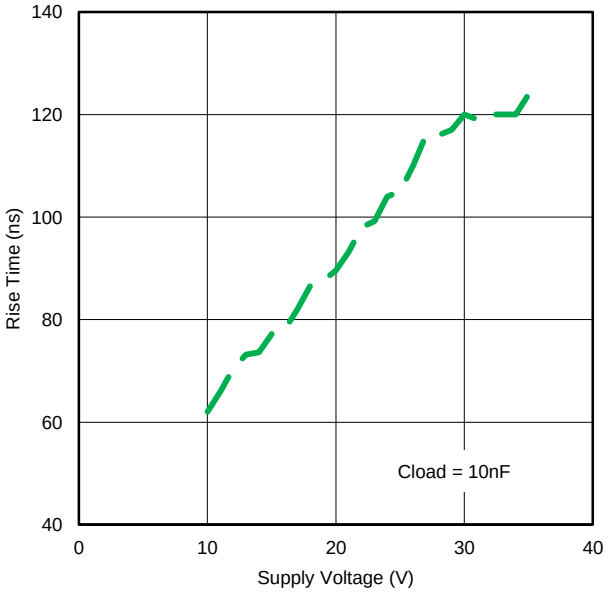


Figure 21. Rise Time vs. Supply Voltage

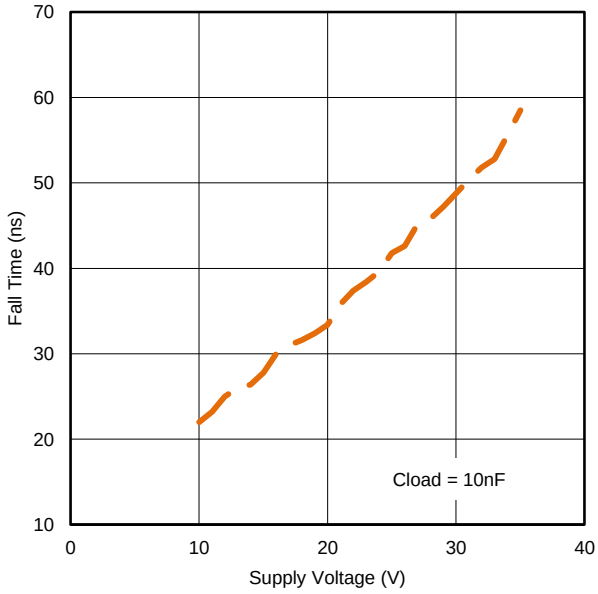


Figure 22. Fall Time vs. Supply Voltage

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APPLICATION INFORMATION

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered since the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or p- n-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this since they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27532 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 35 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -15-V(relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC27532 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC27532. Alternatively, in a high-side drive configuration the UCC27532 can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC27532 need to drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC27532 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

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Table 1. UCC27532 Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC27532 device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative(relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
	High UVLO of 8.9V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.
Outputs held low when input pin (IN) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure (OUTH, OUTL).	Allows independent optimization of turn-on and turn-off speeds using series gate resistors.
Strong sink current (5 A) and low pull-down impedance (0.65 Ω).	High immunity to high dV/dt Miller turn-on events.
CMOS compatible input threshold logic with wide 2.1-V hysteresis.	Excellent noise immunity.
Input capable of withstanding -6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

VDD Under Voltage Lockout

The UCC27532 device has internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when VDD voltage less than V_{ON} during power-up and when VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with 700-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

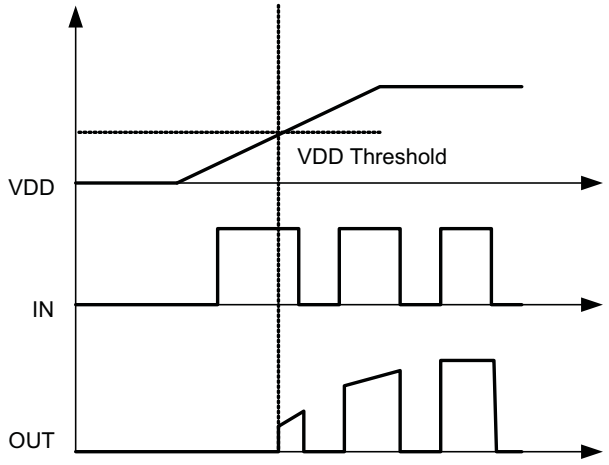


Figure 23. Power Up

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Input Stage

The input pin of UCC27532 device is based on a standard CMOS compatible input threshold logic that is dependent on the VDD supply voltage. The input threshold is approximately 55% of VDD for rise and 45% of VDD for fall. With 18-V VDD, typical high threshold = 9.4 V and typical low threshold = 7.3 V. The 2.1-V hysteresis offers excellent noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. For proper operation using CMOS input, the input signal level should be at a voltage equal to VDD. Using an input signal slightly larger than the threshold but less than VDD for CMOS input can result in slower propagation delay from input to output for example. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and guarantees stable operation across temperature. The very low input capacitance , typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using GND pull-down resistors on the non-inverting input pin (IN pin), as shown in the device block diagram.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17 ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage
- 2.1-V input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Enable Function

The Enable (EN) pin of the UCC27532 has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

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Output Stage

The output stage of the UCC27532 device is illustrated in Figure 24. The UCC27532 device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn on.

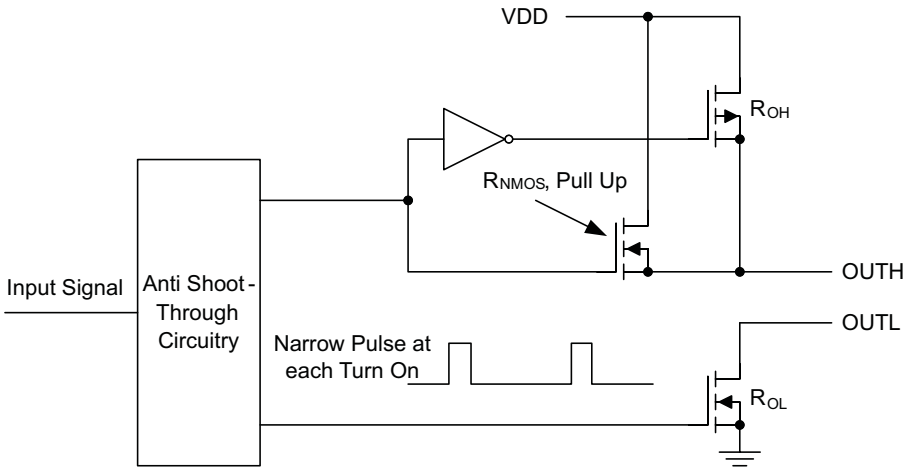


Figure 24. UCC27532 Gate Driver Output Stage

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by ROH parameter. The pull-down structure is composed of a N-Channel MOSFET only. The ROL parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC27532, the effective resistance of the hybrid pull-up structure is approximately 3 x R_{OL}.

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The UCC27532 is capable of delivering 2.5-A source, 5-A Sink (asymmetrical drive) at VDD = 18 V. Strong sink capability in asymmetrical drive results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn-on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches .

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in Off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turn on. This phenomenon is illustrated in Figure 25.

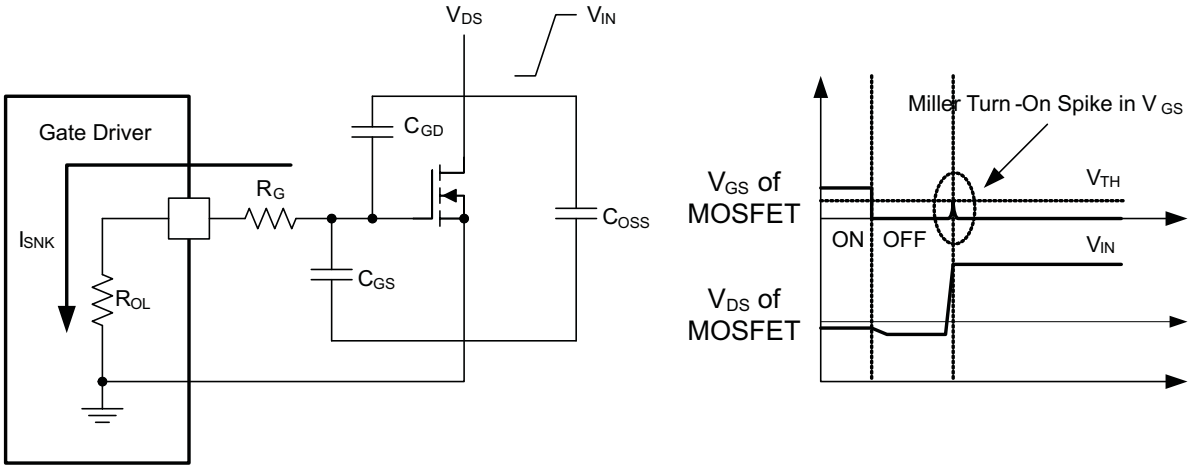


Figure 25. Low Pull-Down Impedance in UCC27532 (output stage mitigates Miller turn-on effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated.

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Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27532 features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver. (2)

There is an equal amount of energy dissipated when the capacitor is discharged. During turn off the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pull-up structure) = 3 x R_{OL} (5)

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Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the 'Thermal Information' section of the datasheet. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled "IC Package Thermal Metrics" (SPRA953A).

PCB Layout

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC27532 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the driver Output pins and the gate of the power switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power switch. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turn-on and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27532DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7532	Samples
UCC27532DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7532	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UCC27532 :

- Automotive: UCC27532-Q1

NOTE: Qualified Version Definitions:

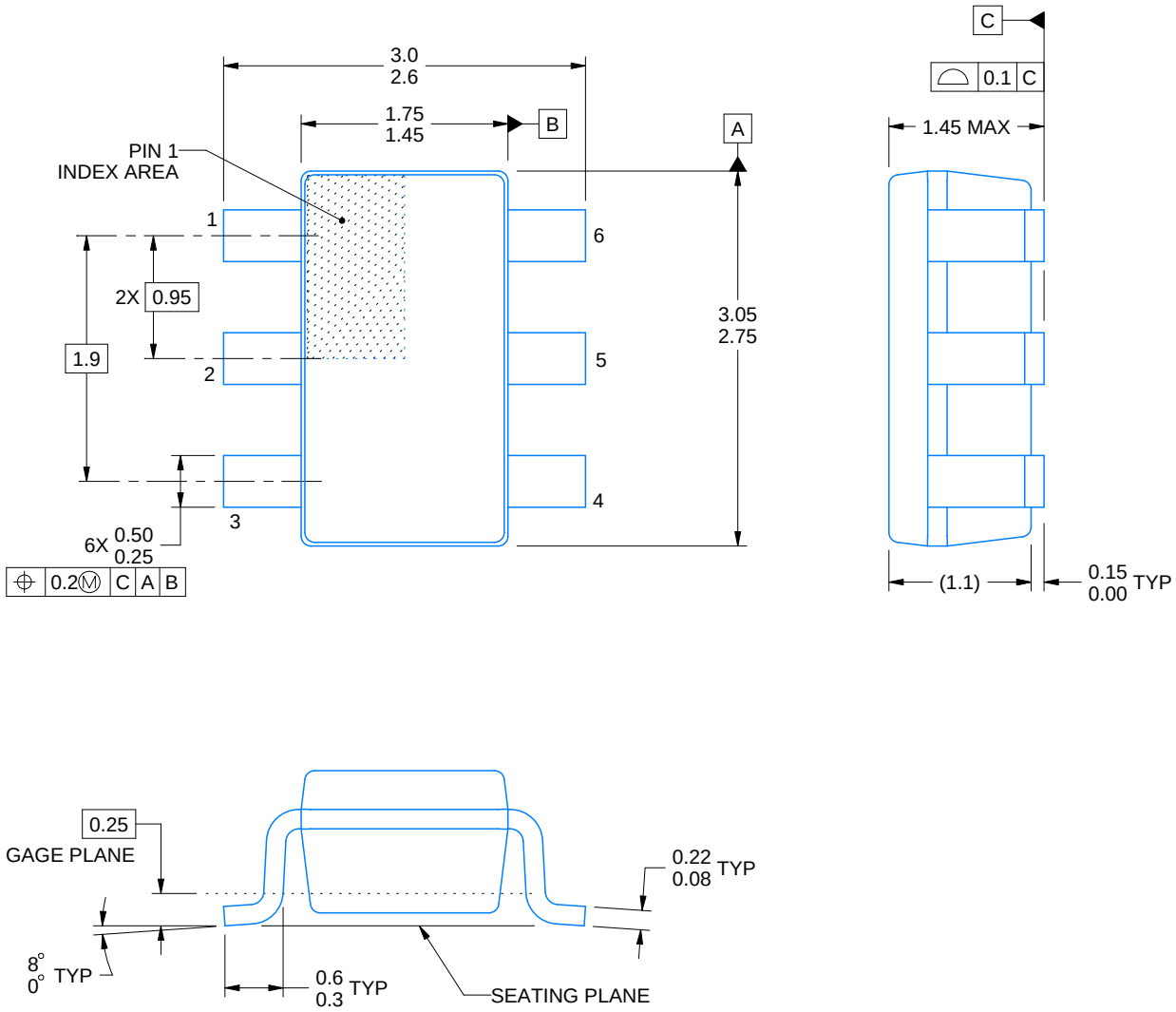
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

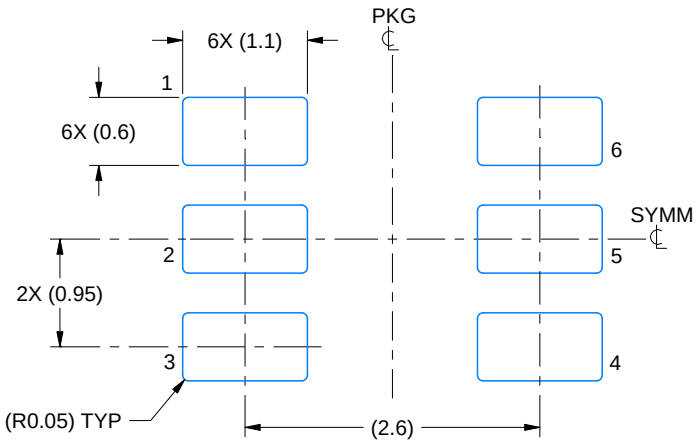
SMALL OUTLINE TRANSISTOR



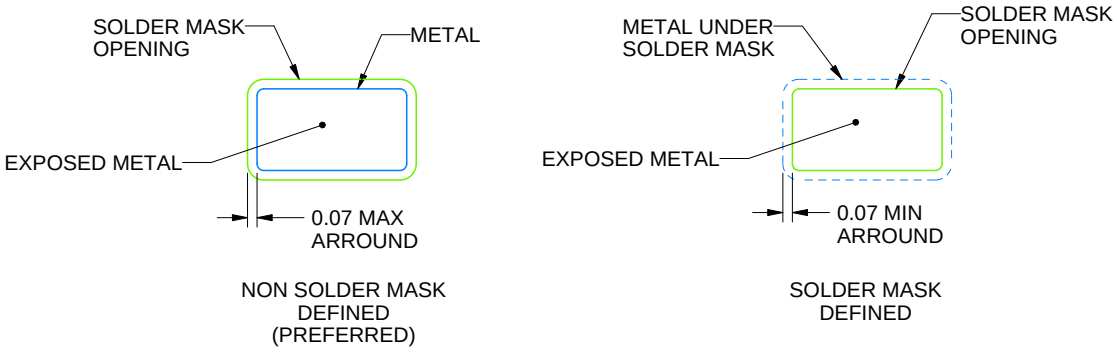
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

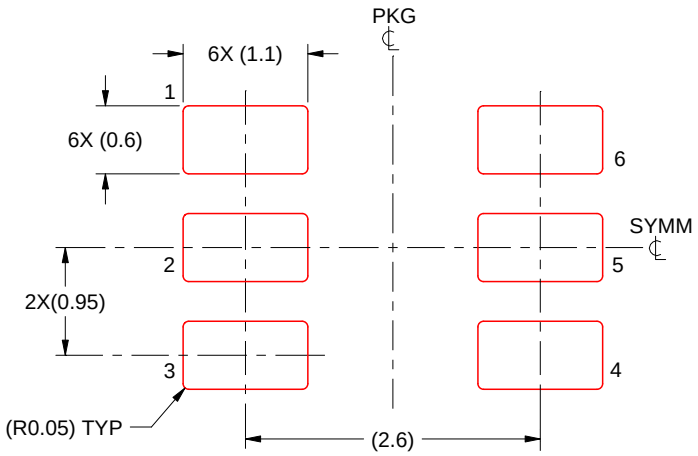


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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