单通道高速低侧栅极驱动器（带有 4A 峰值拉电流和 4A 峰值灌电流的基于 CMOS 的输入阈值）

查询样品: UCC27518A-Q1, UCC27519A-Q1

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 符合器件汽车 **1** 级
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C6**
- 低成本栅极驱动器器件提供 **NPN** 和 **PNP** 离散解决方案的高品质替代产品
- 与 **TI** 的 **TPS2828** 和 **TPS2928** 引脚兼容
- **4A** 峰值拉电流和 **4A** 峰值灌电流对称驱动
- 快速传播延迟（典型值 **17ns**）
- 快速上升和下降时间（典型值 **8ns** 和 **7ns**）
- **4.5V** 至 **18V** 单一电源范围
- 在 **VDD** 欠压闭锁 **(UVLO)** 期间，输出保持低电平（以保证加电和断电时的无毛刺脉冲运行）
- **CMOS** 输入逻辑阈值（带有滞后功能的电源电压）
- 用于高抗噪性的滞后逻辑阈值
- 针对使能功能的使能 **(EN)** 引脚（可不连接）
- 当输入引脚悬空时输出保持在低电平
- 输入引脚绝对最大电压电平不受 **VDD** 引脚偏置电源电压的限制
- **-40°C** 至 **140°C** 的运行温度范围
- **5** 引脚 **DBV** 封装（小外形尺寸晶体管封装 **(SOT)-23**）

应用范围

- 车载应用
- 开关模式电源
- 直流到直流转换器
- 用于数字电源控制器的伴随栅极驱动器器件
- 太阳能、电机控制、不间断电源 **(UPS)**
- 用于新上市的宽带隙电源器件（例如 **GaN**）的栅极驱动器

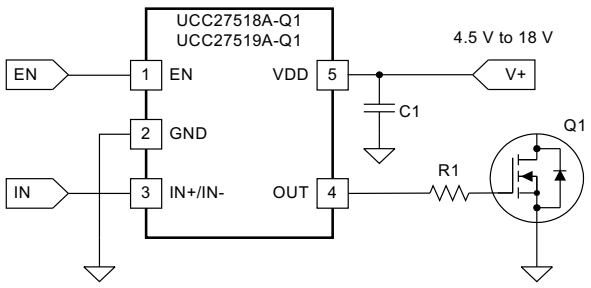
说明

UCC27518A-Q1 和 UCC27519A-Q1 单通道高速低侧栅极驱动器器件有效地驱动金属氧化物半导体场效应晶体管 (MOSFET) 和绝缘栅双极型晶体管 (IGBT) 开关。 借助于固有的大大减少击穿电流的设计，UCC27518A-Q1 和 UCC27519A-Q1 能够灌、拉高峰值电流脉冲进入到电容负载，此电容负载提供了轨到轨驱动能力以及极小传播延迟（典型值为 17ns）。

UCC27518A-Q1 和 UCC27519A-Q1 在 VDD = 12V 时提供 4A 拉电流和 4A 灌电流（对称驱动）峰值驱动电流功能。

UCC27518A-Q1 和 UCC27519A-Q1 在 4.5V 至 18V 的宽 VDD 范围以及 -40°C 到 140°C 的宽温度范围内运行。 VDD 引脚上的内部欠压闭锁 (UVLO) 电路保持 VDD 运行范围之外的输出低电平。 能够运行在诸如低于 5V 的低电压电平上，连同同类产品中最佳的开关特性，使得此器件非常适合于驱动诸如 GaN 功率半导体器件等新上市的宽带隙电源开关器件。 UCC27519A-Q1 可按需提供（只用于预览）。

典型应用图



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这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

说明（继续）

UCC27518A-Q1 和 UCC27519A-Q1 的输入引脚阀值基于 CMOS 逻辑电路，此逻辑电路的阀值电压是 VDD 电源电压的函数。 通常情况下，输入高阀值 (V_{IN-H}) 是 V_{DD} 的 55%，而输入低阀值 (V_{IN-L}) 是 V_{DD} 的 39%。 高阀值和低阀值之间的宽滞后（通常为 V_{DD} 的 16%）提供了出色的抗扰性并使用户能够通过在输入脉宽调制 (PWM) 信号和器件的 INx 引脚间使用 RC 电路来引入延迟。

UCC27518A-Q1 和 UCC27519A-Q1 在 EN 引脚上还特有一个可悬空使能功能。 EN 引脚可以保持在一个不连接的状态，这样可以分别实现 UCC27518A-Q1，UCC27519A-Q1 和 TPS2828，TPS2829 器件间的引脚兼容性。 使能引脚阀值是一个固定电压阀值并且不会随着 V_{DD}偏置电压的改变而变化。 通常情况下，使能高阀值 (V_{EN-H}) 为 2.1V，而使能低阀值 (V_{EN-L}) 是 1.25V。

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ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	20	V
OUT voltage		–0.3	VDD + 0.3	
Output continuous current	I_{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 µs)	I_{OUT_pulsed}(source/sink)		4	
IN+, IN–(4), EN		–0.3	20	V
ESD	Human Body Model, HBM		2500	
	Charged Device Model, CDM SOT-23		1500	
Operating virtual junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{STG}		–65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

THERMAL INFORMATION

THERMAL METRIC(1)		UCC27518A-Q1 UCC27519A-Q1	UNITS
		DBV	
		5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	215.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	136.1	
θ_{JB}	Junction-to-board thermal resistance(4)	43.2	
ψ_{JT}	Junction-to-top characterization parameter(5)	20.3	
ψ_{JB}	Junction-to-board characterization parameter(6)	42.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating ambient temperature range	–40		140	°C
Input voltage, (IN+ and IN–) and Enable (EN)	0		18	V

ELECTRICAL CHARACTERISTICS

VDD = 12 V, T_A = –40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
BIAS Currents							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN– = GND (UCC27518A-Q1)	51	85	123	µA
			IN– = VDD (UCC27519A-Q1)	51	70	103	
Under Voltage Lockout (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.85	4.2	4.57	V
		T_A = –40°C to 140°C		3.8	4.2	4.67	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.19	0.3	0.45	
INPUTS (IN+, IN–)							
V_{IN_H}	Input signal high threshold	VDD = 4.5 V			55	62	%VDD
V_{IN_L}	Input signal low threshold			31	39		
V_{IN_HYS}	Input signal hysteresis				16		
V_{IN_H}	Input signal high threshold	VDD = 12 V			55	59	
V_{IN_L}	Input signal low threshold			31	39		
V_{IN_HYS}	Input signal hysteresis				16		
V_{IN_H}	Input signal high threshold	VDD = 18 V			55	58	
V_{IN_L}	Input signal low threshold			35	38		
V_{IN_HYS}	Input signal hysteresis				17		
ENABLE (EN)							
V_{EN_H}	Enable signal high threshold	VDD = 12 V			2.1	2.3	V
V_{EN_L}	Enable signal low threshold			1	1.25		
V_{EN_HYS}	Enable hysteresis				0.86		

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ELECTRICAL CHARACTERISTICS (continued)

VDD = 12 V, T_A = –40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Source/Sink Current						
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±4		A
Outputs (OUT)						
$V_{DD}–V_{OH}$	High output voltage	VDD = 12 V I_{OUT} = –10 mA		50	90	mV
		VDD = 4.5 V I_{OUT} = –10 mA		60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUT} = 10 mA		5	11	
		VDD = 4.5 V I_{OUT} = 10 mA		6	12	
R_{OH}	Output pull-up resistance(2)	VDD = 12 V I_{OUT} = –10 mA		5	7.5	Ω
		VDD = 4.5 V I_{OUT} = –10 mA		5.0	11	
R_{OL}	Output pull-down resistance	VDD = 12 V I_{OUT} = 10 mA		0.5	1	
		VDD = 4.5 V I_{OUT} = 10 mA		0.6	1.2	
Switching Time						
t_R	Rise time(3)	C_{LOAD} = 1.8 nF		8	12	ns
t_F	Fall time(3)	C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(3)	VDD = 10 V 7-V input pulse, C_{LOAD} = 1.8 nF	6	17	25	
t_{D2}	IN– to output propagation delay(3)	VDD = 10 V 7-V input pulse, C_{LOAD} = 1.8 nF	6	17	24	
t_{D3}	EN to output high propagation delay(3)	C_{LOAD} = 1.8 nF, 5-V enable pulse	4	12	16	
t_{D4}	EN to output low propagation delay(3)	C_{LOAD} = 1.8 nF, 5-V enable pulse	4	12	19	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pullup structure of the output stage of the UCC27518A-Q1 and UCC27519A-Q1.
(3) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4.

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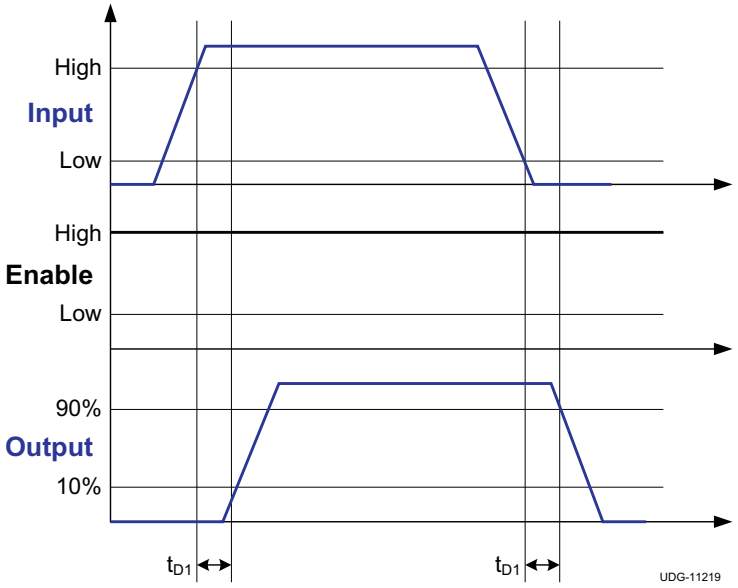


Figure 1. Non-Inverting Configuration (IN+ pin, UCC27519A-Q1)

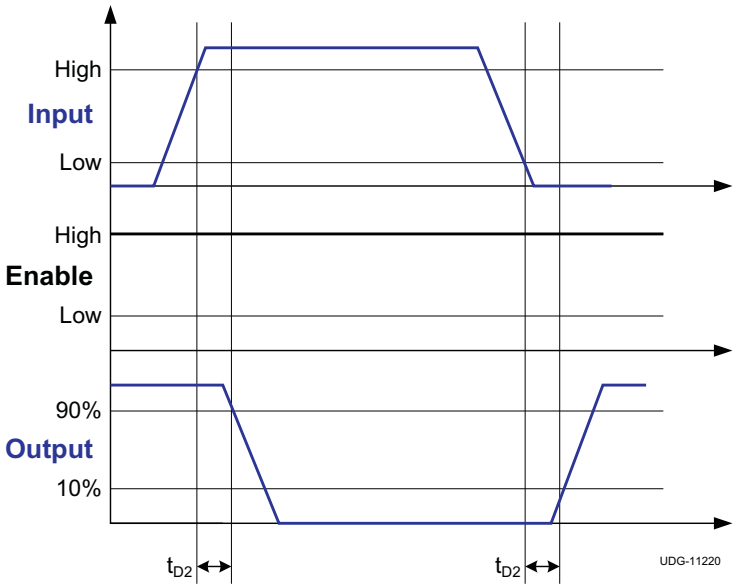


Figure 2. Inverting Configuration (IN– pin, UCC27518A-Q1)

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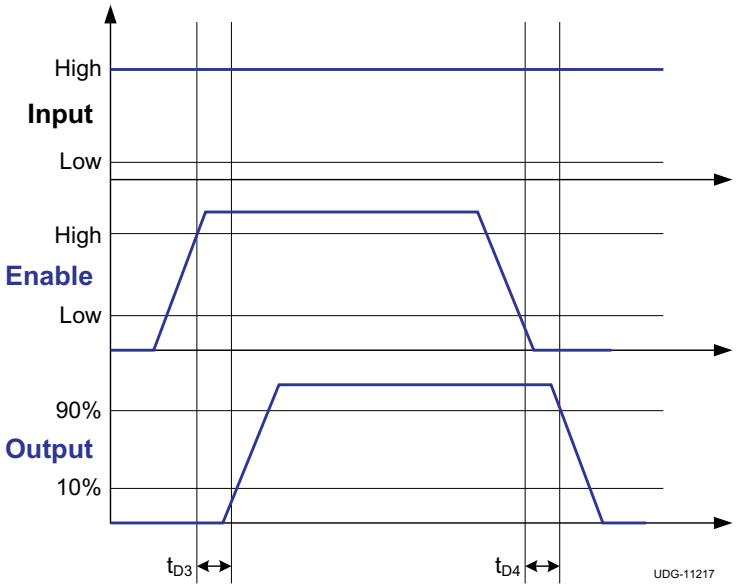


Figure 3. Enable and Disable Function (non-inverting configuration, UCC27519A-Q1)

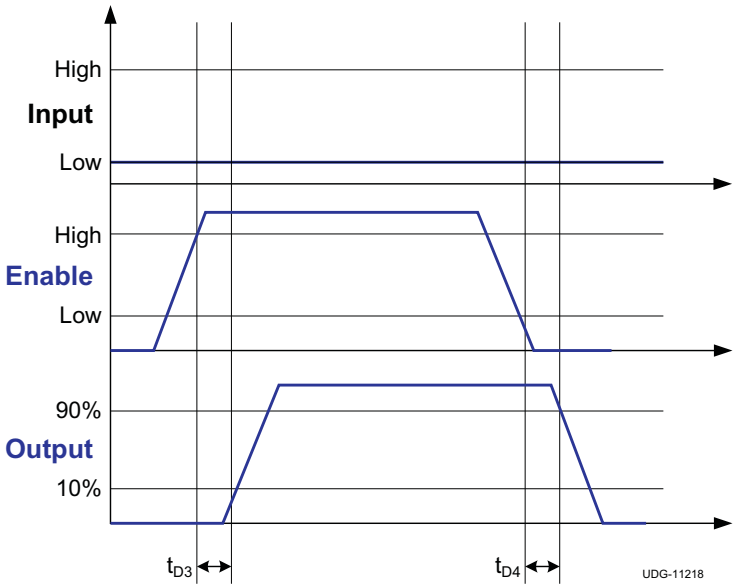
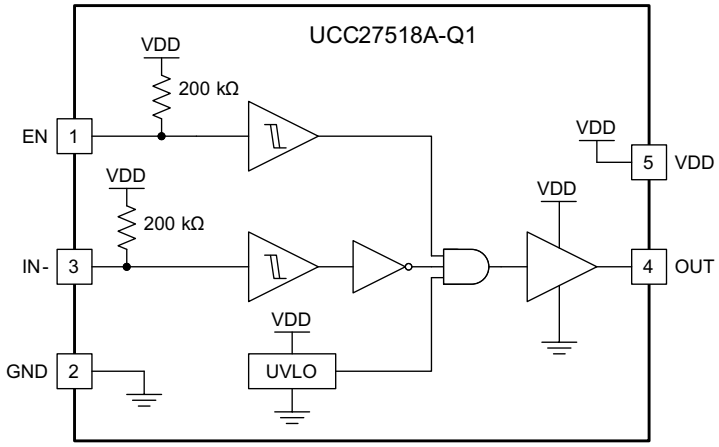


Figure 4. Enable and Disable Function (inverting configuration, UCC27518A-Q1)

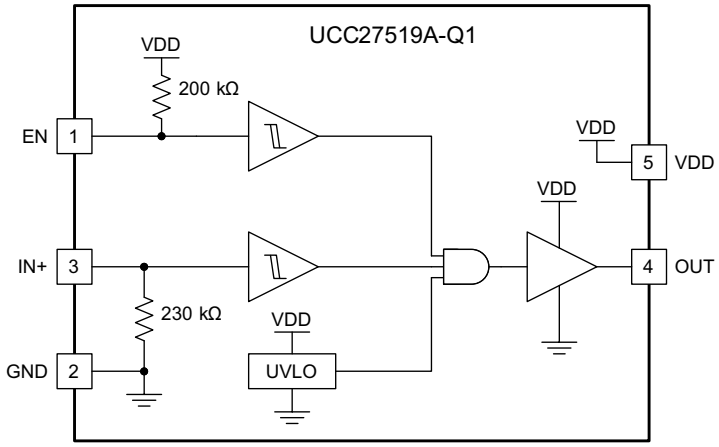
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DEVICE INFORMATION

UCC27518A-Q1 Functional Block Diagram

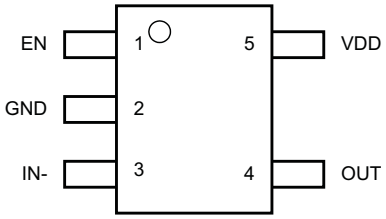


UCC27519A-Q1 Functional Block Diagram

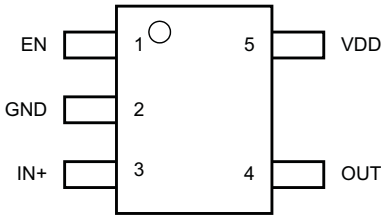


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UCC27518A-Q1
SOT-23 DBV
(Top View)



UCC27519A-Q1
SOT-23 DBV
(Top View)



TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
1	EN	I	**Enable input:** (EN biased LOW disables output regardless of Input state, EN biased high or floating enables output, EN is allowed to float hence it is pin-to-pin compatible with TPS282X N/C pin)
2	GND	–	**Ground:** All signals referenced to this pin.
3	IN–	I	**Input:** Inverting input in the UCC27518A-Q1, output held LOW if IN– is unbiased or floating
	IN+	I	**Input:** Non-inverting input in the UCC27519A-Q1, output held LOW if IN+ is unbiased or floating
4	OUT	O	**Sourcing and sinking current output of driver**.
5	VDD	i	**Supply input.**

Table 1. Device Logic Table

EN	UCC27518A-Q1		UCC27519A-Q1	
	IN– PIN	OUT PIN	IN+ PIN	OUT PIN
H	L	H	L	L
H	H	L	H	H
L	Any	L	Any	L
Any	x(1)	L	x(1)	L
x(1)	L	H	L	L
x(1)	H	L	H	H

(1) x = Floating Condition

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TYPICAL CHARACTERISTICS

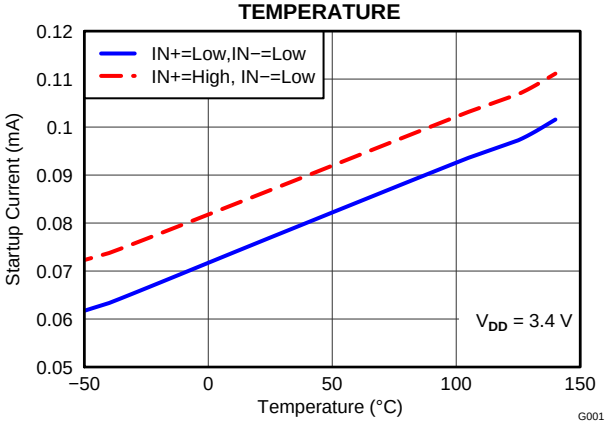


Figure 5.

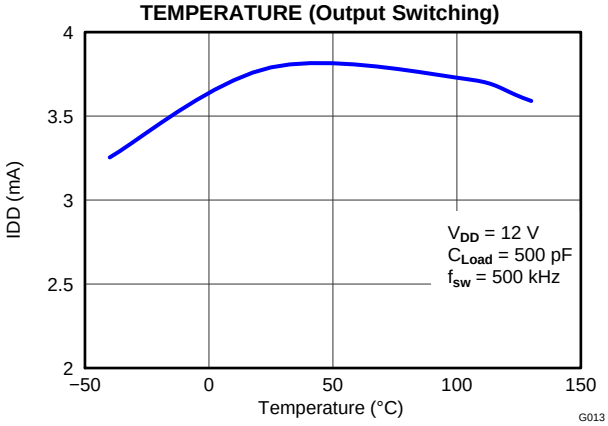


Figure 6.

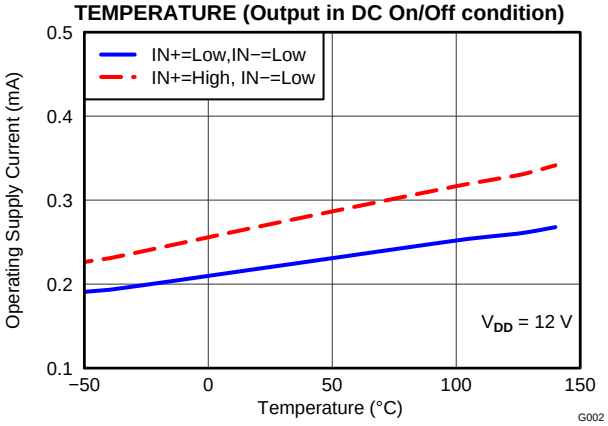


Figure 7.

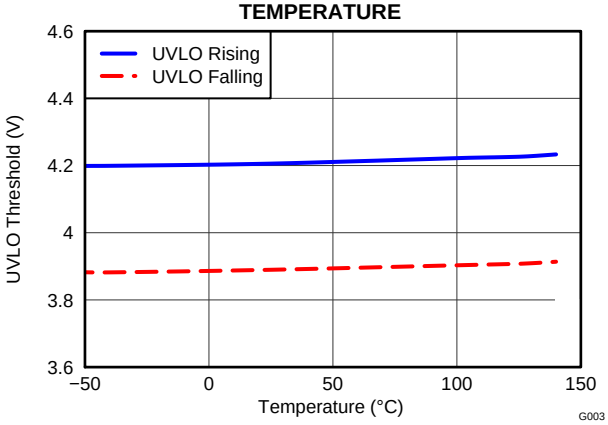


Figure 8.

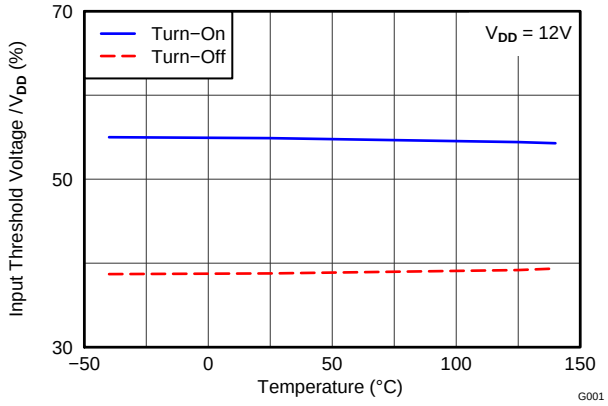


Figure 9.

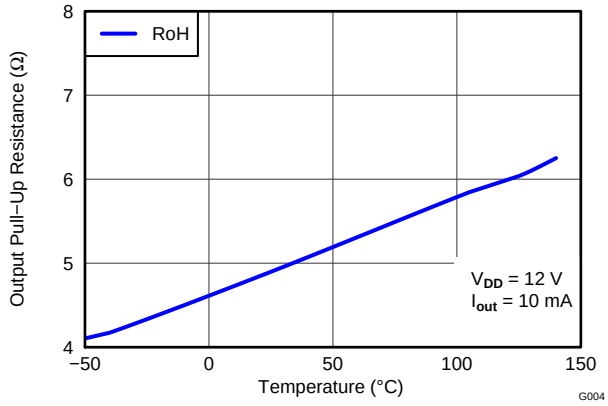


Figure 10.

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TYPICAL CHARACTERISTICS (continued)

OUTPUT PULL-DOWN RESISTANCE vs TEMPERATURE

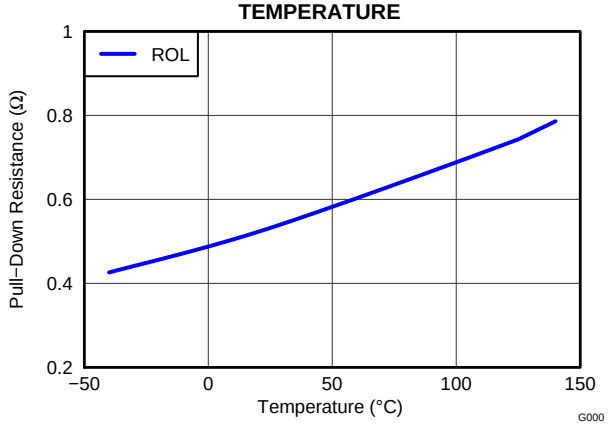


Figure 11.

RISE TIME vs TEMPERATURE

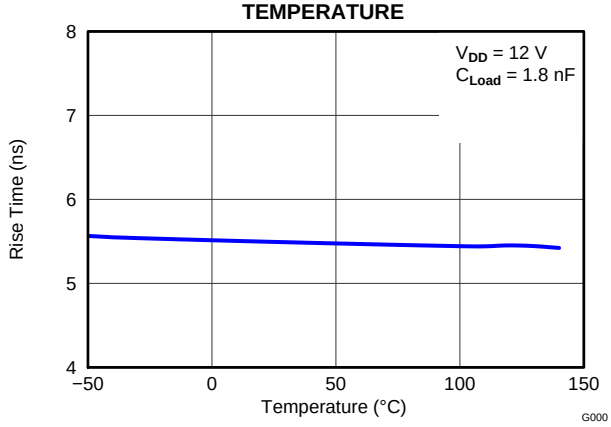


Figure 12.

FALL TIME vs TEMPERATURE

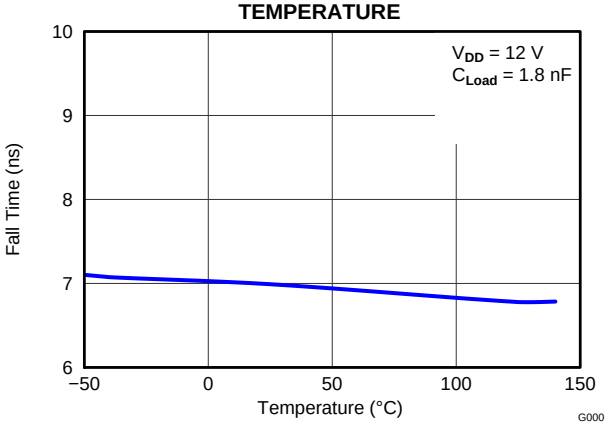


Figure 13.

INPUT TO OUTPUT PROPAGATION DELAY vs TEMPERATURE

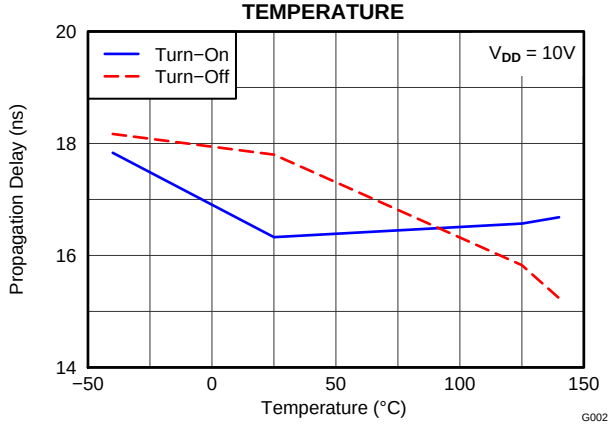


Figure 14.

OPERATING SUPPLY CURRENT vs FREQUENCY

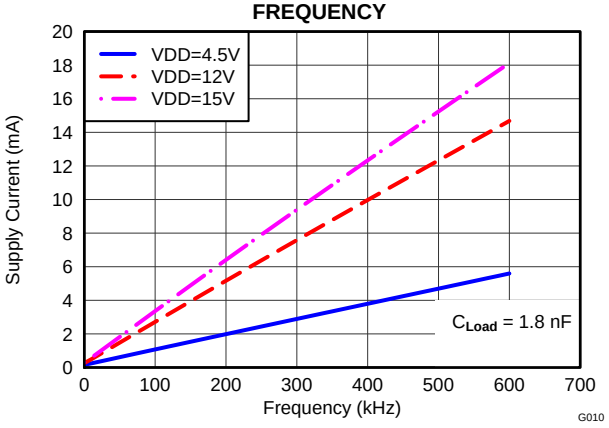


Figure 15.

RISE TIME vs SUPPLY VOLTAGE

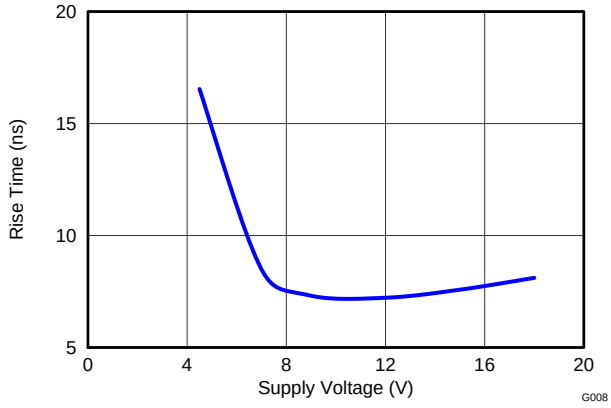


Figure 16.

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TYPICAL CHARACTERISTICS (continued)

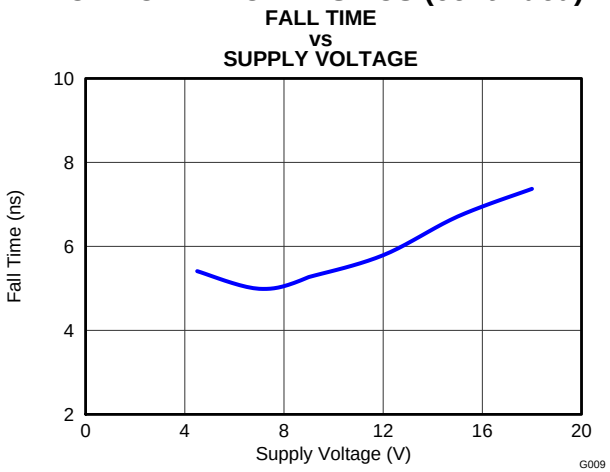


Figure 17.

APPLICATION INFORMATION

Introduction

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

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UCC2751x Product Family

The UCC2751x family of gate-driver products (Table 2) represent Texas Instruments' latest generation of single-channel, low-side high-speed gate driver devices featuring high-source/sink current capability, industry best-in-class switching characteristics and a host of other features (Table 3) all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 2. UCC2751x Product Family Summary

PART NUMBER(1)	PACKAGE	PEAK CURRENT (SOURCE, SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV	SOT-23, 6 pin	4-A, 8-A (Asymmetrical Drive)	CMOS and TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS	3-mm x 3-mm WSON, 6 pin		
UCC27516DRS	3-mm x 3-mm WSON, 6 pin	4-A, 4-A (Symmetrical Drive)	
UCC27517DBV, UCC27517AQ1	SOT-23, 5 pin		
UCC27518DBV, UCC27518ADBVQ1	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV, UCC27519ADBVQ1	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

Table 3. UCC2751x Family of Features and Benefits

FEATURE	BENEFIT
High Source, Sink Current Capability 4 A, 4 A (Symmetrical)	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low pulse transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design Low VDD operation ensures compatibility with emerging wide band-gap power devices such as GaN
Expanded Operating Temperature range of –40°C to 140°C (See ELECTRICAL CHARACTERISTICS table)	
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Ability of input pins (and enable pin in UCC27518A-Q1 and UCC27519A-Q1) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
CMOS/TTL compatible input threshold logic with wide hysteresis in UCC27518A-Q and UCC27519A-Q	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power
CMOS input threshold logic in UCC27518A-Q1 and UCC27519A-Q1 (VIN_H – 70% VDD, VIN_L – 30% VDD)	Well suited for slow input voltage signals, with flexibility to program delay circuits (RCD)

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Typical Application Diagram

Typical application diagram of UCC27518A-Q1 and UCC27519A-Q1 devices is shown in Figure 18.

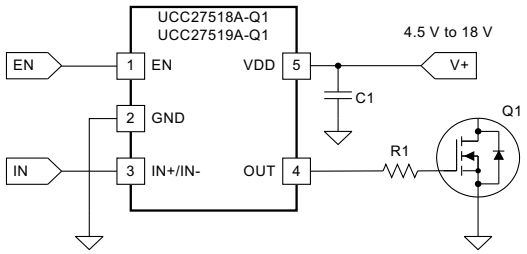


Figure 18. Typical Application Diagram

VDD and Undervoltage Lockout

The UCC2751x devices have internal Under Voltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (such as when V_{DD} voltage less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.

For example, at power up, the UCC2751x driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the non-inverting device (PWM signal applied to IN+ pin) shown in Figure 19, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting device (PWM signal applied to IN– pin) shown in Figure 20, the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input.

Because the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

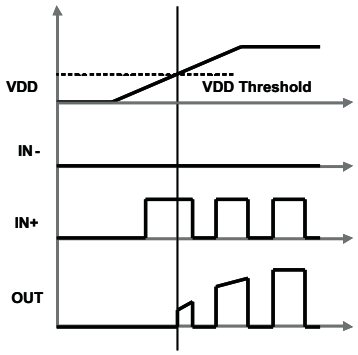


Figure 19. Power-Up (Non-Inverting Drive)

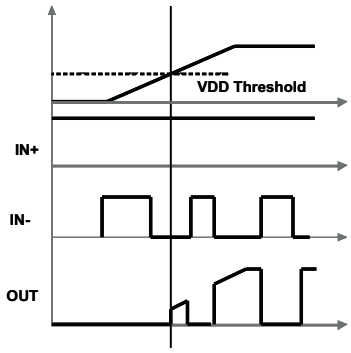


Figure 20. Power-Up (Inverting Drive)

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Operating Supply Current

The UCC27518A-Q1 and UCC27519A-Q1 features very low quiescent I_{DD} currents. The typical operating supply current in Under Voltage LockOut (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to DEVICE INFORMATION for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the IDD current as a function of switching frequency at different VDD bias voltages under 1.8-nF switching load is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

Input Stage

The input pins of UCC27518A-Q1 and UCC27519A-Q1 are based on CMOS input logic where the threshold voltage level is a function of the bias voltage applied on the VDD pin. Typically, the Input High Threshold (V_INH) is 55% VDD and Input Low Threshold (VIN_L) is 39% VDD. Hysteresis (typically 19% VDD) available on the input threshold offers noise immunity. With high VDD voltages resulting in wide hysteresis, slow dV/dt input signals are acceptable in the INx pins and RC circuits can be inserted between the input PWM signal and the INx pins of UCC27518A-Q1 and UCC27519A-Q1, to program a delay between the input signal and output transition.

Enable Function

The Enable pin is based on a non-inverting configuration (active high operation). When EN pin is driven high the output is enabled and when EN pin is driven low the output is disabled. Unlike input pin, the enable pin threshold is based on a TTL/CMOS compatible input threshold logic that does not vary with the supply voltage. Typically, the Enable High Threshold (V_ENH) is 2.1 V and Enable Low Threshold (VEN_L) is 1.25 V. Thus the EN pin can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The EN pin is internally pulled up to VDD using pull-up resistor as a result of which the output of the device is enabled in the default state. Hence the EN pin can be left floating or Not Connected (N/C) for standard operation, when enable feature is not needed. Essentially, this allows the UCC27518A-Q1 and UCC27519A-Q1 devices to be pin-to-pin compatible with TI's previous generation drivers TPS2828/9 respectively, where pins #1 is N/C pin.

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Output Stage

The UCC27518A-Q1 and UCC27519A-Q1 are capable of delivering 4-A source, 4-A sink (symmetrical drive) at VDD = 12 V. The output stage of the UCC27518A-Q1 and UCC27519A-Q1 devices are illustrated in Figure 21. The UCC27518A-Q1 and UCC27519A-Q1 devices features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

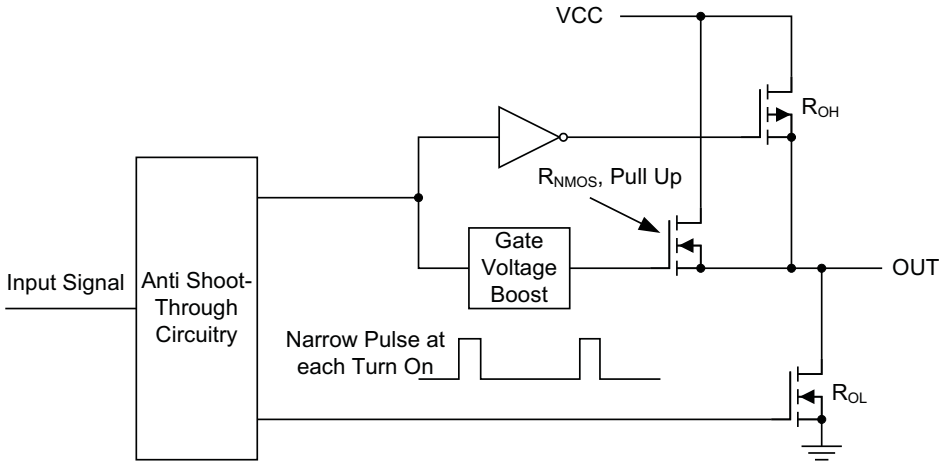


Figure 21. UCC2751x Gate Driver Output Structure

The R_{OH} parameter (see ELECTRICAL CHARACTERISTICS) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, because the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by R_{OH} parameter. The pull-down structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC27518A-Q1 and UCC27519A-Q1, the effective resistance of the hybrid pull-up structure is approximately 1.4 x R_{OL}.

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

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Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27518A-Q1 and UCC27519A-Q1 features very low quiescent currents (less than 1 mA, refer Figure 7) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power MOSFET/IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD}$ x V_{DD}, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = Q_G \times V_{DD} \times f_{SW} \times \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = 1.4 × R_{OL} (5)

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Low Propagation Delays

The UCC27518A-Q1 and UCC27519A-Q1 driver device features best-in-class input-to-output propagation delay of 17 ns (typ) at VDD = 12 V. This promises the lowest level of pulse transmission distortion available from industry standard gate driver devices for high-frequency switching applications. As seen in Figure 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the THERMAL INFORMATION. For detailed information regarding the thermal information table, please refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

PCB Layout

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27518A-Q1 and UCC27519A-Q1 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A, 4-A peak current is at VDD = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch and ground of PWM controller at one point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

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REVISION HISTORY

Changes from Original (August 2013) to Revision A	Page
• Changed 文档状态从*产品预览*改为*生成数据*	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27518AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EAFQ	Samples
UCC27519AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	519Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

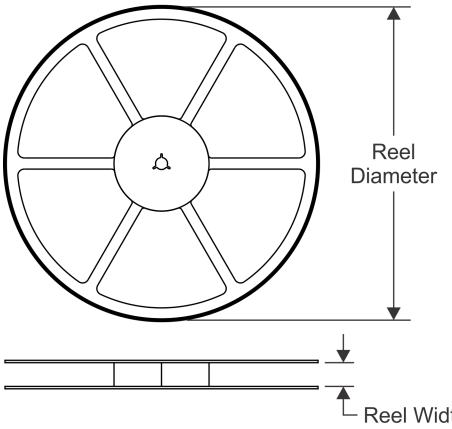
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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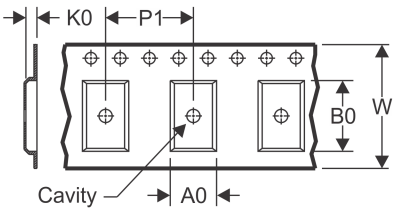
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

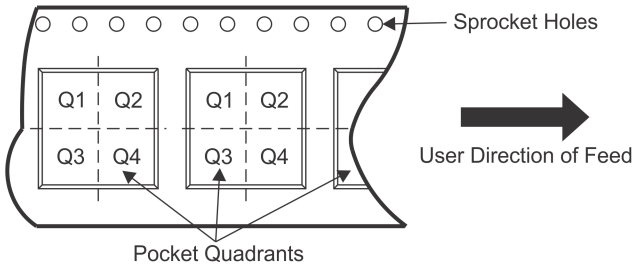


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

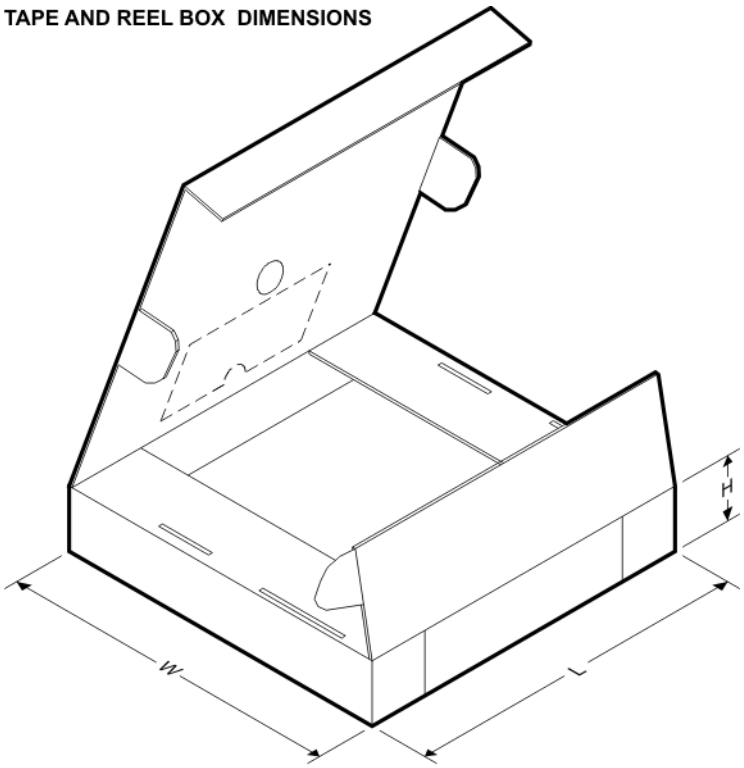
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27518AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27519AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

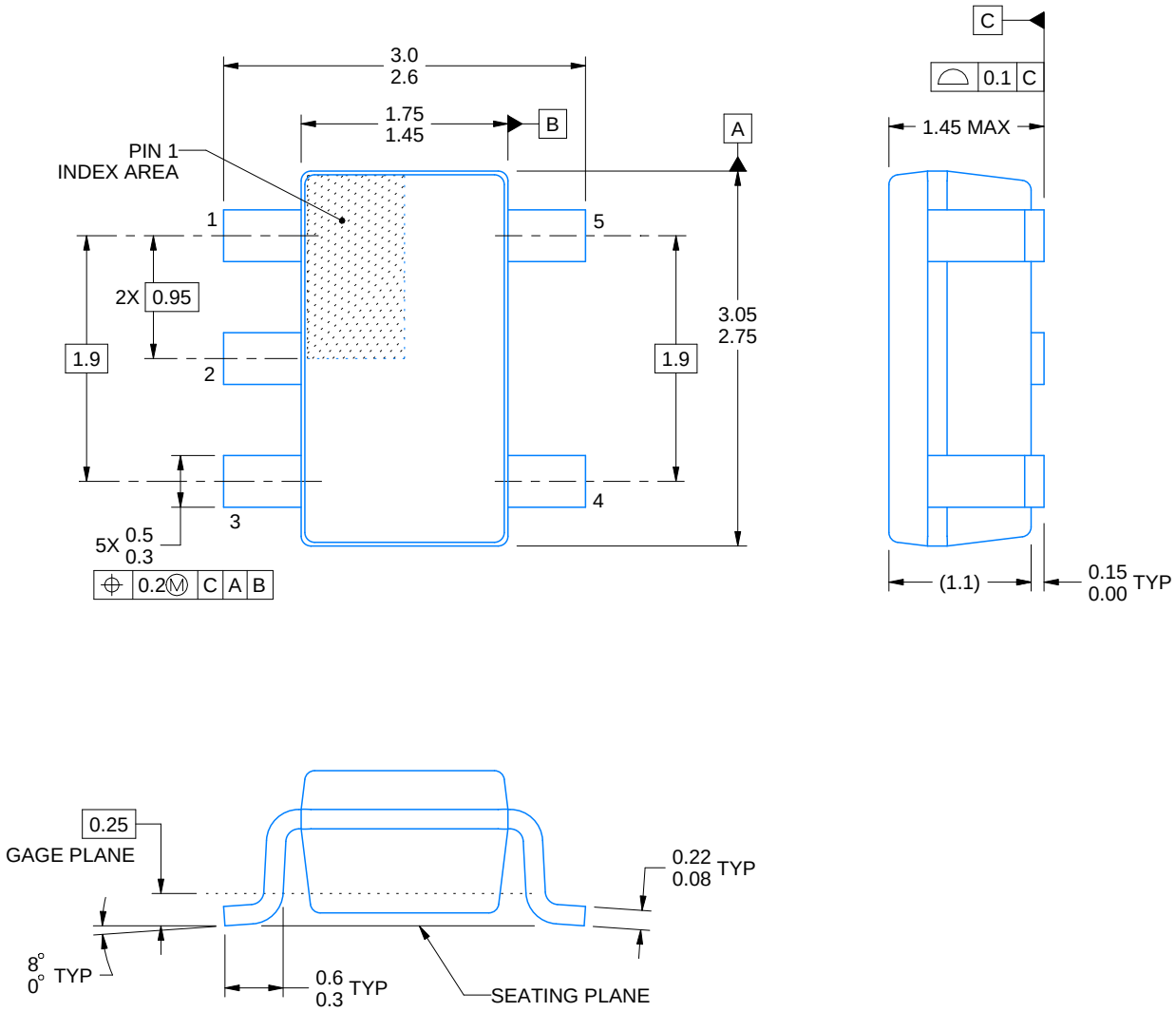
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27518AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
UCC27519AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

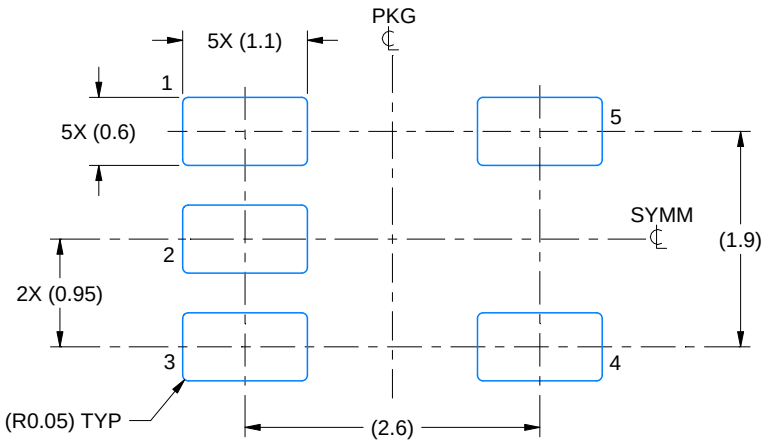
SMALL OUTLINE TRANSISTOR



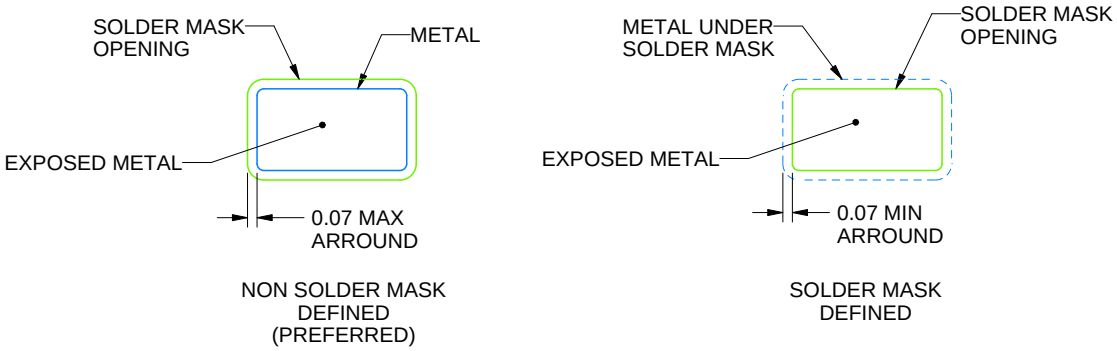
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

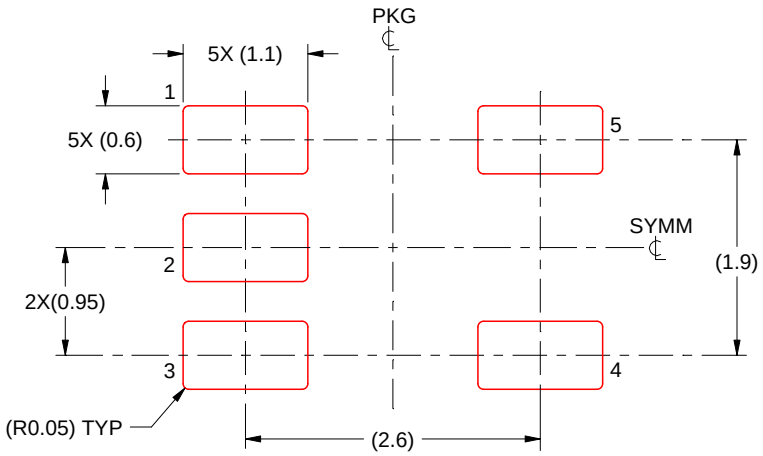


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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