LMG1025-Q1 Automotive Low Side GaN and MOSFET Driver For High Frequency and Narrow Pulse Applications

1 Features

- AEC-Q100 grade 1 qualified
- Very high switching frequency operation capability
- 1.25-ns typical minimum input pulse width
- 2.6-ns typical rising propagation delay
- 2.9-ns typical falling propagation delay
- 300-ps typical pulse distortion
- Independent 7-A pull-up and 5-A pull-down current
- 650-ps typical rise time (220-pF load)
- 850-ps typical fall time (220-pF load)
- Available in 2-mm x 2-mm package
- Inverting and non-inverting inputs
- UVLO and over-temperature protection
- Single 5-V supply voltage

2 Applications

- LiDAR
- ToF
- High efficiency power conversion
- Precision motor drives

3 Description

The LMG1025-Q1 device is a single channel low-side driver targeted at driving enhancement-mode GaN FETs and logic-level silicon FETs in very high switching frequency applications. Very high switching frequency capability combined with very narrow pulse width and very small pulse distortion capability of the LMG1025-Q1 significantly enhances the LiDAR and ToF application performance. Small pulse width allows power/current to increase in these applications. Small distortion allows precise image mapping in LiDAR and ToF applications. The architecture of the device allows for extremely small propagation delay of 2.9 ns. Small propagation delay significantly improves the control loop response time and thus overall performance of the power converters. Split output allows the drive strength to be independently adjusted. This allows adjustment of rise and fall time by connecting external resistors between the gate and OUTH and OUTL, respectively.

The driver features undervoltage lockout (UVLO) and over-temperature protection (OTP) to ensure the device is not damaged in overload or fault conditions. LMG1025-Q1 is available in an extremely compact Q100 automotive qualified package to meet the form-factor and gate loop inductance requirements of new GaN-based very high switching frequency automotive applications.

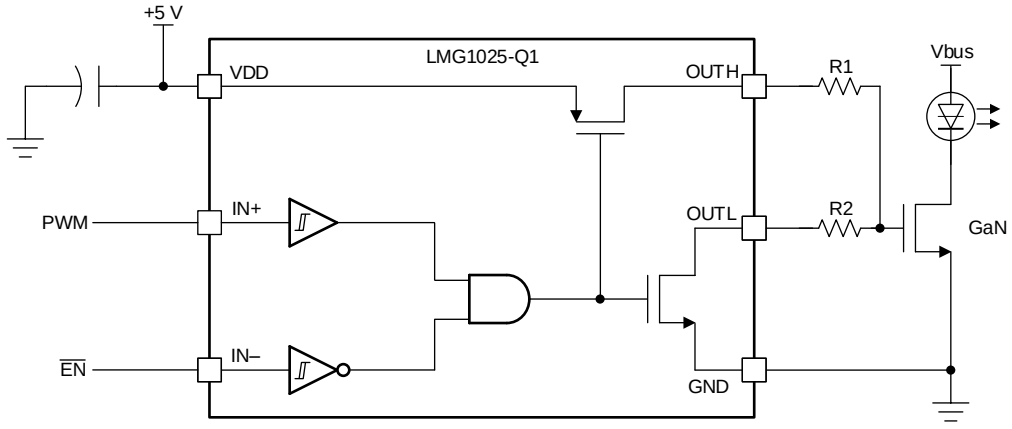
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM) (mm)
LMG1025-Q1	WSON(6)	2-mm x 2-mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Typical (Simplified) System Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics ... 5
6.7 Typical Characteristics ... 6
7 Detailed Description ... 7
7.1 Overview ... 7
7.2 Functional Block Diagram ... 7
7.3 Feature Description ... 7
7.4 Device Functional Modes ... 8
8 Application and Implementation ... 9
8.1 Application Information ... 9
8.2 Typical Application ... 9
9 Power Supply Recommendations ... 14
10 Layout ... 15
10.1 Layout Guidelines ... 15
10.2 Layout Example ... 15
11 Device and Documentation Support ... 16
11.1 Receiving Notification of Documentation Updates 16
11.2 Community Resources ... 16
11.3 Trademarks ... 16
11.4 Electrostatic Discharge Caution ... 16
11.5 Glossary ... 16
12 Mechanical, Packaging, and Orderable Information ... 16

ADVANCE INFORMATION

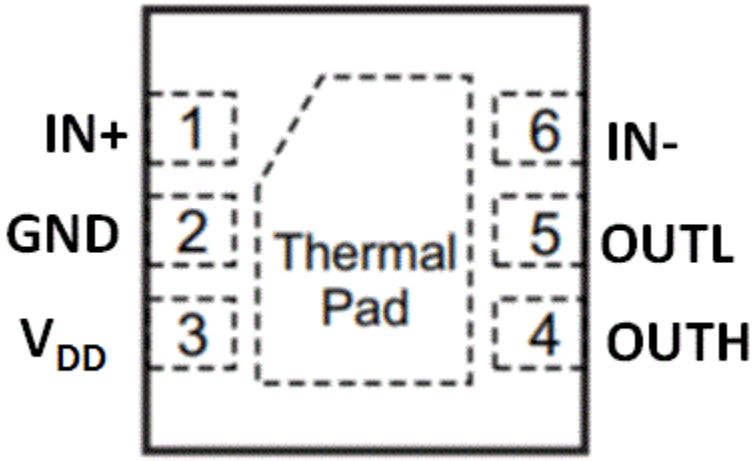
4 Revision History

Changes from Original (May 2019) to Revision A	Page
• Changed select disclosure status to public.	1

Copyright © 2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

DEE
6-Pin WSON
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GND	2	G	Power supply and source return. Connect with a direct path to the transistor's source.
IN+	1	I	Positive logic-level input.
IN–	6	I	Negative logic-level input.
OUTL	5	O	Pull-down gate drive output. Connect through an optional resistor to the target transistor's gate.
OUTH	4	O	Pull-up gate drive output. Connect through a resistor to the target transistor's gate.
VDD	3	P	Input voltage supply. Decouple through a compact capacitor to GND.
Thermal Pad	-	-	Internally connected to GND through substrate. Connect this pad to large copper area, generally a ground plane.

(1) I=Input, O=Output, P=Power, G=Ground

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

All voltages are with respect to GND pin.(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	5.75	V
V_{IN}	IN+, IN- pin voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	OUTH, OUTL pin voltage	-0.3	5.75	V
T_{STG}	Storage Temperature	-55	150	°C
T_J	Operating Temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stessing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{INx}	IN+ or IN- input voltage	0		V_{DD}	V
V_{OUTx}	OUTH, OUTL pin voltage	0		5.25	V
T_J	Operating Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMG1025-Q1 DEE (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	38.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
$I_{VDD, Q}$	VDD Quiescent Current	IN_+ = IN_- = 0 V			75	µA
$I_{VDD, op}$	VDD Operating Current	fsw = 30 MHz, no load		40		mA
		fsw = 30 MHz, 100-pF load		51		mA
$V_{DD, UVLO}$	Under-voltage Lockout	V_{DD} rising	4.0		4.35	V
$\Delta V_{DD, UVLO}$	UVLO Hysteresis			85		mV
T_{OTP}	Over temperature shutdown, turn-off threshold			170		°C
ΔT_{OTP}	Over temperature hysteresis			20		°C
Input DC Characteristics						
V_{IH}	IN+, IN- high threshold		1.7		2.6	V
V_{IL}	IN+, IN- low threshold		1.1		1.8	V
V_{HYST}	IN+, IN- hysteresis		0.5		1	V
R_{IN+}	Positive input pull-down resistance	To GND	100	150	250	kΩ
R_{IN-}	Negative input pull-up resistance	to V_{DD}	100	150	250	kΩ
C_{IN+}	Positive input pin capacitance	To GND		1.45		pF
C_{IN-}	Negative input pin capacitance	To GND		1.45		pF
Output DC Characteristics						
V_{OL}	OUTL voltage	I_{OUTL} = 100 mA, IN+= IN- = 0 V			36	mV
V_{DD}-V_{OH}	OUTH voltage	I_{OUTH} = 100 mA, IN+= 5 V, IN- = 0 V, V_{DD} = 5 V			50	mV
I_{OH}	Peak source current	V_{OUTH} = 0 V, IN+= 5 V, IN- = 0 V, V_{DD} = 5 V		7		A
I_{OL}	Peak sink current	V_{OUTL} = 5 V, IN+= IN- = 0 V, V_{DD} = 5 V		5		A

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{start}	Startup Time, V_{DD} rising above UVLO	IN- = GND, IN+ = V_{DD} , V_{DD} rising to 4.2 V to OUTH rising		40	70	µs
$t_{shut-off}$	ULVO falling	IN- = GND, IN+ = VDD , VDD falling below 4.1 V to OUTH falling	1	1.9	3.1	µs
$t_{pd, r}$	Propagation delay, turn on	IN- = 0 V, IN+ to OUTH, 100-pF load		2.6		ns
$t_{pd, f}$	Propagation delay, turn off	IN- = 0 V, IN+ to OUTL, 100-pF load		2.9		ns
Δt_{pd}	Pulse positive distrortion, ($t_{pd, f}$ - $t_{pd, r}$)		0	300		ps
t_{rise}	Output rise time	0Ω series 220 pF load(1)		650		ps
t_{fall}	Output fall time	0Ω series 220 pF load(1)		850		ps
t_{min}	Minimum input pulse width that changes output state	0Ω series 220 pF load(1)		1.25		ns

(1) refer to the test circuit in section x.xx of this document

ADVANCE INFORMATION

6.7 Typical Characteristics

VDD = 5 V

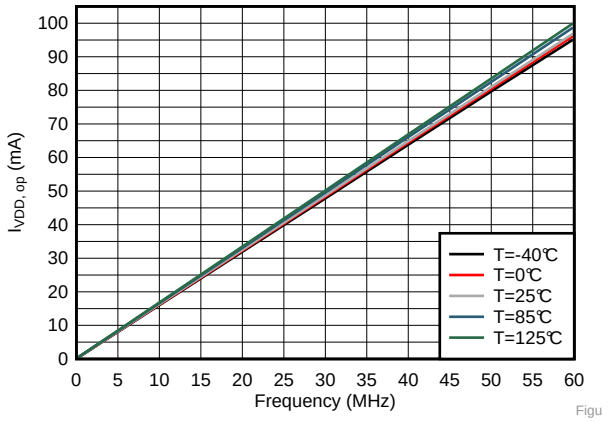


Figure 1. $I_{VDD,op}$ with 2 Ω in series with 100 pF load

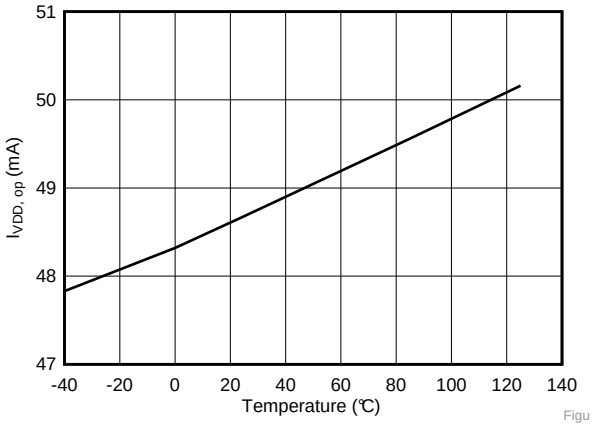


Figure 2. $I_{VDD,op}$ with 2 Ω in series with 100 pF load

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

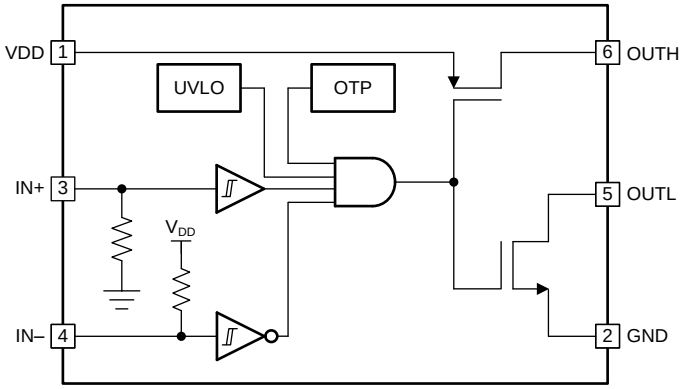
7 Detailed Description

7.1 Overview

LMG1025-Q1 is a high-performance low-side 5-V gate driver for GaN and logic-level silicon power transistors. While it is designed to function well in high-speed applications, such as wireless power transmission and LiDAR / ToF applications, it can be used in any application where a low-side driver is required.

The LMG1025-Q1 is optimized to provide the lowest propagation delay through the driver to the power transistor. By using modern 5-V logic devices, the propagation delay can be minimized.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stage

The input stage features two Schmitt-triggers at the pins IN+ and IN– to reduce sensitivity to noise on the inputs. IN+ signal and the inverted IN– signal are both sent to an AND gate. IN+ is connected with a pull-down resistor while IN– is connected with a pull-up resistor to prevent unintended turnon. The output signal will follow the difference between IN+ and IN–. Both IN+ and IN– are single ended inputs, and these two pins cannot be used as a differential input pair.

7.3.2 Output Stage

LMG1025-Q1 provides 7-A source, 5-A sink (asymmetrical drive) peak-drive current capability, and features a split output configuration. The OUTH and OUTL outputs of the LMG1025-Q1 allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently adjust the turnon and turnoff drive strengths to control slew rate and EMI, and to control ringing on the gate signal. For GaN FETs, controlling ringing is important to reduce stress on the GaN FET and driver. The output stage OUTL is also pulled down in undervoltage condition, which prevents the unintended charge accumulation of device Ciss.

7.3.3 Bias Supply and Under Voltage Lockout

LMG1025-Q1 features nominal 5 V and maximum 5.25 V of supply voltage, and its absolute maximum supply voltage is 5.75 V. In the design, it is recommended to limit the variability of the power supply to be within 5% (0.25 V), and the overshoot voltage during switching transient not to exceed the absolute maximum voltage. Refer to Section VDD and Overshoot for more the detailed design guide. LMG1025-Q1 also features internal undervoltage lockout (UVLO) to protect the driver and circuit in case of fault conditions. The UVLO point is setup between 4.1 V and 4.2 V with a hysteresis of 85mV. This UVLO level is specifically designed to guarantee that GaN power devices can be switched at a low RDS(ON) region. During UVLO condition, the OUTL is pulled down to ground.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

7.4 Device Functional Modes

Table 1. Truth Table

IN-	IN+	OUTH	OUTL
L	L	Open	L
L	H	H	Open
H	L	Open	L
H	H	Open	L

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3-V signal to the gate-drive voltage (such as 5 V) in order to fully turn on the power device and minimize conduction losses.

Gate drivers effectively provide the buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LMG1025-Q1 is a 60-MHz low-side gate driver for enhancement mode GaN FETs and Si FETs in a singleended configuration. The split-gate outputs with strong source and sink capability provides flexibility to adjust the turnon and turnoff strength independently. As a low side driver, LMG1025-Q1 can be used in a variety of applications, including different power converters, LiDAR, time-of-flight laser drivers, class-E wireless chargers, synchronous rectifiers, and augmented reality. LMG1025-Q1 can also be used as a high frequency low current laser diode driver, or as a signal buffer with very fast rise/fall time.

8.2 Typical Application

The LMG1025-Q1 is designed to be used with a single low-side, ground-referenced GaN or logic-level FET, as shown in Figure 3. Independent gate drive resistors, R1 and R2, are used to independently control the turnon and turnoff drive strengths, respectively. For fast and strong turnoff, R2 can be shorted and OUTL directly connected to the transistor's gate. For symmetric drive strengths, it is acceptable to short OUTH and OUTL and use a single gate-drive resistor.

It is strongly recommended to use at least a 2-Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing. Ringing has to be ensured to be below V_{DD}+0.3 V.

For applications requiring smaller resistance, please contact the factory for guidance.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

Typical Application (continued)

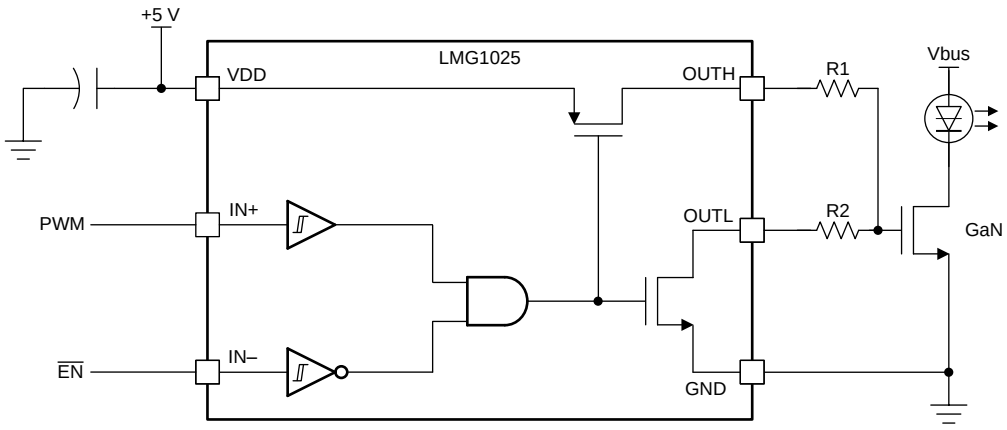


Figure 3. Typical Implementation of a Circuit

8.2.1 Design Requirements

When designing a multi-MHz (or nano-second pulse) application that incorporates the LMG1025-Q1 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

8.2.2 Detailed Design Procedure

8.2.2.1 Handling Ground Bounce

For the best switching performance and gate loop with lowest parasitics, it is recommended to connect the ground return pin of LMG1025-Q1 as close as possible to the source of the low-side FET in a low inductance manner. However, doing so can cause the ground of LMG1025-Q1 to bounce relative to the system or controller ground and lead to erroneous switching logic on the input so as mis-turn on/off on the output.

First of all, LMG1025-Q1 has input hysteresis built into the input buffers to help counteract this effect. The maximum di/dt allowed to prevent the input voltage transient from exceeding the input hysteresis is given by Equation 1

$$\frac{di_S}{dt} = \frac{V_{HYST}}{L_{RS}}$$

where

- Where LRS is the inductance of the sense resistor,
- VHYST is the hysteresis of the input pin,
- and dis/dt is the maximum allowed current slew rate. (1)

For an assumed parasitic inductance of 0.5 nH and a minimum hysteresis of 0.5 V, the maximum slew rate is 1 A/ns. Many applications would exhibit higher current slew rates, up to the 10 A/ns range, which would make this approach impractical. The stability of this approach can be improved by using the IN– input for the PWM signal and locally tying IN+ to VDD. By using the inverting input, the transient voltage applied to the input pin reinforces the PWM signal in a positive feedback loop. While this approach would reduce the probability of false pulses or oscillation, the transient spikes due to high di/dt may overly stress the inputs to the LMG1025-Q1. A current-limiting, 100 Ω resistor can be placed right before the IN– input to limit excessive current spikes in the device.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

Typical Application (continued)

Secondly, for moderate ground-bounce cases, a simple R-C filter can be built with a simple resistor in series with the inputs. By utilizing the input capacitance of LMG1025-Q1, the resistor could be close to its input pin. The addition of a small capacitor on the input as supplement can also be helpful. A small time constant of the R-C filter can can enough to filter out high frequency noises. This solution is acceptable for moderate cases in applications where extra delay is acceptable and the pulse width is not extremely short such as 1ns range.

For more extreme cases, or where no delay is tolerable while pulse width is extremely short, using a commonmode choke provides the best results.

One example application where ground-bounce is particularly challenging is when using a current sense resistor. In configuration A LMG1025-Q1 ground is connected to the source of GaN FET, while the controller ground is connected to the other side of the current sense resistor as shown in Figure 4. Due to the fast switching and very fast current slew rates, the high ground potential bounce induced by inductance of the sense resistor can disrupt the operation of the circuit or even damage the part. To prevent this, a common-mode choke can be used for IN+ and IN–, respectively. Resistors can also added to the signal output line before LMG1025-Q1 depending on the input signal pulse width to provide additional RC filtering. Figure 6 presents the schematic using approach A with the preferred filtering method. Approach B as Figure 5 places the current sense resistor within the gate drive loop path. In this case, the LMG1025-Q1 GND pin is connected to the signal ground, and with good ground plane connection, the ground bounce issue can be less severe than approach A. However, the inductance of the current sense resistor adds common-source inductance to the gate drive loop. The voltage generated across this parasitic inductance will subtract from the gate-drive voltage of the FET, slowing down the turnon and turnoff di/dt of the FET, or even cause mis-turn on and off. Additional gate resistance will have to be added to ensure the loop is stable and ring-free. The slower rise may negate the advantage of the fast switching of the GaN FET and may cause additional losses in the circuit. Therefore, this approach is not recommended.

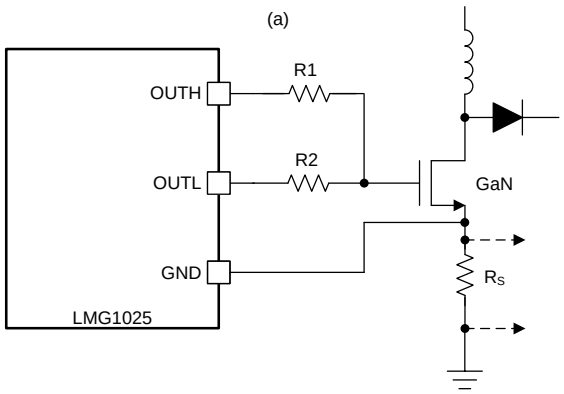


Figure 4. Source Resistor Current Sense A Configuration

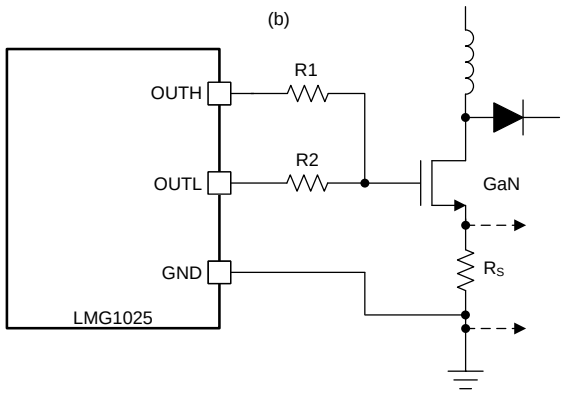


Figure 5. Source Resistor Current Sense B Configuration

ADVANCE INFORMATION

Typical Application (continued)

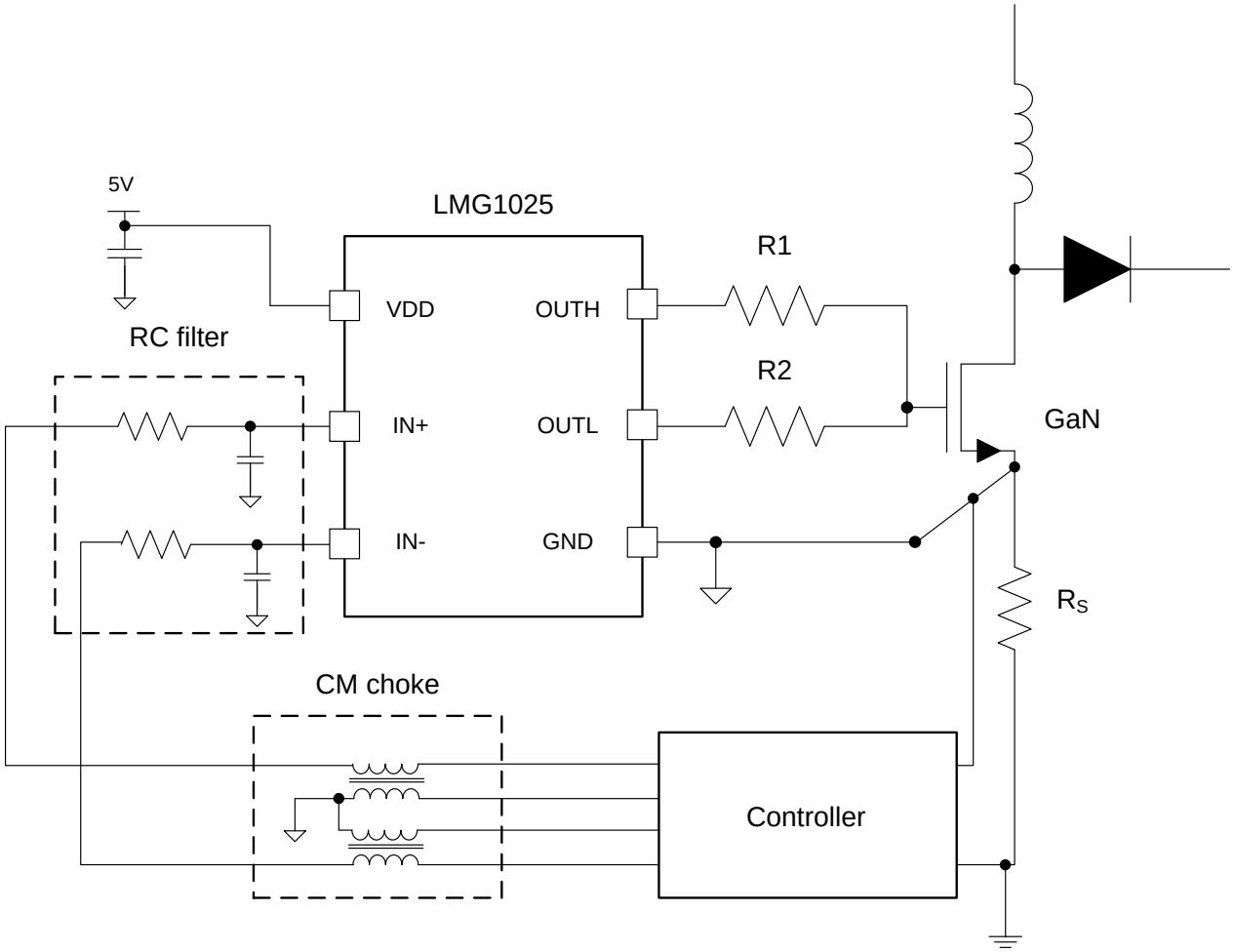


Figure 6. Filtering For Ground Bounce Noise Handling When Using LMG1025-Q1

8.2.3 VDD and Overshoot

Fast switching with high current is prone to ringing with parasitic inductances, including those on PCB traces. Overshoot associated with such ringing transients need to be evaluated and controlled as a part of the PCB design process to limit device stress. The parameters affecting stress are how high the overshoot is above the absolute maximum specification and the ratio of overshoot duration to the switching time period. Recommended design practice is to limit the overshoots to the absolute maximum pin voltages. This is accomplished with carful PCB layout to minimize parasitic inductances, choice of components with low ESL and addition of series resistance to limit rise times. For large overshoots, limiting the variability of the power supply may be required. For example, 0.5V of overshoot will be permissible with a maximum recommended supply of 5.25 V (5% variability); however, for larger overshoots, a supply with lower variability will be preferred.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

Typical Application (continued)

8.2.4 Operating at Higher Frequency

With fast rise/fall time, and capability of achieving 1 ns pulse width, depending on the capacitive load condition, the operating frequency of LMG1025-Q1 can be increased in a burst manner. In conditions which requires very high frequency pulsing, a pulse train with certain period of pause between each burst can be adopted to avoid overheat of the device. This will help maintain the RMS output current similar as lower frequency operation but boost the transient frequency to very high. In addition, higher decoupling capacitance will be needed to supply high frequency charging of the capacitive load.

8.2.5 Application Curves

Figure 7 and Figure 8

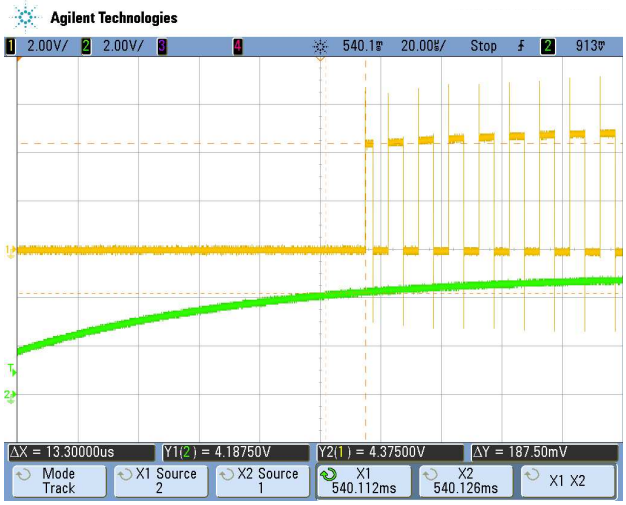


Figure 7. Startup Time



Figure 8. Shutdown Time

ADVANCE INFORMATION

9 Power Supply Recommendations

A low-ESR/ESL ceramic capacitor must be connected close to the IC, between VDD and GND pins to support the high peak current being drawn from VDD during turnon of the FETs. It is most desirable to place the VDD decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

TI recommends the use of a three-terminal capacitor connecting in shunt-through manner to achieve the lowest ESL and best transient performance. This capacitor can be placed as close as possible to the IC, while another capacitor in larger capacitance can be placed closely to the three-terminal cap to supply enough charge but with slightly lower bandwidth. As a general practice, the combination of a 0.1 µF of 0402 or feed-through capacitor (closest to LMG1025-Q1) and a 1 µF 0603 capacitor is recommended.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

The layout of the LMG1025-Q1 is critical to its performance and functionality. The LMG1025-Q1 is available in a 2x2 DSB QFN, which allows a low inductance connection to a FET. Figure 3 shows the recommended layout of the LMG1025-Q1 with a ball-grid GaN FET.

A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package are used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

10.1.1 Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with the LMG1025-Q1. The LMG1025-Q1 should be placed as close to the GaN FET as possible, with gate drive resistors R1 and R2 immediately connecting OUTH and OUTL to the FET gate. Large traces need to be used to minimize resistance and parasitic inductance.

To minimize gate drive loop inductance, the source return should be on layer 2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and the LMG1025-Q1 GND pin connect to this plane with minimal impedance. Finally, care must be taken to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

10.1.2 Bypass Capacitor

The VDD power terminal of the LMG1025-Q1 must by bypassed to ground immediately adjacent to the IC. Because of the fast gate drive of the IC, the placement and value of the bypass capacitor is critical. The bypass capacitor must be located on the top layer, as close as possible to the IC, and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1 µF, up to 1 µF, with temperature coeffient X7R or better. Recommended body types are LICC, IDC, Feed-though, and LGA. Finally, an additional 1µF capacitor (not shown in) should be located as close to the IC as practical.

10.2 Layout Example

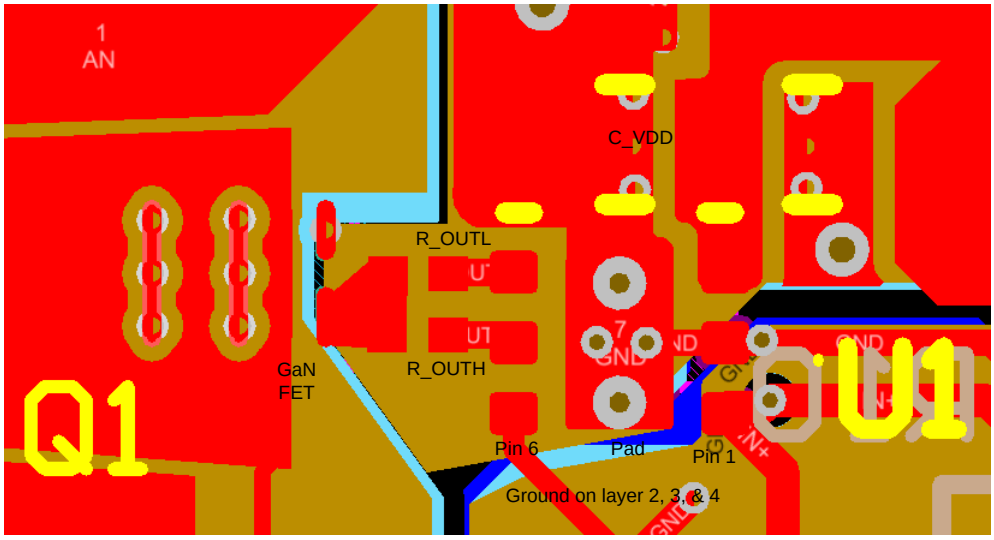


Figure 9. Typical LMG1025-Q1 Layout With Ball-Grid GaN FET

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

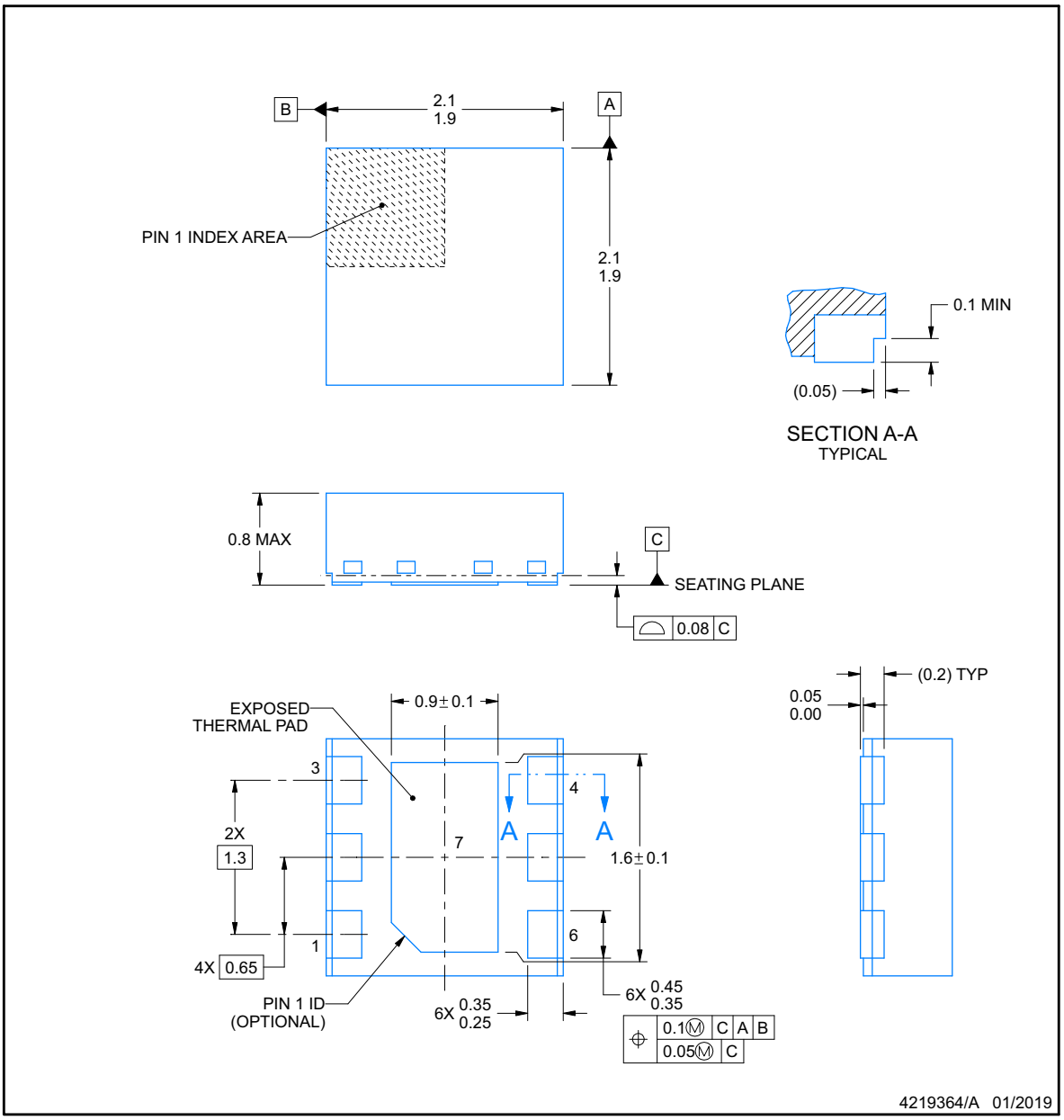
PACKAGE OUTLINE

DEE0006A



WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

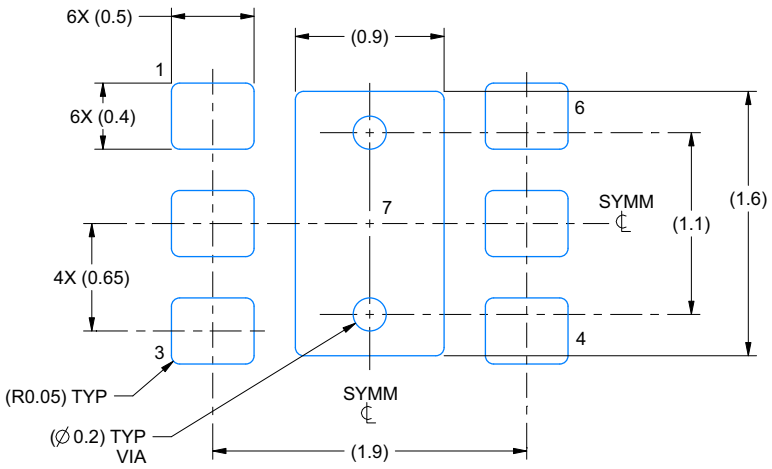
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

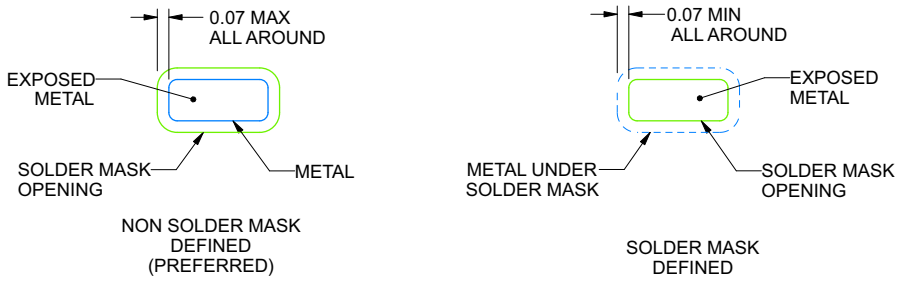
DEE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4219364/A 01/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

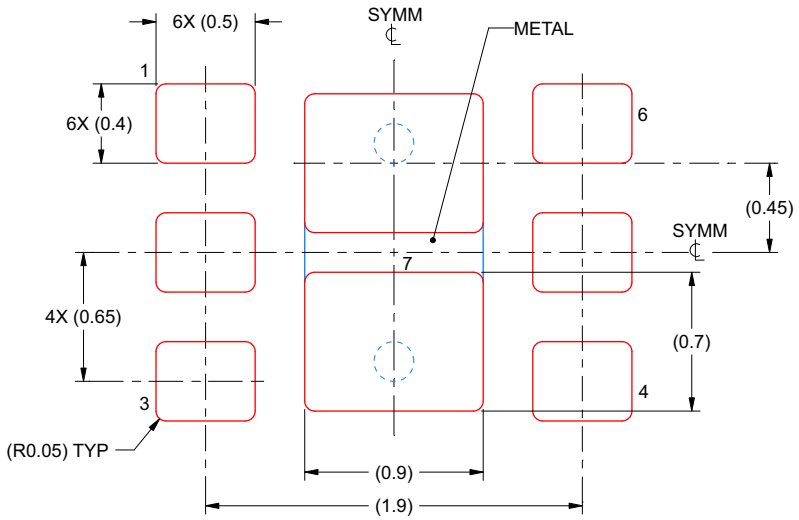
Copyright © 2019, Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

DEE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7:
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4219364/A 01/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

Copyright © 2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG1025QDEERQ1	PREVIEW	WSON	DEE	6	3000	TBD	Call TI	Call TI	-40 to 125		
LMG1025QDEETQ1	PREVIEW	WSON	DEE	6	250	TBD	Call TI	Call TI	-40 to 125		
PMG1025QDEETQ1	ACTIVE	WSON	DEE	6	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated