DRV2700 具有集成升压转换器的工业压电驱动器

1 特性

- 100V 升压或 1kV 反激配置
- 采用升压 + 放大器配置的 ±100V 压电驱动器
  - 4 种可通过 GPIO 调节的增益
  - 差分或单端输出
  - 低压控制
  - 交流和直流输出控制
- 采用反激配置的 0 至 1kV 压电驱动器
  - 低压控制
  - 交流和直流输出控制
- 集成升压或反激转换器
  - 可调节的电流限制
  - 集成功率场效应晶体管 (FET) 和二极管
- 快速启动时间：1.5ms
- 宽电源电压范围：3V 至 5.5V
- 4mm x 4mm 超薄四方扁平无引线 (VQFN) 封装
- 1.8V 兼容数字引脚
- 过热保护

2 应用

- 压电定位致动器
- 压电声响驱动器
- 压电喷墨打印机
- 压电传感器
- 压电微泵

3 说明

DRV2700 是一款单芯片压电驱动器，此驱动器具有集成的 105V 升压开关、集成型功率二极管以及集成的全差分放大器。 这款多用途器件能够驱动高压和低压压电负载。 输入信号既可以是差分信号，也可以是单端信号，而且交流或直流耦合均支持。 DRV2700 器件支持四种 GPIO 控制的增益：28.8dB、34.8dB、38.4dB 和 40.7dB。

升压电压通过两个外部电阻进行设置。 升压电流限值可通过 $R_{(REXT)}$ 电阻进行编程。 升压转换器架构可防止电源电流超出由 $R_{(REXT)}$ 电阻设置的限值，这样用户便可以根据目标性能需求针对给定电感来优化 DRV2700 电路。 此外，该升压转换器基于滞后架构，可最大程度降低开关损耗，从而提高效率。

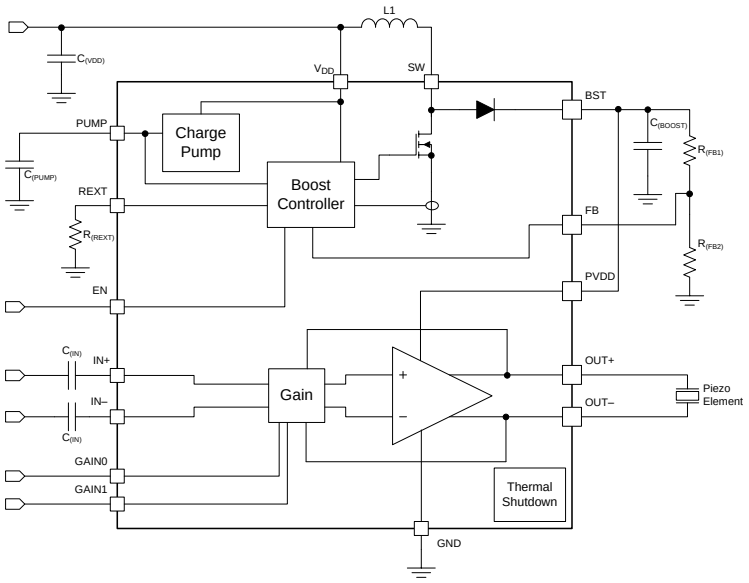
DRV2700 器件的启动时间典型值为 1.5ms，从退出休眠模式的速度方面来讲是一款理想的压电驱动器。 该器件具有热过载保护，可在过驱动时免遭损坏。

器件信息(1)

器件名称	封装	封装尺寸（标称值）
DRV2700	VQFN (20)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 升压 + 放大器配置



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5 修订历史记录

Changes from Revision A (March 2015) to Revision B **Page**

- Changed "minimum switching frequency" to "miminum startup switching frequency" in Switching Characteristics 5

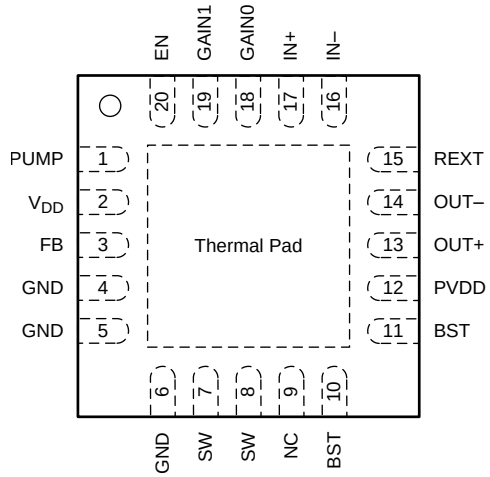
Changes from Original (March 2015) to Revision A **Page**

- 已发布完整版数据表 1

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6 Pin Configuration and Functions

RGP Package
20-Pin VQFN With Exposed Thermal Pad
Top View



NC – no internal connection

Pin Functions

PIN		TYPE (1)	CONNECTION IF UNUSED	DESCRIPTION
NAME	NO.			
BST	10	P	—	Boost output voltage
	11		—	
EN	20	I	—	Chip enable
FB	3	I	—	Boost feedback
GAIN0	18	I	GND	Gain programming pin — least significant bit (LSB)
GAIN1	19	I	GND	Gain programming pin — most significant bit (MSB)
GND	4	P	—	Ground
	5		—	
	6		—	
IN+	17	I	NC	Noninverting input
IN–	16	I	NC	Inverting input
NC	9	—	—	No connect
OUT+	13	O	NC	Noninverting output
OUT–	14	O	NC	Inverting output
PVDD	12	P	NC	Amplifier supply voltage
PUMP	1	P	—	Internal charge-pump voltage
REXT	15	I	—	Resistor to ground. This pin sets the boost current-limit.
SW	7	P	—	Internal-boost switch pin
	8		—	
V_{DD}	2	P	—	Power supply (connect to battery)

(1) I = Input, O = Output, I/O = Input and output, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	–0.3	6	V
Input voltage	IN+, IN–, EN, GAIN0, GAIN1, FB	–0.3	V_{DD} + 0.3	V
Boost/Output Voltage	PV_{DD}, SW, OUT+, OUT–		120	V
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			260	°C
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±1500	

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	V_{DD}	3		5.5	V
$V_{(BST)}$	Boost voltage	BST	15		105	V
V_{ID}	Differential input voltage	IN+, IN–		1.8(1)		V
V_{IL}	Digital input low voltage	EN, GAIN0, GAIN1; V_{DD} = 3.6 V			0.75	V
V_{IH}	Digital input high voltage	EN, GAIN0, GAIN1; V_{DD} = 3.6 V	1.4			V
$R_{(REXT)}$	Current-limit control resistor		6		35	kΩ
L	Inductance for boost converter		3.3			µH

(1) Gains are optimized for a 1.8-V peak input

7.4 Thermal Information

THERMAL METRIC(1)		RGP (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	8.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = 25°C, $V_{OUT(PP)}$ = V_{OUT+} – $V_{OUT–}$ = 200 V, $C_{(LOAD)}$ = 47 nF, $G_{(AMP)}$ = 40 dB, L = 4.7 µH (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|I_{IL}\|$	Digital-input low current	EN, GAIN0, GAIN1; V_{DD} = 3.6 V, V_I = 0 V			1	µA
$\|I_{IH}\|$	Digital-input high current	EN, GAIN0, GAIN1; V_{DD} = 3.6 V, V_I = V_{DD}			5	µA
$I_{L(sd)}$	Shutdown current	V_{DD} = 3.6 V, $V_{(EN)}$ = 0 V		13		µA
I_Q	Quiescent current	V_{DD} = 3.6 V, $V_{(EN)}$ = V_{DD}, $V_{(BST)}$ = 105 V, no signal		24		mA
		V_{DD} = 3.6 V, $V_{(EN)}$ = V_{DD}, $V_{(BST)}$ = 80 V, no signal		13		mA
		V_{DD} = 3.6 V, $V_{(EN)}$ = V_{DD}, $V_{(BST)}$ = 55 V, no signal		9		mA
		V_{DD} = 3.6 V, $V_{(EN)}$ = V_{DD}, $V_{(BST)}$ = 30 V, no signal		5		mA
V_{OS}	Offset voltage	V_{DD} = 3.6 V, $V_{(EN)}$ = 3.6 V		25		mV
CMVR	Common-mode voltage	V_{DD} = 3.6 V, $V_{(EN)}$ = 3.6 V	0.2		V_{DD} – 0.4	V
CMRR	Common-mode rejection ratio	V_{DD} = 3.6 V, $V_{(EN)}$ = 3.6 V		100		dB
PSRR	Power-supply rejection ratio	V_{DD} = 3.6 V, $V_{(EN)}$ = 3.6 V		60		dB
R_I	Input impedance	All gains, IN+, IN–		100		kΩ
$G_{(AMP)}$	Amplifier gain	GAIN[1:0] = 00		28.8		dB
		GAIN[1:0] = 01		34.8		
		GAIN[1:0] = 10		38.4		
		GAIN[1:0] = 11		40.7		
SR	Slew rate	GAIN[1:0] = 00, No Load		150		V/ms
		GAIN[1:0] = 01, No Load		300		
		GAIN[1:0] = 10, No Load		450		
		GAIN[1:0] = 11, No Load		600		
BW	Amplifier bandwidth	GAIN[1:0] = 00, $V_{OUT(PP)}$ = 50 V, No Load		20		kHz
		GAIN[1:0] = 01, $V_{OUT(PP)}$ = 100 V, No Load		10		
		GAIN[1:0] = 10, $V_{OUT(PP)}$ = 150 V, No Load		7.5		
		GAIN[1:0] = 11, $V_{OUT(PP)}$ = 200 V, No Load		5		
GBW	Gain-bandwidth product	V_{DD} = 3.6 V, $V_{(EN)}$ = 3.6 V		550		kHz
V_n	Input Voltage Noise	V_{DD} = 3.6 V, $V_{(EN)}$ = 3.6 V		6.5		µV/√Hz
THD+N	Total harmonic distortion plus noise	f = 300 Hz, $V_{OUT(PP)}$ = 200 V		1%		

7.6 Switching Characteristics

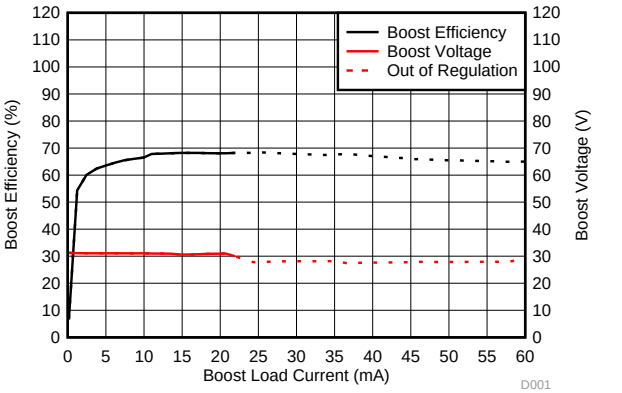
V_{DD} = 3.6 V, T_A = 25°C, $V_{OUT(PP)}$ = V_{OUT+} – $V_{OUT–}$ = 200 V, $C_{(LOAD)}$ = 47 nF, $G_{(AMP)}$ = 40 dB, L = 4.7 µH (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(start)}$	Startup time—time from EN high until boost and amplifier are fully enabled			1.5		ms
f_{MIN}	Minimum startup switching frequency			39		kHz

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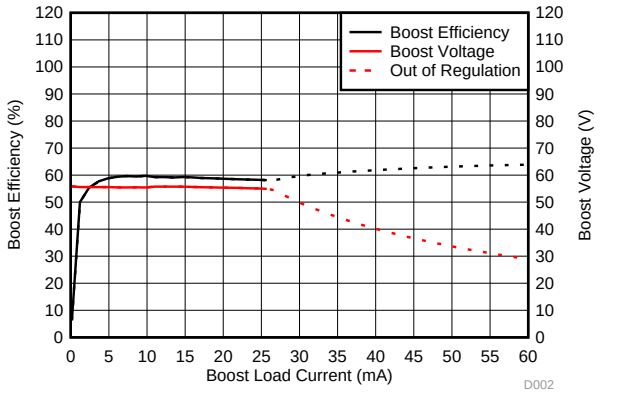
7.7 Typical characteristics

V_{DD} = 3.6 V, $R_{(REXT)}$ = 7.5 kΩ, L = 4.7 µH, differential input, 100-nF DC blocking capacitors on IN±



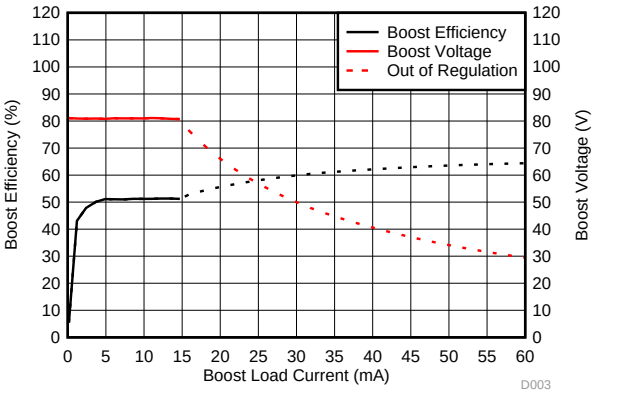
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 30 V
G = 28.8 dB

Figure 1. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 30 V



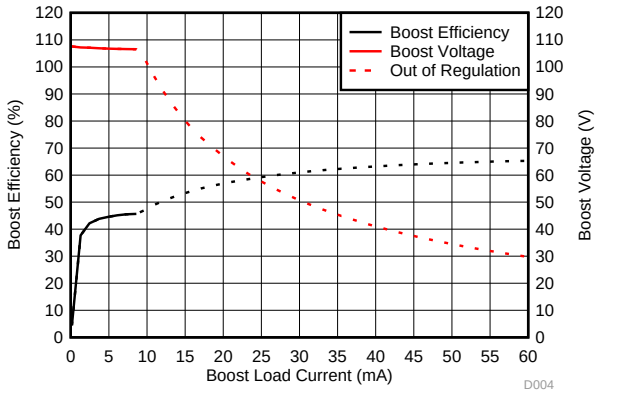
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 55 V
G = 34.8 dB

Figure 2. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 55 V



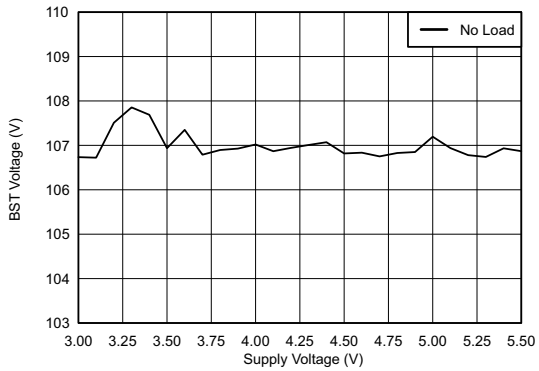
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 80 V
G = 38.4 dB

Figure 3. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 80 V



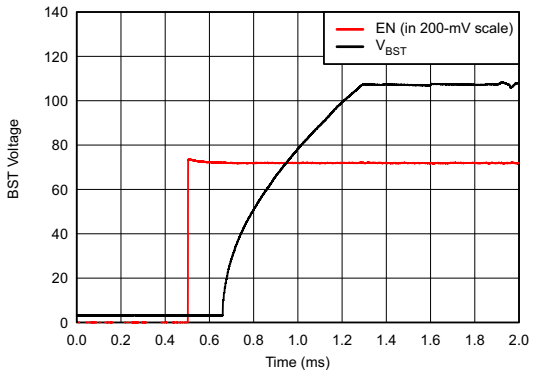
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 40.7 dB

Figure 4. Load Current vs Boost Efficiency (%) and Voltage (V) at V_{PVDD} = 105 V



G = 40.7 dB $C_{(LOAD)}$ = Open V_{PVDD} = 105 V

Figure 5. Line Regulation at PVDD = 105 V



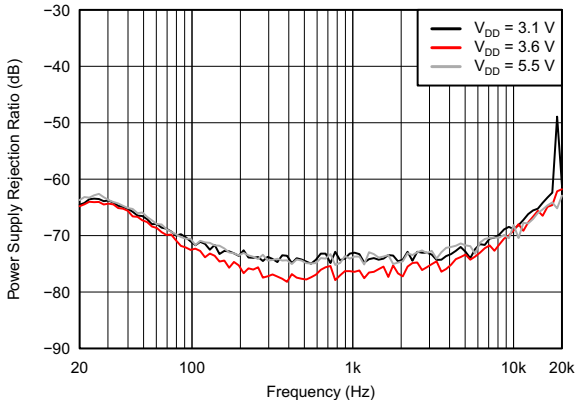
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 40.7 dB

Figure 6. Boost Voltage Startup

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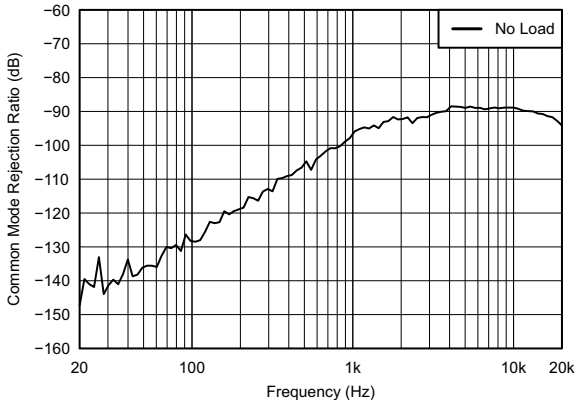
Typical characteristics (continued)

V_{DD} = 3.6 V, $R_{(REXT)}$ = 7.5 kΩ, L = 4.7 µH, differential input, 100-nF DC blocking capacitors on IN±



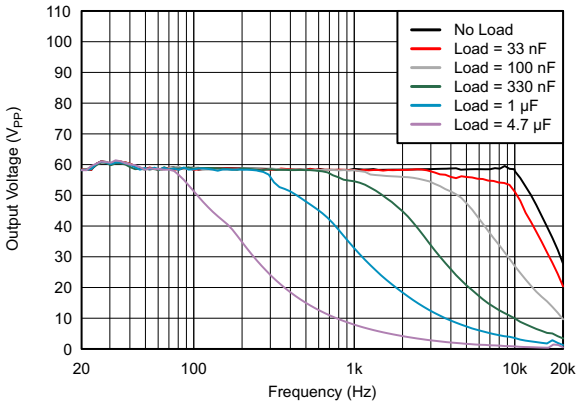
G = 40.7 dB $C_{(LOAD)}$ = Open V_{PVDD} = 105 V

Figure 7. AC PSRR at V_{PVDD} = 105 V



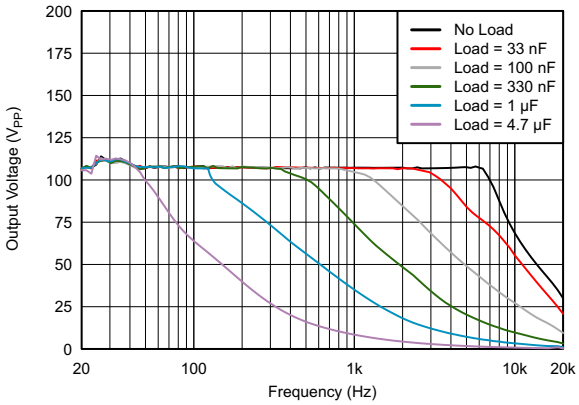
G = 40.7 dB $C_{(LOAD)}$ = Open V_{PVDD} = 105 V

Figure 8. AC CMRR at V_{PVDD} = 105 V



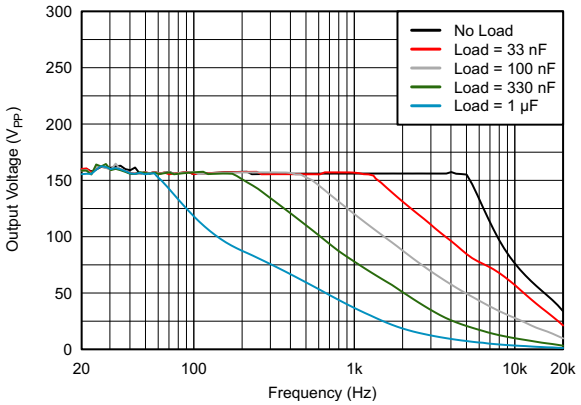
V_{DD} = 3.6 V G = 28.8 dB V_{PVDD} = 30 V

Figure 9. Gain Bandwidth at V_{PVDD} = 30 V



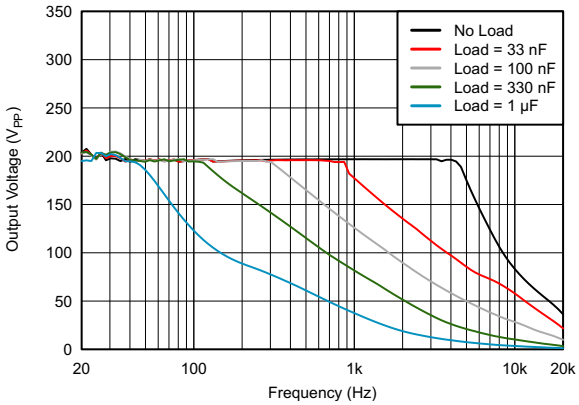
V_{DD} = 3.6 V G = 34.8 dB V_{PVDD} = 55 V

Figure 10. Gain Bandwidth at V_{PVDD} = 55 V



V_{DD} = 3.6 V G = 38.4 dB V_{PVDD} = 80 V

Figure 11. Gain Bandwidth at V_{PVDD} = 80 V



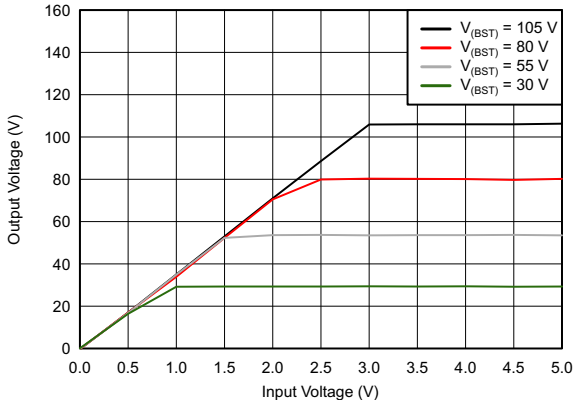
V_{DD} = 3.6 V G = 40.7 dB V_{PVDD} = 105 V

Figure 12. Gain Bandwidth at V_{PVDD} = 105 V

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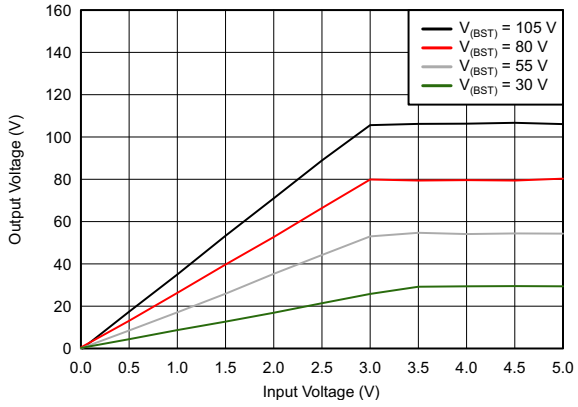
Typical characteristics (continued)

V_{DD} = 3.6 V, $R_{(REXT)}$ = 7.5 kΩ, L = 4.7 µH, differential input, 100-nF DC blocking capacitors on IN±



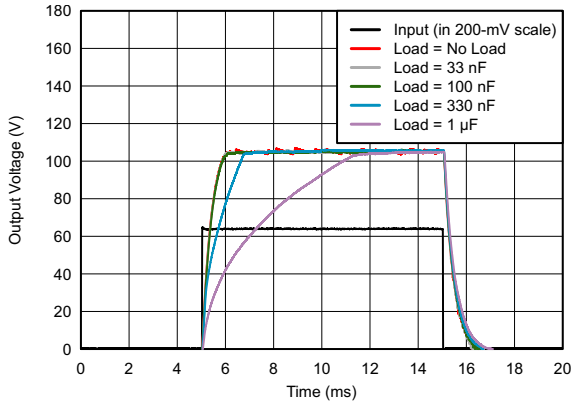
V_{DD} = 3.6 V G = 40.7 dB $C_{(LOAD)}$ = Open

Figure 13. Output Linearity



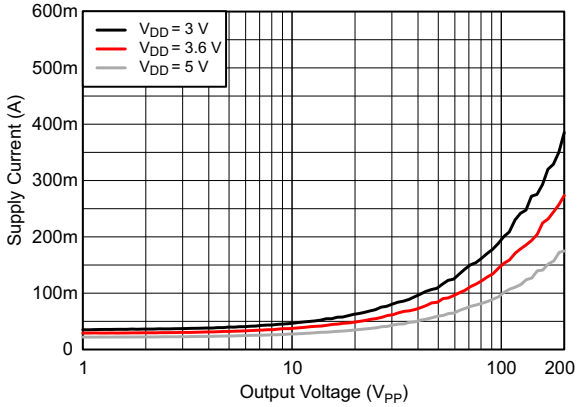
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open
G = 28.8 dB at V_{PVDD} = 30 V G = 34.8 dB at V_{PVDD} = 55 V
G = 38.4 dB at V_{PVDD} = 80 V G = 40.7 dB at V_{PVDD} = 105 V

Figure 14. Output Linearity with Different Gains



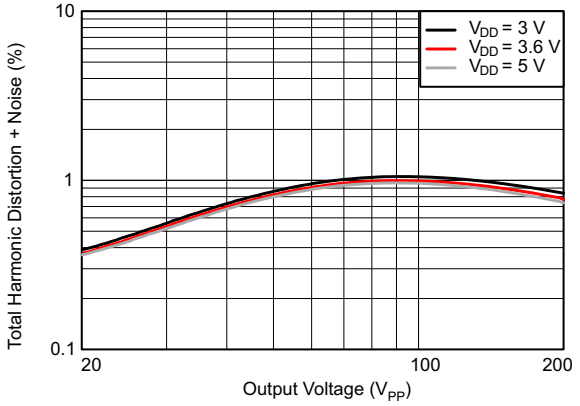
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 40.7 dB

Figure 15. Output Slew Rate



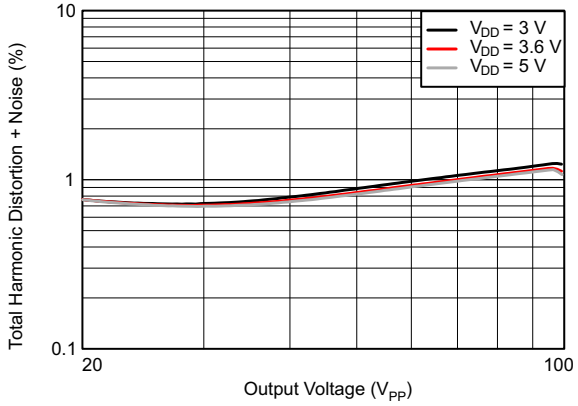
f = 200 Hz $C_{(LOAD)}$ = 47 nF V_{PVDD} = 105 V
G = 40 dB

Figure 16. Supply Current vs Output Voltage



f = 200 Hz $C_{(LOAD)}$ = 47 nF V_{PVDD} = 105 V
G = 40 dB

Figure 17. Total Harmonic Distortion + Noise vs Output Voltage



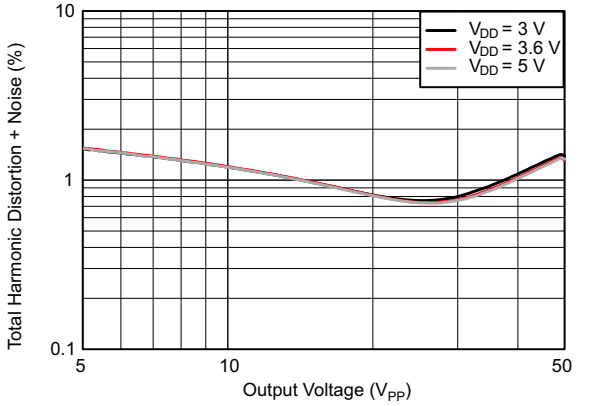
f = 200 Hz $C_{(LOAD)}$ = 330 nF V_{PVDD} = 55 V
G = 34 dB

Figure 18. Total Harmonic Distortion + Noise vs Output Voltage

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Typical characteristics (continued)

V_{DD} = 3.6 V, $R_{(REXT)}$ = 7.5 kΩ, L = 4.7 µH, differential input, 100-nF DC blocking capacitors on IN±



f = 200 Hz $C_{(LOAD)}$ = 680 nF V_{PVDD} = 30 V
G = 28 dB

Figure 19. Total Harmonic Distortion + Noise vs Output Voltage

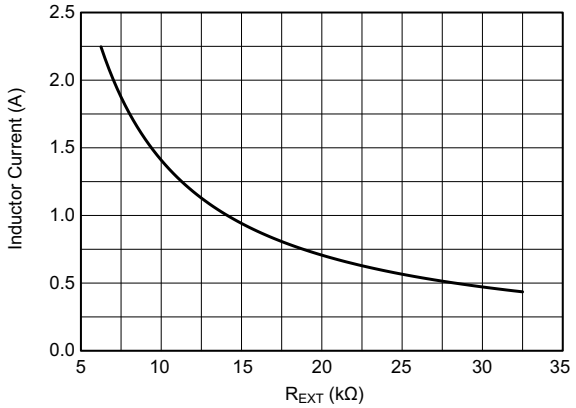
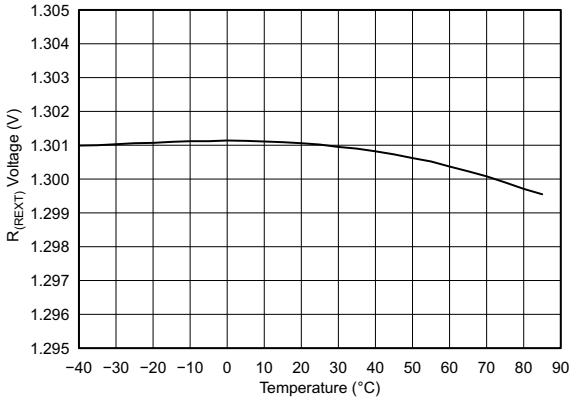


Figure 20. Inductor Current vs $R_{(REXT)}$



V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 40.7 dB

Figure 21. $R_{(REXT)}$ Voltage vs Temperature

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8 Detailed Description

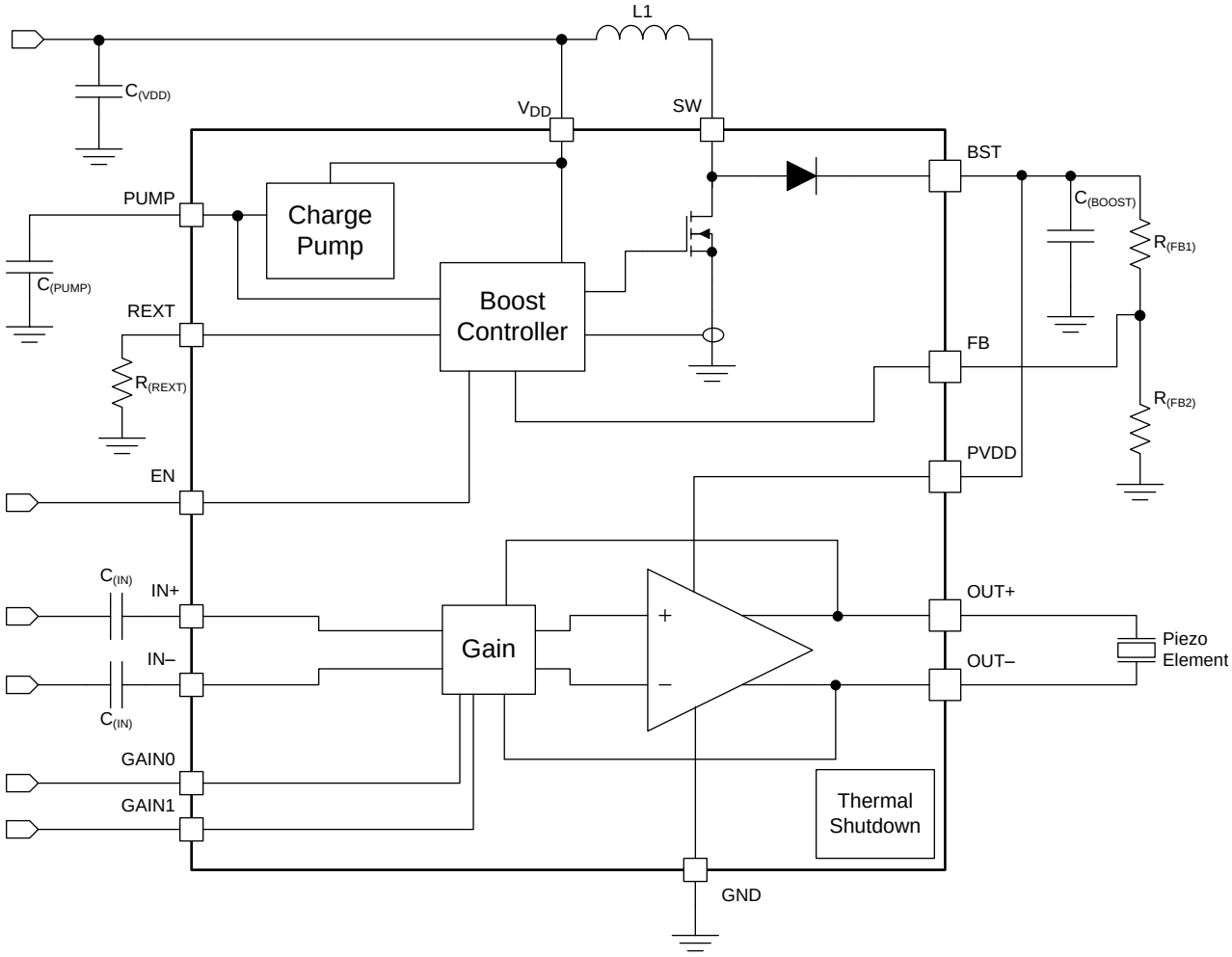
8.1 Overview

The DRV2700 device is a single-chip piezo driver with an integrated 105-V boost switch, integrated power diode, and integrated fully-differential amplifier. This versatile device is capable of driving both high-voltage and low-voltage piezo loads. The input signal can be either differential or single-ended. The DRV2700 device supports four GPIO-controlled gains: 28.8 dB, 34.8 dB, 38.4 dB, and 40.7 dB.

The boost voltage is set using two external resistors. The boost current-limit is programmable through the $R_{(REXT)}$ resistor. The boost converter architecture does not allow the demand on the supply current to exceed the limit set by the $R_{(REXT)}$ resistor; therefore, allowing the user to optimize the DRV2700 circuit for a given inductor based on the desired performance requirements. Additionally, this boost converter is based on a hysteretic architecture to minimize switching losses and therefore increase efficiency.

A typical start-up time of 1.5 ms makes the DRV2700 device an ideal piezo driver for fast responses. Thermal overload protection prevents the device from damage when overdriven.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Boost Converter and Control Loop

The DRV2700 device creates a boosted supply rail with an integrated DC-DC converter that can go up to 105 V. The switch-mode power supplies have a few different sources of losses. When boosting to very high voltages, the efficiency begins to degrade because of these losses. The DRV2700 device has a hysteretic boost design to minimize switching losses and therefore increase efficiency. A hysteretic controller is a self-oscillation circuit that regulates the output voltage by keeping the output voltage within a hysteresis window set by a reference voltage regulator and, in this case, the current-limit comparator. Hysteretic converters typically have a larger ripple as a trade off because of the minimized switching. This ripple may vary depending on the output capacitor and load. The power FET and power diode of the boost converter are both integrated within the device to provide the required switching while minimizing external components. Additionally, the boost voltage output (BST) can be easily fed into the high-voltage amplifier through the adjacent pin (PVDD) to help minimize routing inductance and resistance on the board.

8.3.2 High-Voltage Amplifier

When using the high-voltage amplifier in conjunction with the boost converter, the PVDD pin is located next to the BST pin to immediately feed the high voltage signal back into the device to power the amplifier. The DRV2700 device was designed as a differential amplifier. A major benefit of the fully differential amplifier is the improved common-mode rejection ratio (CMRR) over single-ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity-to-ground offset that is related noise injection which is important in low-noise systems.

The high-voltage amplifier can be used in a single-ended DC input configuration to provide a DC output on the OUT+ and OUT– pins. The amplifier is very linear across the full voltage range and by using a DAC (digital-to-analog converter) input, the output can be controlled with very good granularity.

Precautions must be taken into thermal concerns of this amplifier because high frequencies, voltage, and capacitive load combinations can overheat the device. See the *Piezo Load Selection* section for a general guideline.

8.3.3 Fast Start-Up (Enable Pin)

The DRV2700 device features a fast startup time, which is beneficial for the device come out of shutdown very quickly. When the EN pin transitions from low to high, the boost supply is turned on, the input capacitor is precharged to V_{DD} / 2, and the amplifier is enabled in a 1.5 ms (typical) total start-up time.

When AC coupled with larger input capacitors, the input can require additional time to charge up to V_{DD} / 2. Because the charging current on the input capacitors are not ensured to be exactly the same, a non-zero differential value can exist during startup. Although this differential output voltage (voltage pop) during startup is not specified, it should be fairly small and not exceed 2 V.

8.3.4 Gain Control

The DRV2700 device has programmable gains through the GAIN[1:0] bits. Table 2 lists the gain from IN+ or IN– to OUT+ or OUT–.

Table 1. Programmable Gains

GAIN1	GAIN0	GAIN (dB)
0	0	28.8
0	1	34.8
1	0	38.4
1	1	40.7

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The gains are optimized to achieve approximately 50 V_{PP}, 100 V_{PP}, 150 V_{PP}, or 200 V_{PP} at the output without clipping from a 1.8-V peak source of a single-ended input signal.

8.3.5 Adjustable Boost Voltage

The output voltage of the integrated boost converter is adjusted by a resistive feedback divider between the boost output voltage (BST) and the feedback pin (FB). The boost voltage should be programmed to a value greater than the maximum peak signal voltage that the user expects to create with the DRV2700 amplifier. Lower boost voltages achieve better system efficiency and therefore should be used when lower amplitude signals are applied. The minimum boost voltage that is required should be used to save on not only power but also heat dissipation. The maximum allowed boost voltage is 105 V.

8.3.6 Adjustable Boost Current-Limit

The current-limit of the boost switch is adjusted through a resistor to ground placed on the REXT pin. In order to protect the device, the REXT pin value should remain between 7.5 kΩ and 32.5 kΩ as shown in Figure 20. To avoid damage to both the inductor and the DRV2700 device, the programmed current-limit must be less than the rated saturation limit of the inductor selected by the user. If the combination of the programmed limit and inductor saturation is not high enough, then the output current of the boost converter is not high enough to regulate the boost output voltage under heavy load conditions. This lower output current causes the boosted rail to sag which can possibly cause distortion of the output waveform.

8.3.7 Internal Charge Pump

The DRV2700 device has an integrated charge pump to provide gate drive for internal nodes. The output of this charge pump is placed on the VPUMP pin. An X5R or X7R storage capacitor with a value of 0.1 µF and a voltage rating of 10 V or greater must be placed at this pin for proper operation. This pin and voltage should not be used as an external reference or driver.

8.3.8 Thermal Shutdown

The DRV2700 device contains an internal temperature sensor that shuts down both the boost converter and the amplifier when the temperature threshold is exceeded. When the die temperature falls below the threshold, the device restarts operation automatically as long as the EN pin is high. Continuous operation of the DRV2700 device can cause the device to heat up if proper precautions and operating ranges are not followed. The thermal shutdown function protects the DRV2700 device from damage when overdriven, but usage models which drive the DRV2700 device into thermal shutdown should always be avoided.

8.4 Device Functional Modes

Although a high-voltage amplifier can be used in a number of ways, the DRV2700 device was intended for two main configurations which are boost + amplifier mode and flyback mode.

8.4.1 Boost + Amplifier Mode

In the boost + amplifier mode configuration, the boost converter is used in a boost configuration with a single inductor. The boost output (BST) is then fed into the high-voltage amplifier (PVDD) to drive the outputs. This configuration supports the boost converter up to 100 V_P and the amplifier to drive 200 V_{PP} or 0 to 100 V_P. The *Typical Applications* section describes the various implementations of this mode.

8.4.2 Flyback Mode

In the flyback mode configuration, the boost converter is used in a flyback configuration which allows the boost converter to drive the output to even higher voltages. For example, with a 1:10 turn ratio of the transformer, the transformer can turn the 100 V on the SW node into 1 kV on the high-voltage output. Figure 37 shows a basic circuit diagram.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV2700 is intended to drive piezo loads. This includes: capacitive loads, piezo sounders, piezo valves, piezo positioning actuators, piezo micropumps, piezo polymers and more.

9.2 Typical Applications

9.2.1 AC-Coupled DAC Input Application

The AC-coupled DAC input circuit shown in Figure 22 is typically used in piezo speaker applications. AC-coupling the DRV2700 device allows the device to only amplify the differential portions of the input which minimizes the common-mode amplification. Because a digitized AC signal is provided from an external source, such as a microcontroller, an input filter is not required. However, a low-pass filter can be added to minimize the harmonics of the digitized waveform.

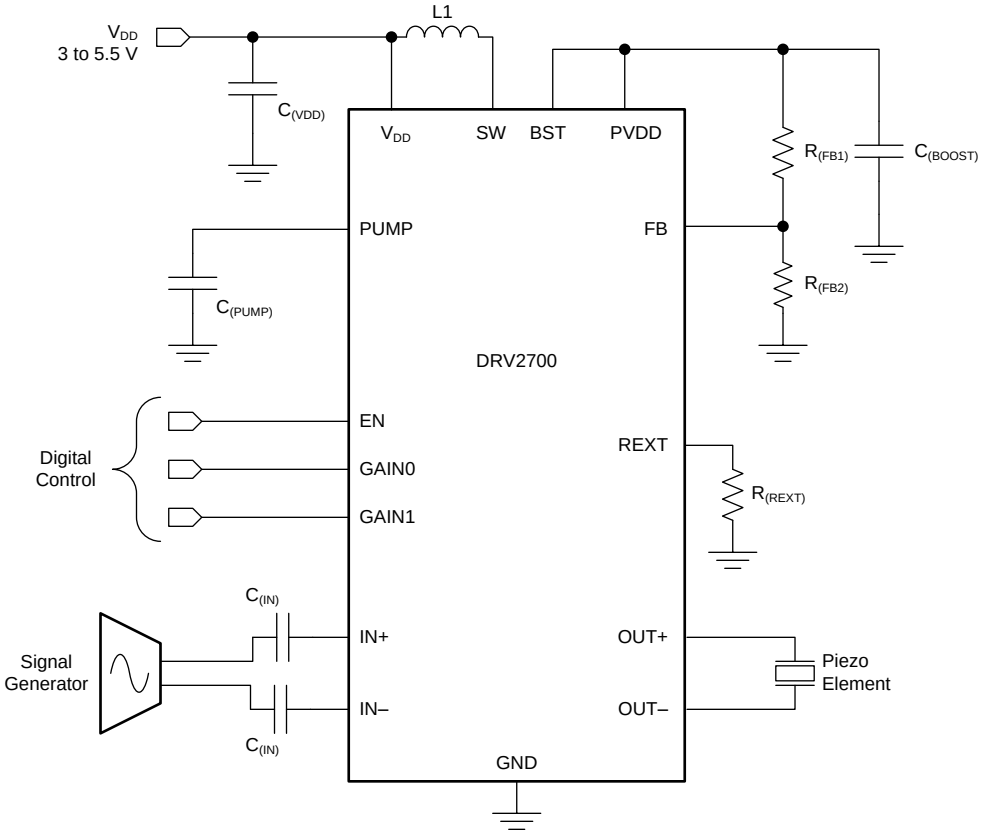


Figure 22. AC-Coupled DAC Input

Typical Applications (continued)

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE	CONSTRAINT
Input voltage	5 V	Power source
Output voltage	±60 V	Piezo load
Maximum output frequency	2 kHz	Application

9.2.1.2 Detailed Design Procedure

To design the entire system follow the design procedure listed in the following sections.

9.2.1.2.1 Piezo Load Selection

Several key specifications must be considered when selecting a piezo actuator such as dimensions, blocking force, and displacement. However, the key electrical specifications from the driver perspective are voltage rating and capacitance. The DRV2700 device operating in boost + amplifier mode can drive a variety of capacitances, frequencies, and voltages. However to extend the range in one specification can decrease the range of another specification. For example, if driving audio tones around 1 kHz, a lower capacitance piezo or lower driving voltage may be required. Figure 23 shows a general guide to selecting the proper parameters.

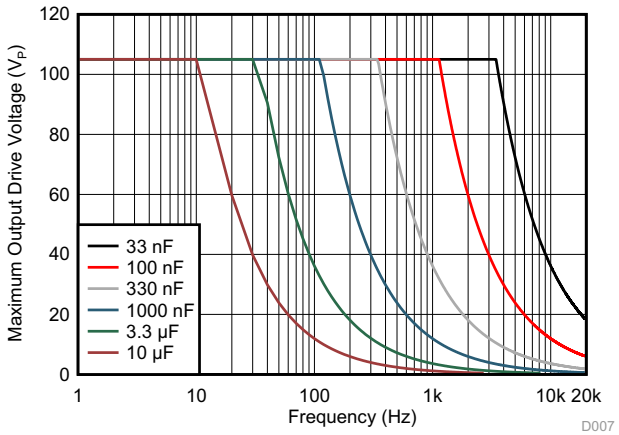


Figure 23. Maximum Frequency versus Maximum Voltage for Different Load Capacitances

Based on the design example, if the output voltage must be ±60 V_{OUT} to 2 kHz, then the piezo capacitance must be less than 100 nF. For ease of calculation, use a piezo load capacitance of 25 nF.

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9.2.1.2.2 Programming The Boost Voltage

The boost or flyback output voltage is programmed by an external network as shown in Figure 24.

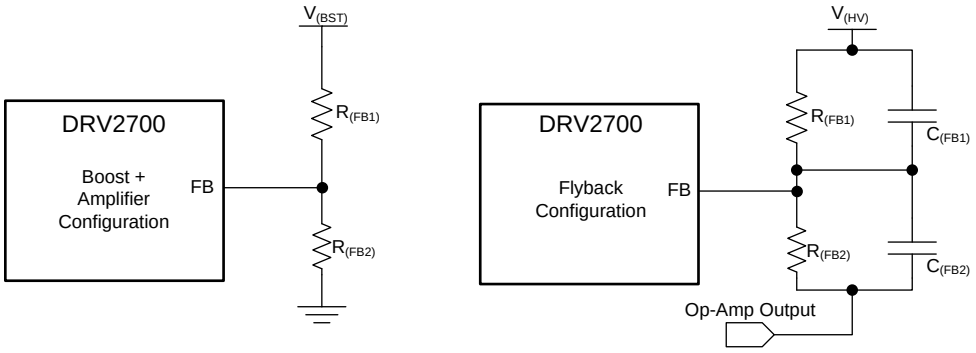


Figure 24. External Network

Depending on which configuration or mode is used in the system, use Equation 1 to calculate the output voltage.

$$V_{BST} = V_{FB}\left(1+\frac{R_{(FB1)}}{R_{(FB2)}}\right) \quad \text{Boost + Amplifier Configuration}$$

$$V_{HV} = V_{FB}\left(1+\frac{R_{(FB1)}}{R_{(FB2)}}\right)-\left(\frac{R_{(FB1)}}{R_{(FB2)}}\right)V_{OP} \quad \text{Flyback Configuration}$$

where

- V_{FB} = 1.30 V
- V_{OP} = V_{OL} of the operational amplifier (op amp). Typically this can be approximated to 0 V. (1)

The BST pin should be programmed to a value 5-V greater than the largest peak voltage in the system expected to allow adequate amplifier headroom. Because the programming range for the boost voltage extends to 105 V, the leakage current through the resistor divider becomes significant. TI recommends that the sum of the resistance of $R_{(FB1)}$ and $R_{(FB2)}$ be greater than 500 kΩ.

The flyback mode configuration may require filtering capacitors to go along with the feedback network to increase the performance at low and high frequencies. Because the charge storage is inversely proportional to the capacitance, use Equation 2 to calculate the values of the capacitors. In general, select a value of 22 pF for $C_{(FB1)}$.

For this design example, because the value of V_{PP} must be negative, the boost + amplifier configuration must be used. Additionally, because the value of V_{BST} must be 5 V more than V_P, V_{BST} is set to 65 V. Using Equation 1, the feedback resistors can be found such that R_{FB1} = 49 × R_{FB2}. Because the total resistance must be greater than 500 kΩ, R_{FB1}= 735 kΩ and R_{FB2}= 15 kΩ.

$$\frac{R_{(FB1)}}{R_{(FB2)}} = \frac{C_{(FB2)}}{C_{(FB1)}} \quad (2)$$

NOTE

When resistor values greater than 1 MΩ are used, PCB contamination causes boost voltage inaccuracy. Use caution when soldering large resistences, and clean the area when finished for best results.

9.2.1.2.3 Inductor and Transformer Selection

Inductor selection plays a critical role in the performance of the DRV2700 device. The range of recommended inductances is from 3.3 to 22 µH. In general, higher inductances within a given manufacturer's inductor series have lower saturation current-limits and lower inductances have higher saturation current-limits. When a larger inductance is selected, the DRV2700 boost converter automatically runs at a lower switching frequency and incurs less switching losses. However, larger values of inductance may have higher ESR which increases the parasitic inductor losses. Because lower values of inductance generally have higher saturation currents, inductors with a lower value are a better choice when attempting to maximize the output current of the boost converter.

Another factor to consider for transformers is the winding ratio. In general, if a 200-V output is desired then, because the SW node can boost up to 100 V, a transformer of 1:2 (100 V:200 V) is the minimum required winding. However, selecting a slightly higher winding ratio to ensure that the 100 V on the primary side is not surpassed while trying to boost up to the desired voltage is good design practice.

For this design example, select an inductor of 3.3 µH with a saturation current of 1.5 A.

9.2.1.2.4 Programing the Boost and Flyback Current-Limit

The peak current drawn from the supply through the inductor is set solely by the $R_{(REXT)}$ resistor. This peak current-limit is independent of the selected inductance value, but the inductor is capable of handling this programmed limit. Use Equation 3 to calculate the relationship between $R_{(REXT)}$ and $I_{(LIM)}$.

$$R_{(REXT)} = \left(K \frac{V_{ref}}{I_{(LIM)}} \right) - R_{(INT)} \quad (3)$$

where

- K = 10 500
- V_{ref} = 1.35 V
- $I_{(LIM)}$ is the desired peak current-limit through the inductor or transformer
- $R_{(INT)}$ = 60 Ω

For this design example, because the saturation current is 1.5 A, select 1 A for the $I_{(LIM)}$ value. Using Equation 3, the value of $R_{(EXT)}$ is approximately 14 kΩ.

9.2.1.2.5 Boost Capacitor Selection

The boost output voltage is programmable as high as 105 V. A capacitor with a voltage rating of at least the boost output voltage must be selected. Because ceramic capacitors come in ratings of 100 V or 250 V, a 250-V rated 100-nF capacitor of the X5R or X7R type is recommended for the 105-V case. The selected capacitor should have a minimum working capacitance of at least 50 nF. If a smaller ripple on this node is required, then a larger capacitor should be selected. If using a differential output in the boost + amplifier configuration, then the ripple is canceled because it is prevelant on both the OUT+ and OUT– pins.

For this design example, a 100-nF capacitor was used.

9.2.1.2.6 Pulldown FET and Resistors

The pulldown FET and resistor are used to help speed up the drain the charge on the high-voltage output. Because the FET must be driven from a comparator, an NMOS FET must be used. During normal operation, the V_{DS} of the NMOS is subject to a any value from approximately 0 V when the FET is on, to the output on the flyback configuration ($V_{(HV)}$) when the FET is off. Therefore, selecting a FET with a V_{DS} breakdown higher than the maximum V_{HV} is required. Additionally, placing a resistor in series with this FET (on the drain side) to limit the current going through the FET is required. This resistor can be sized according to the maximum current allowed per the data sheet of the FET. As an additional measure, a resistor can be placed on the source side to protect the pulldown FET, such that when current flows through the resistor, it raises the source voltage and thereby lowers the V_{GS} and shuts the FET off.

Because this design example is using the boost + amplifier configuration, the pulldown FET and resistors are not required.

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9.2.1.2.7 Low-Voltage Operation

The lowest gain setting is optimized for 50 V_{PP} with a boost voltage of 30 V. Some applications may not require 50 V_{PP}, therefore the designer may choose to program the boost converter as low as 15 V to improve efficiency. When using boost voltages lower than 30 V, consider using a boost capacitor and adjusting the full-scale input range First, to reduce boost ripple to an acceptable level, a 50-V rated, 0.22-µF boost capacitor is recommended. Second, the full-scale input range may require adjustment to avoid clipping. Generally, a 1.8-V single-ended PWM signal provides 50 V_{PP} at the lowest gain. For example, if the boost voltage is set to 25 V for a 40 V_{PP} full-scale output signal, the full-scale input range drops to 1.44 V for single-ended PWM inputs. An input voltage divider may be desired in this case if a 1.8-V I/O is used as a PWM source.

9.2.1.2.8 Current Consumption Calculation

Understanding how the voltage driven onto a piezo actuator relates to the current consumption from the power supply is useful. Modeling a piezo element as a pure capacitor is reasonably accurate. Use Equation 4 to calculate the current through a capacitor for an applied sinusoid.

$$I_{Capacitor(Peak)} = 2\pi \times f \times C \times V_P \quad (4)$$

- f is the frequency of the sinusoid in hertz
- C is the capacitance of the piezo load in farads
- V_P is the peak voltage

At the power supply, the actuator current is multiplied by the boost-supply ratio and divided by the efficiency of the boost converter as shown in Equation 5.

$$I_{DD(Peak)} = 2\pi \times f \times C \times V_P \times \frac{V_{Boost}}{V_{DD} \times \mu_{Boost}} \quad (5)$$

Substituting the design example values for the variables into Equation 5 and using a boost efficiency of 60%, yields a typical peak current from the power supply of 408 mA as shown in Equation 6.

$$I_{DD(Peak)} = 2\pi \times 2\ kHz \times 25\ nF \times 60\ V \times \frac{65\ V}{5\ V \times 0.6} = 408\ mA \quad (6)$$

9.2.1.2.9 Input Filter Considerations

Depending on the quality of the source signal provided to the DRV2700 device, an input filter may be required. Some key factors to consider are whether the source is generated from a DAC or from PWM, and the out-of-band content generated. If proper anti-image rejection filtering is used to eliminate image components, the filter can possibly be eliminated depending on the magnitude of the out-of-band components. If PWM is used, at least a first-order RC filter is required. The PWM sample rate must be greater than 30 kHz to keep the PWM ripple from reaching the piezo element and dissipating unnecessary power. A second-order RC filter may be desirable to further eliminate out-of-band signal content to further drive down power dissipation and eliminate audible noise.

For this design example, to ensure higher harmonics of the input signal do not propagate into the device, use a low pass filter with a 3-dB point of 2 kHz. Refer to *DRV2700EVM High Voltage Piezo Driver Evaluation Kit*, SLOU403, to build this input filter network.

9.2.1.2.10 Output Limiting Factors

Because of the small size of the DRV2700 device, limiting factors must be considered. In each of the applications, four factors can affect the output. These factors include the following:

- Bandwidth of the amplifier
- Limited current
- Slew rate
- Thermal shutdown

Although some of these factors can appear at the same time, each of these factors are shown in the following figures to help the designer differentiate between each factor.

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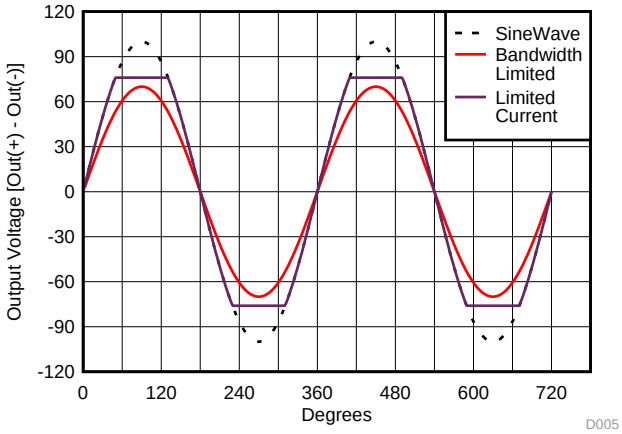


Figure 25. Bandwidth and Limited Current

The internal amplifier has an inherent bandwidth limitation on the order of 5 to 20 kHz depending on the gain settings. Although, this bandwidth limitation occurs primarily with a no-load condition or under a very small voltage swing, the output is essentially unable to drive to the expected output voltage because of a drop in the gain at that bandwidth. The internal boost converter can only support a limited amount of current. If for instance, the load was somewhat resistive as opposed to only capacitive, a situation could occur where the load requires additional current to pull the voltage up, however the boost converter cannot support it. This situation appears to be an out-of-regulation output voltage.

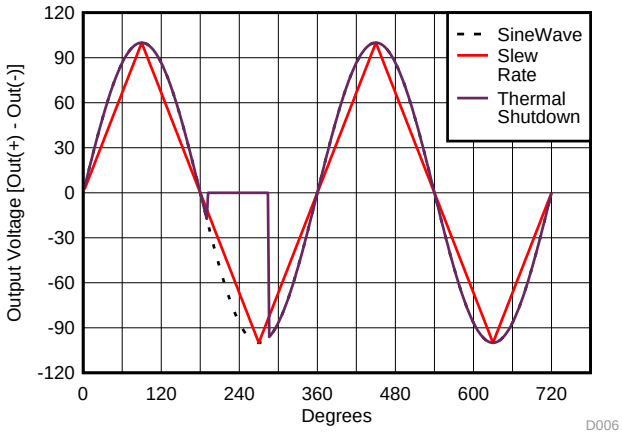


Figure 26. Slew Rate and Thermal Shutdown

As the output frequency increases, the slew rate increases. Because the boost converter can only support a certain amount of current based on the load capacitance, the sine wave begins to turn into more of a triangle wave.

Lastly, the device has a thermal shutdown feature for protection from damaging when the device begins to heat up because of power dissipation. When a load is primarily capacitance, the current leads the voltage (leading power factor). With a leading or lagging power factor, the maximum power does not occur at the maximum voltage or current. However the maximum power does occur at the phase crossing of these. This occurrence looks similar to the waveform in Figure 26, such that the output goes to 0 V and then start back up after it has cooled down below the internal threshold. Figure 23 shows a general guideline to staying below the maximum voltage and frequency based on the capacitance of the load.

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9.2.1.2.11 Startup and Shutdown Sequencing

A simple startup sequence is employed to maintain smooth operation. If the sequence is not followed, unintended events my occur.

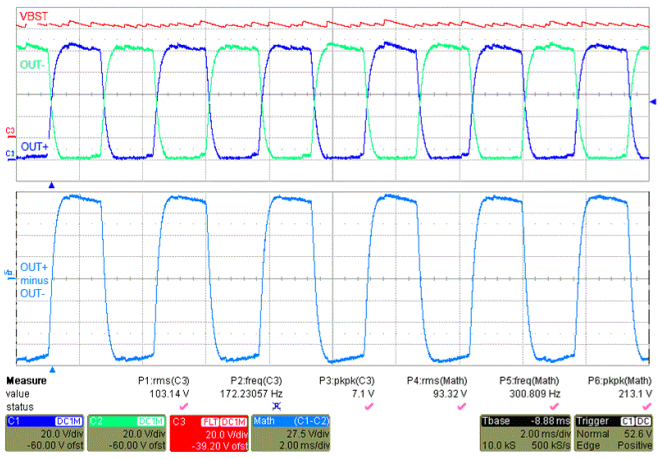
Use the following steps to startup the device in boost + amplifier mode:

1. Transition the DRV2700 enable pin from logic-low to logic-high.
2. Wait 2 ms to ensure that the DRV2700 circuitry is fully enabled and settled.
3. Provide a PWM, audio, or DAC source to be amplified through the DRV2700 device. When the input waveform is complete, continue to step 4.
4. Transition the DRV2700 enable pin from high to low.

Use the following steps to startup the device in flyback mode:

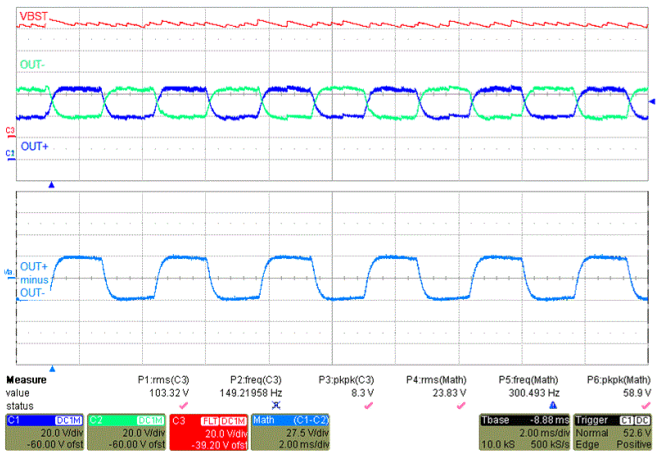
1. Set the processor output to 0 V to set the feedback network to such that V_{HV} = 0 V. This setting ensures that V_{HV} does not spike when the device is enabled.
2. Transition the DRV2700 enable pin from logic-low to logic-high.
3. Wait 2 ms to ensure that the DRV2700 circuitry is fully enabled and settled.
4. Begin and complete playback of the waveform from the processor. When the input waveform is complete, continue to step 4.
5. Transition the DRV2700 enable pin from high to low and power down the DAC source.

9.2.1.3 Application Curves



V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 40.7 dB

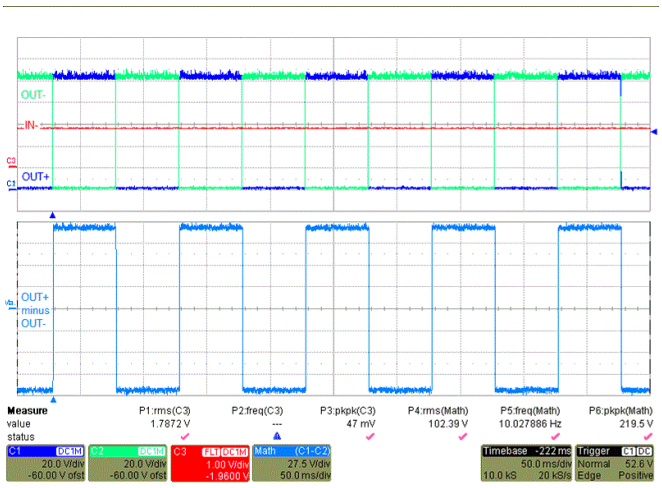
Figure 27. AC Coupled Differential Output



V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 28.8 dB

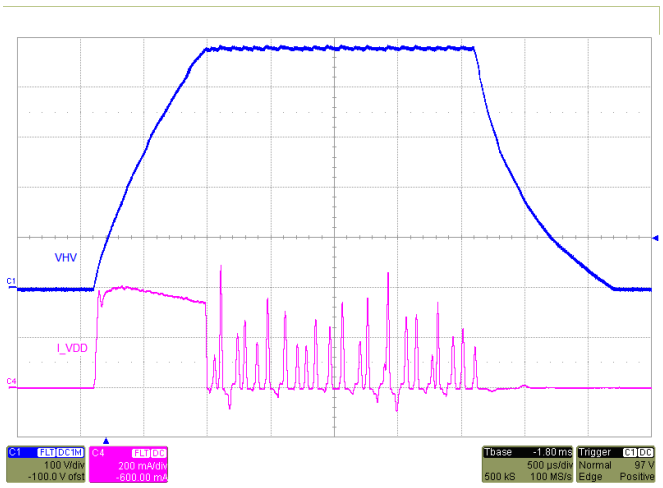
Figure 28. AC Coupled Differential Output

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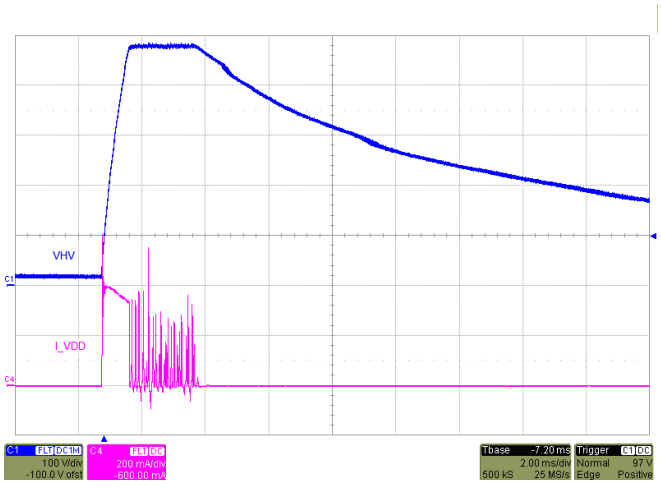
V_{DD} = 3.6 V $C_{(LOAD)}$ = Open V_{PVDD} = 105 V
G = 28.8 dB

Figure 29. DC Coupled Differential Output



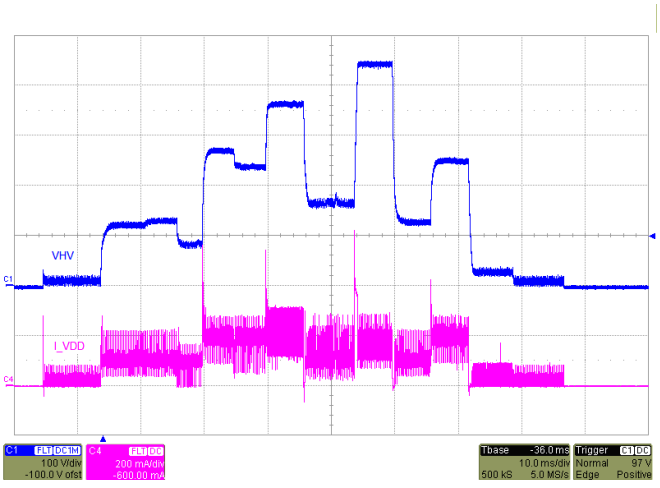
V_{DD} = 5 V $C_{(LOAD)}$ = 22 nF V_{HV} = 0 to 500 V

Figure 30. High Voltage Mode with FET Pulldown



V_{DD} = 5 V $C_{(LOAD)}$ = 22 nF V_{HV} = 0 to 500 V

Figure 31. High Voltage Mode without FET Pulldown



V_{DD} = 5 V $C_{(LOAD)}$ = 22 nF V_{HV} = 0 to 500 V

Figure 32. High Voltage Mode Arbitrary Waveform

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9.2.2 Filtered AC Coupled Single-Ended PWM Input Application

The AC coupled single-ended PWM input is very similar to the application described in the *AC-Coupled DAC Input Application* section, however because the input is a true PWM signal, a low-pass filter is highly recommended. Typically, a low cutoff frequency is desired to ensure the higher frequencies have been attenuated and are not amplified.

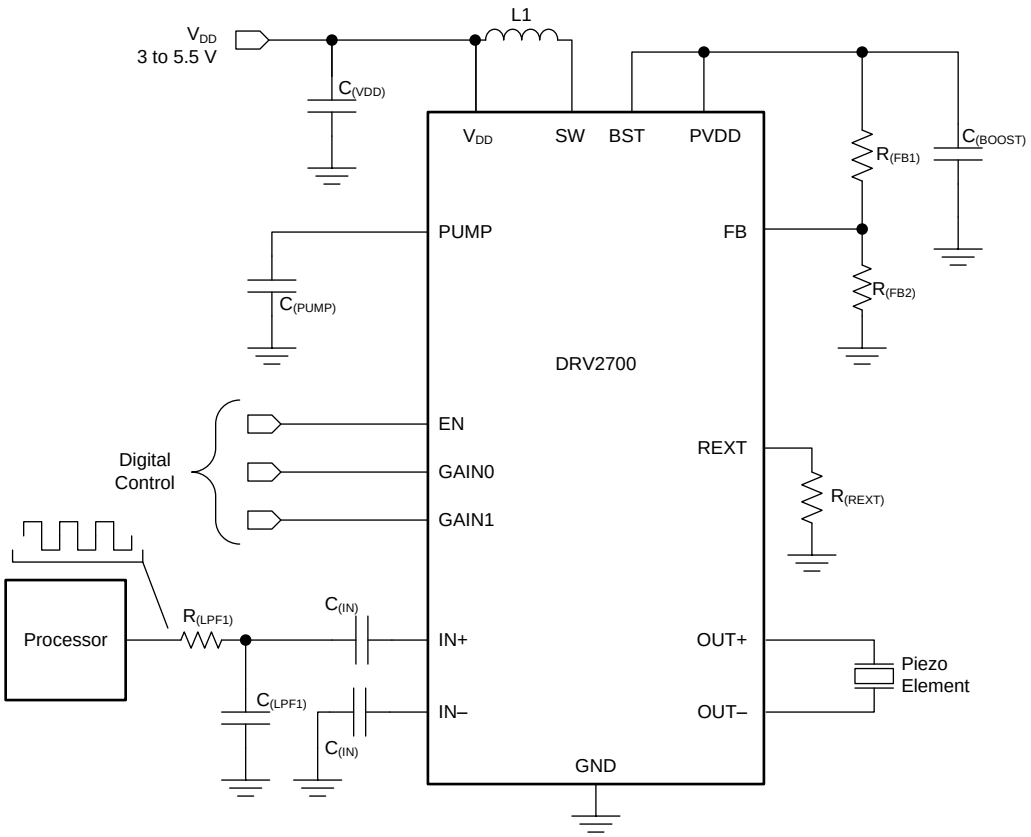


Figure 33. Filtered AC Coupled Single-Ended PWM Input

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9.2.3 DC-Coupled DAC Input Application

The DC-coupled DAC input is used in applications when the user might need to drive the output at a constant DC level. A typical application for th the DC-coupled DAC input is for piezo pneumatic valves. A benefit to this application circuit is that all of the inputs, including power, are at a very low voltage while keeping the high-voltage piezo load separated. This feature allows easy implementation into systems and to help separate or isolate the high voltages loads from the critical controls.

Piezoelectric materials have a certain voltage that debias the piezo phenomenon. To prevent this debiasing from occurring, limit the input using a controlled input signal. As a backup measure, place a Zener diode to restrict the input.

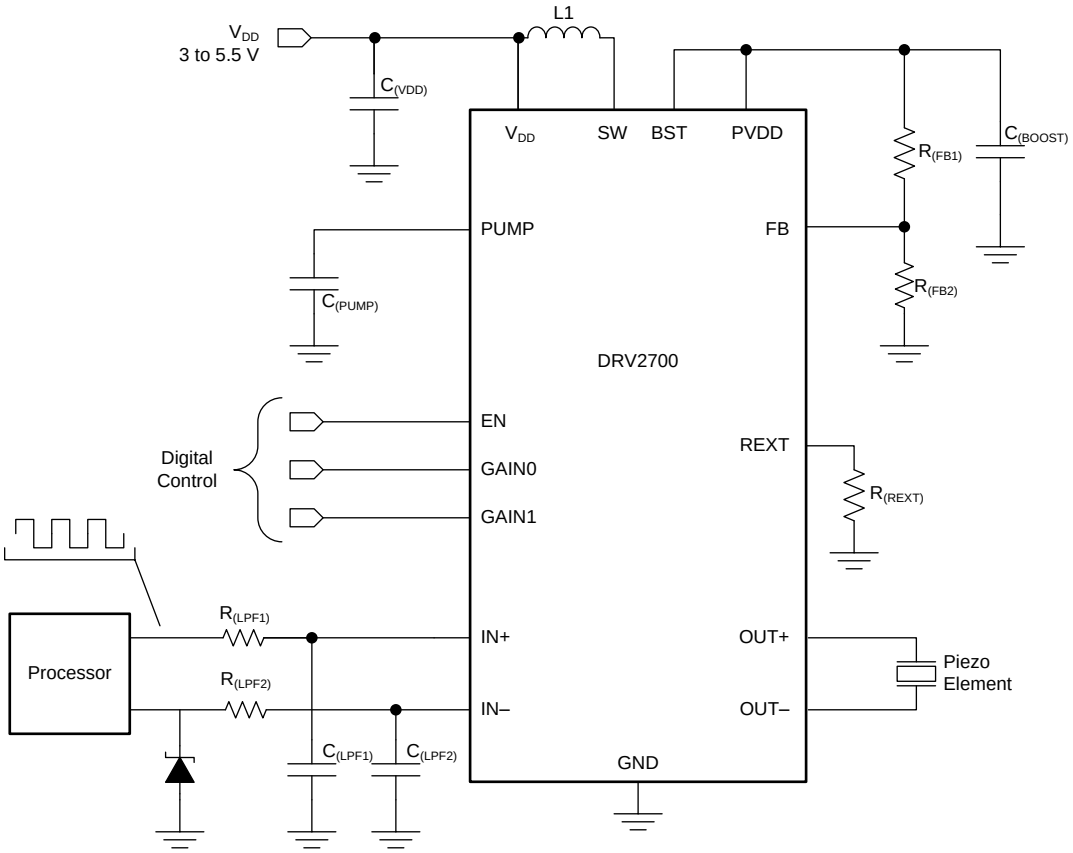


Figure 34. DC-Coupled DAC Input

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9.2.4 DC-Coupled Reference Input Application

The DC-coupled referenced to V_{DD} input is used in applications when the user might need to drive the output at a constant DC level in an on-off implementation. A typical application for this configuration is for piezo pneumatic valves. A benefit to this application circuit is that all of the inputs, including power, are at a very low voltage while keeping the high-voltage piezo load separated. Additionally, all that is required is the V_{DD} input. This feature allows easy implementation into systems and to help separate or isolate the high voltages loads from the critical controls.

As mentioned in the previous section, piezoelectric materials have a certain voltage that debias the piezo phenomenon. This configuration protects the piezo from negative voltages because the input is always positive.

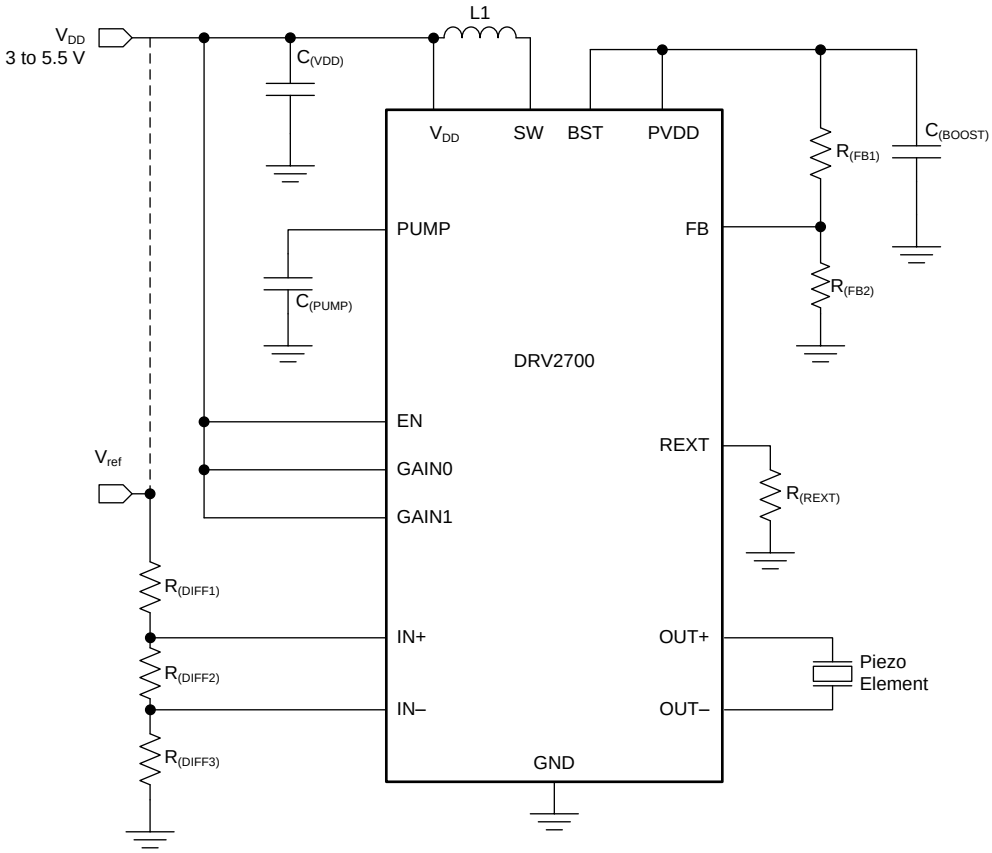


Figure 35. DC-Coupled Referenced Input

This application circuit can also be altered to only use the boost as shown in Figure 36. The benefits of altering this circuit is that it requires less components and has better power efficiency because no power is used in the amplifier. The drawback is that ripple occurs on the piezo element and the fall time of the output is longer because it is drained based on the RC time constant on the BST node.

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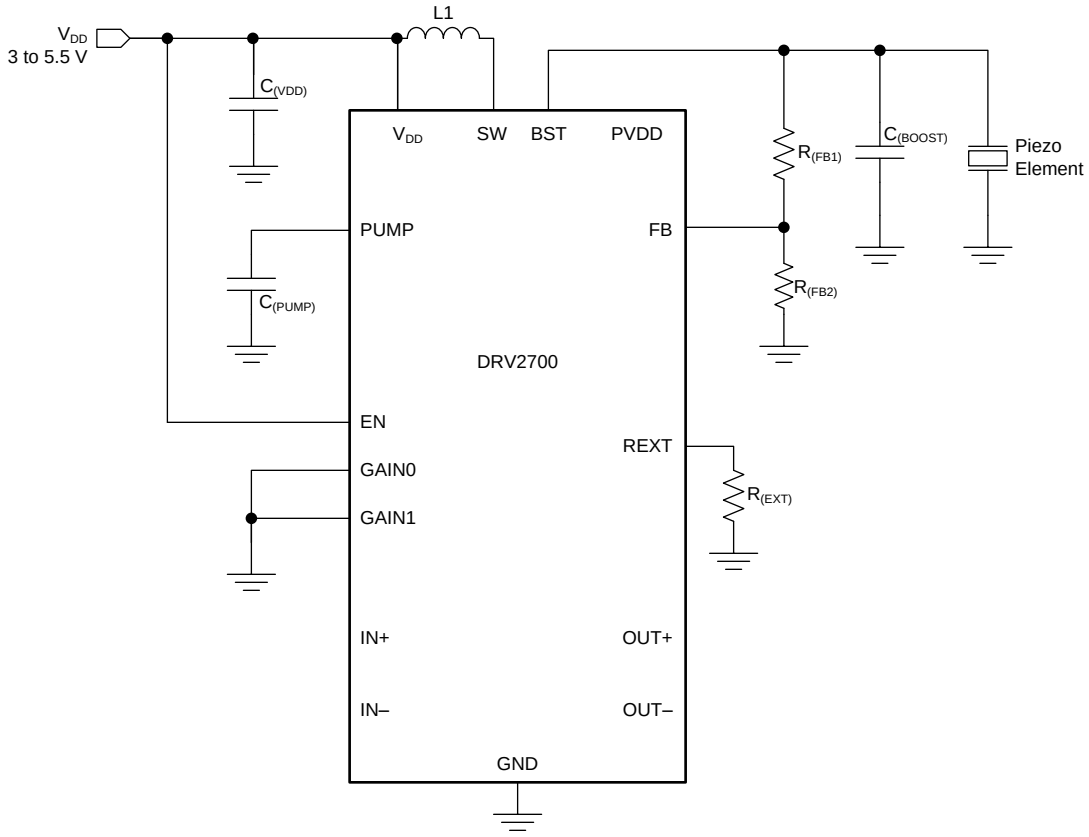


Figure 36. Boost Driving Piezo

9.2.5 Flyback Circuit

The flyback circuit is intended for applications using piezo valves, piezo polymers, and other high-voltage loads. The previously listed applications go from ±100 V, however this circuit can go up to even higher voltages (1 kV for example) depending on the feedback network and maximum operating conditions of the external components. The input is controlled using PWM, a DAC, or a purely analog signal. Therefore, a proper input filter may be required as discussed in the previous application circuits.

The increased voltage range, however, comes at a price. As the output voltage increases, the capable output sourcing current is lowered. However, because most piezo loads require a small current for the holding or blocking force, the drop in current may not impact the performance of the application. Figure 37 shows a typical flyback circuit.

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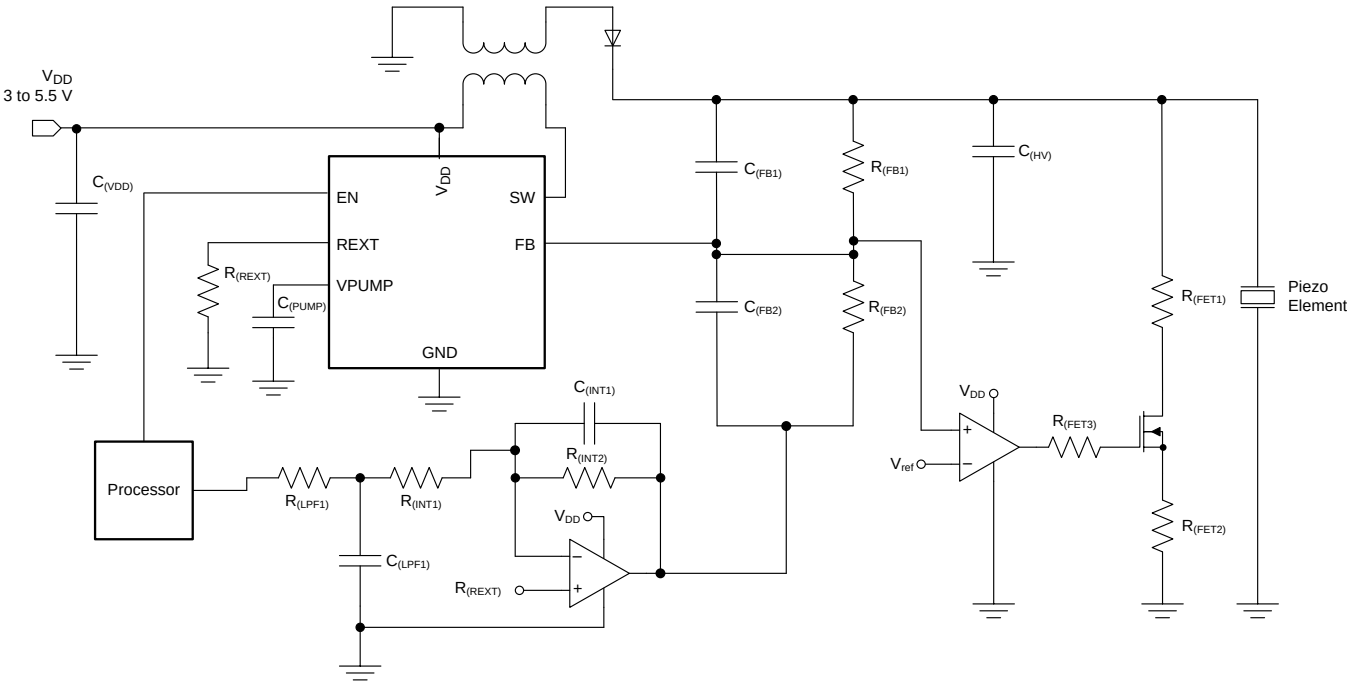


Figure 37. Flyback Circuit

The following sections shown in Figure 37 must be explained:

- Op-amp integrator
- Comparator and pulldown FET
- $C_{(HV)}$ value

The op-amp integrator shown at the bottom of the circuit in Figure 37, is used to control the output voltage. Because the input can be a PWM or DAC signal, it helps smooth out the input signal. Additionally, the output controls the virtual ground of the feedback network. For example, when the output of the integrator is equal to V_{OL} (approximately 0 V), the current through $R_{(FB2)}$ is at the maximum and therefore increase the current (and voltage) on $R_{(FB1)}$ which raises the voltage across the piezo load. Likewise, as the output voltage of the integrator increases, it then decreases the current through $R_{(FB2)}$ and therefore decreases the voltage on $R_{(FB1)}$, which lowers the voltage across the piezo load.

The comparator and pulldown FET are used to drain the charge on the high-voltage output. Because a high resistance (or low current) is desired through for the feedback network, the RC-time constant of draining charge can be very long. To help with this long RC-time constraint, the comparator and pulldown FET are added to drain charge when $V_{FB} > V_{ref}$ which adds a low resistance in parallel and therefore lowers the RC time constant. Ensure that this pulldown network can support the voltage and the current. As shown in Figure 30 and Figure 31, the pulldown allows for better regulation and faster stopping time.

Lastly, the $C_{(HV)}$ value is determined by the system. A value of >1-nF total capacitance is required on the high-voltage node for proper regulation. This total capacitance is the combination of the piezo load and the onboard $C_{(HV)}$.

NOTE

As the capacitance increases, the voltage ripple on the output decreases. However, this decrease in ripple also slows down the startup or slew rate on the output. Ensure that the $C_{(HV)}$ and the piezo load can support the high voltage across $C_{(HV)}$ and the load.

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9.3 System Example

To use the DRV2700 in a system, all that is required is a controller for the input signal and digital control, power management to provide power to the device, and a high-voltage load. Figure 38 shows a typical system diagram using the DRV2700 device. Because most systems already include some type of controller and power management, the DRV2700 device can easily be added to an existing system.

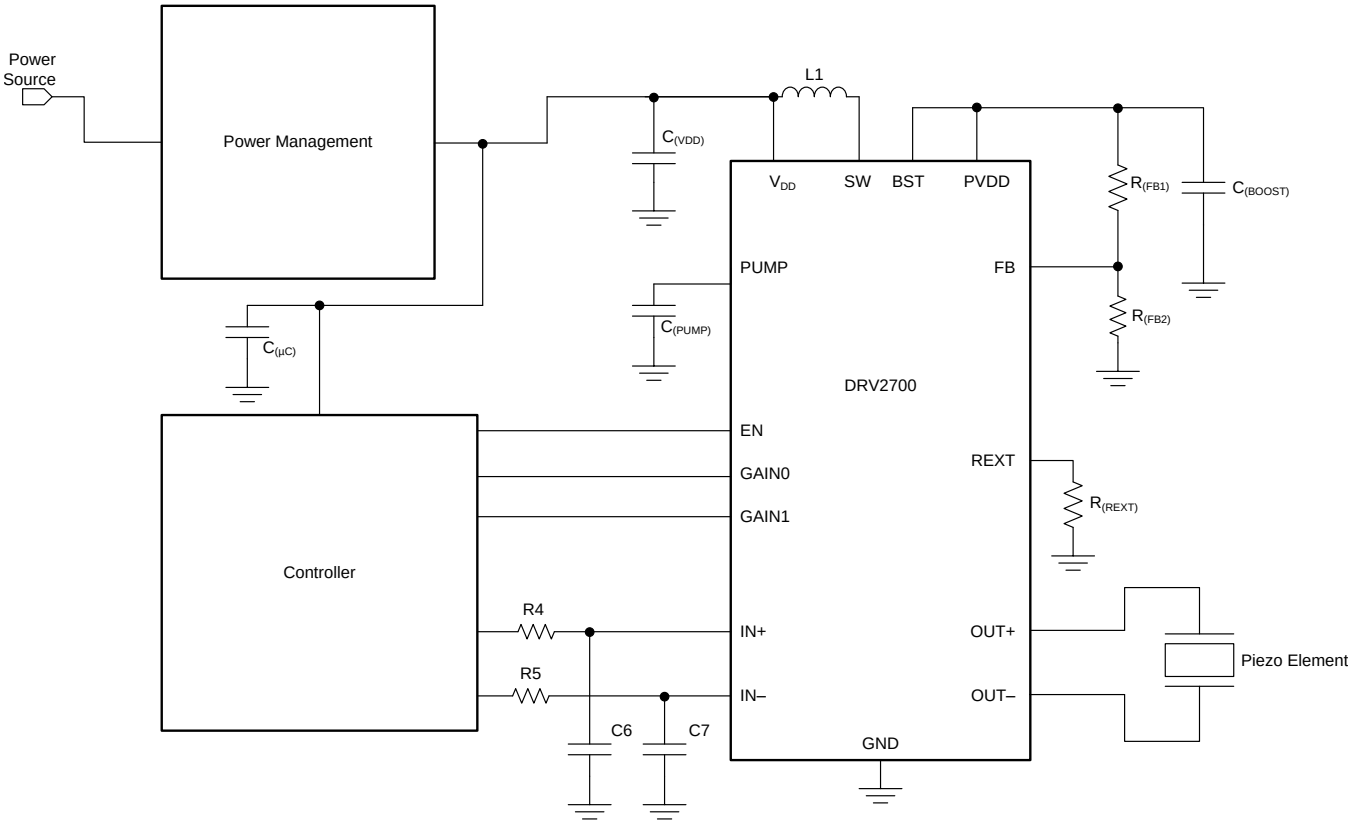


Figure 38. DRV2700 System Diagram

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10 Power Supply Recommendations

The recommended voltage supply range for the DRV8662 device is 3 to 5.5 V. For proper operation, place a 0.1-µF low-equivalent series resistance (ESR) supply-bypass capacitor of X5R or X7R type near the V_{DD} pin. This bypass capacitor should have a voltage rating of at least 10 V. The internal charge pump requires a 0.1-µF capacitor of X5R or X7R type with a voltage rating of 10 V or greater to be placed between the PUMP pin and ground for proper operation and stability. Do not use the charge pump as a voltage source for any other devices.

11 Layout

11.1 Layout Guidelines

11.1.1 Boost + Amplifier Configuration Layout Considerations

To achieve ideal device performance, use of the thermal footprint outlined by this data sheet is recommended. See the land pattern diagram in the *机械、封装和可订购信息* section for exact dimensions. The thermal pad of the DRV2700 device must be soldered directly to the thermal pad on the printed circuit board (PCB). The thermal pad of the PCB must be connected to the ground net with thermal vias to any existing backside or internal copper ground planes. Connection to a ground plane on the top layer near the corners of the device is also recommended.

Additionally to help minimize crosstalk between the FB voltage and the SW signal, keep the boost programming resistors (R_{FB1} and R_{FB2}) as close as possible to the FB pin of the DRV2700 device. Routing this trace underneath the middle of the inductor is also helpful. If possible, provide a grounding plane between the two signals.

Lastly, keep the BST trace and plane as large as possible to help minimize the resistance and inductance.

11.1.2 Flyback Configuration Layout Considerations

To achieve ideal device performance, use of the thermal footprint outlined by this data sheet is recommended. See the land pattern diagram in the *机械、封装和可订购信息* section for exact dimensions. The thermal pad of the DRV2700 device must be soldered directly to the thermal pad on the PCB. The thermal pad of the PCB must be connected to the ground net with thermal vias to any existing backside or internal copper ground planes. Connection to a ground plane on the top layer near the corners of the device is also recommended.

Additionally, minimizing the capacitance on the SW node is very important. Minimizing this capacitance is accomplished by placing the transformer very close to the SW pin and by removing the ground plane beneath the transformer pads.

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11.2 Layout Example

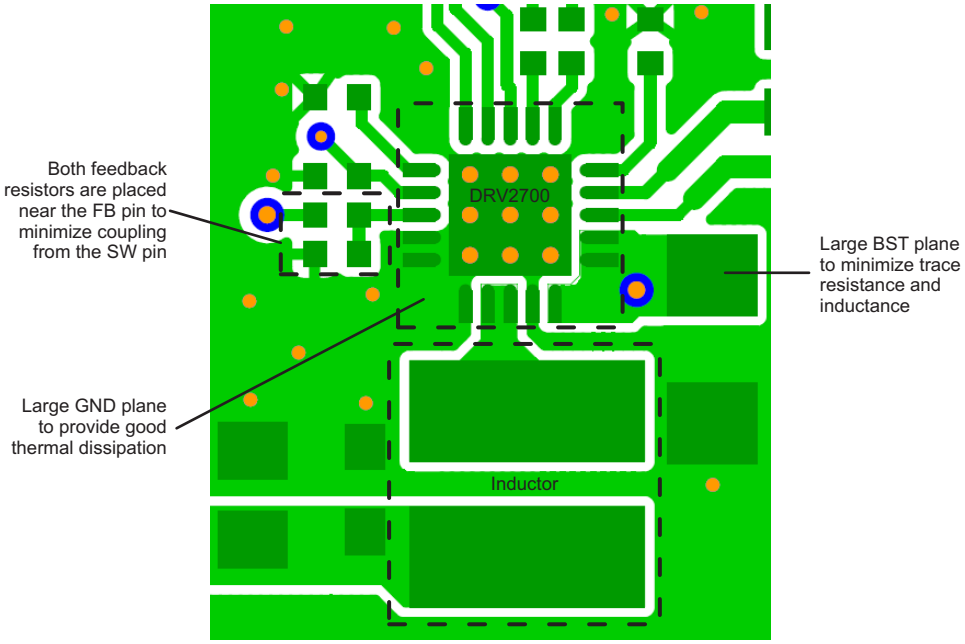


Figure 39. DRV2700 Boost + Amplifier Layout Example

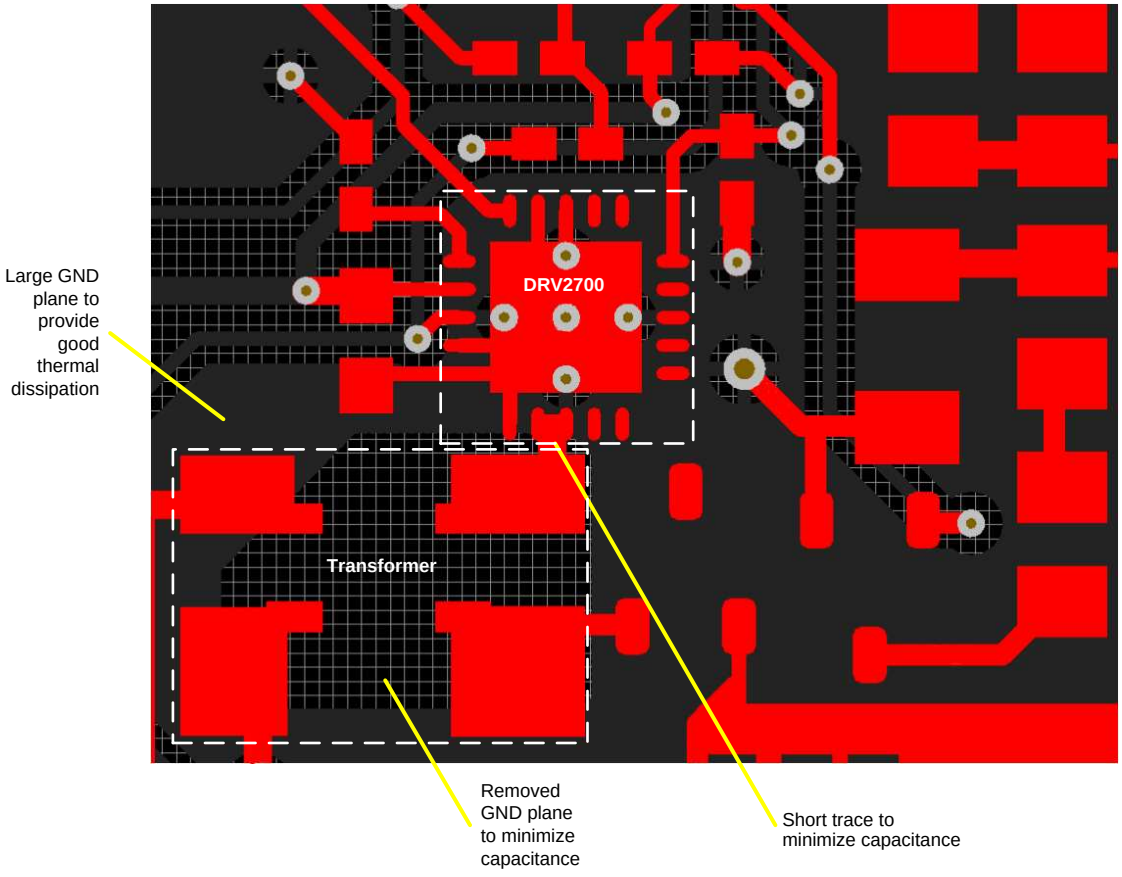


Figure 40. DRV2700 Flyback Layout Example

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

《DRV2700EVM 高压压电驱动器评估套件》，SLOU403

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12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV2700RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV2700	Samples
DRV2700RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV2700	Samples

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

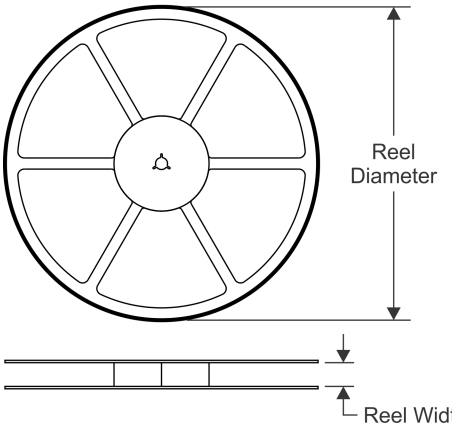
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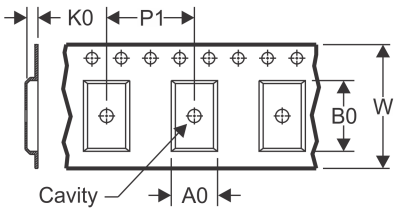
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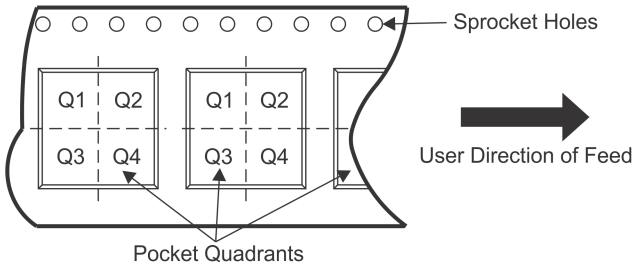


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

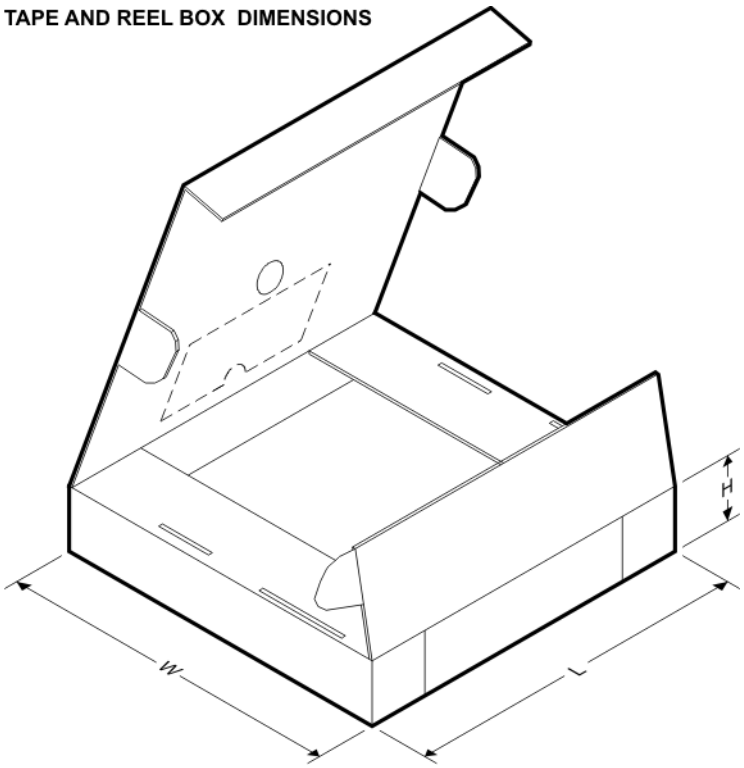
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2700RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV2700RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

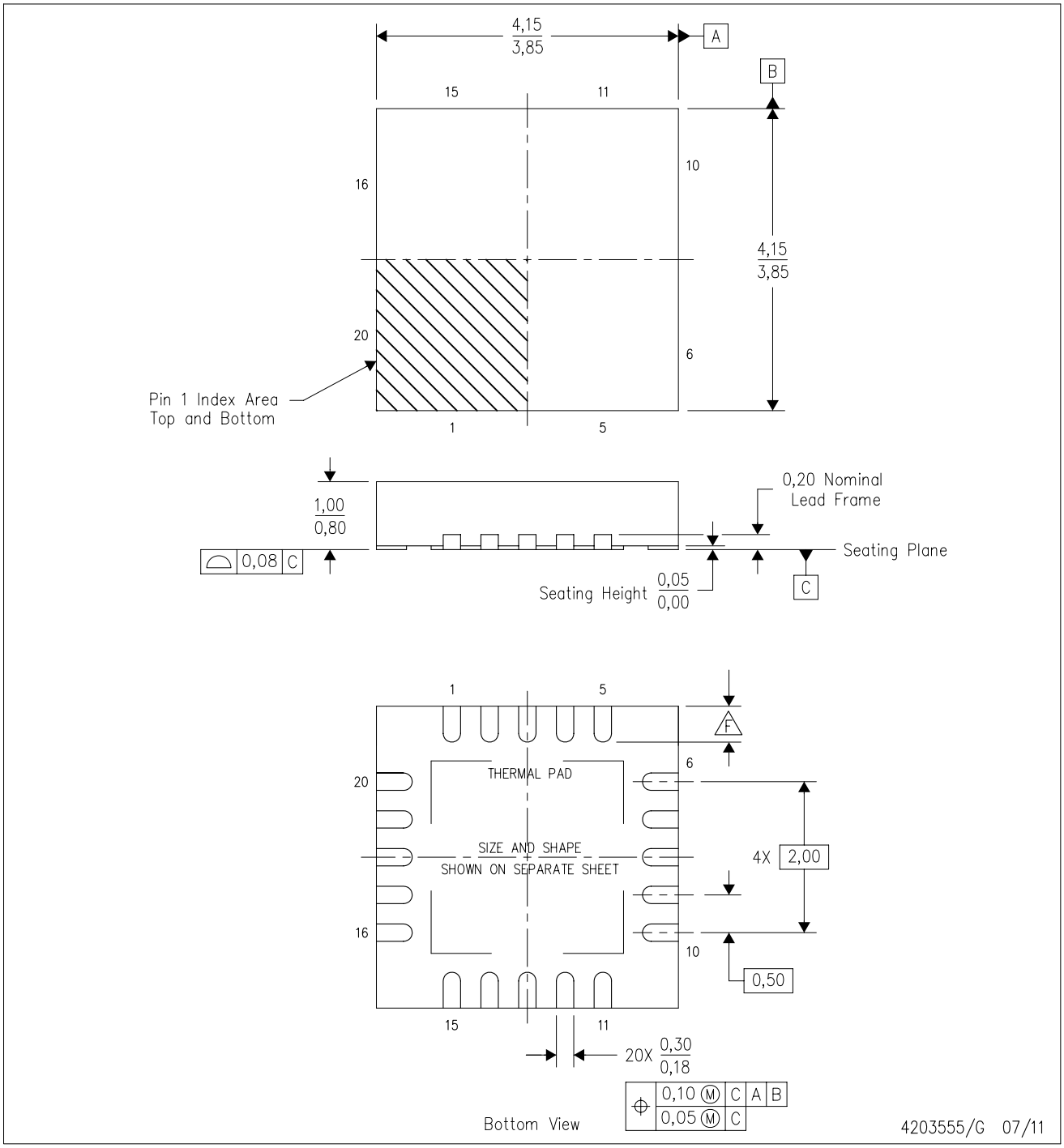
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2700RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
DRV2700RGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

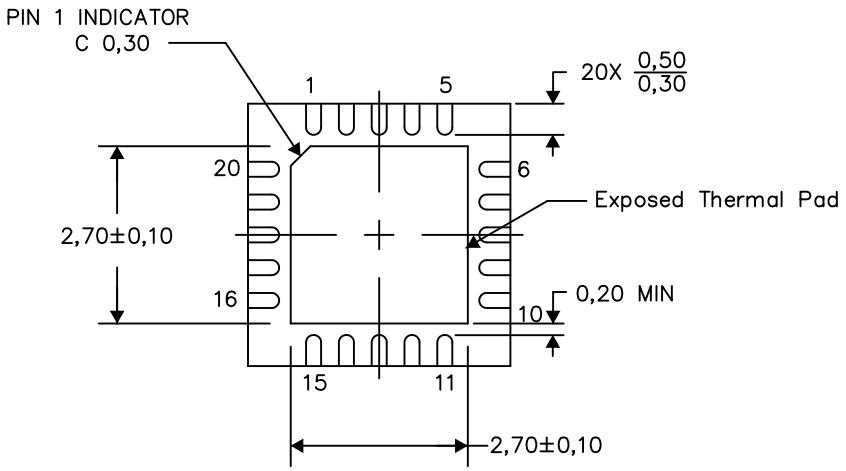
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



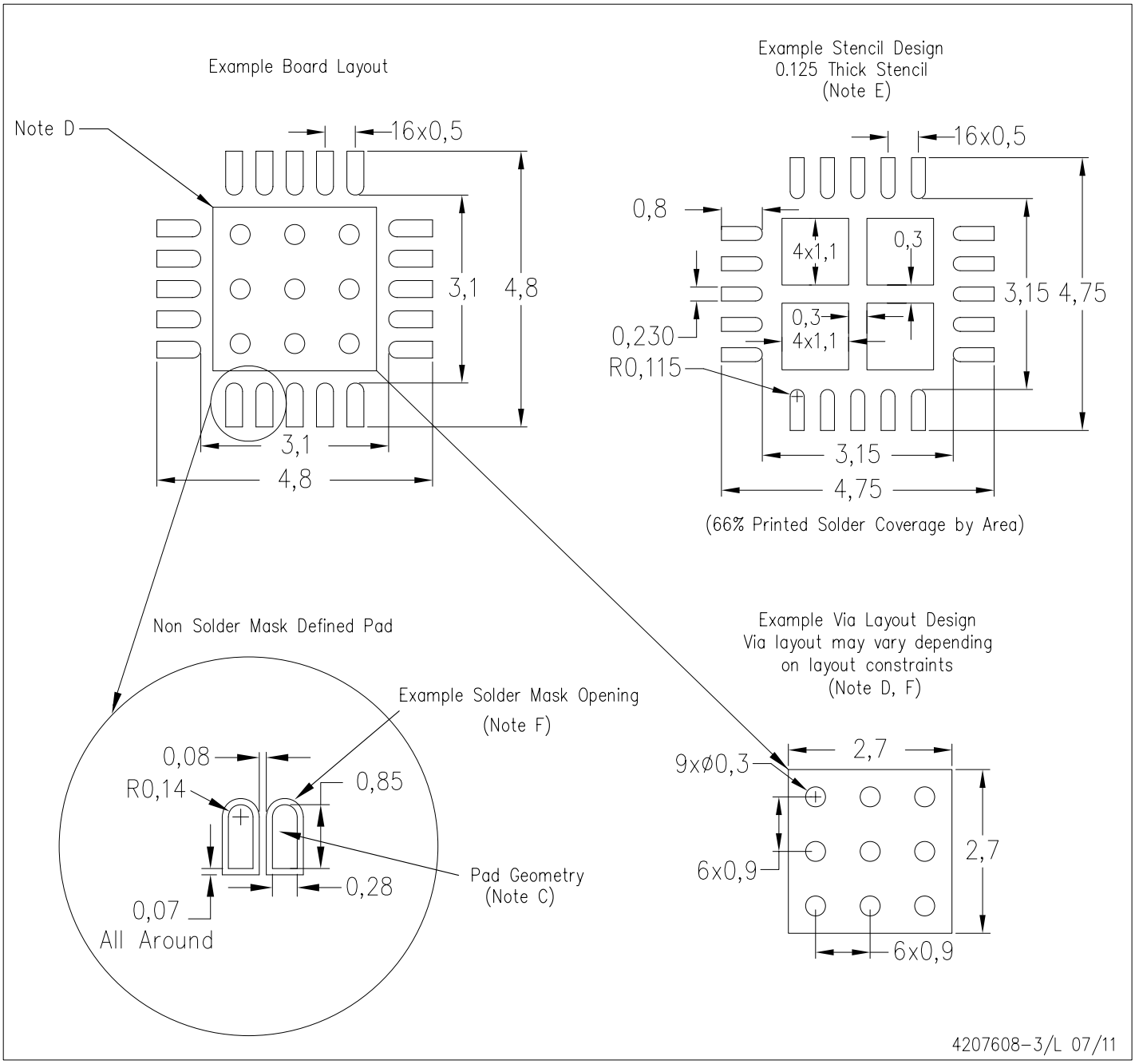
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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