Piezo Haptic Driver with Integrated Boost Converter and Digital Front End

Check for Samples: DRV2665

FEATURES

- **Integrated Digital Front End**
  - **I^2C Bus Control up to 400 kHz**
  - **Internal 100 Byte FIFO Interface**
  - **Immersion TS5000 Compliant**
  - **Optional Analog Inputs**
- **High Voltage Piezo-Haptic Driver**
  - **Drives up to 100 nF at 200 V_{PP} and 300 Hz**
  - **Drives up to 150 nF at 150 V_{PP} and 300 Hz**
  - **Drives up to 330 nF at 100 V_{PP} and 300 Hz**
  - **Drives up to 680 nF at 50 V_{PP} and 300 Hz**
  - **Differential Output**
- **Integrated 105 V Boost Converter**
  - **Adjustable Boost Voltage**
  - **Adjustable Boost Current Limit**
  - **Integrated Power FET and Diode**
  - **No Transformer Required**
- **Fast Start Up Time of 2 ms (typical)**
- **Wide Supply Voltage Range of 3 V to 5.5 V**
- **1.8 V Compatible, VDD Tolerant Digital Pins**
- **Available in a 4 mm × 4 mm × 0.9 mm QFN package (RGP)**
- **Pin-Similar with DRV8662**

APPLICATIONS

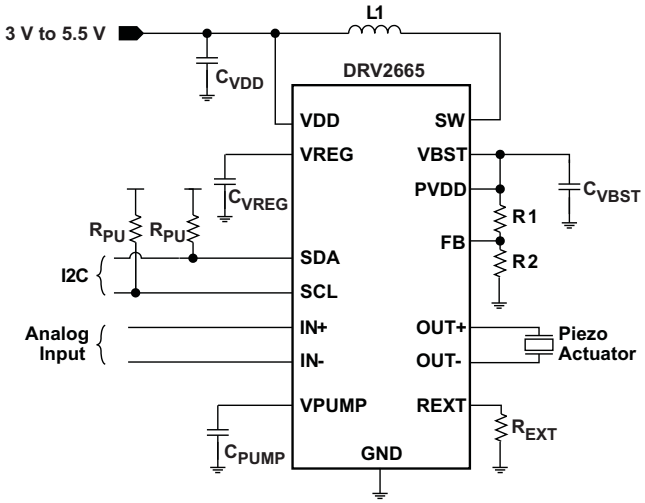
- **Mobile Phones**
- **Tablets**
- **Portable Computers**
- **Keyboards and Mice**
- **Electronic Gaming**
- **Touch Enabled Devices**

DESCRIPTION

The DRV2665 is a piezo haptic driver with integrated 105 V boost switch, integrated power diode, integrated fully-differential amplifier, and integrated digital front end. This versatile device is capable of driving both high-voltage and low-voltage piezo haptic actuators. The input signal can be driven as haptic packets over the I^2C port or via the analog inputs.

The DRV2665 digital interface is available via an I^2C compatible bus. A digital interface relieves the costly processor burden of PWM generation or additional analog channel requirements in the host system. Any writes to the internal first-in, first-out buffer (FIFO) will automatically wake up the device and begin playing the waveform after the 2 ms internal startup procedure. When the data flow stops or the FIFO under-runs, the DRV2665 will automatically enter a pop-less shutdown procedure.

The boost voltage is set using two external resistors, and the boost current limit is programmable via the R_{EXT} resistor. A typical start-up time of 2 ms makes the DRV2665 an ideal piezo driver for fast haptic responses. Thermal overload protection prevents the device from being damaged when overdriven.



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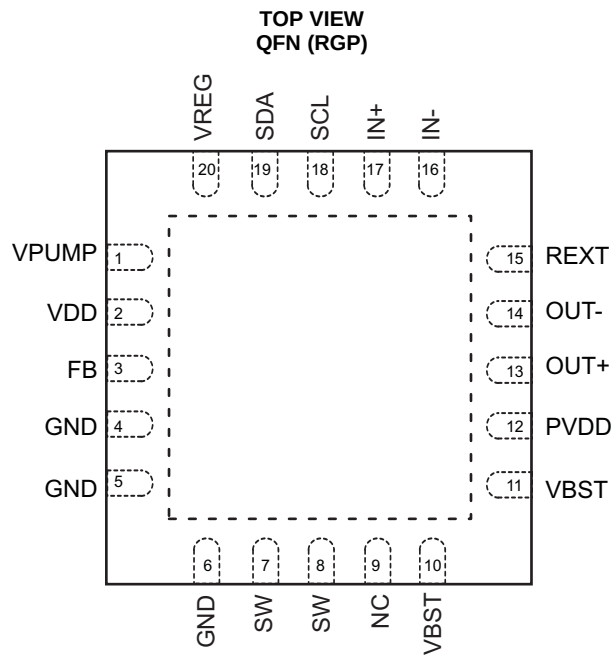
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

	QFN (RGP) 4 mm × 4 mm × 0.9 mm	ORDERING NUMBER	TRANSPORT MEDIA
Device	DRV2665RGP	DRV2665RGPR	3000 Unit Reel
		DRV2665RGPT	250 Unit Reel
Symbolization	2665		

PINOUT INFORMATION

TOP VIEW
QFN (RGP)



PIN FUNCTIONS

NAME	PIN	INPUT/ OUTPUT/POWER (I/O/P)	DESCRIPTION
IN+	17	I	Non-inverting analog input
IN-	16	I	Inverting analog input
OUT+	13	O	Non-inverting haptic driver output
OUT-	14	O	Inverting haptic driver output
VDD	2	P	Power supply (connect to battery)
GND	4, 5, 6	P	Ground
SW	7, 8	P	Internal boost switch pin
PVDD	12	P	Boost output voltage
SCL	18	I	I^2C Clock
SDA	19	I/O	I^2C Data
VREG	20	O	LDO Output (Requires 0.1 µF capacitor)
VPUMP	1	P	Internal charge-pump voltage
FB	3	I	Boost feedback
VBST	10, 11	P	Boost output voltage
REXT	15	I	Resistor to ground, sets boost current limit

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

			VALUE	UNIT
	Supply voltage, VDD		–0.3 to 6.0	V
V_I	Input Voltage	IN+, IN–, SDA, SCL, FB	–0.3 to V_{DD} + 0.3 V	V
	Boost Output Voltage	PVDD, SW, OUT+, OUT–	120	V
T_A	Operating free-air temperature range		–40 to 70	°C
T_J	Operating junction temperature range		–40 to 150	°C
T_{stg}	Storage temperature range		–65 to 85	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds (RGP)		260	°C
	ESD Protection	HBM	2500	V
		CDM	500	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV2665 RGP (20 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	30.4	
θ_{JB}	Junction-to-board thermal resistance	8.2	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	8.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

				MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	VDD		3.0		5.5	V
V_{BST}	Boost voltage	VBST		15		105	V
V_{IN}	Differential input voltage	IN+, IN-			1.8(1)		V
C_L	Load capacitance	VBST = 105 V, Frequency = 500 Hz, V_{OUT} = 200 V_{PP}				50	nF
		VBST = 105 V, Frequency = 300 Hz, V_{OUT} = 200 V_{PP}				100	
		VBST = 80 V, Frequency = 300 Hz, V_{OUT} = 150 V_{PP}				150	
		VBST = 55 V, Frequency = 300 Hz, V_{OUT} = 100 V_{PP}				330	
		VBST = 30 V, Frequency = 300 Hz, V_{OUT} = 50 V_{PP}				680	
		VBST = 25 V, Frequency = 300 Hz, V_{OUT} = 40 V_{PP}				1000	
		VBST = 15 V, Frequency = 300 Hz, V_{OUT} = 20 V_{PP}				3000	
V_{IL}	Digital input low voltage	SDA, SCL	V_{DD} = 3.6 V			0.5	V
V_{IH}	Digital input high voltage	SDA, SCL	V_{DD} = 3.6 V	1.4			V
R_{EXT}	Current limit control resistor			6		35	kΩ
L	Inductance for Boost Converter			3.3			µH

(1) Gains are optimized for a 1.8 V peak input

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.6 V, C_L = 47 nF, R_{EXT} = 7.5 kΩ, A_V = 40.7 dB, L = 4.7 µH (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REG}	Regulator output voltage	VREG		1.6	1.75	1.9	V
$\|I_{IL}\|$	Digital input low current	SDA, SCL	V_{DD} = 3.6 V, V_{IN} = 0 V			1	µA
$\|I_{IH}\|$	Digital input high current	SDA, SCL	V_{DD} = 3.6 V, V_{IN} = V_{DD}			1	µA
I_{SD}	Shut down current (Low-Power Standby)	V_{DD} = 3.6 V, STANDBY = 1			10		µA
I_{DDQ}	Quiescent current (Digital Mode)	V_{DD} = 3.6 V, STANDBY = 0			130	175	µA
I_{DDQ}	Quiescent current (Analog Mode)	V_{DD} = 3.6 V, Analog Input Mode, VBST = 105 V_{PP}			24		mA
		V_{DD} = 3.6 V, Analog Input Mode, VBST = 80 V_{PP}			13		
		V_{DD} = 3.6 V, Analog Input Mode, VBST = 55 V_{PP}			9		
		V_{DD} = 3.6 V, Analog Input Mode, VBST = 30 V_{PP}			5		
R_{IN}	Input impedance	IN+, IN-	All Gains		100		kΩ
$VOUT_{FS}$	Full-Scale Output Voltage (Digital Mode)	GAIN<1:0> = 00		49	50	51	V_{PP}
		GAIN<1:0> = 01		98	100	102	
		GAIN<1:0> = 10		147	150	153	
		GAIN<1:0> = 11		196	200	204	
$VOUT_{OS}$	Output Offset	All Gains		-0.25		0.25	V
BW	Amplifier bandwidth	GAIN<1:0> = 00, V_{OUT} = 50 V_{PP}, No Load			20		kHz
		GAIN<1:0> = 01, V_{OUT} = 100 V_{PP}, No Load			10		
		GAIN<1:0> = 10, V_{OUT} = 150 V_{PP}, No Load			7.5		
		GAIN<1:0> = 11, V_{OUT} = 200 V_{PP}, No Load			5		
$I_{BAT, AVG}$	Average battery current during operation	C_L = 220 nF, f = 200 Hz, VBST = 30 V, GAIN<1:0> = 00, V_{OUT} = 50 V_{PP}			69		mA
		C_L = 680 nF, f = 150 Hz, VBST = 30 V, GAIN<1:0> = 00, V_{OUT} = 50 V_{PP}			75		
		C_L = 680 nF, f = 300 Hz, VBST = 30 V, GAIN<1:0> = 00, V_{OUT} = 50 V_{PP}			115		
		C_L = 22 nF, f = 200 Hz, VBST = 80 V, GAIN<1:0> = 10, V_{OUT} = 150 V_{PP}			67		
		C_L = 47 nF, f = 150 Hz, VBST = 105 V, GAIN<1:0> = 11, V_{OUT} = 200 V_{PP}			210		
		C_L = 47 nF, f = 300 Hz, VBST = 105 V, GAIN<1:0> = 11, V_{OUT} = 200 V_{PP}			400		
THD+N	Total harmonic distortion plus noise	f = 300 Hz, V_{OUT} = 200 V_{PP}			1		%
t_{SU}	Start-up time	Time from I2C write until boost and amplifier are fully enabled			2		ms
f_s	Output sample rate	Digital playback sample rate		7.8	8	8.05	kHz

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TIMING CHARACTERISTICS

For I^2C interface signals over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states			400	kHz
$t_{W(H)}$	Pulse duration, SCL high		0.6			µs
$t_{W(L)}$	Pulse duration, SCL low		1.3			µs
t_{SU1}	Setup time, SDA to SCL		100			ns
t_{H1}	Hold time, SCL to SDA		10			ns
$t_{(BUF)}$	Bus free time between stop and start condition		1.3			µs
t_{SU2}	Setup time, SCL to start condition		0.6			µs
t_{H2}	Hold time, start condition to SCL		0.6			µs
t_{SU3}	Setup time, SCL to stop condition		0.6			µs

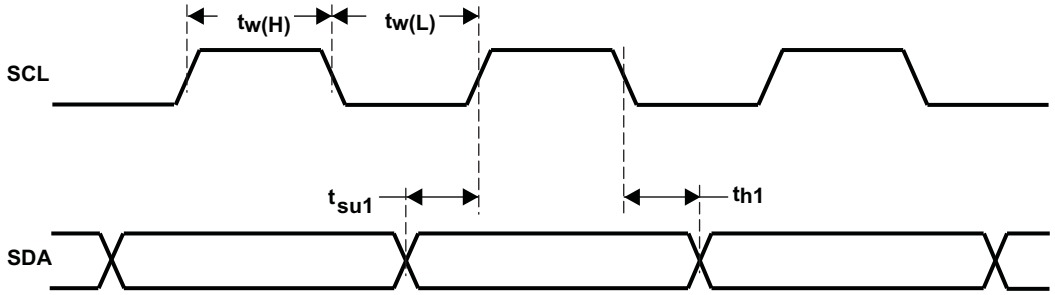


Figure 1. SCL and SDA Timing

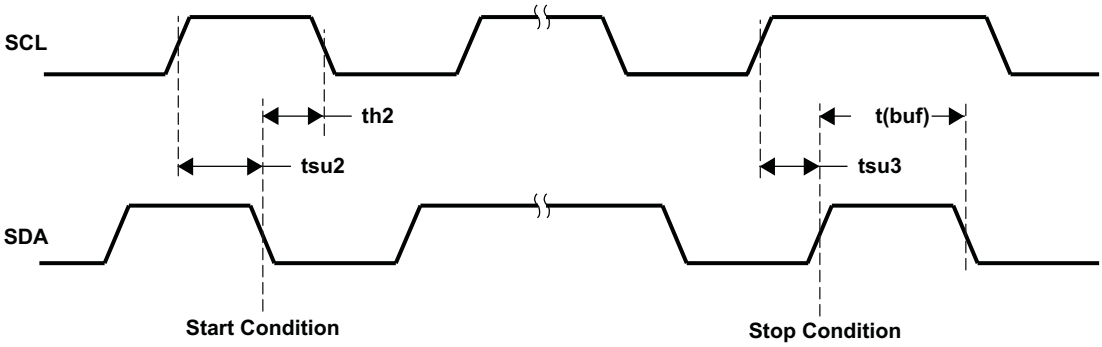


Figure 2. Start and Stop Conditions Timing

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs OUTPUT VOLTAGE

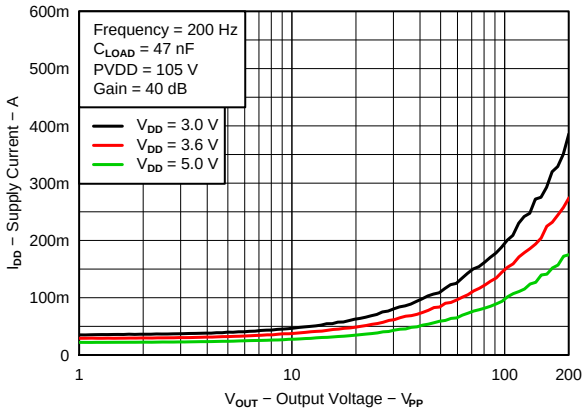


Figure 3.

SUPPLY CURRENT vs OUTPUT VOLTAGE

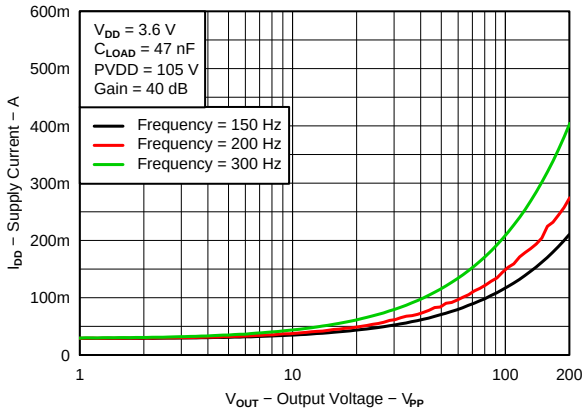


Figure 4.

SUPPLY CURRENT vs OUTPUT VOLTAGE

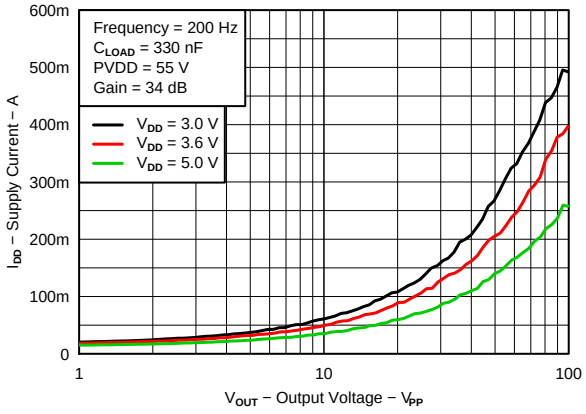


Figure 5.

SUPPLY CURRENT vs OUTPUT VOLTAGE

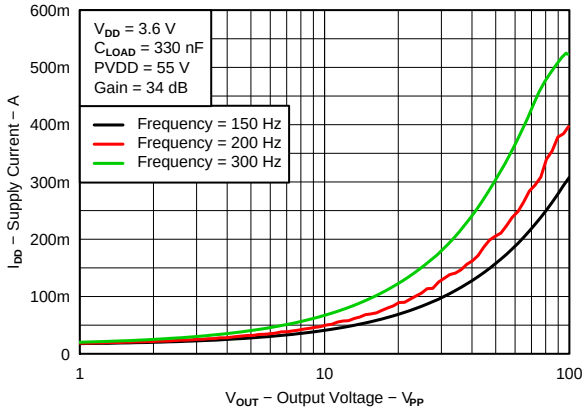


Figure 6.

SUPPLY CURRENT vs OUTPUT VOLTAGE

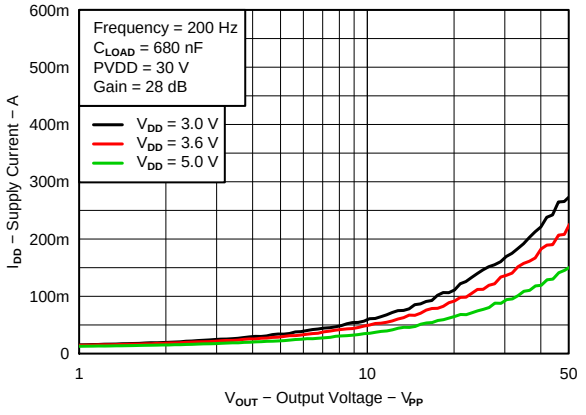


Figure 7.

SUPPLY CURRENT vs OUTPUT VOLTAGE

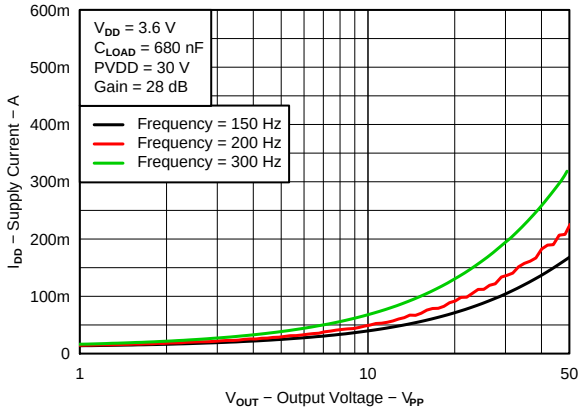


Figure 8.

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TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

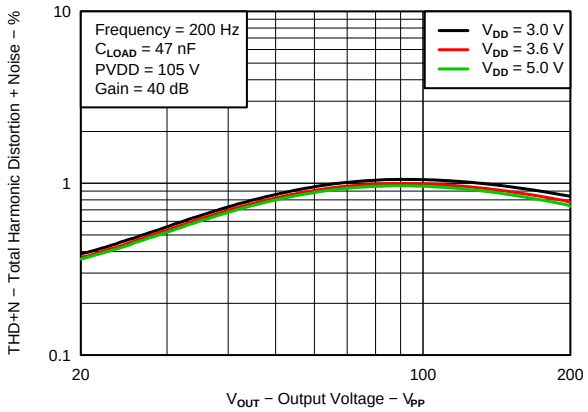


Figure 9.

TYPICAL WAVEFORM

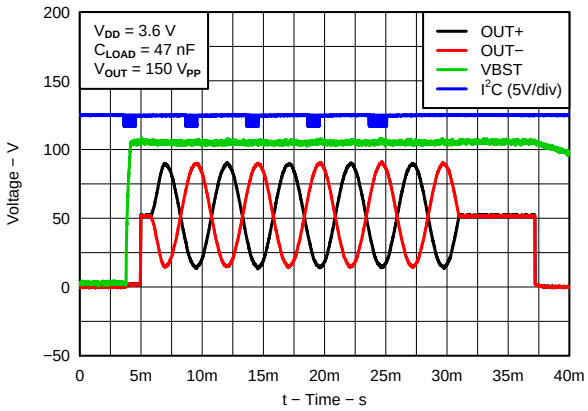


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

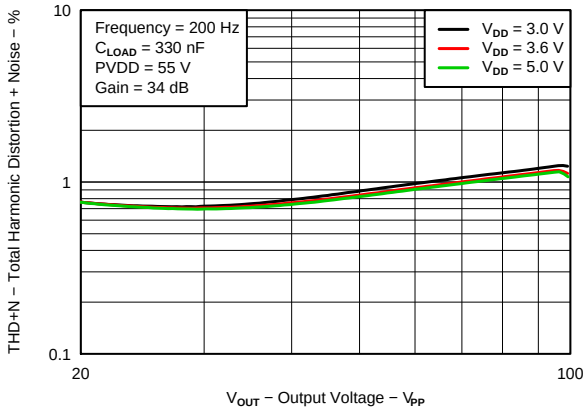


Figure 11.

TYPICAL WAVEFORM - DIFFERENTIAL

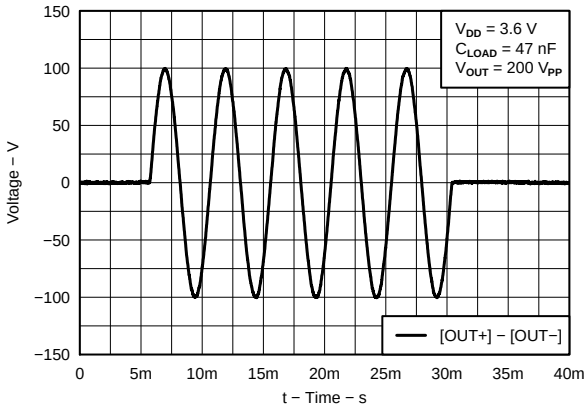


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

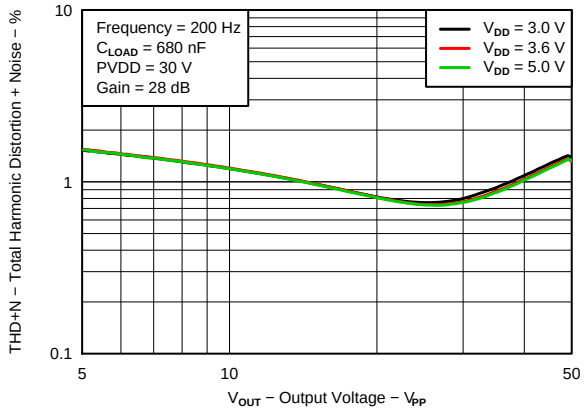


Figure 13.

I_{LIM} vs R_{EXT}

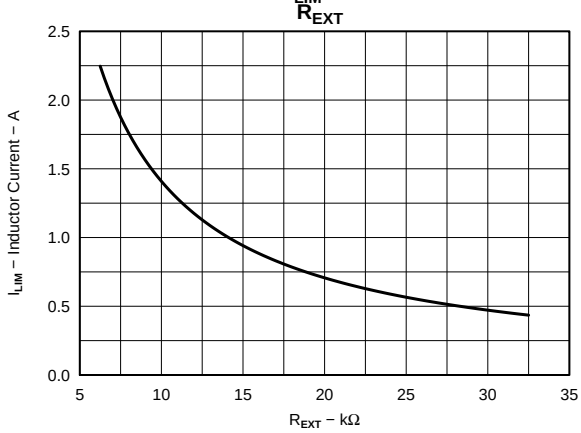
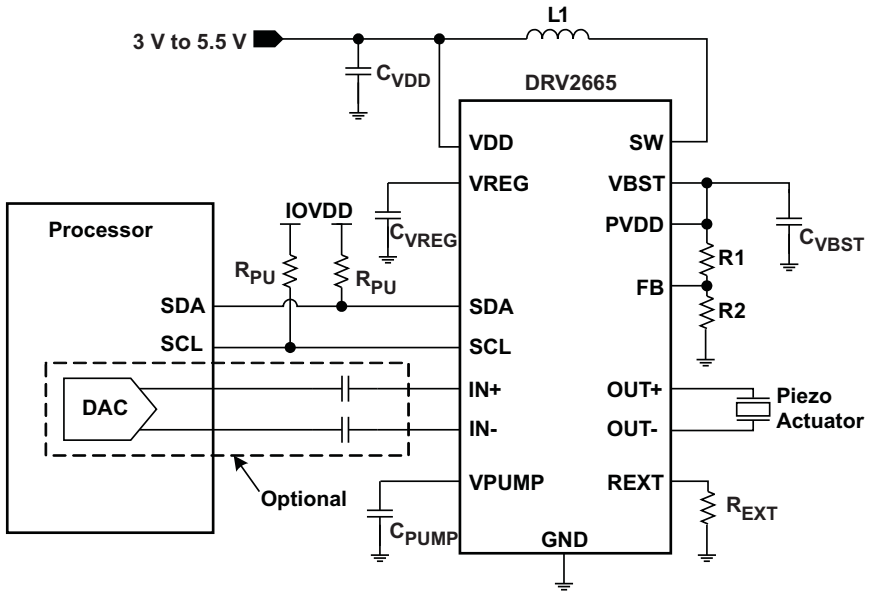


Figure 14.

DETAILED DESCRIPTION

SYSTEM DIAGRAM



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OPERATION

The DRV2665 takes the typical battery range used in portable applications (3.0 V to 5.5 V) and creates a boosted supply rail with an integrated DC-DC converter. This boosted supply rail is fed to an internal, high-voltage, fully-differential amplifier that is capable of driving capacitive loads such as piezos with signals up to 200 V_{PP}.

The DRV2665 interface has two modes of operation.

1. FIFO Mode
2. Analog Bypass Mode

The FIFO mode accepts 8-bit digital haptic waveform data over an I^2C compatible bus, which is written into an on-chip FIFO. The data is read out of the FIFO automatically at an 8 kHz sampling rate and fed into a digital-to-analog converter (DAC). The DAC then drives the high-voltage amplifier. Alternatively, the DRV2665 can accept analog waveforms that can be multiplexed into the high voltage amplifier directly through the IN+ and IN- pins.

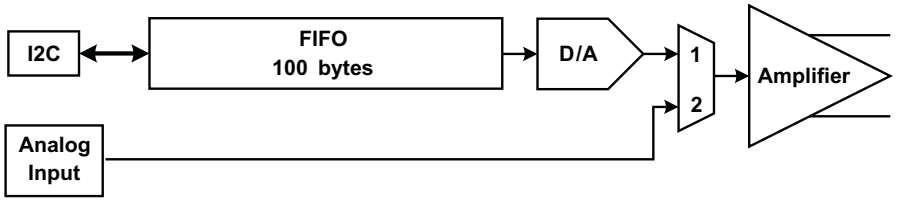


Figure 15. Signal Path

LOW-POWER STANDBY MODE

The DRV2665 has a low-power standby mode via the I^2C interface that puts the device in its lowest power state. This mode is entered when the Software Standby bit (STANDBY) is set from low to high. When the STANDBY bit is set high, no other mode of operation is enabled. When the STANDBY bit is transitioned from high to low, the device readied for operation and may receive data.

DEVICE RESET

The DRV2665 does not have a “RESET” pin, however it does have a register bit that provides the same functionality. When the DEV_RST bit is set, the device will immediately stop any transaction in process, reset all of its internal registers to their default values as well as put itself in STANDBY mode.

GAIN CONTROL

The DRV2665 gain is user-programmable via I^2C. The GAIN value determines the full-scale peak voltage when sending data to the FIFO, and the gain from IN+/IN– to OUT+/OUT– when using the analog inputs.

GAIN[1]	GAIN[0]	Full Scale Peak Voltage (V)	Gain (dB) Analog Mode
0	0	25	28.8
0	1	50	34.8
1	0	75	38.4
1	1	100	40.7

The gains are optimized to achieve approximately 50 V_{PP}, 100 V_{PP}, 150 V_{PP}, or 200 V_{PP} without clipping from the digital interface or from a 1.8 V supplied single-ended source through the analog interface. Note the boost voltage should be programmed for the rated voltage of the actuator or below. The user should take care not to select higher gains than necessary. Clipping of the amplifier will occur if the expected peak voltage is greater than the boost converter output voltage (VBST).

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FIFO OPERATION

When the first data byte is written to the FIFO, the DRV2665 will go through the proper startup sequence and begin outputting the waveform automatically. An internal timing sequence will wait approximately 2 ms before the first data is sent through the DAC and output by the device. The data plays out of the FIFO at an 8 kHz sample rate. It is important that the data values start and end at or near the mid-scale code (0x00) to avoid large steps at the beginning and end of the waveform. Once the FIFO is empty, the device will wait for the timeout period, and then enter an idle state.

Since the data rate of the serial interface could be faster than the read-out rate of the FIFO, the device will not acknowledge, or NAK, if the FIFO is full during a FIFO write transaction. If at any time the FIFO becomes completely full, the FIFOFull bit will be set. When in this condition, the FIFO cannot accept more data without overwriting previous data that has not yet been played. If this occurs, the user must wait until data has had a chance to empty from the FIFO before sending more data. The data should be resent starting at the byte that received a NAK.

Any multi-byte I2C write to the FIFO register is treated as a continuous write to the FIFO. Multi-byte writes are preferred for optimum performance. The FIFO interprets the incoming data as 2's complement. This means the maximum full-scale code is 0x7F, the maximum negative code is 0x80, and the mid-scale is 0x00.

WAVEFORM TIMEOUT

The DRV2665 has a timeout period after the FIFO has emptied. This timeout period allows the user time to send a subsequent waveform before the DRV2665 logic puts the device into idle mode. This allows the host processor time to cue up an adjoining waveform from memory. After the timeout expires, the DRV2665 must re-enter the 2 ms startup sequence before the next waveform plays. The timeout period is register-selectable to be 5, 10, 15, or 20 ms.

RAMP DOWN BEHAVIOR

If the user leaves the state of the DAC at any level other than mid-scale (0x00), the DAC will automatically ramp down at a safe rate after the timeout period has expired. If the DRV2665 is properly programmed, the ramp down sequence will never be used. It is a failsafe for any unavoidable interruptions to the playback process. Any writes to the FIFO during the ramp down period will be discarded.

ANALOG BYPASS MODE

When the Input_MUX bit is set, the DRV2665 will switch the analog inputs (IN+/IN-) to the high voltage amplifier. While in the analog mode, the gain is still register selectable. Also, the high-voltage amplifier enable is controlled directly via the EN_Override bit, so the EN_Override bit must be set for the boost and amplifier to be active.

ADJUSTABLE BOOST VOLTAGE

The output voltage of the integrated boost converter may be adjusted by a resistive feedback divider between the boost output voltage (VBST) and the feedback pin (FB). The boost voltage should be programmed to a value greater than the maximum peak signal voltage that the user expects to create with the DRV2665 amplifier. Lower boost voltages will achieve better system efficiency when lower amplitude signals are applied, so the user should take care not to use a higher boost voltage than necessary. The maximum allowed boost voltage is 105V.

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ADJUSTABLE BOOST CURRENT LIMIT

The current limit of the boost switch may be adjusted via a resistor to ground placed on the REXT pin. The programmed current limit should be less than the rated saturation limit of the inductor to avoid damage to both the inductor and the DRV2665. If the combination of the programmed limit and inductor saturation is not high enough, then the output current of the boost converter will not be high enough to regulate the boost output voltage under heavy load conditions. This will, in turn, cause the boosted rail to sag, possibly causing distortion of the output waveform.

INTERNAL CHARGE PUMP

The DRV2665 has an integrated charge pump to provide adequate gate drive for internal nodes. The output of this charge pump is placed on the VPUMP pin. An X5R or X7R storage capacitor of 0.1 µF with a voltage rating of 10 V or greater must be placed at this pin.

THERMAL SHUTDOWN

The DRV2665 contains an internal temperature sensor that will shut down both the boost converter and the amplifier when the temperature threshold is exceeded. When the die temperature falls below the threshold, the device will restart operation automatically. Continuous operation of the DRV2665 is not recommended. Most haptic use models only operate the DRV2665 in short bursts. The thermal shutdown function will protect the DRV2665 from damage when overdriven, but usage models which drive the DRV2665 into thermal shutdown should always be avoided.

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APPLICATION INFORMATION

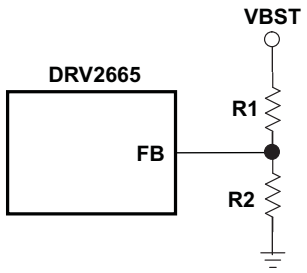
DEVICE STARTUP AND SHUTDOWN

The DRV2665 features a fast startup time, which is essential for achieving low latency in haptic applications. When the STANDBY bit is transitioned from low to high, the device enters a low-power standby mode. When the STANDBY bit is transitioned from high to low, the DRV2665 is ready for operation. The DRV2665 logic will automatically control the internal boost converter and amplifier enable signals. The boost converter and amplifier will be enabled only when needed and will otherwise remain in a lower power idle state. When the DRV2665 receives a data byte via the FIFO interface, the boost converter and amplifier will wake up and the FIFO will send the first sample through the internal DAC after the wake-up is completed. In the system application, the entire system latency should be kept to less than 30 ms total to be imperceptible to the end user. At a 2 ms wake-up time, the DRV2665 will be a small percentage of the total system latency.

If the EN_Override bit is set, the device will immediately enter the startup procedure and the boost converter amplifier will remain enabled, bypassing the internal controls. Subsequent transactions will occur immediately with no wake-up overhead, but the boost converter and amplifier will draw quiescent current until the EN_Override bit is cleared by the user.

PROGRAMMING THE BOOST VOLTAGE

The boost output voltage is programmed via two external resistors as shown in the diagram below.



The boost output voltage is given by Equation 1, where V_{FB} = 1.32 V.

$$V_{BOOST} = V_{FB}\left(1+\frac{R_1}{R_2}\right) \quad (1)$$

V_{BST} should be programmed to a value 5.0 V greater than the largest peak voltage expected in the system to allow adequate amplifier headroom. Since the programming range for the boost voltage extends to 105 V, the leakage current through the resistor divider can become significant. It is recommended that the sum of the resistance of R1 and R2 be greater than 400 kΩ. Note that when resistor values greater than 1 MΩ are used, PCB contamination may cause boost voltage inaccuracy. Exercise caution when soldering large resistances, and clean the area when finished for best results.

R1	R2	GAIN[1:0]	V_{BST}	Full Scale Peak Voltage (V)
402 kΩ	18.2 kΩ	00	30	25
392 kΩ	9.76 kΩ	01	55	50
768 kΩ	13 kΩ	10	80	75
768 kΩ	9.76 kΩ	11	105	100

PROGRAMMING THE BOOST CURRENT LIMIT

The peak current drawn from the supply through the inductor is set solely by the R_{EXT} resistor. Note that this peak current limit is independent of the inductance value chosen, but the inductor should be capable of handling this programmed limit. The relationship of R_{EXT} to I_{LIM} is approximated by Equation 2

$$R_{EXT} = \left(K\frac{V_{REF}}{I_{LIM}}\right) - R_{INT} \quad (2)$$

where K = 10500, V_{REF} = 1.35 V, R_{INT} = 60 Ω, and I_{LIM} is the desired peak current limit through the inductor.

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INDUCTOR SELECTION

Inductor selection plays a critical role in the performance of the DRV2665. The range of recommended inductances is from 3.3 µH to 22 µH. In general, higher inductances within a given manufacturer's inductor series have lower saturation current limits, and vice-versa. When a larger inductance is chosen, the DRV2665 boost converter will automatically run at a lower switching frequency and incur less switching losses; however, larger values of inductance may have higher equivalent series resistance (ESR), which will increase the parasitic inductor losses. Since lower values of inductance generally have higher saturation currents, they are a better choice when attempting to maximize the output current of the boost converter.

PIEZO ACTUATOR SELECTION

There are several key specifications to consider when choosing a piezo actuator for haptics such as dimensions, blocking force, and displacement. However, the key electrical specifications from the driver perspective are voltage rating and capacitance. At the maximum frequency of 500 Hz, the DRV2665 is optimized to drive up to 50 nF at 200 V_{PP}, which is the highest voltage swing capability. It will drive larger capacitances if the programmed boost voltage is lowered and/or the user limits the input frequency range to lower frequencies (e.g. 300 Hz).

BOOST CAPACITOR SELECTION

The boost output voltage may be programmed as high as 105 V. A capacitor with a voltage rating of at least the boost output voltage must be selected. Since ceramic capacitors tend to come in ratings of 100 V or 250 V, a 250 V rated 0.1 µF capacitor of the X5R or X7R type is recommended for the 105 V case. The selected boost capacitor should have a minimum working capacitance of at least 50 nF. For boost voltages from 30 V to 80 V, a 100 V rated or 250 V rated 0.1 µF capacitor is acceptable. For boost voltages less than 30 V, a 50 V, 0.22 µF capacitor is recommended.

LOW-VOLTAGE OPERATION

The lowest gain setting is optimized for 50 V_{PP} with a boost voltage of 30 V. Some applications may not need 50 V_{PP}, so the user may elect to program the boost converter as low as 15 V to improve efficiency. When using boost voltages lower than 30 V, some special considerations are in order. First, to reduce boost ripple to an acceptable level, a 50 V rated, 0.22 µF boost capacitor is recommended. Second, the maximum code range of the digital interface will be limited. For example, the user may elect to program the boost voltage to 25 V, and plan for a maximum drive signal of 40 V_{PP} at the actuator. Any digital code given to the FIFO that is greater than 20 V_P/25 V_P × 127 = ±102 may induce clipping, so the user should only send digital codes between -102 and 102. Use of codes outside this range for this example may clip or drive the actuator beyond its rating.

THERMAL/LAYOUT CONSIDERATIONS

To achieve optimum device performance, use of the thermal footprint outlined by this datasheet is recommended. See land pattern diagram for exact dimensions. The DRV2665 power pad must be soldered directly to the thermal pad on the printed circuit board. The printed circuit board thermal pad should be connected to the ground net with thermal vias to any existing backside/internal copper ground planes. Connection to a ground plane on the top layer near the corners of the device is also recommended. Another key layout consideration is to keep the boost programming resistors (R1 and R2) as close as possible to the FB pin of the DRV2665. Care should be taken to avoid getting the FB trace near the SW trace.

INPUT FILTER CONSIDERATIONS

When using the analog input mode, an input filter may be required depending on the quality of the source signal provided to the DRV2665. Some key factors to consider are whether the source is generated from a DAC or from PWM and the out-of-band content generated. If proper anti-image rejection filtering is used to eliminate image components, the filter can possibly be eliminated depending on the magnitude of the out-of-band components. If PWM is used, at least a 1st order RC filter is required. The PWM sample rate should be greater than 30 kHz to keep the PWM ripple from reaching the piezo element and dissipating unnecessary power. A 2nd order RC filter may be desirable to further eliminate out-of-band signal content to further drive down power dissipation and eliminate audible noise.

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GENERAL I²C OPERATION

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 16 shows a typical sequence. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with a slave device and then waits for an acknowledge condition. The slave device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 16.

Use external pull up resistors for the SDA and SCL signals to set the logic-high level for the bus. Pull up resistors between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2665 supply voltage, VDD.

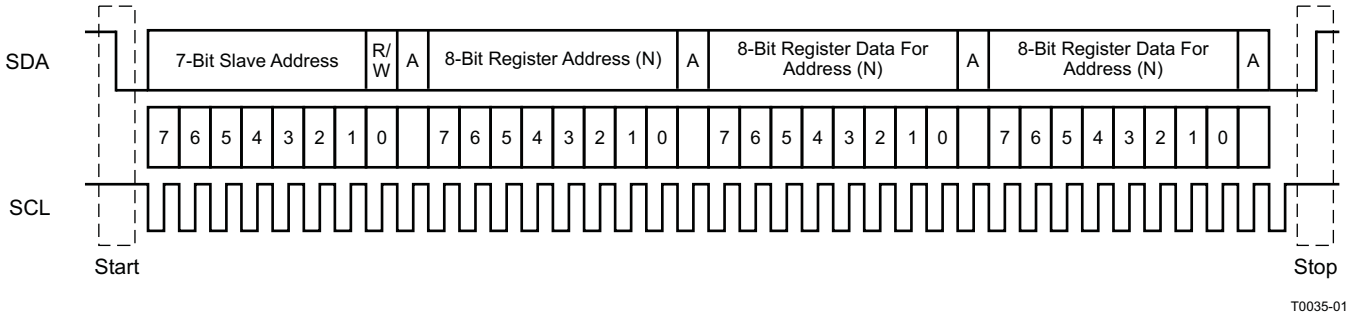


Figure 16. Typical I²C Sequence

The DRV2665 operates as an I²C slave with 1.8 V logic thresholds, but can operate up to the VDD voltage. The device address is 0x59 (7-bit), or 1011001 in binary. This is equivalent to 0xB2 (8-bit) for writing and 0xB3 (8-bit) for reading.

SINGLE-BYTE AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers.

During multiple-byte read operations, the DRV2665 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The DRV2665 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

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SINGLE-BYTE WRITE

As shown in Figure 17, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the DRV2665 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the DRV2665 internal memory address being accessed. After receiving the register byte, the DRV2665 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

The DRV2665 address is 0x59 (7-bit), or 1011001 in binary.

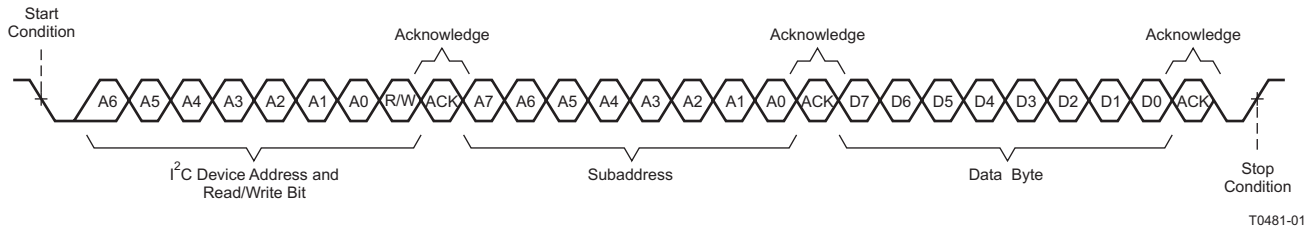


Figure 17. Single-Byte Write Transfer

MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2665 as shown in Figure 18. After receiving each data byte, the DRV2665 responds with an acknowledge bit.

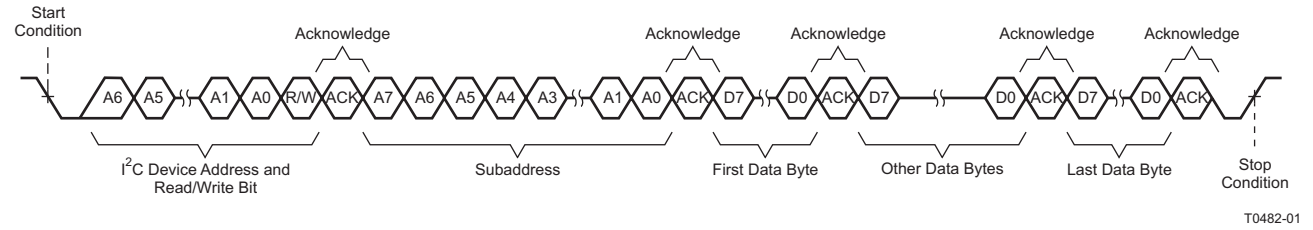


Figure 18. Multiple-Byte Write Transfer

SINGLE-BYTE READ

As shown in Figure 19, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the DRV2665 address and the read/write bit, the DRV2665 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the DRV2665 issues an acknowledge bit. The master device transmits another start condition followed by the DRV2665 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the DRV2665 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

The DRV2665 address is 0x59 (7-bit), or 1011001 in binary.

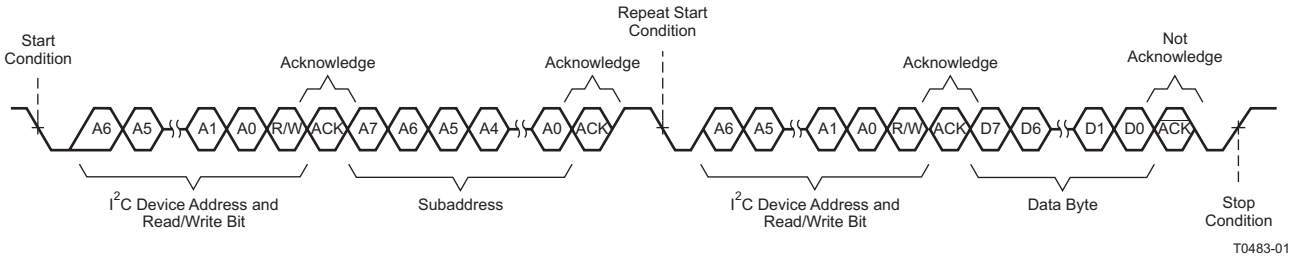


Figure 19. Single-Byte Read Transfer

MULTIPLE-BYTE READ

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2665 to the master device as shown in Figure 20. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

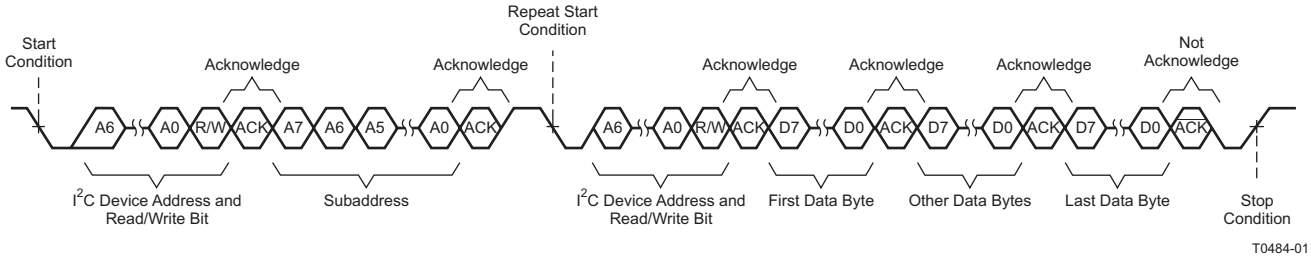


Figure 20. Multiple-Byte Read Transfer

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DEVICE PROGRAMMING

REGISTER MAP

Address	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0x00							FIFOEmpty	FIFOFull
0x01	0x28		ID[3]	ID[2]	ID[1]	ID[0]	Input_MUX	Gain[1]	Gain[0]
0x02	0x40	DEV_RST	STANDBY			Timeout[1]	Timeout[0]	EN_Override	
0x0B	0x00	FIFOData[7]	FIFOData[6]	FIFOData[5]	FIFOData[4]	FIFOData[3]	FIFOData[2]	FIFOData[1]	FIFOData[0]

Status (Address: 0x00)

Bit	7	6	5	4	3	2	1	0
Function							FIFOEmpty	FIFOFull
Type							Read Only	Read Only
Default							1	0

FIFOEmpty — Indicates that the internal, 100-byte FIFO is completely empty

FIFOFull — Indicates that the internal, 100-byte FIFO is full and can not accept data until another byte has played out through the internal DAC. This bit self-clears after being read by the user.

Control (Address: 0x01)

Bit	7	6	5	4	3	2	1	0
Function		ID[3]	ID[2]	ID[1]	ID[0]	Input_MUX	Gain[1]	Gain[0]
Type		Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default		0	1	0	1	0	0	0

ID[3:0] — Identification number for DRV2665.

Input_MUX — 0: FIFO input is selected
1: Analog Input is selected

Gain[1:0] — See "Gain Control" section for gain description

Control 2 (Address: 0x02)

Bit	7	6	5	4	3	2	1	0
Function	DEV_RST	STANDBY			Timeout[1]	Timeout[0]	EN_Override	
Type	Read/Write	Read/Write			Read/Write	Read/Write	Read/Write	
Default	0	1			0	0	0	

DEV_RST — Device Reset. When the DEV_RST bit is set, the device will immediately stop any transaction in process, reset all of its internal registers to their default values as well as put itself in STANDBY mode.

STANDBY — Low-Power Standby
0: Device is active and ready to receive a signal
1: Device is in low-power standby mode

Timeout[1:0] — Time period between when the FIFO runs empty and the DRV2665 goes into idle mode, powering down the boost converter and amplifier.
0: 5 ms
1: 10 ms
2: 15 ms
3: 20 ms

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EN_Override Override bit for the boost converter and amplifier enables
0: Boost converter and amplifier enables are controlled by DRV2665 logic
1: Boost converter and amplifier are enabled indefinitely

FIFO (Address: 0x0B)

Bit	7	6	5	4	3	2	1	0
Function	FIFOData[7]	FIFOData[6]	FIFOData[5]	FIFOData[4]	FIFOData[3]	FIFOData[2]	FIFOData[1]	FIFOData[0]
Type	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default	0	0	0	0	0	0	0	0

FIFOData[7:0] Entry point for FIFO data. The user repeatedly writes this register with continuous haptic waveform data during haptic playback. Multi-byte writes to this register are preferred for optimum performance. Data is interpreted as two's-complement.

Initialization

The DRV2665 features an easy to use interface with a simple initialization procedure.

Initialization Procedure

1. Apply power to DRV2665.
2. Wait for 1 millisecond before attempting an I2C write for the DRV2665 to power up.
3. Exit low-power standby mode by clearing the STANDBY bit (Register 2, Bit[6])
4. If using the digital interface mode, choose the desired timeout period (Register 2, Bit[3:2]).
5. Choose the interface mode, analog or digital (Register 1, Bit[2]), and gain setting (Register 1, Bit[1:0])
6. If using the digital interface mode, the device is now ready to receive data. If using the analog input mode, set the EN_Override bit (Register 2, Bit[1]) to enable the boost and high-voltage amplifier and begin sending the haptic waveform from the source.

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REVISION HISTORY

Changes from Original (May 2012) to Revision A	Page
• Changed from 1 page data sheet to full data sheet in product folder	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV2665RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 70	2665	Samples
DRV2665RGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	-40 to 70	2665	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

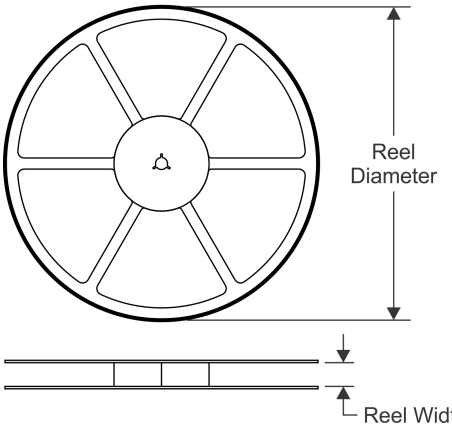
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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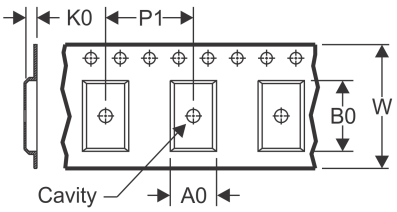
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

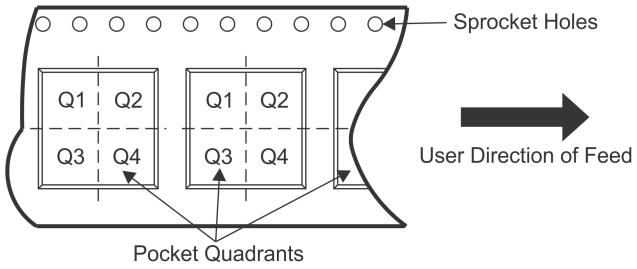


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

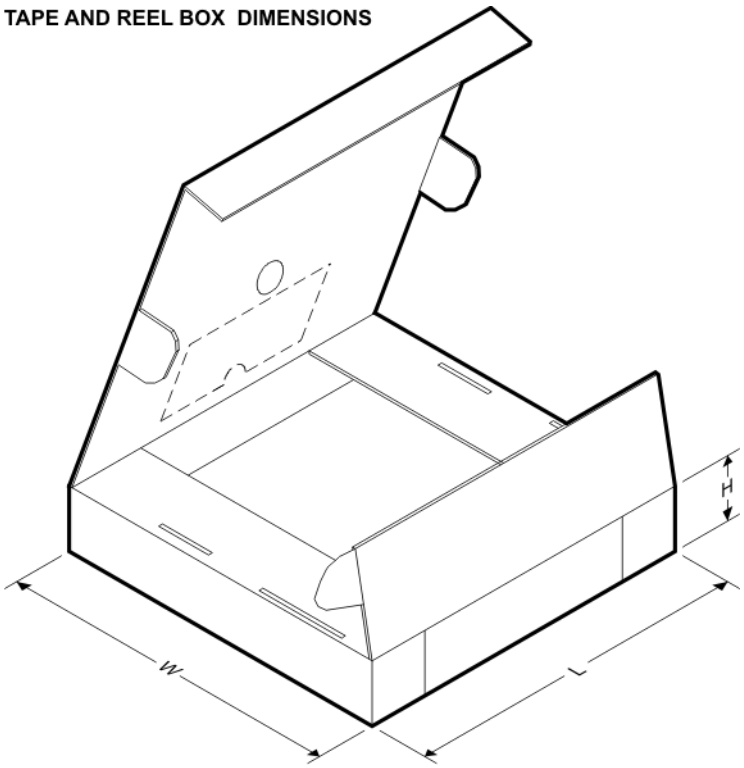
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2665RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV2665RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

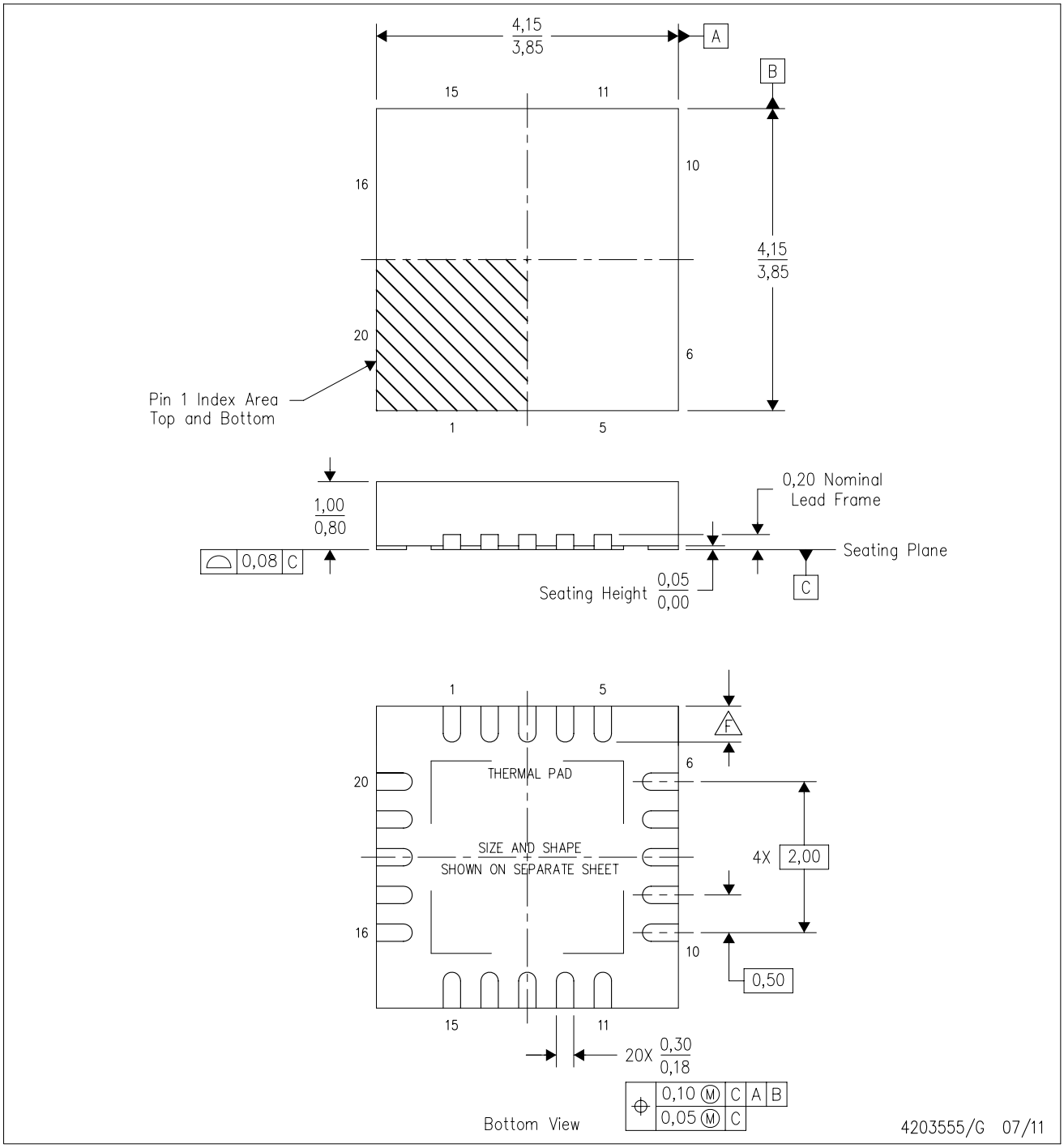
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2665RGPR	QFN	RGP	20	3000	367.0	367.0	35.0
DRV2665RGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

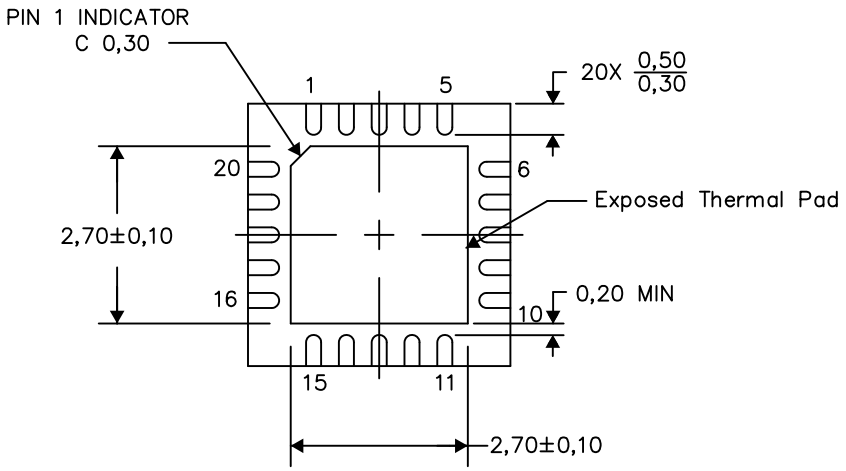
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



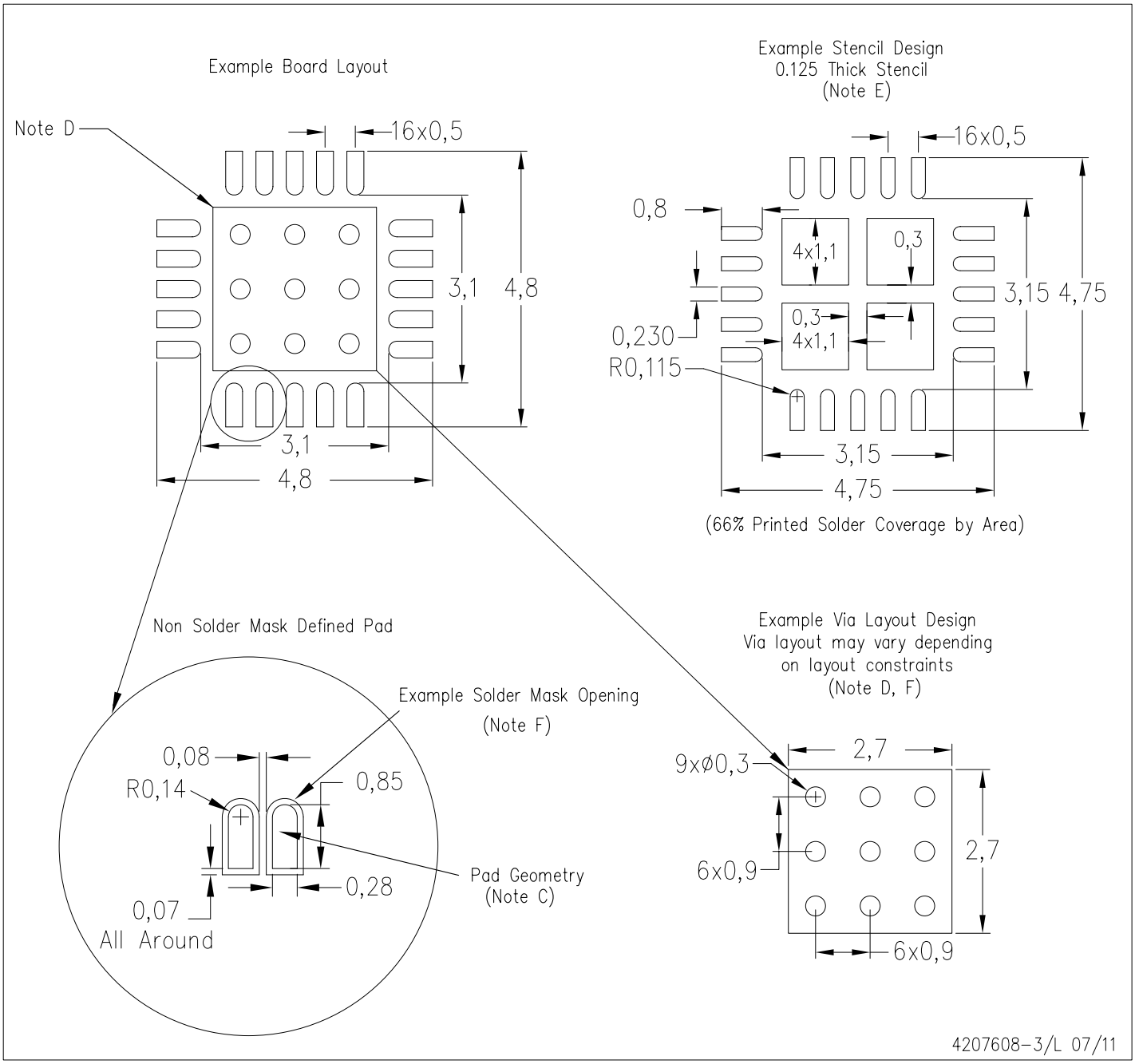
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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