步进电机控制器 IC

查询样品: DRV8818

特性

- 脉宽调制 **(PWM)** 微步进电机驱动器
  - 内置微步进分度器
  - 每绕组高达 **2.5-A** 电流
  - 微步进分度器提供高达 **1/8** 步长运行
  - **0.37Ω (HS + LS)** 低金属氧化物场效应晶体管 **(MOSFET)** 接通电阻（**25°** 时）
  - 可编程混合衰退、消隐和关闭时间
- 对具有较低 R_{ds}（接通）的 **DRV8811** 进行引脚兼容升级
- 耐热增强型表面贴装式封装

应用

- 打印机
- 纺织机械
- 定位/跟踪
- 工厂自动化
- 机器人技术

说明/订购信息

DRV8818 可为打印机、扫描仪以及其它自动化设备应用提供集成型电机驱动器解决方案。 此器件具有两个 H 桥驱动器以及步用于控制步进电机的微步进分度器逻辑。

每个输出驱动器块包含被配置为全 H 桥的 N 通道功率MOSFET 以驱动电机绕组。

一个简单的步进/方向接口可轻松连接到控制器电路。引脚支持按全步进、半步进、四分之一步进或八分之一步进模式配置电机。衰退模式和脉宽调制(PWM) 关闭时间均可编程。

内部关断功能用于实现过流保护、短路保护、欠电压闭锁和过温保护。

DRV8818 采用PowerPAD™ 28 引脚带散热片的薄型小尺寸(HTSSOP) 封装，此封装具有PowerPAD™ （环境 友好：符合RoHS 标准且无铅/无卤素）

订购信息 (1)

封装 (2)		可订购部件号	正面标记
PowerPAD™ (HTSSOP) – PWP	2000 卷带式包装	DRV8818PWPR	DRV8818
	50 管式封装	DRV8818PWP	

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者登录 TI 的网站 www.ti.com.
(2) 封装图样、热数据和符号可登录 www.ti.com/packaging 获取。

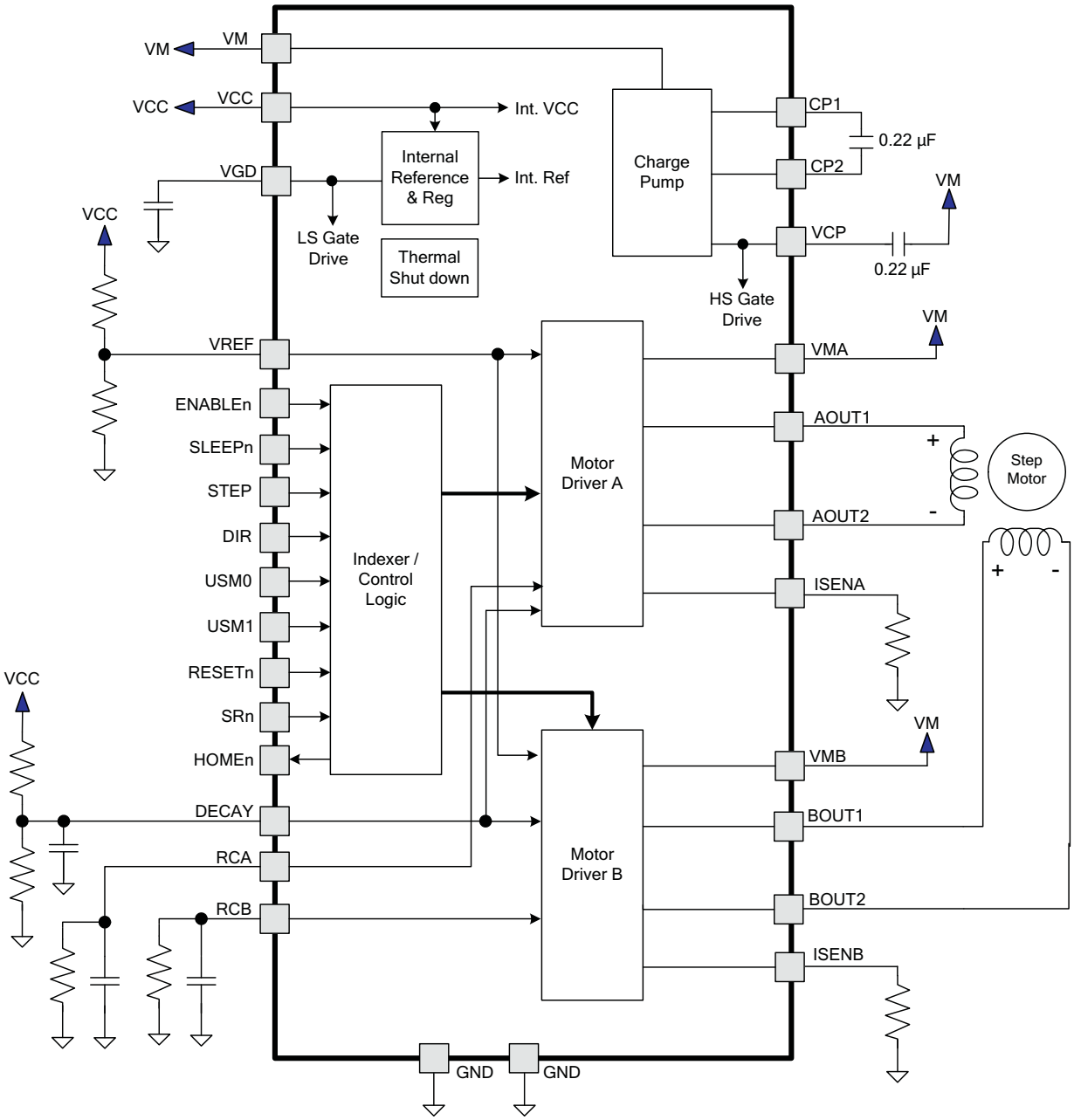
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FUNCTIONAL BLOCK DIAGRAM



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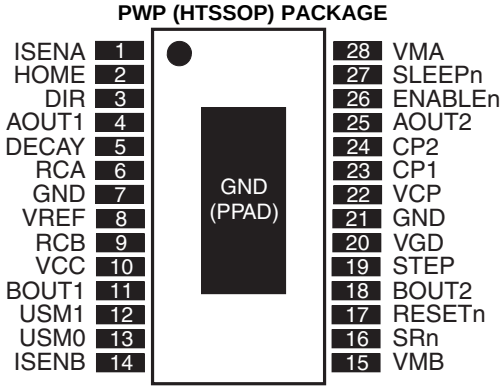
TERMINAL FUNCTIONS

NAME	NO.	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	7, 21	-	Device ground	
VMA	28	-	Bridge A power supply	Connect to motor supply (8 V to 35 V). Both pins must be connected to same supply.
VMB	15	-	Bridge B power supply	Connect to motor supply (8 V to 35 V). Both pins must be connected to same supply.
VCC	10	-	Logic supply voltage	Connect to 3-V to 5-V logic supply. Bypass to GND with a 0.1-µF ceramic capacitor.
CP1	23	IO	Charge pump flying capacitor	Connect a 0.22-µF capacitor between CP1 and CP2.
CP2	24	IO	Charge pump flying capacitor	Connect a 0.22-µF capacitor between CP1 and CP2.
VCP	22	IO	High-side gate drive voltage	Connect a 0.22-µF ceramic capacitor to V_M.
VGD	20	IO	Low-side gate drive voltage	Bypass to GND with a 0.22-µF ceramic capacitor.
CONTROL				
ENABLEn	26	I	Enable input	Logic high to disable device outputs, logic low to enable outputs. Weak internal pullup to VCC.
SLEEPn	27	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Weak internal pulldown.
DECAY	5	I	Decay mode select	Voltage applied sets decay mode - see motor driver description for details. Bypass to GND with a 0.1-µF ceramic capacitor. Weak internal pulldown.
STEP	19	I	Step input	Rising edge causes the indexer to move one step. Weak internal pulldown.
DIR	3	I	Direction input	Level sets the direction of stepping. Weak internal pulldown.
USM0	13	I	Microstep mode 0	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step. Weak internal pulldown.
USM1	12	I	Microstep mode 1	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step. Weak internal pulldown.
RESETn	17	I	Reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs. Weak internal pullup to VCC.
SRn	16	I	Sync. Rect. enable input	When active low, synchronous rectification is enabled. Weak internal pulldown.
VREF	8	I	Current set reference input	Reference voltage for winding current set
RCA	6	I	Bridge A blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details.
RCB	9	I	Bridge B blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details.
ISENA	1	-	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	14	-	Bridge B ground / Isense	Connect to current sense resistor for bridge B
OUTPUTS				
AOUT1	4	O	Bridge A output 1	Connect to bipolar stepper motor winding
AOUT2	25	O	Bridge A output 2	Positive current is AOUT1 → AOUT2
BOUT1	11	O	Bridge B output 1	Connect to bipolar stepper motor winding
BOUT2	18	O	Bridge B output 2	Positive current is BOUT1 → BOUT2
HOMEn	2	O	Home position	Logic low when at home state of step table, logic high at other states

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output

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PWP (HTSSOP) PACKAGE



ABSOLUTE MAXIMUM RATINGS(1) (2) (3)

		MIN	MAX	UNIT
V_{MX}	Power supply voltage range	–0.3	35	V
V_{CC}	Power supply voltage range	–0.3	7	V
	Digital pin voltage range	–0.5	7	V
V_{REF}	Input voltage range	–0.3 V	V_{CC}	V
	ISENSEx pin voltage range	–0.3	0.5	V
$I_{O(peak)}$	Peak motor drive output current	Internally limited		
P_D	Continuous total power dissipation	See Thermal Information table		
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–60	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8818 PWP 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	32.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	16.3	
θ_{JB}	Junction-to-board thermal resistance(4)	14	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	13.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	8		35	V
V_{CC}	Logic power supply voltage range	3		5.5	V
V_{REF}	VREF input voltage	0		V_{CC}	V
R_X	R_X resistance value	12	56	100	kΩ
C_X	C_X capacitance value	470	680	1500	pF

(1) All V_M pins must be connected to the same supply voltage.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
I_{VM}	V_M operating supply current	V_M = 35 V, f_{PWM} < 50 KHz		7	10	mA
I_{VCC}	V_{CC} operating supply current	f_{PWM} < 50 KHz		0.4	4	mA
I_{VMQ}	V_M sleep mode supply current	V_M = 35 V		3	20	µA
I_{VCCQ}	V_{CC} sleep mode supply current			0.5	20	µA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.7	7.5	V
	V_{CC} undervoltage lockout voltage	V_{CC} rising		2.75	2.95	
VREF Input/Current Control Accuracy						
I_{REF}	VREF input current	VREF = 3.3 V	–3		3	µA
ΔI_{CHOP}	Chopping current accuracy	VREF = 2.0 V, 70% to 100% current	–5		5	%
		VREF = 2.0 V, 20% to 56% current	–10		10	%
Logic-Level Inputs						
V_{IL}	Input low voltage				0.3 × V_{CC}	V
V_{IH}	Input high voltage		0.7 × V_{CC}			V
V_{HYS}	Input hysteresis			300		mV
I_{IL}	Input low current	VIN = 0.3 × V_{CC}	–20		20	µA
I_{IH}	Input high current	VIN = 0.3 × V_{CC}	–20		20	µA
R_{PU}	Pullup resistance			1		MΩ
R_{PD}	Pulldown resistance			1		MΩ
HOMEn Output						
V_{OL}	Output low voltage	I_O = 200 µA			0.3 × VCC	V
V_{OH}	Output high voltage	I_O = –200 µA	0.7 × VCC			V
Decay Input						
V_{IL}	Input low threshold voltage	For fast decay mode		0.21 × VCC		V
V_{IH}	Input high threshold voltage	For slow decay mode		0.6 × VCC		V
H-Bridge FETS						
$R_{ds(on)}$	HS FET on resistance	V_M = 24 V, I_O = 2.5 A, T_J = 25°C		0.22	0.30	Ω
$R_{ds(on)}$	LS FET on resistance	V_M = 24 V, I_O = 2.5 A, T_J = 25°C		0.15	0.24	Ω
I_{OFF}			–20		20	µA
Motor Driver						
t_{OFF}	Off time	Rx = 56 kΩ, Cx = 680 pF	35	44	53	µs
t_{BLANK}	Current sense blanking time	Rx = 56 kΩ, Cx = 680 pF	900	1250	1500	ns
t_{DT}	Dead time	SRn = 0	100	475	800	ns
t_R	Rise time		10		80	ns
t_F	Fall time		10		80	ns

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ELECTRICAL CHARACTERISTICS (continued)

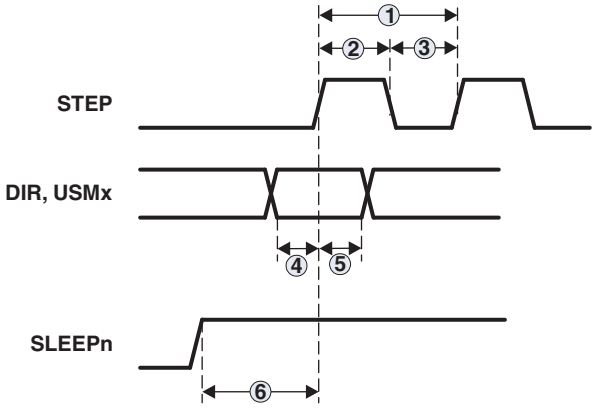
T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Protection Circuits						
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
I_{OCP}	Overcurrent protection level		3.5			A
t_{OCP}	OCP deglitch time			1.5		µs
t_{RET}	OCP retry time			800		µs

TIMING REQUIREMENTS

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
f_{STEP}	Step frequency		500	kHz
$t_{WH(STEP)}$	Pulse duration, STEP high	1		µs
$t_{WL(STEP)}$	Pulse duration, STEP low	1		µs
$t_{SU(STEP)}$	Setup time, command to STEP rising	200		ns
$t_{H(STEP)}$	Hold time, command to STEP rising	200		ns
t_{WAKE}	Wakeup time, SLEEPn inactive to STEP	1.5		ms



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FUNCTIONAL DESCRIPTION

PWM H-Bridge Drivers

DRV8818 contains two H-bridge motor drivers with current-control PWM circuitry, and a microstepping indexer. A block diagram of the motor control circuitry is shown below.

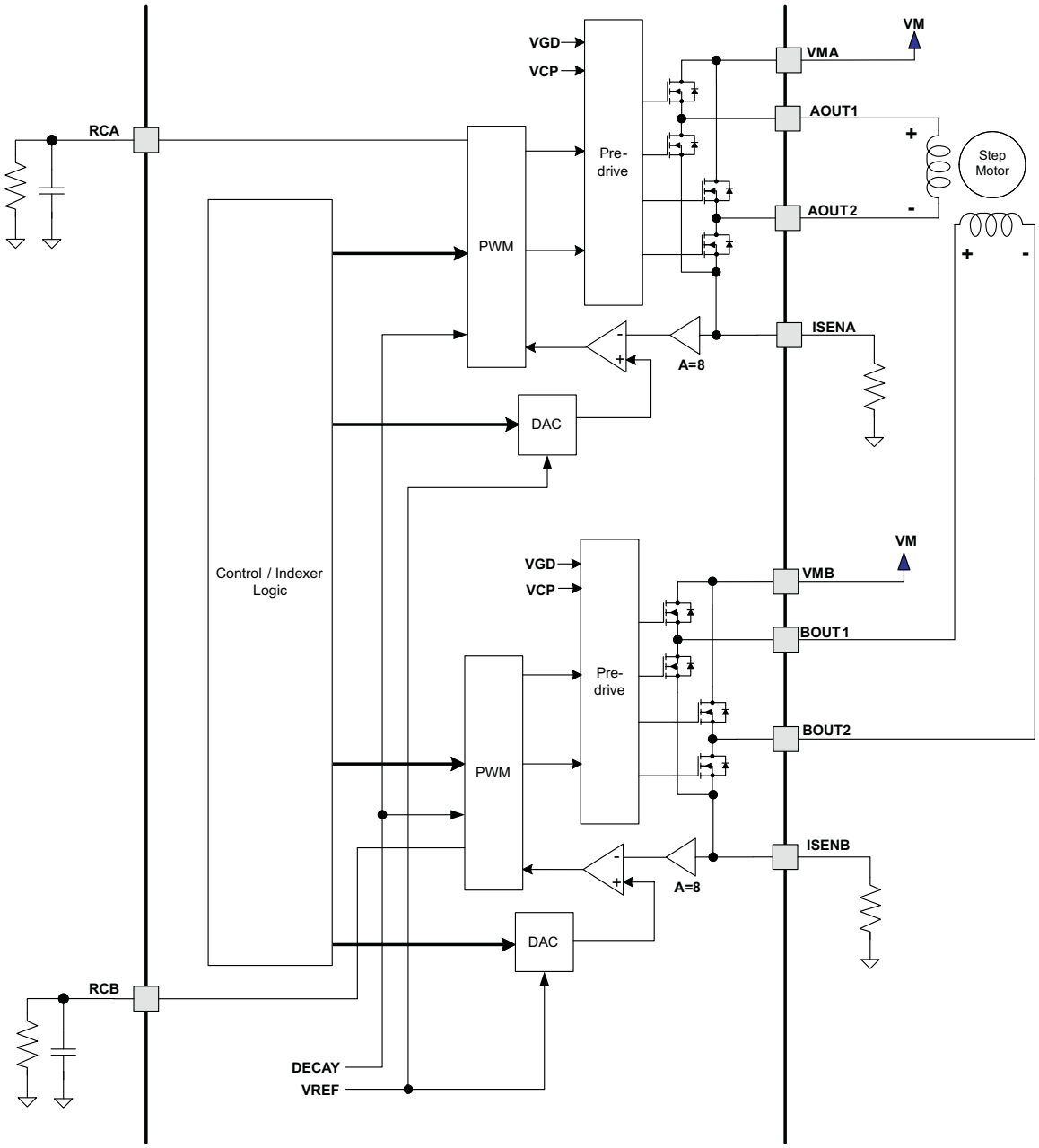


Figure 1. Motor Control Circuitry

Current Regulation

The PWM chopping current is set by a comparator, which compares the voltage across a current sense resistor, multiplied by a factor of 8, with a reference voltage. The reference voltage is input from the VREF pin. The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{8 \bullet R_{ISENSE}} \quad (1)$$

Example:

If a 0.22-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current is 3.3 V/(8 * 0.22 Ω) = 1.875 A.

The reference voltage is also scaled by an internal DAC that allows torque control for fractional stepping of a bipolar stepper motor, as described in the "Microstepping Indexer" section below.

When a winding is activated, the current through it rises until it reaches the chopping current threshold described above, then the current is switched off for a fixed off time. The off time is determined by the values of a resistor and capacitor connected to the RCA (for bridge A) and RCB (for bridge B) pins. The off time is approximated by:

$$t_{OFF} = R \bullet C \quad (2)$$

To avoid falsely tripping on transient currents when the winding is first activated, a blanking period is used immediately after turning on the FETs, during which the state of the current sense comparator is ignored. The blanking time is determined by the value of the capacitor connected to the RCx pin and is approximated by:

$$t_{BLANK} = 1400 \bullet C \quad (3)$$

Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 2, Item 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If synchronous rectification is enabled (SRn pin logic low), the opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. If SRn is high, current is recirculated through the body diodes, or through external Schottky diodes. Fast-decay mode is shown in Figure 2, Item 2.

In slow-decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 2, Item 3.

If SRn is high, current is recirculated only through the body diodes, or through external Schottky diodes. In this case fast decay is always used.

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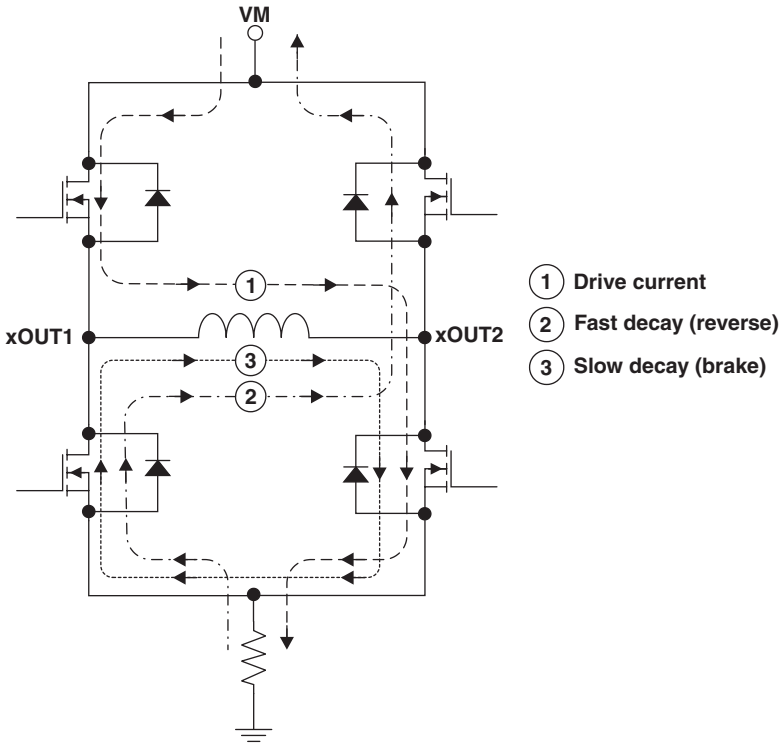


Figure 2. Decay Mode

The DRV8818 also supports a mixed decay mode. Mixed decay mode begins as fast decay, but after a period of time switches to slow decay mode for the remainder of the fixed off time.

Fast and mixed decay modes are only active if the current through the winding is decreasing; if the current is increasing, then slow decay is always used.

Which decay mode is used is selected by the voltage on the DECAY pin. If the voltage is greater than 0.6 x V_{CC}, slow decay mode is always used. If DECAY is less than 0.21 x V_{CC}, the device operates in fast decay mode when the current through the winding is decreasing. If the voltage is between these levels, mixed decay mode is enabled.

In mixed decay mode, the voltage on the DECAY pin sets the point in the cycle that the change to slow decay mode occurs. This time can be approximated by:

$$t_{FD} = R \bullet C \bullet ln\left(\frac{0.6 \bullet V_{CC}}{V_{DECAY}}\right) \quad (4)$$

Mixed decay mode is only used while the current though the winding is decreasing; slow decay is used while the current is increasing.

Operation of the blanking, fixed off time, and mixed decay mode is illustrated in Figure 3.

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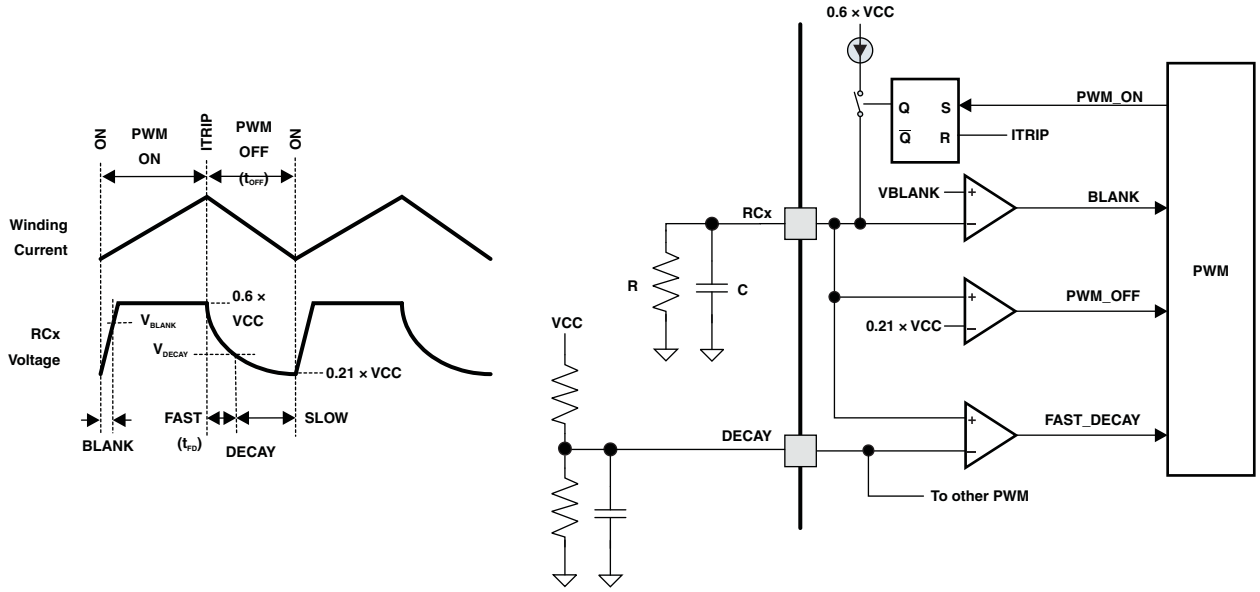


Figure 3. PWM

Microstepping Indexer

Built-in indexer logic in the DRV8818 allows a number of different stepping configurations. The USM1 and USM0 pins are used to configure the stepping format as shown in the table below:

USM1	USM0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	1/2 step (1-2 phase excitation)
1	0	1/4 step (W1-2 phase excitation)
1	1	Eight microsteps/steps

The following table shows the relative current and step directions for different settings of USM1 and USM0. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that the home state is 45 degrees. This state is entered at power-up or device reset. The HOMEn output pin is driven low in this state. In all other states it is driven logic high.

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FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	1	1	1	100	0	0
			2	98	20	11.325
		2	3	92	38	22.5
			4	83	56	33.75
1	2	3	5	71	71	45 (home state)
			6	56	83	56.25
		4	7	38	92	67.5
			8	20	98	78.75
	3	5	9	0	100	90
			10	–20	98	101.25
		6	11	–38	92	112.5
			12	–56	83	123.75
2	4	7	13	–71	71	135
			14	–83	56	146.25
		8	15	–92	38	157.5
			16	–98	20	168.75
	5	9	17	–100	0	180
			18	–98	–20	191.25
		10	19	–92	–38	202.5
			20	–83	–56	213.75
3	6	11	21	–71	–71	225
			22	–56	–83	236.25
		12	23	–38	–92	247.5
			24	–20	–98	258.75
	7	13	25	0	–100	270
			26	20	–98	281.25
		14	27	38	–92	292.5
			28	56	–83	303.75
4	8	15	29	71	–71	315
			30	83	–56	326.25
		16	31	92	–38	337.5
			32	98	–20	348.75

RESETn, ENABLEn and SLEEPn Operation

The RESETn pin, when driven active low, resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while RESETn is active.

The ENABLEn pin is used to control the output drivers. When ENABLEn is low, the output H-bridges are enabled. When ENABLEn is high, the H-bridges are disabled and the outputs are in a high-impedance state.

Note that when ENABLEn is high, the input pins and control logic, including the indexer (STEP and DIR pins) are still functional.

The SLEEPn pin is used to put the device into a low power state. If SLEEPn is low, the H-bridges are disabled, the gate drive charge pump is stopped, and all internal clocks are stopped. In this state all inputs are ignored until the SLEEPn pin returns high.

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Protection Circuits

Overcurrent Protection (OCP)

If the current through any FET exceeds the preset overcurrent threshold, all FETs in the H-bridge will be disabled for a period of approximately 800 µs, or until the ENABLEn pin has been brought inactive high and then back low, or power is removed and re-applied. Overcurrent conditions are sensed in both directions; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Note that overcurrent protection does not use the current sense circuitry used for PWM current control and is independent of the Isense resistor value or VREF voltage.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down and the indexer is reset to the home state. Once the die temperature has fallen to a safe level operation resumes.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM or VCC pins falls below the VM or VCC undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and the indexer will be reset to the home state. Operation will resume when VM and VCC both rise above their UVLO thresholds.

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THERMAL INFORMATION

Thermal Protection

The DRV8818 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8818 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = 4 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (5)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the DRV8818 is dependent on ambient temperature and heatsinking. The thermal dissipation ratings table in the datasheet can be used to estimate the temperature rise for typical PCB constructions.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI Application Report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI Application Brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8818PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818	Samples
DRV8818PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8818	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

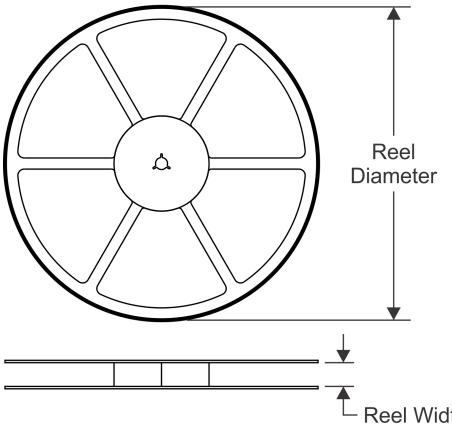
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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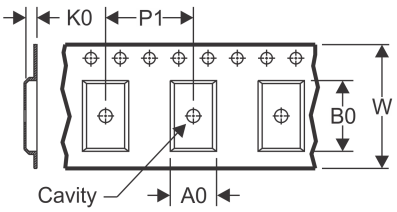
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

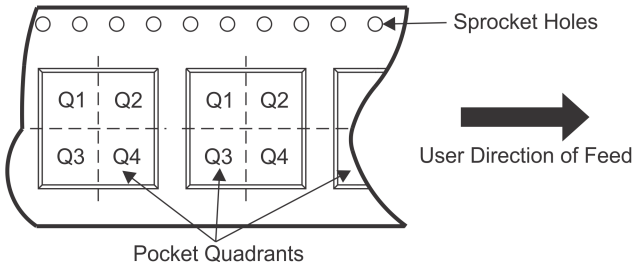


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

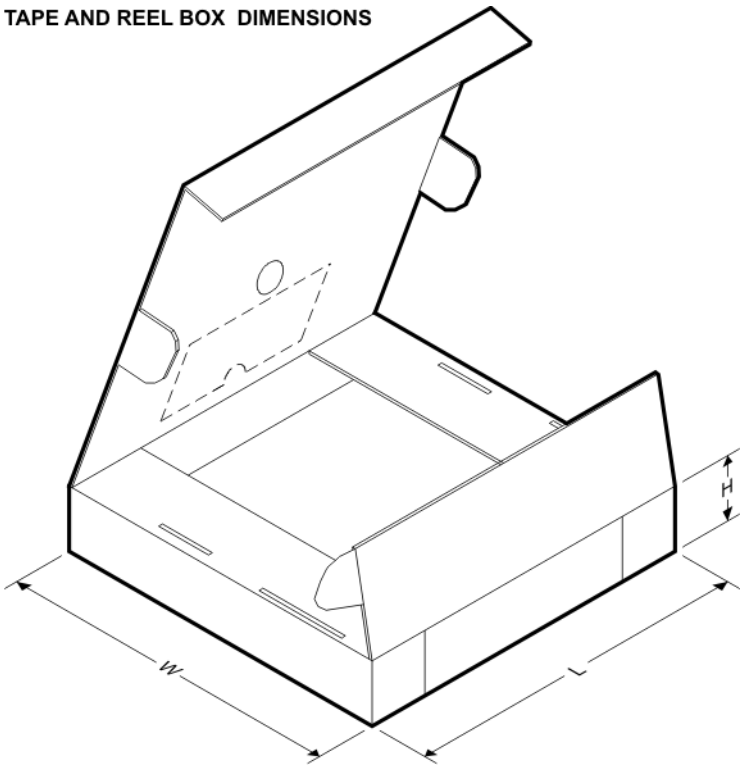
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8818PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8818PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

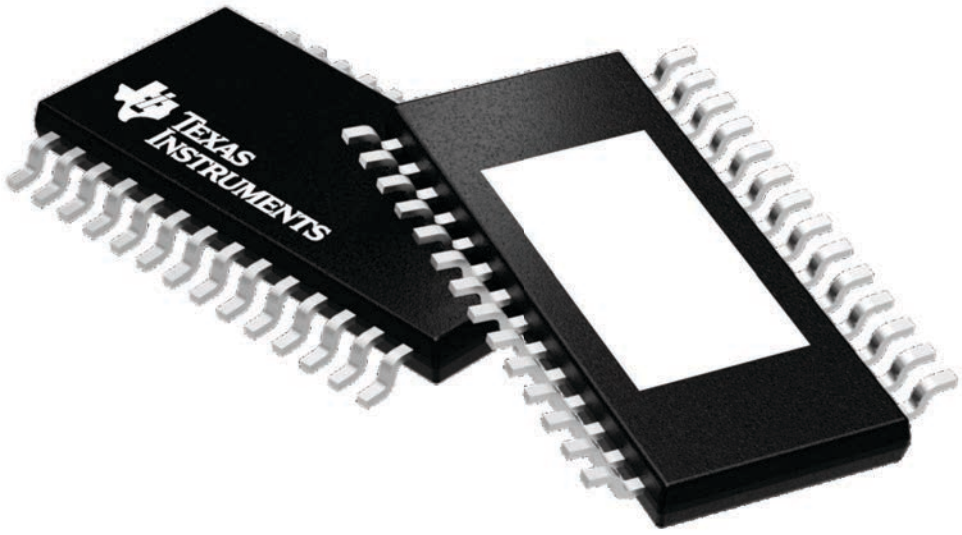
GENERIC PACKAGE VIEW

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

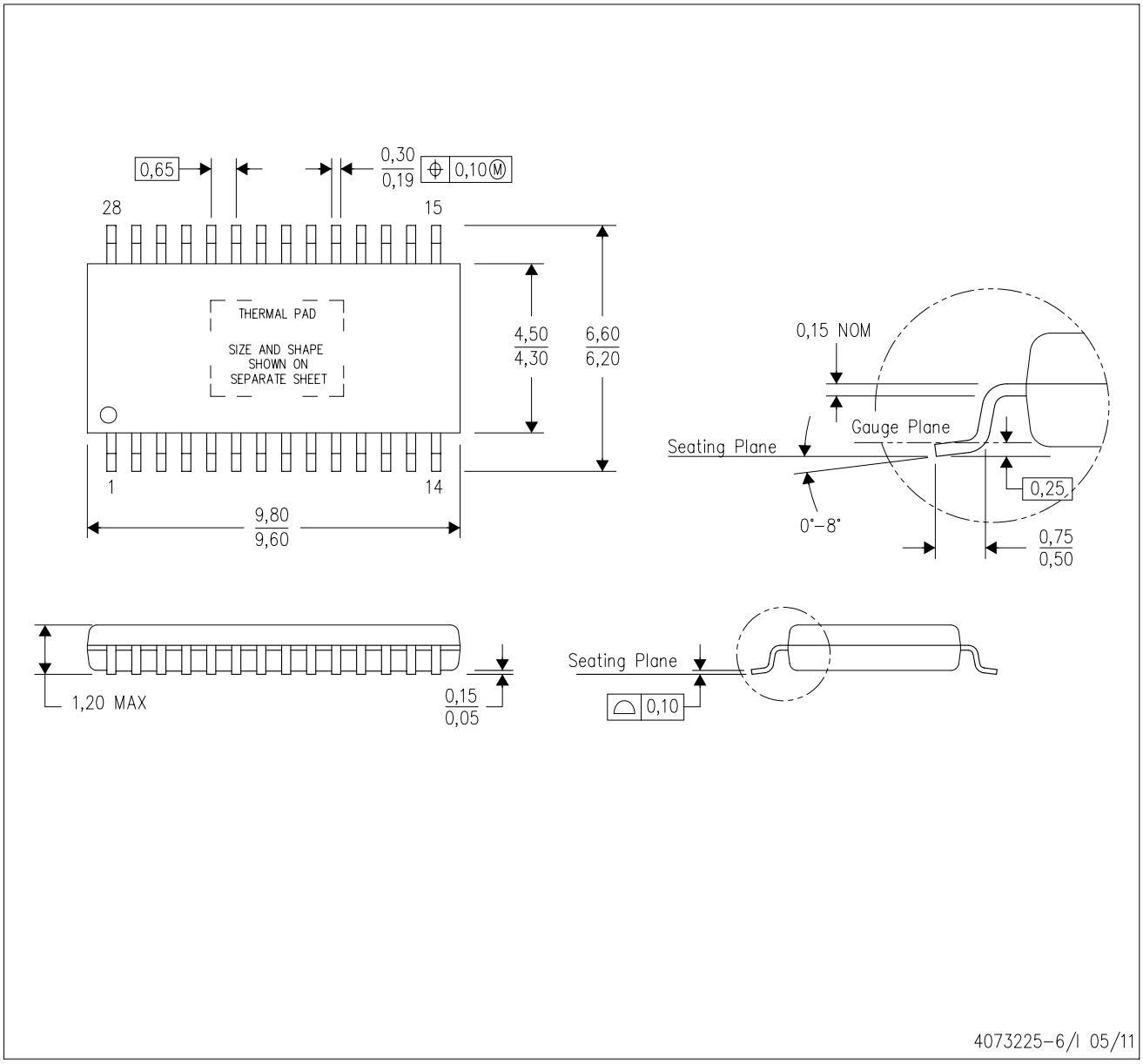
SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/A

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

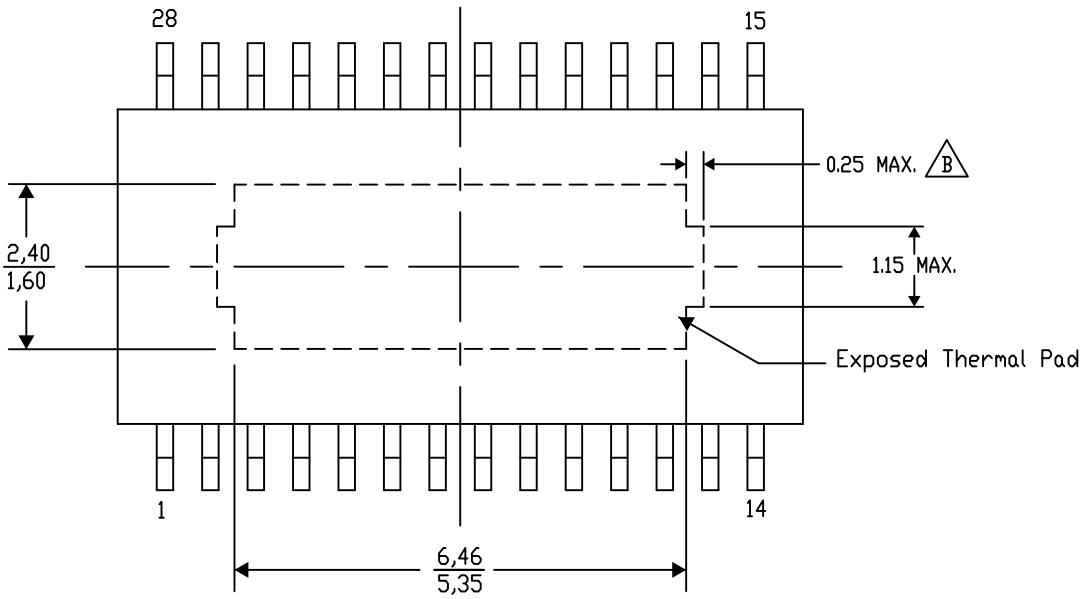
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

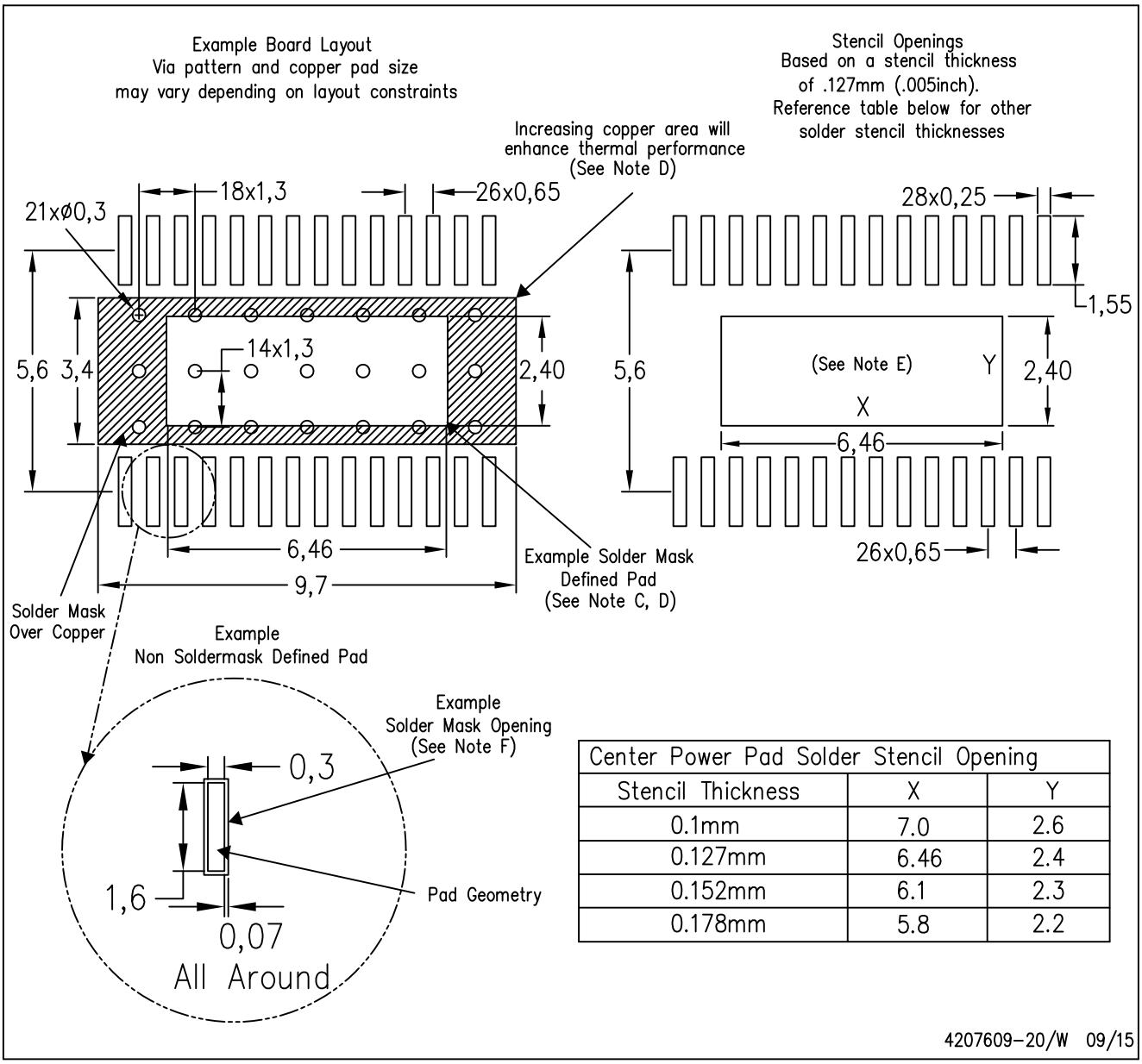
4206332–34/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.0	2.6
0.127mm	6.46	2.4
0.152mm	6.1	2.3
0.178mm	5.8	2.2

4207609–20/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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