具有互锁功能的 UCC27712-Q1 汽车类 620V、1.8A、2.8A 高侧低侧栅极驱动器

1 特性

- 符合面向汽车应用的 AEC-Q100标准
  - 器件 HBM 分类等级 1C
  - 器件 CDM 分类等级 C4B
- 高侧和低侧配置
- 双输入，带输出互锁和 150ns 死区时间
- 在高达 620V 的电压下完全可正常工作，HB 引脚上的绝对最高电压为 700V
- VDD 建议范围为 10V 至 20V
- 峰值输出电流 2.8A 灌电流、1.8A 拉电流
- 50V/ns 的 dv/dt 抗扰度
- HS 引脚上的逻辑运行电压高达 –11V
- 输入负电压容差为 –5V
- 大型负瞬态安全工作区
- 为两个通道提供 UVLO 保护
- 短传播延迟（典型值 100ns）
- 延迟匹配（典型值 12ns）
- 低静态电流
- TTL 和 CMOS 兼容输入
- 行业标准 SOIC-8 封装
- 所有参数额定温度范围：–40°C 至 +125°C

2 应用

- 汽车逆变器
- 车载充电器（PFC，移相全桥）
- 用于汽车应用的 电机驱动 （步进电机、风扇）

3 说明

UCC27712-Q1 是一款 620V 高侧和低侧栅极驱动器，具有 1.8A 拉电流、2.8A 灌电流能力，专用于驱动功率 MOSFET 或 IGBT。

对于 IGBT，建议的 VDD 工作电压为 10V 至 20V，对于功率 MOSFET，建议的 VDD 工作电压为 10V 至 17V。

UCC27712-Q1 包含保护 功能， 在此情况下，当输入保持开路状态时，或当未满足最低输入脉宽规范时，输出保持低位。互锁和死区时间功能可防止两个输出同时打开。此外，该器件可接受的偏置电源范围宽幅达 10V 至 22V，并且为 VDD 和 HB 偏置电源提供了 UVLO 保护。

该器件采用 TI 先进的高压器件技术， 具有 强大的驱动器，拥有卓越的噪声和瞬态抗扰度，包括较大的输入负电压容差、高 dV/dt 容差、开关节点上较宽的负瞬态安全工作区 (NTSOA)，以及互锁。

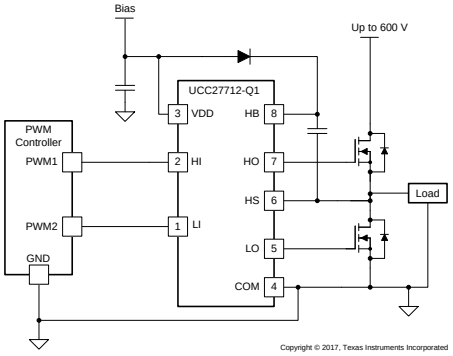
该器件包含一个接地基准通道 (LO) 和一个悬空通道 (HO)，后者专用于自举电源或隔离式电源操作。该器件 具有 快速传播延迟和两个通道之间卓越的延迟匹配。在 UCC27712-Q1 上，每个通道均由其各自的输入引脚 HI 和 LI 控制。

器件信息(1)

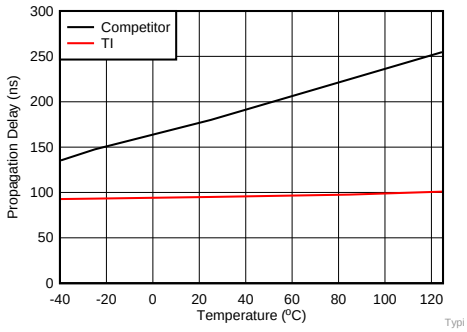
器件型号	封装	封装尺寸（标称值）
UCC27712-Q1	SOIC (8)	3.91mm × 8.65mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



典型传播延迟比较



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4 修订历史记录

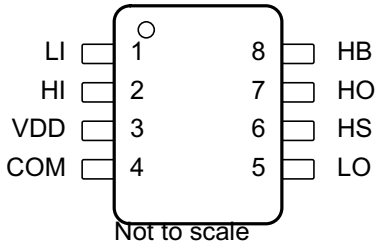
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2017 年 8 月	*	初始发行版。

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5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COM	4	–	Ground
HB	8	I	High-side floating supply. Bypass this pin to HS with a suitable capacitor to sustain boot-strap circuit operation, typically 10 times bigger than the MOSFETs/IGBTs gate capacitance.
HI	2	I	Logic input for high-side driver. If HI is unbiased or floating, HO is held low
HO	7	O	High-side driver output.
HS	6	–	Return for high-side floating supply.
LI	1	I	Logic input for low-side driver. If LI is unbiased or floating, LO is held low
LO	5	O	Low-side driver output.
VDD	3	I	Bias supply input. Power supply for the input logic side of the device and also low-side driver output. Bypass this pin to COM with a 0.1-µF or larger value ceramic capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to COM (unless otherwise noted), currents are positive into and negative out of the specified terminal.(1)

PARAMETER			MIN	MAX	UNIT
Input voltage	HI, LI (2)		–5	22	V
	VDD supply voltage		–0.3	22	
	HB		–0.3	700	
	HB–HS		–0.3	22	
Output voltage	HO	DC	HS–0.3	HB+0.3	V
		Transient, less than 100 ns(3)	HS–2	HB+0.3	
	LO	DC	–0.3	VDD+0.3	V
		Transient, less than 100 ns(3)	–2	VDD+0.3	
Output current	HO, LO	I_{OUT_PULSED} (100 ns)		2.8/–1.8	A
		I_{OUT_DC}		0.15	
dV_{HS}/dt	Allowable offset supply voltage transient		–50	50	V/ns
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum voltage on the input pins is not restricted by the voltage on the VDD pin
(3) Values are verified by characterization on bench.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±1500	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

All voltages are with respect to COM, over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	IGBT applications	10		20	V
		MOSFET applications	10		17	
HB–HS	Driver bootstrap voltage	IGBT applications	10		20	
		MOSFET applications	10		17	
HS	Source terminal voltage (1)		–11		600	
HI, LI	Input voltage with respect to COM		–4		20	
T_A	Ambient temperature		–40		125	°C

(1) Logic operational for HS of –11 V to +600 V at HB–HS = 15 V

6.4 Thermal Information

THERMAL METRIC (1)		UCC27712-Q1 (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At VDD = VHB = 15 V, COM = VHS = 0, all voltages are with respect to COM, no load on LO and HO, –40°C < T_J < +125°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY BLOCK						
$V_{VDD\ ON}$	Turn-on threshold voltage of VDD		8.0	8.9	9.8	V
$V_{VDD\ OFF}$	Turn-off threshold voltage of VDD		7.5	8.4	9.3	
$V_{VDD\ HYS}$	Hysteresis of VDD			0.5		
$V_{VHB\ ON}$	Turn-on threshold voltage of VHB–VHS		7.2	8.2	9.2	
$V_{VHB\ OFF}$	Turn-off threshold voltage of VHB–VHS		6.4	7.3	8.3	
$V_{VHB\ HYS}$	Hysteresis of VHB–VHS		0.5	0.9		
I_Q	Total quiescent supply current	HI = LI = 0 V or 5 V, DC on/off state	180	255	420	µA
I_{QVDD}	Quiescent VDD-COM supply current	HI = LI = 0 V or 5 V, DC on/off state		190	320	
I_{QBS}	Quiescent HB-HS supply current	HI = 0 V or 5 V, HO in DC on/off state		65	100	
I_{BL}	Bootstrap supply leakage current	HB = HS = 600 V			20	
I_{OP}	Dynamic operating current	HI = LI = 0 V or 5 V, f = 100 kHz, duty = 50%, C_L= 1 nF		3800 (1)	4500	

(1) Ensured by design, not tested in production

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Electrical Characteristics (continued)

At VDD = VHB = 15 V, COM = VHS = 0, all voltages are with respect to COM, no load on LO and HO, –40°C < T_J < +125°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT BLOCK						
V_{INH}	Input Pin (HI, LI) high threshold		1.6	2.0	2.4	V
V_{INL}	Input Pin (HI, LI) low threshold		0.8	1.2	1.5	
V_{INHYS}	Input Pin (HI, LI) threshold hysteresis			0.8		
I_{INL}	HI, LI input low bias current	HI, LI = 0 V	–5	0	5	µA
I_{INH}	HI, LI input high bias current	HI, LI = 5 V	1.7		70	
OUTPUT BLOCK						
V_{DD}-V_{LOH}	LO output high voltage	LI = 5 V, I_{LO} = –20 mA		60	136	mV
V_{HB}-V_{HOH}	HO output high voltage	HI = 5 V, I_{HO} = –20 mA		60	136	
V_{LOL}	LO output low voltage	LI = 0 V, I_{LO} = 20 mA		30	80	
V_{HOL}	HO output low voltage	HI = 0 V, I_{HO} = 20 mA		30	80	
R_{LOL}, R_{HOL}	LO, HO output pull-down resistance	I_{LO} = I_{HO} = 20 mA		1.5	4	Ω
R_{LOH}, R_{HOH}	LO, HO output pull-up resistance	I_{LO} = I_{HO} = –20 mA		3.0	6.8	
I_{GPK-} (1)	HO, LO output low short circuit pulsed current	HI = LI = 0 V, HO = LO = 15 V, PW < 10 µs		2.8		A
I_{GPK+} (1)	HO, LO output high short circuit pulsed current	HI = LI = 5 V, HO = LO = 0 V, PW < 10 µs		–1.8		

6.6 Dynamic Electrical Characteristics

At VDD = VHB = 15 V, COM = VHS = 0, all voltages are with respect to COM, no load on LO and HO, –40°C < T_J < +125°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DYNAMIC CHARACTERISTICS						
t_{PDLH}	Turn-on propagation delay (without deadtime)	LI to LO, HI to HO, HS = COM = 0 V		100	160	ns
t_{PDHL}	Turn-off propagation delay	LI to LO, HI to HO, HS = COM = 0 V		100	160	
t_{PDRM}	Low-to-high delay matching			5	30	
t_{PDFM}	High-to-low delay matching			12	30	
t_{RISE}	Turn-on rise time	10% to 90%, HO/LO with 1000-pF load		16	50	
t_{FALL}	Turn-off fall time	10% to 90%, HO/LO with 1000-pF load		10	30	
t_{ON}	Minimum HI/LI ON pulse that changes output state	0-V to 5-V input signal on HI and LI pins		25	45	
t_{OFF}	Minimum HI/LI OFF pulse that changes output state	5-V to 0-V input signal on HI and LI pins		35	45	
DT	Deadtime	Internal deadtime for Interlock	100	150	200	

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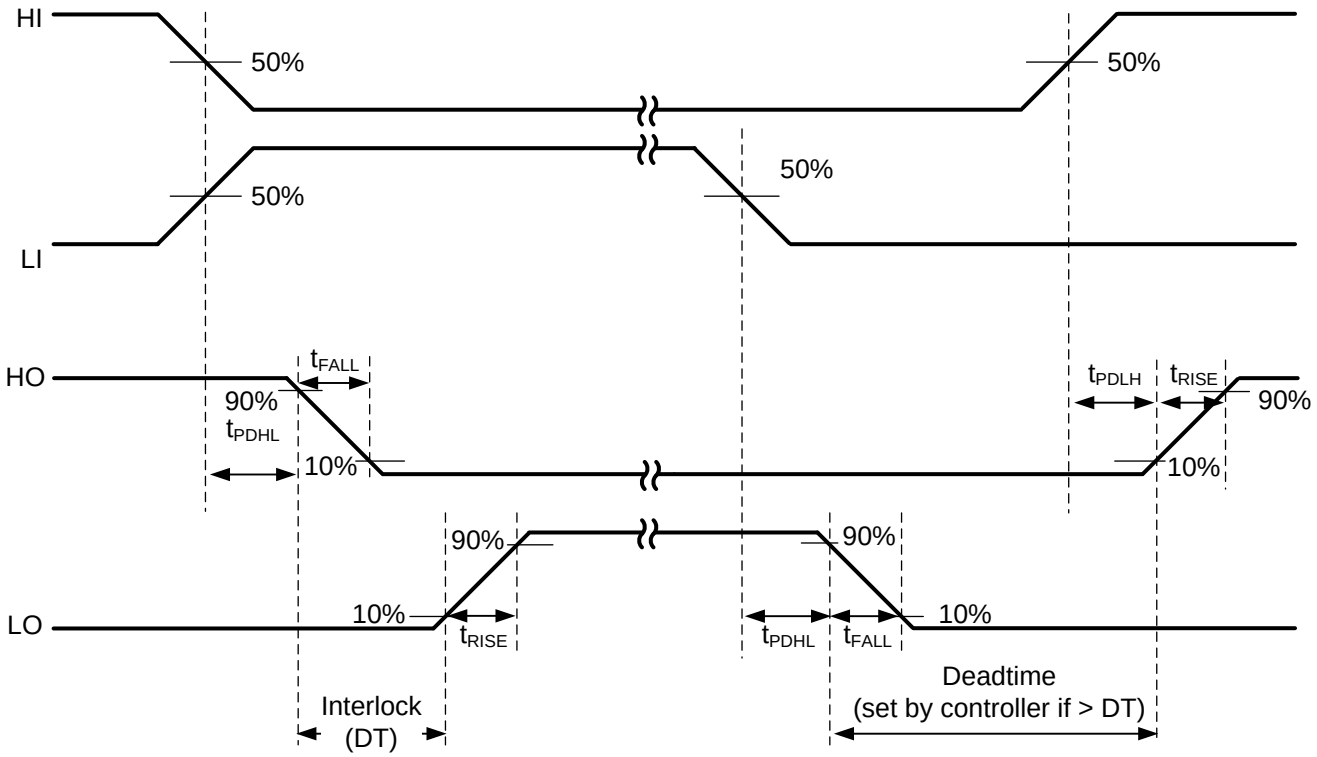


图 1. Typical Test Timing Diagram

6.7 Typical Characteristics

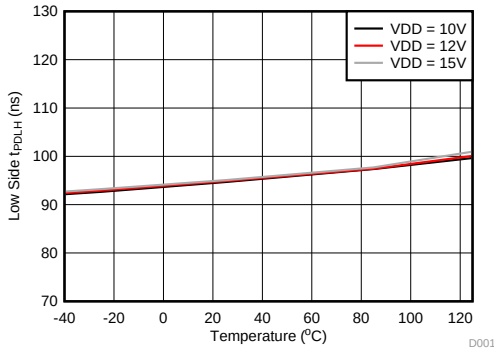


图 2. Low-Side, Turn-On Propagation Delay vs Temperature

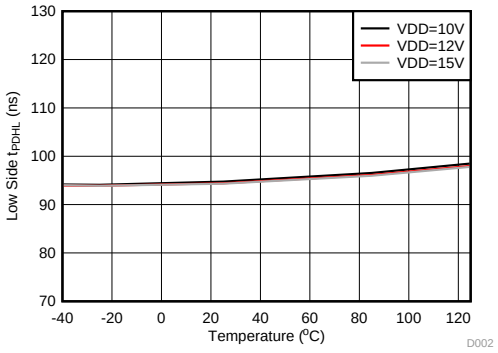


图 3. Low-Side, Turn-Off Propagation Delay vs Temperature

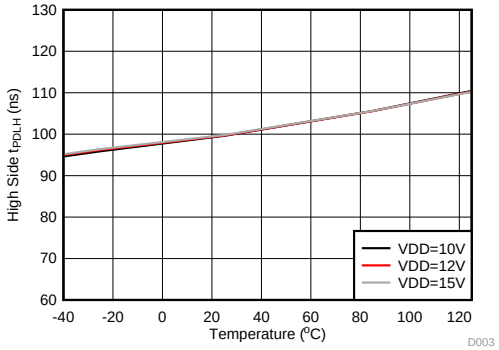


图 4. High-Side, Turn-On Propagation Delay vs Temperature

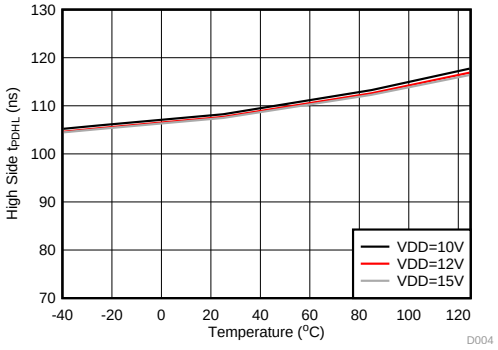


图 5. High-Side, Turn-Off Propagation Delay vs Temperature

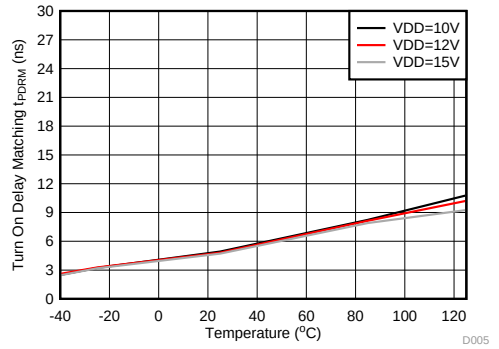


图 6. Turn-On Delay Matching vs Temperature

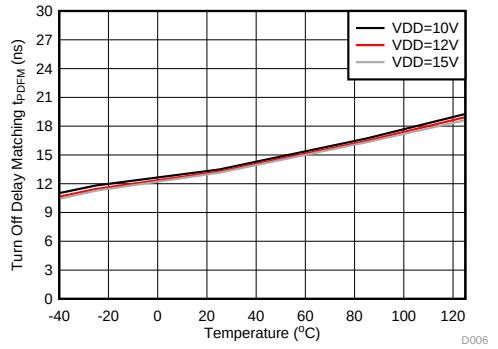


图 7. Turn-Off Delay Matching vs Temperature

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Typical Characteristics (接下页)

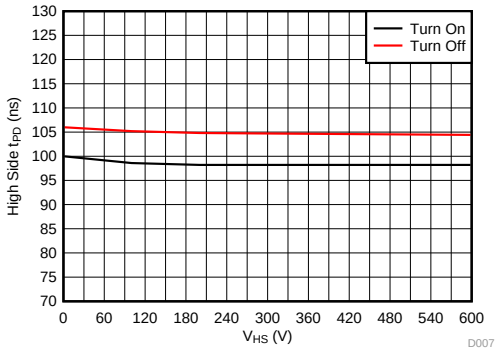


图 8. High-Side Propagation Delay vs HS

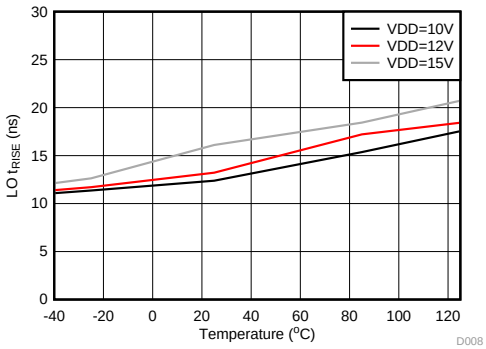


图 9. LO Rise Time with 1000-pF Load vs Temperature

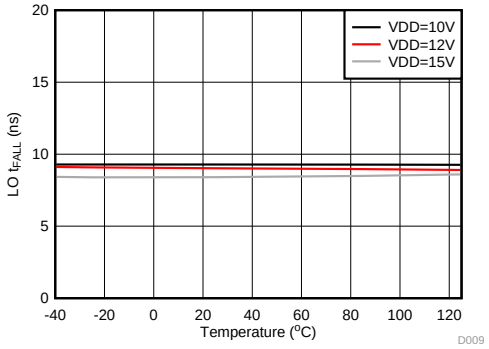


图 10. LO Fall Time with 1000-pF Load vs Temperature

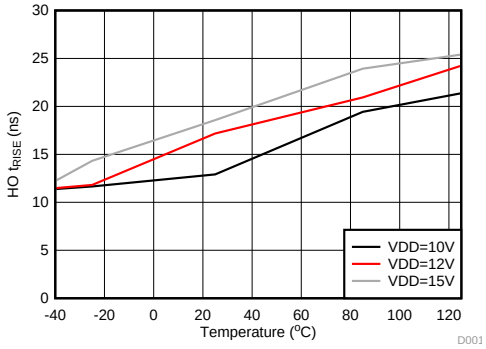


图 11. HO Rise Time with 1000-pF Load vs Temperature

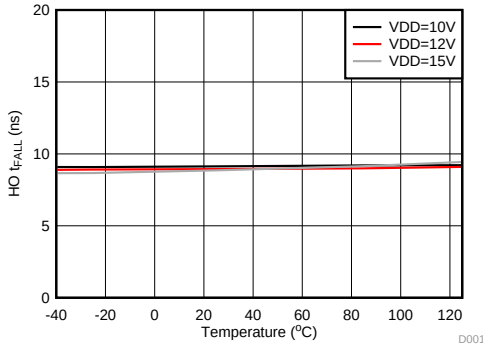


图 12. HO Fall Time with 1000-pF Load vs Temperature

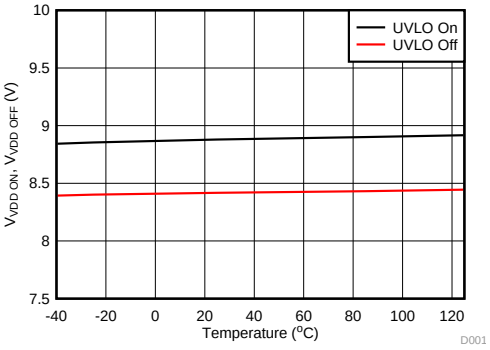


图 13. VDD UVLO Thresholds vs Temperature

Typical Characteristics (接下页)

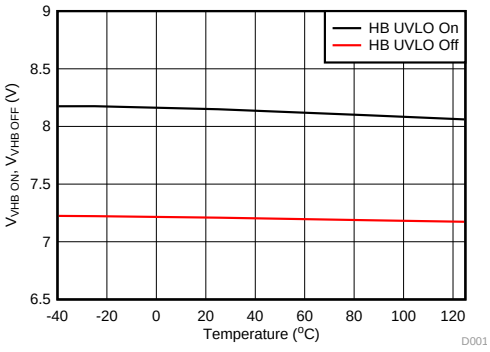


图 14. VHB-VHS UVLO Thresholds vs Temperature

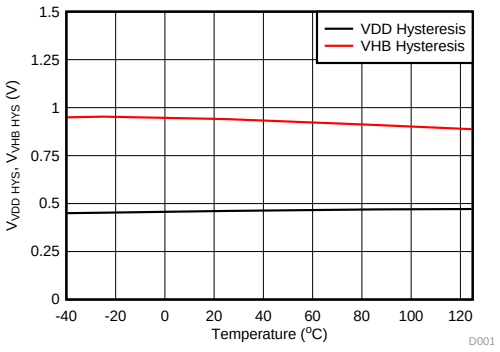


图 15. VDD and VHB-VHS UVLO Hysteresis vs Temperature

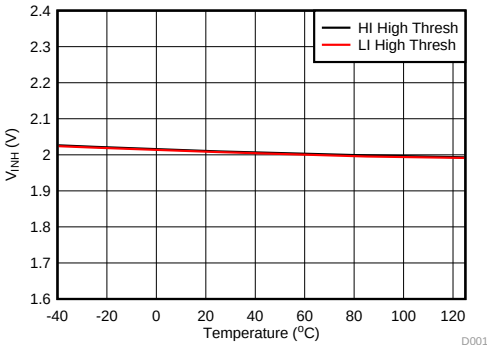


图 16. HI/LI Pin High Threshold vs Temperature

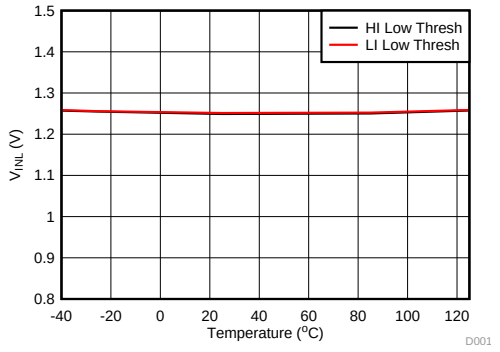


图 17. HI/LI Pin Low Threshold vs Temperature

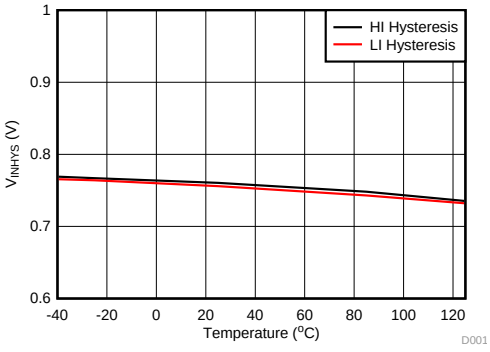


图 18. HI/LI Pin Hysteresis vs Temperature

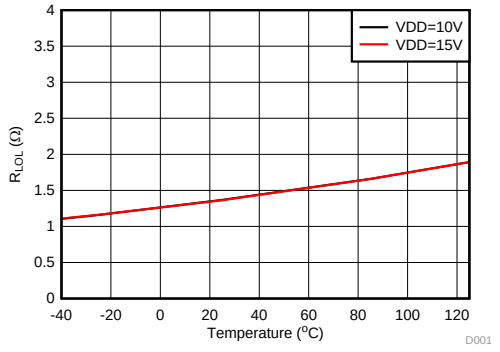


图 19. LO Output Pull-Down Resistance vs Temperature

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Typical Characteristics (接下页)

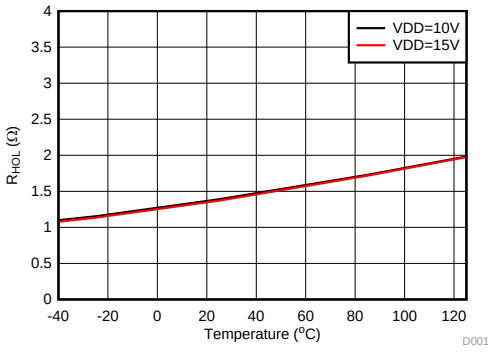


图 20. HO Output Pull-Down Resistance vs Temperature

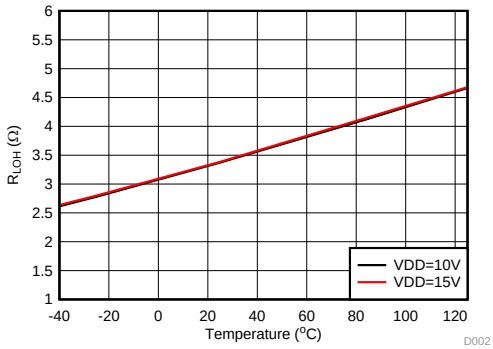


图 21. LO Output Pull-Up Resistance vs Temperature

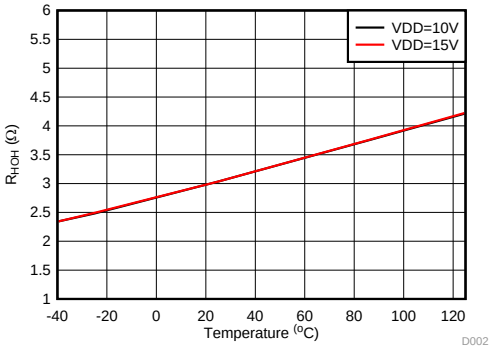


图 22. HO Output Pull-Up Resistance vs Temperature

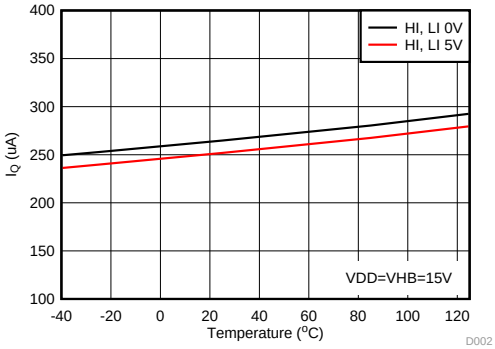


图 23. Total Quiescent VDD plus HB Supply Current vs Temperature

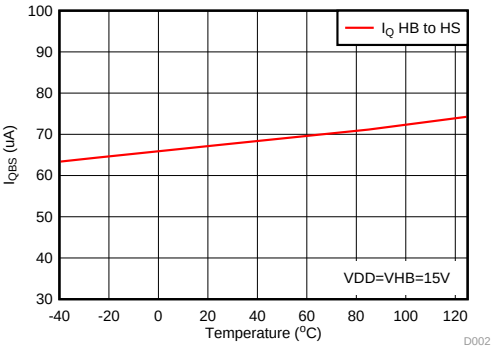


图 24. Quiescent HB to HS Supply Current vs Temperature

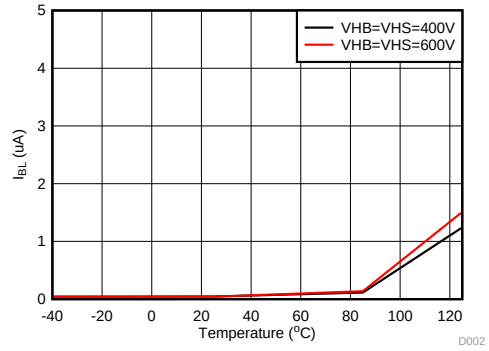


图 25. HB to COM Bootstrap Supply Leakage Current vs Temperature

Typical Characteristics (接下页)

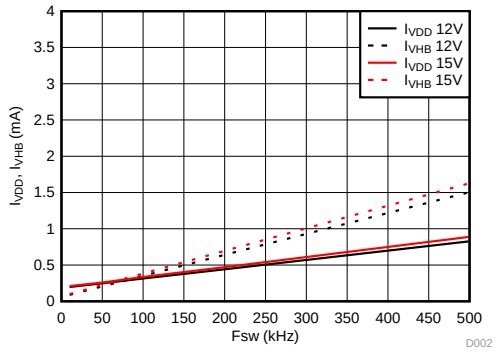


图 26. VDD and HB Operating Current with No Load vs Switching Frequency

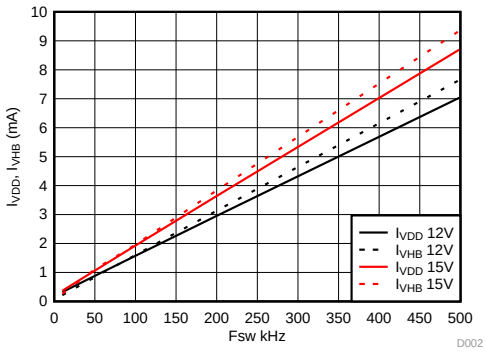


图 27. VDD and HB Operating Current with 1000-pF Load vs Switching Frequency

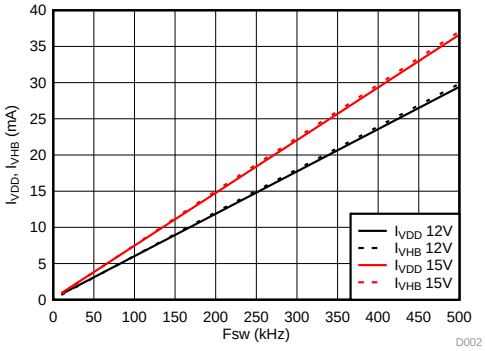


图 28. VDD and HB Operating Current with 4700-pF Load vs Switching Frequency

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7 Detailed Description

7.1 Overview

The UCC27712-Q1 consists of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap or isolated power supplies. The device features fast propagation delays and excellent delay matching between both channels. On the UCC27712-Q1, each channel is controlled by its respective input pins,

Developed with TI's state of the art high-voltage technology, the device features robust drive with excellent noise and transient immunity including large negative voltage tolerance on its inputs, high dv/dt tolerance, and wide negative transient safe operating area (NTSOA) on the switch node (HS).

The UCC27712-Q1 includes protection features where the outputs are held low when the inputs are floating or when the minimum input pulse width specification is not met. Interlock and deadtime functions prevent both outputs from being turned on simultaneously. In addition, the device accepts a wide range bias supply range from 10 V ~ 22 V, and offers UVLO protection for both the VDD and HB bias supply.

High-current, gate-driver devices are required in switching power applications for a variety of reasons. In order to implement fast switching of power devices and reduce associated switching power losses, a powerful gate-driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when having the PWM controller device directly drive the gates of the switching devices is sometimes not feasible. In the case of digital power supply controllers, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch.

In bridge topologies, like hard-switch half bridge, hard-switch full bridge, half-bridge and full-bridge LLC, and phase-shift full bridge, the source and emitter pin of the top-side power MOSFET and IGBT switch is referenced to a node whose voltage changes dynamically; that is, not referenced to a fixed potential, so floating-driver devices are necessary in these topologies.

The UCC27712-Q1 is a high-side and low-side driver dedicated for offline AC-to-DC power supplies and inverters. The high side is a floating driver that can be biased effectively using a bootstrap circuit, and can handle up to 600-V. The driver can be used with 100% duty cycle as long as HB-HS can be above UVLO of the high side.

The device features industry best-in-class propagation delay and delay matching between both channels aimed at minimizing pulse width distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing independent flexibility to control on and off state of the output but does not allow the HO and LO outputs to be on at the same time. The UCC27712-Q1 includes an interlock feature which guarantees a 150ns dead time between the HO and LO outputs if the HI and LI inputs are complimentary. The UCC27712-Q1 includes protection features wherein the outputs are held low when inputs are floating or when the minimum input pulse width specification is not met. The driver inputs are CMOS and TTL compatible for easy interface to digital power controllers and analog controllers alike.

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7.2 Functional Block Diagram

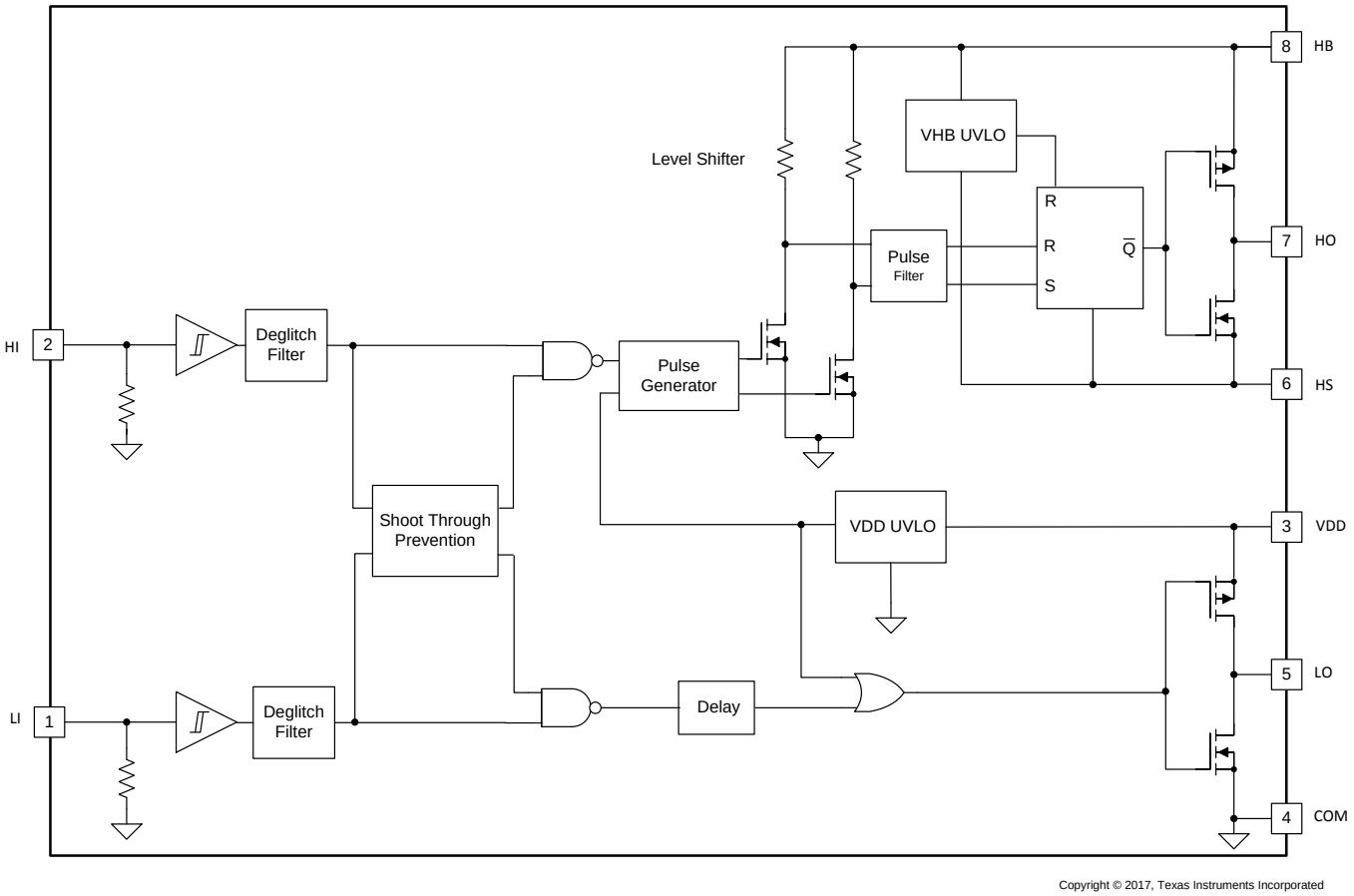


图 29. UCC27712-Q1 Block Diagram

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7.3 Feature Description

7.3.1 VDD and Under Voltage Lockout

The UCC27712-Q1 has an internal under voltage-lockout (UVLO) protection feature on the supply circuit blocks between VDD and VSS pins, as well as between HB and HS pins. When VDD bias voltage is lower than the $V_{VDD(on)}$ threshold at device start-up or lower than $V_{VDD(off)}$ after start-up, the VDD UVLO feature holds both the LO and HO outputs low, regardless of the status of the HI and LI inputs. On the other hand, if HB-HS bias supply voltage is lower than the $V_{VHB(on)}$ threshold at start-up or $V_{VHB(off)}$ after start-up, the HB-HS UVLO feature only holds HO to low, regardless of the status of the HI. The LO output status is not affected by the HB-HS UVLO feature (see 表 1 and 表 2). This allows the LO output to turn-on and re-charge the HB-HS capacitor using the boot-strap circuit and thus allows HB-HS bias voltage to surpass the $V_{VHB(on)}$ threshold.

Both the VDD and VHB UVLO protection functions are provided with a hysteresis feature. This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept a small drop in the bias voltage which is bound to happen when the device starts switching and quiescent current consumption increases instantaneously, as well as when the boot-strap circuit charges the HB-HS capacitor during the first instance of LO turn-on causing a drop in VDD voltage.

The UVLO circuit of VDD-VSS and HB-HS in UCC27712-Q1 generate internal signals to enable/disable the outputs after UVLO_ON/UVLO_OFF thresholds are crossed respectively (please refer to 图 30). Design considerations indicate that the UVLO propagation delay before the outputs are enabled and disabled can vary from 20 μs to 50 μs.

表 1. VDD UVLO Feature Logic Operation

CONDITION (VHB-VHS>$V_{VHB, ON}$ FOR ALL CASES BELOW)	HI	LI	HO	LO
VDD-VSS < $V_{VDD(on)}$ during device start up	H	L	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	L	H	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	H	H	L	L
VDD-VSS < $V_{VDD(on)}$ during device start up	L	L	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	H	L	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	L	H	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	H	H	L	L
VDD-VSS < $V_{VDD(off)}$ after device start up	L	L	L	L

表 2. VHB UVLO Feature Logic Operation

CONDITION (VDD-VSS > $V_{VDD,ON}$ FOR ALL CASES BELOW)	HI	LI	HO	LO
VHB-VHS < $V_{VHB(on)}$ during device start up	H	L	L	L
VHB-VHS < $V_{VHB(on)}$ during device start up	L	H	L	H
VHB-VHS < $V_{VHB(on)}$ during device start up	H	H	L	L
VHB-VHS < $V_{VHB(on)}$ during device start up	L	L	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	H	L	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	L	H	L	H
VHB-VHS < $V_{VHB(off)}$ after device start up	H	H	L	L
VHB-VHS < $V_{VHB(off)}$ after device start up	L	L	L	L

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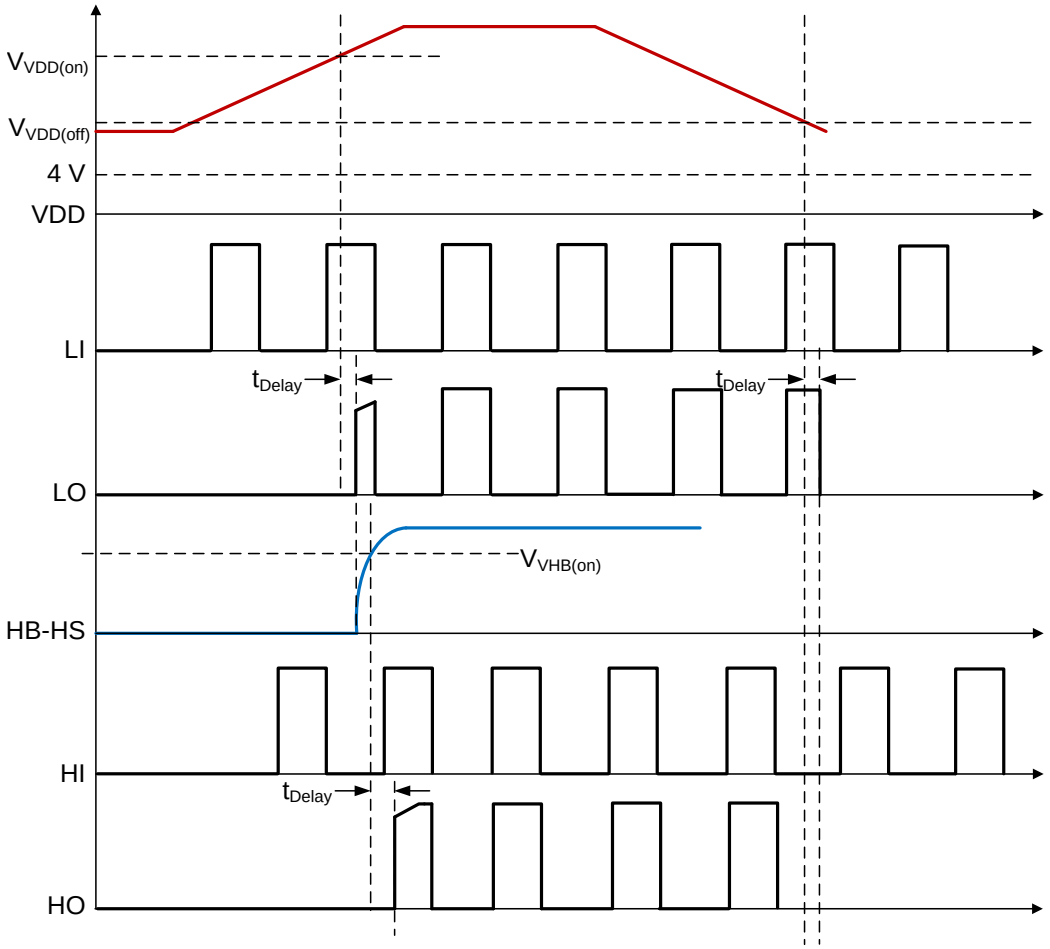


图 30. Power-Up Driver

7.3.2 Input and Output Logic Table

UCC27712-Q1 features separate inputs, HI and LI, for controlling the state of the outputs, HO and LO, respectively. The device does include internal cross-conduction prevention logic and does not allow both HO and LO outputs to be turned on simultaneously (refer to 表 3). This feature prevents cross conduction in bridge topologies in the case of incorrect timing from the controller.

表 3. Input/Output Logic Table
(Assuming no UVLO fault condition exists for VDD and VHB)

HI	LI	HO	LO	Note
L	L	L	L	
L	H	L	H	Output transitions occur after the dead time expires
H	L	H	L	
H	H	L	L	
Left Open	Left Open	L	L	

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7.3.3 Input Stage

The input pins of UCC27712-Q1 are based on a TTL and CMOS compatible input-threshold logic that is independent of the VDD supply voltage. With typical high threshold (V_{INH}) of 2.0 V and typical low threshold (V_{INL}) of 1.2 V, along with very little temperature variation as summarized in 图 16 and 图 17, the input pins are conveniently driven with logic level PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (typically 0.8 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27712-Q1 also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature.

The UCC27712-Q1 includes an important feature: wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using COM pull-down resistors on all the input pins (HI, LI).

The UCC27712-Q1 input pins are capable of sustaining voltages higher than the bias voltage applied on the VDD pin of the device, as long as the absolute magnitude is less than the recommended operating condition's maximum ratings. This features offers the convenience of driving the PWM controller at a higher VDD bias voltage than the UCC27712-Q1 helping to reduce gate charge related switching losses. This capability is envisaged in UCC27712-Q1 by way of two ESD diodes tied back-to-front as shown in 图 31.

Additionally, the input pins are also capable of sustaining negative voltages below COM, as long as the magnitude of the negative voltage is less than the recommended operating condition minimum ratings. A similar diode arrangement exists between the input pins and COM as illustrated in 图 31.

The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, when the input signals are provided by a PWM controller or logic gates with fast transition times. With a slow changing input voltage, the output of driver may switch repeatedly at a high frequency. While the wide hysteresis offered in UCC27712-Q1 definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate-driver device package and transferring it into the external resistor itself. If an RC filter is to be added on the input pins for reducing the impact of system noise and ground bounce, the time constant of the RC filter is recommended to be 20 ns or less, for example, 50 Ω with 220 pF is an acceptable choice.

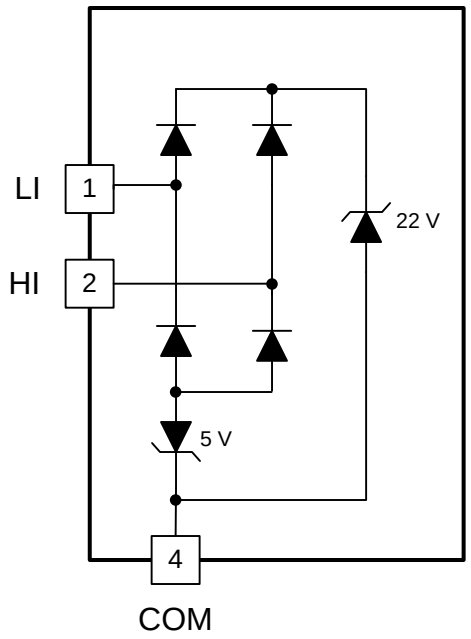


图 31. Diode Structure of Input Stage

7.3.4 Output Stage

The UCC27712-Q1 device output stage pull-up structure features a P-Channel MOSFET to provide source current until the output is saturated to VDD or HB. The R_{OH} parameter (see 图 21) is a DC measurement and it is representative of the on-resistance of the P-Channel device.

The pull-down structure in UCC27712-Q1 is composed of a N-Channel MOSFET. The R_{OL} parameter (see 图 19), which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in UCC27712-Q1 is capable of supplying 1.8-A peak source and 2.8-A peak sink current pulses. The output voltage swings between (VDD and COM) / (HB and HS) providing rail-to-rail operation, thanks to the MOSFET output stage which delivers very low drop-out.

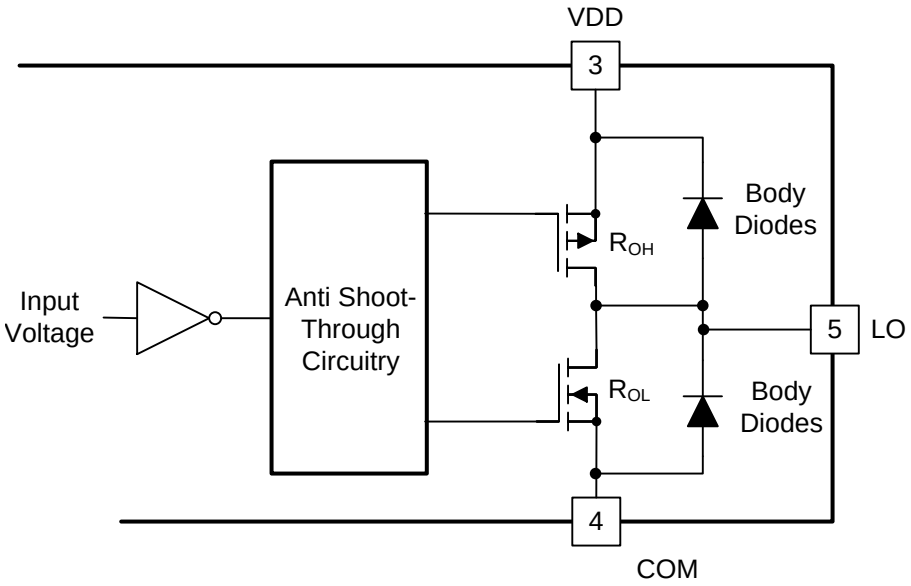


图 32. Output Stage Structure

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7.3.5 Level Shift

The level shift circuit (refer to the Functional Block Diagram) is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). It is a pulsed generated level shifter. With an input signal the pulse generator generates "on" pulses based on the rising edge of the signal and "off" pulses based on the falling edge. On pulses and off pulses turn on each branch of the level shifter so that current flows in each branch to generate different voltages, which is transferred to the set and reset signal in the high side. The signal is rebuilt by the RS latch in the high side domain. The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver. The delay matching of UCC27712-Q1 is summarized in 图 6 and 图 7.

The level shifter in UCC27712-Q1 offers best-in-class capability while operating under negative voltage conditions on HS pin. The level shifter is able to transfer signals from the HI input to HO output with only 4-V headroom between HB and COM. Refer to Operation Under Negative HS Voltage Condition for detailed explanations.

7.3.6 Low Propagation Delays and Tightly Matched Outputs

The UCC27712-Q1 features a best in class, 100-ns (typical) propagation delay (refer to 图 2, 图 3, 图 4 and 图 5) between input and output in high voltage 600-V driver, which goes to offer a low level of pulse width distortion for high frequency switching applications.

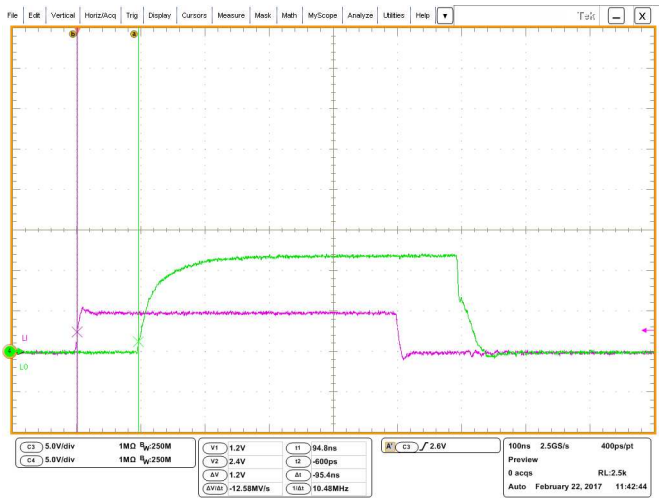


图 33. Turn-On Propagation Delay

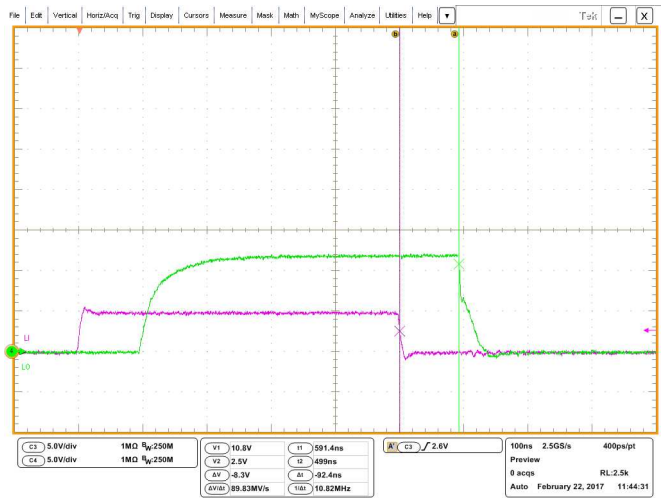


图 34. Turn-Off Propagation Delay

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7.3.7 Parasitic Diode Structure

图 35 illustrates the multiple parasitic diodes involved in the ESD protection components of UCC27712-Q1 device. This provides a pictorial representation of the absolute maximum rating for the device.

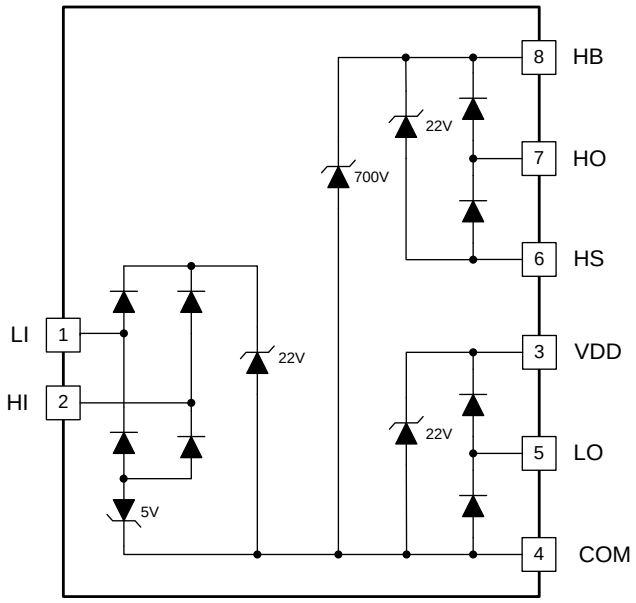


图 35. ESD Structure

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7.4 Device Functional Modes

7.4.1 Minimum Input Pulse Operation

The UCC27712-Q1 device has a minimum turn-on, turn-off pulse transfer function to the output pin from the input pin. This function ensures UCC27712-Q1 is in the correct state when the input signal is very narrow. The function is summarized in 图 36 and 图 37. The t_{ON} which is 25 ns typical is shown in 图 36 and t_{OFF} which is 35ns typical is shown in 图 37

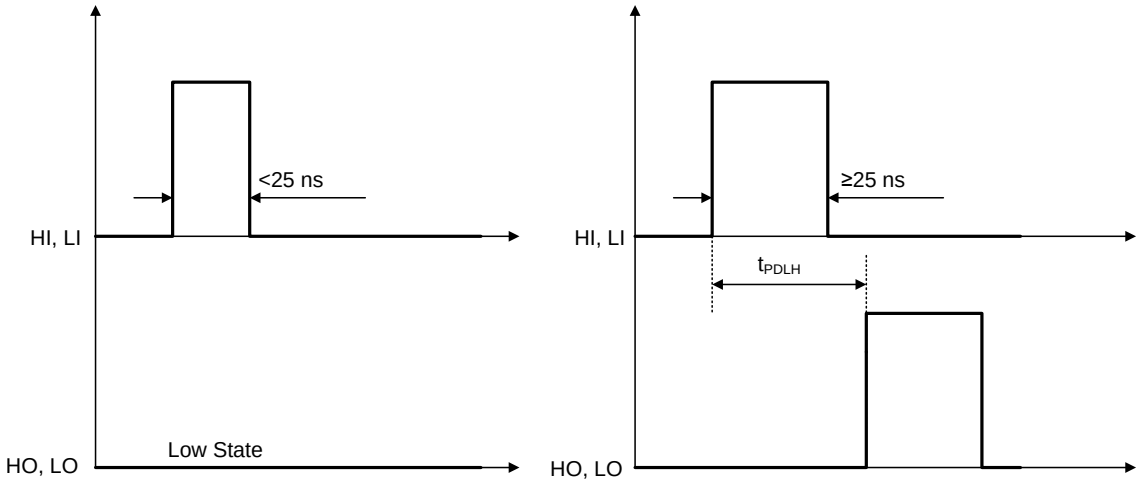


图 36. Minimum Turn-On Pulse

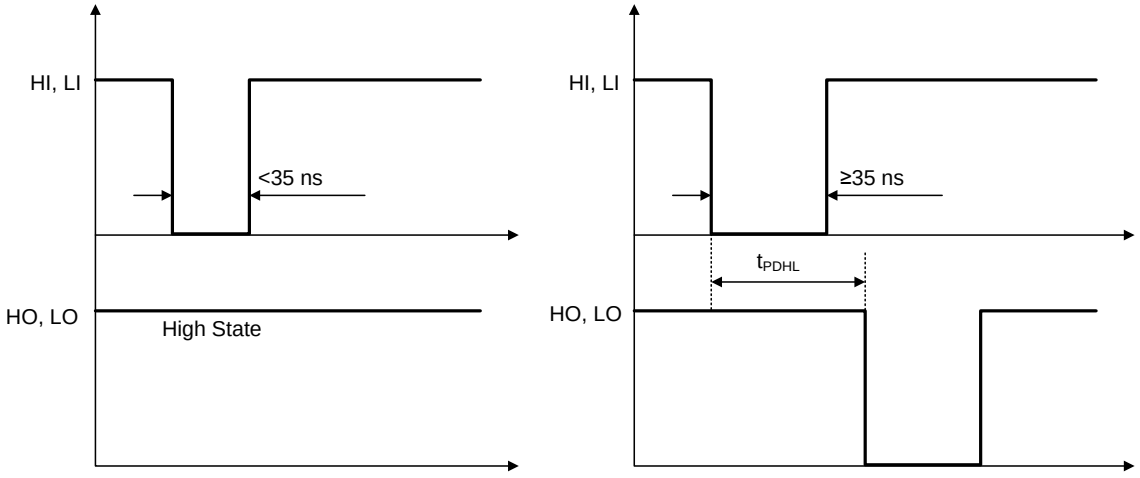


图 37. Minimum Turn-Off Pulse

Device Functional Modes (接下页)

7.4.2 Output Interlock and Dead Time

The UCC27712-Q1 has cross-conduction prevention logic, which is a feature that does not allow both the high-side and low-side outputs to be in high state simultaneously. In bridge power supply topologies, such as half-bridge or full-bridge, the UCC27712-Q1 interlock feature will prevent the high-side and low-side power switches to be turned on simultaneously. The UCC27712-Q1 generates a fixed minimum dead time of t_{DT} which is 150ns nominal in the case of LI and HI overlap or no dead time. 图 38 illustrates the mode of operation where LI and HI have no dead time and HO and LO outputs have the minimum dead time of t_{DT}.

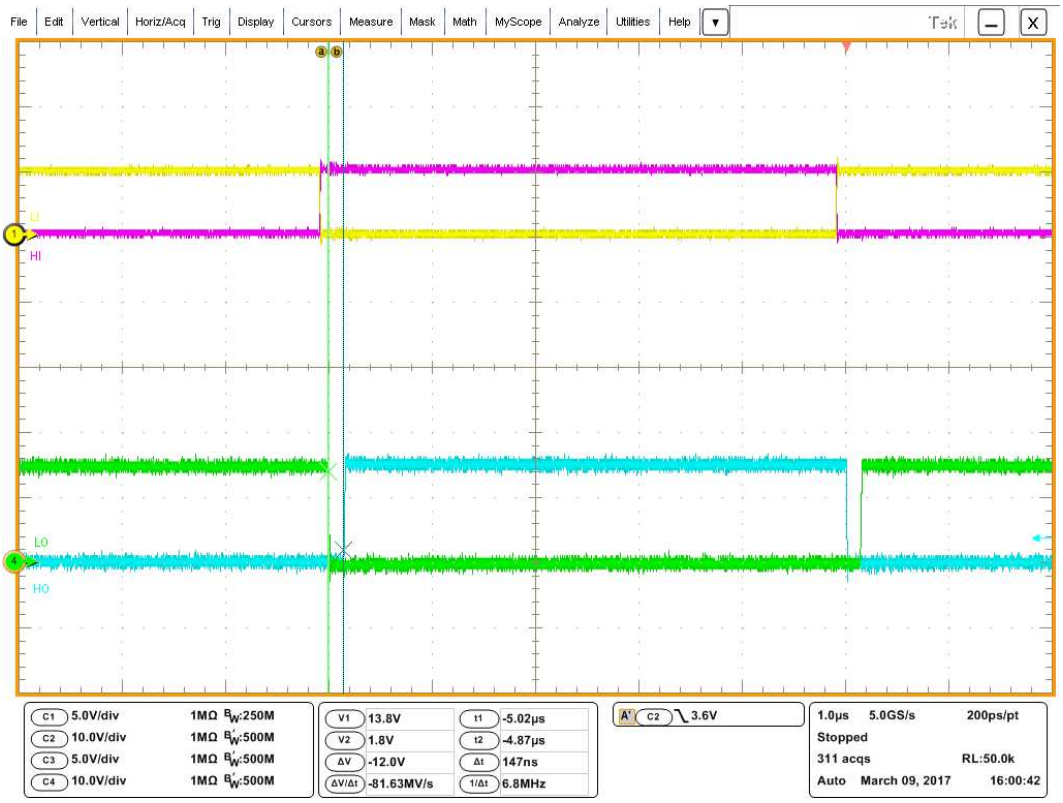


图 38. HO and LO Minimum Dead Time with LI HI Complementary

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Device Functional Modes (接下页)

An input signal's falling edge activates the dead time for the other signal. The output signal's dead time is always set to the longer of either the driver's minimum dead time, t_{DT}, or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent cross conduction, and it does not affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in 图 39.

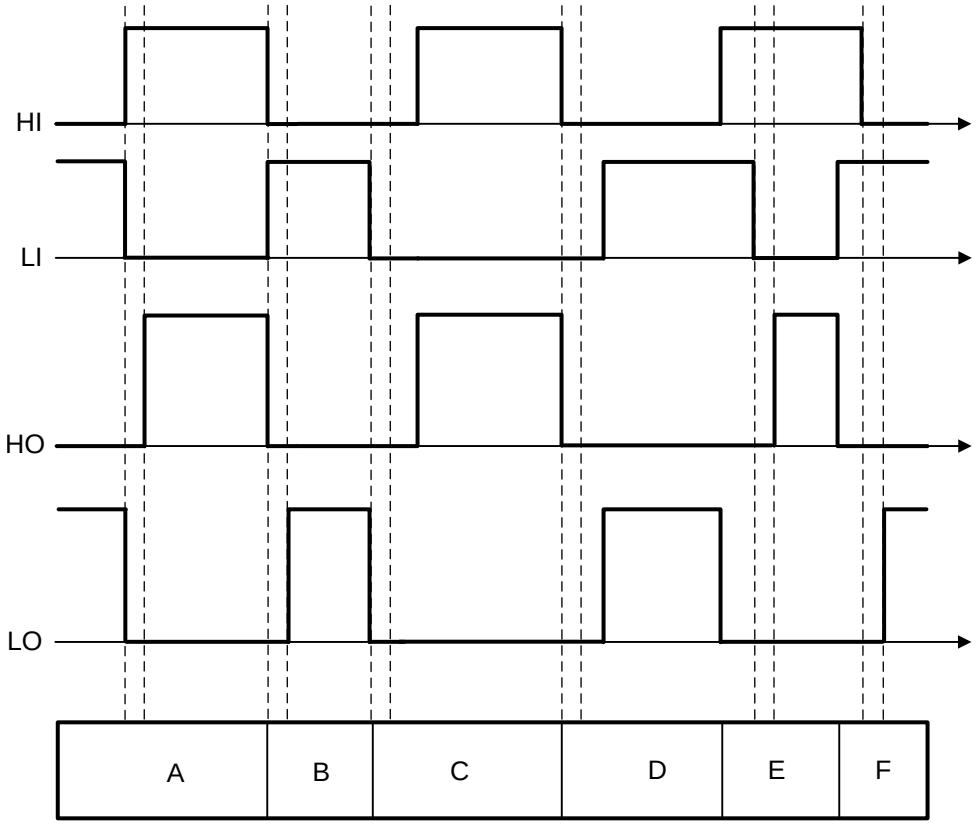


图 39. Input and Output Logic Relationship

Condition A: HI goes high, LI goes low. LI sets LO low immediately and assigns t_{DT} to HO. HO is allowed to go high after t_{DT}.

Condition B: LI goes high, HI goes low. HI sets HO low immediately and assigns t_{DT} to HO. LO is allowed to go high after t_{DT}.

Condition C: LI goes low, HI is still low. LI sets LO low immediately and assigns t_{DT} to HO. In this case, the input signal's own dead time is longer than t_{DT}. Thus when HI goes high HO is set high immediately.

Condition D: HI goes low, LI is still low. HI sets HO low immediately and assigns t_{DT} to LO. In this case, the input signal's own dead time is longer than t_{DT}. Thus when LI goes high LO is set high immediately.

Condition E: HI goes high, while LI and LO are still high. To avoid cross-conduction, HI immediately sets LO low and keeps HO low. After some time LI goes low and assigns t_{DT} to HO. LO is already low. After t_{DT} HO is allowed to go high.

Condition F: LI goes high, while HI and HO are still high. To avoid cross-conduction, LI immediately sets HO low and keeps LO low. After some time HI goes low and assigns t_{DT} to LO. HO is already low. After t_{DT} LO is allowed to go high.

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Device Functional Modes (接下页)

7.4.3 Operation Under 100% Duty Cycle Condition

The UCC27712-Q1 allows constant on or constant off operation (0% and/or 100% duty cycle) as long as the VDD and VHB bias supplies are maintained above the UVLO thresholds. This is a challenge when boot-strap supplies are used for VHB. However, when a dedicated bias supply is used, constant on or constant off conditions can be supported. Also consider the HI and LI interlock function prevents both outputs from being high.

7.4.4 Operation Under Negative HS Voltage Condition

A typical half-bridge configuration with UCC27712-Q1 is shown in 图 40. There are parasitic inductances in the power circuit from die bonding and pinning in QT/QB and PCB tracks of power circuit, the parasitic inductances are labeled $L_{K1,2,3,4}$.

During switching of HS caused by turning off HO, the current path of power circuit is changed to current path 2 from current path 1. This is known as current commutation. The current across L_{K3}, L_{K4} and body diode of QB pulls HS lower than COM. The negative voltage of HS with respect to COM causes a logic error of HO if the driver cannot handle negative voltage of HS. However, the UCC27712-Q1 offers robust operation under these conditions of negative voltage on HS.

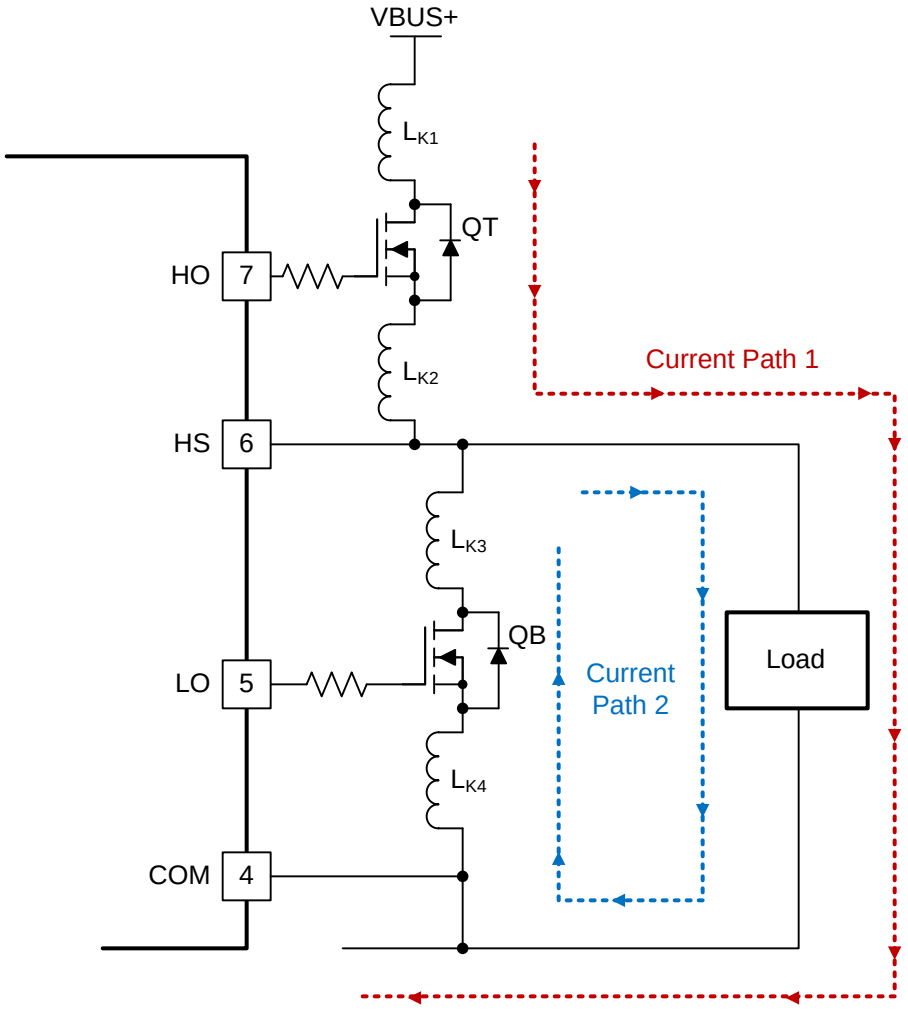


图 40. HS Negative Voltage In Half-Bridge Configuration

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Device Functional Modes (接下页)

The level shifter circuit is with respect to COM (refer to Functional Block Diagram), the voltage from HB to COM is the supply voltage of level shifter. Under the condition of HS is negative voltage with respect to COM, the voltage of HB-COM is decreased, as shown in 图 41. There is a minimum operational supply voltage of level shifter, if the supply voltage of level shifter is too low, the level shifter cannot pass through HI signal to HO. The minimum supply voltage of level shifter of UCC27712-Q1 is 4 V, so the recommended HS specification is dependent on HB-HS. The specification of recommended HS is –11 V at HB – HS = 15 V.

In general, HS can operate until -11 V when HB – HS = 15 V as the ESD structure in 图 35 allows a maximum voltage difference of 22 V between both pins. If HB-HS voltage is different, the minimum HS voltage changes accordingly.

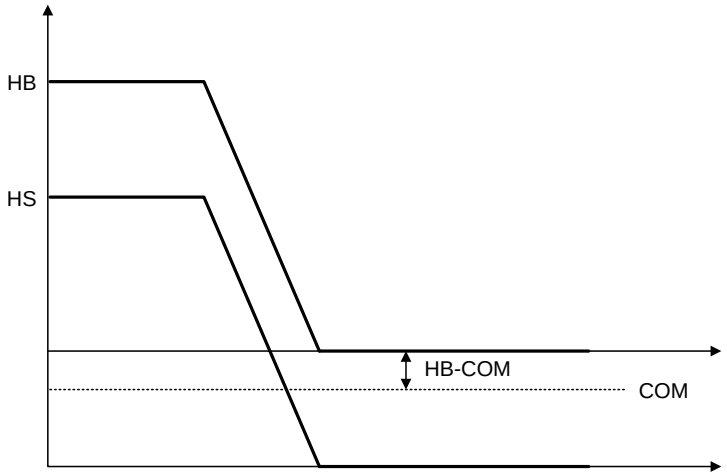


图 41. Level Shifter Supply Voltage with Negative HS

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Logic operational for HS of –11 V to 600 V at HB – HS = 15 V

Device Functional Modes (接下页)

The capability of a typical UCC27712-Q1 device to operate under a negative voltage condition in HS pin is reported in 图 43. The test method is shown in 图 42.

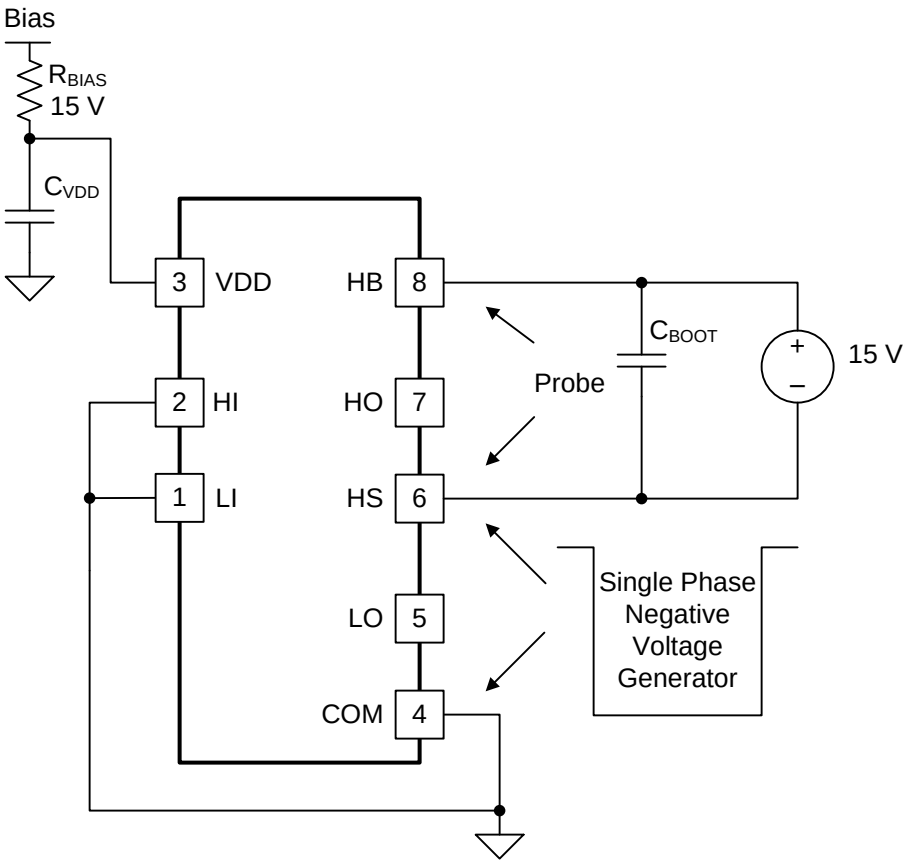


图 42. Negative Voltage Test Method

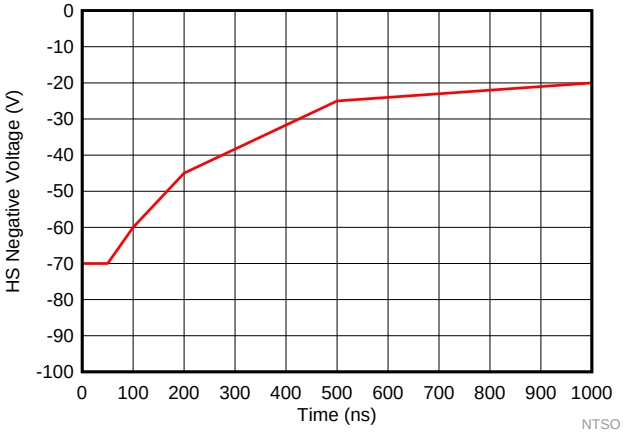


图 43. Negative Voltage Chart
Pulse Width vs Negative Voltage

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8 Application and Implementation

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Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

8.2 Typical Application

The circuit in 图 44 shows a reference design example with UCC27712-Q1 driving a typical half-bridge configuration which could be used in several common power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and motor drive applications.

For more information, please refer to 图 44.

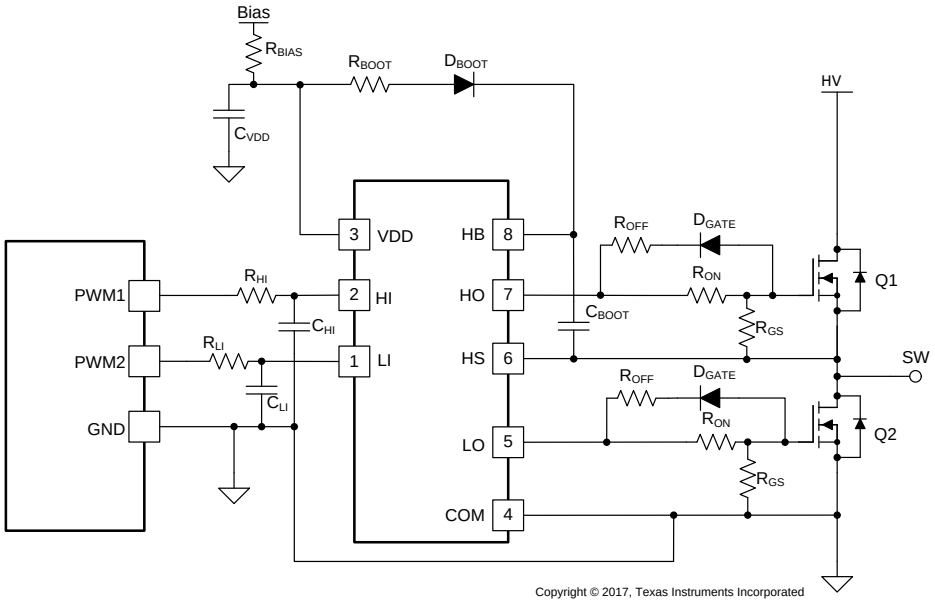


图 44. Typical Application Schematic

Typical Application (接下页)

8.2.1 Design Requirements

表 4 shows the reference design parameters for the example application: UCC27712-Q1 driving 650-V MOSFETs in a high side-low side configuration.

表 4. UCC27712-Q1 Design Requirements

PARAMETER	VALUE	UNIT
Power transistor	IPB65R190CFD	-
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_{SW})	100	kHz
DC link voltage (V_{HV})	400	V

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a 600-V high-side, low-side gate driver with 1.8-A source and 2.8-A sink current capability, targeted to drive power MOSFETs or IGBTs using the UCC27712-Q1. Refer to 图 44 for component names and network locations. For additional design help see the UCC27712EVM-287 User Guide, SLUUBO1.

8.2.2.1 Selecting HI and LI Low Pass Filter Components (R_{HI}, R_{LI}, C_{HI}, C_{LI})

It is recommended that users avoid shaping the input signals to the gate driver in an attempt to slow down (or delay) the signal at the driver output. However it is good practice to have a small RC filter added between PWM controller and input pin of UCC27712-Q1 to filter the high frequency noise, like R_{HI}/C_{HI} and R_{LI}/C_{LI} which is shown in 图 44.

Such a filter should use a R_{HI}/R_{LI} in the range of 10 Ω to 100 Ω and a C_{HI}/C_{LI} between 10 pF and 220 pF. In the example, a R_{HI}/R_{LI} = 49.9 Ω and a C_{HI}/C_{LI} = 33 pF are selected.

8.2.2.2 Selecting Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor should be sized to have more than enough energy to drive the gate of FET Q1 high, and maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with:

$$Q_{Total} = Q_G + \frac{I_{QBS}}{f_{SW}} = 68nC + \frac{65\mu A}{f_{SW}} = 68.65nC \quad (1)$$

This design example targets a boot capacitor ripple voltage of 0.5 V. Therefore, the absolute minimum C_{BOOT} requirement is:

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}} = \frac{68.65nC}{0.5V} \approx 137nF \quad (2)$$

In practice, the value of C_{BOOT} needs to be greater than the calculated value. This allows for capacitance shift from DC bias and temperature, and also skipped cycles that occur during load transients. For this design example 2x 220-nF capacitors were chosen for the bootstrap capacitor.

$$C_{BOOT} = 440nF \quad (3)$$

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8.2.2.3 Selecting VDD Bypass/Holdup Capacitor (C_{VDD}) and R_{bias}

The VDD capacitor (C_{VDD}) should be chosen to be at least 10 times larger than C_{BOOT} so there is minimal voltage drop on the VDD capacitor when charging the boot capacitor . For this design example a 4.7-µF capacitor was selected.

$$C_{VDD} \geq 10 \times C_{BOOT} = 4.7\,\mu F \tag{4}$$

A 10-Ω resistor R_{BIAS} in series with bias supply and VDD pin is recommended to make the VDD ramp up time larger than 20 µs to minimize LO and HO rising as shown in 图 45

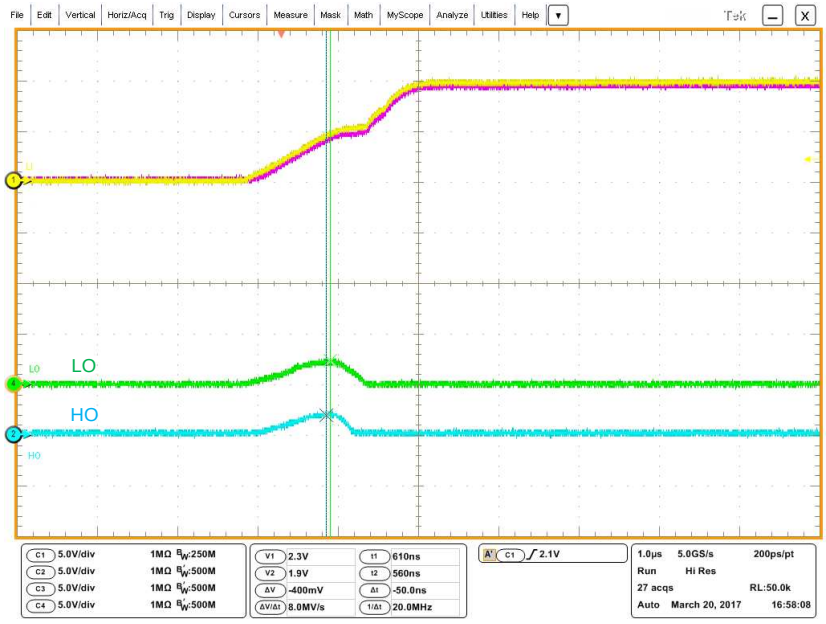


图 45. VDD/HB-HS Fast Ramp Up

8.2.2.4 Selecting Bootstrap Resistor (R_{BOOT})

Resistor R_{BOOT} is selected to limit the current in D_{BOOT} and limit the ramp up slew rate of voltage of HB-HS to avoid the phenomenon shown in 图 45. It is recommended when using the UCC27712-Q1 that R_{BOOT} is between 2 Ω and 20 Ω. For this design we selected an R_{BOOT} current limiting resistor of 2.2 Ω. The bootstrap diode current ($I_{DBOOT(pk)}$) was limited to roughly 5.0 A.

$$I_{DBOOT(pk)} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} = \frac{12\,V - 1V}{2.2\Omega} = 5.0\,A \tag{5}$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the boot-strap capacitor. This energy is equivalent to 1/2 × CBOOT × V^2. This energy is dissipated during the charging time of the bootstrap capacitor (~3 × R_{BOOT} × C_{BOOT}). Special attention must be paid to use a bigger size R_{BOOT} when a bigger value of C_{BOOT} is chosen.

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8.2.2.5 Selecting Gate Resistor R_{ON}/R_{OFF}

Resistor R_{ON} and R_{OFF} are sized to achieve the following:

- Limit ringing caused by parasitic inductances and capacitances.
- Limit ringing caused by high voltage/current switching dV/dt, dI/dt, and body diode reverse recovery.
- Fine-tune gate drive strength to optimize switching loss.
- Reduce electromagnetic interference (EMI).

As mentioned in Output Stage, the UCC27712-Q1 has a pull up structure with a P-channel MOSFET providing a peak source current of 1.8A.

For this example 3.3-Ω resistors for R_{ON} and 2.2-Ω resistors for R_{OFF} were selected to provide damping for ringing and ample gate drive current.

$$R_{ON} = 3.3\Omega, R_{OFF} = 2.2\Omega \tag{6}$$

Therefore the peak source current can be predicted with:

$$I_{HO+} = MIN\left(1.8\,A, \frac{V_{DD} - V_{DBOOT}}{R_{HOH} + R_{ON} + R_{GFET_Int}}\right) \tag{7}$$

$$I_{LO+} = MIN\left(1.8\,A, \frac{V_{DD}}{R_{LOH} + R_{ON} + R_{GFET_Int}}\right) \tag{8}$$

where

- R_{ON}: External turn-on resistance
- R_{GFET_Int}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current. The maximum values between 1.8 A, the UCC27712-Q1 peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{HO+} = \frac{V_{DD} - V_{DBOOT}}{R_{HOH} + R_{ON} + R_{GFET_Int}} = \frac{12\,V\text{-}0.6\,V}{3.0\Omega + 3.3\Omega + 1.0\Omega} \approx 1.6\,A \tag{9}$$

$$I_{LO+} = \frac{V_{DD}}{R_{LOH} + R_{ON} + R_{GFET_Int}} = \frac{12\,V}{3.0\Omega + 3.3\Omega + 1.0\Omega} \approx 1.6\,A \tag{10}$$

Therefore, the high-side and low side peak source current is 1.6 A. Similarly, the peak sink current can be calculated with:

$$I_{HO-} = MIN\left(2.8\,A, \frac{V_{DD} - V_{DBOOT} - V_{DGATE}}{R_{HOL} + R_{OFF} + R_{GFET_Int}}\right) \tag{11}$$

$$I_{LO-} = MIN\left(2.8\,A, \frac{V_{DD} - V_{DGATE}}{R_{LOL} + R_{OFF} + R_{GFET_Int}}\right) \tag{12}$$

where

- R_{OFF}: External turn-off resistance
- V_{DGATE}: The diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MBRM130L.
- I_{O-} = Peak sink current. The maximum values between 2.8 A, the UCC27712-Q1 peak sink current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{HO-} = \frac{V_{DD} - V_{DBOOT} - V_{DGATE}}{R_{HOL} + R_{ON} + R_{GFET_Int}} = \frac{12\,V\text{-}0.6\,V\text{-}0.6\,V}{1.5\Omega + 2.2\Omega + 1.0\Omega} \approx 2.3\,A \tag{13}$$

$$I_{LO-} = \frac{V_{DD} - V_{DGATE}}{R_{LOL} + R_{ON} + R_{GFET_Int}} = \frac{12\,V\text{-}0.6\,V}{1.5\Omega + 2.2\Omega + 1.0\Omega} \approx 2.4\,A \tag{14}$$

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8.2.2.6 Selecting Bootstrap Diode

A fast recovery diode should be chosen to avoid charge being taken away from the bootstrap capacitor. Thus, a fast reverse recovery time t_{RR}, low forward voltage V_F and low junction capacitance is recommended.

Suggested parts include MURA160T3G and BYG20J.

8.2.2.7 Estimate the UCC27712-Q1 Power Losses ($P_{UCC27712-Q1}$)

The power losses of UCC27712-Q1 ($P_{UCC27712-Q1}$) are estimated by calculating losses from several components. The gate drive loss in the UCC27712-Q1 is typically dominated by gate drive losses associated with charging and discharging the power device gate charge. There are other losses to consider especially if operating at high switching frequencies outlined below.

To determine the UCC27712-Q1 operating with no driver load, refer to the Typical Characteristics 图 26 for IDD and IHB to determine the operating current at the appropriate f_{SW}. The operating current power losses with no driver load are calculated in 公式 15:

$$P_Q = V_{VDD} \times \left(I_{VDD,100kHz} + I_{HB,100kHz}\right) = 12\,V \times \left(310\ \mu A + 350\ \mu A\right) \approx 8\,mW \quad (15)$$

Static losses due to leakage current (I_{BL}) are calculated from the HB high-voltage node as shown in 公式 16:

$$P_{IBL} = V_{HB} \times I_{BL} \times D = 400\,V \times 20\,\mu A \times 0.5 = 4\,mW \quad (16)$$

公式 17 calculates dynamic losses during the operation of the level shifter at HO turn-off edge. Q_P, typically 0.6 nC, is the charge absorbed by the level shifter during operation at each edge. Please note that if high-voltage switching occurs during HO turn-on as well (as in the case of ZVS topologies), then the power loss due to this component must be effectively doubled.

$$P_{LevelShift} = \left[V_{HV} + (V_{HB} - V_{HS})\right] \times Q_P \times f_{SW} = 411.4\,V \times 0.6\,nC \times 100\,kHz = 24.7\,mW \quad (17)$$

where

- V_{HV}: DC link high voltage input in V
- f_{SW}: Switching frequency of converter in Hz.

Dynamic losses incurred due to the gate charge while driving the FETs Q1 and Q2 are calculated 公式 18. Please note that this component typically dominates over the dynamic losses related to the internal VDD and VHB switching logic circuitry in UCC27712-Q1. The losses incurred driving the gate charge are not all dissipated in the gate driver device, this includes losses in the external gate resistance and internal power switch gate resistance.

$$P_{QG1,QG2} = 2 \times V_{VDD} \times Q_G \times f_{SW} = 2 \times 12\,V \times 68\,nC \times 100\,kHz = 163\,mW \quad (18)$$

The UCC27712-Q1 gate driver loss on the output stage ,P_{GDO}, is part of $P_{QG1,QG2}$. If the external gate resistances are zero most of the $P_{QG1,QG2}$ will be dissipated in the UCC27712-Q1. If there are external gate resistances, the total loss will be distributed between the gate driver pull-up/down resistances and the external gate resistances.

The gate drive power dissipated within the UCC27712-Q1 driver can be determined by 公式 19:

$$P_{GDO} = \frac{P_{QG1,QG2}}{2} \times \left(\frac{R_{HOH}}{R_{HOH} + R_{ON} + R_{GFET_Int}} + \frac{R_{HOL}}{R_{HOL} + R_{OFF} + R_{GFET_Int}} \right) \quad (19)$$

In this example the gate drive related losses are approximately 60mW as shown in 公式 20:

$$P_{GDO} = \frac{163\,mW}{2} \times \left(\frac{3\,\Omega}{3\,\Omega + 3.3\,\Omega + 1\,\Omega} + \frac{1.5\,\Omega}{1.5\,\Omega + 2.2\,\Omega + 1\,\Omega} \right) \approx 60\,mW \quad (20)$$

For the conditions, VDD=12V, VHB = 400V, HO On-state Duty cycle D = 50%, Q_G = 68nC, f_{SW} = 100kHz, the total power loss in UCC27712-Q1 driver for a half bridge power supply topology can be estimated as follows:

$$P_{UCC27712} = P_Q + P_{IBL} + P_{LevelShift} + P_{GDO} = 8\,mW + 4\,mW + 25\,mW + 60\,mW = 97\,mW \quad (21)$$

8.2.2.8 Estimating Junction Temperature

The junction temperature can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{UCC27712} \quad (22)$$

where

- T_C is the UCC27712-Q1 case-top temperature measured with a thermocouple or some other instrument. and
- Ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table. Importantly.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of estimating the junction temperature. The majority of the power dissipation of most devices is released into the PCB through the package leads, whereas only a small percentage of the total dissipation is released through the top of the case (where thermocouple measurements are usually taken). $R_{\theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or a heatsink is applied to the device package. In other cases $R_{\theta JC}$ will inaccurately estimate the true junction temperature of the device. Ψ_{JT} is experimentally derived by assuming the amount of thermal energy dissipated through the top of the device will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature can be estimated accurately to within a few degrees Celsius. For more information, see the Semiconductor and IC Package Thermal Metrics application report.

Additional Considerations: In the application example schematic there are 10-kΩ resistors across the gate and source terminals of FET Q1 and Q2. These resistors are placed across these nodes to ensure FETs Q1 and Q2 are not turned on if the UCC27712-Q1 is not in place or properly soldered to the circuit board or if UCC27712-Q1 is in an unbiased state.

8.2.2.9 Operation With IGBT's

The UCC27712-Q1 is well suited for driving IGBT's in various applications including motor drive and inverters. The design procedure is as the previous MOSFET example but the VDD voltage is typically 15-V to drive IGBT devices. Use the power transistor parameters and application specifications to determine the detail design and component values. See 图 46 below for a typical IGBT application.

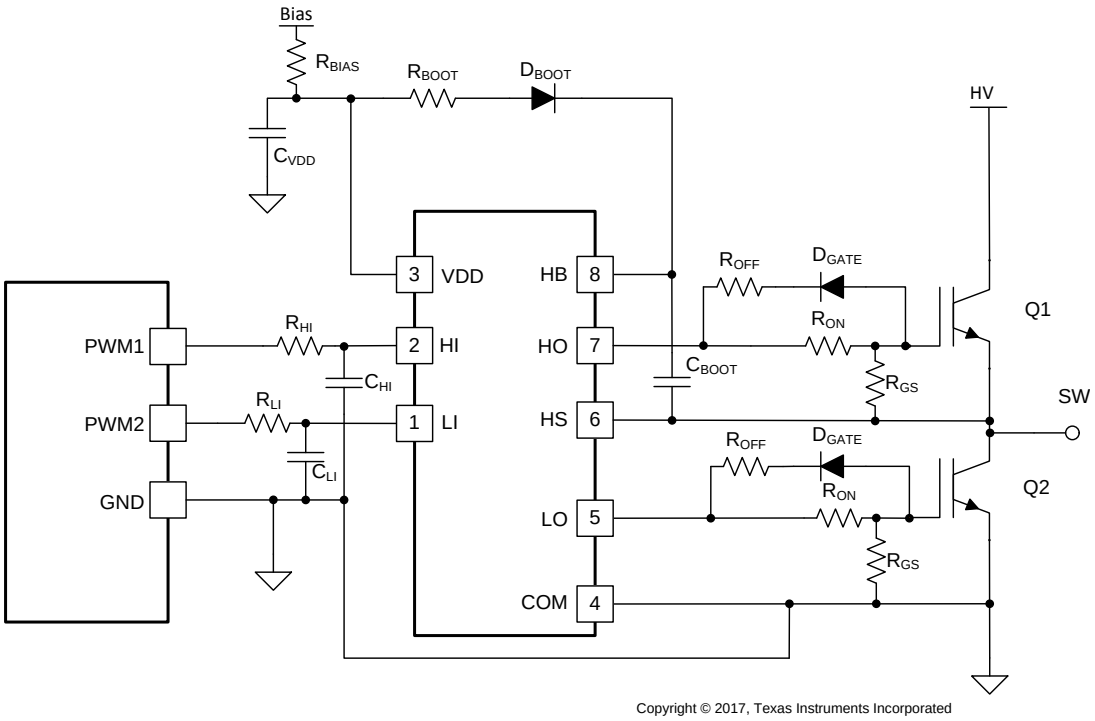


图 46. Typical IGBT Application Schematic

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Refer to 图 47 below for the UCC27712-Q1 driving 40-A, 650-V IGBT's in a high voltage sync buck configuration. The input voltage is 400 V, output 100 V with a 150-W output load. Channel 1 is the inductor current, Channel 2 is high-side IGBT VGE, Channel 3 is low-side IGBT VGE, and Channel 4 is the switch node or HS voltage.

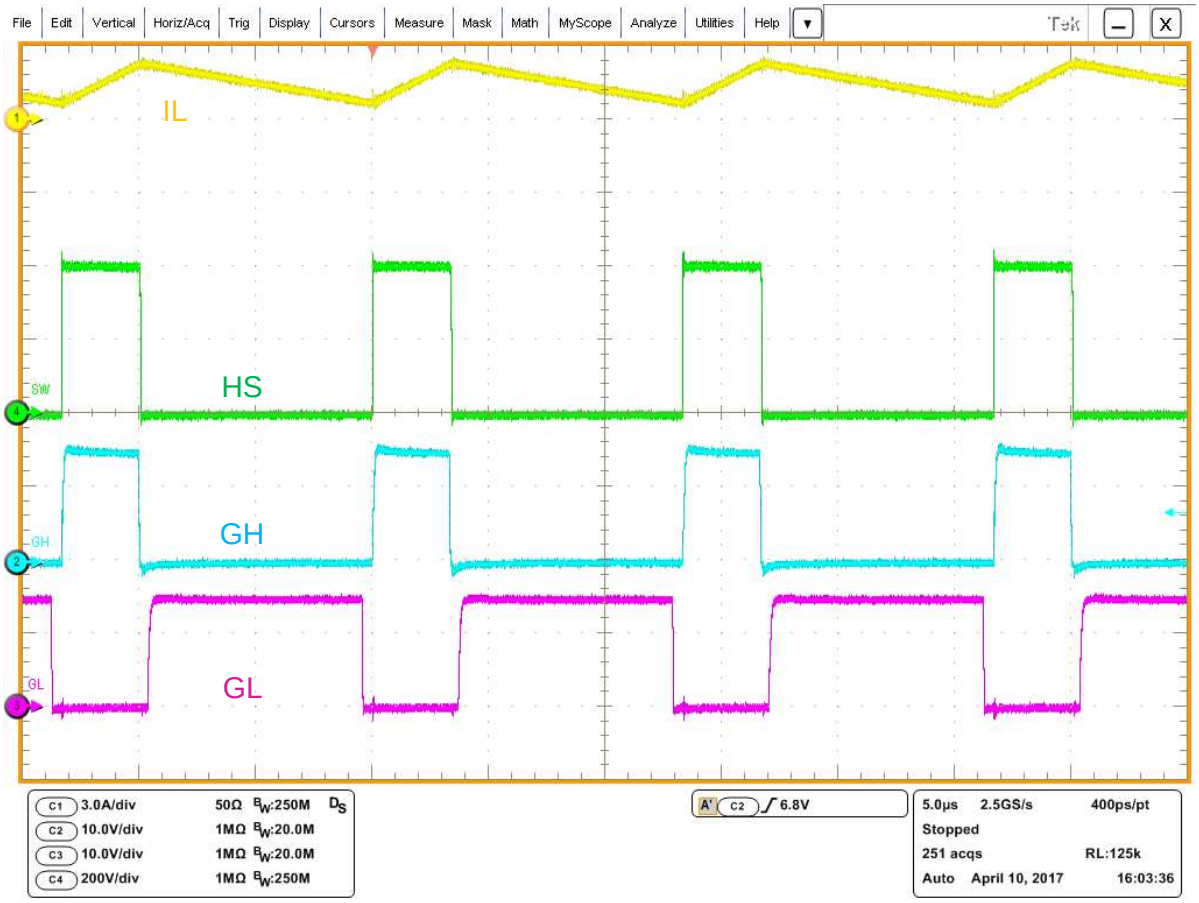


图 47. IGBT Sync-Buck Operating at 400 V and 150 W

8.2.3 Application Curves

图 48 and 图 49 show the measured LI to LO turn-on and turn-off delay of one UCC27712-Q1 device. Channel 3 depicts LI and Channel 4 LO.

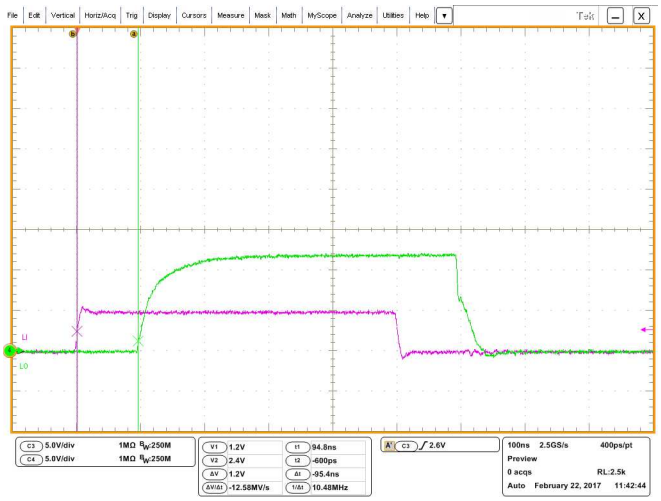


图 48. LI to LO Turn-On Propagation Delay

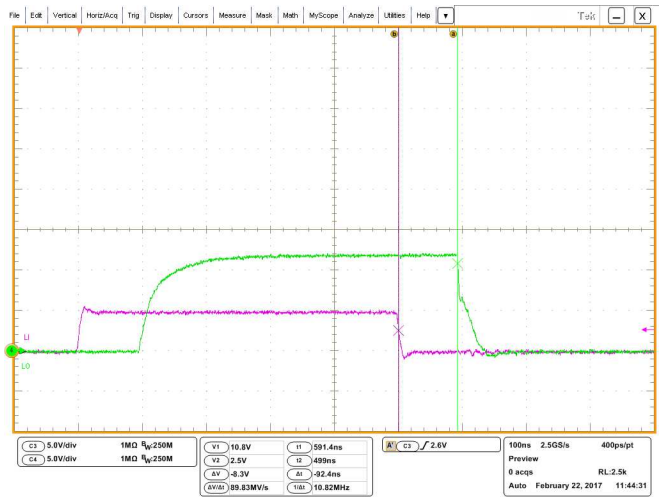


图 49. LI to LO Turn-Off Propagation Delay

图 50 and 图 51 show the measured HI to HO turn-on and turn-off delay of one UCC27712-Q1 device. Channel 1 depicts HI and Channel 2 HO.

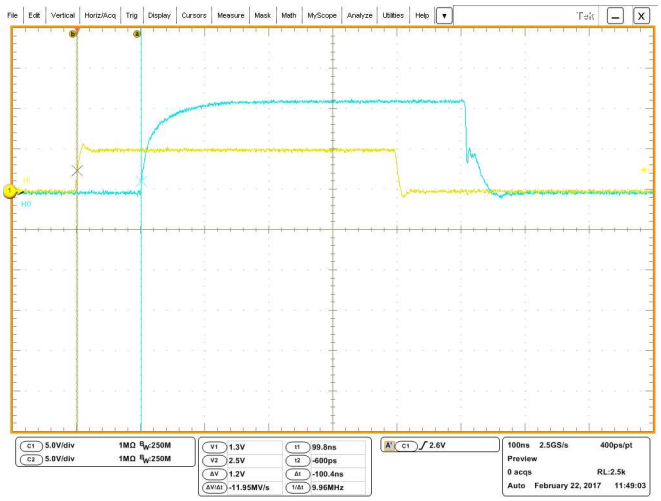


图 50. HI to HO Turn-On Propagation Delay

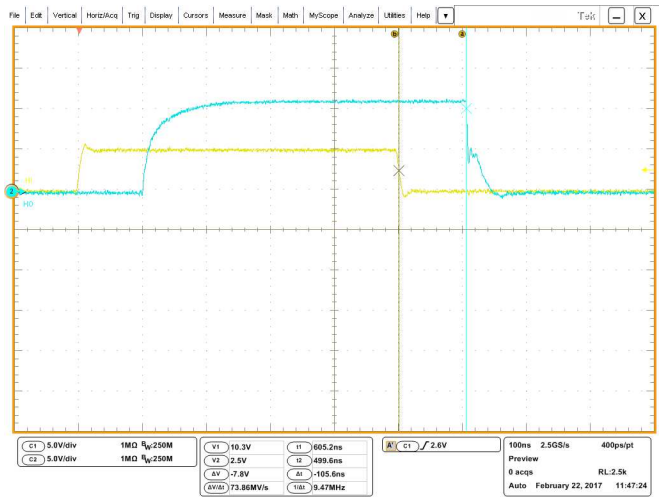


图 51. HI to HO Turn-Off Propagation Delay

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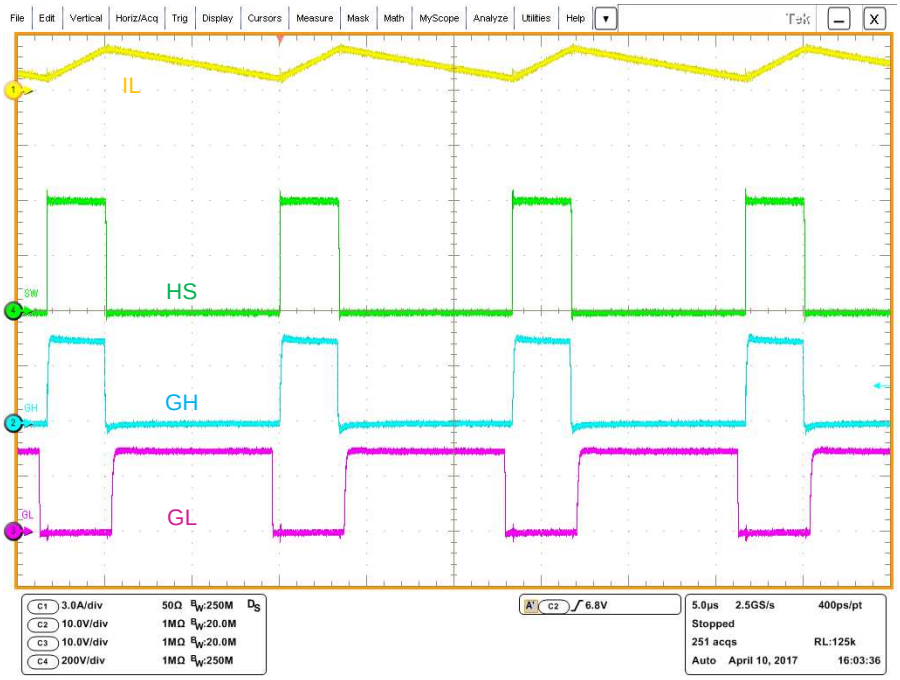


图 52. MOSFET Sync-Buck Operating at 400 V and 150 W

图 52 shows UCC27712-Q1 operating in a high voltage sync-buck. Channel 1 depicts inductor current, Channel 2 high side MOSFET VGS, Channel 3 low side MOSFET VGS, and Channel 4 high voltage switch node.

9 Power Supply Recommendations

The VDD power terminal for the device requires the placement of an energy storage capacitor, because of UCC27712-Q1 is 1.8-A, peak-current driver. And requires the placement of low-esr noise-decoupling capacitance as directly as possible from the VDD terminal to the COM terminal, ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better.

The recommended storage capacitor is an X7R, 50-V capacitor. The recommended decoupling capacitors are a 1-µF 0805-sized 50-V X7R capacitor, ideally with (but not essential) a second smaller parallel 100-nF 0603-sized 50-V X7R capacitor.

Similarly, a low-esr X7R capacitance is recommended for the HB-HS power terminals which must be placed as close as possible to device pins.

10 Layout

10.1 Layout Guidelines

- Locate UCC27712-Q1 as close as possible to the MOSFETs in order to minimize the length of high-current traces between the HO/LO and the Gate of MOSFETs, as well as the return current path to the driver HS and COM.
- A resistor in series with bias supply and VDD pin is recommended.
- Locate the VDD capacitor (CVDD) and VHB capacitor (CBOOT) as close as possible to the pins of UCC27712-Q1.
- A 2-Ω to 20-Ω resistor series with bootstrap diode is recommended to limit bootstrap current.
- A RC filter with 10 Ω to 100 Ω and 10 pF to 220 pF for HI/LI is recommended.
- Separate power traces and signal traces, such as output and input signals.
- Maintain as much separation as possible from the from the low voltage pins and floating drive HB, HO and HS pins.
- Ensure there is not high switching current flowing in the control ground (input signal reference) from the power train ground.

10.2 Layout Example

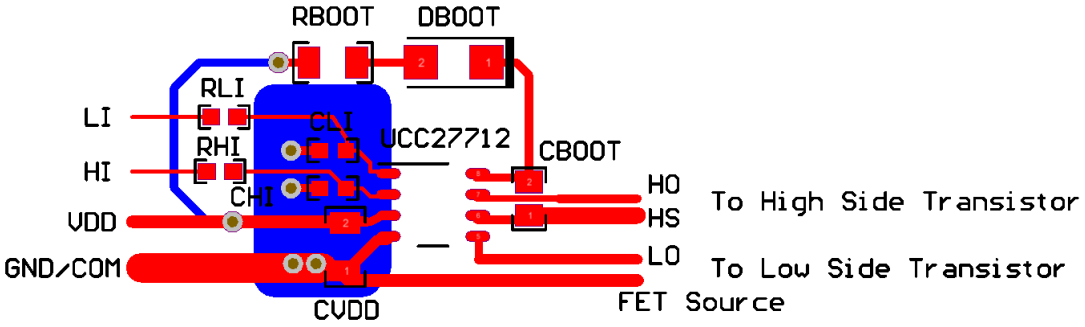


图 53. UCC27712-Q1 Layout Example

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

用户指南，*使用 UCC27712EVM-287*，(SLUUBO1)

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
UCC27712-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27712QDQ1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27712Q	Samples
UCC27712QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27712Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

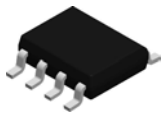
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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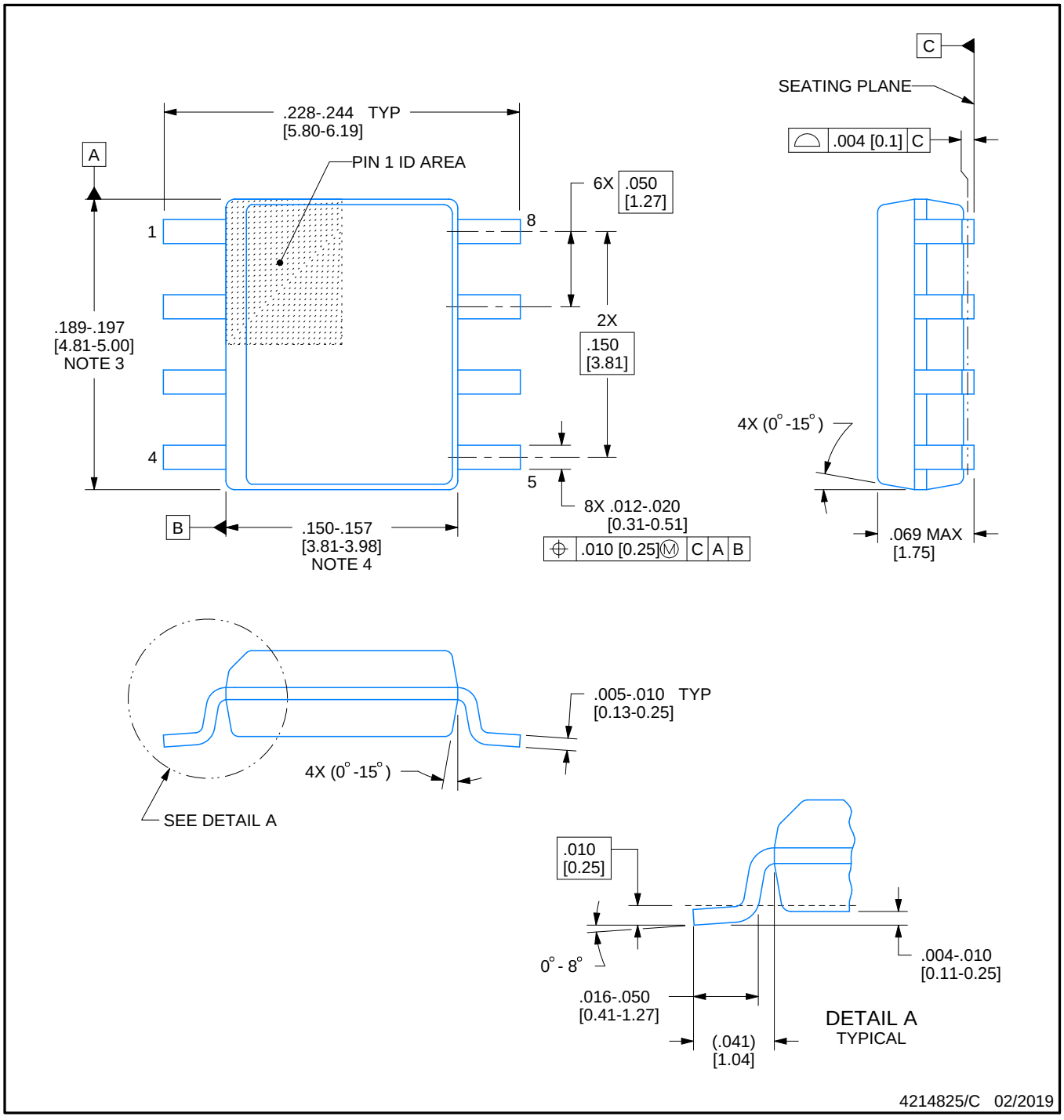


PACKAGE OUTLINE

D0008A

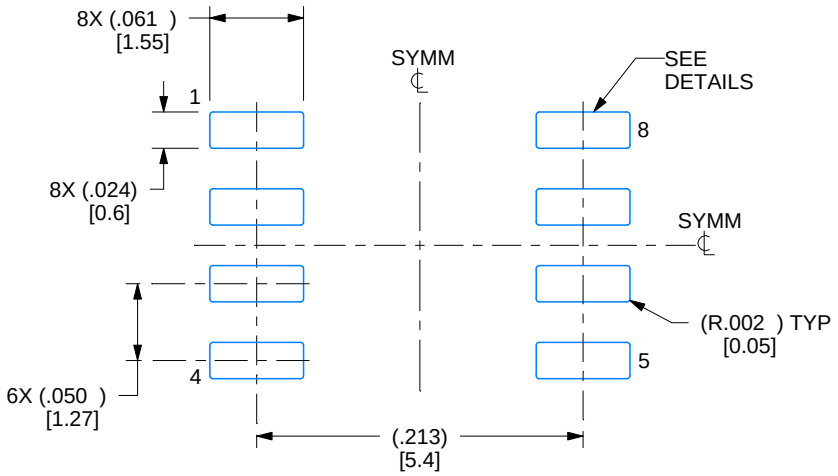
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

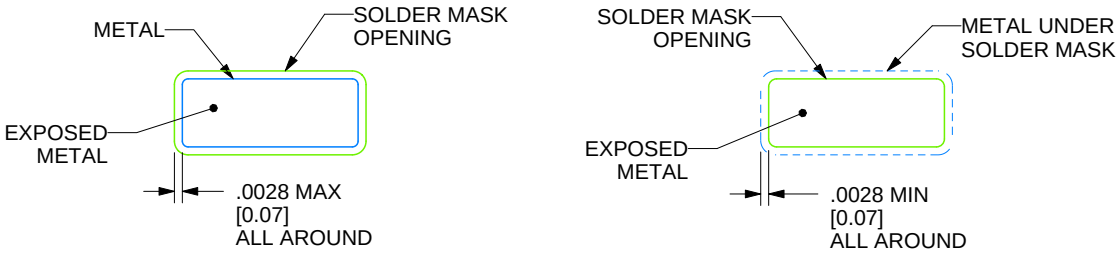


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

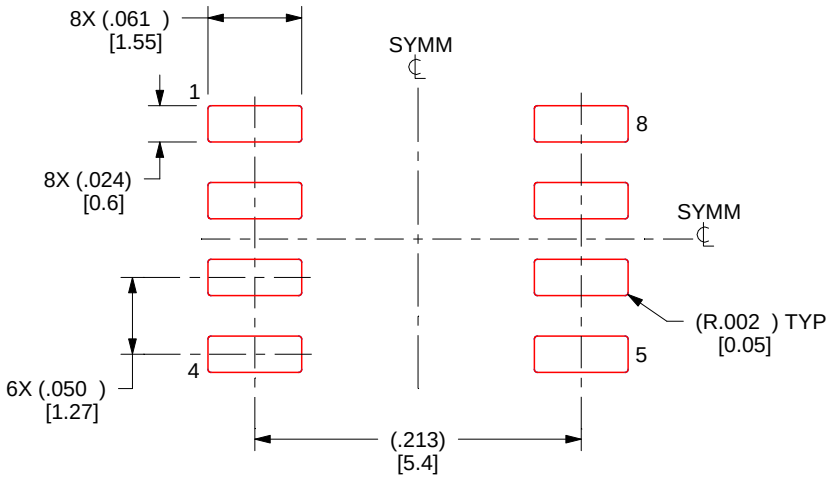
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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