

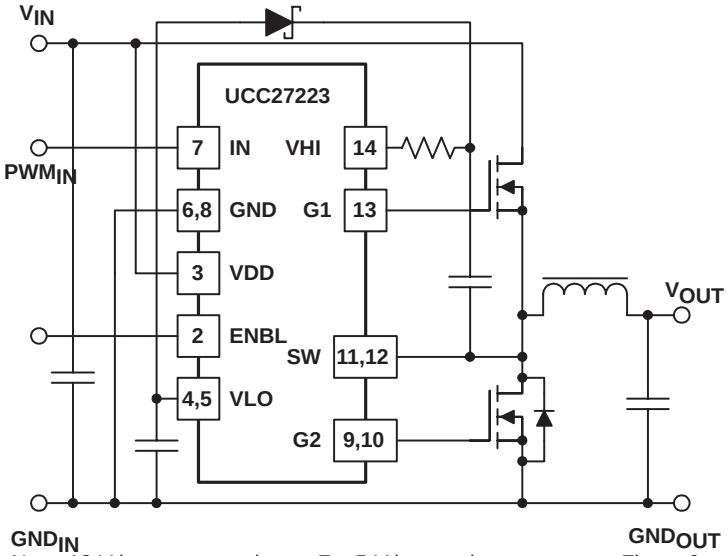
SLUS558 − DECEMBER 2003

HIGH-EFFICIENCY PREDICTIVE SYNCHRONOUS BUCK DRIVER WITH ENABLE

FEATURES

- **Maximizes Efficiency by Minimizing Body-Diode Conduction and Reverse Recovery Losses**
- **Transparent Synchronous Buck Gate Drive Operation From the Single Ended PWM Input Signal**
- **12-V or 5-V Input Operation**
- **3.3-V Input Operation With Availability of 12-V Bus Bias**
- **High-Side and Low-Side ±3-A Dual Drivers**
- **On-Board 6.5-V Gate Drive Regulator**
- **±3-A TrueDrive™ Gate Drives for High Current Delivery at MOSFET Miller Thresholds**
- **Automatically Adjusts for Changing Operating Conditions**
- **Thermally Enhanced 14-Pin PowerPAD™ HTSSOP Package Minimizes Board Area and Junction Temperature Rise**

FUNCTIONAL APPLICATION DIAGRAM



Note: 12-V input system shown. For 5-V input only systems, see Figure 6.

APPLICATIONS

- **Multiphase Converters in Combination With the TPS40090**
- **Non-Isolated 3.3-V, 5-V and 12-V Input dc-to-dc Converters for Processor Power, General Computer, Telecom and Datacom Applications**

DESCRIPTION

The UCC27223 is a high-speed synchronous buck drivers for today's high-efficiency, lower-output voltage designs. Using Predictive Gate Drive™ (PGD) control technology, these drivers reduce diode conduction and reverse recovery losses in the synchronous rectifier MOSFET(s).

The UCC27223 includes an enable pin that controls the operation of both outputs. A logic latch is also included to keep both outputs low until the first PWM input pulse comes in. The RDS(on) of the SR pull-down sourcing device is also minimized for higher frequency operations.

This closed loop feedback system detects body-diode conduction, and adjusts deadtime delays to minimize the conduction time interval. This virtually eliminates body-diode conduction while adjusting for temperature, load- dependent delays, and for different MOSFETs. Precise gate timing at the nanosecond level reduces the reverse recovery time of the synchronous rectifier MOSFET body-diode, reducing reverse recovery losses seen in the main (high-side) MOSFET. The lower junction temperature in the low-side MOSFET increases product reliability. Since the power dissipation is minimized, a higher switching frequency can also be used, allowing for smaller component sizes.

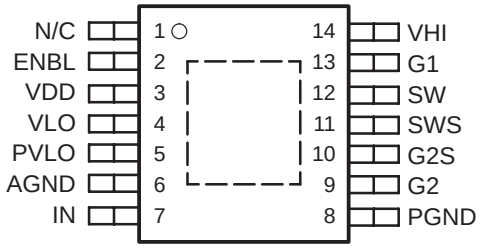
The UCC27223 is offered in the thermally enhanced 14-pin PowerPAD™ package with 2°C/W θ_{jc}.

Predictive Gate Drive™ and PowerPAD™ are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PWP PACKAGE
(TOP VIEW)



N/C − No internal connection

AVAILABLE OPTIONS

T_A	PWM INPUT (IN)	PACKAGED DEVICES
		PowerPAD™ HTSSOP−14 (PWP)
−40°C to 105°C	**NON-INVERTING**	UCC27223PWP

†The PWP package is available taped and reeled. Add R suffix to device type (e.g. UCC27223PWPR) to order quantities of 2,000 devices per reel and 90 units per tube.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage range, VDD . . . . . −0.3 to 20 V
Input voltage, VHI . . . . . 30 V
SW, SWS . . . . . 20 V
Supply current, I_{DD}, including gate drive current . . . . . 100 mA
Sink current (peak) pulsed, G1/G2 . . . . . 4.0 A
Source current (peak) pulsed, G1/G2 . . . . . −4.0 A
Analog inputs, IN, ENBL . . . . . −3.0 V to V_{DD} + 0.3 V, not to exceed 15 V
Power Dissipation at T_A = 25°C (PWP package) . . . . . 3 W
Operating junction temperature range, T_J . . . . . −55°C to 115°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to AGND and PGND. Currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12-V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VHI to SW, 0.1-µF and 2.2-µF capacitor from PVLO to PGND, PVLO tied to VLO, T_A = −40°C to 105°C for the UCC27223, T_A = T_J (unless otherwise noted)

VLO regulator

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Regulator output voltage	V_{DD} = 12 V,	I_{VLO} = 0 mA	6.2	6.5	6.8	V
	V_{DD} = 20 V,	I_{VLO} = 0 mA	6.2	6.5	6.8	
	V_{DD} = 10 V,	I_{VLO} = 100 mA	6.1	6.5	6.9	
Line Regulation	V_{DD} = 12 V to 20 V			2	10	mV
Load Regulation	I_{VLO} = 0 mA to 100 mA			15	40	
Short-circuit current(1)	V_{DD} = 8.5 V			220		mA
Dropout voltage, (VDD at 5% VLO drop)	VLO = 6.175 V,	I_{VLO} = 100 mA	7.1	7.8	8.5	V

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage	Measured at VLO	3.30	3.82	4.40	V
Minimum operating voltage after start		3.15	3.70	4.15	
Hysteresis		0.07	0.12	0.20	

bias currents

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{LO} bias current at VLO (ON), 5 V applications only	VLO = 4.5 V,	VDD = no connect	3.6	4.7	5.8	mA
V_{DD} bias current	VDD = 8.5 V		5.5	7.1	8.5	
	f_{IN} = 500 kHz,	No load on G1/G2	8	16	25	

input command (IN)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	10 V < VDD < 20 V	3.3	3.6	3.9	V
Low-level input voltage	10 V < VDD < 20 V	2.2	2.5	2.8	
Input bias current	V_{DD} = 15 V			1	µA

input (SWS)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level input threshold voltage	f_{IN} = 500 kHz, G2S = 0.0 V	$t_{ON, G2}$ maximum,	1.4	2.0	2.6	V
Low-level input threshold voltage	f_{IN} = 500 kHz, G2S = 0.0 V	$t_{ON, G2}$ minimum,	0.7	1.0	1.3	
	f_{IN} = 500 kHz,	$t_{ON, G1}$ minimum	−100	−300	−500	mV
Input bias current	SWS = 0.0 V		−0.9	−1.2	−1.5	mA

input (G2S)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level input voltage	f_{IN} = 500 kHz, SWS = 0.0 V	$t_{ON, G2}$ maximum,	1.4	2.0	2.6	V
Low-level input voltage	f_{IN} = 500 kHz, SWS = 0.0 V	$t_{ON, G2}$ minimum,	0.7	1.0	1.3	
Input bias current	G2S = 0 V		−370	−470	−570	µA

NOTE 1: Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12-V, 1-µF capacitor from VDD to GND, 1-µF capacitor from VHI to SW, 0.1-µF and 2.2-µF capacitor from PVLO to PGND, PVLO tied to VLO, T_A = −40°C to 105°C for the UCC27223, T_A = T_J (unless otherwise noted)

enable (ENBL)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
V_{IN_H}, high-level input voltage	LO to HI transition	2.25	2.45	2.85	V
V_{IN_L}, low-level input voltage	HI to LO transition	1.55	1.70	1.90	V
Hysteresis			1.1		V
R_{ENBL}, enable impedance	V_{DD} = 14 V, ENBL = GND	75	112	150	kΩ
t_{D3}, propagation delay time(5)			TBD		ns
t_{D4}, propagation delay time(5)			TBD		ns
t_r, Rise time	VLO = PVLO = 8.5 V		2.5		ms
tf, Fall time	VLO = PVLO = 8.5 V		2.5		ms

G1 main output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sink resistance	SW = 0 V, VHI = 6 V, IN = 0 V, G1 = 0.5 V	0.5	0.9	1.5	Ω
Source resistance(2)	SW = 0 V, VHI = 6 V, IN = 6.5 V, G1 = 5.5 V	10	25	45	Ω
Source current(1)(2)	SW = 0 V, VHI = 6 V, IN = 6.5 V, G1 = 3.0 V	−3	−3.3		A
Sink current(1)(2)	SW = 0 V, VHI = 6 V, IN = 0 V, G1 = 3.0 V	3	3.3		A
Rise time	C = 2.2 nF from G1 to SW, V_{DD} = 20 V		17	25	ns
Fall time	C = 2.2 nF from G1 to SW, V_{DD} = 20 V		17	25	ns

G2 SR output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sink resistance(2)	PVLO = 6.5 V, IN = 6.5 V, G1 = 0.25 V	0.5	1.6	4.0	Ω
Source resistance(2)	PVLO = 6.5 V, IN = 0 V, G2 = 6.0 V	10	20	35	Ω
Source current(1)(2)	PVLO = 6.5 V, IN = 0 V G2 = 3.25 V	3	3.3		A
Sink current(1)(2)	PVLO = 6.5 V, IN = 6.5 V G2 = 3.25 V	−3	3.3		A
Rise time(2)	C = 2.2 nF from G2 to PGND V_{DD} = 20 V		17	25	ns
Fall time	C = 2.2 nF from G2 to PGND V_{DD} = 20 V		20	35	ns

deadtime delay

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OFF, G2}$, IN to G2 falling		40	80	125	ns
$t_{OFF, G1}$, IN to G1 falling		55	80	110	ns
Delay Step Resolution		4.0	4.5	5.2	ns
$t_{ON, G1}$ minimum			−17		ns
$t_{ON, G1}$ maximum			49		ns
$t_{ON, G2}$ minimum			−15		ns
$t_{ON, G2}$ maximum			54		ns

NOTE 1: Ensured by design. Not production tested.

2: The pullup / pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

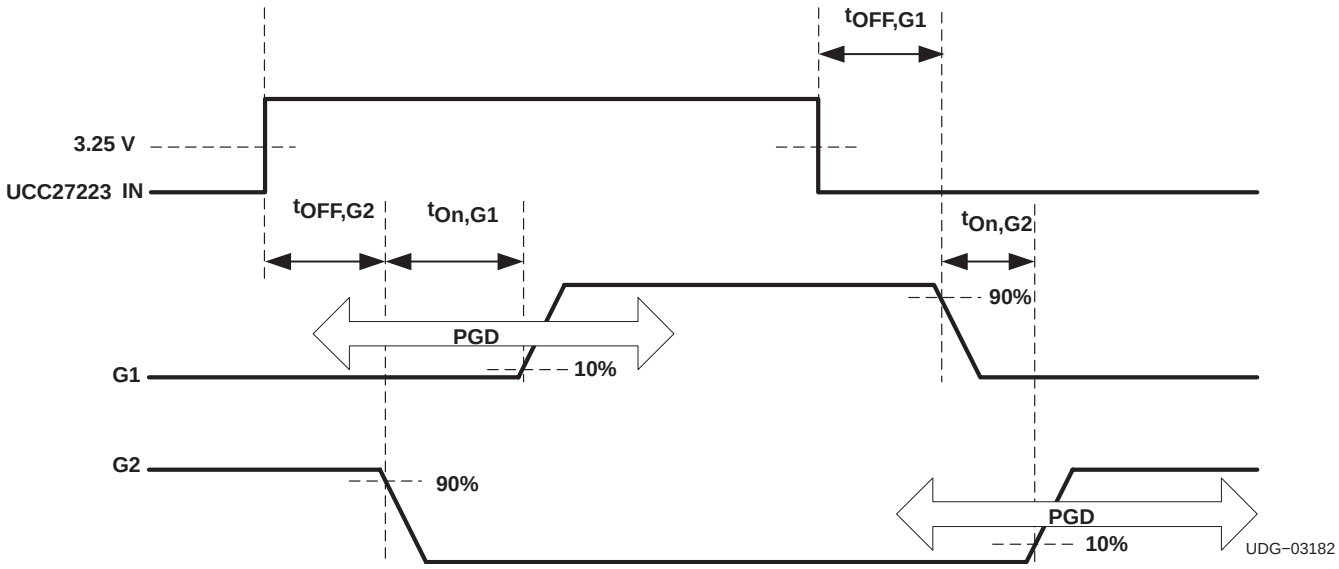
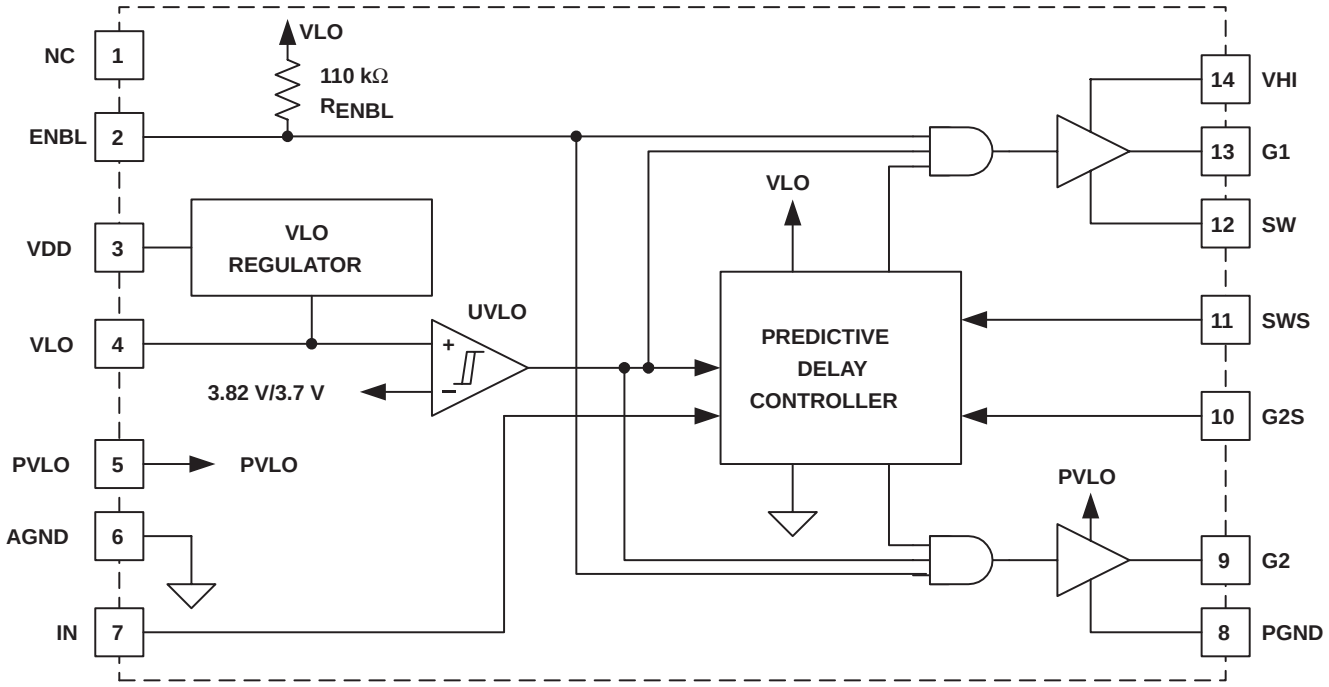


Figure 1. Predictive Gate Drive Timing Diagram

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6	−	Analog ground for all internal logic circuitry. AGND and PGND should be tied to the PCB ground plane with vias.
G1	13	O	High-side gate driver output that swings between SW and VHI.
G2	9	O	Low-side gate driver output that swings between PGND and PVLO.
G2S	10	I	Used by the predictive deadtime controller for sensing the SR MOSFET gate voltage to set the appropriate deadtime.
IN	7	I	Digital input command pin. A logic high forces on the main switch and forces off the synchronous rectifier.
PGND	8	−	Ground return for the G2 driver. Connect PGND to PCB ground plane with several vias.
PVLO	5	I	PVLO supplies the G2 driver. Connect PVLO to VLO and bypass on the PCB.
SW	12	−	G1 driver return connection.
SWS	11	I	Used by the predictive controller to sense SR body-diode conduction. Connect to SR MOSFET drain close to the MOSFET package.
VDD	3	I	Input to the internal VLO regulator. Nominal VDD range is from 8.5 V to 20 V. Bypass with at least 0.1 μF of capacitance.
VHI	14	I	Floating G1 driver supply pin. VHI is fed by an external Schottky diode during the SR MOSFET on-time. Bypass VHI to SW with an external capacitor.
VLO	4	O	Output of the VLO regulator and supply input for the logic and control circuitry. Connect VLO to PVLO and bypass on the PCB with a maximum capacitor value of 4.7 μF.
ENBL	2	I	Enable input that controls the operation of both outputs (G1 and G2). It is internally pulled up to VLO with a 110-kΩ resistor for active-high operation.

SIMPLIFIED BLOCK DIAGRAM



APPLICATION INFORMATION

predictive gate drive technique

The Predictive Gate Drive™ technology utilizes a digital feedback system to detect body-diode conduction, and then adjusts the deadtime delays to minimize it. This system virtually eliminates the body-diode conduction time intervals for the synchronous MOSFET, while adjusting for different MOSFETs characteristics, propagation and load dependent delays. Maximum power stage efficiency is the end result.

Two internal feedback loops in the predictive delay controller continuously adjusts the turn on delays for the two MOSFET gate drives G1 and G2. As shown in Figure 2, $t_{ON,G1}$ and $t_{ON,G2}$ are varied to provide minimum body-diode conduction in the synchronous rectifier MOSFET Q_2. The turn-off delay for both G1 and G2, $t_{OFF,G1}$ and $t_{OFF,G2}$ are fixed by propagation delays internal to the device.

The predictive delay controller is implemented using a digital control technique, and the time delays are therefore discrete. The turn-on delays, $t_{ON,\,G1}$ and $t_{ON,\,G2}$, are changed by a single step (typically 3 ns) every switching cycle. The minimum and maximum turn-on delays for G1 and G2 are specified in the electrical characteristics table.

APPLICATION INFORMATION

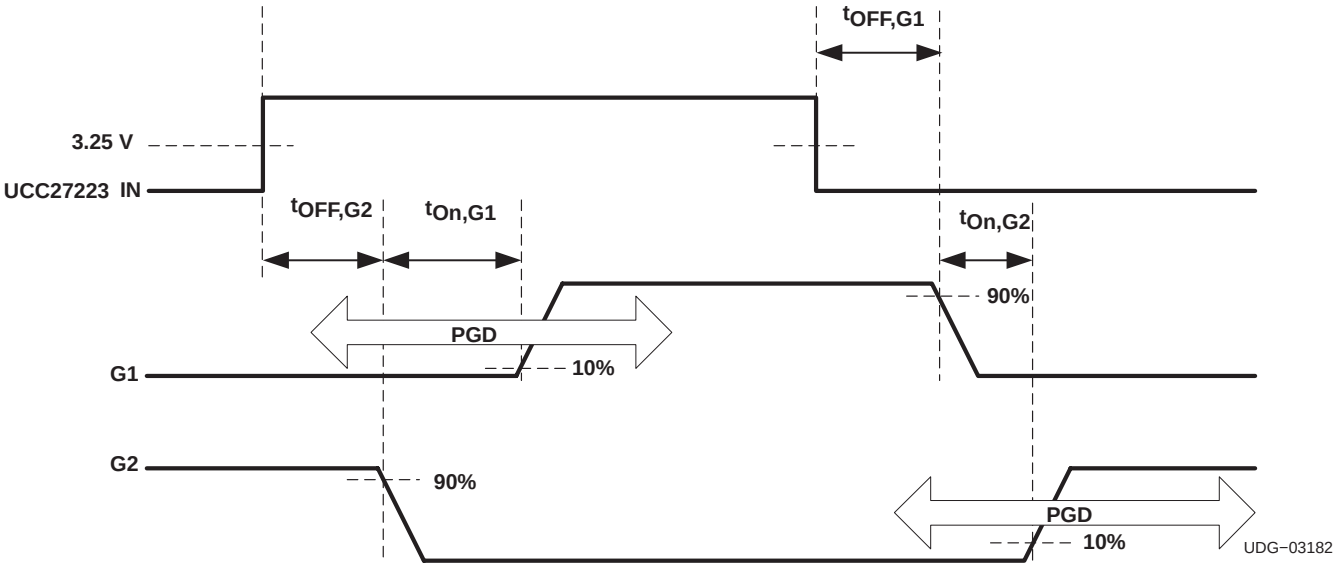


Figure 2. Predictive Gate Drive Timing Diagram

A typical application circuit for systems with 8.5-V to 20-V input is shown in Figure 3.

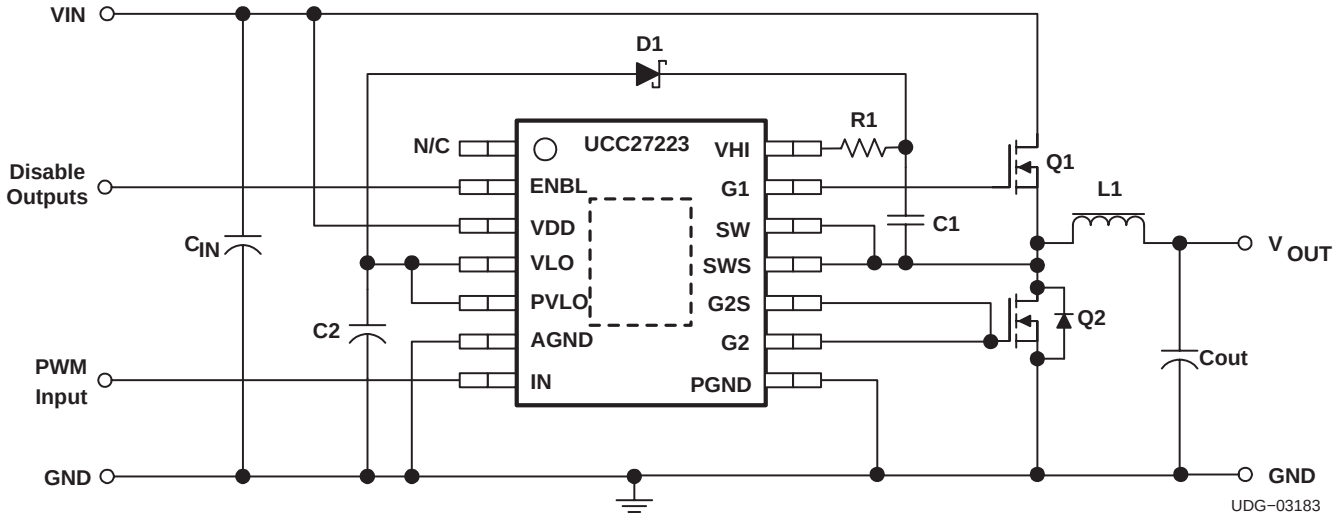


Figure 3. System Application: 8.5-V to 20-V Input

APPLICATION INFORMATION

selection of VHI series resistor R1 (dV/dt Considerations):

The series resistor R1 may be needed to slowdown the turn-on of the main forward switch to limit the dV/dt which can inadvertently turn on the synchronous rectifier switch. In nominal 12-V input designs, a R1 value of 4-Ω to 10-Ω can be used depending on the type of MOSFET used and the high-side/low-side MOSFET ratio. In 5-V or lower input applications however, R1 is not needed.

When the drain-source voltage of a MOSFET quickly rises, inadvertent dV/dt induced turn-on of the device is possible. This can especially be a problem for input voltages of 12 V or greater. As Q1 rapidly turns on, the drain-to-source voltage of Q2 rises sharply, resulting in a dV/dt voltage spike appearing on the gate signal of Q2. If the dV/dt induced voltage spike were to exceed the given threshold voltage, the MOSFET may briefly turn on when it should otherwise be commanded off. Obviously this undesired event would have a negative impact on overall efficiency.

Minimizing the dV/dt effect on Q2 can be accomplished by proper MOSFET selection and careful layout techniques. The details of how to select a MOSFET to minimize dV/dt susceptibility are outlined in SEM−1400, Topic 2, Appendix A, Section A5. Secondly, the switch node connecting Q1, Q2 and L1 should be laid out as tight as possible, minimizing any parasitic inductance, which might worsen the dV/dt problem.

If the dV/dt induced voltage spike is still present on the gate Q2, a 4W to 10W value of R1 is recommended to minimize the possibility of inadvertently turning on Q2. The addition of R1 slows the turn-on of Q1, limiting the dV/dt rate appearing on the drain-to-source of Q2. Slowing down the turn-on of Q1 will result in slightly higher switching loss for that device only, but the efficiency gained by preventing dV/dt turn-on of Q2 will far outweigh the negligible effect of adding R1.

When Q2 is optimally selected for dV/dt robustness and careful attention is paid to the PCB layout of the switch node, R1 may not be needed at all, and can therefore be replaced with a 0-Ω jumper to maintain high efficiency. The goal of the designer should not be to completely eliminate the dV/dt turn-on spike but to assure that the maximum amplitude is less than the MOSFET gate-to-source turn-on threshold voltage under all operating conditions.

selection of bypass capacitor C1

Bypass capacitors should be selected based upon allowable ripple voltage, usually expressed as a percent of the regulated power supply rail to be bypassed. In all of the UCC27223 application circuits shown herein, C1 provides the bypass for the main (high-side) gate driver. Every time Q1 is switched on, a packet of charge is removed from C1 to charge Q1's gate to approximately 6.0 V. The charge delivered to the gate of Q1 can be found in the manufacturer's datasheet curves. An example of a gate charge curve is shown in Figure 4.

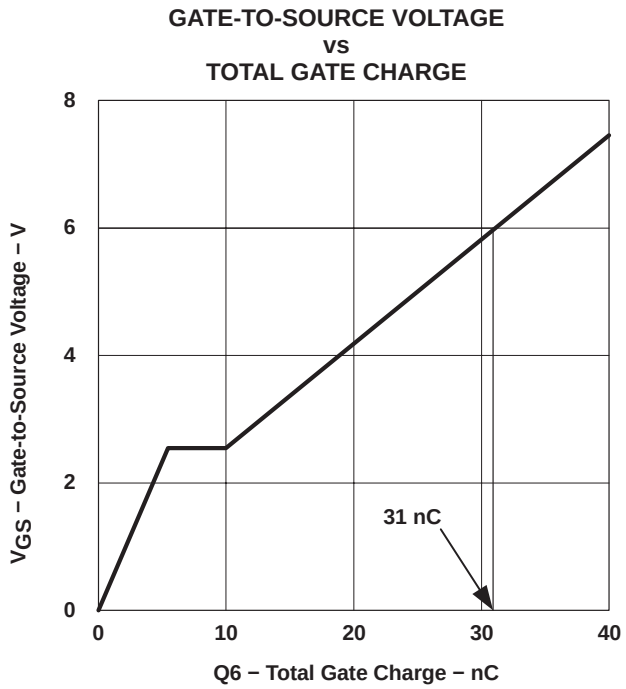


Figure 4.

As shown in Figure 4, 31 nC of gate charge is required in order for Q1's gate to be charged to 6.0 V, relative to its source. The minimum bypass capacitor value can be found using the following calculation:

$$C1_{MIN} = \frac{Q_G}{k \times \left(VHI - V_{SW}\right)} \quad (1)$$

where k is the percent ripple on C1, Q_G is the total gate charge required to drive the gate of Q1 from zero to the final value of (VHI−VSW). In this example gate charge curve, the value of the quantity (VHI−VSW) is taken to be 6.0 V. This value represents the nominal VLO regulator output voltage minus the forward voltage drop of the external Schottky diode, D1. For the MOSFET with the gate charge described in Figure 4, the minimum capacitance required to maintain a 3% peak-to-peak ripple voltage can be calculated to be 172 nF, so a 180-nF or a 220-nF capacitor could be used. The maximum peak-to-peak C1 ripple must be kept below 0.4 V for proper operation.

APPLICATION INFORMATION

selection of MOSFETs

The peak current rating of a driver imposes a limit on the maximum gate charge of the external power MOSFET driven by it. The limit is based on the amount of time needed to deliver or remove the required charge to achieve the desired switching speed during turn-on and turn-off of the external transistor. Hence, there are the families of gate driver circuits with different current ratings.

To demonstrate this, assume a constant time interval for the switching transition and a fixed gate drive amplitude. A larger MOSFET with more gate charge will require higher current capability from the driver to turn-on or turn-off the device in the same amount of time. Accordingly, there is a practical upper limit on gate charge which can be driven by the UCC27223. Considering the current capability of the TrueDrive™ output stage and the available dynamic range (delay adjust range) of the Predictive Gate Drive™ circuitry, this limit is approximately 120 nC of gate charge.

Some higher current applications require several MOSFETs to be connected parallel and driven by the same gate drive signal. If their combined gate charge exceeds 120 nC, the rise and fall times of the gate drive signals will extend and limit the delay adjust range of the PGD circuit in the UCC27223. This may limit the benefits of the PGD technology under certain operating conditions.

Note that there are additional considerations in the gate drive circuit design which influence the maximum gate charge of the external MOSFETs. The most significant of these is the operating frequency which, together with the amount of gate charge, will define the power dissipation in the driver. The allowable power dissipation is a function of the maximum junction and operating temperatures, thermal and reliability considerations.

selection of bypass capacitor C2

C2 supplies the peak current required to turn on the Q2 synchronous rectifier MOSFET, as well as the peak current to charge the C1 capacitor through the bootstrap diode. Since the synchronous MOSFET is turned on with 0 V across its drain-to-source, there is no Miller, or gate-to-drain charge. Therefore the synchronous MOSFET gate can be modeled as a simple linear capacitance. The value of this capacitance can be found from the datasheet's gate charge curve. Referring to Figure 5, the slope of the curve past the Miller plateau indicates the equivalent gate capacitance. Because the Y-axis is described in volts, the capacitance is actually the inverse of the slope of the curve. For example, the curve in Figure 4 has a slope of approximately 2 V / 12 nC over the gate charge range of 10 nC to 40 nC. The equivalent capacitance is 12 nC / 2 V = 6 nF. With the equivalent capacitance, the minimum bypass capacitor value can be calculated as:

$$C2_{MIN} = \frac{C_{EQ}}{k} \tag{2}$$

where

- C_{EQ} is the equivalent gate capacitance,
- k is the voltage ripple on C2, expressed as a percentage

For a peak-to-peak ripple of 3%, the minimum C2 capacitor value is calculated to be 200 nF. A 220-nF capacitor would be used in this case. $C2_{MAX}$ should not exceed 4.7 µF. In addition to the calculated capacitance, a 100-nF low ESL by-pass capacitor should be placed as close to the UCC27223 chip as possible. The capacitor provides the transient currents needed by the drive stage and prevents UVLO shutdown of the driver during turn-on.

APPLICATION INFORMATION

regulator current and power dissipation

The regulator current can be calculated from the dc or average current required by the two gate drivers. This current can be expressed as:

$$I_{REG} = F_{SW} \times \left(C_{EQ} \times VLO + Q_G\right) \quad (3)$$

Assuming all the power dissipation is internal to the device, and the internal bias current is negligible, the power dissipated by the device is:

$$P_{DIS} = F_{SW} \times \left(C_{EQ} \times VLO + Q_G\right) \times VDD \quad (4)$$

For a 500-kHz design, using MOSFETs with the gate charge characteristics shown in Figure 4 for both Q1 and Q2, the average regulator current would be 35 mA, and, when operated from a 12-V input rail, the resulting power dissipation is calculated to be 420 mW.

systems using 3.3-V or 5-V power input and 12-V gate drive

Figure 5 shows a schematic for systems where the power bus input is 5 V and 12 V is available for powering the gate drives. This system provides the 6.5-V gate drive to both MOSFETs, while the power stage operates off the 3.3-V or 5-V bus.

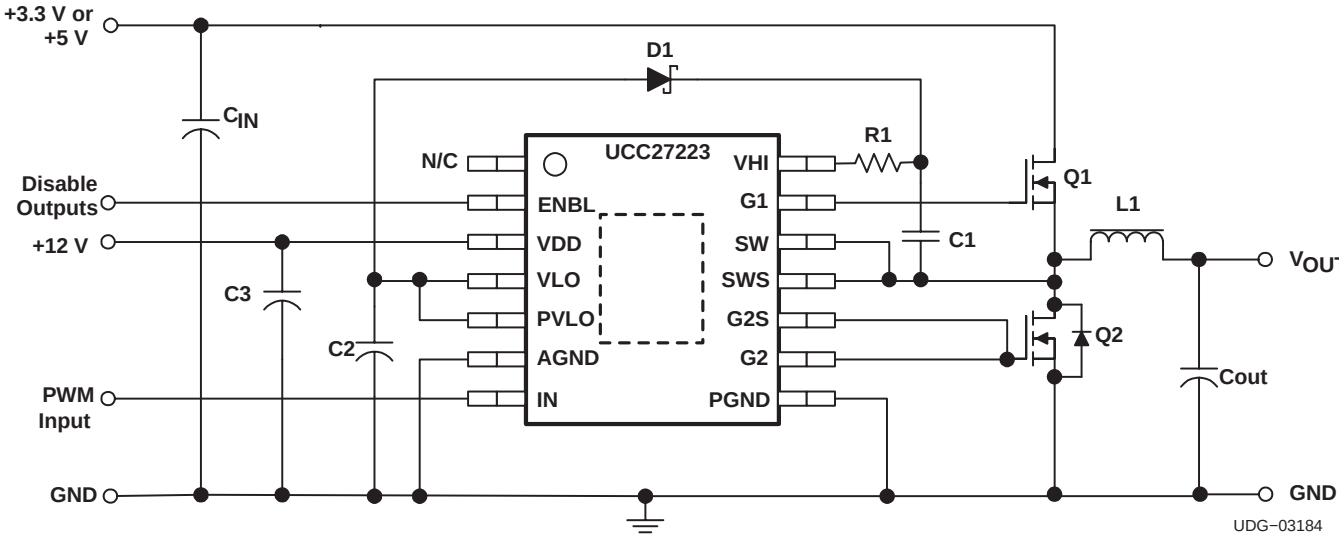


Figure 5. System Application: 3.3-V or 5-V Power Input with 12 V Available for Gate Drive

Note that the series resistor R1 may be needed to slowdown the turn-on of the main forward switch to limit the dV/dt which can inadvertently turn on the synchronous rectifier switch. The dV/dt considerations and the selection of R1 are discussed in the previous section.

APPLICATION INFORMATION

systems with 5-V input only

The circuit pictured in Figure 6 starts up from a 5-V input bus and provides a 6.5-V gate drive to the power MOSFETs. This circuit uses a charge pump consisting of D_3, D_4 and C_3 to effectively double the input voltage and apply this to the input of the linear regulator. The regulator then regulates the doubled input voltage to the 6.5-V nominal for VLO.

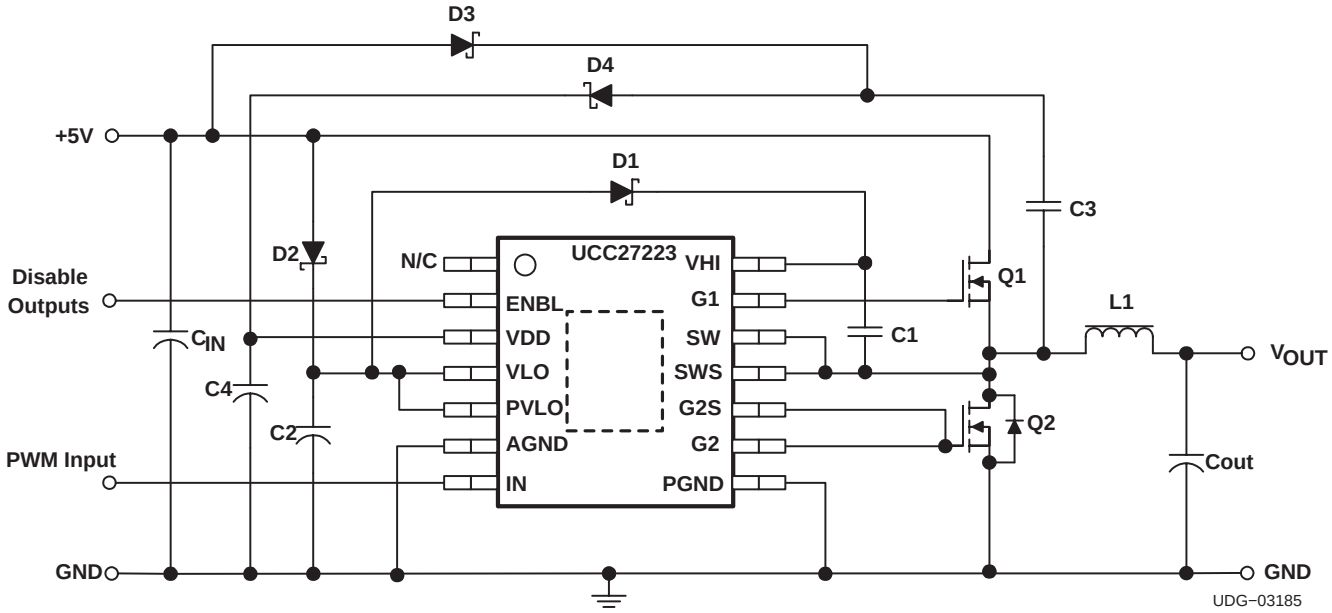


Figure 6. System Application: 5-V-Only Power Input with 6.5-V Gate Drive Using Charge Pump Circuit

selecting D_2, D_3, and D_4

Selection of suitable diodes is based upon the conducted peak and average currents. D2 simply provides a path to charge C2 at converter power-up. Virtually any one of the common BAT54 series of Schottky diodes can be used. To select D3 and D4, the peak currents of these two diodes need to be taken into account. First, the average current flowing in both D3 and D4 is the same as the regulator current described in equation (3). The peak currents in D3 and D4 are described as:

$$I_{D3PK} = \frac{I_{REG}}{1 - D} \quad (5)$$

$$I_{D4PK} = \frac{I_{REG}}{D} \quad (6)$$

For most UCC272223applications, the duty cycle is much less than 50%, and the peak current in D3 is quite reasonable. However, the peak current in D4 is quite high. This high peak current requires using a diode with a higher current rating for D4.

To maintain a reasonable charge pump efficiency, BAT54-type diodes can be used for applications where the peak currents are below approximately 40 mA. For applications where the peak current is greater than 40 mA, a 350-mA or 500-mA diode should be used. A typical 350-mA diode is SD103CW, SOD−123 package, manufactured by Diodes Inc. A typical 500-mA diode is the ZHCS500, SOT−23 package, available from Zetex Inc.

APPLICATION INFORMATION

selection of the flying capacitor C3

The flying capacitor is subjected to large peak currents, and to keep the peak-to-peak ripple voltage low, this capacitor has to be larger than C1 and C2. Selection of C3 should be done based on allowable peak-to-peak ripple on C3:

$$C3_{MIN} = \frac{I_{REG}}{F_{SW} \times k \times \left(VIN - V_{FD3}\right)} \quad (7)$$

where I_{REG} is the regulator output current, F_{SW} is the switching frequency, k is the percent ripple on C3, and V_{FD2} is the forward drop of D3.

selection of bypass capacitor C4

The bypass capacitor C4 needs to be sized to take the peak current from the charge pump diode D4. The capacitor is sized based on allowable ripple voltage:

$$C_{MIN} = \frac{I_{REG} \times (1 - D)}{F_{SW} \times k \times \left(2 \times VIN - V_{FD3} - V_{FD4}\right)} \quad (8)$$

where V_{FD3} and V_{FD4} are the forward voltages of D3 and D4 and k is the percent ripple allowed on C4.

enable pin and driver operation at start-up

In the UCC27223, an active-high ENBL function is implemented on pin 2. This pin when pulled low will shut off both G1 and G2 outputs regardless of the state of the PWM input signal. The ENBL pin is pull up to VLO internally with a 110-kΩ resistor so that the chip will be functional if the pin is left open. Enable thresholds are 2.45 V on, and 1.7 V off. The UCC27223 also includes a logic latch to keep both outputs low at start-up even when V_{DD} is past UVLO turn-on threshold. Both outputs will always be low until the first PWM input signal comes in.

APPLICATION INFORMATION

synchronous rectification and predictive delay

In a normal buck converter, when the main switch turns off, current is flowing to the load in the inductor. This current cannot be stopped immediately without using infinite voltage. For the current path to flow and maintain voltage levels at a safe level, a rectifier or catch device is used. This device can be either a conventional diode, or it can be a controlled active device if a control signal is available to drive it. The UCC27223 provides a signal to drive an N-channel MOSFET as a rectifier. This control signal is carefully coordinated with the drive signal for the main switch so that there is minimum delay from the time that the rectifier MOSFET turns off and the main switch turns on, and minimum delay from when the main switch turns off and the rectifier MOSFET turns on. This scheme, Predictive Gate Drive™ delay, uses information from the current switching cycle to adjust the delays that are to be used in the next cycle. Figure 7 shows the switch-node voltage waveform for a synchronously rectified buck converter. Illustrated are the relative effects of a fixed-delay drive scheme (constant, pre-set delays for the turnoff to turn on intervals), an adaptive delay drive scheme (variable delays based upon voltages sensed on the current switching cycle) and the predictive delay drive scheme.

Note that the longer the time spent in body-diode conduction during the rectifier conduction period, the lower the efficiency. Also, not described in Figure 7 is the fact that the predictive delay circuit can prevent the body diode from becoming forward biased at all while at the same time avoiding cross conduction or shoot through. This results in a significant power savings when the main MOSFET turns on, and minimizes reverse recovery loss in the body diode of the rectifier MOSFET.

The power dissipation on the main (forward) MOSFET is reduced as well, although that savings is not as significant as the savings in the rectifier MOSFET.

During reverse recovery the body diode is still forward biased, thus the reverse recovery current goes through the forward MOSFET while the drain−source voltage is still high, causing additional switching losses. Without PGD during this switching transition, Vds = Vin and Ids = Iload + Irr in the main MOSFET. With PGD however, Vds = Vin and Ids = Iload. The reduction in current accounts for additional power savings in the main MOSFET.

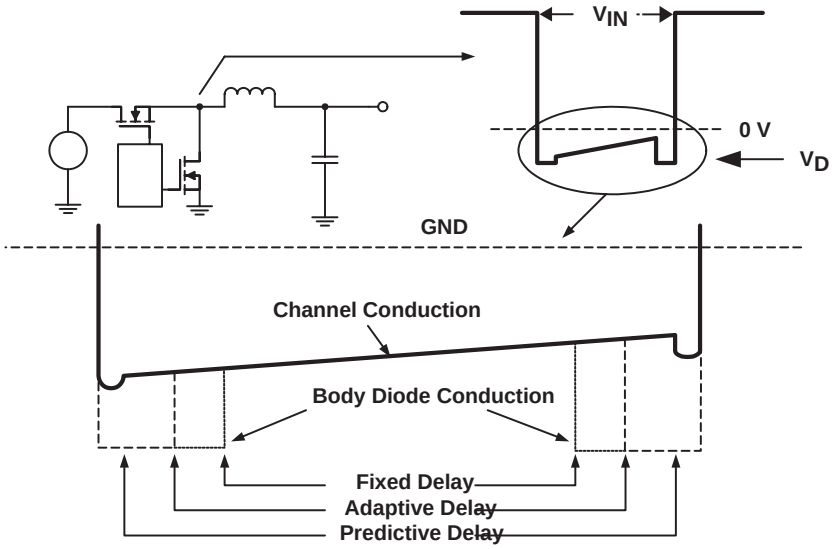


Figure 7. Switch Node Waveforms for Synchronous Buck Converter

APPLICATION INFORMATION

comparison between predictive and adaptive gate drive techniques

The first synchronous rectifier controllers had a fixed turn-on delay between the two gate drivers. The advantage of this well-known technique is its simplicity. The drawbacks include the need to make the delay times long enough to cover the entire application of the device and the temperature and lot-to-lot variation of the time delay. Since the body-diode of the synchronous rectifier conducts during this deadtime, the efficiency of this technique varies with different MOSFETs, ambient temperature, and with the lot-to-lot variation of the deadtime delay.

To combat the variability of the internal time delays, second generation controllers used state information from the power stage to control the turn-on of the two gate drivers. This technique is usually referred to as adaptive gate drive technique and is pictured in FIgure 8.

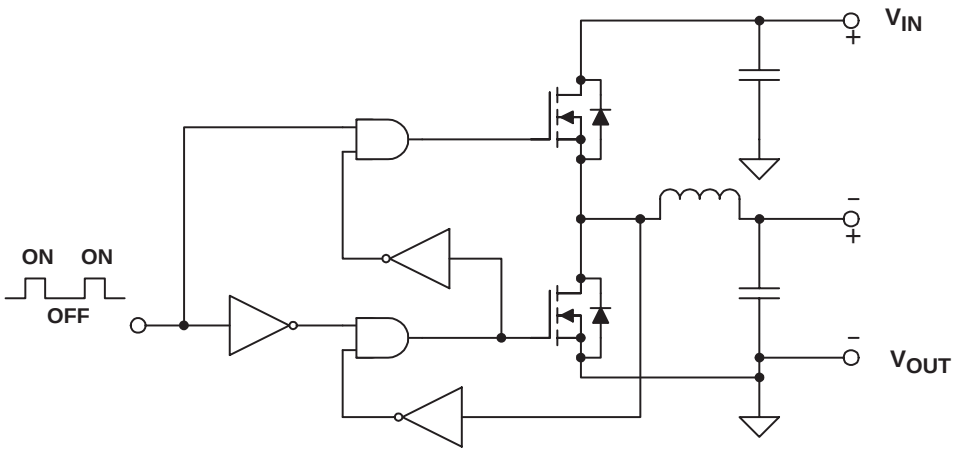


Figure 8. Adaptive Gate Drive Technique

The main advantage of the adaptive technique is the on-the-fly delay adjustment for different MOSFETs and temperature-variable time delays. The disadvantages include the body-diode conduction time intervals caused by delays in the cross-coupling loops and the inability to compensate for the delay to charge the MOSFET gates to the threshold levels. Additionally, it is difficult to determine whether the synchronous MOSFET channel is off by solely monitoring the SR MOSFET gate voltage. Some devices actually add a programmable delay between the turn-off of the synchronous rectifier and the turn-on of the main MOSFET via an external capacitor. This added delay directly affects the power stage efficiency through additional body-diode conduction losses. Since these losses are centralized in the synchronous MOSFET, the stress and temperature rise in this component becomes a major design headache.

The third-generation predictive control technique is different from the adaptive technique in that it uses information from the previous switching cycle to set the deadtime for the current cycle. The adaptive technique on the other hand uses the current state information to set the delay times. The inherent feedback loop propagation delays cause body-diode conduction.

APPLICATION INFORMATION

adaptive vs. predictive waveforms

Figures 9 through 11 illustrate the adaptive (left) vs. predictive (right) switching waveforms. Key comparison regions are denoted with (A), (B), (C), (D), and (E) for the adaptive control waveforms and (A′), (B′), (C′), (D′), and (E′) for the predictive control waveforms. Figures 10 and 11 are close-ups of each transition edge.

At (A), the propagation delay from sensing the synchronous rectifier gate going low to the high-side gate going high results in approximately 60 ns of body-diode conduction shown at (B). With the predictive drive, as soon as the body-diode conduction of the SR MOSFET (B) is sensed, the high-side turn-on delay is adjusted to minimize the body-diode conduction time (B′).

At (A′), the high side gate-to-source voltage is increasing while the synchronous rectifier gate-to-source voltage is decreasing. A natural result of the precise timing of the high-side MOSFET turn-on is shown at (C) and (C′). The overshoot and ringing for the predictive drive (C′) has much smaller amplitude than the adaptive drive (C) due a reduction in reverse recovery in the SR MOSFET body diode. This reduction in reverse recovery is only possible with the extremely precise gate timing used in the predictive drive technique.

At (D), the propagation delay from the synchronous rectifier drain-to-source voltage falling to the gate-to-source voltage rising causes the body diode of the SR MOSFET to conduct for approximately 60 ns (E). When the predictive drive is enabled (D′), the inherent delay is eliminated and virtually no body-diode conduction is shown at (E′).

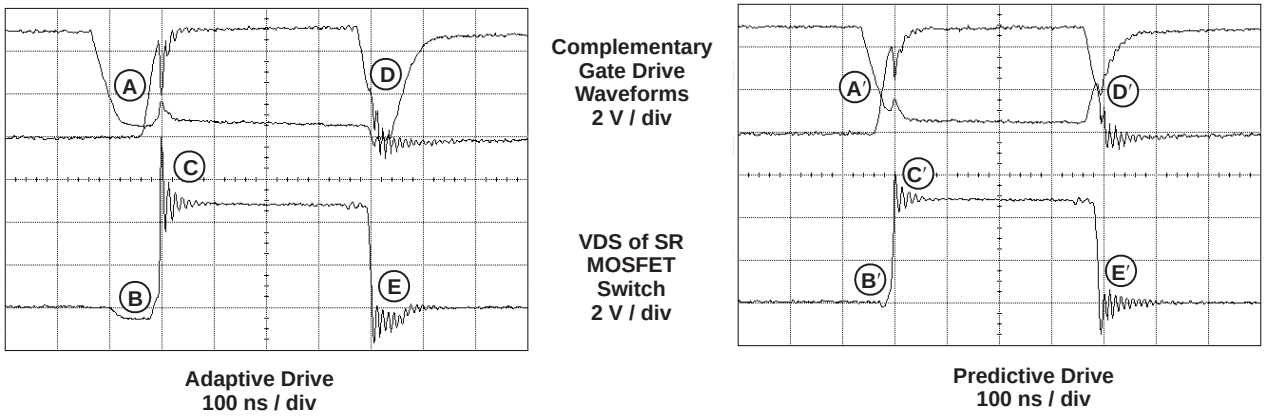


Figure 9. Adaptive vs. Predictive Switching Waveforms

APPLICATION INFORMATION

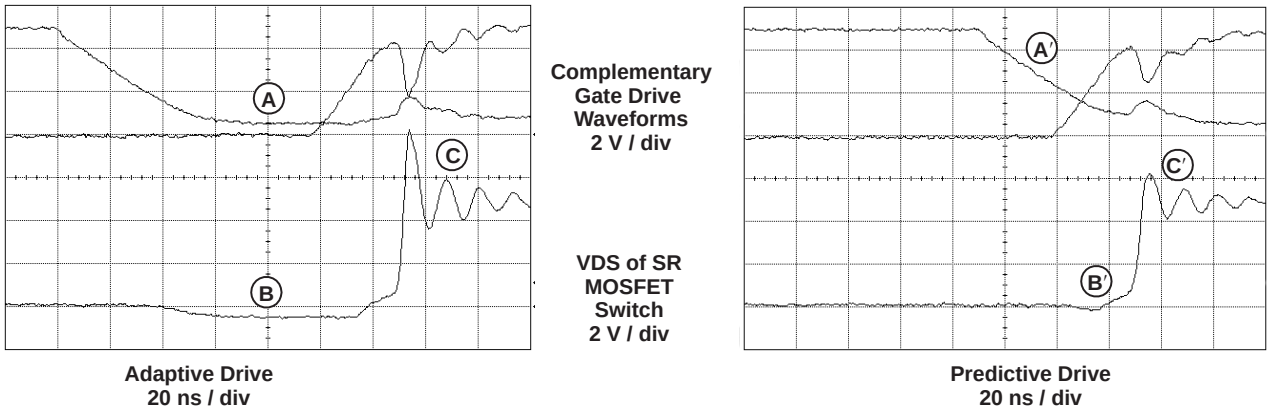


Figure 10. Close-Up: Turn-Off of Synchronous Rectifier Switch to Turn-On of Main Switch

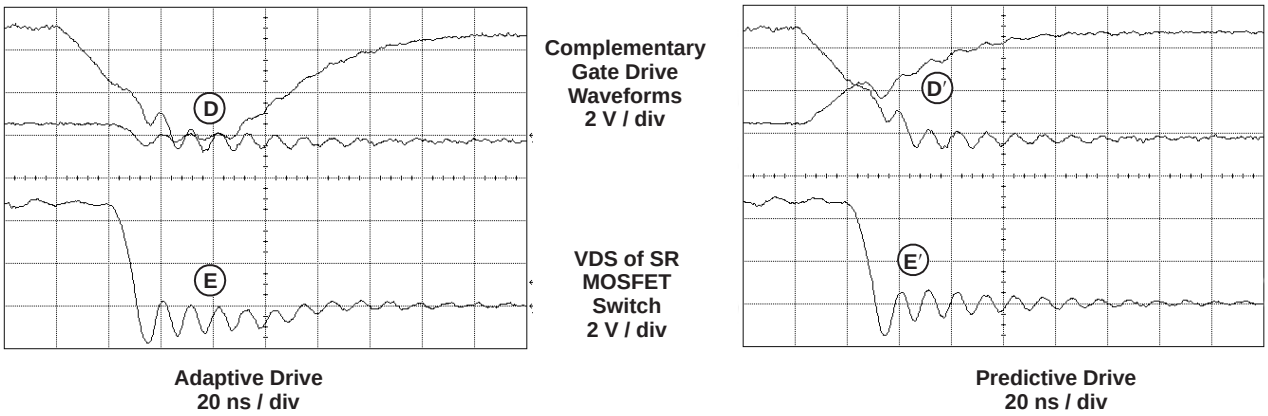


Figure 11. Close-Up: Turn-Off of Main Switch to Turn-On of Synchronous Rectifier Switch

efficiency comparison

Figures 12 through 15 show a series of efficiency measurements taken at two output voltages (0.9 V and 1.8 V) and two switching frequencies (250 kHz and 500 kHz) for both predictive and adaptive delay techniques.

The efficiency gain using the predictive technique is 1% for a V_{OUT} level of 1.8 V and at a switching frequency of 250 kHz (Figure 12). Figures 13 and 14 show the efficiency gain approximately doubles when V_{OUT} is lowered by a factor of two (to 0.9 V), or when the switching frequency is doubled to 500 kHz. With both doubled frequency and one-half of the output voltage, the efficiency gain of predictive technology is about 4% over the adaptive technology (Figure 15). Therefore, as the switching frequency increases and output voltages are lowered, the efficiency gains are higher. This results in lower operational temperatures for increased reliability as well as smaller size designs for increased frequencies.

APPLICATION INFORMATION

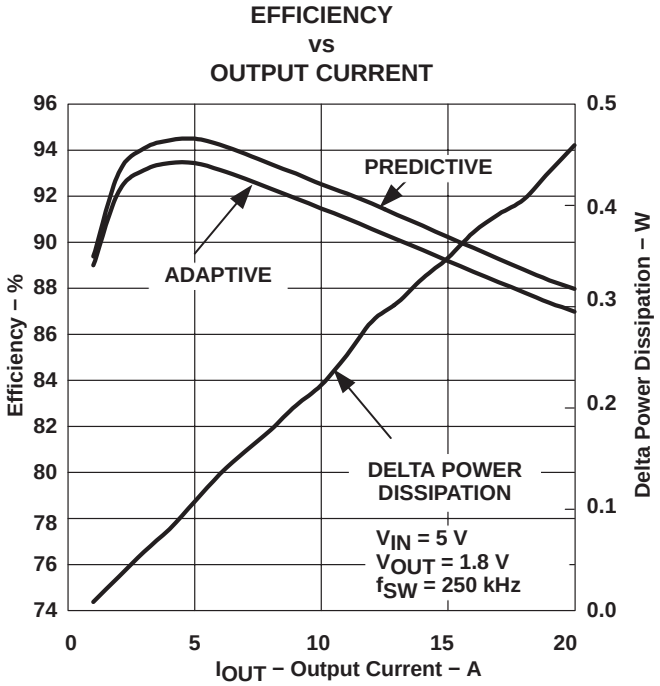


Figure 12

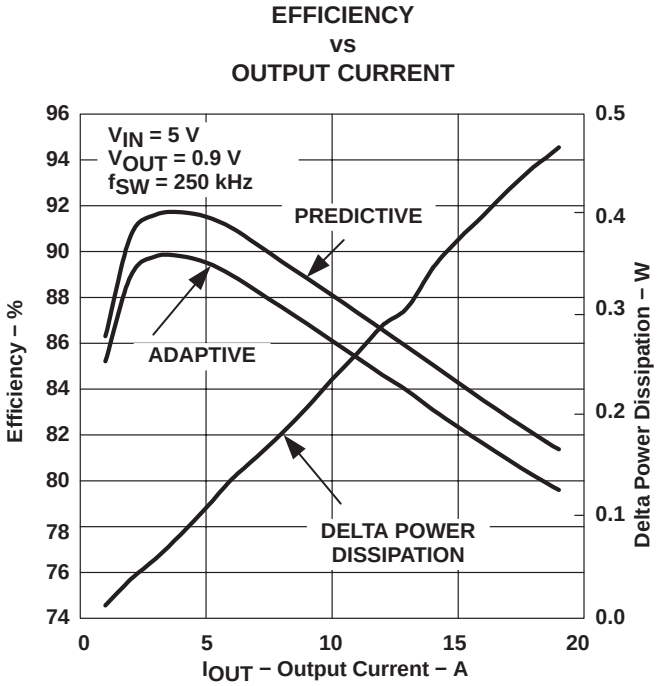


Figure 13

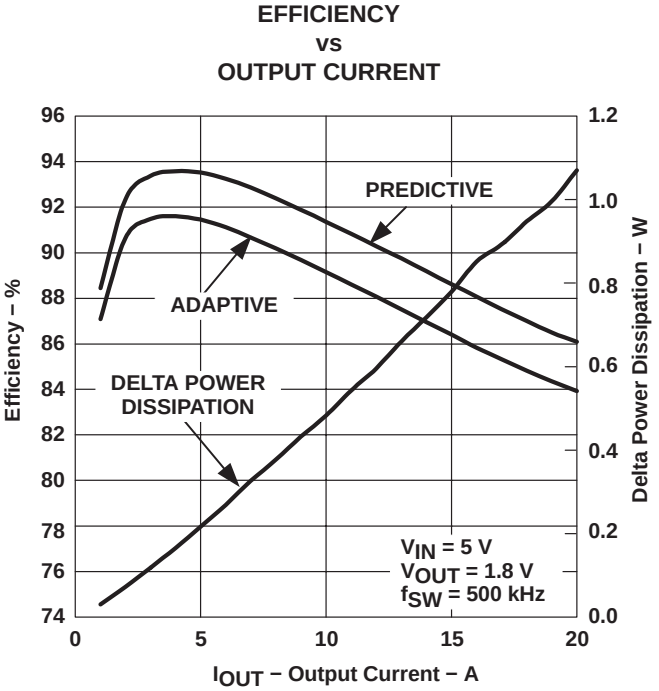


Figure 14

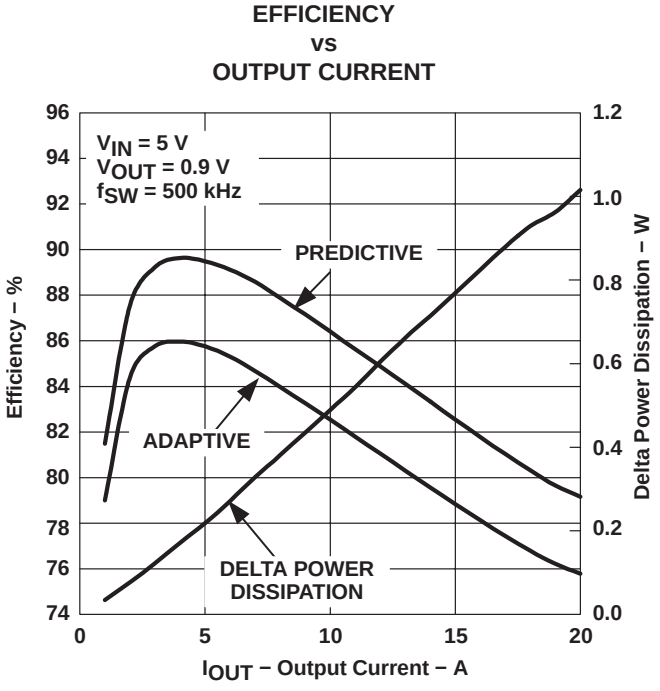


Figure 15

LAYOUT CONSIDERATIONS

packaging

The UCC27223 is only available in TI's thermally enhanced 14-pin PowerPad™ package. This package offers exceptional thermal impedance with a junction-to-case rating of 2°C/W. Shown as the crosshatched region in Figure 16, PowerPad™ includes an exposed leadframe die pad located on the bottom side of the package. Exposed pad dimensions for the PowerPad™ TSSOP 14-pin package are 69 mils x 56 mils (1.8 mm x 1.4 mm). However, the exposed pad tolerances can be + 41 / − 2 mils (+ 1.05 /− .05 mm) due to position and mold flow variation. Effectively removing the heat from the PowerPAD™ package requires a thermal land area, shown as the shaded gray region in Figure 16, designed into the PCB directly beneath the package. A minimum thermal land area of 5 mm by 3.4 mm is recommended as illustrated in Figure 16. Any tolerance variances of the exposed PowerPad™ falls well within the thermal land area when the recommended minimum land area is included on the printed circuit board. In addition, a 2-by-3 array of 13-mil thermal vias is required within the exposed PowerPad™ area, as shown in Figure 16. If additional heat sinking capability is required, larger 25-mil vias can be added to the thermal land area.

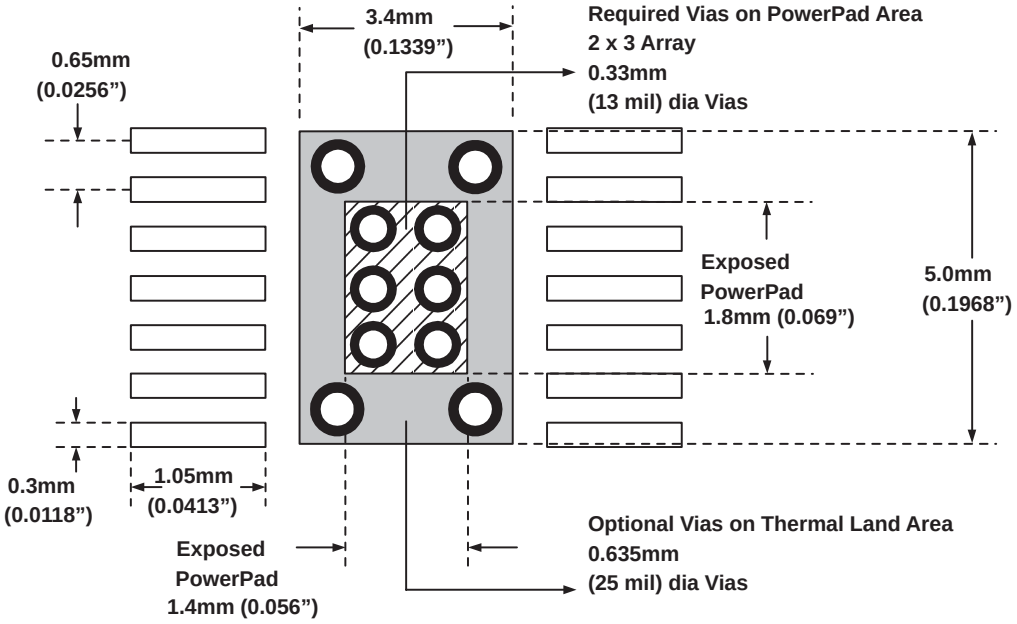


Figure 16. TSSOP−14PWP Package Outline and Minimum PowerPAD™ PCB Thermal Land

REFERENCE DESIGN AND EVALUATION MODULE

A reference design is discussed in, 5 *V to 0.9 V − 1.8 V (adjustable), 20-A High Efficiency Synchronous Buck Converter Using the UCC27223 with Predictive Gate Drive*™, TI Literature Number SLUU181 and accompanying evaluation module UCC27223EVM. The design highlights UCC27223 and its Predictive Gate Drive™ synchronous buck operation using a simple single ended PWM controller. The schematic is shown in Figure 17.

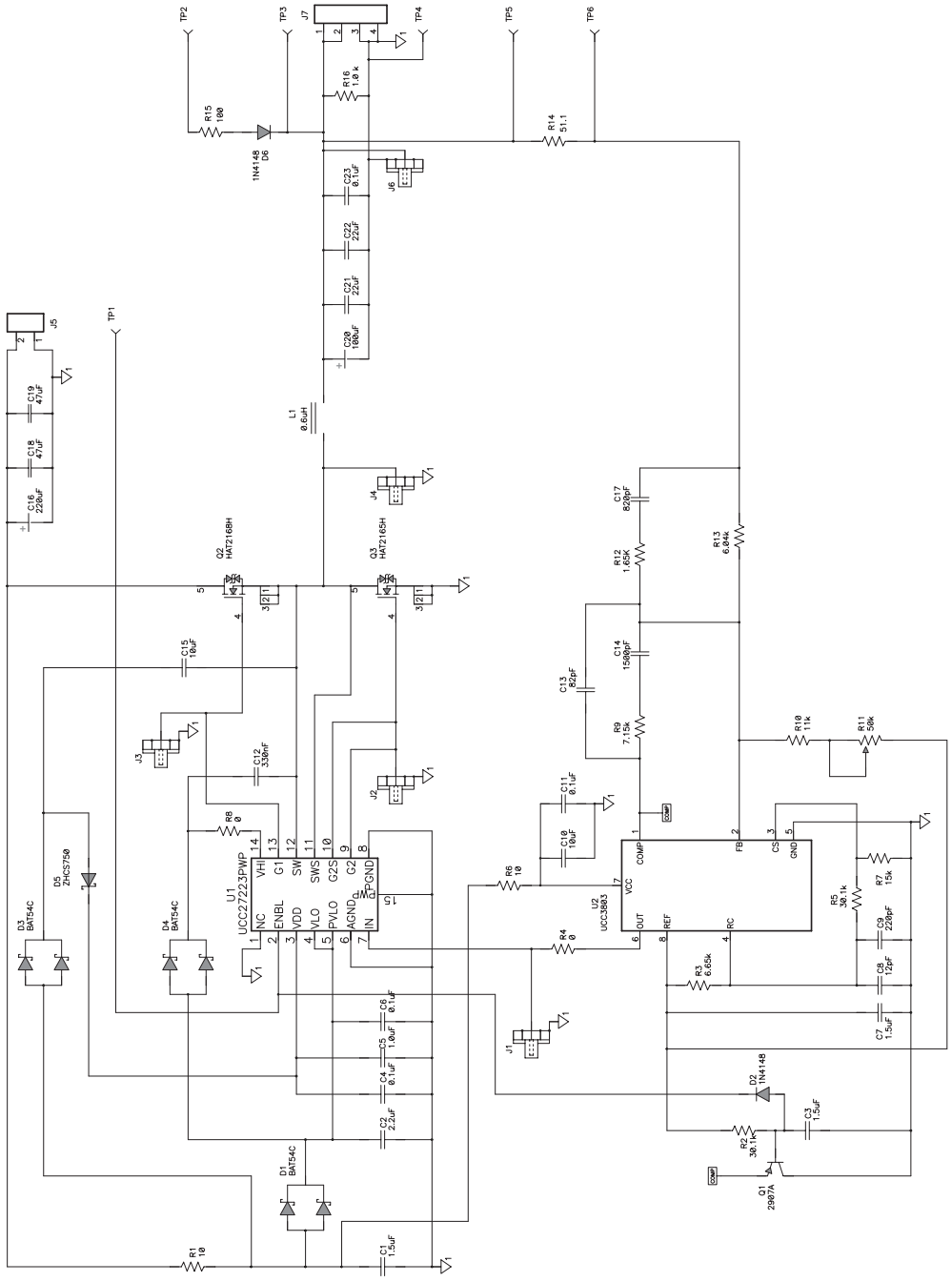


Figure 17. Typical Application Diagram

TYPICAL CHARACTERISTICS

BIAS CURRENT vs TEMPERATURE (NO LOAD)

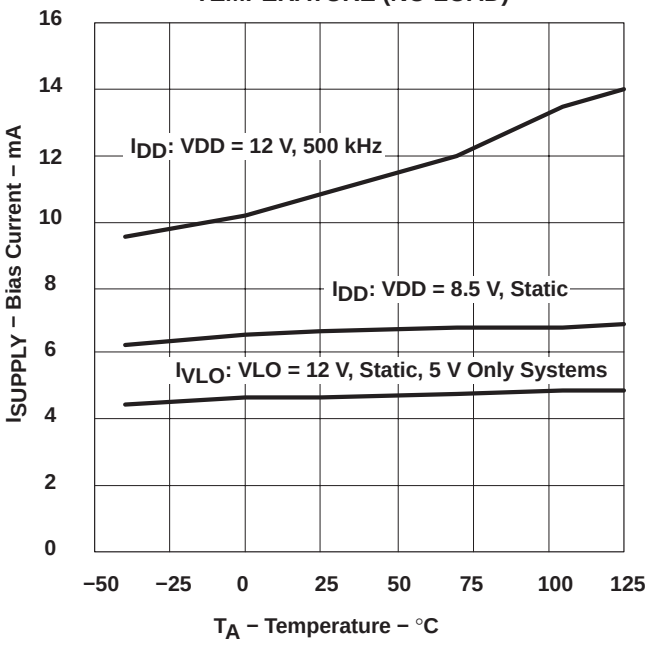


Figure 18

UVLO THRESHOLD vs TEMPERATURE

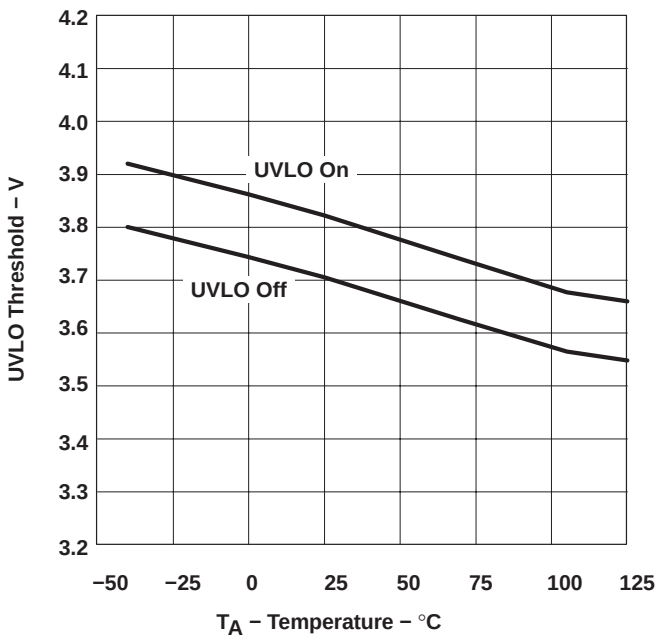


Figure 19

VLO LINE REGULATION vs TEMPERATURE (NO LOAD, IVLO = 0 mA)

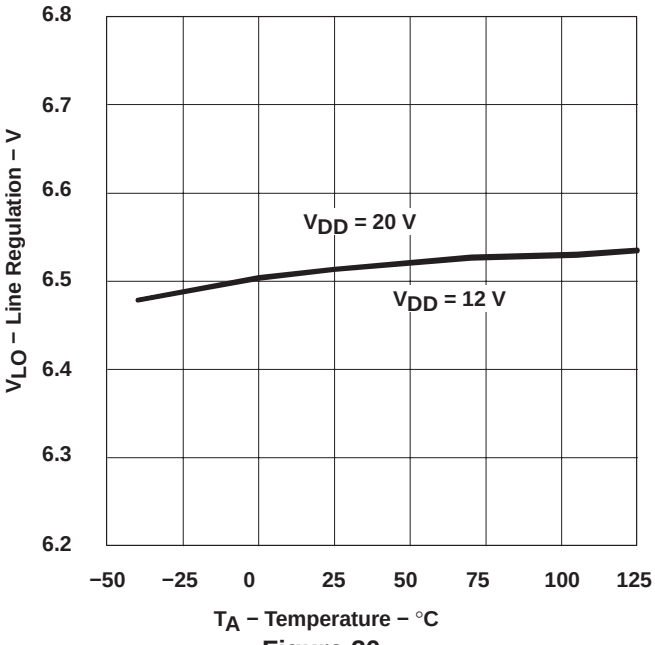


Figure 20

VLO LOAD REGULATION vs TEMPERATURE

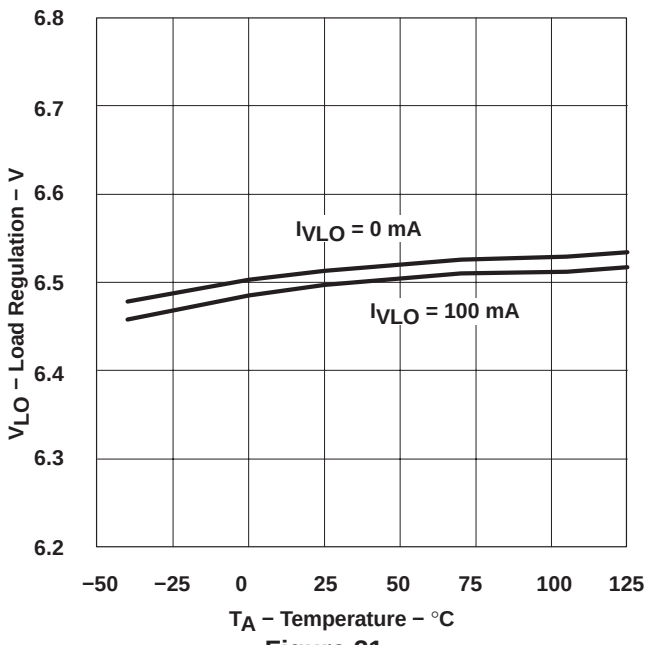


Figure 21

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE (VDD AT VLO = 6.175 V)
vs
OUTPUT CURENT

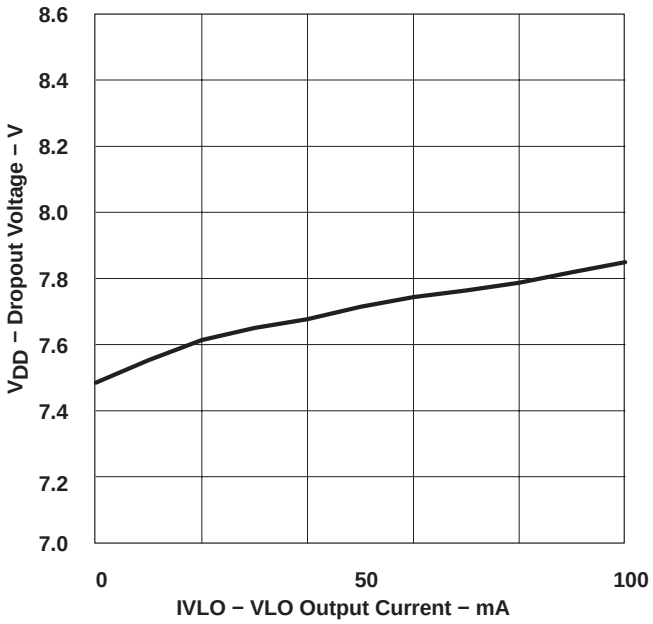


Figure 22

DROPOUT VOLTAGE (VDD AT VLO = 6.175 V)
vs
TEMPERATURE (I_{VLO} = 100 mA)

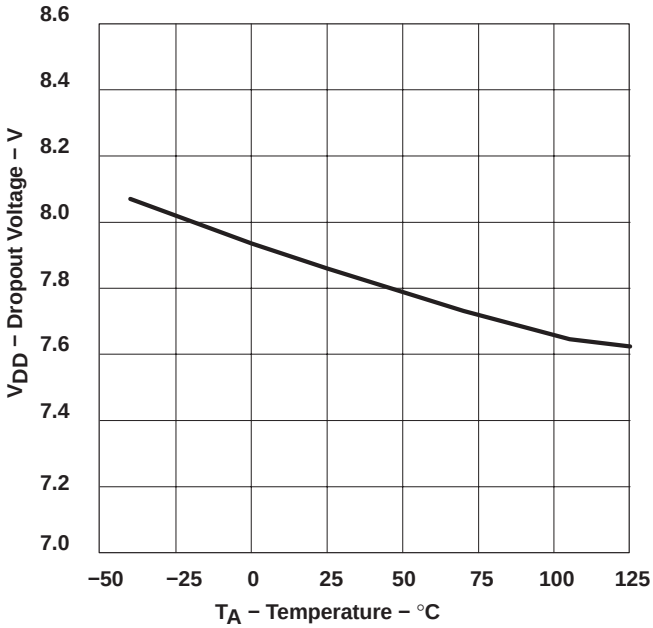


Figure 23

VLO SHORT CIRCUIT CURRENT
vs
TEMPERATURE

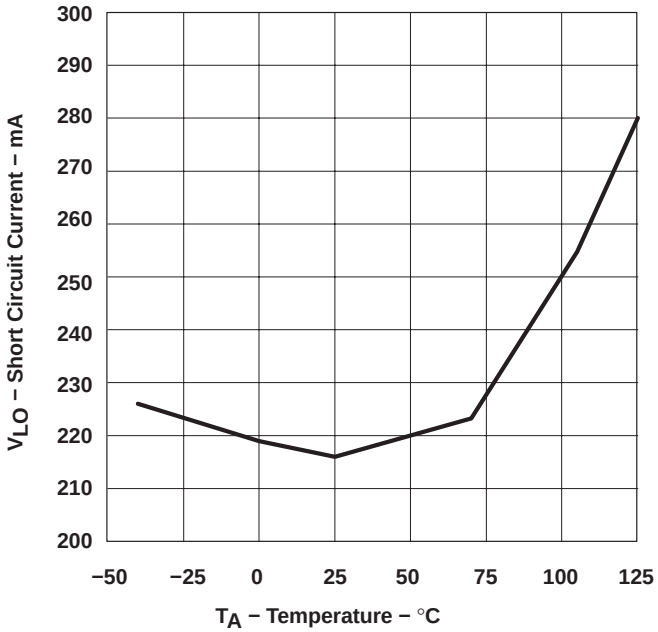


Figure 24

INPUT THRESHOLD
vs
TEMPERATURE (VDD = 10 V TO 20 V)

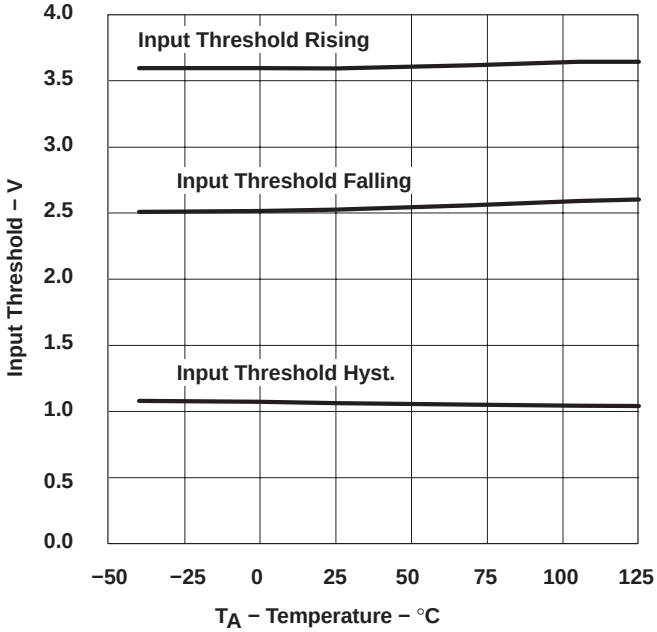


Figure 25

TYPICAL CHARACTERISTICS

PREDICTIVE DELAY BIT WEIGHT
vs
TEMPERATURE

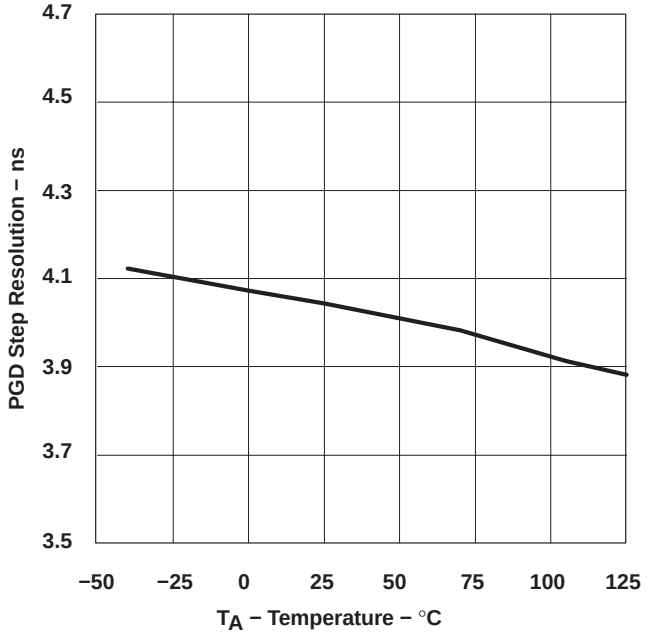


Figure 26

PROPAGATION DELAYS
vs
TEMPERATURE

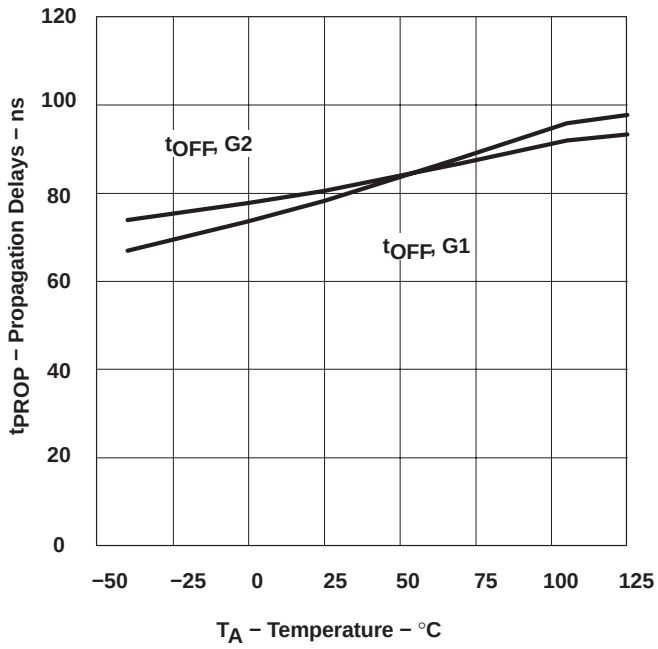


Figure 27

PREDICTIVE DELAY RANGE
vs
TEMPERATURE

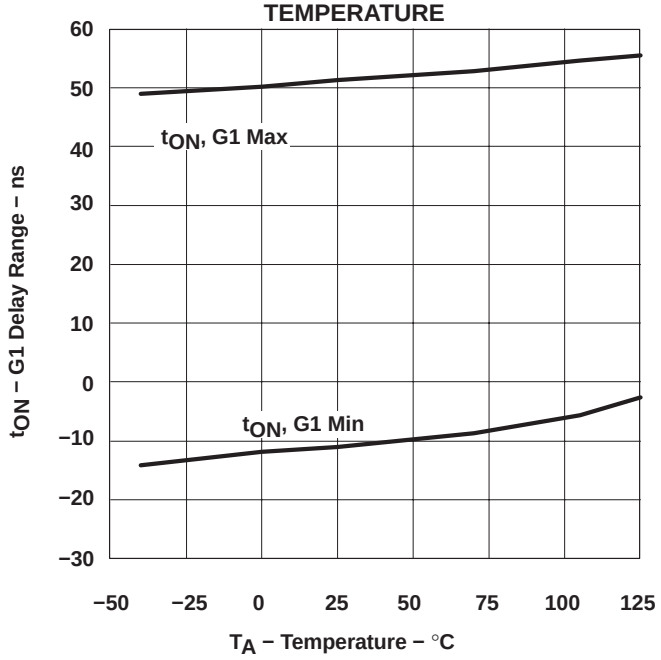


Figure 28

PREDICTIVE DELAY RANGE
vs
TEMPERATURE

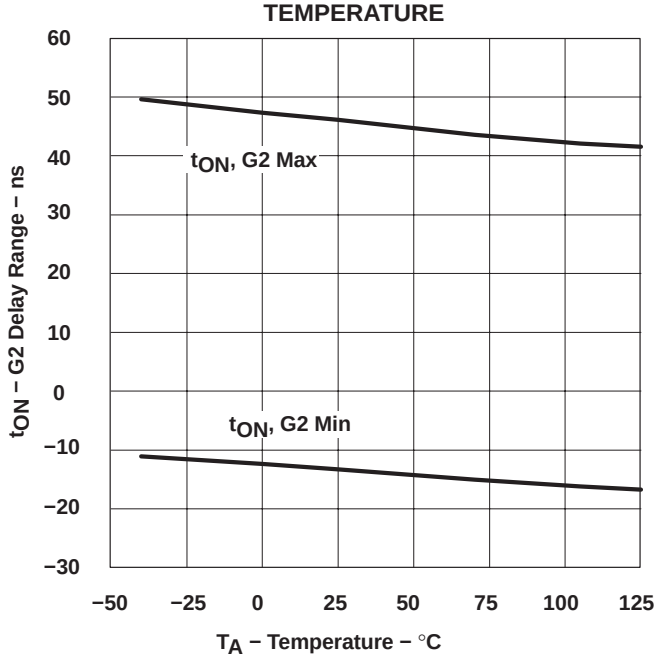


Figure 29

TYPICAL CHARACTERISTICS

G1 RISE AND FALL TIMES vs TEMPERATURE (2.2 nF)

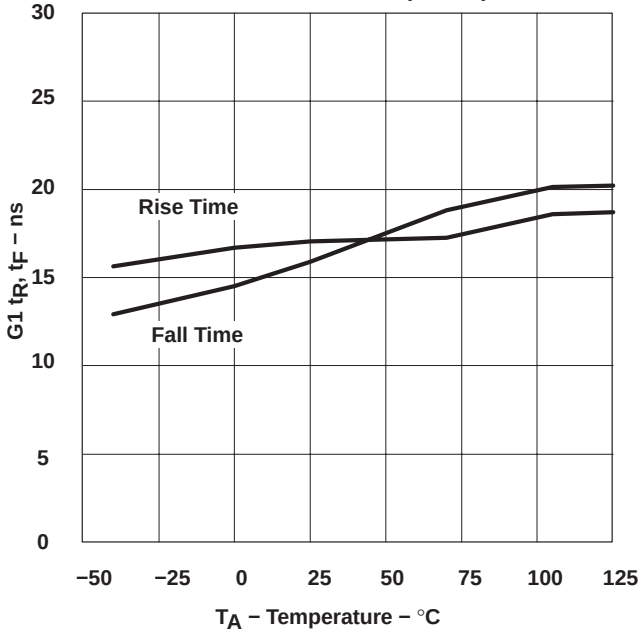


Figure 30

G2 RISE AND FALL TIMES vs TEMPERATURE (2.2 nF)

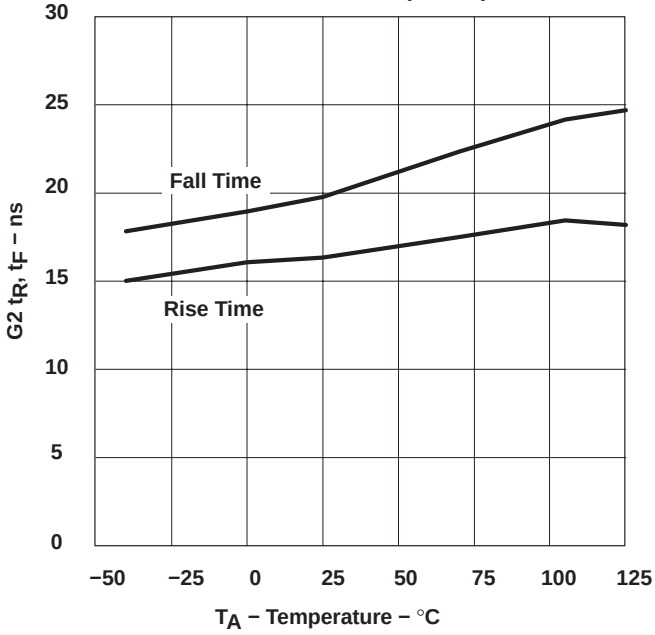


Figure 31

G1 SINK RESISTANCE vs TEMPERATURE ($R_{DS(on)}$)

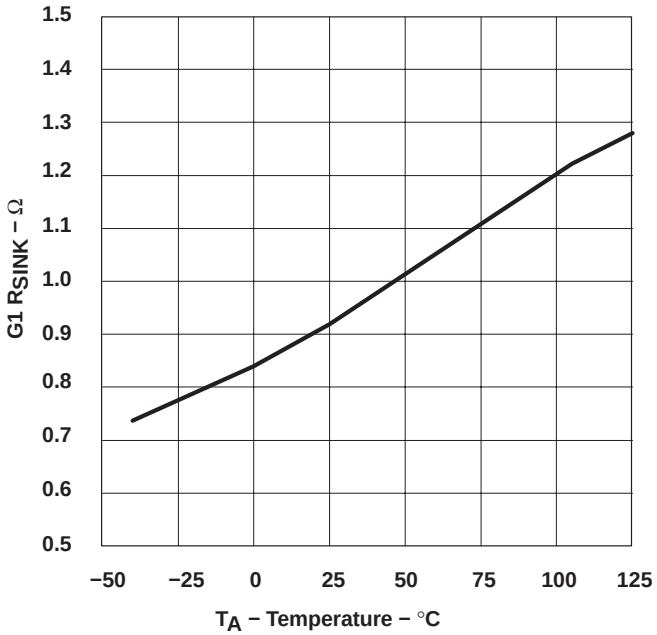


Figure 32

G1 SOURCE RESISTANCE vs TEMPERATURE

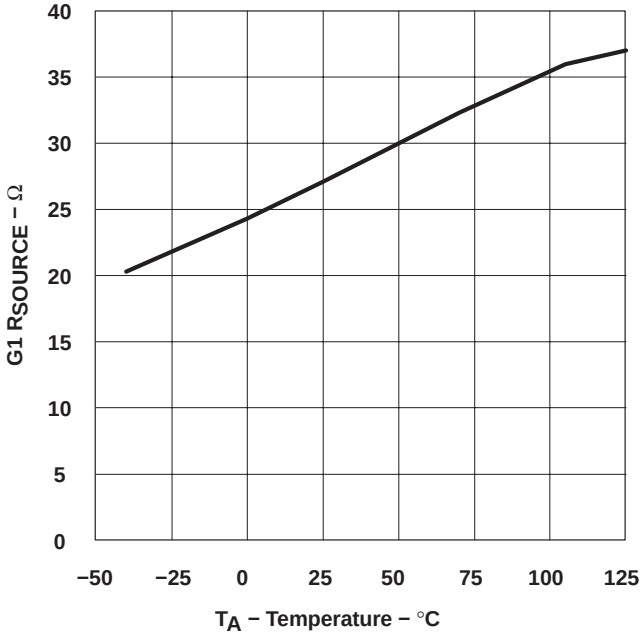


Figure 33

TYPICAL CHARACTERISTICS

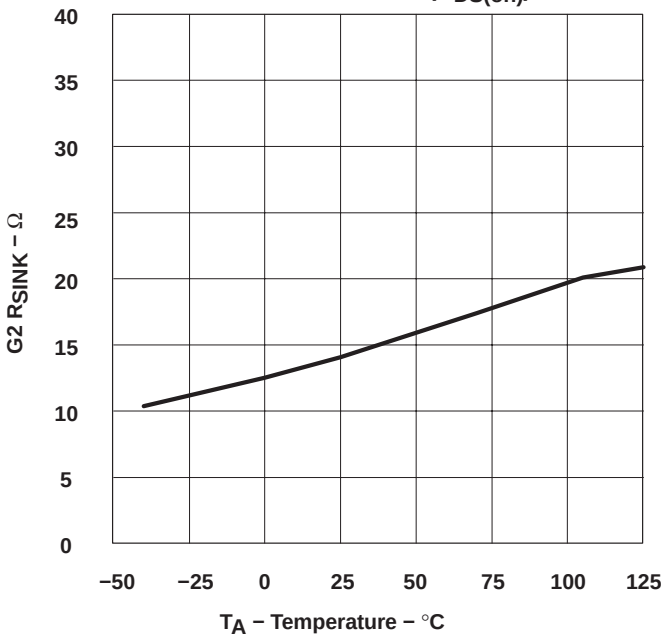


Figure 34

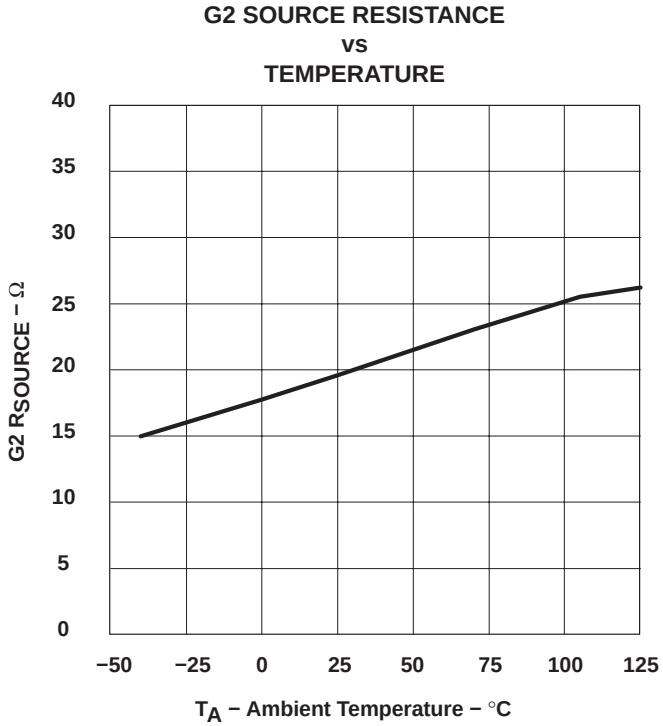


Figure 35

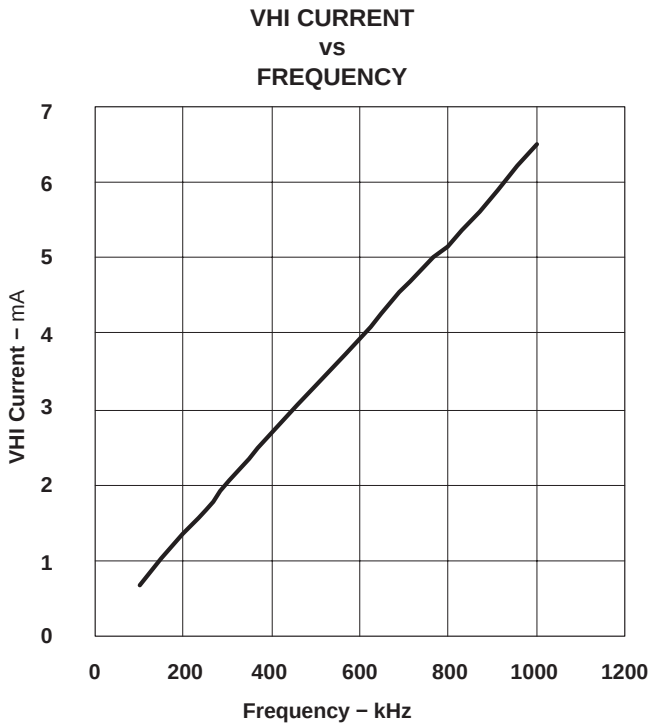


Figure 36

RELATED PRODUCTS

PART NUMBER	DESCRIPTION	GATE DRIVE	PACKAGE
TPS40090	High Frequency 2, 3, 4−Phase Multiphase Controller	−	TSSOP−24
UCC27221/2	High Efficiency Predictive Synchronous Buck	± 3.3 A	PowerPAD™ HTSSOP−14
TPS2830/1	Fast synchronous buck MOSFET drivers with dead-time control	± 2.4 A	PowerPAD™ HTSSOP−14, SOIC−14
TPS2832/3	Fast synchronous buck MOSFET drivers with dead-time control	± 2.4 A	SOIC−8
TPS2834/5	Synchronous buck MOSFET drivers with dead-time control	± 2.4 A	PowerPAD™ HTSSOP−14, SOIC−14
TPS2836/7	Synchronous buck MOSFET drivers with dead-time control	± 2.4 A	SOIC−8
TPS2838/9	Synchronous buck MOSFET drivers with drive regulator	± 4 A	PowerPAD™ HTSSOP−16
TPS2848/9	Synchronous buck MOSFET drivers with drive regulator	± 4 A	PowerPAD™ HTSSOP−14

REFERENCES

1. Power Supply Design Seminar SEM−1400 Topic 2: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature Number SLUP169.
2. User's Guide: *5 V to 0.9 V − 1.8 V (adjustable), 20-A High−Efficiency Synchronous Buck Converter using UCC27223 with Predictive Gate Drive™*, TI Literature Number SLUU181.
3. User's Guide: *12 V to 1.8 V, 20 A High-Efficiency Synchronous Buck Converter Using UCC27222 With Predictive Gate Drive™ Technology*, TI Literature Number SLUU140.
4. Application Note: *UCC27221/2 Predictive Gate Drive™ FAQ,* TI Literature Number SLUA280.
5. Application Note: *Predictive Gate Drive™ Boosts Converter Efficiency*, TI Literature Number SLUA281.
6. Application Note: *Increasing UCC27221/2 Gate Drive Voltage*, TI Literature Number SLUA292.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27223PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	27223	Samples
UCC27223PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	27223	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

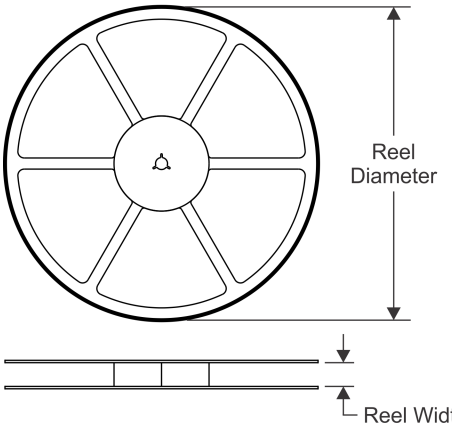
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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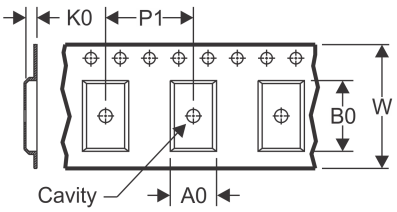
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

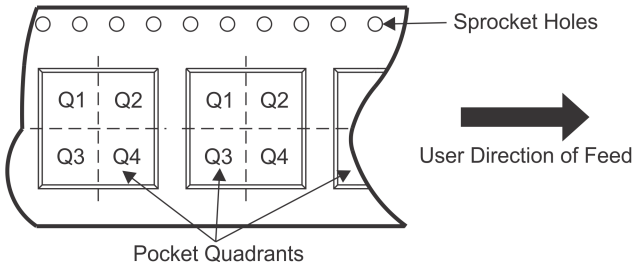


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

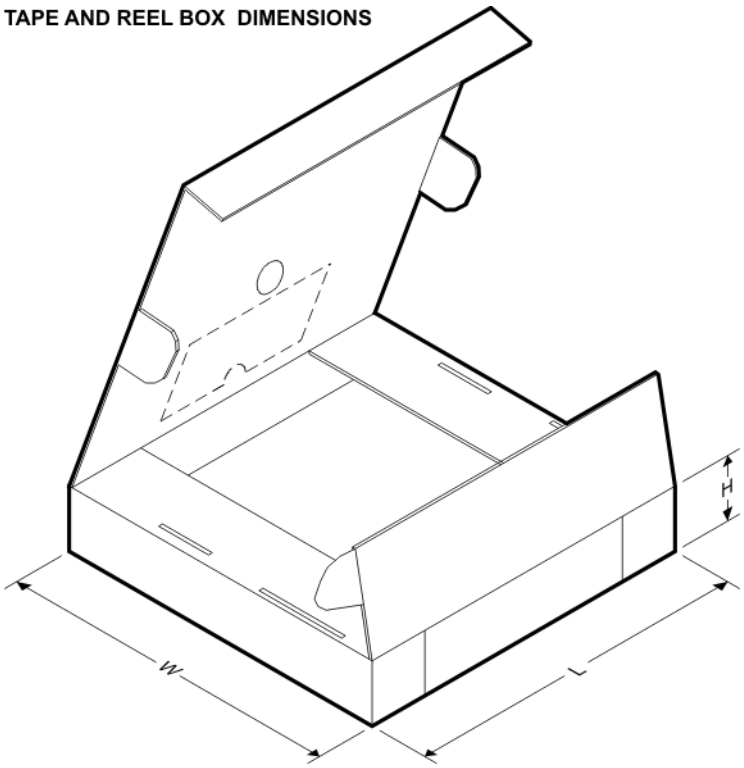
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27223PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

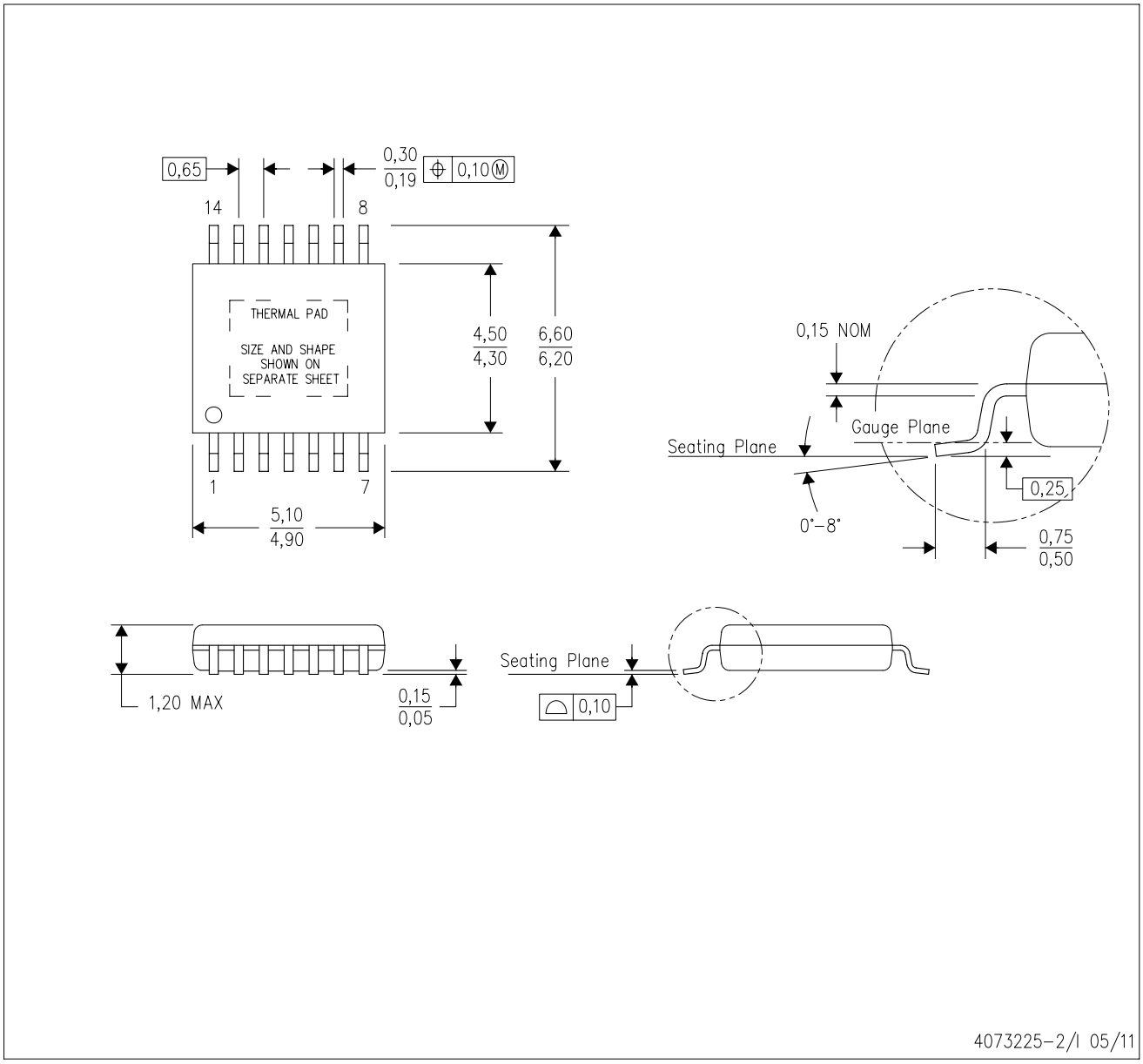
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27223PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

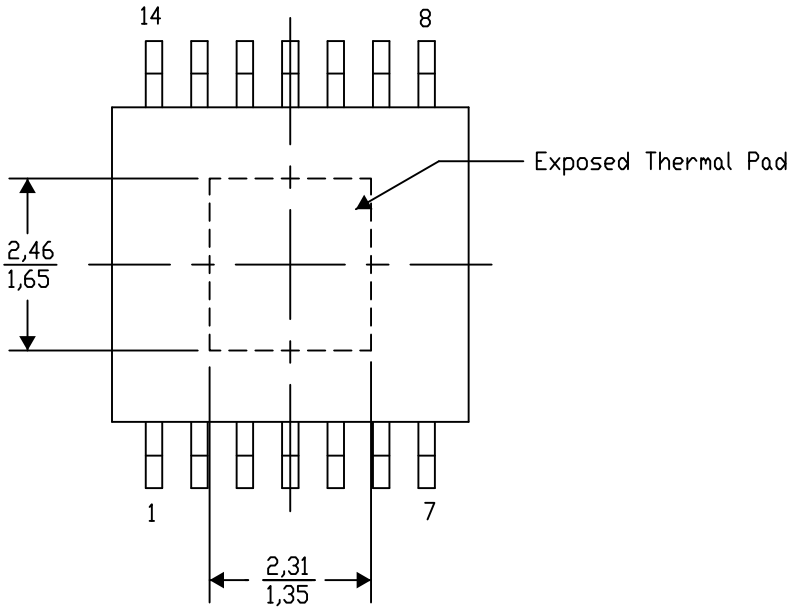
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

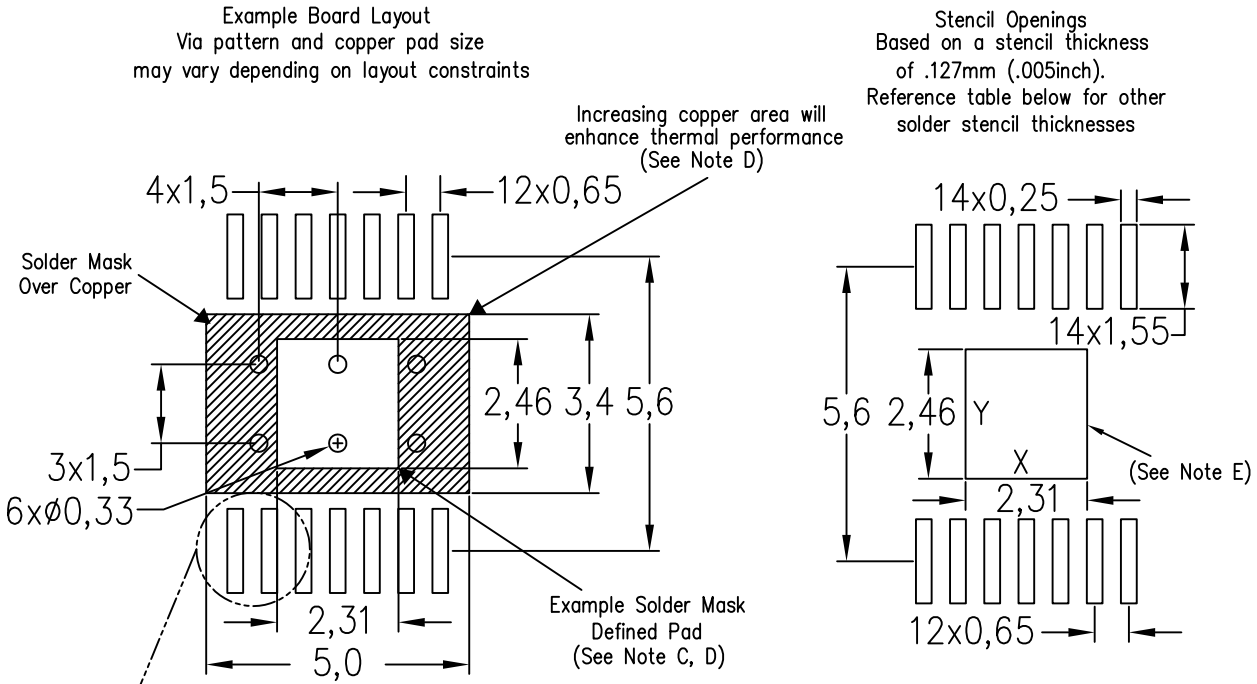
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

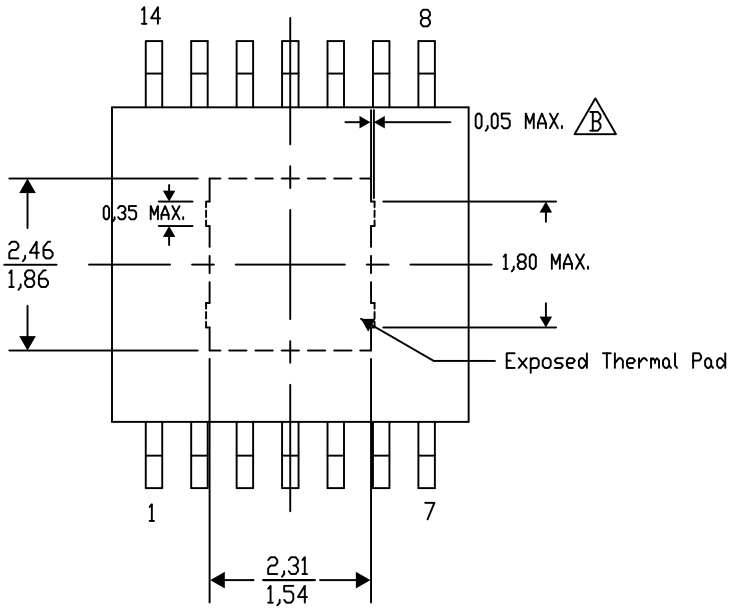
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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Top View

Exposed Thermal Pad Dimensions

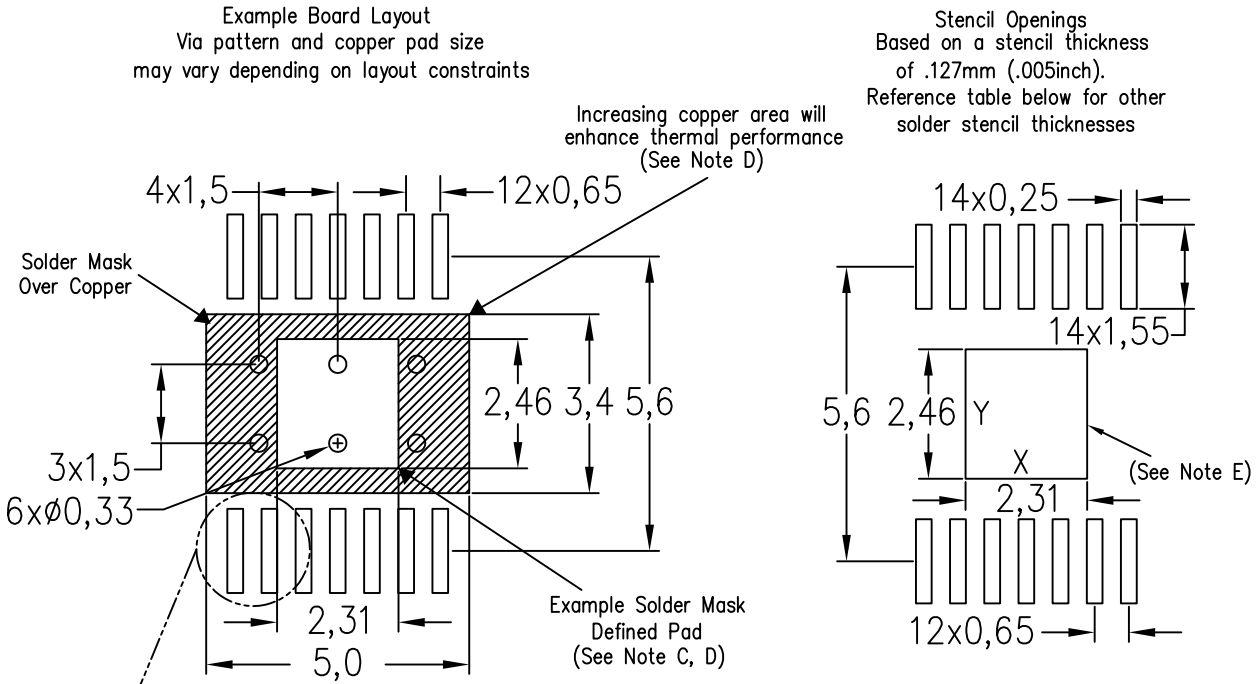
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
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F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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