UCC27212A-Q1 汽车120V 自举 4A 峰值电流高频高侧和低侧驱动器

1 特性

- 符合汽车应用 要求
- 具有符合 AECA-Q100 标准的下列特性：
  - 器件温度等级 –40°C 至 +140°C
  - 器件 HBM 分类等级 2
  - 器件 CDM 分类等级 C6
- 5V 关断欠压锁定 (UVLO)
- 通过独立输入驱动高侧和低侧配置中的两个 N 沟道 MOSFET
- 最大引导电压 120V 直流
- 4A 拉电流，4A灌电流能力
- 0.9Ω 上拉和下拉电阻
- 输入引脚能够耐受 –10V 至 +20V 的电压，并且与电源电压范围无关
- TTL 兼容输入
- 5V 至 17V VDD 工作范围，（最大绝对值 20V）
- 7.2ns 上升时间和 5.5ns 下降时间（采用 1000pF 负载）
- 快速传播延迟时间（典型值 20ns）
- 4ns 典型延迟匹配
- 采用 SOIC8(Powerpad) 封装

2 应用

- 汽车应用中的 电源
- 半桥和全桥转换器
- 高电压同步降压转换器
- 双开关正向转换器
- 推挽式和有源钳位正向转换器
- D 类音频放大器

3 说明

UCC27212A-Q1 驱动器是基于常用的 UCC27211 MOSFET 驱动器设计的。此外，UCC27212A-Q1 具有更宽的工作电压范围，可低至 5V，有助于降低功率损耗。

峰值输出上拉和下拉电流分别为 4A 拉电流和 4A 灌电流，而且上拉和下拉电阻均为 0.9Ω。这使得该器件能够驱动大功率 MOSFET，减少由于 MOSFET 的米勒平台导致的开关损耗。

输入结构可直接处理 -10V 电压，这提高了器件的鲁棒性，并且无需使用整流二极管即可实现与栅极驱动变压器直接连接。此外，输入还独立于电源电压，且具有 20V 的最大额定值。

UCC27212A-Q1 的开关节点（HS 引脚）最高可处理 -18V 电压，从而保护高侧通道不受寄生电感和杂散电容所固有的负电压影响。UCC27212A-Q1 具有更高的迟滞，因而支持连接至具有增强型抗噪性能的模拟或数字 PWM 控制器。

低侧和高侧栅极驱动器是独立控制的，且彼此的开通和关断时间均为 4ns。

由于使用了一个额定电压为 100V 的片上自举二极管，因此无需采用外部分立式二极管。高侧和低侧驱动器均配有欠压锁定功能，可提供对称的开通和关断行为，并且能够在驱动电压低于额定阈值时将输出强拉至低电平。

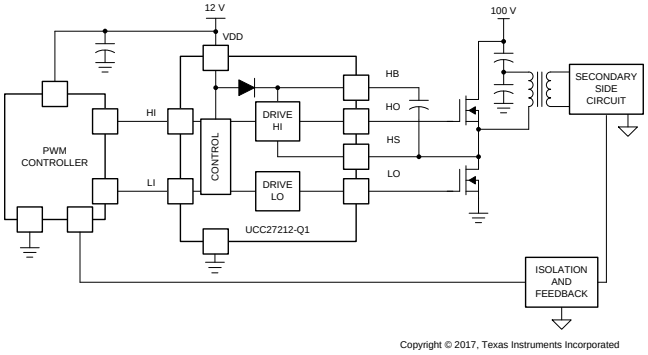
器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC27212A-Q1	SOIC8(Powerpad)	5.0mm x 6.0mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

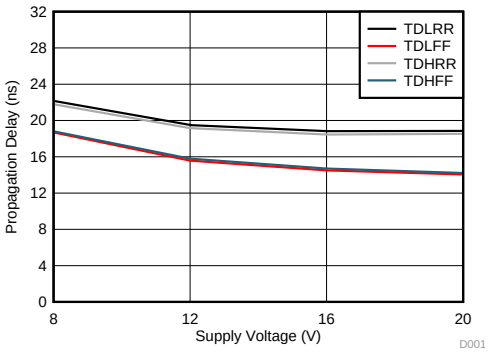
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典型应用图



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传播延迟与电源电压间的关系 **(T = 25°C)**



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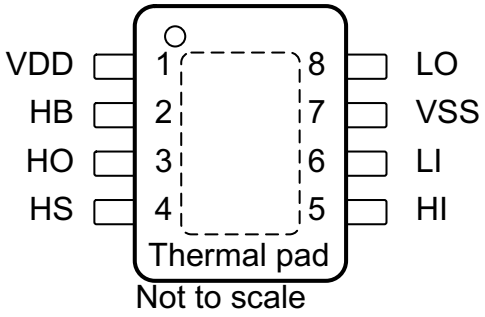
4 修订历史记录

日期	修订版本	说明
2017 年 7 月	*	初始发行版。

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5 Pin Configuration and Functions

DDA Package
8-Pin SO-PowerPAD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
2	HB	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF. The capacitor value is dependant on the gate charge of the high-side MOSFET and must also be selected based on speed and ripple criteria.
5	HI	I	High-side input.(1)
3	HO	O	High-side output. Connect to the gate of the high-side power MOSFET.
4	HS	P	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
6	LI	I	Low-side input.(1)
8	LO	O	Low-side output. Connect to the gate of the low-side power MOSFET.
1	VDD	P	Positive supply to the lower-gate driver. De-couple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 µF to 4.7 µF (See (2)).
7	VSS	—	Negative supply terminal for the device that is generally grounded.
Pad	Thermal pad(3)	—	Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100 Ω. If the source impedance is greater than 100 Ω, add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.
(2) For cold temperature applications TI recommends the upper capacitance range. Follow the for PCB layout.
(3) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}(2), $V_{HB} – V_{HS}$	Supply voltage range		–0.3	20	V
V_{LI}, V_{HI}	Input voltages on LI and HI		–10	20	V
V_{LO}	Output voltage on LO	DC	–0.3	VDD + 0.3	V
		Repetitive pulse < 100 ns(3)	–2	VDD + 0.3	V
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3	VHB + 0.3	V
		Repetitive pulse < 100 ns(3)	V_{HS} – 2	VHB + 0.3	V
V_{HS}	Voltage on HS	DC	–1	100	V
		Repetitive pulse < 100 ns(3)	–(24 V – VDD)	115	V
V_{HB}	Voltage on HB		–0.3	120	V
T_J	Operating virtual junction temperature range		–40	150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to VSS unless otherwise noted. Currents are positive into and negative out of the specified terminal.
(3) Verified at bench characterization. VDD is the value used in an application design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

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6.3 Recommended Operating Conditions

over operating free-air temperature range, all voltages are with respect to VSS; currents are positive into and negative out of the specified terminal. –40°C < T_J = T_A < 140°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range, V_{HB} – V_{HS}	7	12	17	V
V_{HS}	Voltage on HS	–1		100	V
V_{HS}	Voltage on HS (repetitive pulse < 100 ns)	–(20 V – VDD)		110	V
V_{HB}	Voltage on HB	V_{HS} + 8		115	V
	Voltage slew rate on HS			50	V/ns
	Operating junction temperature	–40		140	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC27212A-Q1 DDA (SOIC8 Powerpad) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{HS} = V_{SS} = 0 V, no load on LO or HO, T_A = T_J = –40°C to +140°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS, V_{DD} = V_{HB} = 12 V						
I_{DD}	V_{DD} quiescent current	$V_{(LI)}$ = $V_{(HI)}$ = 0 V	0.05	0.085	0.17	mA
I_{DDO}	V_{DD} operating current	f = 500 kHz, C_{LOAD} = 0	2.1	2.5	6.5	mA
I_{HB}	Boot voltage quiescent current	$V_{(LI)}$ = $V_{(HI)}$ = 0 V	0.015	0.065	0.1	mA
I_{HBO}	Boot voltage operating current	f = 500 kHz, C_{LOAD} = 0	1.5	2.5	5.1	mA
I_{HBS}	HB to V_{SS} quiescent current	$V_{(HS)}$ = $V_{(HB)}$ = 115 V		0.0005	1	µA
I_{HBSO}	HB to V_{SS} operating current	f = 500 kHz, C_{LOAD} = 0		0.07	1.2	mA
SUPPLY CURRENTS, V_{DD} = V_{HB} = 6.8 V						
I_{DD}	VDD quiescent current	$V_{(LI)}$ = $V_{(HI)}$ = 0 V	0.02	0.065	0.14	mA
I_{DDO}	VDD operating current	f = 500 kHz, C_{LOAD} = 0	0.7	1.4	6.5	mA
I_{HB}	Boot voltage quiescent current	$V_{(LI)}$ = $V_{(HI)}$ = 0 V	0.01	0.04	0.08	mA
I_{HBO}	Boot voltage operating current	f = 500 kHz, C_{LOAD} = 0	0.5	1.23	5.1	mA
I_{HBS}	HB to VSS quiescent current	$V_{(HS)}$ = $V_{(HB)}$ = 115 V		0.0005	1	µA
I_{HBSO}	HB to VSS operating current	f = 500 kHz, C_{LOAD} = 0		0.07	1.2	mA
INPUT, V_{DD} = V_{HB} = 12 V						
V_{HIT}	Input voltage threshold		1.7	2.3	2.55	V
V_{LIT}	Input voltage threshold		1.2	1.6	1.9	V
V_{IHYS}	Input voltage hysteresis			700		mV
R_{IN}	Input pulldown resistance			68		kΩ
INPUT, V_{DD} = V_{HB} = 6.8 V						
V_{HIT}	Input voltage threshold		1.6	2.0	2.6	V

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Electrical Characteristics (continued)

over operating free-air temperature range, V_{HS} = V_{SS} = 0 V, no load on LO or HO, T_A = T_J = –40°C to +140°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LIT}	Input voltage threshold		1.1	1.5	2.1	V
V_{IHYS}	Input voltage hysteresis			500		mV
R_{IN}	Input pulldown resistance			68		kΩ
UNDER-VOLTAGE LOCKOUT (UVLO), V_{DD} = V_{HB} = 12 V						
V_{DDR}	V_{DD} turnon threshold		4.9	5.7	6.4	V
V_{DDHYS}	Hysteresis			0.4		V
V_{HBR}	V_{HB} turnon threshold		4.35	5.3	6.3	V
V_{HBHYS}	Hysteresis			0.3		V
BOOTSTRAP DIODE, V_{DD} = V_{HB} = 12 V						
V_F	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.65	0.8	V
V_{FI}	High-current forward voltage	I_{VDD-HB} = 100 mA		0.85	0.95	V
R_D	Dynamic resistance, ΔVF/ΔI	I_{VDD-HB} = 100 mA and 80 mA	0.3	0.5	0.85	Ω
BOOTSTRAP DIODE, V_{DD} = V_{HB} = 6.8 V						
V_F	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.65	0.8	V
V_{FI}	High-current forward voltage	I_{VDD-HB} = 100 mA		0.85	0.95	V
R_D	Dynamic resistance, ΔVF/ΔI	I_{VDD-HB} = 100 mA and 80 mA	0.3	0.5	0.85	Ω
LO GATE DRIVER, V_{DD} = V_{HB} = 12 V						
V_{LOL}	Low-level output voltage		0.05	0.1	0.19	V
V_{LOH}	High level output voltage		0.1	0.16	0.29	V
	Peak pullup current(1)			3.7		A
	Peak pulldown current (1)			4.5		A
LO GATE DRIVER, V_{DD} = V_{HB} = 6.8 V						
V_{LOL}	Low-level output voltage	I_{LO} = 100 mA	0.04	0.13	0.35	V
V_{LOH}	High level output voltage	I_{LO} = –100 mA, V_{LOH} = V_{DD} – V_{LO}	0.12	0.23	0.42	V
	Peak pullup current	V_{LO} = 0 V		1.3		A
	Peak pulldown current	V_{LO} = 12 V for VDD = 6.8V		1.7		A
HO GATE DRIVER, V_{DD} = V_{HB} = 12 V						
V_{HOL}	Low-level output voltage		0.05	0.1	0.19	V
V_{HOH}	High-level output voltage		0.1	0.16	0.29	V
	Peak pullup current (1)			3.7		A
	Peak pulldown current (1)			4.5		A
HO GATE DRIVER, V_{DD} = V_{HB} = 6.8 V						
V_{LOL}	Low-level output voltage	I_{HO} = 100 mA	0.04	0.13	0.35	V
V_{LOH}	High level output voltage	I_{HO} = –100 mA, V_{HOH} = V_{HB} – V_{HO}	0.12	0.23	0.42	V
	Peak pullup current	V_{HO} = 0 V		1.3		A
	Peak pulldown current	V_{HO} = 12 V for VDD = 6.8V		1.7		A

(1) Ensured by design.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATION DELAYS, V_{DD} = V_{HB} = 12 V						
T_{DLFF}	V_{LI} falling to V_{LO} falling	C_{LOAD} = 0	10	16	30	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling	C_{LOAD} = 0	10	16	30	ns
T_{DLRR}	V_{LI} rising to V_{LO} rising	C_{LOAD} = 0	10	20	42	ns

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Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{DHRR}	V_{HI} rising to V_{HO} rising	C_{LOAD} = 0	10	20	42	ns
PROPAGATION DELAYS, V_{DD} = V_{HB} = 6.8 V						
T_{DLFF}	V_{LI} falling to V_{LO} falling	C_{LOAD} = 0	10	24	50	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling	C_{LOAD} = 0	10	24	50	ns
T_{DLRR}	V_{LI} rising to V_{LO} rising	C_{LOAD} = 0	13	28	57	ns
T_{DHRR}	V_{HI} rising to V_{HO} rising	C_{LOAD} = 0	13	28	57	ns
DELAY MATCHING, V_{DD} = V_{HB} = 12 V						
T_{MON}	From HO OFF to LO ON	T_J = 25°C		4	9.5	ns
		T_J = –40°C to +140°C		4	17	ns
T_{MOFF}	From LO OFF to HO ON	T_J = 25°C		4	9.5	ns
		T_J = –40°C to +140°C		4	17	ns
DELAY MATCHING, V_{DD} = V_{HB} = 6.8 V						
T_{MON}	From HO OFF to LO ON	T_J = 25°C		8		ns
		T_J = –40°C to +140°C		8	18	ns
T_{MOFF}	From LO OFF to HO ON	T_J = 25°C		6		ns
		T_J = –40°C to +140°C		6	18	ns
OUTPUT RISE AND FALL TIME, V_{DD} = V_{HB} = 12 V						
t_R	LO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		7.8		ns
t_R	HO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		7.8		ns
t_F	LO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		6.0		ns
t_F	HO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		6.0		ns
t_R	LO, HO	C_{LOAD} = 0.1 µF, (3 V to 9 V)		0.36	0.6	µs
t_F	LO, HO	C_{LOAD} = 0.1 µF, (9 V to 3 V)		0.20	0.4	µs
OUTPUT RISE AND FALL TIME, V_{DD} = V_{HB} = 6.8 V						
t_R	LO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		9.5		ns
t_R	HO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		13.0		ns
t_F	LO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		9.5		ns
t_F	HO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		13.0		ns
t_R	LO, HO	C_{LOAD} = 0.1 µF, (30% to 70%)		0.45	0.7	µs
t_F	LO, HO	C_{LOAD} = 0.1 µF, (70% to 30%)		0.2	0.5	µs
MISCELLANEOUS						
Minimum input pulse width that changes the output					100	ns
Bootstrap diode turnoff time (1)(2)		IF = 20 mA, I_{REV} = 0.5 A (3)		20		ns
Extended output pulse		when VDD = VHB = 6.8 V, VHS = 100 V, and input pulse width is 100 ns		250		ns

(1) Ensured by design.
(2) I_F: Forward current applied to bootstrap diode, IREV: Reverse current applied to bootstrap diode.
(3) Typical values for T_A = 25°C.

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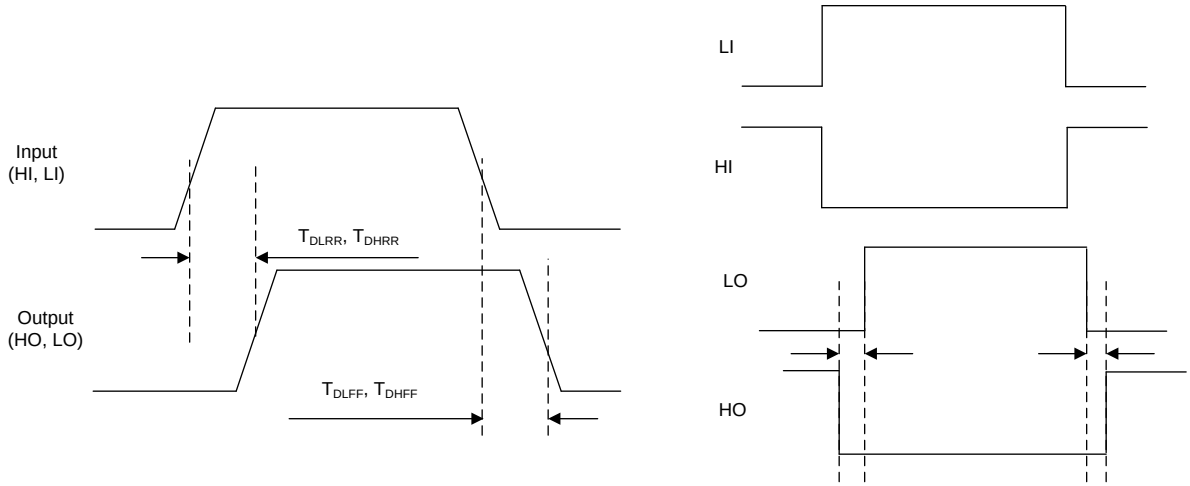


图 1. Timing Diagram

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6.7 Typical Characteristics

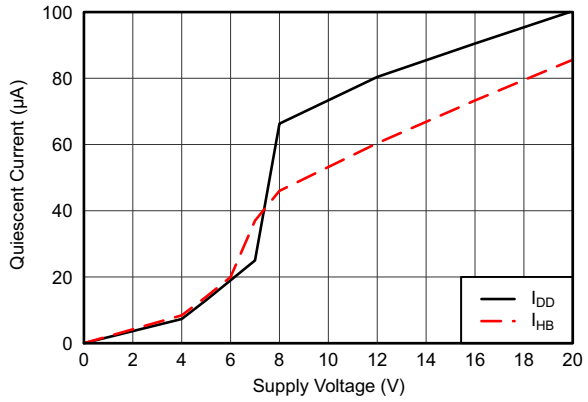


图 2. Quiescent Current vs Supply Voltage

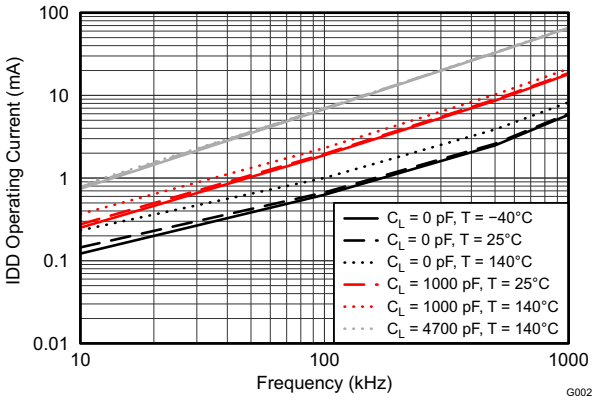


图 3. IDD Operating Current vs Frequency

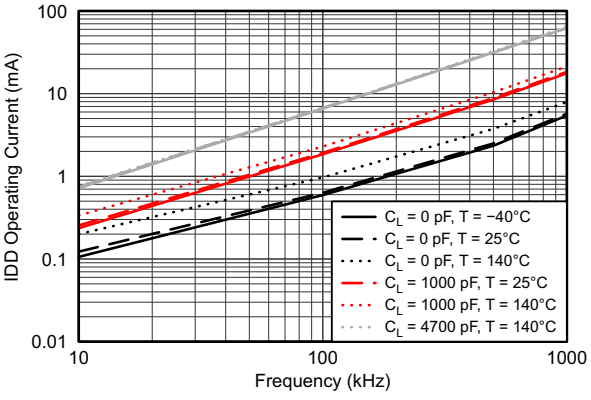


图 4. IDD Operating Current vs Frequency

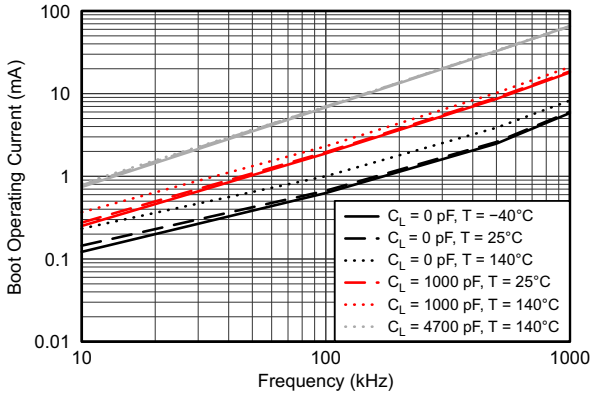


图 5. Boot Voltage Operating Current vs Frequency (HB To HS)

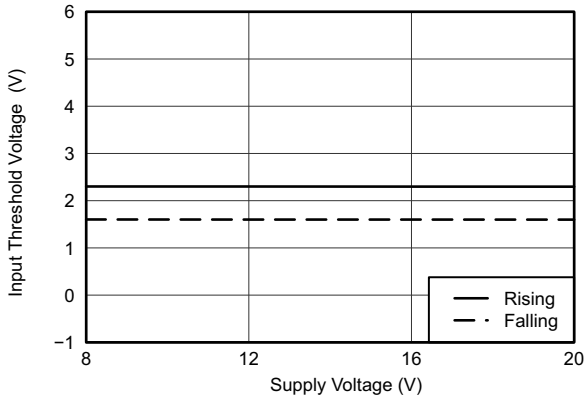


图 6. Input Threshold vs Supply Voltage

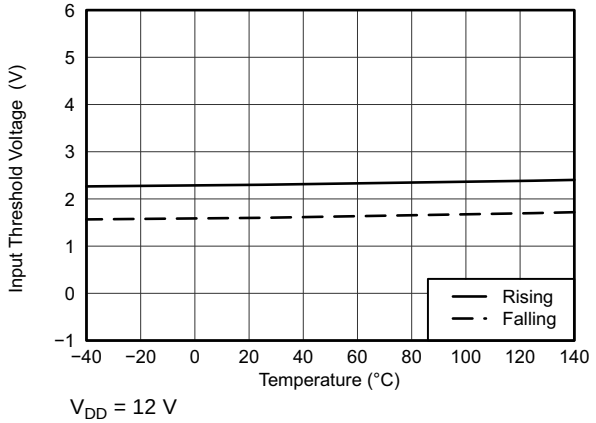
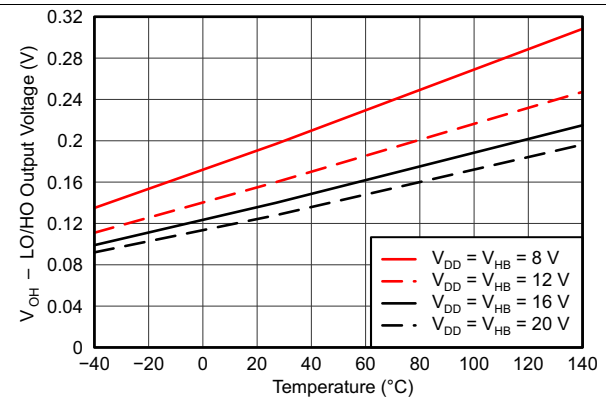


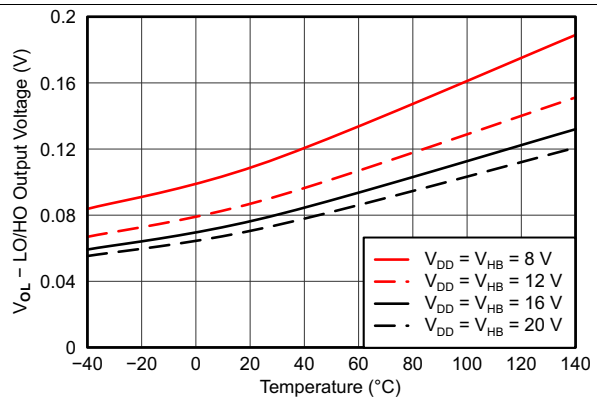
图 7. Input Thresholds vs Temperature

Typical Characteristics (接下页)



I_{HO} = I_{LO} = 100 mA

图 8. LO and HO High-Level Output Voltage vs Temperature



I_{HO} = I_{LO} = 100 mA

图 9. LO and HO Low-Level Output Voltage vs Temperature

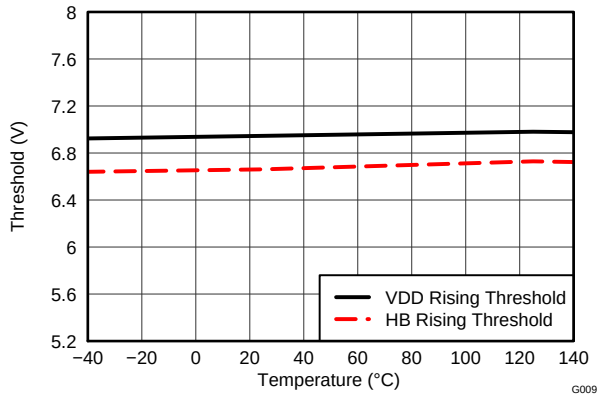


图 10. Undervoltage Lockout Threshold vs Temperature

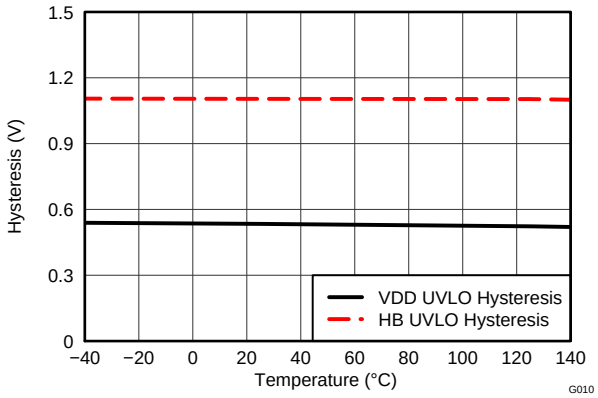
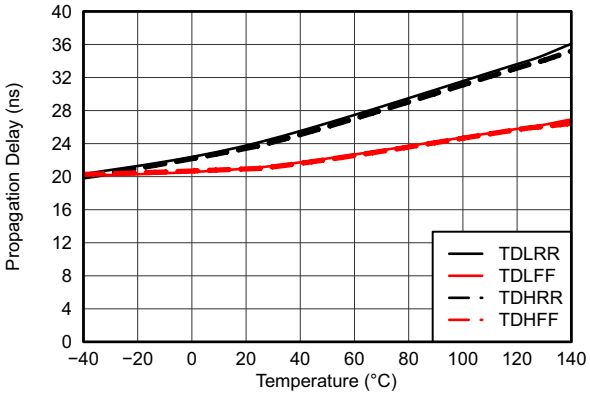
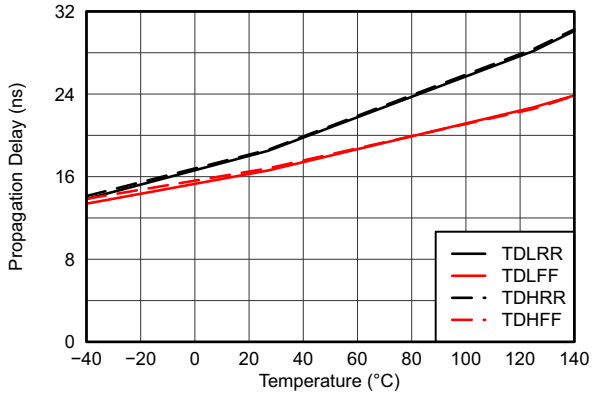


图 11. Undervoltage Lockout Threshold Hysteresis vs Temperature



V_{DD} = V_{HB} = 12 V

图 12. Propagation Delays vs Temperature



V_{DD} = V_{HB} = 12 V

图 13. Propagation Delays vs Temperature

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Typical Characteristics (接下页)

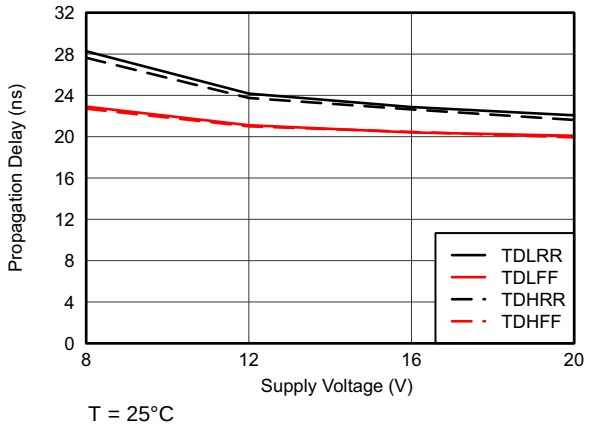


图 14. Propagation Delays vs Supply Voltage (V_{DD} = V_{HB})

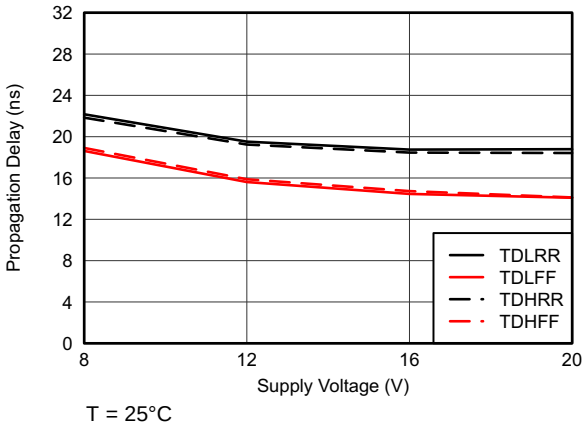


图 15. Propagation Delays vs Supply Voltage (V_{DD} = V_{HB})

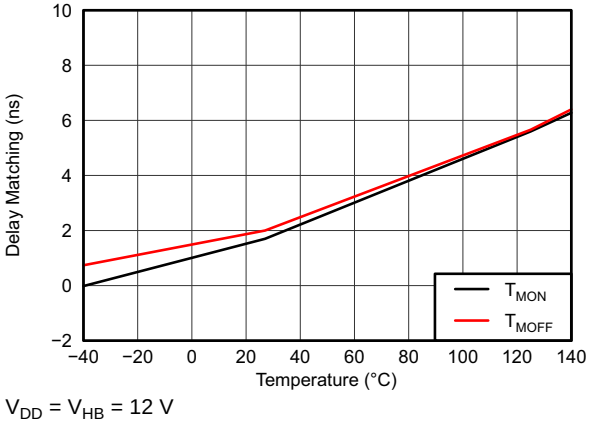


图 16. Delay Matching vs Temperature

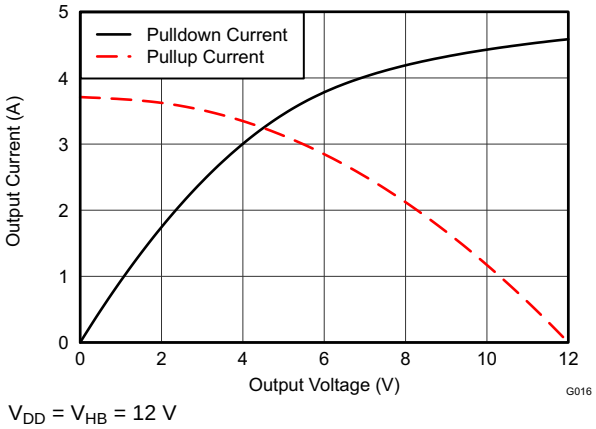


图 17. Output Current vs Output Voltage

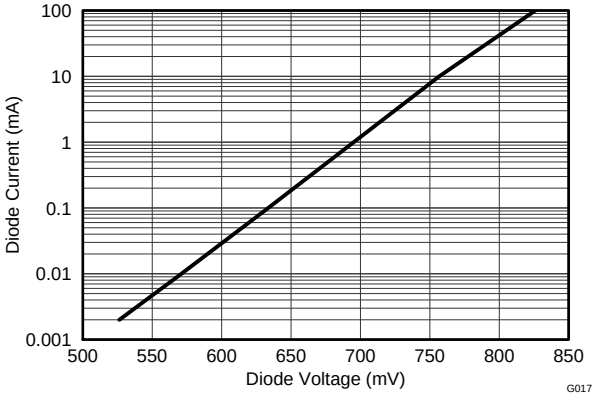


图 18. Diode Current vs Diode Voltage

7 Detailed Description

7.1 Overview

The UCC27212A-Q1 device represents Texas Instruments' latest generation of high-voltage gate drivers, which are designed to drive both the high-side and low-side of N-Channel MOSFETs in a half- and full-bridge or synchronous-buck configuration. The floating high-side driver can operate with supply voltages of up to 120 V, which allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two-switch forward, and active clamp forward converters.

The UCC27212A-Q1 device feature 4-A source and sink capability, industry best-in-class switching characteristics and a host of other features listed in 表 1. These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

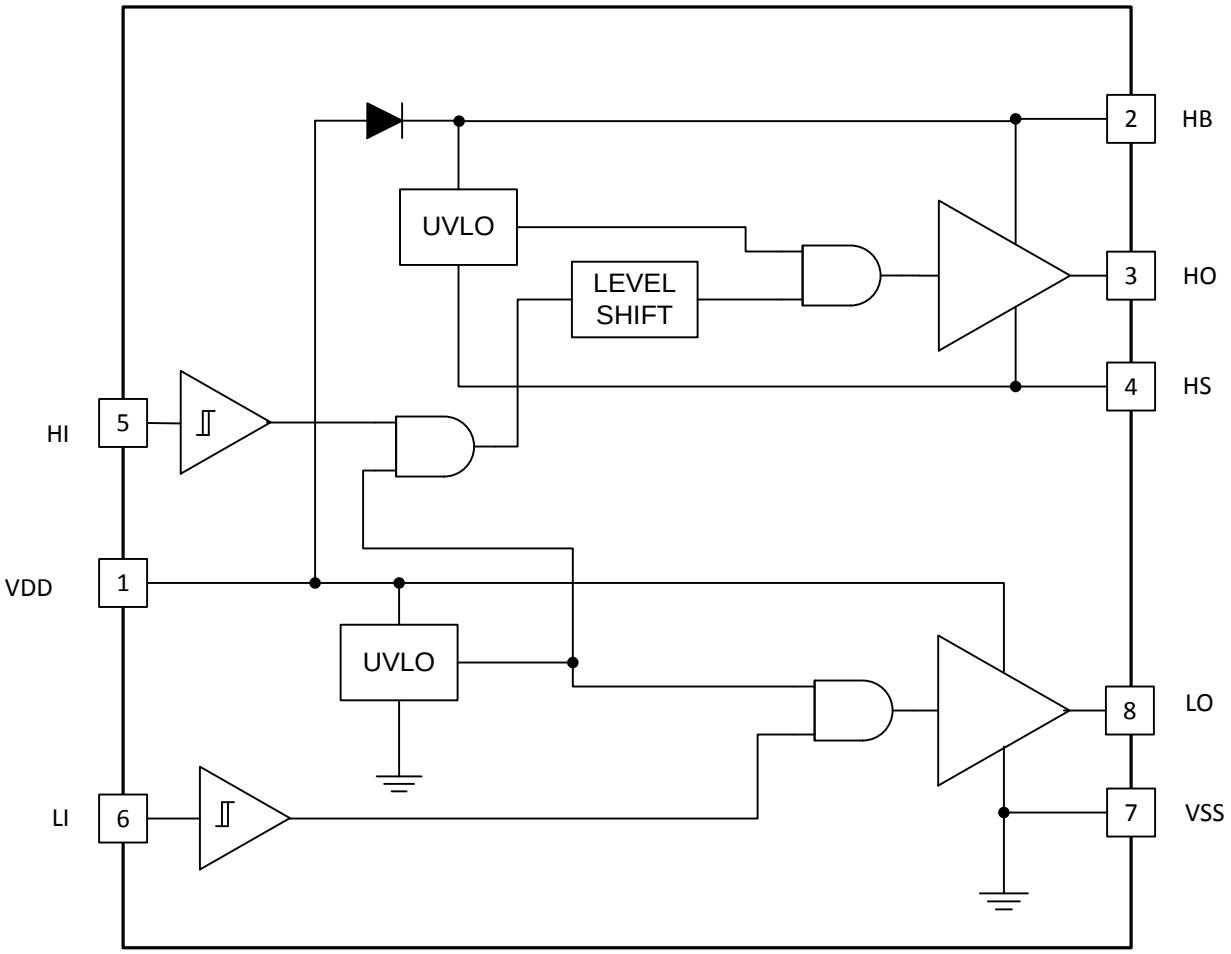
表 1. UCC27212A-Q1 Highlights

FEATURE	BENEFIT
4-A source and sink current with 0.9-Ω output resistance	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle –10 VDC up to 20 VDC	Increased robustness and ability to handle undershoot and overshoot can interface directly to gate-drive transformers without having to use rectification diodes.
120-V internal boot diode	Provides voltage margin to meet telecom 100-V surge requirements
Switch node (HS pin) able to handle –18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused by parasitic inductance and stray capacitance
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
18-ns propagation delay with 7.2-ns rise time and 5.5-ns fall time	Best-in-class switching characteristics and extremely low-pulse transmission distortion
2-ns (typical) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers; increased hysteresis offers added noise immunity

In the UCC27212A-Q1 device, the high side and low side each have independent inputs that allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27212A-Q1. The UCC27212A-Q1 is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS}, which is typically ground. The UCC27212A-Q1 functions are divided into the input stages, UVLO protection, level shift, boot diode, and output driver stages.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input stages of the UCC27212A-Q1 device have impedance of 70-kΩ nominal and input capacitance is approximately 2 pF. Pulldown resistance to V_{SS} (ground) is 70 kΩ. The logic level compatible input provides a rising threshold of 2.3 V and a falling threshold of 1.6 V. There is enough input hysteresis to avoid noise related jitter issues on the input.

7.3.2 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 5.7 V with 0.4-V hysteresis. The VHB UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 5.3 V with 0.4 V hysteresis.

Feature Description (接下页)

7.3.3 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27212A-Q1 family of drivers. The diode anode is connected to V_{DD} and cathode connected to V_{HB}. With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

7.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high side is referenced from V_{HB} to V_{HS}.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *Undervoltage Lockout (UVLO)* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the HI and LI pins. 表 2 lists the output states for different input pin combinations.

表 2. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.
(2) LO is measured with respect to VSS.

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8 Application and Implementation

注

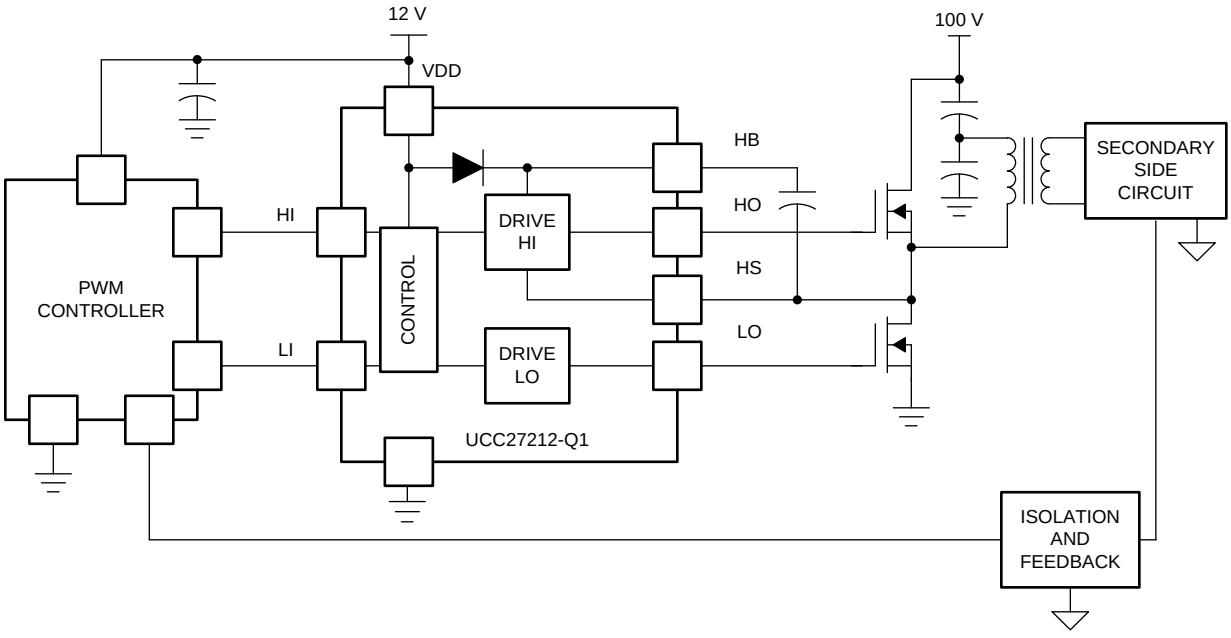
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. Gate-driver devices are extremely important components in switching power, and they combine the benefits of high-performance, low-cost component count and board-space reduction as well as simplified system design.

8.2 Typical Application



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图 19. UCC27212A-Q1 Typical Application

Typical Application (接下页)

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 3.

表 3. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output current rating, IO	–4 A to 4 A
Operating frequency	500 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 公式 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use 公式 2 to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD}$$

where

- I_Q is the quiescent current for the driver. (2)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27212A-Q1 features very low quiescent currents (less than 0.17 mA, refer to the table and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage VDD)
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by 公式 3.

$$EG = ½C_{LOAD} \times V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (3)

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by 公式 4.

$$PG = C_{LOAD} \times V_{DD}^2 \times f_{SW}$$

where

- f_{SW} is the switching frequency (4)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide 公式 5 for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

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8.2.3 Application Curves

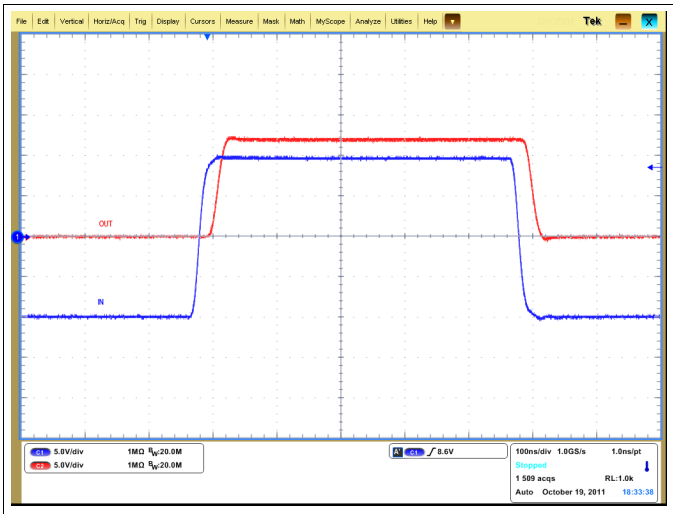


图 20. Negative 10-V Input

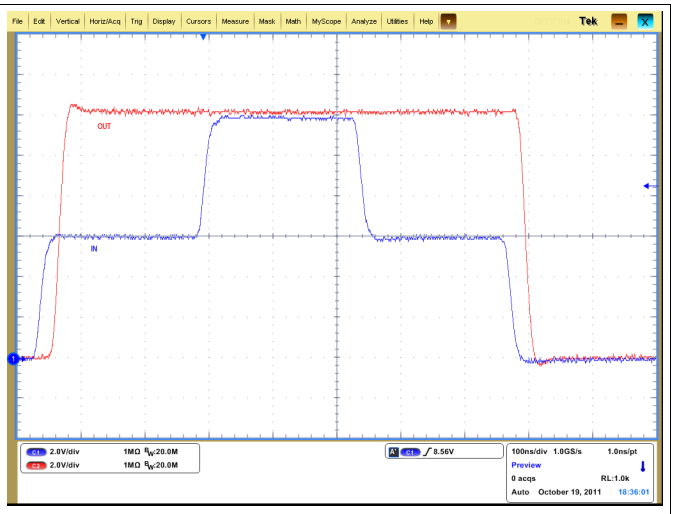


图 21. Step Input

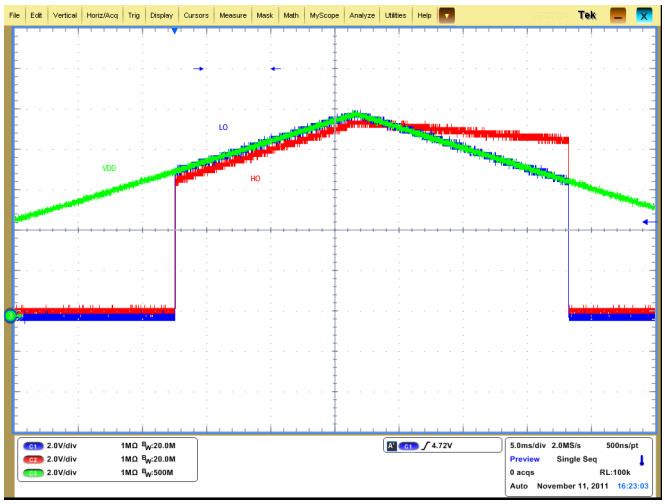


图 22. Symmetrical UVLO

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9 Power Supply Recommendations

The bias supply voltage range for which the UCC27212A-Q1 device is recommended to operate is from 7 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 17 V. The UVLO protection feature also involves a hysteresis function, which means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 7 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the V_{DD} pin voltage has exceeded the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the HO pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the HO pin, a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus, ensure that a local bypass capacitor is provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range 0.22 µF to 4.7 µF between V_{DD} and GND. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore a 0.022-µF to 0.1-µF local decoupling capacitor is recommended between the HB and HS pins.

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10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} – V_{SS} and V_{HB}-V_{HS} (bootstrap) capacitors as close as possible to the device (see).
- Pay close attention to the GND trace. Use the thermal pad of the package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high current path of the MOSFET drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple UCC27212A-Q1 devices, TI recommends that dedicated decoupling capacitors be located at V_{DD}–V_{SS} for each device.
- Care must be taken to avoid placing VDD traces close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. A width of 60 to 100 mils is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

A poor layout can cause a significant drop in efficiency or system malfunction, and it can even lead to decreased reliability of the whole system.

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10.2 Layout Example

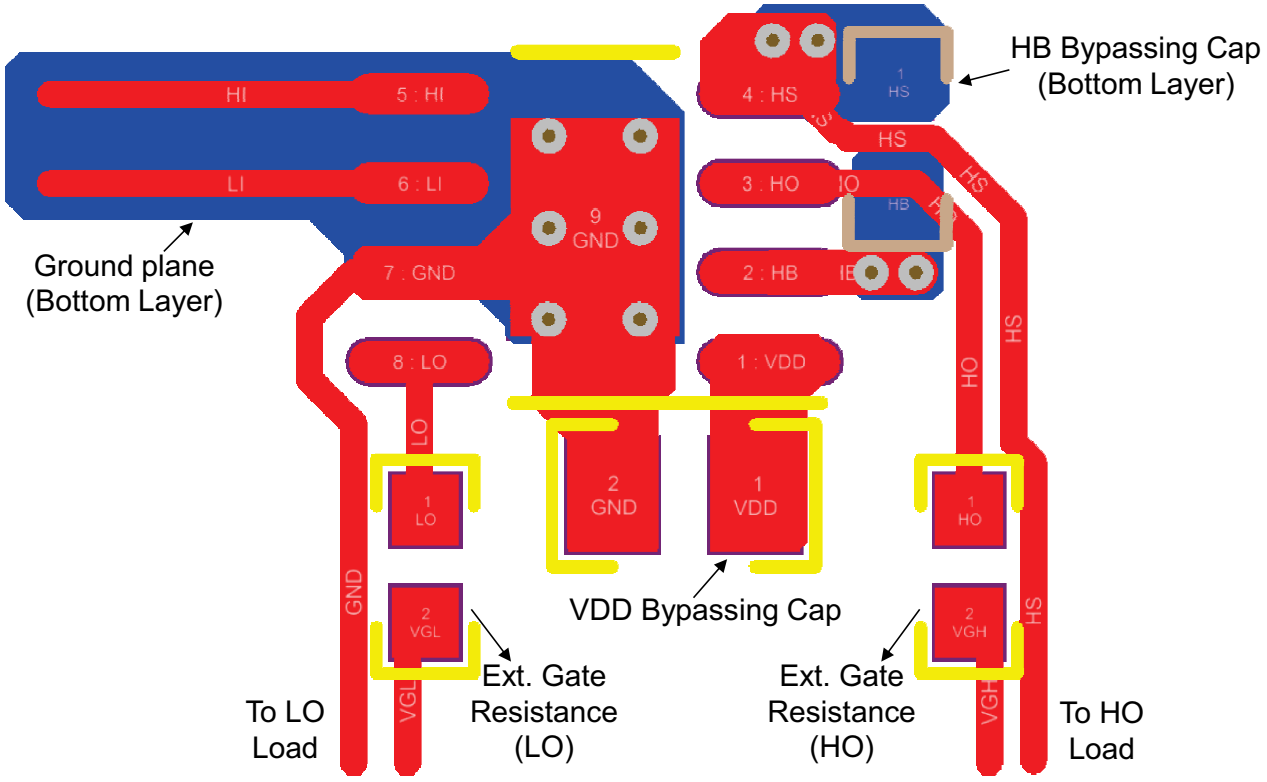


图 23. UCC27212A-Q1 Layout Example

10.2.1 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range, the package must allow for efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are listed in . For detailed information regarding the table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953). The UCC27212A-Q1 device is offered in SOIC (8) and VSON (8). The section lists the thermal performance metrics related to the SOT-23 package.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 《PowerPAD™ 散热增强型封装》，应用报告
- 《PowerPAD™ 速成》，应用报告

11.2 接收文档更新通知

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27212AQDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 140	27212Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

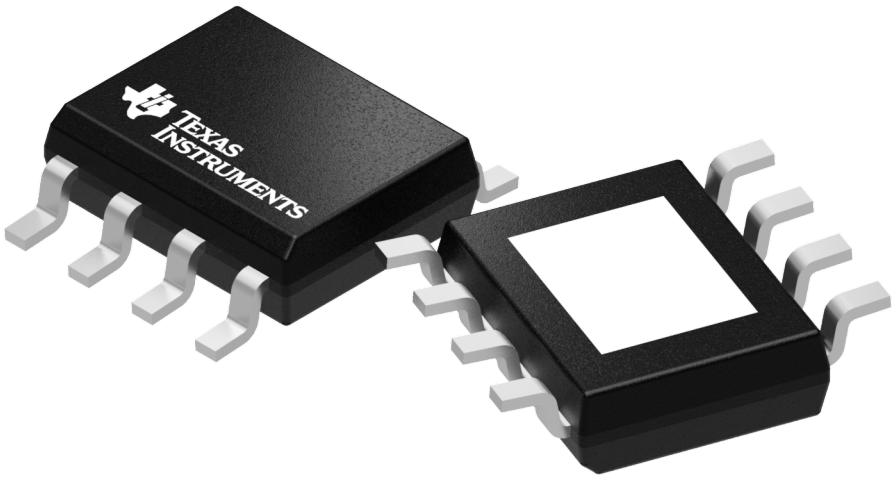
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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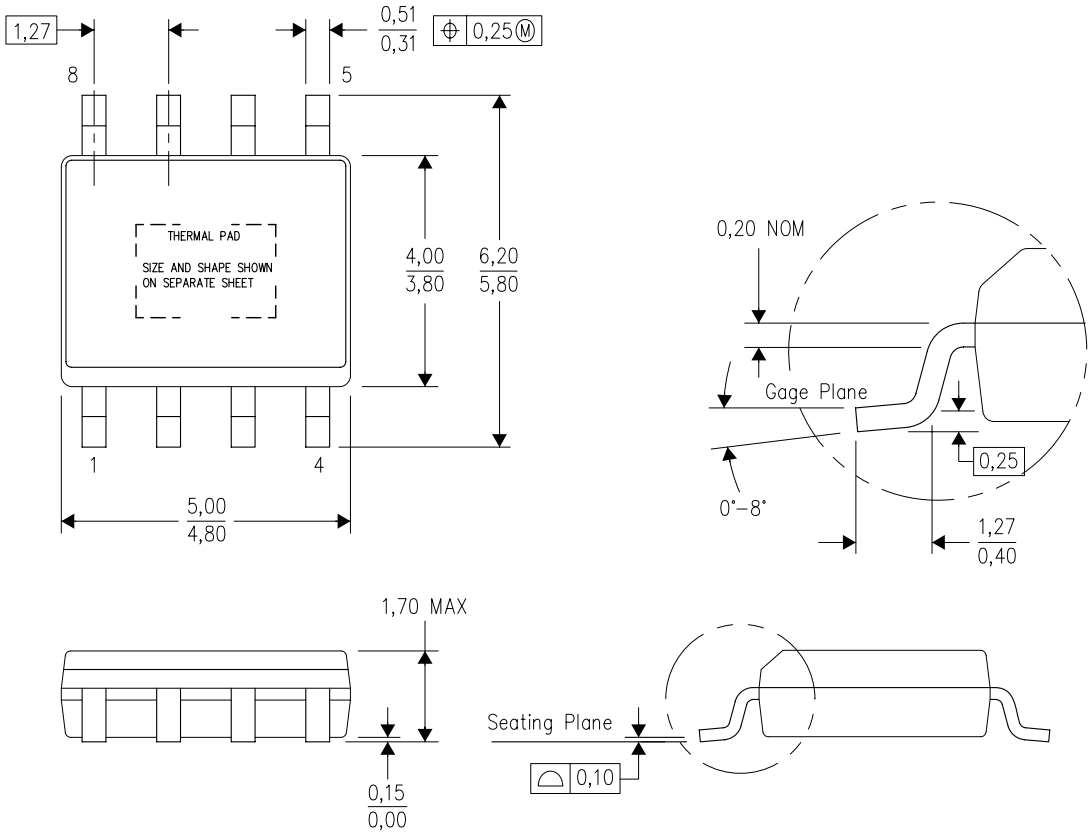
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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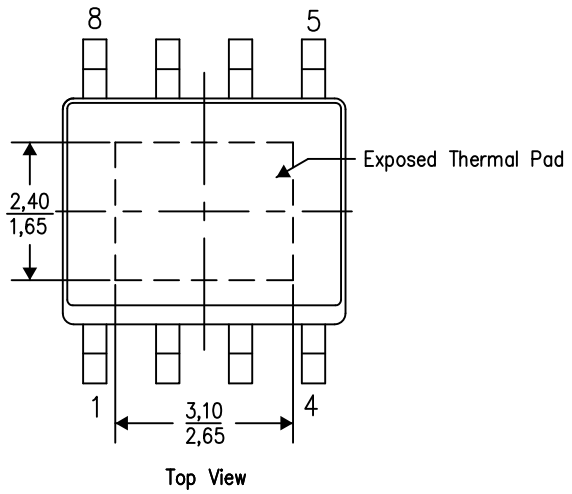
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



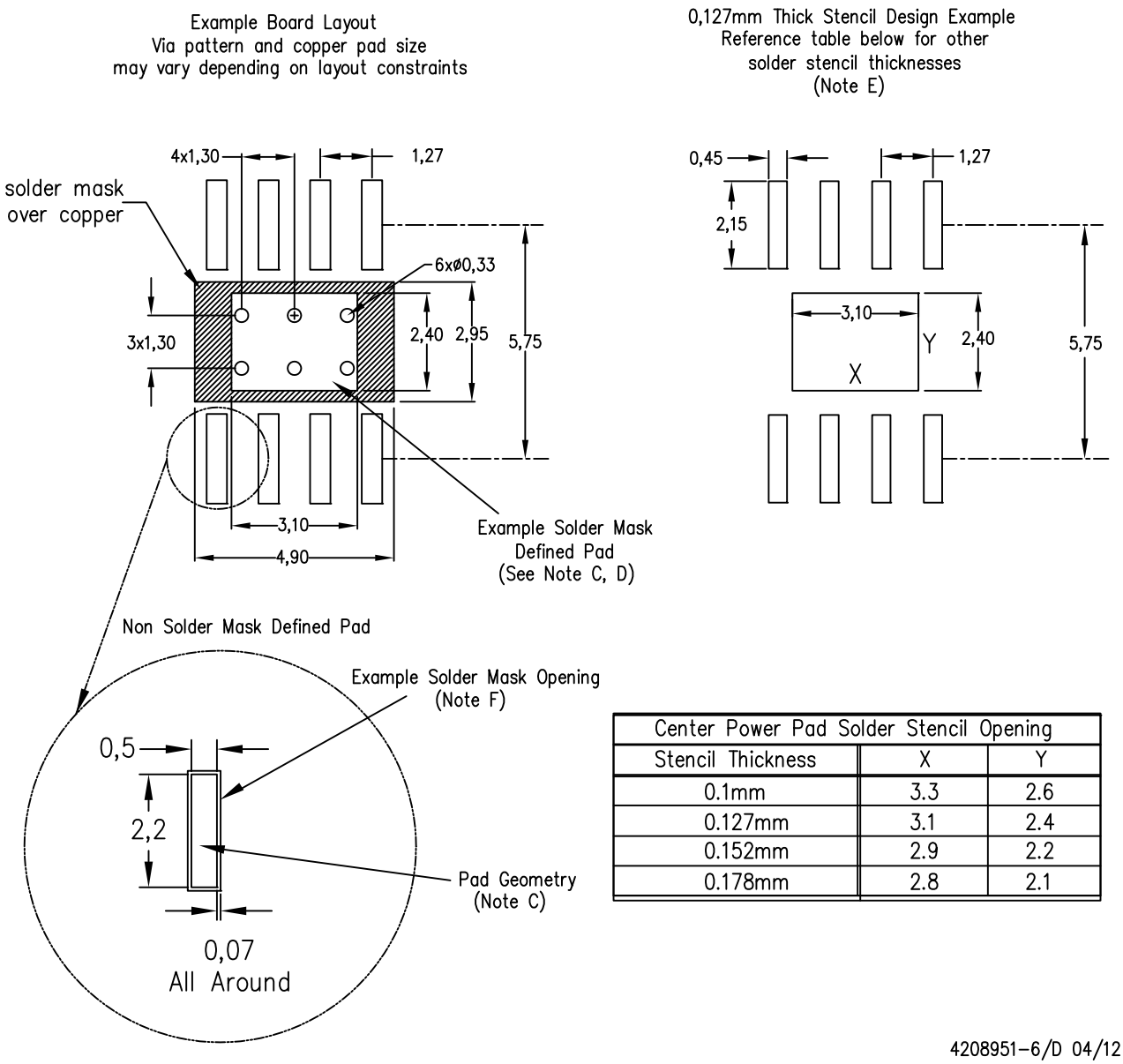
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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