

# ADS4245-EP 双通道, 14 位, 125MSPS 超低功率模数转换器 (ADC)

## 1 特性

- 超低功耗, 采用 1.8V 单电源供电:  
CMOS 输出:
  - 125MSPS 时总体功耗 277mW
- 高动态性能:
  - 170MHz 时无杂散动态范围 (SFDR) 为 88dBc
  - 170MHz 时信噪比 (SNR) 为 71.4dBFS
- 串扰: 185MHz 时大于 90dB
- 高达 6dB 的可编程增益以支持 SNR/SFDR 平衡
- 直流偏移校正
- 输出接口选项:
  - 1.8V 并行 CMOS 接口
  - 支持可编程摆幅的双倍数据速率 (DDR) 低压差分信令 (LVDS):
    - 标准摆幅: 350mV
    - 低摆幅: 200mV
- 支持低输入时钟振幅  
低至 200mV<sub>pp</sub>
- 支持国防、航天和医疗 应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 支持军用 (-55°C 至 125°C) 温度范围
  - 延长的产品生命周期
  - 延长的产品变更通知
  - 产品可追溯性

## 2 应用

- 无线通信基础设施
- 由软件定义的无线电
- 功率放大器线性化

## 3 说明

ADS4245 是 ADS42xx 双通, 14 位模数转换器 (ADC) 超低功耗系列产品的低速变体。采用创新设计技术实现高动态性能, 同时在由 1.8V 电源供电时功耗极低。该拓扑使 ADS4245 非常适合多载波、高带宽通信应用。

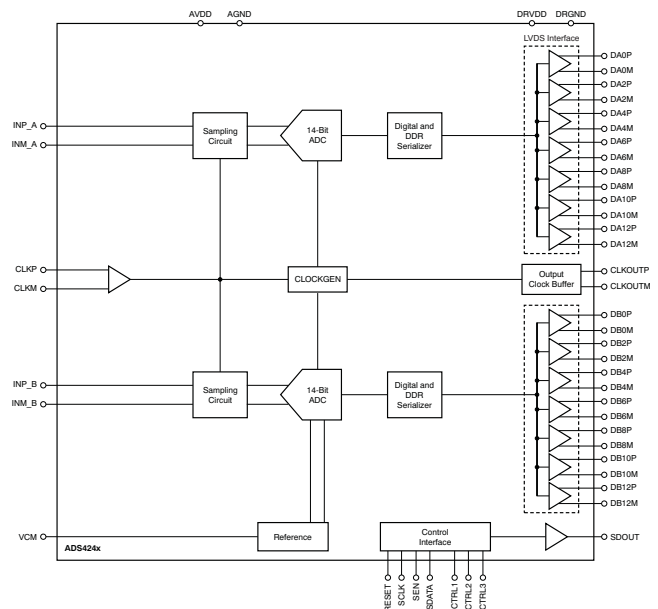
ADS4245 具有可被用于在较低满量程输入范围内改进 SFDR 性能的增益选项。这个器件还包括一个直流偏移校正环路, 此环路可被用于消除 ADC 偏移。DDR (双数据速率) LVDS 与并行 CMOS 数字输出接口都采用紧凑型超薄四方扁平无引线 (VQFN)-64 PowerPAD™ 封装。

此器件包含内部基准, 而删除了传统基准引脚和相关的去耦合电容器。ADS4245 可在军用温度范围 (-55°C 至 125°C) 内额定运行。

### 器件信息

订货编号	封装	封装尺寸
ADS4245MRGC25EP	VQFN (64)	9mm x 9mm

### 方框图



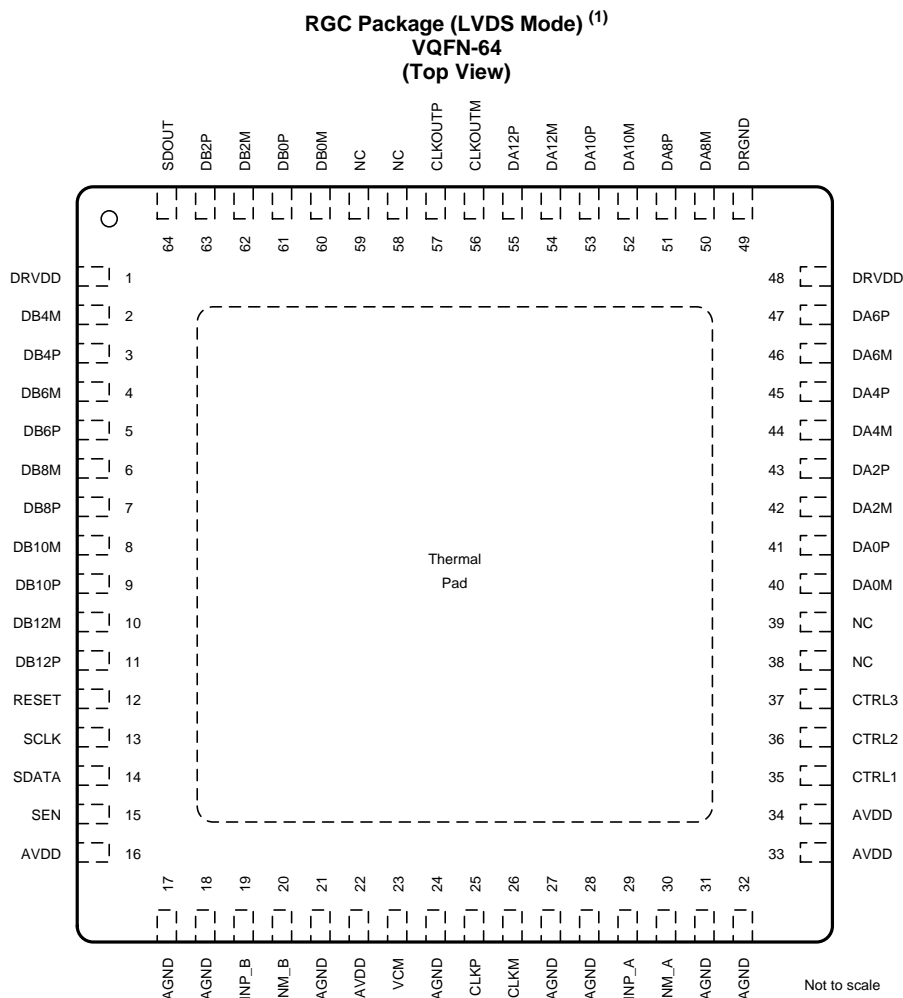
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## 4 修订历史记录

Changes from Original (April 2014) to Revision A	Page
• Changed <i>Handling Rating To: ESD Ratings</i> .....	7
• Moved Storage temperature, $T_{stg}$ From the <i>ESD Ratings</i> table to the <i>Absolute Maximum Ratings</i> table .....	7
• Added a MIN value of 1 MSPS to Low-speed mode enabled in the <i>Recommended Operating Conditions</i> .....	8
• Added NOTE to the <i>Application and Implementation</i> .....	46

## 5 Pin Configuration and Functions



(1) The PowerPAD™ is connected to DRGND.

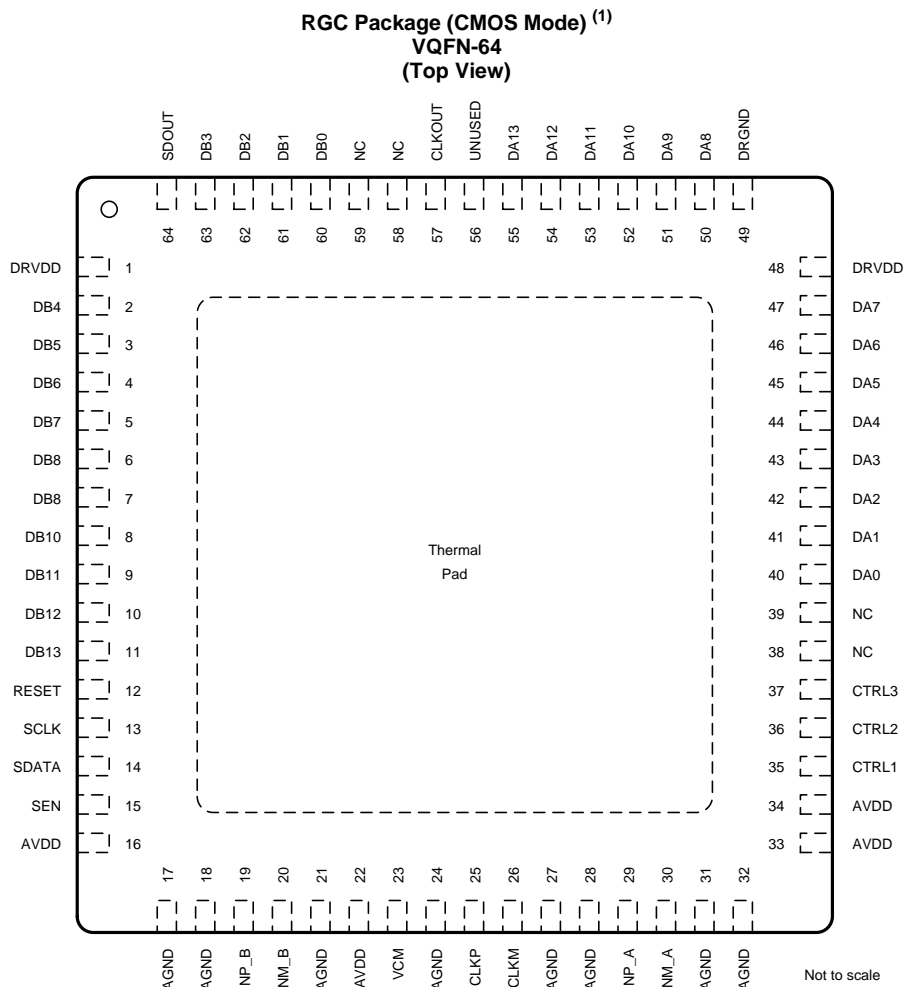
NOTE: NC = do not connect; must float.

### Pin Functions: LVDS Mode

NO.	NAME	# OF PINS	FUNCTION	DESCRIPTION
1, 48	DRVDD	2	Input	Output buffer supply
12	RESET	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this terminal or by using the software reset option; refer to the <a href="#">Serial Interface Configuration</a> section. In parallel interface mode, the RESET terminal must be permanently tied high. SCLK and SEN are used as parallel control terminals in this mode. This terminal has an internal 150kΩ pull-down resistor.
13	SCLK	1	Input	This terminal functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see <a href="#">表 9</a> for detailed information. This terminal has an internal 150kΩ pull-down resistor.
14	SDATA	1	Input	Serial interface data input; this terminal has an internal 150kΩ pull-down resistor.
15	SEN	1	Input	This terminal functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see <a href="#">表 10</a> for detailed information. This terminal has an internal 150kΩ pull-up resistor to AVDD.
16, 22, 33, 34	AVDD	4	Input	Analog power supply
17, 18, 21, 24, 27, 28, 31, 32	AGND	8	Input	Analog ground
19	INP_B	1	Input	Differential analog positive input, channel B

**Pin Functions: LVDS Mode (continued)**

NO.	NAME	# OF PINS	FUNCTION	DESCRIPTION
20	INM_B	1	Input	Differential analog negative input, channel B
23	VCM	1	Output	This terminal outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input terminals
25	CLKP	1	Input	Differential clock positive input
26	CLKM	1	Input	Differential clock negative input
29	INP_A	1	Input	Differential analog positive input, channel A
30	INM_A	1	Input	Differential analog negative input, channel A
35	CTRL1	1	Input	Digital control input terminals. Together, they control the various power-down modes.
36	CTRL2	1	Input	Digital control input terminals. Together, they control the various power-down modes.
37	CTRL3	1	Input	Digital control input terminals. Together, they control the various power-down modes.
49	DRGND	2	Input	Output buffer ground
56	CLKOUTM	1	Output	Differential output clock, complement
57	CLKOUTP	1	Output	Differential output clock, true
64	SDOUT	1	Output	This terminal functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this terminal is in high-impedance state.
40	DA0M	2	Output	Channel A differential output data pair, D0 and D1 multiplexed
41	DA0P			
42	DA2M	2	Output	Channel A differential output data D2 and D3 multiplexed
43	DA2P			
44	DA4M	2	Output	Channel A differential output data D4 and D5 multiplexed
45	DA4P			
46	DA6M	2	Output	Channel A differential output data D6 and D7 multiplexed
47	DA6P			
50	DA8M	2	Output	Channel A differential output data D8 and D9 multiplexed
51	DA8P			
52	DA10M	2	Output	Channel A differential output data D10 and D11 multiplexed
53	DA10P			
54	DA12M	2	Output	Channel A differential output data D12 and D13 multiplexed
55	DA12P			
60	DB0M	2	Output	Channel B differential output data pair, D0 and D1 multiplexed
61	DB0P			
62	DB2M	2	Output	Channel B differential output data D2 and D3 multiplexed
63	DB2P			
2	DB4M	2	Output	Channel B differential output data D4 and D5 multiplexed
3	DB4P			
4	DB6M	2	Output	Channel B differential output data D6 and D7 multiplexed
5	DB6P			
6	DB8M	2	Output	Channel B differential output data D8 and D9 multiplexed
7	DB8P			
8	DB10M	2	Output	Channel B differential output data D10 and D11 multiplexed
9	DB10P			
10	DB12M	2	Output	Channel B differential output data D12 and D13 multiplexed
11	DB12P			
38, 39, 58, 59	NC	4	—	Do not connect, must be floated



(1) The PowerPAD™ is connected to DRGND.

NOTE: NC = do not connect; must float.

**Pin Functions: CMOS Mode**

NO.	NAME	# OF PINS	FUNCTION	DESCRIPTION
1, 48	DRVDD	2	Input	Output buffer supply
12	RESET	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this terminal or by using the software reset option; refer to the <a href="#">Serial Interface Configuration</a> section. In parallel interface mode, the RESET terminal must be permanently tied high. SDATA and SEN are used as parallel control terminals in this mode. This terminal has an internal 150kΩ pull-down resistor.
13	SCLK	1	Input	This terminal functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see <a href="#">表 9</a> for detailed information. This terminal has an internal 150kΩ pull-down resistor.
14	SDATA	1	Input	Serial interface data input; this terminal has an internal 150kΩ pull-down resistor.
15	SEN	1	Input	This terminal functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see <a href="#">表 10</a> for detailed information. This terminal has an internal 150kΩ pull-up resistor to AVDD.
16, 22, 33, 34	AVDD	4	Input	Analog power supply
17, 18, 21, 24, 27, 28, 31, 32	AGND	8	Input	Analog ground
19	INP_B	1	Input	Differential analog positive input, channel B
20	INM_B	1	Input	Differential analog negative input, channel B

**Pin Functions: CMOS Mode (continued)**

NO.	NAME	# OF PINS	FUNCTION	DESCRIPTION
23	VCM	1	Output	This terminal outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input terminals
25	CLKP	1	Input	Differential clock positive input
26	CLKM	1	Input	Differential clock negative input
29	INP_A	1	Input	Differential analog positive input, channel A
30	INM_A	1	Input	Differential analog negative input, channel A
35	CTRL1	1	Input	Digital control input terminals. Together, they control various power-down modes.
36	CTRL2	1	Input	Digital control input terminals. Together, they control various power-down modes.
37	CTRL3	1	Input	Digital control input terminals. Together, they control various power-down modes.
49	DRGND	2	Input	Output buffer ground
56	UNUSED	1	—	This terminal is not used in the CMOS interface
57	CLKOUT	1	Output	CMOS output clock
64	SDOUT	1	Output	This terminal functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this terminal is in high-impedance state.
40	DA0	12	Output	Channel A ADC output data bits, CMOS levels
41	DA1			
42	DA2			
43	DA3			
44	DA4			
45	DA5			
46	DA6			
47	DA7			
50	DA8			
51	DA9			
52	DA10			
53	DA11			
54	DA12	2	Output	Channel A ADC output data bits, CMOS levels
55	DA13			
60	DB0	12	Output	Channel B ADC output data bits, CMOS levels
61	DB1			
62	DB2			
63	DB3			
2	DB4			
3	DB5			
4	DB6			
5	DB7			
6	DB8			
7	DB8			
8	DB10			
9	DB11			
10	DB12	2	Output	Channel B ADC output data bits, CMOS levels
11	DB13			
38, 39, 58, 59	NC	1	—	Do not connect, must be floated

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, AVDD		−0.3	2.1	V
Supply voltage, DRVDD		−0.3	2.1	V
Voltage between AGND and DRGND		−0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		−2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		−2.4	2.4	V
Voltage applied to input terminals	INP_A, INM_A, INP_B, INM_B	−0.3	Minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM <sup>(2)</sup>	−0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	−0.3	3.9	V
Junction temperature, T <sub>J</sub>		−55	+150	°C
Storage temperature, T <sub>stg</sub>		−65	+150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|). This configuration prevents the ESD protection diodes at the clock input terminals from turning on.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>ESD</sub> <sup>(1)</sup>	Human body model (HBM) <sup>(2)</sup>	±2000	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

PARAMETER	MIN	NOM	MAX	UNIT
<b>SUPPLIES</b>				
Analog supply voltage, AVDD	1.7	1.8	1.9	V
Digital supply voltage, DRVDD	1.7	1.8	1.9	V
<b>ANALOG INPUTS</b>				
Differential input voltage	2			V <sub>PP</sub>
Input common-mode voltage	VCM ±0.05			V
Maximum analog input frequency with 2V <sub>PP</sub> input amplitude <sup>(1)</sup>	400			MHz
Maximum analog input frequency with 1V <sub>PP</sub> input amplitude <sup>(1)</sup>	600			MHz
<b>CLOCK INPUT</b>				
<b>Input clock sample rate</b>				
Low-speed mode enabled <sup>(2)</sup>	1		80	MSPS
Low-speed mode disabled <sup>(2)</sup> (by default after reset)	80		125	MSPS
<b>Input clock duty cycle</b>				
Low-speed mode disabled <sup>(3)</sup>	35%	50%	65%	
Low-speed mode enabled <sup>(3)</sup>	40%	50%	60%	
<b>DIGITAL OUTPUTS</b>				
Maximum external load capacitance from each output terminal to DRGND, C <sub>LOAD</sub>	5			pF
Differential load resistance between the LVDS output pairs (LVDS mode), R <sub>LOAD</sub>	100			Ω
Operating junction temperature, T <sub>J</sub>	-55		+125	°C

(1) See the [Theory of Operation](#) section in the Application Information.

(2) See the [Serial Interface Configuration](#) section for details on programming the low-speed mode.

(3) Ensured by design for temperature range -40°C to 85°C.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADS4245-EP	UNIT
		RGC	
		64 TERMINAL	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	23.9	°C/W
R <sub>θJctop</sub>	Junction-to-case (top) thermal resistance	10.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	4.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.1	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	4.4	
R <sub>θJcbot</sub>	Junction-to-case (bottom) thermal resistance	0.6	

(1) 有关传统和新热指标的更多信息，请参见应用报告《半导体和 IC 封装热指标》（文献编号：SPRA953）。

**表 1. High-Performance Modes<sup>(1)(2)</sup>**

PARAMETER	DESCRIPTION
High-performance mode	Set the HIGH PERF MODE register bit to obtain best performance across sample clock and input signal frequencies. Register address = 03h, data = 03h
High-frequency mode	Set the HIGH FREQ MODE CH A and HIGH FREQ MODE CH B register bits for high input signal frequencies greater than 200MHz. Register address = 4Ah, data = 01h Register address = 58h, data = 01h

(1) It is recommended to use these modes to obtain best performance.

(2) See the [Serial Interface Configuration](#) section for details on register programming.

## 6.5 Electrical Characteristics:

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, LVDS interface, and 0dB gain (unless otherwise noted). Minimum and maximum values are across the recommended operating condition (unless otherwise noted), AVDD = 1.8V, and DRVDD = 1.8V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14	Bits
Signal-to-noise ratio	SNR	$f_{IN} = 20\text{MHz}$	73.4		dBFS
		$f_{IN} = 70\text{MHz}$	68	72.9	dBFS
		$f_{IN} = 100\text{MHz}$		72.6	dBFS
		$f_{IN} = 170\text{MHz}$		71.4	dBFS
		$f_{IN} = 300\text{MHz}$		69.3	dBFS
Signal-to-noise and distortion ratio	SINAD	$f_{IN} = 20\text{MHz}$	73.2		dBFS
		$f_{IN} = 70\text{MHz}$	68	72.6	dBFS
		$f_{IN} = 100\text{MHz}$		72.3	dBFS
		$f_{IN} = 170\text{MHz}$		71.2	dBFS
		$f_{IN} = 300\text{MHz}$		68.5	dBFS
Spurious-free dynamic range	SFDR	$f_{IN} = 20\text{MHz}$		88	dBc
		$f_{IN} = 70\text{MHz}$	71	86	dBc
		$f_{IN} = 100\text{MHz}$		85	dBc
		$f_{IN} = 170\text{MHz}$		88	dBc
		$f_{IN} = 300\text{MHz}$		78	dBc
Total harmonic distortion	THD	$f_{IN} = 20\text{MHz}$		86	dBc
		$f_{IN} = 70\text{MHz}$	68	84	dBc
		$f_{IN} = 100\text{MHz}$		83	dBc
		$f_{IN} = 170\text{MHz}$		84	dBc
		$f_{IN} = 300\text{MHz}$		75	dBc
Second-harmonic distortion	HD2	$f_{IN} = 20\text{MHz}$		88	dBc
		$f_{IN} = 70\text{MHz}$	66.5	86	dBc
		$f_{IN} = 100\text{MHz}$		85	dBc
		$f_{IN} = 170\text{MHz}$		88	dBc
		$f_{IN} = 300\text{MHz}$		78	dBc
Third-harmonic distortion	HD3	$f_{IN} = 20\text{MHz}$		93	dBc
		$f_{IN} = 70\text{MHz}$	72.5	89	dBc
		$f_{IN} = 100\text{MHz}$		89	dBc
		$f_{IN} = 170\text{MHz}$		90	dBc
		$f_{IN} = 300\text{MHz}$		81	dBc
Worst spur (other than second and third harmonics)		$f_{IN} = 20\text{MHz}$		95	dBc
		$f_{IN} = 70\text{MHz}$	73	94	dBc
		$f_{IN} = 100\text{MHz}$		93	dBc
		$f_{IN} = 170\text{MHz}$		91	dBc
		$f_{IN} = 300\text{MHz}$		89	dBc
Two-tone intermodulation distortion	IMD	$f_1 = 46\text{MHz}$ , $f_2 = 50\text{MHz}$ , each tone at –7dBFS		96	dBFS
		$f_1 = 185\text{MHz}$ , $f_2 = 190\text{MHz}$ , each tone at –7dBFS		92	dBFS
Crosstalk	20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel		95		dB
Input overload recovery	Recovery to within 1% (of full-scale) for 6dB overload with sine-wave input		1		Clock cycle
AC power-supply rejection ratio	PSRR For 100mV <sub>pp</sub> signal on AVDD supply, up to 10MHz		> 30		dB
Effective number of bits	ENOB $f_{IN} = 70\text{MHz}$		11.5		LSBs
Differential nonlinearity	DNL $f_{IN} = 70\text{MHz}$	–0.97	±0.5	1.9	LSBs
Integrated nonlinearity	INL $f_{IN} = 70\text{MHz}$		±2	±5	LSBs

## 6.6 Electrical Characteristics: General

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, 50% clock duty cycle, and –1dBFS differential analog input (unless otherwise noted). Minimum and maximum values are across the recommended operating condition (unless otherwise noted), AVDD = 1.8V, and DRVDD = 1.8V.

PARAMETER	MIN	TYP	MAX	UNIT
<b>ANALOG INPUTS</b>				
Differential input voltage range (0dB gain)		2		V <sub>PP</sub>
Differential input resistance (at 200MHz)		0.75		kΩ
Differential input capacitance (at 200MHz)		3.7		pF
Analog input bandwidth (with 50Ω source impedance, and 50Ω termination)		550		MHz
Analog input common-mode current (per input terminal of each channel)		1.5		μA/MSPS
Common-mode output voltage	VCM	0.95		V
VCM output current capability		4		mA
<b>DC ACCURACY</b>				
Offset error	–25	2.5	25	mV
Temperature coefficient of offset error		0.003		mV/°C
Gain error as a result of internal reference inaccuracy alone	E <sub>GREF</sub>	–4	4	%FS
Gain error of channel alone	E <sub>GCHAN</sub>	±0.1		%FS
Temperature coefficient of E <sub>GCHAN</sub>		0.002		Δ%/°C
<b>POWER SUPPLY</b>				
IAVDD Analog supply current		105	130	mA
IDRVDD Output buffer supply current LVDS interface, 350mV swing with 100Ω external termination, f <sub>IN</sub> = 2.5MHz		99	120	mA
IDRVDD Output buffer supply current CMOS interface, no load capacitance <sup>(1)</sup> f <sub>IN</sub> = 2.5MHz		49		mA
Analog power		189		mW
Digital power LVDS interface, 350mV swing with 100Ω external termination, f <sub>IN</sub> = 2.5MHz		179		mW
Digital power CMOS interface, no load capacitance <sup>(1)</sup> f <sub>IN</sub> = 2.5MHz		88		mW
Global power-down			25	mW

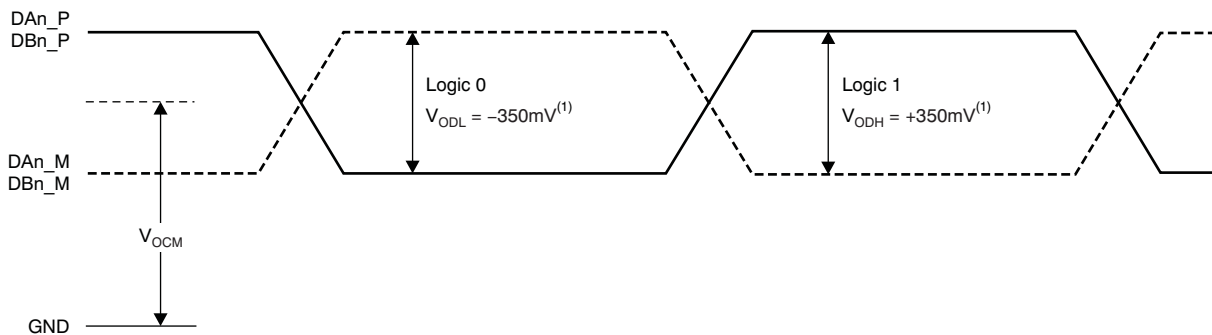
(1) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output terminals, input frequency, and the supply voltage (see the [CMOS Interface Power Dissipation](#) section in the [Application Information](#)).

## 6.7 Digital Characteristics

At AVDD = 1.8V and DRVDD = 1.8V (unless otherwise noted). DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'.

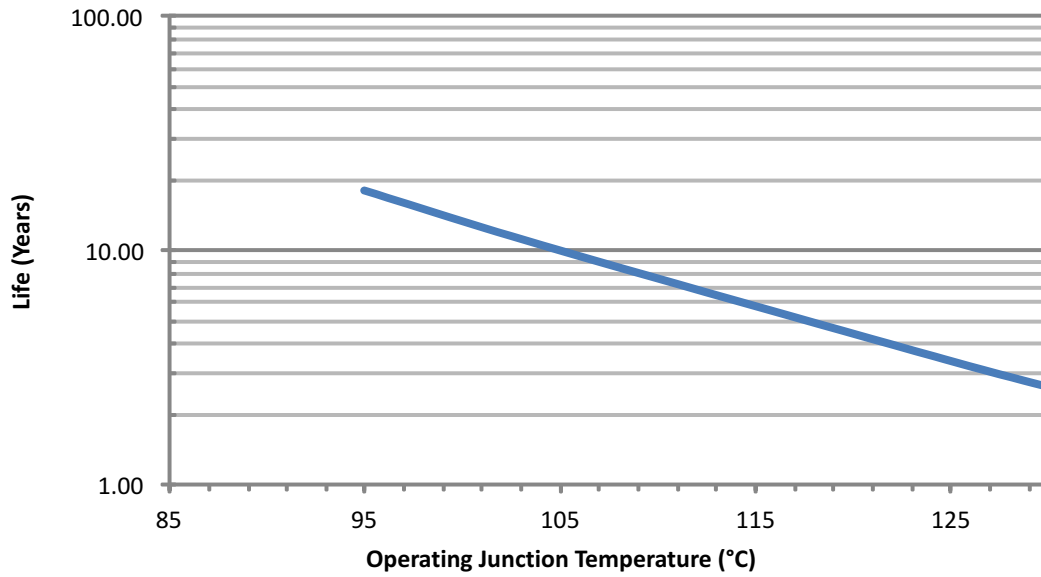
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)<sup>(1)</sup></b>						
High-level input voltage		All digital inputs support 1.8V and 3.3V CMOS logic levels	1.3			V
Low-level input voltage			0.4			V
High-level input current	SDATA, SCLK <sup>(2)</sup>	V <sub>HIGH</sub> = 1.8V	10			μA
	SEN <sup>(3)</sup>	V <sub>HIGH</sub> = 1.8V	0			μA
Low-level input current	SDATA, SCLK	V <sub>LOW</sub> = 0V	0			μA
	SEN	V <sub>LOW</sub> = 0V	10			μA
<b>DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT)</b>						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
Output capacitance (internal to device)						pF
<b>DIGITAL OUTPUTS, LVDS INTERFACE</b>						
High-level output differential voltage	V <sub>ODH</sub>	With an external 100Ω termination	220	350	490	mV
Low-level output differential voltage	V <sub>ODL</sub>	With an external 100Ω termination	–490	–350	–220	mV
Output common-mode voltage	V <sub>OCM</sub>		0.9	1.05	1.25	V

- (1) SCLK, SDATA, and SEN function as digital input terminals in serial configuration mode.
- (2) SDATA, SCLK have internal 150kΩ pull-down resistor.
- (3) SEN has an internal 150kΩ pull-up resistor to AVDD. Because the pull-up is weak, SEN can also be driven by 1.8V or 3.3V CMOS buffers.



- (1) With external 100Ω termination.

**图 1. LVDS Output Voltage Levels**



- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

**图 2. ADS4245-EP Electromigration Fail Mode Chart**

## 6.8 Timing Characteristics: LVDS And CMOS Modes<sup>(1)</sup>

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8V, sampling frequency = 160MSPS, sine wave input clock, 1.5V<sub>pp</sub> clock amplitude, C<sub>LOAD</sub> = 5pF<sup>(2)</sup>, and R<sub>LOAD</sub> = 100Ω<sup>(3)</sup>, unless otherwise noted. Minimum and maximum values are across the full temperature range: T<sub>MIN</sub> = -55°C to T<sub>MAX</sub> = +125°C, AVDD = 1.8V, and DRVDD = 1.7V to 1.9V.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT		
t <sub>A</sub>	Aperture delay		0.8		ns		
	Aperture delay matching	Between the two channels of the same device		±70	ps		
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150	ps		
t <sub>J</sub>	Aperture jitter		140		f <sub>S</sub> rms		
	Wakeup time	Time to valid data after coming out of STANDBY mode		50	100	μs	
		Time to valid data after coming out of GLOBAL power-down mode		100	500	μs	
ADC latency <sup>(4)</sup>	Default latency after reset		16		Clock cycles		
	Digital functions enabled (EN DIGITAL = 1)		24		Clock cycles		
<b>DDR LVDS MODE<sup>(5)</sup></b>							
t <sub>SU</sub>	Data setup time	Data valid <sup>(6)</sup> to zero-crossing of CLKOUTP		1.5	2.0	ns	
t <sub>H</sub>	Data hold time	Zero-crossing of CLKOUTP to data becoming invalid <sup>(6)</sup>		0.35	0.6	ns	
t <sub>PDI</sub>	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over		5.0	6.1	7.5	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM)		49		%	
t <sub>RISE</sub> , t <sub>FALL</sub>	Data rise time, Data fall time	Rise time measured from -100mV to +100mV Fall time measured from +100mV to -100mV <i>1MSPS ≤ Sampling frequency ≤ 160MSPS</i>		0.13		ns	
t <sub>CLKRISE</sub> , t <sub>CLKFALL</sub>	Output clock rise time, Output clock fall time	Rise time measured from -100mV to +100mV Fall time measured from +100mV to -100mV <i>1MSPS ≤ Sampling frequency ≤ 160MSPS</i>		0.13		ns	
<b>PARALLEL CMOS MODE</b>							
t <sub>SU</sub>	Data setup time	Data valid <sup>(7)</sup> to zero-crossing of CLKOUT		1.6	2.5	ns	
t <sub>H</sub>	Data hold time	Zero-crossing of CLKOUT to data becoming invalid <sup>(7)</sup>		2.3	2.7	ns	
t <sub>PDI</sub>	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over		4.5	6.4	8.5	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT <i>1MSPS ≤ Sampling frequency ≤ 160MSPS</i>		46		%	
t <sub>RISE</sub> , t <sub>FALL</sub>	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD <i>1MSPS ≤ Sampling frequency ≤ 160MSPS</i>		1		ns	
t <sub>CLKRISE</sub> , t <sub>CLKFALL</sub>	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD <i>1MSPS ≤ Sampling frequency ≤ 160MSPS</i>		1		ns	

(1) Timing parameters are ensured by design and characterization and not tested in production.

(2) C<sub>LOAD</sub> is the effective external single-ended load capacitance between each output terminal and ground

(3) R<sub>LOAD</sub> is the differential load resistance between the LVDS output pair.

(4) At higher frequencies, t<sub>PDI</sub> is greater than one clock period and overall latency = ADC latency + 1.

(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.

(6) Data valid refers to a logic high of +100mV and a logic low of -100mV.

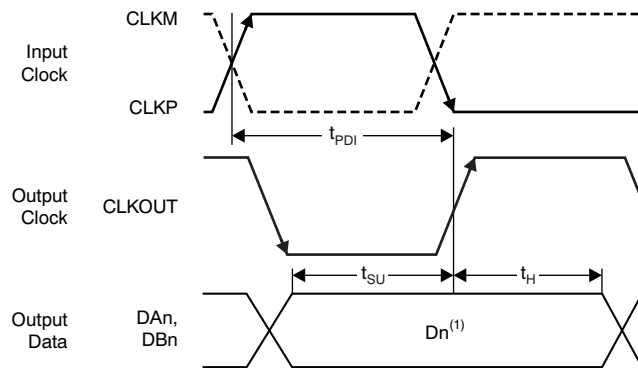
(7) Data valid refers to a logic high of 1.26V and a logic low of 0.54V

表 2. LVDS Timings At Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)			$t_{PDI}$ , CLOCK PROPAGATION DELAY (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	5.9	6.6		0.35	0.6		5.0	6.1	7.5
80	4.5	5.2		0.35	0.6		5.0	6.1	7.5
125	2.3	2.9		0.35	0.6		5.0	6.1	7.5

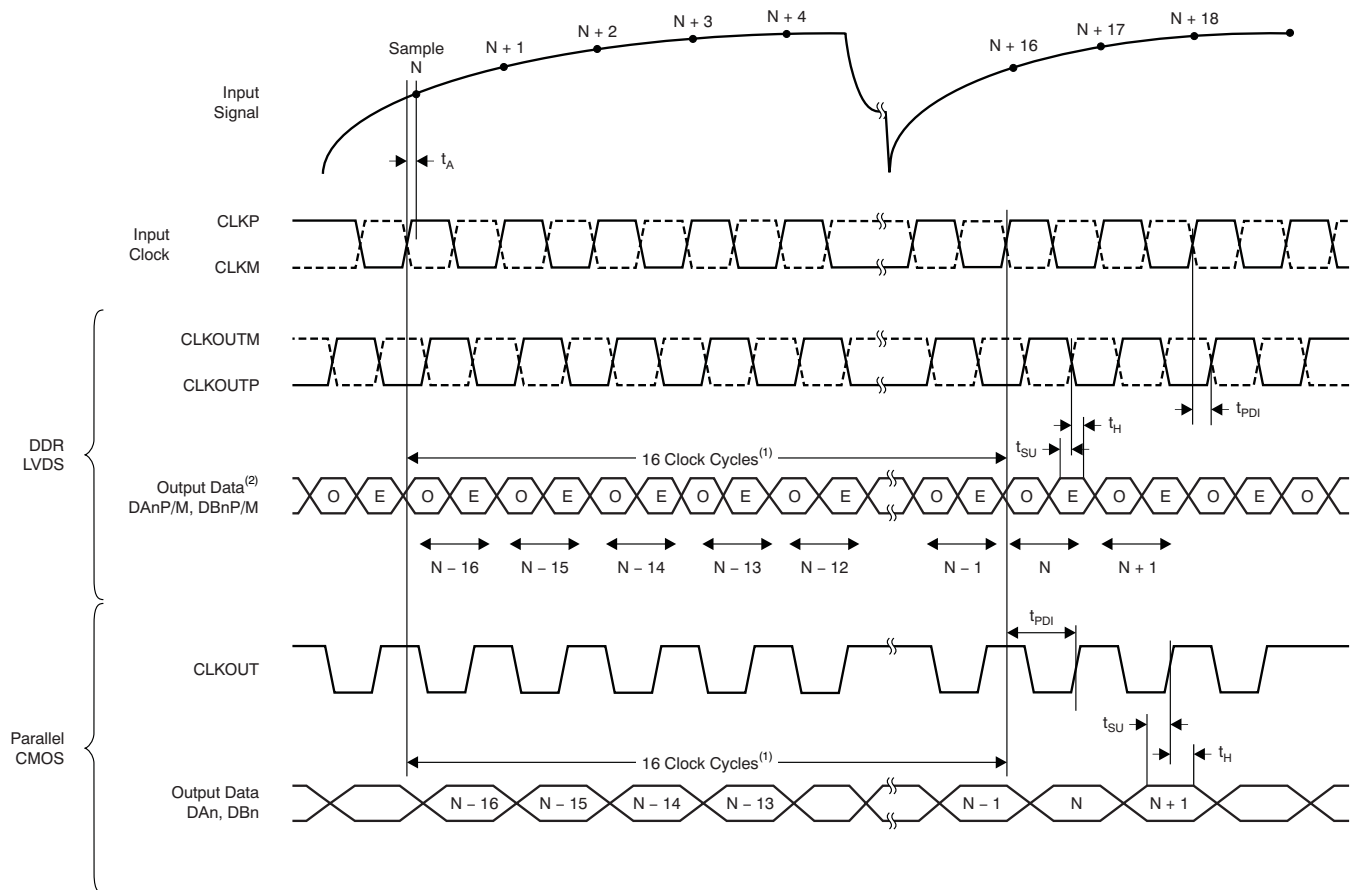
表 3. CMOS Timings At Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT								
	SETUP TIME (ns)			HOLD TIME (ns)			$t_{PDI}$ , CLOCK PROPAGATION DELAY (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	6.1	7.2		6.7	7.1		4.5	6.4	8.5
80	4.7	5.8		5.3	5.8		4.5	6.4	8.5
125	2.7	3.6		3.1	3.6		4.5	6.4	8.5



(1) Dn = bits D0, D1, D2, etc. of channels A and B.

图 3. CMOS Interface Timing Diagram



(1) ADC latency after reset. At higher sampling frequencies,  $t_{PDI}$  is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.

(2) E = even bits (D0, D2, D4, etc.); O = odd bits (D1, D3, D5, etc.).

图 4. Latency Timing Diagram

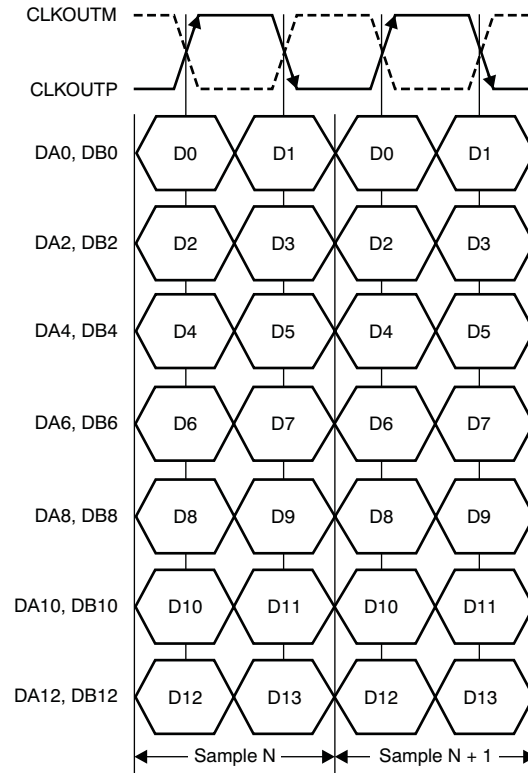


图 5. ADS4245 LVDS Interface Timing Diagram

**6.9 Typical Characteristics:**

At  $T_A = +25^\circ\text{C}$ ,  $AV_{DD} = 1.8\text{V}$ ,  $DRV_{DD} = 1.8\text{V}$ , maximum rated sampling frequency, sine wave input clock,  $1.5\text{V}_{PP}$  differential clock amplitude, 50% clock duty cycle,  $-1\text{dBFS}$  differential analog input, High-Performance Mode disabled,  $0\text{dB}$  gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

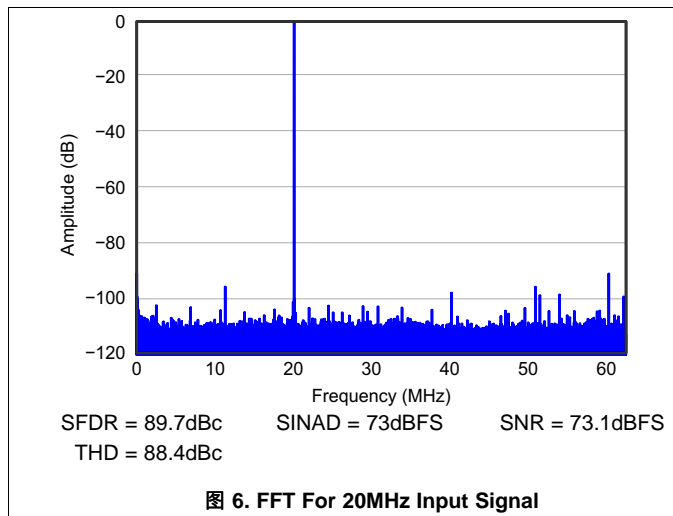


图 6. FFT For 20MHz Input Signal

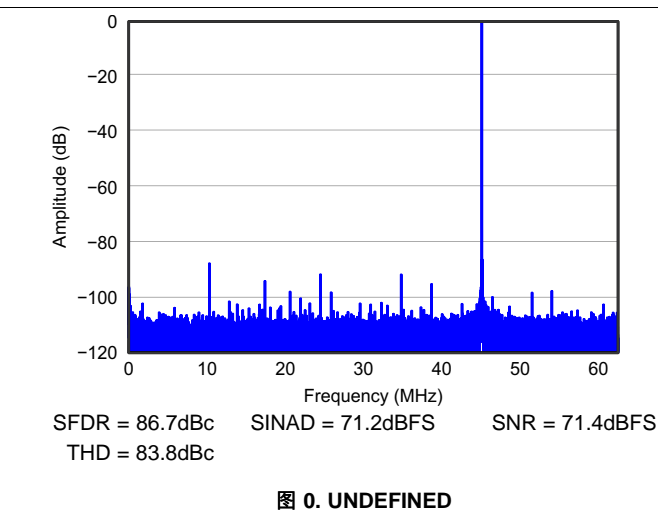


图 0. UNDEFINED

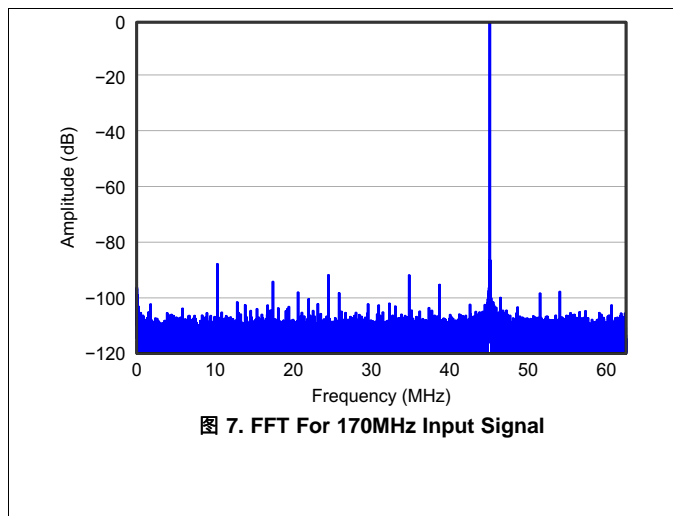


图 7. FFT For 170MHz Input Signal

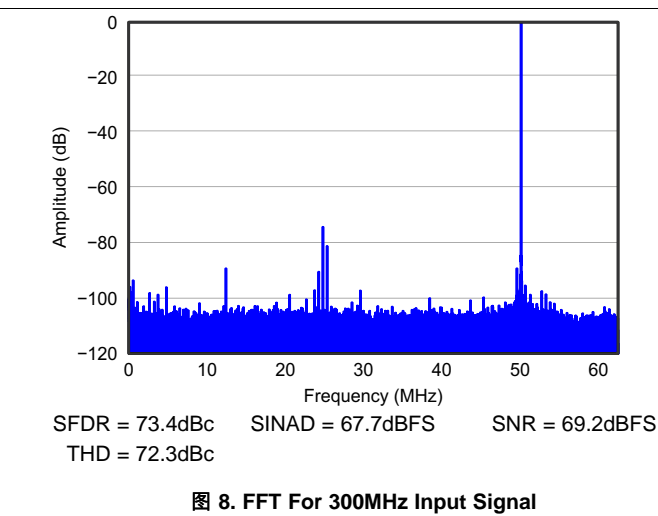


图 8. FFT For 300MHz Input Signal

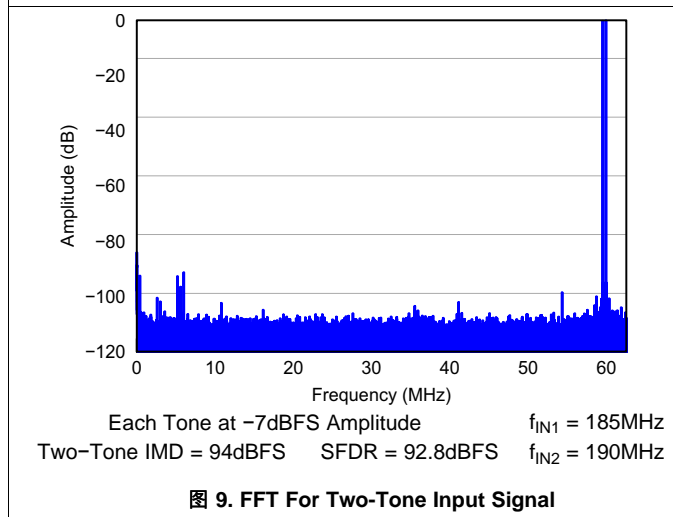


图 9. FFT For Two-Tone Input Signal

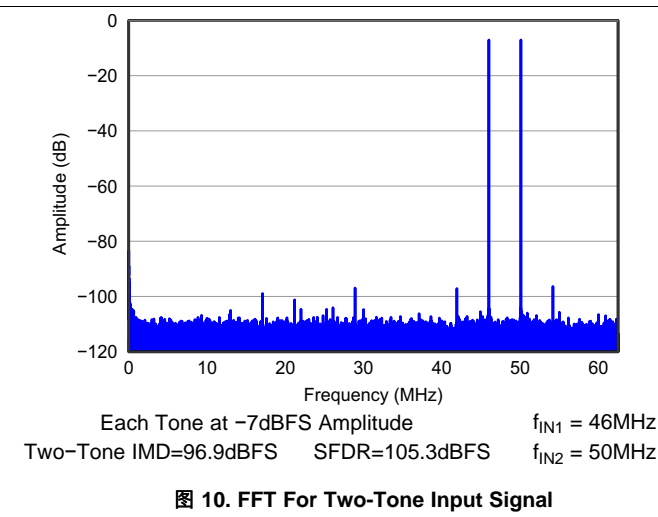
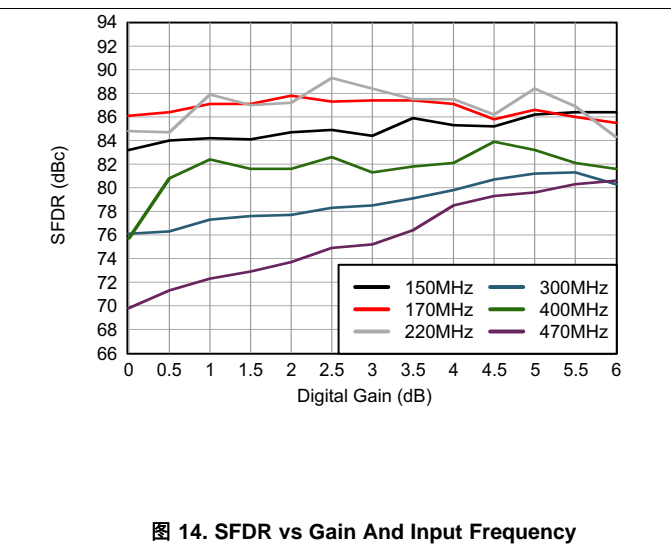
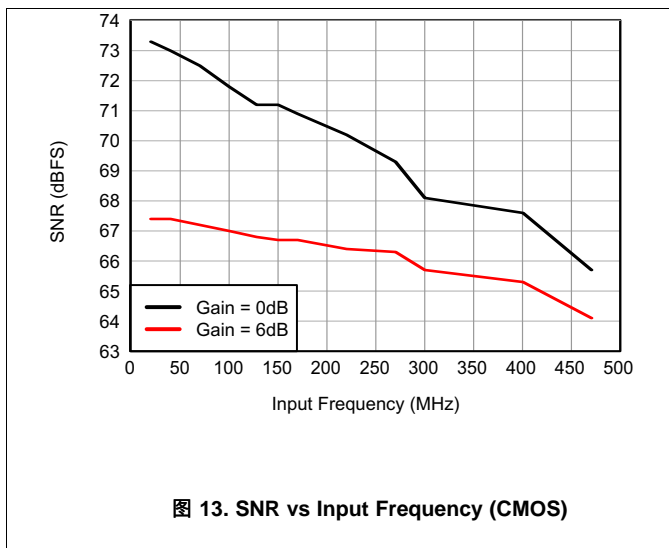
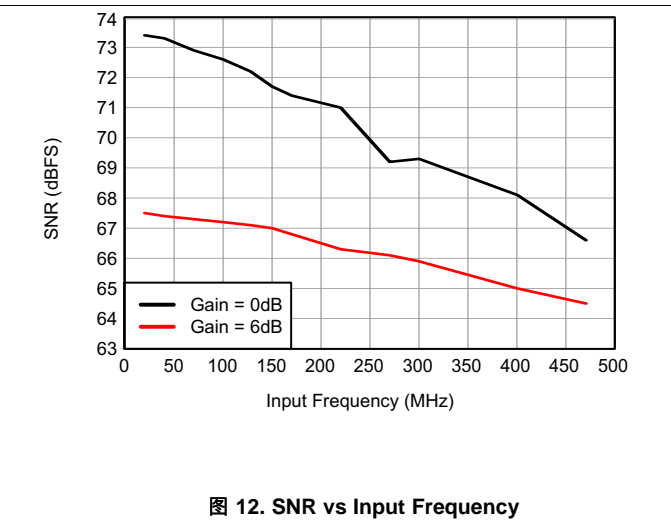
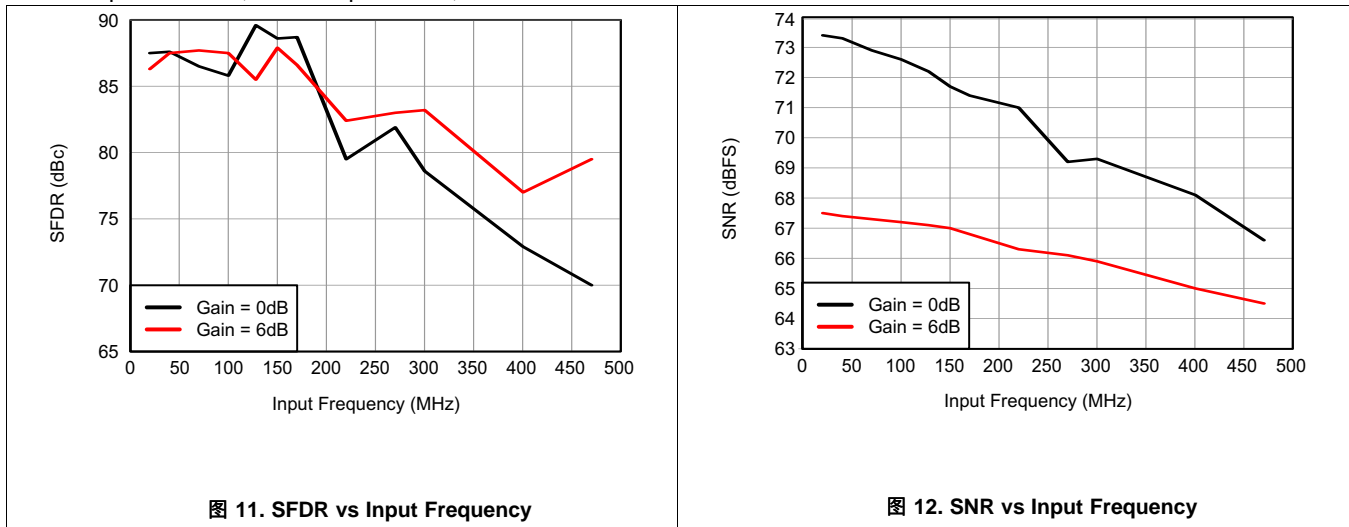


图 10. FFT For Two-Tone Input Signal

**Typical Characteristics: (接下页)**

At  $T_A = +25^\circ\text{C}$ ,  $AV_{DD} = 1.8\text{V}$ ,  $DRV_{DD} = 1.8\text{V}$ , maximum rated sampling frequency, sine wave input clock,  $1.5\text{V}_{PP}$  differential clock amplitude, 50% clock duty cycle,  $-1\text{dBFS}$  differential analog input, High-Performance Mode disabled,  $0\text{dB}$  gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



Typical Characteristics: (接下页)

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 1.8\text{V}$ ,  $DRVDD = 1.8\text{V}$ , maximum rated sampling frequency, sine wave input clock,  $1.5\text{V}_{PP}$  differential clock amplitude, 50% clock duty cycle,  $-1\text{dBFS}$  differential analog input, High-Performance Mode disabled,  $0\text{dB}$  gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

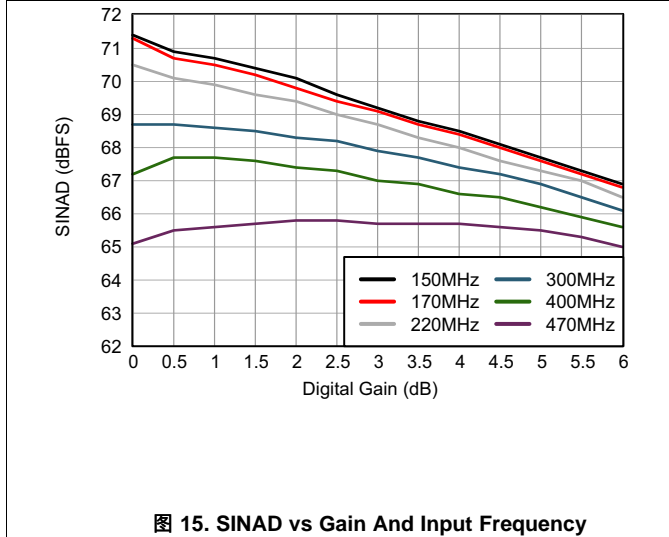


图 15. SINAD vs Gain And Input Frequency

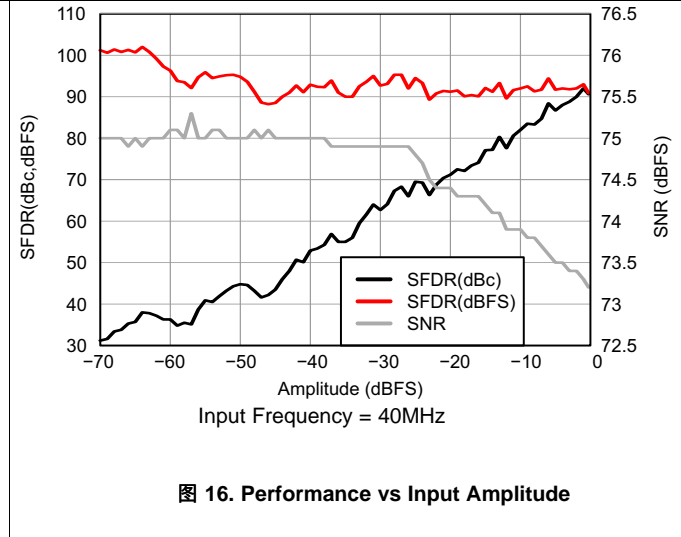


图 16. Performance vs Input Amplitude

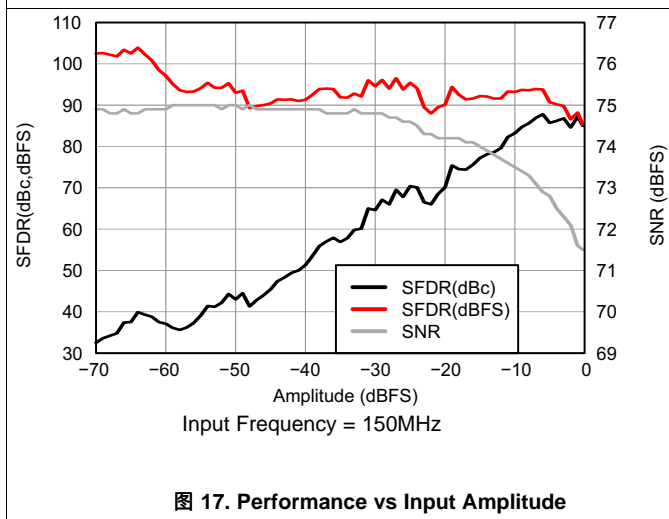


图 17. Performance vs Input Amplitude

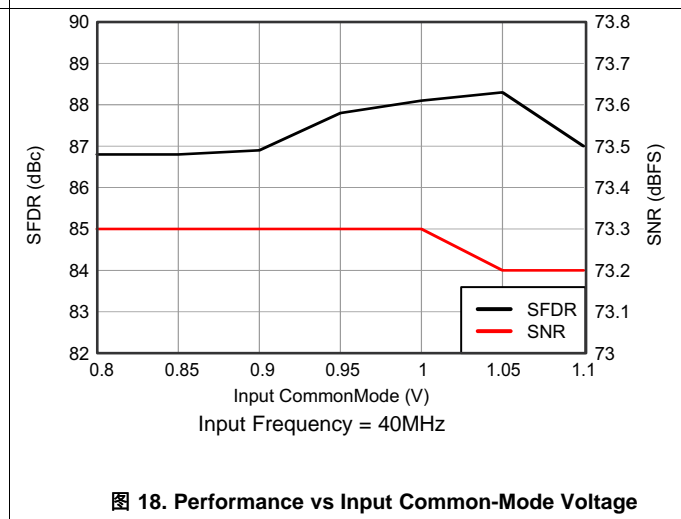


图 18. Performance vs Input Common-Mode Voltage

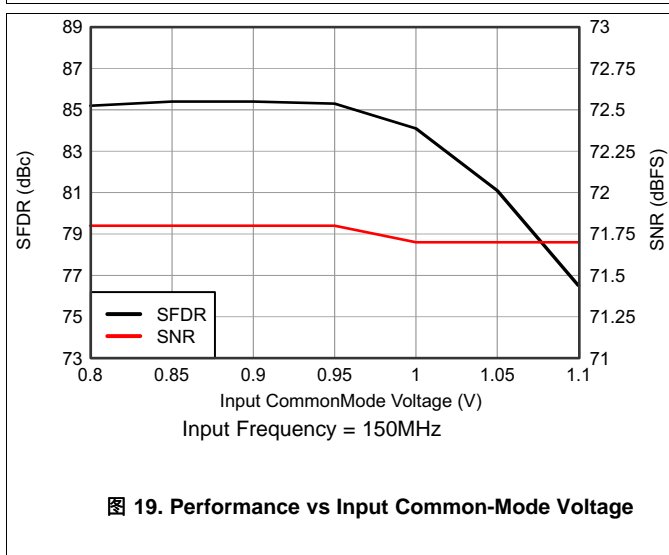


图 19. Performance vs Input Common-Mode Voltage

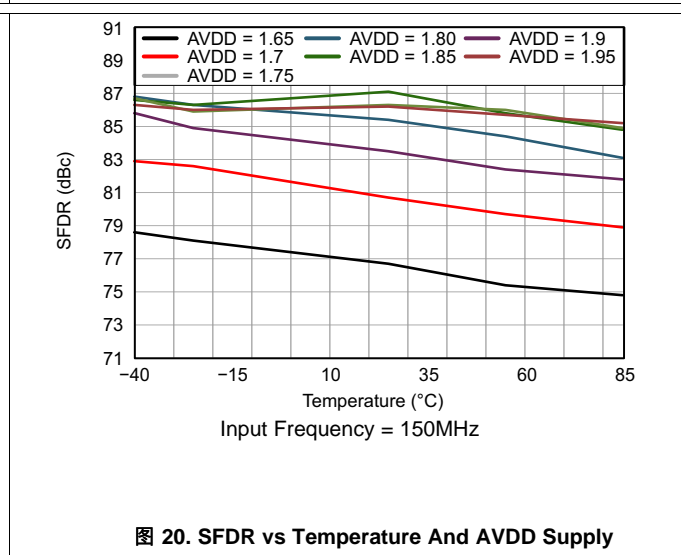


图 20. SFDR vs Temperature And AVDD Supply

**Typical Characteristics: (接下页)**

At  $T_A = +25^\circ\text{C}$ , AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock,  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle,  $-1\text{dBFS}$  differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

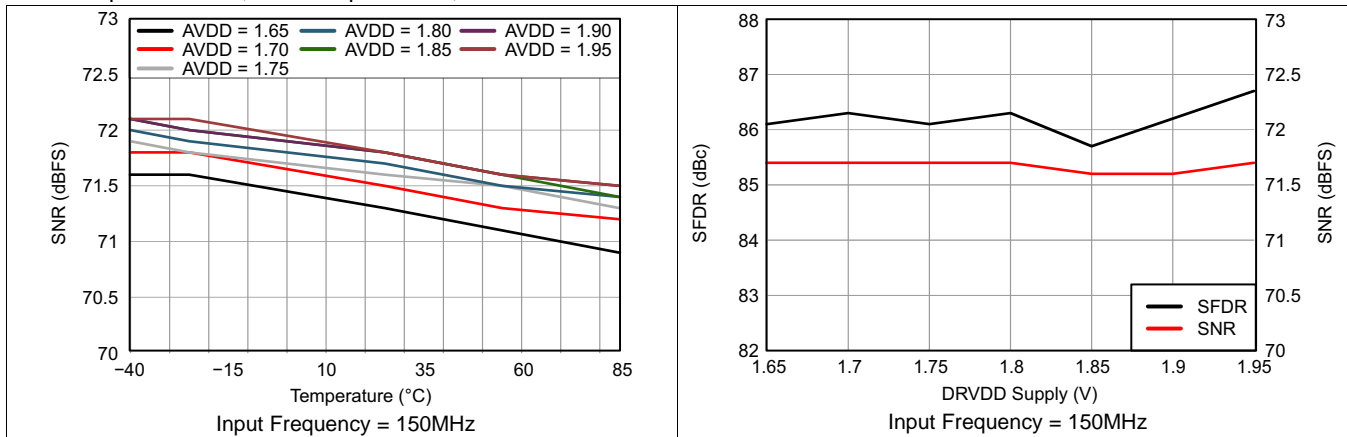


图 21. SNR vs Temperature And AVDD Supply

图 22. Performance vs DRVDD Supply Voltage

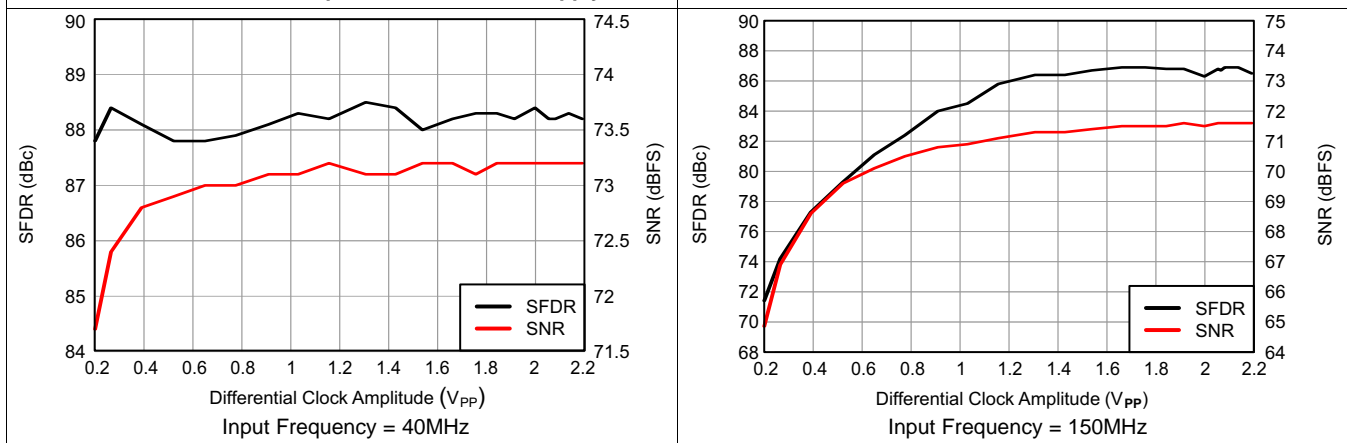
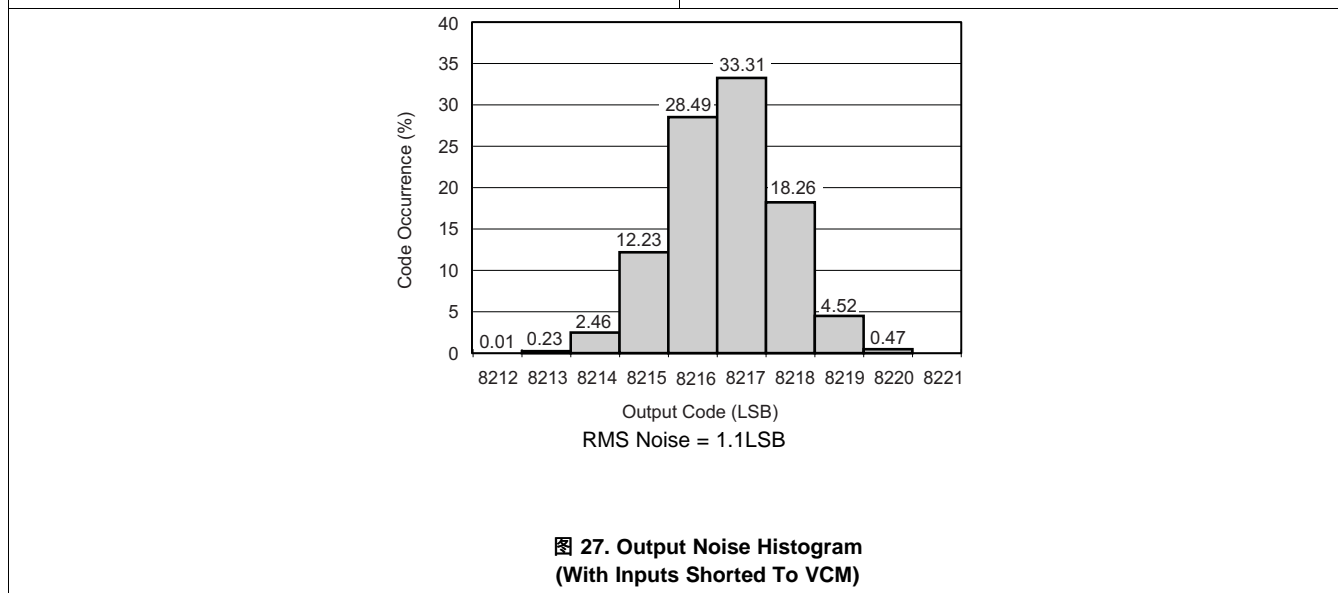
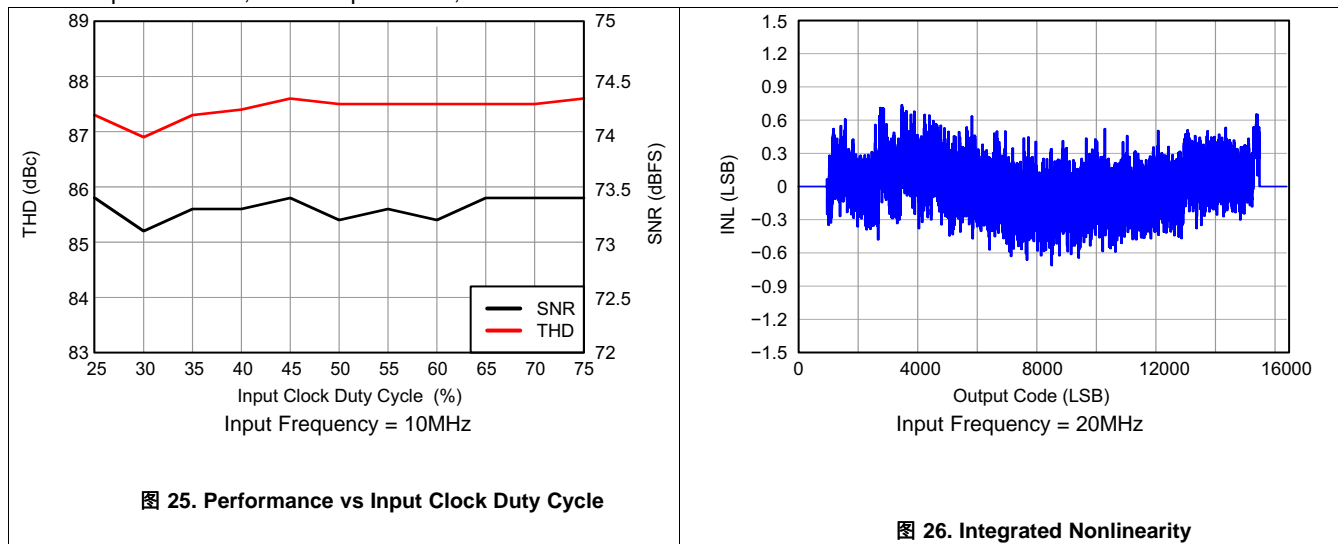


图 23. Performance vs Input Clock Amplitude

图 24. Performance vs Input Clock Amplitude

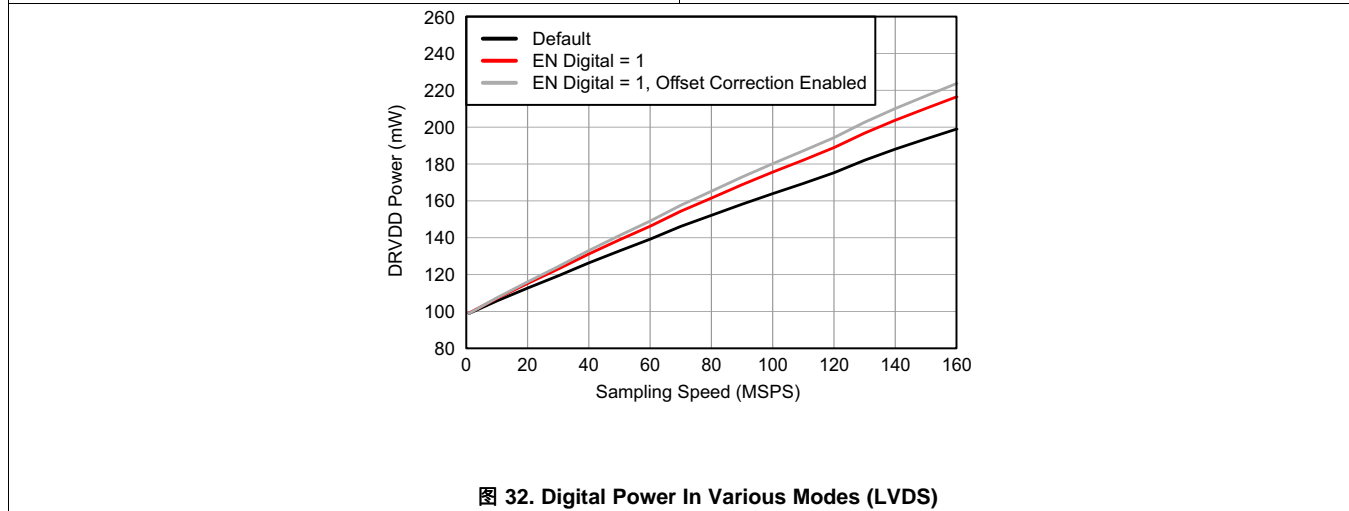
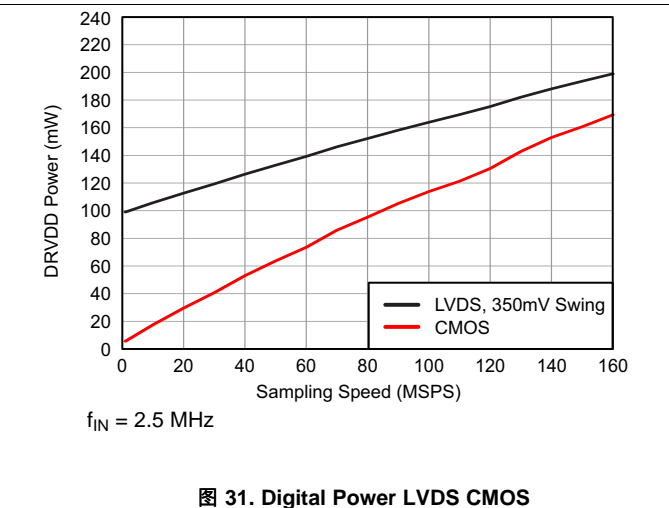
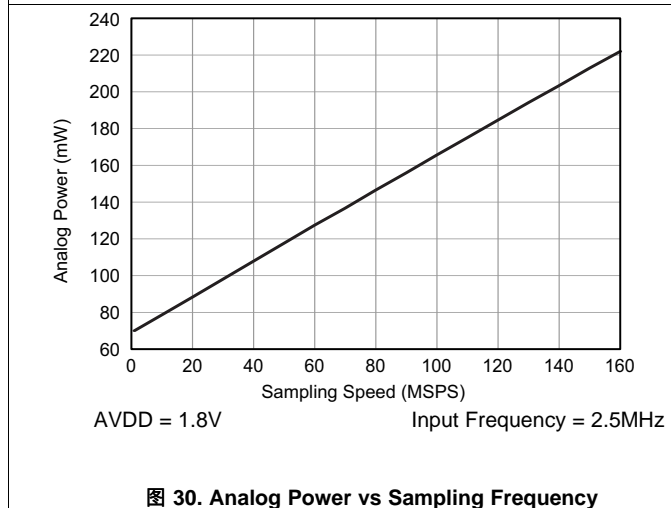
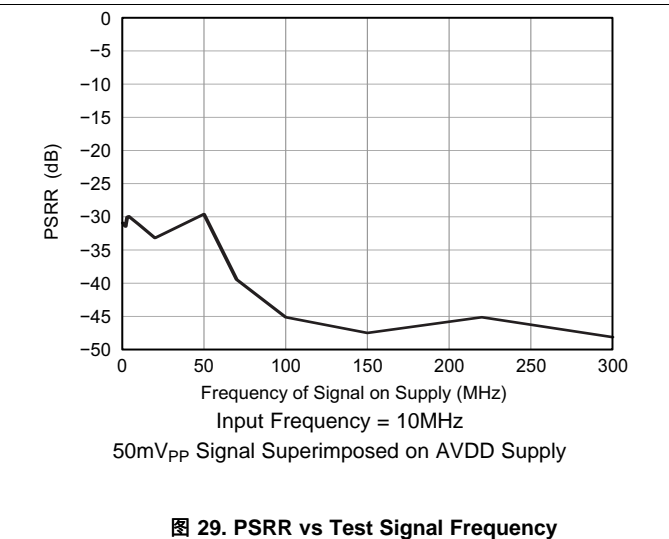
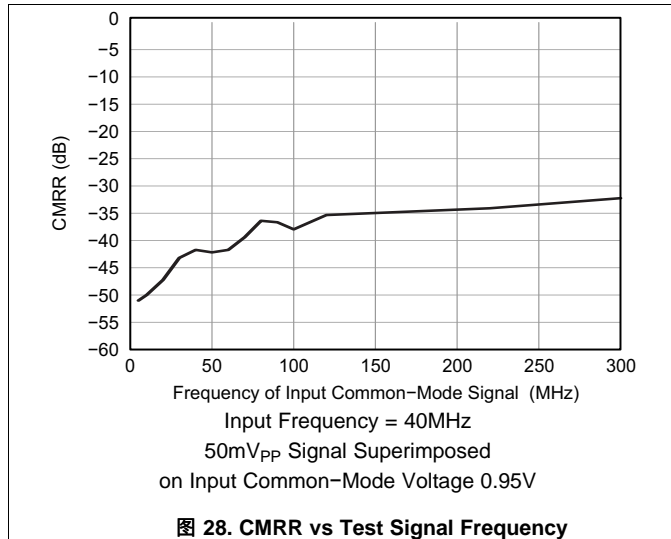
**Typical Characteristics: (接下页)**

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 1.8\text{V}$ ,  $DRVDD = 1.8\text{V}$ , maximum rated sampling frequency, sine wave input clock,  $1.5V_{PP}$  differential clock amplitude, 50% clock duty cycle,  $-1\text{dBFS}$  differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



### 6.10 Typical Characteristics: General

At  $T_A = +25^\circ\text{C}$ ,  $AVDD = 1.8\text{V}$ ,  $DRVDD = 1.8\text{V}$ , maximum rated sampling frequency, sine wave input clock,  $1.5\text{V}_{PP}$  differential clock amplitude, 50% clock duty cycle,  $-1\text{dBFS}$  differential analog input, High-Performance Mode disabled,  $0\text{dB}$  gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.



### 6.11 Typical Characteristics: Contour

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V<sub>pp</sub> differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, High-Performance Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

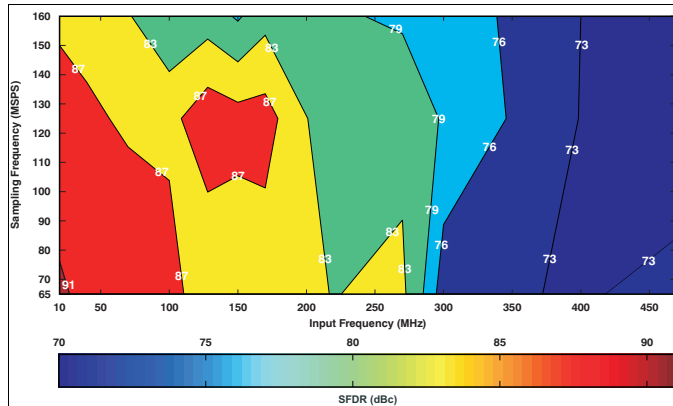


图 33. Spurious-Free Dynamic Range (0dB Gain)

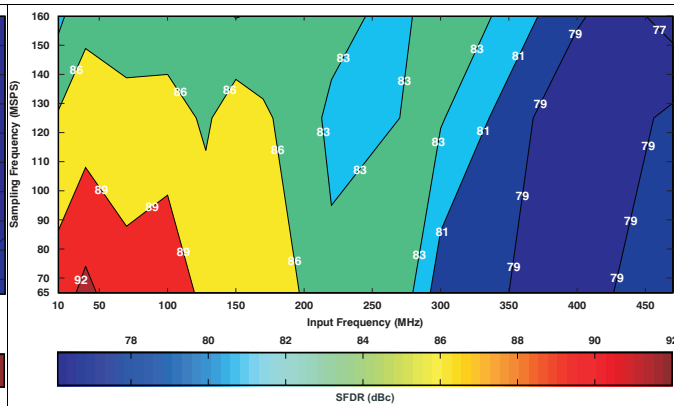


图 34. Spurious-Free Dynamic Range (6dB Gain)

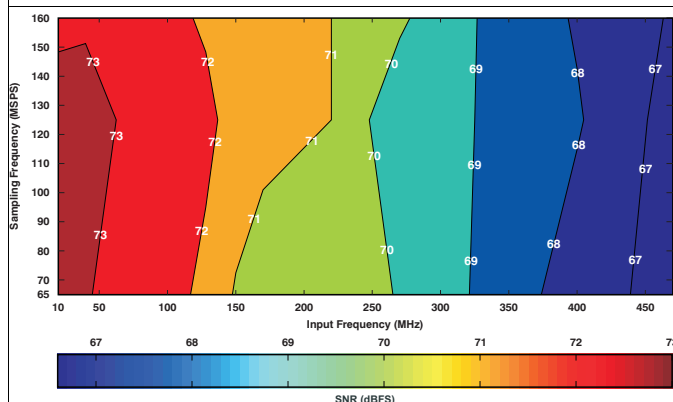


图 35. Signal-To-Noise Ratio (0dB Gain)

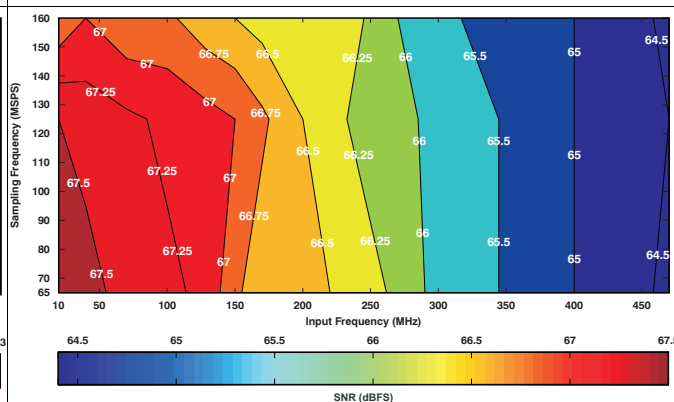


图 36. Signal-To-Noise Ratio (6dB Gain)

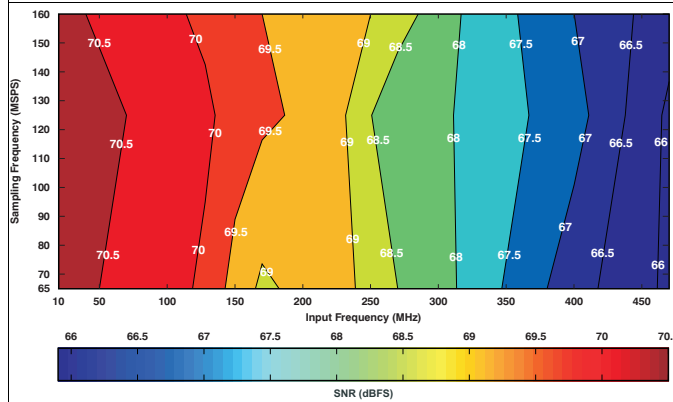


图 37. Signal-To-Noise Ratio (0dB Gain)

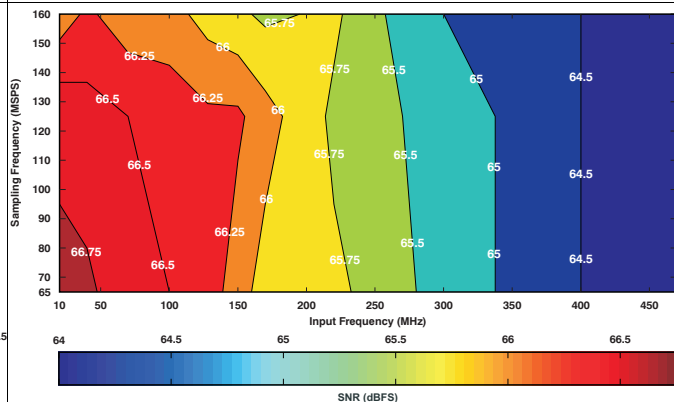


图 38. Signal-To-Noise Ratio (6dB Gain)

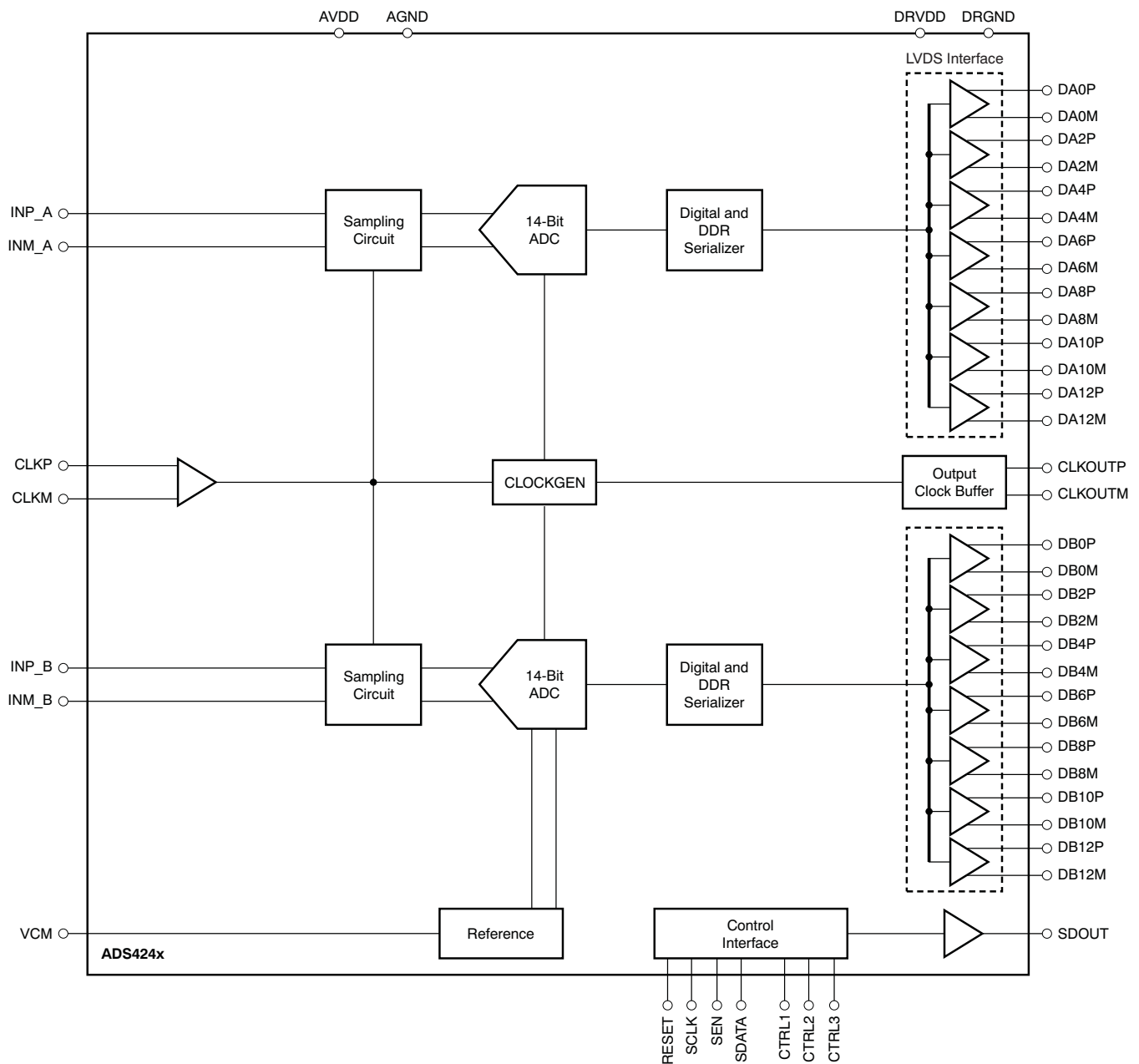
## 7 Detailed Description

### 7.1 Overview

The ADS4245 is a low-speed variant of the ADS42xx ultralow-power family of dual-channel, 14-bit analog-to-digital converters (ADCs). Innovative design techniques are used to achieve high-dynamic performance, while consuming extremely low power with 1.8V supply.

The ADS4245 has gain options that can be used to improve SFDR performance at lower full-scale input ranges. This device includes a dc offset correction loop that can be used to cancel the ADC offset.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The ADS4245 is terminal-compatible with the previous generation ADS62P49 family of data converters; this architecture enables easy migration. However, there are some important differences between the two device generations, summarized in 表 4.

表 4. Migrating From The ADS62P49

ADS62P49 FAMILY	ADS4245 FAMILY
<b>TERMINALS</b>	
Terminal 22 is NC (not connected)	Terminal 22 is AVDD
Terminals 38 and 58 are DRVDD	Terminals 38 and 58 are NC (do not connect, must be floated)
Terminals 39 and 59 are DRGND	Terminals 39 and 59 are NC (do not connect, must be floated)
<b>SUPPLY</b>	
AVDD is 3.3V	AVDD is 1.8V
DRVDD is 1.8V	No change
<b>INPUT COMMON-MODE VOLTAGE</b>	
VCM is 1.5V	VCM is 0.95V
<b>SERIAL INTERFACE</b>	
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map
<b>EXTERNAL REFERENCE</b>	
Supported	Not supported

### 7.4 Device Functional Modes

#### 7.4.1 Digital Functions

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data terminals with a latency of 16 clock cycles. 图 39 shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to '1'. After this, the respective register bits must be programmed as described in the following sections and in the [Serial Register Map](#) section.

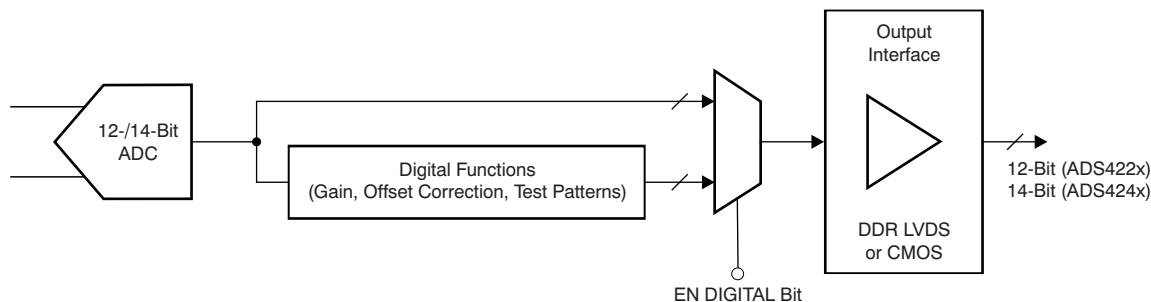


图 39. Digital Processing Block

#### 7.4.2 Gain For SFDR/SNR Trade-Off

The ADS4245 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0dB to 6dB (in 0.5dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in 表 5.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5dB and 1dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0dB.

**Device Functional Modes (接下页)**
**表 5. Full-Scale Range Across Gains**

GAIN (dB)	TYPE	FULL-SCALE ( $V_{PP}$ )
0	Default after reset	2
1	Fine, programmable	1.78
2	Fine, programmable	1.59
3	Fine, programmable	1.42
4	Fine, programmable	1.26
5	Fine, programmable	1.12
6	Fine, programmable	1

**7.4.3 Offset Correction**

The ADS4245 has an internal offset correction algorithm that estimates and corrects dc offset up to  $\pm 10\text{mV}$ . The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in 表 6.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

**表 6. Time Constant Of Offset Correction Algorithm**

OFFSET CORR TIME CONSTANT	TIME CONSTANT, $TC_{CLK}$ (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (ms) <sup>(1)</sup>
0000	1M	7
0001	2M	13
0010	4M	26
0011	8M	52
0100	16M	105
0101	32M	210
0110	64M	419
f0111	128M	839
1000	256M	1678
1001	512M	3355
1010	1G	6711
1011	2G	13422
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency,  $f_S = 160\text{MSPS}$ .

## 7.4.4 Power-Down

The ADS4245 has two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control terminals CTRL1 to CTRL3 (as shown in 表 7).

**表 7. Power-Down Settings**

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Default
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Global power-down
High	Low	High	Channel A powered down, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data is multiplexed and output on DB[10:0] terminals

### 7.4.4.1 Global Power-Down

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of approximately 20mW when the CTRL terminals are used and 3mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100 $\mu$ s.

### 7.4.4.2 Channel Standby

In this mode, each ADC channel can be powered down. The internal references are active, resulting in a quick wake-up time of 50 $\mu$ s. The total power dissipation in standby is approximately 200mW at 160MSPS.

### 7.4.4.3 Input Clock Stop

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1MSPS. The power dissipation is approximately 160mW.

## 7.4.5 Digital Output Information

The ADS4245 provides 14-bit digital data for each channel and an output clock synchronized with the data.

### 7.4.5.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN terminal in parallel configuration mode.

### 7.4.5.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in [图 40](#).

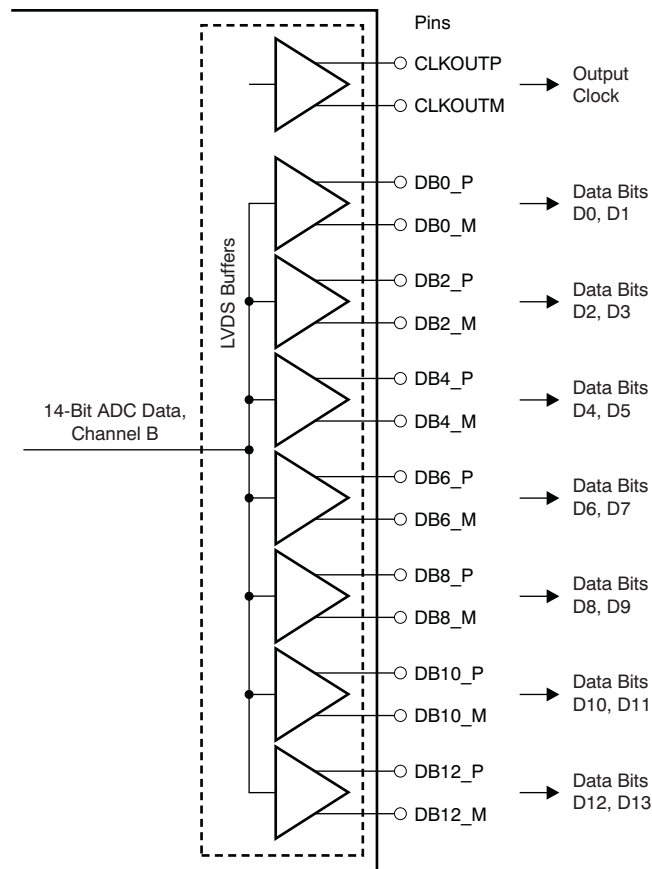
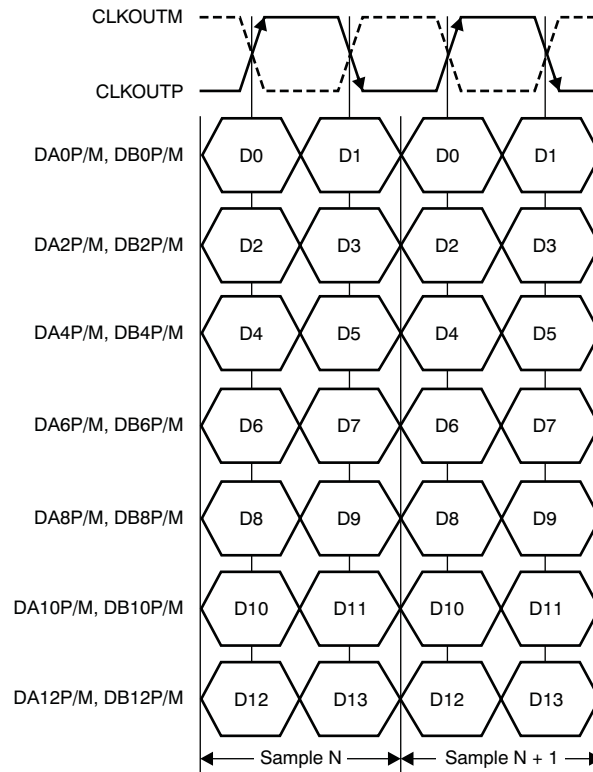


图 40. LVDS Interface

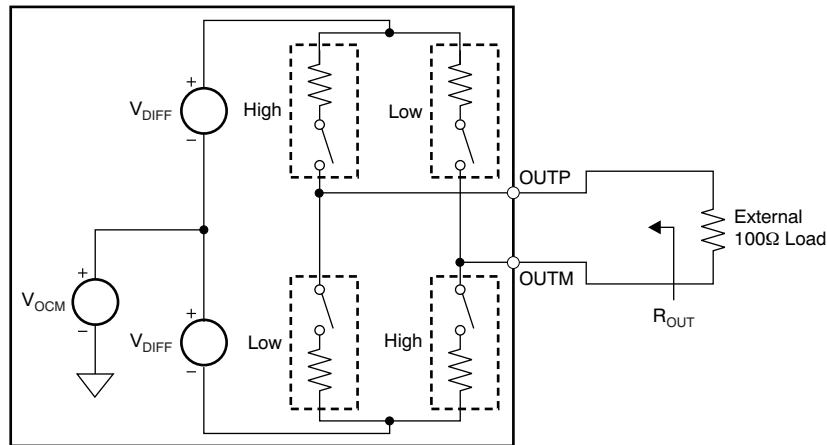
Even data bits (D0, D2, D4, etc.) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, etc.) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in 图 41.



**图 41. DDR LVDS Interface Timing**

### 7.4.5.3 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in [图 42](#). After reset, the buffer presents an output impedance of 100Ω to match with the external 100Ω termination.



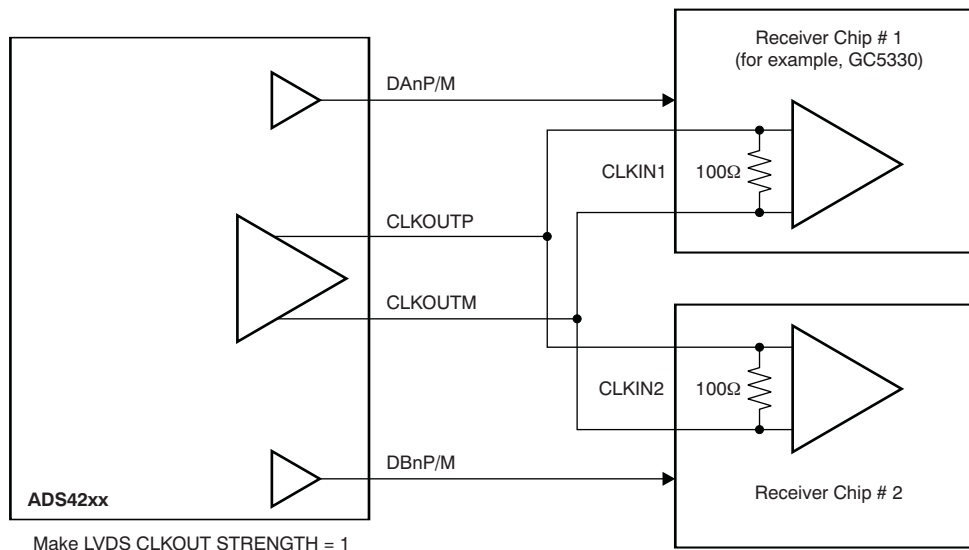
NOTE: Default swing across 100Ω load is ±350mV. Use the LVDS SWING bits to change the swing.

**图 42. LVDS Buffer Equivalent Circuit**

The  $V_{DIFF}$  voltage is nominally 350mV, resulting in an output swing of ±350mV with 100Ω external termination. The  $V_{DIFF}$  voltage is programmable using the LVDS SWING register bits from ±125mV to ±570mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50Ω differential termination, as shown in [图 43](#). This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.



**图 43. LVDS Buffer Differential Termination**

7.4.5.4 Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate terminals as CMOS voltage level, every clock cycle, as 图 44 shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. It is recommended to minimize the load capacitance of the data and clock output terminals by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

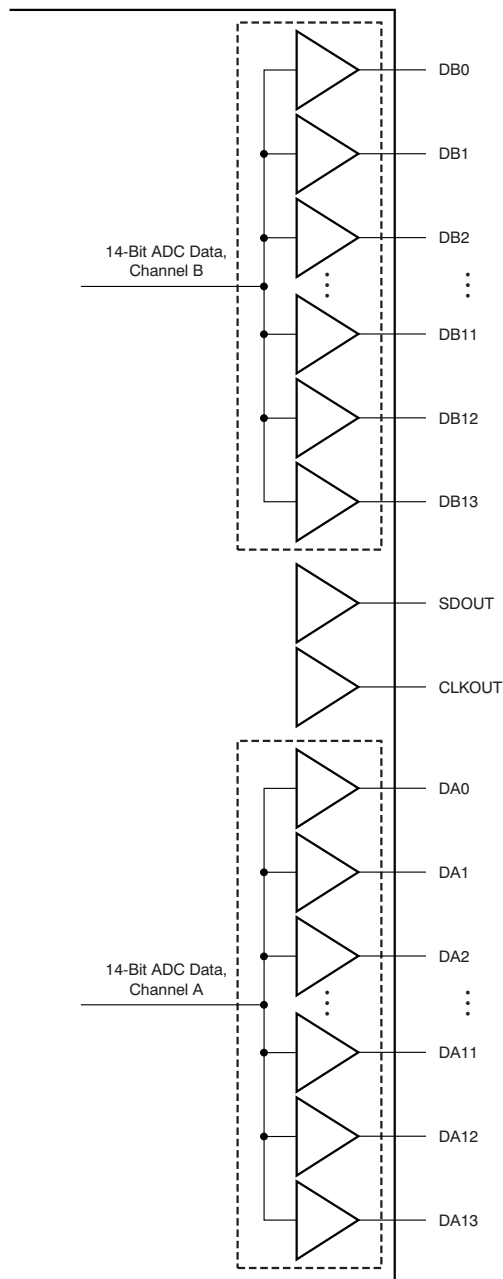


图 44. CMOS Outputs

### 7.4.5.5 CMOS Interface Power Dissipation

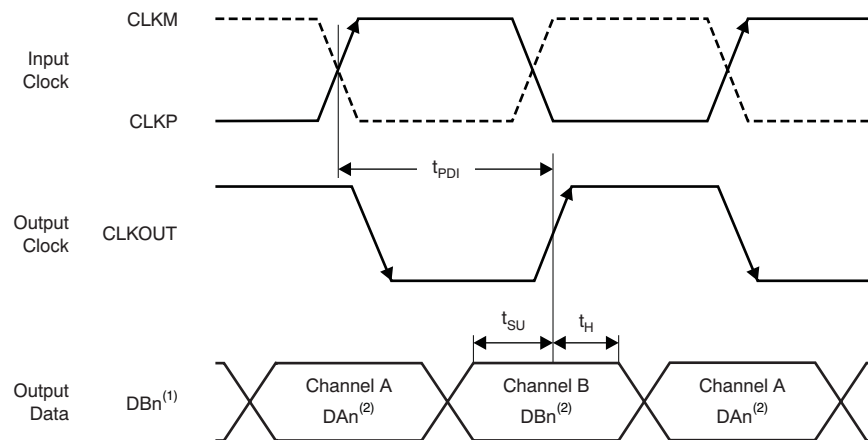
With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output terminal. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

$$\text{Digital current as a result of CMOS output switching} = C_L \times \text{DRVDD} \times (N \times F_{\text{AVG}}),$$

where  $C_L$  = load capacitance,  $N \times F_{\text{AVG}}$  = average number of output bits switching.

### 7.4.5.6 Multiplexed Mode Of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[13:0] terminals), as shown in [图 45](#). The channel A output terminals (DA[13:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 80MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel terminals.



- (1) In multiplexed mode, both channels outputs come on the channel B output terminals.
- (2) Dn = bits D0, D1, D2, etc.

**图 45. Multiplexed Mode Timing Diagram**

### 7.4.5.7 Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit or by controlling the DFS terminal in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is FFFh for the ADS422x and 3FFFh for the ADS424x in offset binary output format; the output code is 7FFh for the ADS422x and 1FFFh for the ADS424x in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 800h for the ADS422x and 2000h for the ADS424x in twos complement output format.

## 7.5 Device Configuration

The ADS4245 can be configured independently using either parallel interface control or serial interface programming.

### 7.5.1 Parallel Configuration Only

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 terminals to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel terminals to the correct voltage levels (as described in [表 8](#) to [表 11](#)). There is no need to apply a reset and SDATA can be connected to ground.

## Device Configuration (接下页)

In this mode, SEN and SCLK function as parallel interface control terminals. Some frequently-used functions can be controlled using these terminals. 表 8 describes the modes controlled by the parallel terminals.

**表 8. Parallel Terminal Definition**

TERMINAL	CONTROL MODE
SCLK	Low-speed mode selection
SEN	Output data format and output interface selection
CTRL1	Together, these terminals control the power-down modes
CTRL2	
CTRL3	

### 7.5.2 Serial Interface Configuration Only

To enable this mode, the serial registers must first be reset to the default values and the RESET terminal must be kept low. SEN, SDATA, and SCLK function as serial interface terminals in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET terminal or by setting the RESET bit high. The [Serial Register Map](#) section describes the register programming and the register reset process in more detail.

### 7.5.3 Using Both Serial Interface And Parallel Controls

For increased flexibility, a combination of serial interface registers and parallel terminal controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control terminals CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these terminals (see 表 11). SEN, SDATA, and SCLK function as serial interface digital terminals and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET terminal or by setting the RESET bit to '1'. After reset, the RESET terminal must be kept low. The [Serial Register Map](#) section describes register programming and the register reset process in more detail.

### 7.5.4 Parallel Configuration Details

The functions controlled by each parallel terminal are described in 表 9, 表 10, and 表 11. A simple way of configuring the parallel terminals is shown in 图 46.

**表 9. SCLK Control Terminal**

VOLTAGE APPLIED ON SCLK	DESCRIPTION
Low	Low-speed mode is disabled
High	Low-speed mode is enabled <sup>(1)</sup>

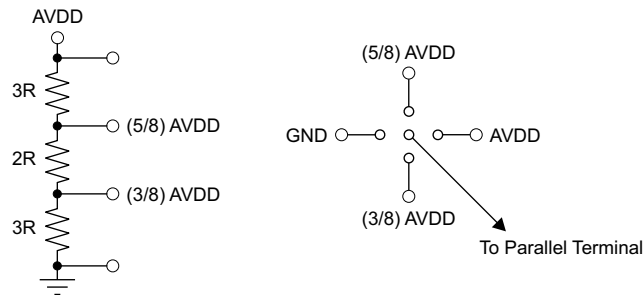
(1) Low-speed mode is enabled in the ADS4222/42 by default.

**表 10. SEN Control Terminal**

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (+50mV/0mV)	Twos complement and parallel CMOS output
(3/8) AVDD (±50mV)	Offset binary and parallel CMOS output
(5/8) 2AVDD (±50mV)	Offset binary and DDR LVDS output
AVDD (0mV/–50mV)	Twos complement and DDR LVDS output

**表 11. CTRL1, CTRL2, And CTRL3 Terminals**

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Global power-down
High	Low	High	Channel A standby, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data are multiplexed and output on the DB[13:0] terminals.


**图 46. Simple Scheme To Configure The Parallel Terminals**

### 7.5.5 Serial Interface Details

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) terminals. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

#### 7.5.5.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET terminal (of width greater than 10ns), as shown in 图 47; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET terminal is kept low.

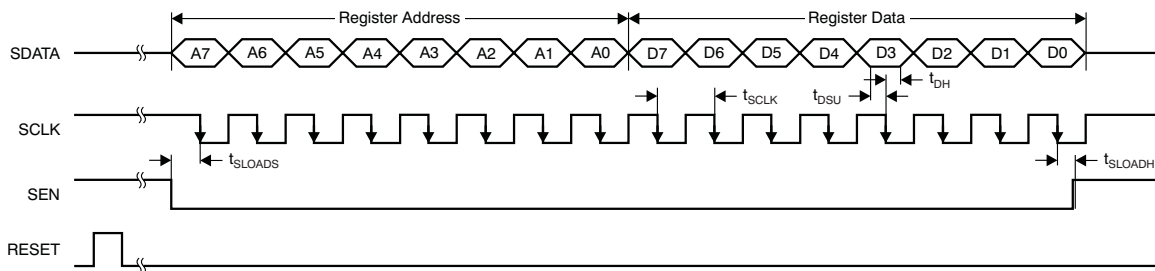


图 47. Serial Interface Timing

表 12. Serial Interface Timing Characteristics<sup>(1)</sup>

PARAMETER		MIN	TYP	MAX	UNIT
f <sub>SCLK</sub>	SCLK frequency (equal to 1/t <sub>SCLK</sub> )	> DC		20	MHz
t <sub>SLOADS</sub>	SEN to SCLK setup time	30			ns
t <sub>SLOADH</sub>	SCLK to SEN hold time	30			ns
t <sub>DSU</sub>	SDATA setup time	30			ns
t <sub>DH</sub>	SDATA hold time	30			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T<sub>MIN</sub> = -55°C to T<sub>MAX</sub> = +125°C, AVDD = 1.8V, and DRVDD = 1.8V, unless otherwise noted.

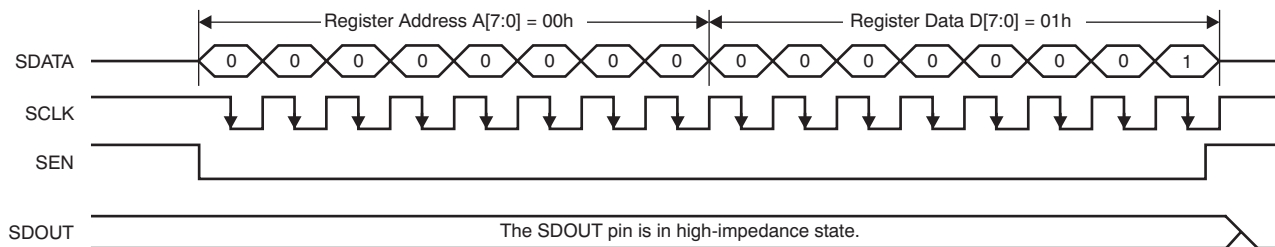
#### 7.5.5.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

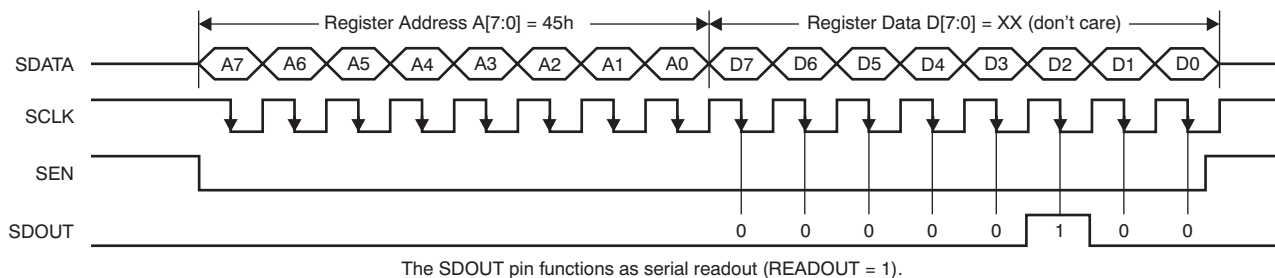
1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT terminal (terminal 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on terminal 64.

When READOUT is disabled, the SDOUT terminal is in high-impedance state. If serial readout is not used, the SDOUT terminal must float.



a) Enable serial readout (READOUT = 1)



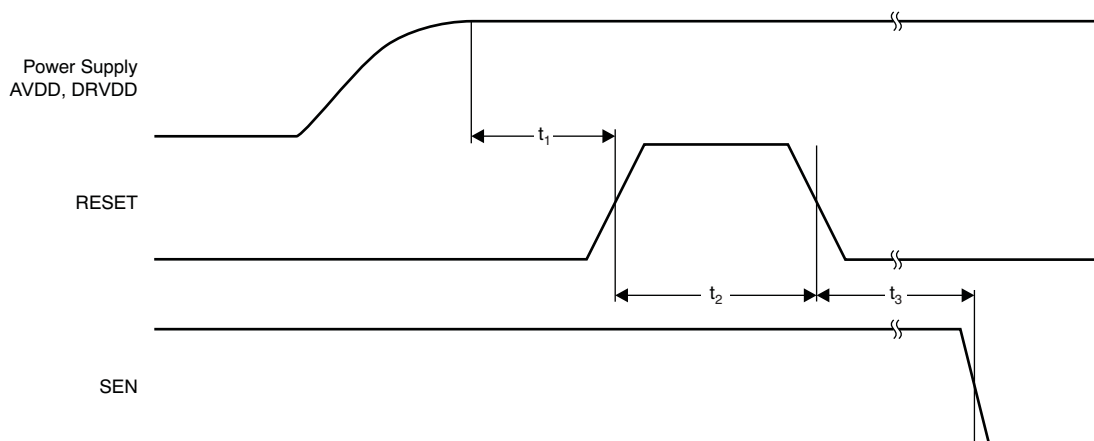
b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)

图 48. Serial Readout Timing Diagram

表 13. Reset Timing (Only When Serial Interface Is Used)<sup>(1)</sup>

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_1$	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
$t_2$	Reset pulse width	Active RESET signal pulse width	100			ns
					1	$\mu$ s
$t_3$	Register write delay	Delay from RESET disable to SEN active	350			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range:  $T_{MIN} = -55^\circ\text{C}$  to  $T_{MAX} = +125^\circ\text{C}$ , unless otherwise noted.



NOTE: A high pulse on the RESET terminal is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

图 49. Reset Timing Diagram

## 7.6 Serial Register Map

表 14 summarizes the functions supported by the serial interface.

表 14. Serial Interface Register Map<sup>(1)</sup>

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	RESET	READOUT
01	LVDS SWING						0	0
03	0	0	0	0	0	0	HIGH PERF MODE	
25	CH A GAIN				0	CH A TEST PATTERNS		
29	0	0	0	DATA FORMAT		0	0	0
2B	CH B GAIN				0	CH B TEST PATTERNS		
3D	0	0	ENABLE OFFSET CORR	0	0	0	0	0
3F	0	0	CUSTOM PATTERN D[13:8]					
40	CUSTOM PATTERN D[7:0]							
41	LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	
42	CLKOUT FALL POSN		CLKOUT RISE POSN		EN DIGITAL	0	0	0
45	STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0
4A	0	0	0	0	0	0	0	HIGH FREQ MODE CH B <sup>(2)</sup>
58	0	0	0	0	0	0	0	HIGH FREQ MODE CH A <sup>(2)</sup>
BF	CH A OFFSET PEDESTAL						0	0
C1	CH B OFFSET PEDESTAL						0	0
CF	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DB	0	0	0	0	0	0	0	LOW SPEED MODE CH B
EF	0	0	0	EN LOW SPEED MODE	0	0	0	0
F1	0	0	0	0	0	0	EN LVDS SWING	
F2	0	0	0	0	LOW SPEED MODE CH A	0	0	0

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to '0' after reset.

(2) These bits improve SFDR on high frequencies. The frequency limit is 200MHz.

## 7.7 Description Of Serial Registers

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

**Bits[7:2] Always write '0'**

**Bit 1 RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

**Bit 0 READOUT: Serial readout**

This bit sets the serial readout of the registers.

0 = Serial readout of registers disabled; the SDOOUT terminal is placed in high-impedance state.

1 = Serial readout enabled; the SDOOUT terminal functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the [Serial Register Readout](#) section.

7	6	5	4	3	2	1	0
LVDS SWING						0	0

**Bits[7:2] LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to '1' before programming swing.

000000 = Default LVDS swing;  $\pm 350\text{mV}$  with external  $100\Omega$  termination

011011 = LVDS swing increases to  $\pm 410\text{mV}$

110010 = LVDS swing increases to  $\pm 465\text{mV}$

010100 = LVDS swing increases to  $\pm 570\text{mV}$

111110 = LVDS swing decreases to  $\pm 200\text{mV}$

001111 = LVDS swing decreases to  $\pm 125\text{mV}$

**Bits[1:0] Always write '0'**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH PERF MODE	

**Bits[7:2] Always write '0'**

**Bits[1:0] HIGH PERF MODE: High-performance mode**

00 = Default performance

01 = Do not use

10 = Do not use

11 = Obtain best performance across sample clock and input signal frequencies

7	6	5	4	3	2	1	0
CH A GAIN				0	CH A TEST PATTERNS		

**Bits[7:4] CH A GAIN: Channel A gain programmability**

These bits set the gain programmability in 0.5dB steps for channel A.

0000 = 0dB gain (default after reset)

0001 = 0.5dB gain

0010 = 1dB gain

0011 = 1.5dB gain

0100 = 2dB gain

0101 = 2.5dB gain

0110 = 3dB gain

0111 = 3.5dB gain

1000 = 4dB gain

1001 = 4.5dB gain

1010 = 5dB gain

1011 = 5.5dB gain

1100 = 6dB gain

**Bit 3 Always write '0'**
**Bits[2:0] CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern.

Output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.

100 = Outputs digital ramp.

Output data increment by one LSB (14-bit) every clock cycle from code 0 to code 16383.

101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern

110 = Unused

111 = Unused

7	6	5	4	3	2	1	0
0	0	0	DATA FORMAT		0	0	0

**Bits[7:5] Always write '0'**
**Bits[4:3] DATA FORMAT: Data format selection**

00 = Twos complement

01 = Twos complement

10 = Twos complement

11 = Offset binary

**Bits[2:0] Always write '0'**

7	6	5	4	3	2	1	0
CH B GAIN				0	CH B TEST PATTERNS		

**Bits[7:4] CH B GAIN: Channel B gain programmability**

These bits set the gain programmability in 0.5dB steps for channel B.

0000 = 0dB gain (default after reset)  
 0001 = 0.5dB gain  
 0010 = 1dB gain  
 0011 = 1.5dB gain  
 0100 = 2dB gain  
 0101 = 2.5dB gain  
 0110 = 3dB gain  
 0111 = 3.5dB gain  
 1000 = 4dB gain  
 1001 = 4.5dB gain  
 1010 = 5dB gain  
 1011 = 5.5dB gain  
 1100 = 6dB gain

**Bit 3 Always write '0'**
**Bits[2:0] CH B TEST PATTERNS: Channel B data capture**

These bits verify data capture for channel B.

000 = Normal operation  
 001 = Outputs all 0s  
 010 = Outputs all 1s  
 011 = Outputs toggle pattern.  
 Output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.  
 100 = Outputs digital ramp.  
 Output data increment by one LSB (14-bit) every clock cycle from code 0 to code 16383.  
 101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern  
 110 = Unused  
 111 = Unused

7	6	5	4	3	2	1	0
0	0	ENABLE OFFSET CORR	0	0	0	0	0

**Bits[7:6] Always write '0'**
**Bit 5 ENABLE OFFSET CORR: Offset correction setting**

This bit enables the offset correction.

0 = Offset correction disabled  
 1 = Offset correction enabled

**Bits[4:0] Always write '0'**

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

**Bits[7:6] Always write '0'**
**Bits[5:0] CUSTOM PATTERN D[13:8]**

These are the six upper bits of the custom pattern available at the output instead of ADC data.

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

**Bits[7:0] CUSTOM PATTERN D[7:0]**

These are the eight upper bits of the custom pattern available at the output instead of ADC data.

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	

**Bits[7:6] LVDS CMOS: Interface selection**

These bits select the interface.

00 = DDR LVDS interface

01 = DDR LVDS interface

10 = DDR LVDS interface

11 = Parallel CMOS interface

**Bits[5:4] CMOS CLKOUT STRENGTH**

These bits control the strength of the CMOS output clock.

00 = Maximum strength (recommended)

01 = Medium strength

10 = Low strength

11 = Very low strength

**Bits[3:2] Always write '0'**
**Bits[1:0] DIS OBUF**

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.

00 = Default

01 = Power-down data output buffers for channel B

10 = Power-down data output buffers for channel A

11 = Power-down data output buffers for both channels as well as the clock output buffer

7	6	5	4	3	2	1	0
CLKOUT FALL POSN		CLKOUT RISE POSN		EN DIGITAL	0	0	0

**Bits[7:6] CLKOUT FALL POSN**

In LVDS mode:

00 = Default

01 = The falling edge of the output clock advances by 450 ps

10 = The falling edge of the output clock advances by 150 ps

11 = The falling edge of the output clock is delayed by 550 ps

In CMOS mode:

00 = Default

01 = The falling edge of the output clock is delayed by 150 ps

10 = Do not use

11 = The falling edge of the output clock advances by 100 ps

**Bits[5:6] CLKOUT RISE POSN**

In LVDS mode:

00 = Default

01 = The rising edge of the output clock advances by 450 ps

10 = The rising edge of the output clock advances by 150 ps

11 = The rising edge of the output clock is delayed by 250 ps

In CMOS mode:

00 = Default

01 = The rising edge of the output clock is delayed by 150 ps

10 = Do not use

11 = The rising edge of the output clock advances by 100 ps

**Bit 3 EN DIGITAL: Digital function enable**

0 = All digital functions disabled

1 = All digital functions (such as test patterns, gain, and offset correction) enabled

**Bits[2:0] Always write '0'**

7	6	5	4	3	2	1	0
STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0

**Bit 7 STBY: Standby setting**

0 = Normal operation

1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50µs).

**Bit 6 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100Ω external termination

1 = LVDS output clock buffer has double strength to be used with 50Ω external termination

**Bit 5 LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100Ω external termination

1 = All LVDS data buffers have double strength to be used with 50Ω external termination

**Bits[4:3] Always write '0'**

**Bit 2 PDN GLOBAL**

0 = Normal operation

1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100µs).

**Bits[1:0] Always write '0'**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH B

**Bits[7:1] Always write '0'**

**Bit 0 HIGH FREQ MODE CH B: High-frequency mode for channel B**

0 = Default

1 = Use this mode for high input frequencies

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH A

**Bits[7:1] Always write '0'**
**Bit 0 HIGH FREQ MODE CH A: High-frequency mode for channel A**

0 = Default

1 = Use this mode for high input frequencies

7	6	5	4	3	2	1	0
CH A OFFSET PEDESTAL						0	0

**Bits[7:2] CH A OFFSET PEDESTAL: Channel A offset pedestal selection**

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the [Offset Correction](#) section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+32 by adding pedestal D7-D2.

**ADS4245 (Program Bits D[7:2])**

011111 = Midcode+31

011110 = Midcode+30

011101 = Midcode+29

...

000000 = Midcode

111111 = Midcode-1

111110 = Midcode-2

111101 = Midcode-3

...

100000 = Midcode-32

**Bits[1:0] Always write '0'**

7	6	5	4	3	2	1	0
CH B OFFSET PEDESTAL						0	0

**Bits[7:2] CH B OFFSET PEDESTAL: Channel B offset pedestal selection**

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the [Offset Correction](#) section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+32 by adding pedestal D[7:2].

**ADS424x (Program Bits D[7:2])**

011111 = Midcode+31

011110 = Midcode+30

011101 = Midcode+29

...

000000 = Midcode

111111 = Midcode-1

111110 = Midcode-2

111101 = Midcode-3

...

100000 = Midcode-32

**Bits[1:0] Always write '0'**

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

**Bit 7 FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.

0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)

1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the [Offset Correction](#) section.

**Bit 6 Always write '0'**
**Bits[5:2] OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the [Offset Correction](#) section.

**Bits[1:0] Always write '0'**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LOW SPEED MODE CH B

**Bits[7:1] Always write '0'**
**Bit 0 LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.

0 = Low-speed mode is disabled for channel B

1 = Low-speed mode is enabled for channel B

7	6	5	4	3	2	1	0
0	0	0	EN LOW SPEED MODE	0	0	0	0

**Bits[7:5] Always write '0'**
**Bit 4 EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits (ADS42x5 and ADS42x6 only)**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.

0 = Low-speed mode is disabled

1 = Low-speed mode is controlled by serial register bits

**Bits[3:0] Always write '0'**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN LVDS SWING	

**Bits[7:2] Always write '0'**
**Bits[1:0] EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.

00 = LVDS swing control using the LVDS SWING register bits is disabled

01 = Do not use

10 = Do not use

11 = LVDS swing control using the LVDS SWING register bits is enabled

7	6	5	4	3	2	1	0
0	0	0	0	LOW SPEED MODE CH A	0	0	0

**Bits[7:4] Always write '0'**

**Bit 3 LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.

0 = Low-speed mode is disabled for channel A

1 = Low-speed mode is enabled for channel A

**Bits[2:0] Always write '0'**

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The ADS4245 belongs to TI's ultralow-power family of dual-channel 14-bit analog-to-digital converters (ADCs). At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled/held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and digitally processed to create the final code after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format. The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to approximately 400MHz (with 2V<sub>PP</sub> amplitude) or approximately 600MHz (with 1V<sub>PP</sub> amplitude).

#### 8.1.1 Clock Input

The ADS4245 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in 图 50, 图 51 and 图 52. The internal clock buffer is shown in 图 53.

(1) R<sub>T</sub> = termination resistor, if necessary.

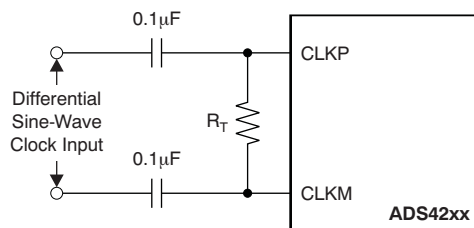


图 50. Differential Sine-Wave Clock Driving Circuit

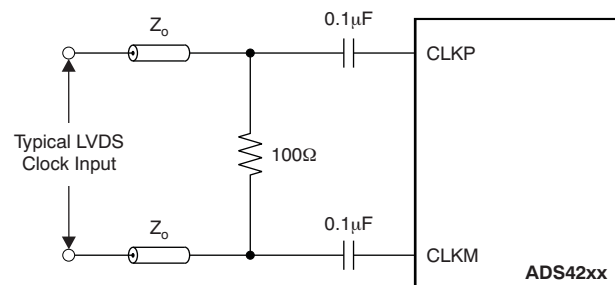


图 51. LVDS Clock Driving Circuit

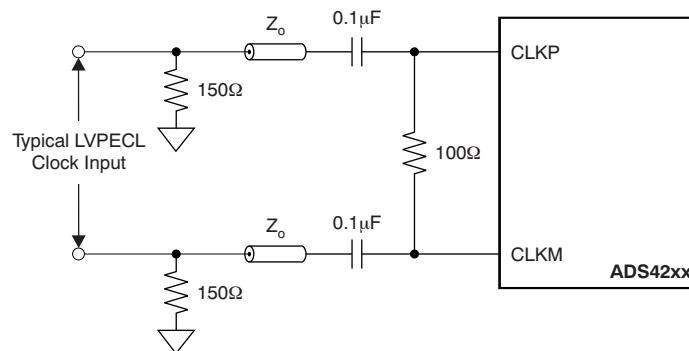
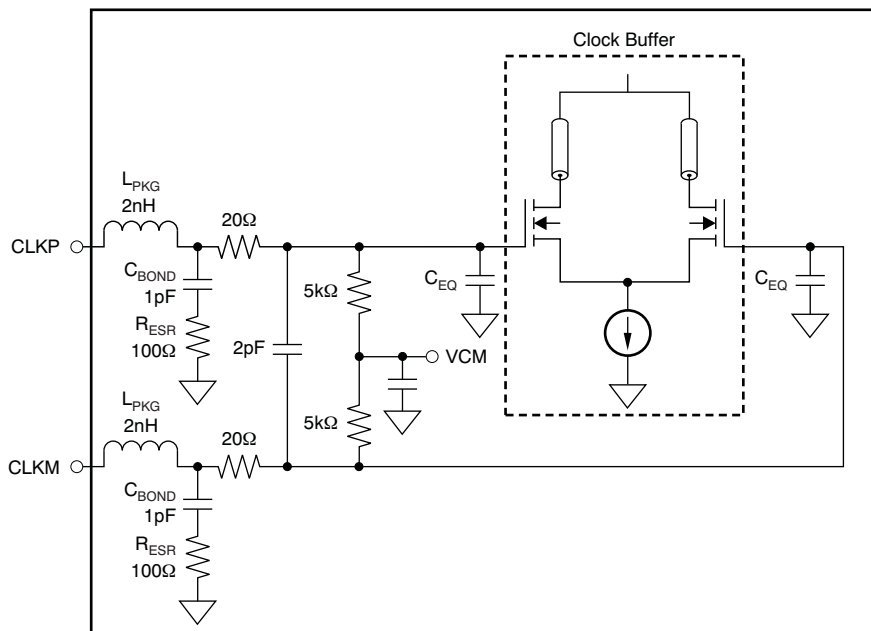


图 52. LVPECL Clock Driving Circuit

Application Information (接下页)



NOTE:  $C_{EQ}$  is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

图 53. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1μF capacitor, as shown in 图 54. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

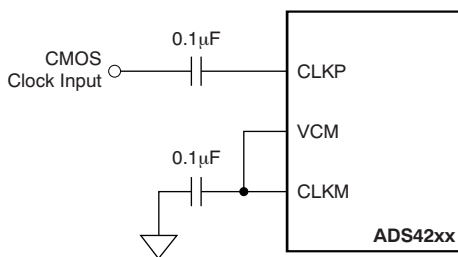
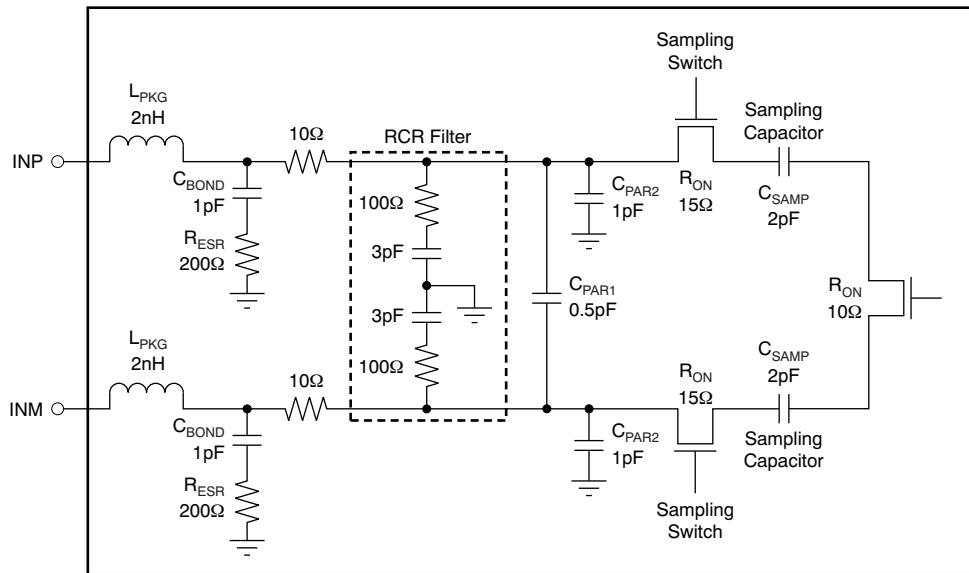


图 54. Single-Ended Clock Driving Circuit

8.2 Typical Applications

8.2.1 Analog Input

The analog input consists of a switched-capacitor based, differential sample-and-hold (S/H) architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM terminals must be externally biased around a common-mode voltage of 0.95V, available on the VCM terminal. For a full-scale differential input, each input terminal (INP and INM) must swing symmetrically between  $V_{CM} + 0.5V$  and  $V_{CM} - 0.5V$ , resulting in a  $2V_{PP}$  differential input swing. The input sampling circuit has a high 3dB bandwidth that extends up to 550MHz (measured from the input terminals to the sampled voltage). 图 55 shows an equivalent circuit for the analog input.

**Typical Applications (接下页)**

**图 55. Analog Input Equivalent Circuit**
**8.2.1.1 Design Requirements for Drive Circuits**

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A 5Ω to 15Ω resistor in series with each input terminal is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches; nonlinearity of the sampling circuit; and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200MHz). It is also necessary to present low impedance (less than 50Ω) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches now must be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

In the ADS4245, the R-C component values have been optimized while supporting high input bandwidth (up to 550MHz). However, in applications with input frequencies up to 200MHz to 300MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see [图 56](#) and [图 57](#).

## Typical Applications (接下页)

### 8.2.1.2 Detailed Design Procedure

Two example driving circuit configurations are shown in 图 56 and 图 57—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. Note that both of the drive circuits have been terminated by  $50\Omega$  near the ADC side. The termination is accomplished by a  $25\Omega$  resistor from each input to the  $1.5V$  common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in 图 56, 图 57, and 图 58. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective  $50\Omega$  (in the case of  $50\Omega$  source impedance).

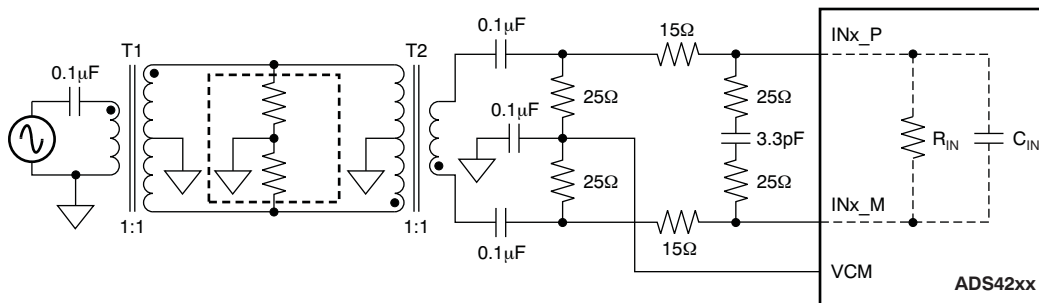


图 56. Drive Circuit With Low Bandwidth (For Low Input Frequencies Less Than 150MHz)

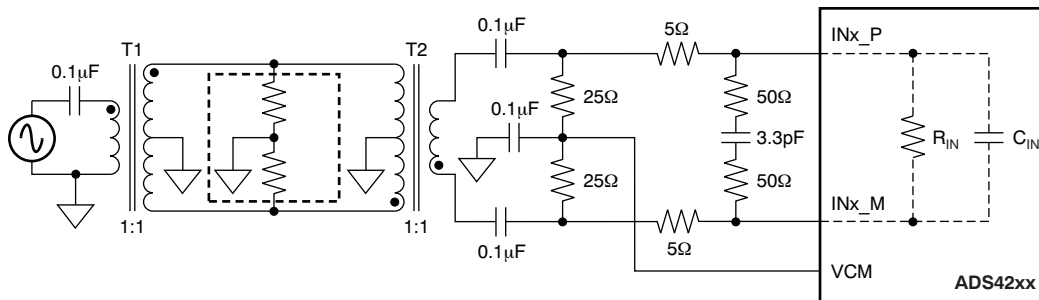


图 57. Drive Circuit With High Bandwidth (For High Input Frequencies Greater Than 150MHz And Less Than 270MHz)

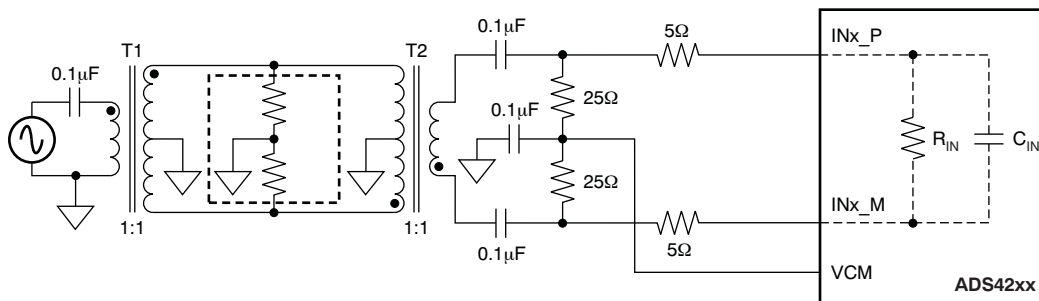


图 58. Drive Circuit With Very High Bandwidth (Greater Than 270MHz)

### Typical Applications (接下页)

All of these examples show 1:1 transformers being used with a 50Ω source. As explained in the [Drive Circuit Requirements](#) section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a band-pass or low-pass filter is required to obtain the desired dynamic performance, as shown in [图 59](#). Such filters present low source impedance at the high frequencies corresponding to the sampling glitch and help avoid the performance loss with the high source impedance.

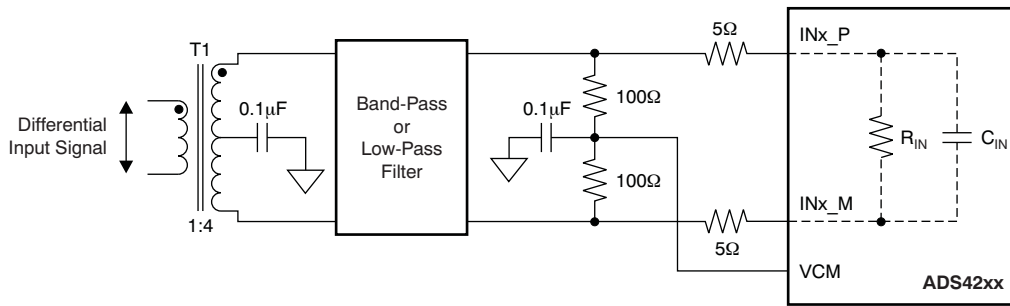
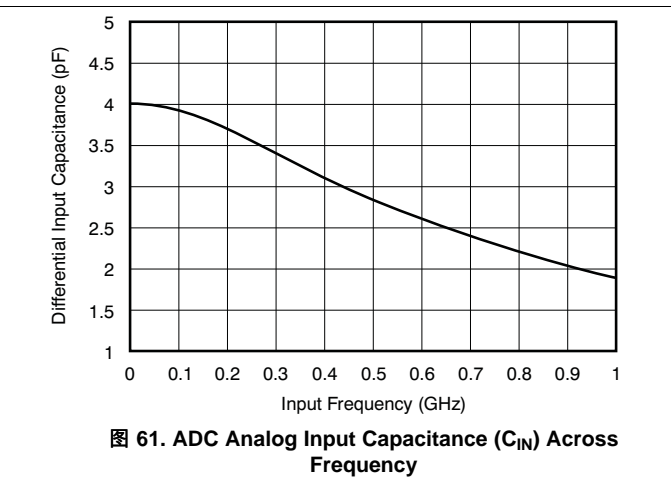
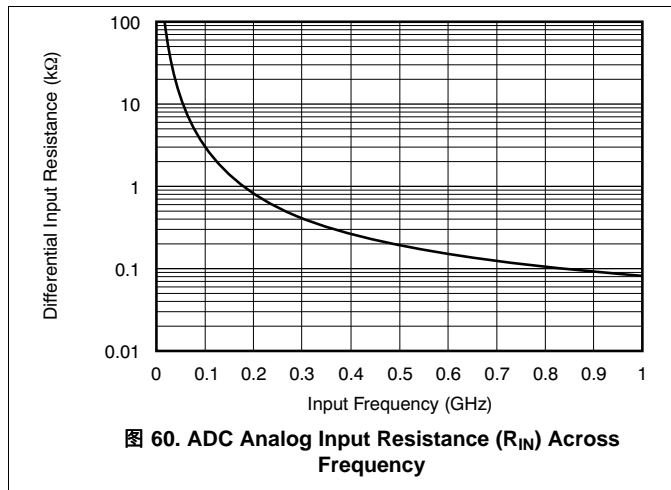


图 59. Drive Circuit With A 1:4 Transformer

#### 8.2.1.3 Application Curves

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. [图 60](#) and [图 61](#) show the impedance ( $Z_{IN} = R_{IN} \parallel C_{IN}$ ) looking into the ADC input terminals.



## 9 Power Supply Recommendations

The recommended analog/digital power supply range for ADS4245 is 1.7V to 1.9V.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the [ADS4226 Evaluation Module \(SLAU333\)](#) for details on layout and grounding.

#### 10.1.2 Supply Decoupling

Because the ADS4245 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply terminals.

#### 10.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes [QFN Layout Guidelines \(SLOA122\)](#) and [QFN/SON PCB Attachment \(SLUA271\)](#).

#### 10.1.4 Routing Analog Inputs

It is advisable to route differential analog input pairs (INP\_x and INM\_x) close to each other. To minimize the possibility of coupling from a channel analog input to the sampling clock, the analog input pairs of both channels should be routed perpendicular to the sampling clock. See the [ADS4226 Evaluation Module \(SLAU333\)](#) for reference routing.

## 10.2 Layout Example

Figure 62 shows a snapshot of the PCB layout from the ADS424x EVM.

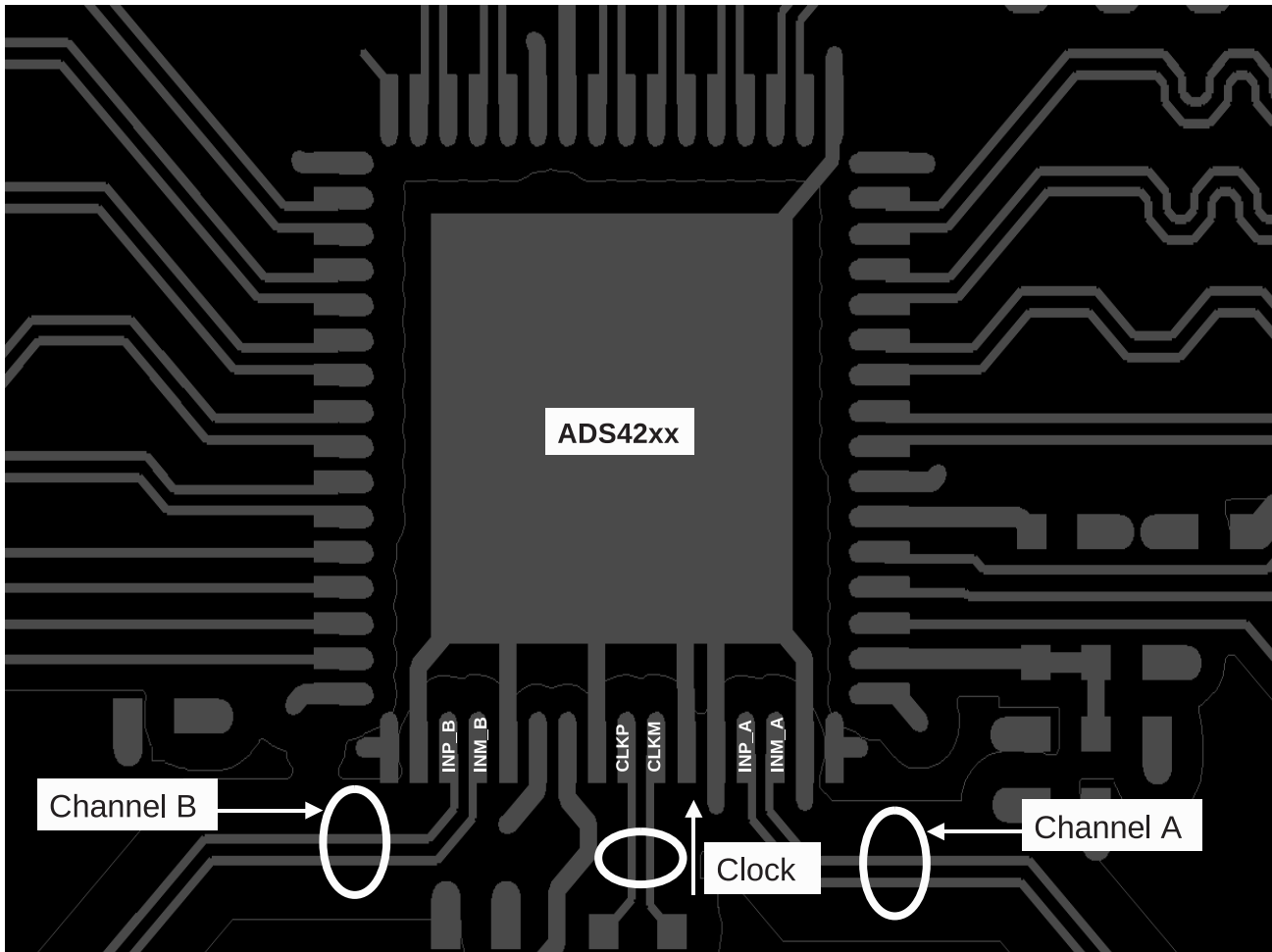


Figure 62. ADS42XX EVM PCB Layout

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 器件支持

##### 11.1.1.1 规格定义

**模拟带宽** – 基频功率相对低频值下降 3dB 时的模拟输入频率。

**孔径延迟** – 从输入采样时钟的上升沿到实际发生采样之间的延迟时间。该延迟在各通道中会有所不同。最大差值被定义为孔径延迟差异（通道间）。

**孔径不确定性（抖动）** – 采样间的孔径延迟差异。

**时钟脉冲宽度/占空比** – 时钟信号的占空比为时钟信号保持逻辑高电平的时间（时钟脉冲宽度）与时钟信号周期的比值。占空比通常以百分比的形式表示。理想差分正弦波时钟的占空比为 50%。

**最大转换速率** – 执行指定操作时所采用的最大采样率。除非另外注明，否则所有参数测试均以该采样率执行。

**最小转换速率** – ADC 正常工作时的最小采样率。

**微分非线性 (DNL)** – 理想 ADC 对模拟输入值进行编码转换时以 1 LSB 为步长。DNL 是指任意单个步长与这一理想值之间的偏差（以 LSB 为计量单位）。

**积分非线性 (INL)** – INL 是 ADC 传递函数与其最小二乘法曲线拟合所确定的最佳拟合曲线的偏差（以 LSB 为计量单位）。

**增益误差** – 增益误差是指 ADC 实际输入满量程范围与其理想值的偏差。增益误差以理想输入满量程范围的百分比形式表示。增益误差包括两部分：基准不精确所导致的误差 ( $E_{GREF}$ ) 和通道所导致的误差 ( $E_{GCHAN}$ )。这两种误差分别定义为  $E_{GREF}$  和  $E_{GCHAN}$ 。

对于一阶近似，总增益误差  $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$ 。

例如，如果  $E_{TOTAL} = \pm 0.5\%$ ，则满量程输入范围为  $(1 - 0.5 / 100) \times FS_{ideal}$  至  $(1 + 0.5 / 100) \times FS_{ideal}$ 。

**偏移误差** – 偏移误差是指 ADC 实际平均空闲通道输出编码与理想平均空闲通道输出编码之间的差值（以 LSB 数表示）。该数量通常转换为毫伏。

**温度漂移** – 温度漂移系数（相对于增益误差和偏移误差）指定参数从  $T_{MIN}$  到  $T_{MAX}$  每摄氏度的变化量。温度漂移的计算方法是用参数在  $T_{MIN}$  至  $T_{MAX}$  范围内的最大变化量除以  $T_{MAX} - T_{MIN}$  的值。

**信噪比** – SNR 是指基频功率 ( $P_S$ ) 与噪底功率 ( $P_N$ ) 的比值，不包括直流功率和前 9 个谐波的功率。

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (1)$$

当基频的绝对功率用作基准时，SNR 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SNR 以 dBFS（相对于满量程的分贝数）为单位。

**信噪比和失真 (SINAD)** – SINAD 是指基频功率 ( $P_S$ ) 与所有其他频谱成分（包括噪声 ( $P_N$ ) 和失真 ( $P_D$ )，但不包括直流）功率的比值。

$$SINAD = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (2)$$

当基频的绝对功率用作基准时，SINAD 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SINAD 以 dBFS（相对于满量程的分贝数）为单位。

**有效位数 (ENOB)** – ENOB 测量的是转换器相对于理论限值（基于量化噪声）的性能。

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

**总谐波失真 (THD)** – THD 是指基频功率 ( $P_S$ ) 与前 9 个谐波功率 ( $P_D$ ) 的比值。

**器件支持 (接下页)**

$$\text{THD} = 10 \log^{10} \frac{P_S}{P_N} \quad (4)$$

THD 通常以 dBc 为单位（相对于载波的分贝数）。

**无杂散动态范围 (SFDR)** – 基频功率与最高的其他频谱成分（毛刺或谐波）功率的比值。SFDR 通常以 dBc 为单位（相对于载波的分贝数）。

**双频互调失真 – IMD3** 是指基频功率（ $f_1$  和  $f_2$  频率处）与最差频谱成分（ $2f_1 - f_2$  或  $2f_2 - f_1$  频率处）功率的比值。当基频的绝对功率用作基准时，IMD3 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，IMD3 以 dBFS（相对于满量程的分贝数）为单位。

**直流电源抑制比 (DC PSRR)** – DC PSRR 是偏移误差变化量与模拟电源电压变化量的比值。DC PSRR 通常以 mV/V 为单位进行表示。

**交流电源抑制比 (AC PSRR)** – AC PSRR 测量的是 ADC 对电源电压变化的抑制能力。如果  $\Delta V_{\text{SUP}}$  表示电源电压的变化， $\Delta V_{\text{OUT}}$  表示 ADC 输出编码的相应变化（相对输入而言），则：

$$\text{PSRR} = 20 \log^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{SUP}}} \quad (\text{Expressed in dBc}) \quad (5)$$

**电压过载恢复** – 使过载的模拟输入端的误差恢复至 1% 以下所需的时钟数。该技术参数的测试方法是分别施加具有 6dB 正过载和负过载的正弦波信号。然后记录下过载后前几个采样（相对于期望值）的偏差。

**共模抑制比 (CMRR)** – CMRR 测量的是 ADC 对模拟输入共模变化的抑制能力。如果  $\Delta V_{\text{CM\_IN}}$  为输入端共模电压变化值， $\Delta V_{\text{OUT}}$  为相应的 ADC 输出代码变化值（以输入为基准），则：

$$\text{CMRR} = 20 \log^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{CM}}} \quad (\text{Expressed in dBc}) \quad (6)$$

**串扰 (仅限多通道 ADC)** – 串扰测量的是目标通道与其相邻通道之间的内部信号耦合。串扰分两种情况：一种是与紧邻通道（近端通道）之间的耦合，另一种是与跨封装通道（远端通道）之间的耦合。通常采用对邻近通道施加满量程信号的方式来测量串扰。串扰是指耦合信号功率（在目标通道的输出端测得）与邻近通道输入端所施加信号功率的比值。串扰通常以 dBc 为单位进行表示。

## 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 **通知我** 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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## 11.4 商标

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## 11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.6 术语表

**SLYZ022** — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS4245MRGC25EP	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	AZ4245EP	<a href="#">Samples</a>
V62/14609-01XE	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	AZ4245EP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS4245MRGC25EP	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS4245MRGC25EP	VQFN	RGC	64	250	213.0	191.0	55.0

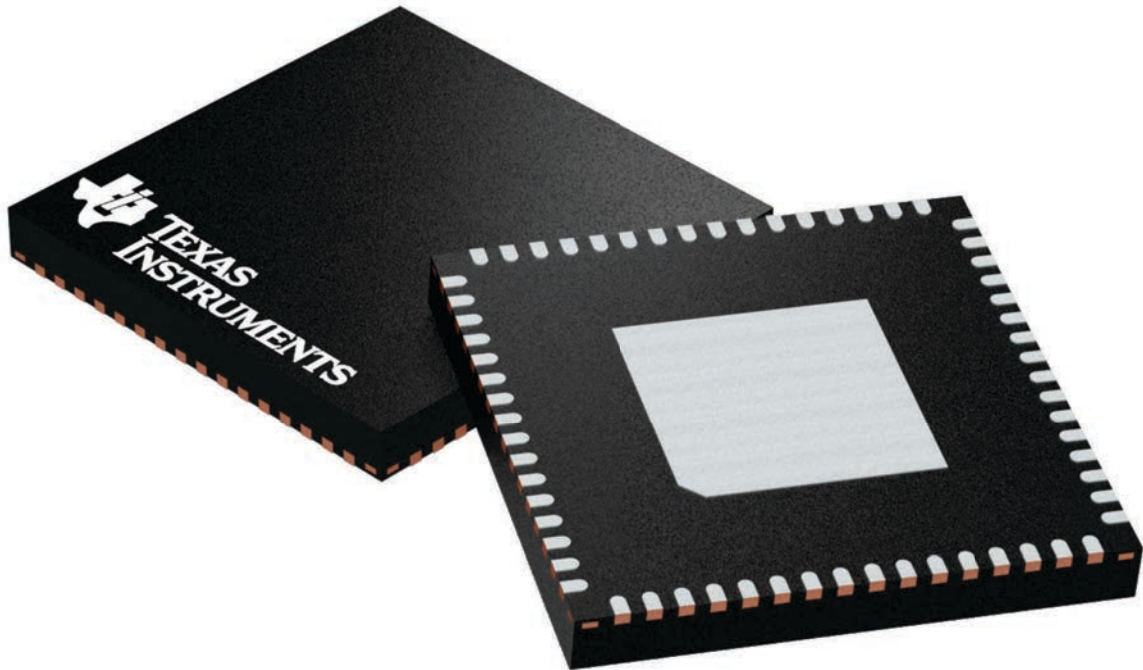
## GENERIC PACKAGE VIEW

**RGC 64**

**VQFN - 1 mm max height**

9 x 9, 0.5 mm pitch

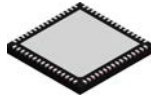
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224597/A

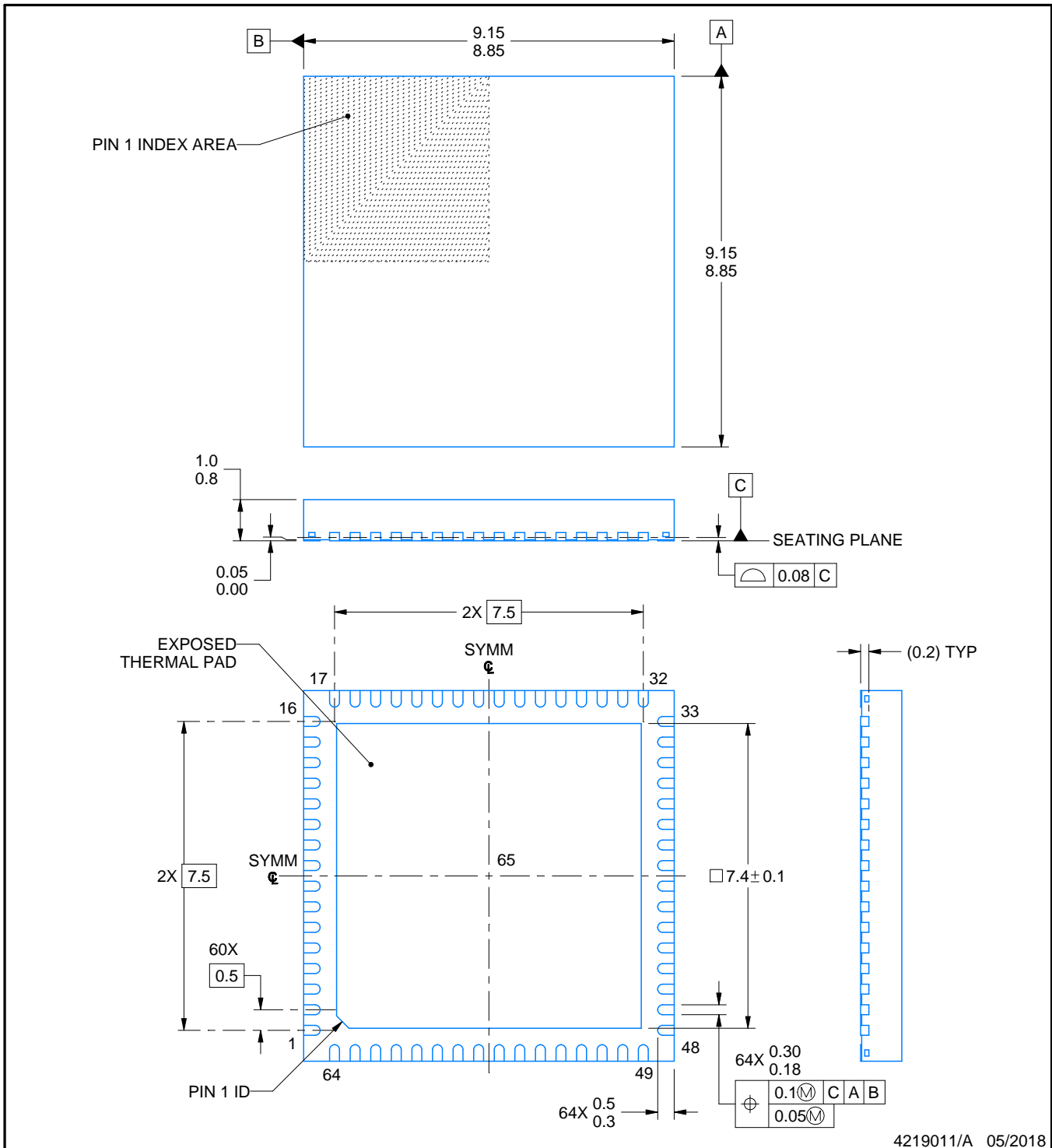
# RGC0064H



## PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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### NOTES:

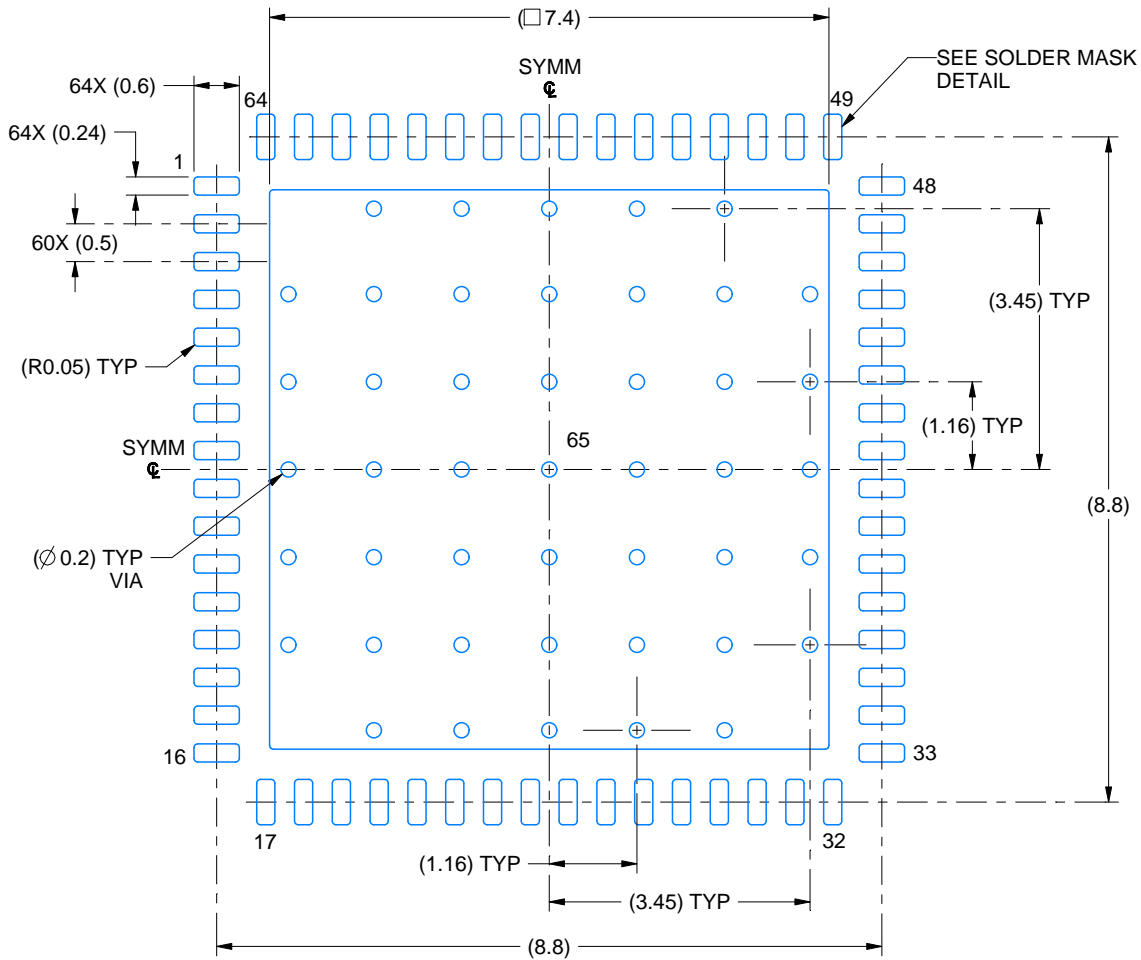
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

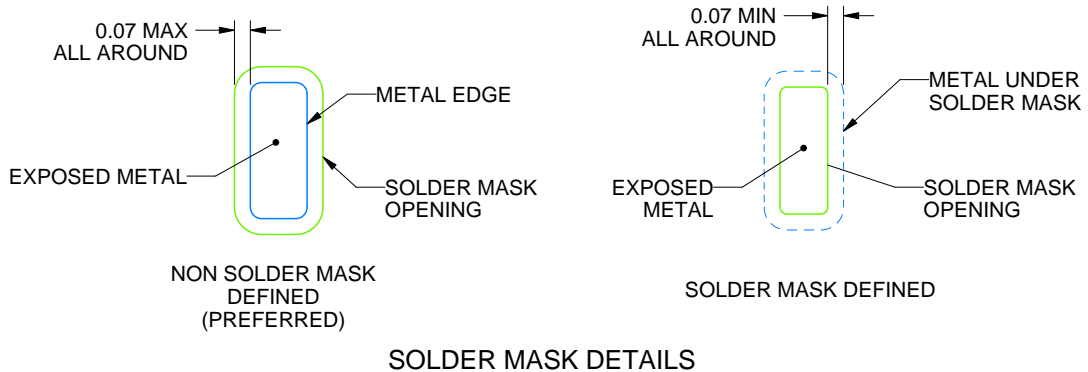
RGC0064H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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