12/10/8-Bit, 2MSPS, Dual-Channel, Unipolar, Pseudo-Differential, Ultralow-Power SAR Analog-to-Digital Converters

Check for Samples: ADS7947 , ADS7948, ADS7949

FEATURES

- **Sample Rate: 2MSPS**
- **Pin-Compatible Family: 12/10/8-Bit**
- **Outstanding Performance:**
  - **No Missing Codes**
  - **INL: 1LSB (max)**
  - **SNR: 72dB (min)**
- **Low Power:**
  - **7.5mW at 2MSPS Operation**
  - **Auto Power-Down at Lower Speeds:**
    - **3.8mW at 500kSPS**
    - **0.8mW at 100kSPS**
    - **0.16mW at 20kSPS**
- **Wide Supply Range:**
  - **Analog: 2.7V to 5.5V**
  - **Digital: 1.65V to AVDD**
- **Simple Serial Interface (SPI)**
- **Fully Specified from –40°C to +125°C**
- **Tiny Footprint: 3mm × 3mm QFN**

APPLICATIONS

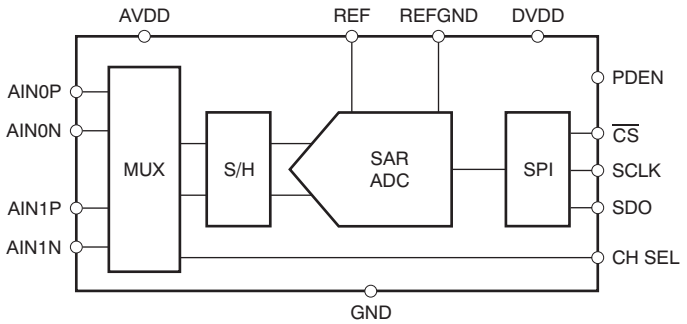
- **Communication Systems**
- **Optical Networking**
- **Medical Instrumentation**
- **Battery-Powered Equipment**
- **Data Acquisition Systems**

DESCRIPTION

The ADS7947/8/9 are 12-bit, 10-bit, and 8-bit 2MSPS analog-to-digital converters (ADCs), respectively. Devices operate at 2MSPS sample rate with a standard 16 clock data frame. In addition, it is possible to operate the ADS7947 (12-bit) at 2.1MSPS, the ADS7948 (10-bit) at 2.57MSPS, and the ADS7949 (8-bit) at 3MSPS with a short data frame optimized for the number of clocks sufficient for conversion with no drop in performance. The devices feature both outstanding dc precision and excellent dynamic performance, this family of pin-compatible devices includes a two-channel input multiplexer and a low-power successive approximation register (SAR) ADC with an inherent sample-and-hold (S/H) input stage.

The ADS7947/8/9 support a wide analog supply range that allows the full-scale input range to extend to 5V. A simple SPI™, with a digital supply that can operate as low as 1.65V, allows for easy interfacing to a wide variety of digital controllers. Automatic power-down can be enabled when operating at slower speeds to dramatically reduce power consumption.

Offered in a tiny 3mm × 3mm QFN package, the ADS7947/8/9 are fully specified over the extended temperature range of –40°C to +125°C and are suitable for a wide variety of data acquisition applications where high performance, low power, and small size are key.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FAMILY AND ORDERING INFORMATION(1)

PRODUCT	RESOLUTION (Bits)	INPUT	SAMPLE RATE (MSPS)
ADS7947	12	Unipolar, pseudo-differential	2
ADS7948	10	Unipolar, pseudo-differential	2
ADS7949	8	Unipolar, pseudo-differential	2

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS7947, ADS7948, ADS7949		UNIT
	MIN	MAX	
AINxP to GND or AINxN to GND	–0.3	AVDD + 0.3	V
AVDD to GND or DVDD to GND	–0.3	+7	V
Digital input voltage to GND	–0.3	DVDD + 0.3	V
Digital output to GND	–0.3	DVDD + 0.3	V
Operating temperature range	–40	+125	°C
Storage temperature range	–65	+150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *electrical characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS7947/48/49 RTE 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	54.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.7	
θ_{JB}	Junction-to-board thermal resistance	19.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	14.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: ADS7947 (12-Bit)

Minimum/maximum specifications at AVDD = 2.7V to 5.5V, DVDD = 1.65V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2MSPS, unless otherwise noted. Typical specifications at AVDD = 3V, DVDD = 1.8V, T_A = +25°C, and f_{SAMPLE} = 2MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Full-scale input span(1)		AINxP – AINxN	0		V_{REF}	V
Absolute input range		AIN0P, AIN1P	–0.2		AVDD + 0.2	V
		AIN0N, AIN1N	–0.2		0.2	V
Input capacitance(2)				32		pF
Input leakage current		At +125°C		1.5		nA
SYSTEM PERFORMANCE						
Resolution				12		Bits
No missing codes			12			Bits
Integral linearity			–1	±0.3	1	LSB(3)
Differential linearity			–1	±0.3	1	LSB
Offset error(4)			–1	±0.3	1	LSB
Gain error			–1	±0.3	1	LSB
Transition noise					25	μV_{RMS}
Power-supply rejection				60		dB
SAMPLING DYNAMICS						
Conversion time					13.5	SCLK
Acquisition time			80			ns
Maximum sample rate (throughput rate)		34MHz SCLK with a 16-clock frame			2	MSPS
		34MHz SCLK and $\overline{CS}$ low for 13.5 clocks			2.1	MSPS
Aperture delay					5	ns
Aperture jitter				10		ps
Step response				80		ns
Overvoltage recovery				80		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)(5)		100kHz		–85		dB
Signal-to-noise ratio (SNR)		100kHz	72	73		dB
Signal-to-noise and distorion ratio (SINAD)		100kHz		72.75		dB
Spurious-free dynamic range (SFDR)		100kHz		86		dB
Full-power bandwidth		At –3dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	I_{SOURCE} = 200µA	DVDD – 0.2			V
	V_{OL}	I_{SINK} = 200µA	0.4			V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA
External reference			2.5		AVDD	V

(1) Ideal input span; does not include gain or offset error.
(2) Refer to Figure 39 for sampling circuit details.
(3) LSB means Least Significant Bit.
(4) Measured relative to an ideal full-scale input.
(5) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: ADS7947 (12-Bit) (continued)

Minimum/maximum specifications at AVDD = 2.7V to 5.5V, DVDD = 1.65V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2MSPS, unless otherwise noted. Typical specifications at AVDD = 3V, DVDD = 1.8V, T_A = +25°C, and f_{SAMPLE} = 2MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
AVDD			2.7	3.3	5.5	V
DVDD			1.65	3.3	AVDD	V
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3V, f_{SAMPLE} = 2MSPS		2.5		mA
		AVDD = 5V, f_{SAMPLE} = 2MSPS		3	3.5	mA
	I_{STATIC}	AVDD = 3.3V, SCLK off		1.8		mA
		AVDD = 5V, SCLK off		1.9	2.5	mA
DVDD supply current(6)		DVDD = 3.3V, SCLK = 34MHz, SDO load 20pF		500		µA
Power-down state AVDD supply current	$I_{PD-DYNAMIC}$	SCLK = 34MHz			550	µA
	$I_{PD-STATIC}$	SCLK off			2.5	µA
Power-up time					1	µs
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(6) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD} \times DVDD \times$ number of 0→1 transitions in SDO $\times f_{SAMPLE}$. This is a load-dependent current and there is no DVDD current when the output is not toggling.

ELECTRICAL CHARACTERISTICS: ADS7948 (10-Bit)

Minimum/maximum specifications at AVDD = 2.7V to 5.5V, DVDD = 1.65V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2MSPS, unless otherwise noted. Typical specifications at AVDD = 3V, DVDD = 1.8V, T_A = +25°C, and f_{SAMPLE} = 2MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Full-scale input span(1)		AINxP – AINxN	0		V_{REF}	V
Absolute input range		AIN0P, AIN1P	–0.2		AVDD + 0.2	V
		AIN0N, AIN1N	–0.2		0.2	V
Input capacitance(2)				32		pF
Input leakage current		At +125°C		1.5		nA
SYSTEM PERFORMANCE						
Resolution				10		Bits
No missing codes			10			Bits
Integral linearity			–0.5	±0.15	0.5	LSB(3)
Differential linearity			–0.5	±0.15	0.5	LSB
Offset error(4)			–0.5	±0.15	0.5	LSB
Gain error			–0.5	±0.15	0.5	LSB
Transition noise					25	μV_{RMS}
Power-supply rejection				60		dB
SAMPLING DYNAMICS						
Conversion time					10.5	SCLK
Acquisition time			80			ns
Maximum sample rate (throughput rate)		34MHz SCLK in 16-clock frame			2	MSPS
		34MHz SCLK and $\overline{CS}$ low for 10.5 clocks			2.57	MSPS
Aperture delay					5	ns
Aperture jitter				10		ps
Step response				80		ns
Overvoltage recovery				80		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)(5)		100kHz		–80		dB
Signal-to-noise ratio (SNR)		100kHz	61			dB
Signal-to-noise and distortion ratio (SINAD)		100kHz		61		dB
Spurious-free dynamic range (SFDR)		100kHz		81		dB
Full-power bandwidth		At –3dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	I_{SOURCE} = 200µA	DVDD – 0.2			V
	V_{OL}	I_{SINK} = 200µA	0.4			V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA
External reference			2.5		AVDD	V

(1) Ideal input span; does not include gain or offset error.
(2) Refer to Figure 39 for sampling circuit details.
(3) LSB means Least Significant Bit.
(4) Measured relative to an ideal full-scale input.
(5) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: ADS7948 (10-Bit) (continued)

Minimum/maximum specifications at AVDD = 2.7V to 5.5V, DVDD = 1.65V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2MSPS, unless otherwise noted. Typical specifications at AVDD = 3V, DVDD = 1.8V, T_A = +25°C, and f_{SAMPLE} = 2MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
AVDD			2.7	3.3	5.5	V
DVDD			1.65	3.3	AVDD	V
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3V, f_{SAMPLE} = 2MSPS		2.5		mA
		AVDD = 5V, f_{SAMPLE} = 2MSPS		3	3.5	mA
	I_{STATIC}	AVDD = 3.3V, SCLK off		1.8		mA
		AVDD = 5V, SCLK off		1.9	2.5	mA
DVDD supply current(6)		DVDD = 3.3V, SCLK = 34MHz, SDO load 20pF		500		µA
Power-down state AVDD supply current	$I_{PD-DYNAMIC}$	SCLK = 34MHz			550	µA
	$I_{PD-STATIC}$	SCLK off			2.5	µA
Power-up time					1	µs
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(6) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD} \times DVDD \times$ number of 0→1 transitions in SDO $\times f_{SAMPLE}$. This is a load-dependent current and there is no DVDD current when the output is not toggling.

ELECTRICAL CHARACTERISTICS: ADS7949 (8-Bit)

Minimum/maximum specifications at AVDD = 2.7V to 5.5V, DVDD = 1.65V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2MSPS, unless otherwise noted. Typical specifications at AVDD = 3V, DVDD = 1.8V, T_A = +25°C, and f_{SAMPLE} = 2MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Full-scale input span(1)		AINxP – AINxN	0		V_{REF}	V
Absolute input range		AIN0P, AIN1P	–0.2		AVDD + 0.2	V
		AIN0N, AIN1N	–0.2		0.2	V
Input capacitance(2)				32		pF
Input leakage current		At +125°C		1.5		nA
SYSTEM PERFORMANCE						
Resolution				8		Bits
No missing codes			8			Bits
Integral linearity			–0.3	±0.06	0.3	LSB(3)
Differential linearity			–0.3	±0.06	0.3	LSB
Offset error(4)			–0.3	±0.06	0.3	LSB
Gain error			–0.3	±0.06	0.3	LSB
Transition noise					25	μV_{RMS}
Power-supply rejection				60		dB
SAMPLING DYNAMICS						
Conversion time					8.5	SCLK
Acquisition time			80			ns
Maximum sample rate (throughput rate)		34MHz SCLK in 16-clock frame			2	MSPS
		34MHz SCLK and $\overline{CS}$ low for 8.5 clocks			3	MSPS
Aperture delay					5	ns
Aperture jitter				10		ps
Step response				80		ns
Overvoltage recovery				80		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)(5)		100kHz		–80		dB
Signal-to-noise ratio (SNR)		100kHz	49			dB
Signal-to-noise and distortion ratio (SINAD)		100kHz		49		dB
Spurious-free dynamic range (SFDR)		100kHz		81		dB
Full-power bandwidth		At –3dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	I_{SOURCE} = 200µA	DVDD – 0.2			V
	V_{OL}	I_{SINK} = 200µA	0.4			V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA
External reference			2.5		AVDD	V

(1) Ideal input span; does not include gain or offset error.
(2) Refer to Figure 39 for sampling circuit details.
(3) LSB means Least Significant Bit.
(4) Measured relative to an ideal full-scale input.
(5) Calculated on the first nine harmonics of the input frequency.

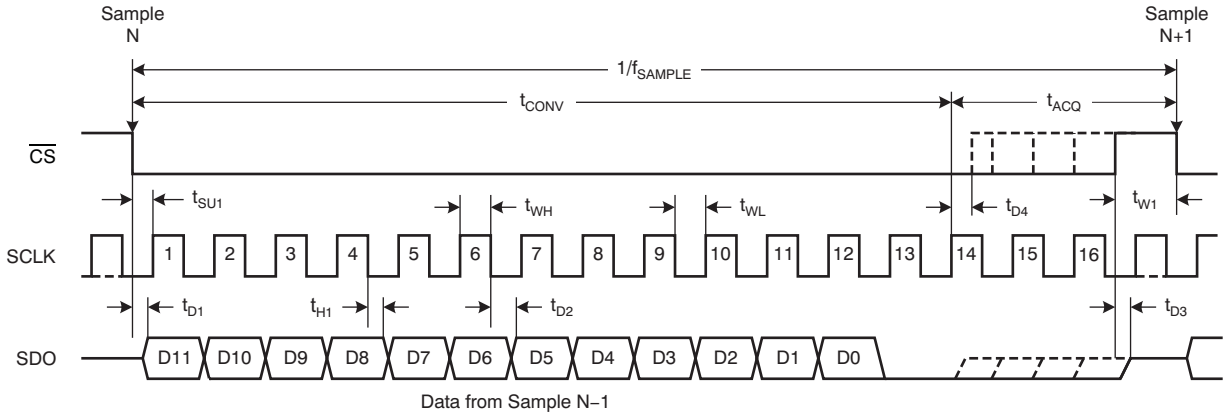
ELECTRICAL CHARACTERISTICS: ADS7949 (8-Bit) (continued)

Minimum/maximum specifications at AVDD = 2.7V to 5.5V, DVDD = 1.65V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2MSPS, unless otherwise noted. Typical specifications at AVDD = 3V, DVDD = 1.8V, T_A = +25°C, and f_{SAMPLE} = 2MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
AVDD			2.7	3.3	5.5	V
DVDD			1.65	3.3	AVDD	V
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3V, f_{SAMPLE} = 2MSPS		2.5		mA
		AVDD = 5V, f_{SAMPLE} = 2MSPS		3	3.5	mA
	I_{STATIC}	AVDD = 3.3V, SCLK off		1.8		mA
		AVDD = 5V, SCLK off		1.9	2.5	mA
DVDD supply current(6)		DVDD = 3.3V, SCLK = 34MHz, SDO load 20pF		500		µA
Power-down state AVDD supply current	$I_{PD-DYNAMIC}$	SCLK = 34MHz			550	µA
	$I_{PD-STATIC}$	SCLK off			2.5	µA
Power-up time					1	µs
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(6) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD} \times DVDD \times$ number of 0→1 transitions in SDO $\times f_{SAMPLE}$. This is a load-dependent current and there is no DVDD current when the output is not toggling.

TIMING DIAGRAM



TIMING REQUIREMENTS

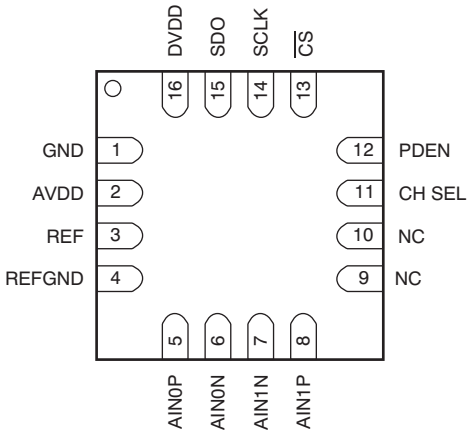
All specifications at DVDD = 1.65V to AVDD and T_A = –40°C to +125°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time	ADS7947 (12-bit)				13.5	SCLK
		ADS7948 (10-bit)				10.5	SCLK
		ADS7949 (8-bit)				8.5	SCLK
t_{ACQ}	Acquisition time			80			ns
f_{SAMPLE}	Sample rate (throughput rate)		SCLK = 34MHz, 16 clock frame			2	MSPS
	$f_{SAMPLE\ MAX} = 1/(t_{CONV\ MAX} + t_{ACQ\ MIN})$	ADS7947 (12-bit)	SCLK = 34MHz			2.1	MSPS
		ADS7948 (10-bit)	SCLK = 34MHz			2.57	MSPS
		ADS7949 (8-bit)	SCLK = 34MHz			3	MSPS
t_{W1}	Pulse width $\overline{CS}$ high			25			ns
t_{D1}	Delay time, $\overline{CS}$ low to first data (D0-15) out		DVDD = 1.8V			14.5	ns
			DVDD = 3V			12.5	ns
			DVDD = 5V			8.5	ns
t_{SU1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK		DVDD = 1.8V	3.5			ns
			DVDD = 3V	3.5			ns
			DVDD = 5V	3.5			ns
t_{D2}(2)	Delay time, SCLK falling to SDO		DVDD = 1.8V			11	ns
			DVDD = 3V			9	ns
			DVDD = 5V			7.1	ns
t_{H1}	Hold time, SCLK falling to data valid		DVDD = 1.8V	4			ns
			DVDD = 3V	3			ns
			DVDD = 5V	2			ns
t_{D3}	Delay time, $\overline{CS}$ high to SDO 3-state		DVDD = 1.8V			15	ns
			DVDD = 3V			12.5	ns
			DVDD = 5V			8.5	ns
t_{D4}	Delay time $\overline{CS}$ rising edge from conversion end (refer to the t_{CONV} specification for conversion time)			10			ns
t_{WH}	Pulse duration, SCLK high			11			ns
t_{W1}	Pulse duration, SCLK low			11			ns
	SCLK frequency			0.4	34	40	MHz
t_{PDSU}	Setup time, PDEN high to $\overline{CS}$ rising edge (refer to Figure 50 and Figure 51)			2			ns
t_{PDH}	Hold time, $\overline{CS}$ rising edge to PDEN falling edge (refer to Figure 50)			20			ns

(1) 1.8V specifications apply from 1.65V to 2V; 3V specifications apply form 2.7V to 3.6V; 5V specifications apply from 4.75V to 5.25V.
(2) With 50pF load.

PIN CONFIGURATION

RTE PACKAGE
QFN-16
(TOP VIEW)



PIN FUNCTIONS

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
1	GND	Analog/digital	Power supply ground; all analog and digital signals are referred with respect to this pin
2	AVDD	Analog	ADC power supply
3	REF	Analog	ADC positive reference input; decouple this pin with REFGND
4	REFGND	Analog	Reference return; short to analog ground plane
5	AIN0P	Analog input	Positive analog input, channel 0
6	AIN0N	Analog input	Negative analog input, channel 0. Note that the allowable signal swing on this pin is ±0.2V; this pin can be grounded.
7	AIN1N	Analog input	Negative analog input, channel 1. Note that the allowable signal swing on this pin is ±0.2V; this pin can be grounded.
8	AIN1P	Analog input	Positive analog input, channel 1
9	NC	—	Not connected internally, it is recommended to externally short this pin to GND
10	NC	—	Not connected internally, it is recommended to externally short this pin to GND
11	CH SEL	Digital input	This pin selects the analog input channel. Low = channel 0, high = channel 1. It is recommended to change the channel within a window of one clock; from half a clock after the $\overline{CS}$ falling edge. This change ensures the settling on the multiplexer output before the sample start.
12	PDEN	Digital input	This pin enables a power-down feature if it is high at the $\overline{CS}$ rising edge
13	$\overline{CS}$	Digital input	Chip select signal; active low
14	SCLK	Digital input	Serial SPI clock
15	SDO	Digital output	Serial data out
16	DVDD	Digital	Digital I/O supply

TYPICAL CHARACTERISTICS: ADS7947, ADS7948, ADS7949

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

SUPPLY CURRENT vs ANALOG SUPPLY VOLTAGE

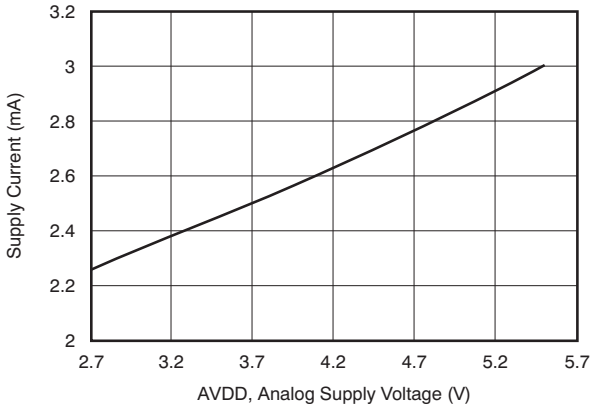


Figure 1.

SUPPLY CURRENT vs TEMPERATURE

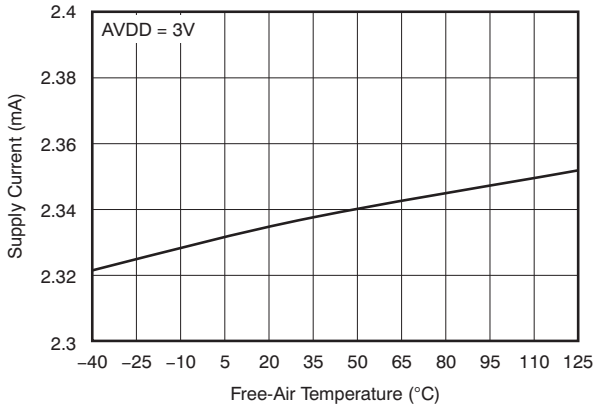


Figure 2.

STATIC CURRENT vs ANALOG SUPPLY VOLTAGE

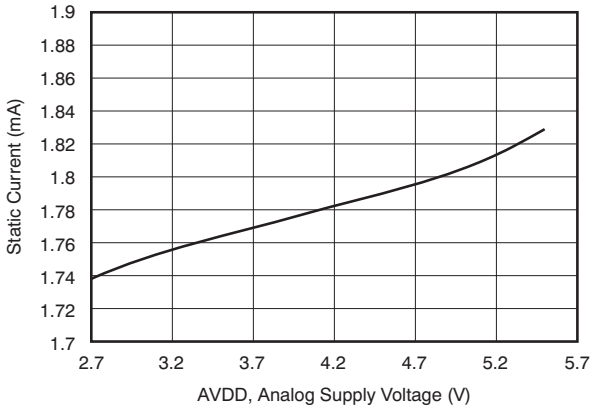


Figure 3.

STATIC CURRENT vs FREE-AIR TEMPERATURE

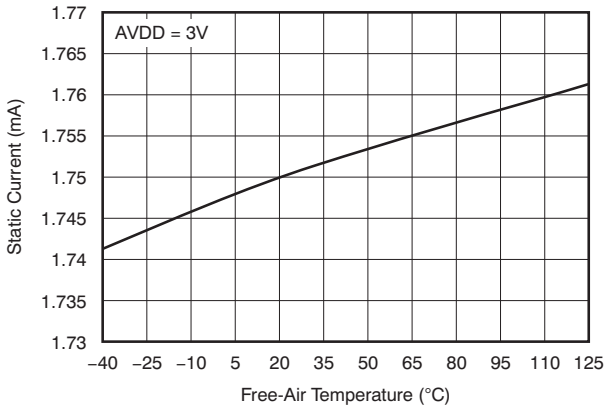


Figure 4.

SUPPLY CURRENT vs THROUGHPUT

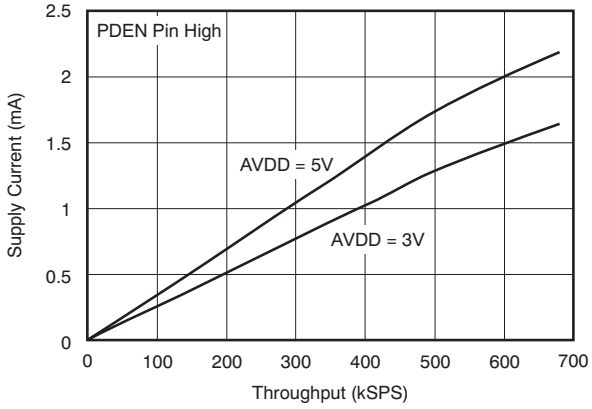


Figure 5.

TYPICAL CHARACTERISTICS: ADS7947 (12-Bit)

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

DIFFERENTIAL LINEARITY vs ANALOG SUPPLY VOLTAGE

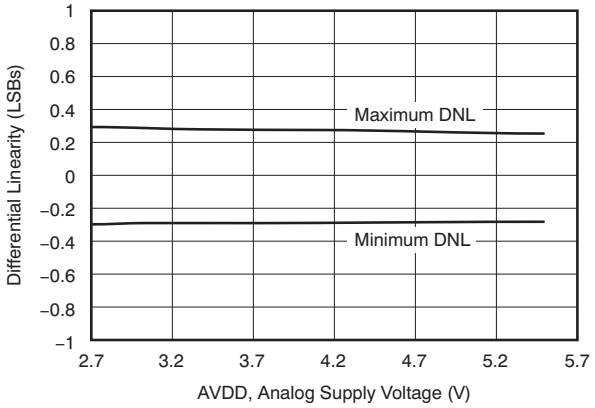


Figure 6.

INTEGRAL LINEARITY vs ANALOG SUPPLY VOLTAGE

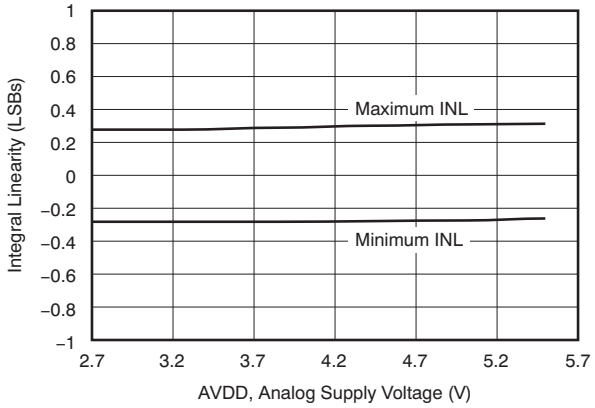


Figure 7.

DIFFERENTIAL LINEARITY vs TEMPERATURE

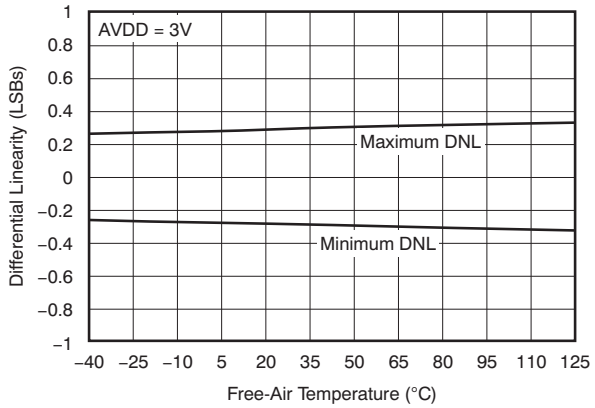


Figure 8.

INTEGRAL LINEARITY vs TEMPERATURE

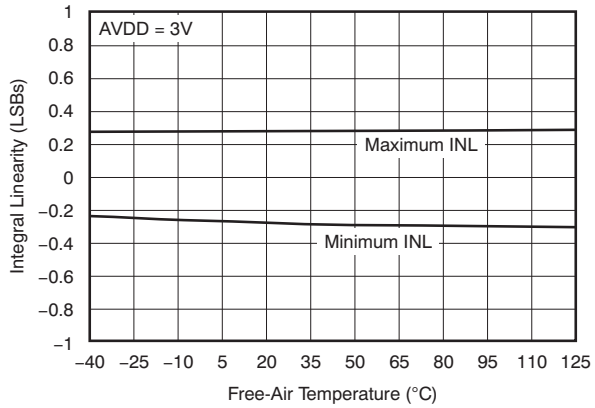


Figure 9.

DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE

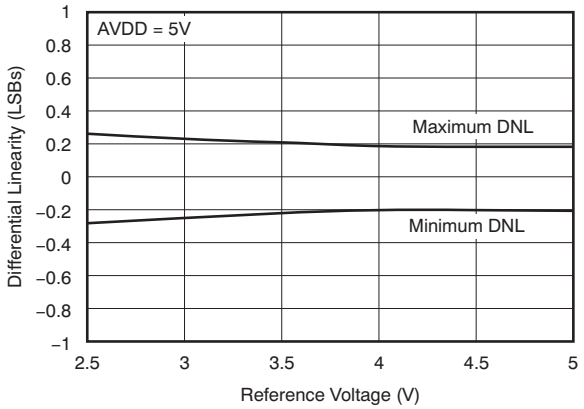


Figure 10.

INTEGRAL LINEARITY vs REFERENCE VOLTAGE

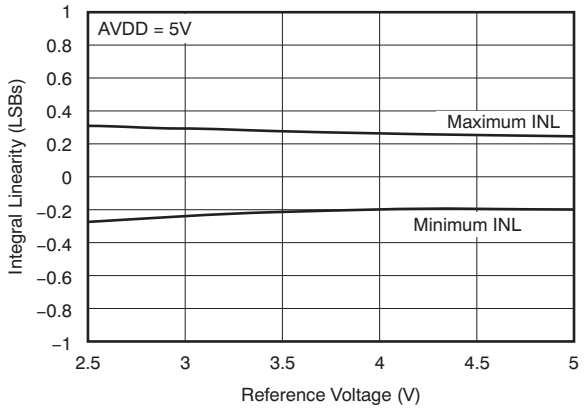


Figure 11.

TYPICAL CHARACTERISTICS: ADS7947 (12-Bit) (continued)

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

OFFSET ERROR vs ANALOG SUPPLY VOLTAGE

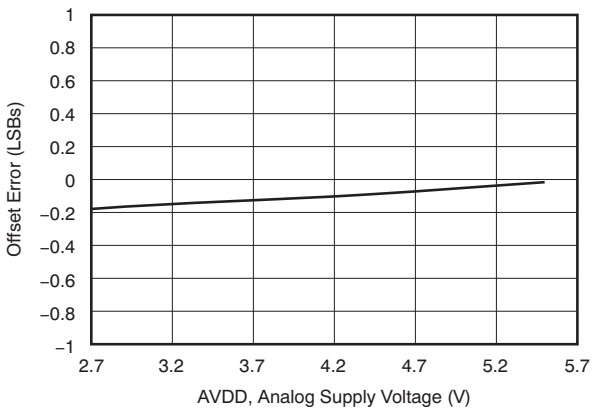


Figure 12.

OFFSET ERROR vs TEMPERATURE

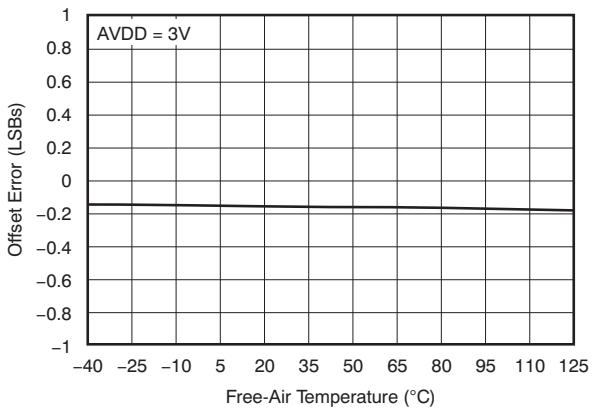


Figure 13.

OFFSET ERROR vs REFERENCE VOLTAGE

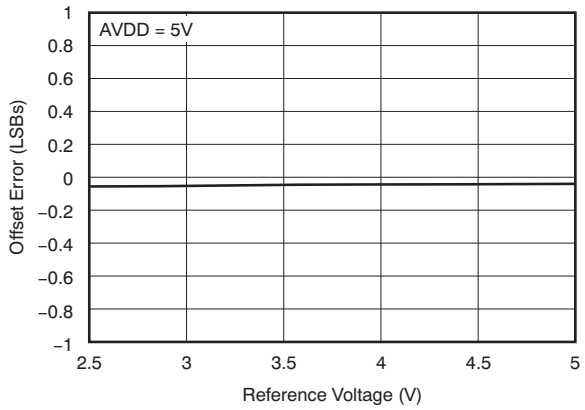


Figure 14.

GAIN ERROR vs ANALOG SUPPLY VOLTAGE

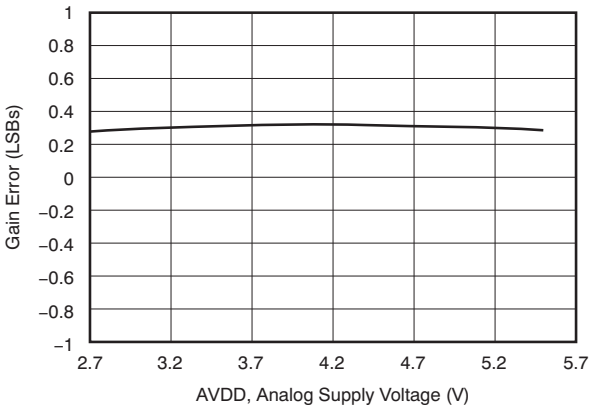


Figure 15.

GAIN ERROR vs TEMPERATURE

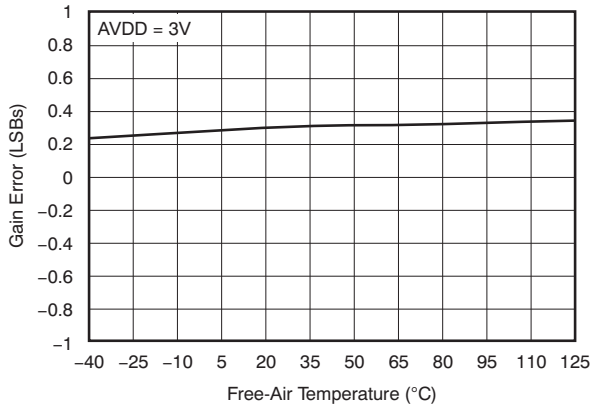


Figure 16.

GAIN ERROR vs REFERENCE VOLTAGE

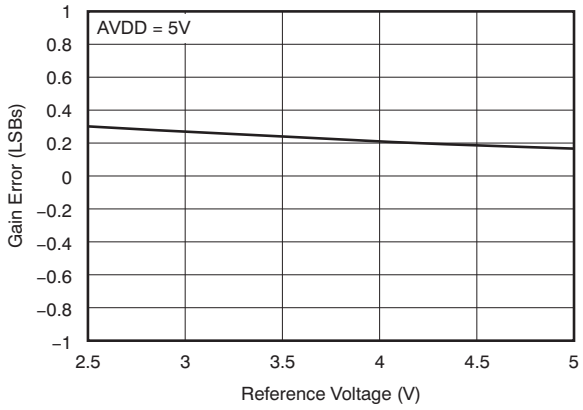


Figure 17.

TYPICAL CHARACTERISTICS: ADS7947 (12-Bit) (continued)

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

SNR vs ANALOG SUPPLY VOLTAGE

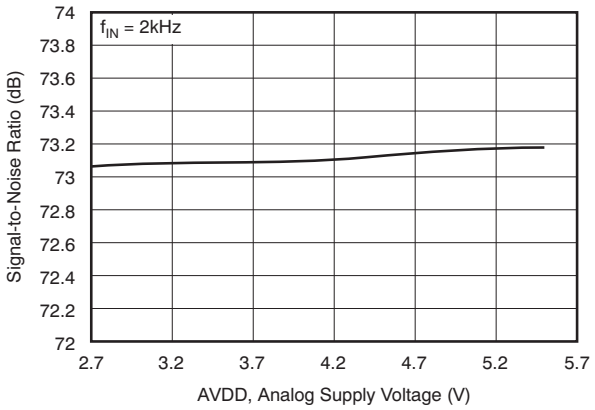


Figure 18.

SNR vs TEMPERATURE

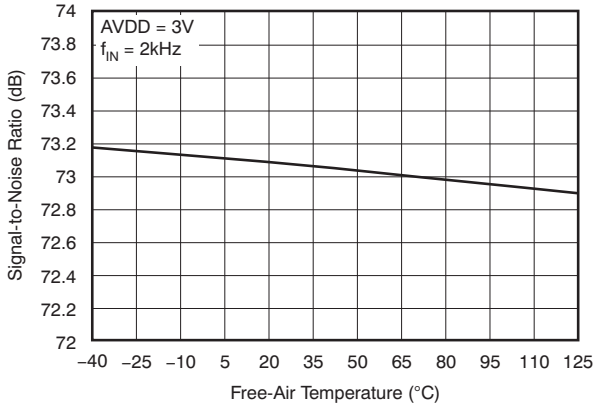


Figure 19.

SNR vs REFERENCE VOLTAGE

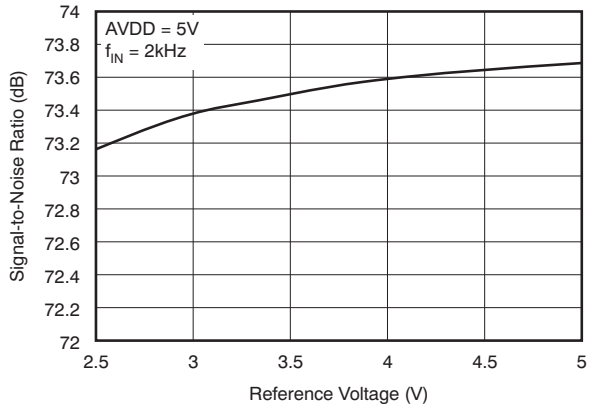


Figure 20.

SNR vs INPUT FREQUENCY

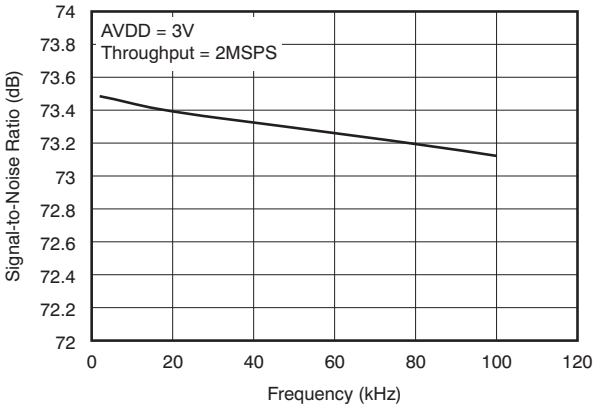


Figure 21.

SINAD vs ANALOG SUPPLY VOLTAGE

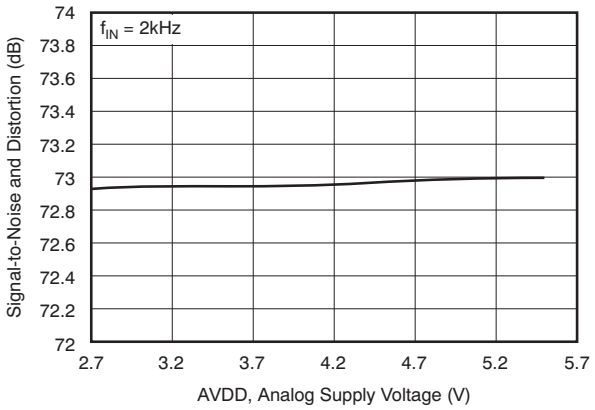


Figure 22.

SINAD vs TEMPERATURE

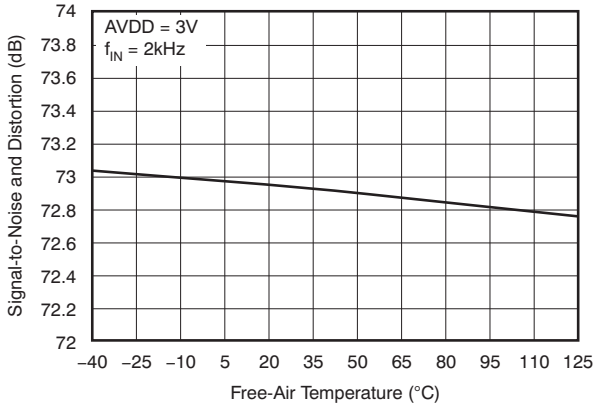


Figure 23.

TYPICAL CHARACTERISTICS: ADS7947 (12-Bit) (continued)

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

SINAD vs REFERENCE VOLTAGE

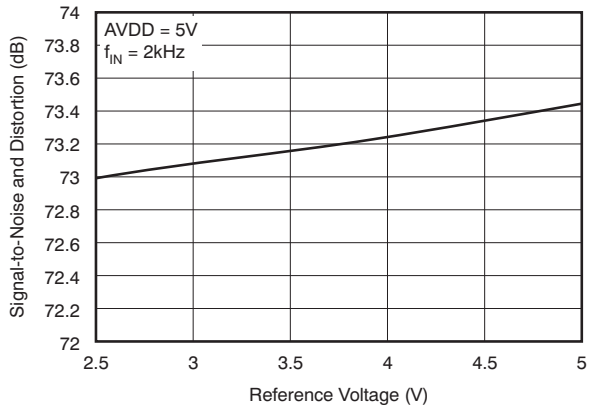


Figure 24.

SINAD vs INPUT FREQUENCY

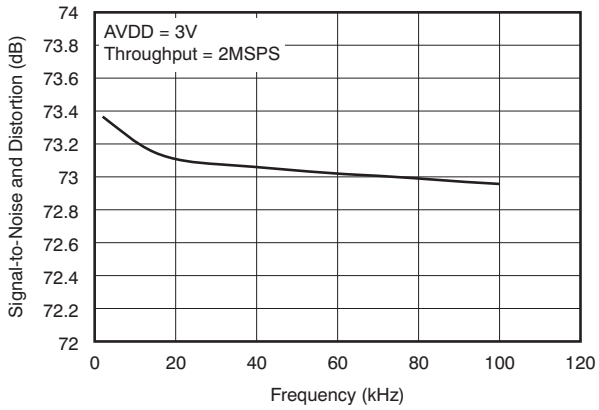


Figure 25.

SFDR vs AVDD

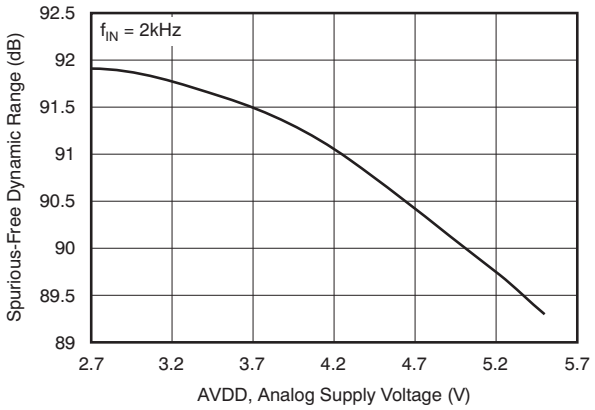


Figure 26.

SFDR vs TEMPERATURE

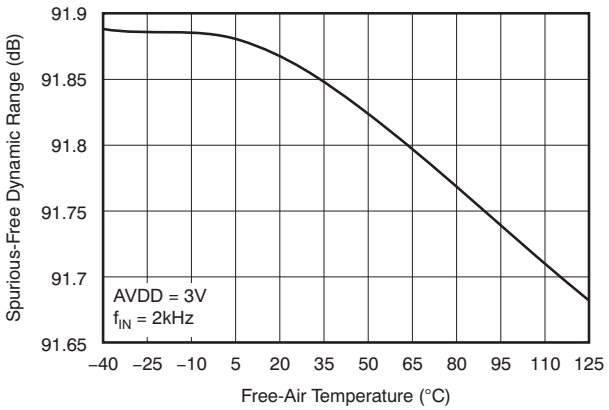


Figure 27.

SFDR vs REFERENCE VOLTAGE

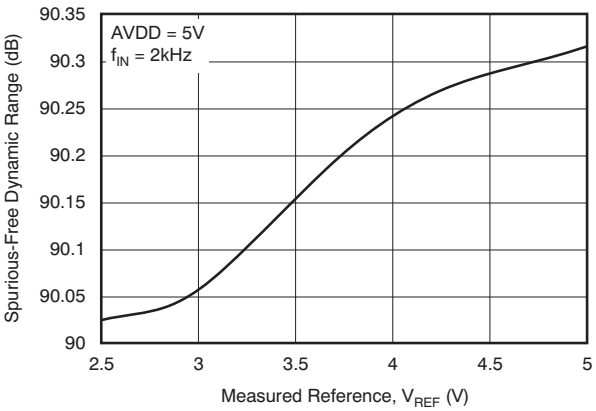


Figure 28.

SFDR vs INPUT FREQUENCY

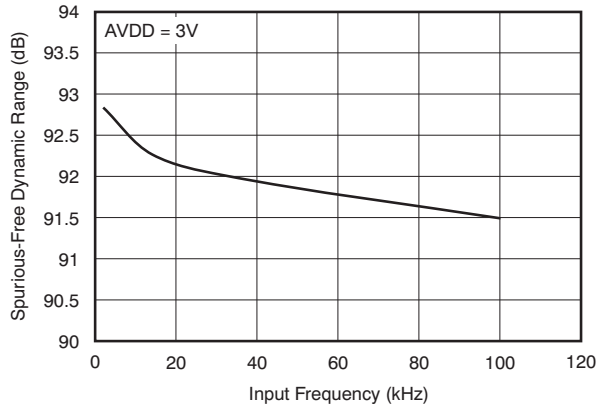


Figure 29.

TYPICAL CHARACTERISTICS: ADS7947 (12-Bit) (continued)

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

SFDR vs AVDD

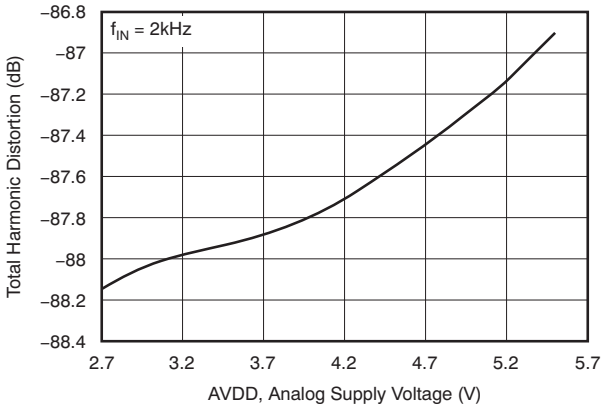


Figure 30.

SFDR vs TEMPERATURE

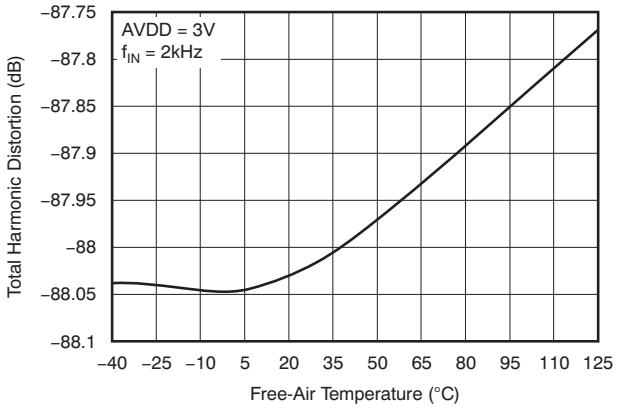


Figure 31.

THD vs REFERENCE VOLTAGE

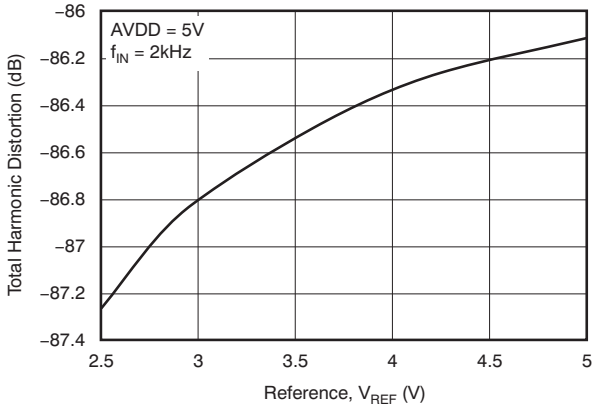


Figure 32.

THD vs INPUT FREQUENCY

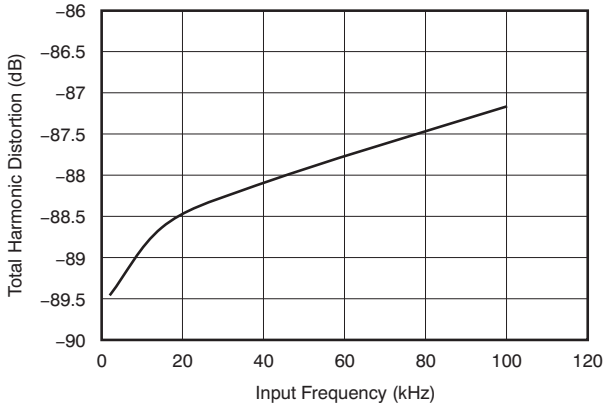
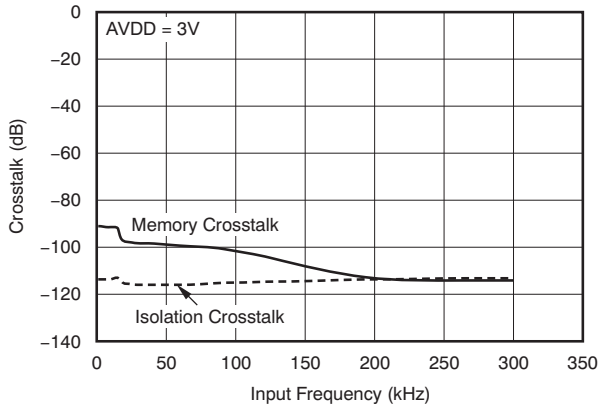


Figure 33.

CROSSTALK vs INPUT FREQUENCY(1)



(1) Memory crosstalk is the effect of the last converted channel on the current converted channel data. Isolation crosstalk is the effect on the channel being converted that is coming from the signal on the channel that is off.

Figure 34.

SPECTRAL RESPONSE (8192-Point FFT)

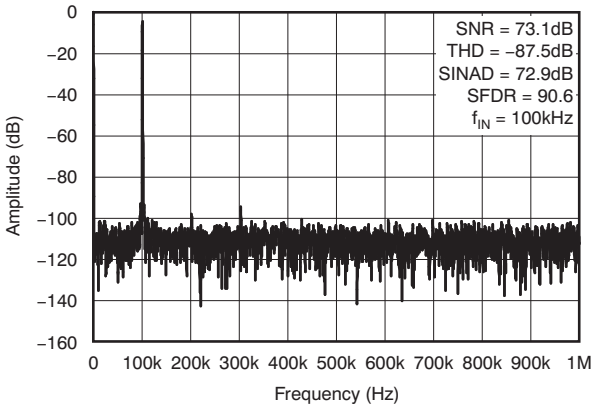


Figure 35.

TYPICAL CHARACTERISTICS: ADS7947 (12-Bit) (continued)

At T_A = +25°C, DVDD = 1.8V, V_{REF} = 2.5V, and f_{SAMPLE} = 2MSPS, unless otherwise noted.

TYPICAL INL

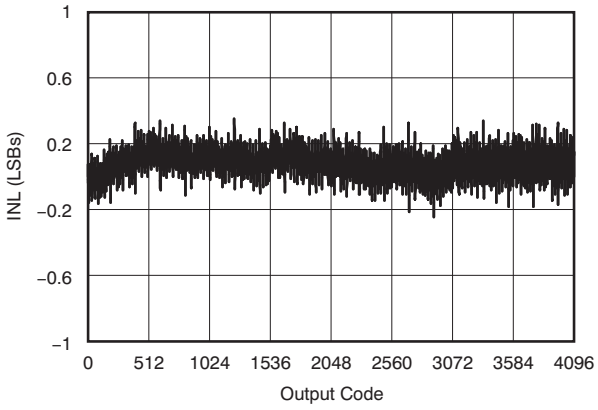


Figure 36.

TYPICAL DNL

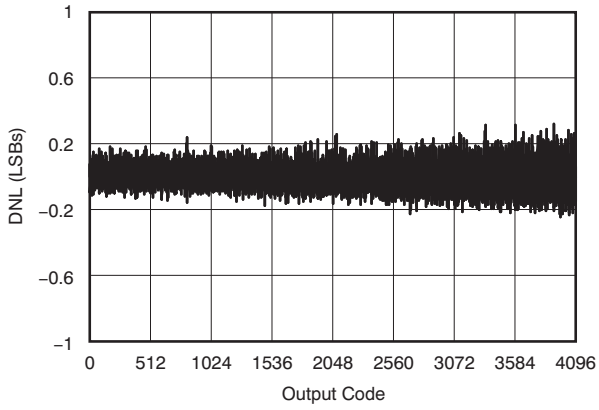


Figure 37.

OVERVIEW

The ADS7947 is 12-bit, miniature, dual-channel, low-power SAR ADC. The ADS7948 and ADS7949 are 10-bit and 8-bit devices, respectively, from the same product family. These devices feature very low power consumption at rated speed. The PDEN pin enables an auto power-down mode that further reduces power consumption at lower speeds.

MULTIPLEXER AND ADC INPUT

The devices feature pseudo-differential inputs with a double-pole, double-throw multiplexer. The negative inputs (AINxN) can accept swings of ±0.2V; the positive inputs (AINxP) allow signals in the range of 0V to V_{REF} over the negative input. The ADC converts the difference in voltage: $V_{AINxP} – V_{AINxN}$. This feature can be used in multiple ways.

Two signals can be connected from different sensors with unequal ground potentials (within ±0.2V) to a single ADC. The pseudo-differential ADC rejects common-mode offset and noise. This feature also allows the use of a single-supply op amp. The signal and the AINxN input can be offset by +0.2V, which provides the ground clearance needed for a single-supply op amp.

Figure 38 shows the electrostatic discharge (ESD) diodes to supply and ground at every analog input. Make sure that these diodes do not turn on by keeping the supply voltage within the specified input range.

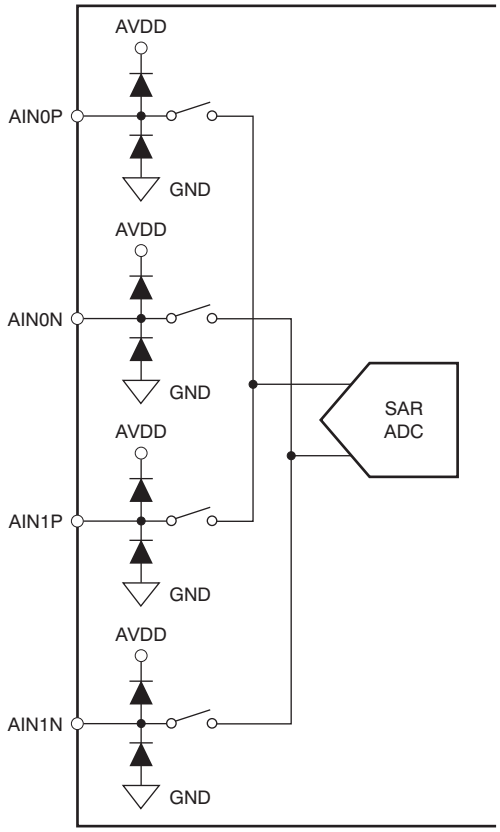


Figure 38. Analog Inputs

Figure 39 shows an equivalent circuit of the multiplexer and ADC sampling stage. The positive and negative inputs are separately sampled on 32pF sampling capacitorss. The multiplexer and sampling switches are represented by an ideal switch in series with a 12Ω resistance. During sampling, the devices connect the 32pF sampling capacitor to the ADC driver. This connection creates a glitch at the device input. It is recommended to connect a capacitor across the AINxP and AINxN terminals to reduce this glitch. A driving circuit must have sufficient bandwidth to settle this glitch within the acquisition time.

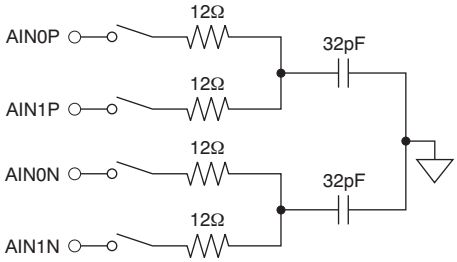
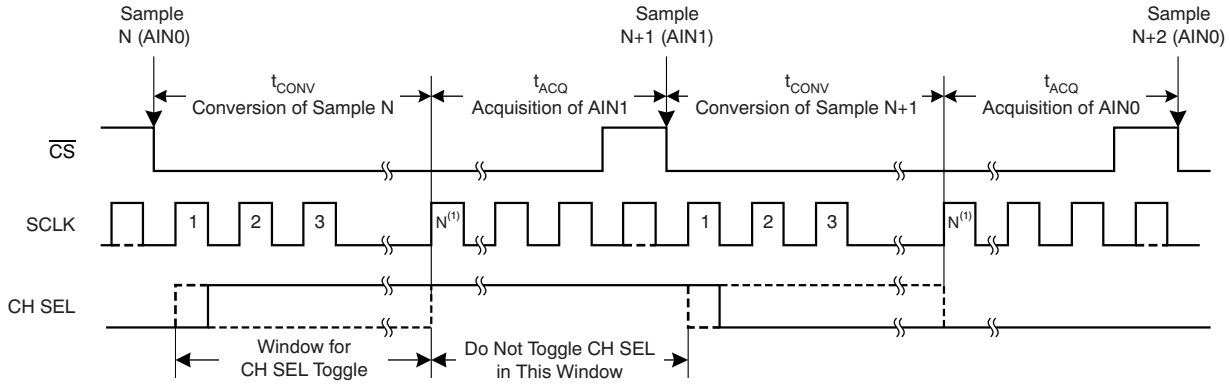


Figure 39. Input Sampling Stage Equivalent Circuit
(See the *Application Information* section for details on the driving circuit.)

Figure 40 shows a timing diagram for the ADC analog input channel selection. As shown in Figure 40, the CH SEL signal selects the analog input channel to the ADC. CH SEL = 0 selects channel 0 (AIN0P – AIN0N) and CH SEL = 1 selects channel 1 (AIN1P – AIN1N). It is recommended not to toggle the CH SEL signal during an ADC acquisition phase until the device sees the first valid SCLK rising edge after the device samples the analog input. If CH SEL is toggled during this period, it can cause erroneous output code as the device might see unsettled analog input.

CH SEL can be toggled at any time during the window specified in Figure 40; however, it is recommended to select the desired channel after the first SCLK rising edge and before the second SCLK rising edge. This timing ensures that the multiplexer output is settled before the ADC starts acquisition of the analog input.



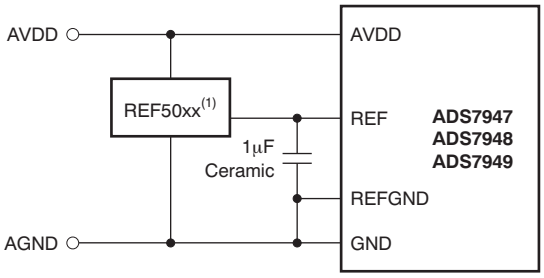
(1) *N* indicates the 14th SCLK rising edge for the ADS7947 (12-bit) , the 11th rising edge for the ADS7948 (10-bit), and the ninth rising edge for the ADS7949 (8-bit).

Figure 40. ADC Analog Input Channel Selection

REFERENCE

The ADS7947/8/9 use an external reference voltage during the conversion of a sampled signal. The devices switch the capacitors used in the conversion process to the reference terminal during conversion. The switching frequency is the same as the SCLK frequency. It is necessary to decouple the REF terminal to REFGND with a 1µF ceramic capacitor in order to get the best noise performance from the device. The capacitor must be placed closest to these pins. The reference input can be driven with the REF50xx series precision references from TI. Figure 41 shows a typical reference driving circuit.

Sometimes it is convenient to use AVDD as a reference. The ADS794x allow reference ranges up to AVDD. However, make sure that AVDD is well-bypassed and that there is a separate bypass capacitor between REF and REFGND.



(1) Select the appropriate device as described by the required reference value. For example, select the REF5040 for a 4V reference, the REF5030 for a 3V reference, and the REF5025 for a 2.5V reference. Ensure that (AVDD – REF) > 0.2V so that the REF50xx functions properly.

Figure 41. Typical Reference Driving Circuit

CLOCK

The ADS794x use SCLK for conversions (typically 34MHz). A lower frequency SCLK can be used for applications requiring sample rates less than 2MSPS. However, it is better to use a 34MHz SCLK and slow down the device speed by choosing a lower frequency for $\overline{CS}$, which allows more acquisition time. This configuration relaxes constraints on the output impedance of the driving circuit. Refer to the *Application Information* section for calculation of the driving circuit output impedance.

ADC TRANSFER FUNCTION

The ADS7947 (12-bit), ADS7948 (10-bit), and ADS7949 (8-bit) devices are unipolar, pseudo-differential input. The ADC output is in straight binary format. Figure 42 shows ideal characteristics for this family of devices. Here, FSR is the full-scale range for the ADC input (AINxP – AINxN) and is equal to the reference input voltage to the ADC (V_{REF}). 1LSB is equal to ($V_{REF}/2^N$) where *N* is the resolution of the ADC (for example, N = 12 for the ADS7947).

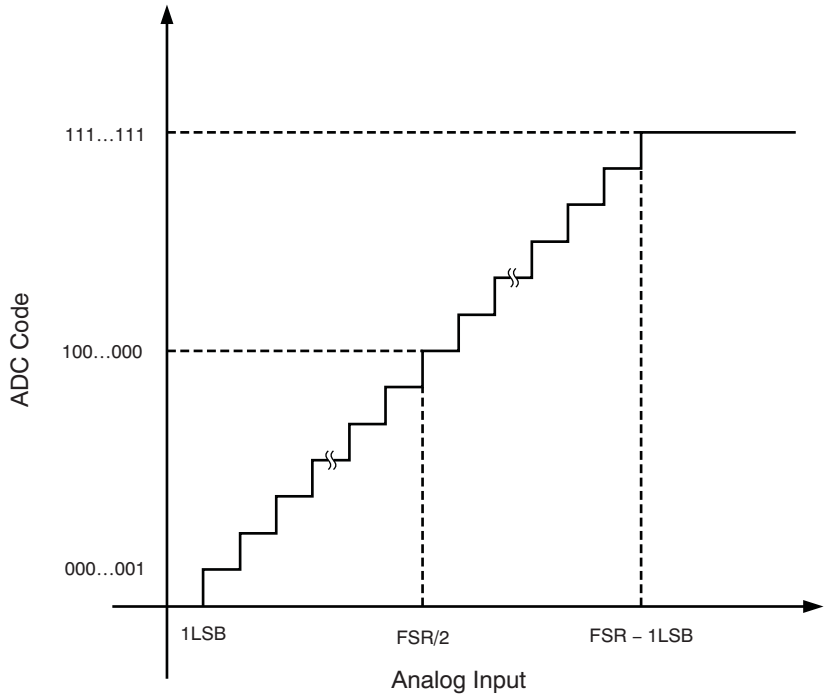


Figure 42. ADS7947/8/9 Transfer Characteristics

DEVICE OPERATION

The ADS7947/8/9 are typically operated with either a 16-clock frame or 32-clock frame for ease of interfacing with the host processor.

16-CLOCK FRAME

Figure 43 through Figure 45 show the devices operating in 16-clock mode. This mode is the fastest mode for device operation. In this mode, the devices output data from previous conversions while converting the recently sampled signal.

As shown in Figure 43, the ADS7947 starts acquisition of the analog input from the 14th rising edge of SCLK. The device samples the input signal on the $\overline{CS}$ falling edge. SDO comes out of 3-state and the device outputs the MSB on the $\overline{CS}$ falling edge. The device outputs the next lower SDO bits on every SCLK falling edge after it has first seen the SCLK rising edge. The data correspond to the sample and conversion completed in the previous frame. During a $\overline{CS}$ low period, the device converts the recently sampled signal. It uses SCLK for conversions. The number of clocks needed for a conversion for 12-bit and 8-bit devices are different. For the ADS7947, conversion is complete on the 14th SCLK rising edge. $\overline{CS}$ can be high at any time after the 14th SCLK rising edge. The $\overline{CS}$ rising edge after the 14th SCLK rising edge and before the 29th SCLK falling edge keeps the device in the 16-clock data frame. The device output goes to 3-state with $\overline{CS}$ high.

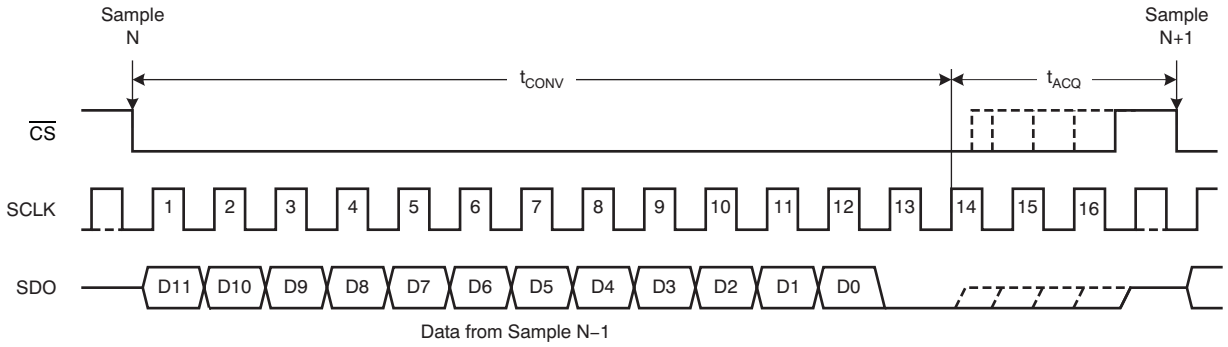


Figure 43. ADS7947 Operating in 16-Clock Mode without Power-Down (PDEN = 0)

It is also permissible to stop SCLK after device has seen the 14th SCLK rising edge.

Figure 44 and Figure 45 show the 16-clock mode operation for the ADS7948 and ADS7949, respectively. The operation for these 10-bit and 8-bit devices is identical to the ADS7947 except that the conversion ends on different edges of SCLK. For the ADS7948, the conversion ends and acquisition starts on the 11th SCLK rising edge. For the ADS7949, the device uses the ninth SCLK rising edge for the conversion end and acquisition start. Similar to the ADS7947, $\overline{CS}$ can go high and SCLK may be stopped once the device enters acquisition.

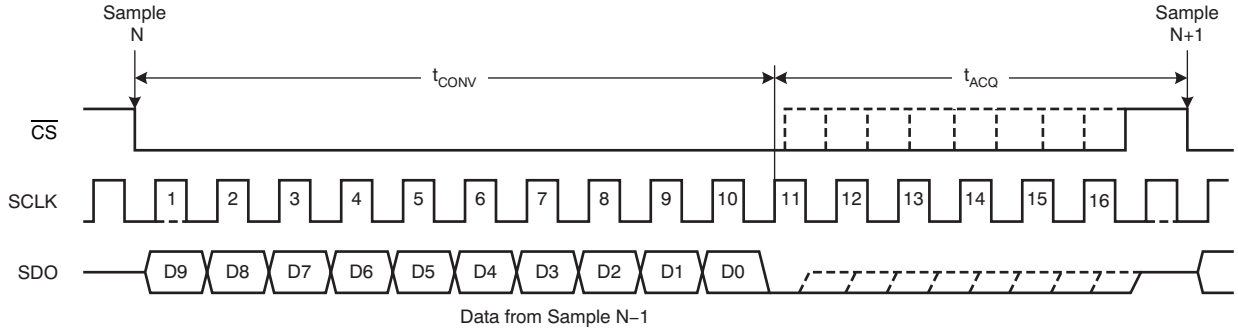


Figure 44. ADS7948 Operating in 16-Clock Mode without Power-Down (PDEN = 0)

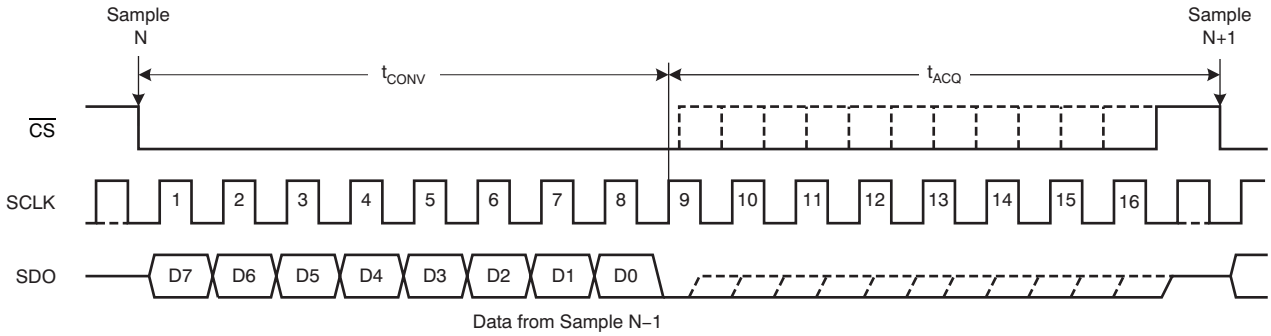


Figure 45. ADS7949 Operating in 16-Clock Mode without Power-Down (PDEN = 0)

32-CLOCK FRAME

Figure 46 through Figure 48 show the devices operating in 32-clock mode. In this mode, the devices convert and output the data from the most recent sample before taking the next sample.

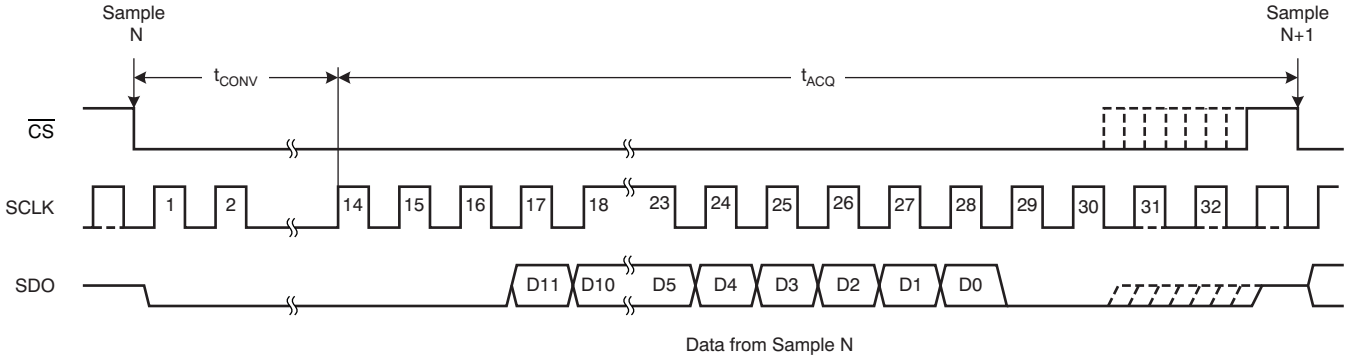


Figure 46. ADS7947 Operation in 32-Clock Frame without Power-Down (PDEN = 0)

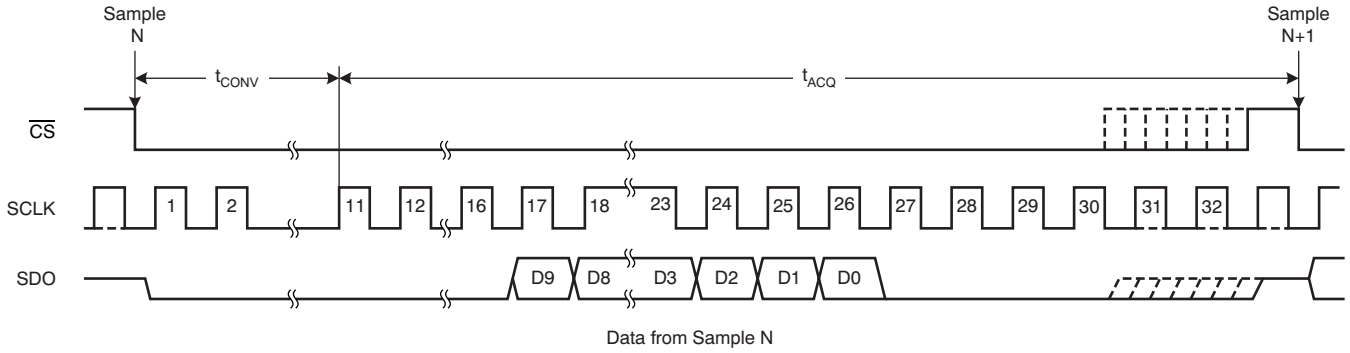


Figure 47. ADS7948 Operating in 32-Clock Frame without Power-Down (PDEN = 0)

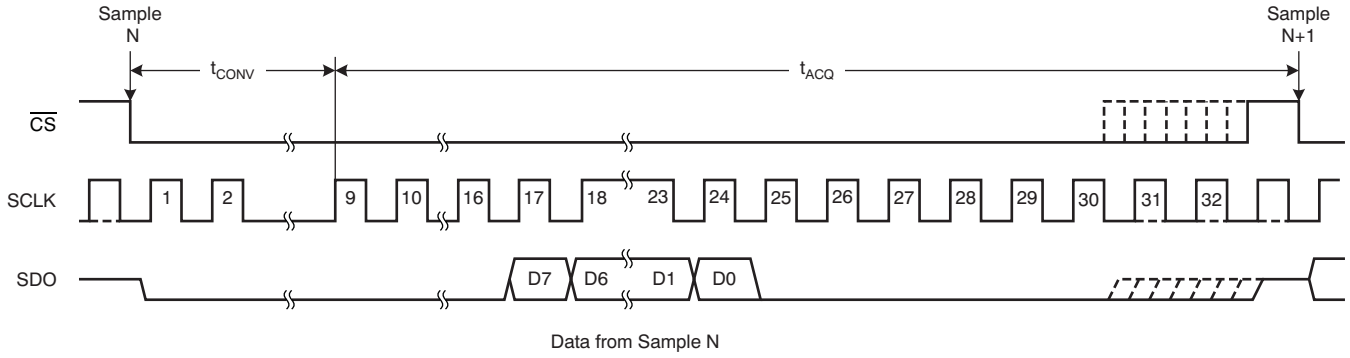


Figure 48. ADS7949 Operating in 32-Clock Frame without Power-Down (PDEN = 0)

$\overline{CS}$ can be held low past the 16th falling edge of SCLK. The device continues to output recently converted data starting with the 16th SCLK falling edge. If $\overline{CS}$ is held low until the 30th SCLK falling edge, then the device detects 32-clock mode. Note that the device data from recent conversions are already out with no latency before the 30th SCLK falling edge. Once 32-clock mode is detected, the device outputs 16 zeros during the next conversion (in fact, for the first 16 clocks), unlike 16-clock mode where the device outputs the previous conversion result. SCLK can be stopped after the device has seen the 30th falling edge with $\overline{CS}$ low.

POWER-DOWN

The ADS7947/8/9 family of devices offer an easy-to-use power-down feature available through a dedicated PDEN pin (pin 12). A high level on PDEN at the $\overline{CS}$ rising edge enables the power-down mode for that particular cycle. Figure 49 to Figure 51 illustrate device operation with power-down in both 32-clock and 16-clock mode.

Many applications must slow device operation. For speeds below approximately 500kSPS, it is convenient to use 32-clock mode with power-down. This results in considerable power savings.

As shown in Figure 49, PDEN is held at a logic '1' level. Note that the device looks at the PDEN status only at the $\overline{CS}$ rising edge; however, for continuous low-speed operation, it is convenient to continuously hold PDEN = 1. The devices detect power-down mode on the $\overline{CS}$ rising edge with PDEN = 1.

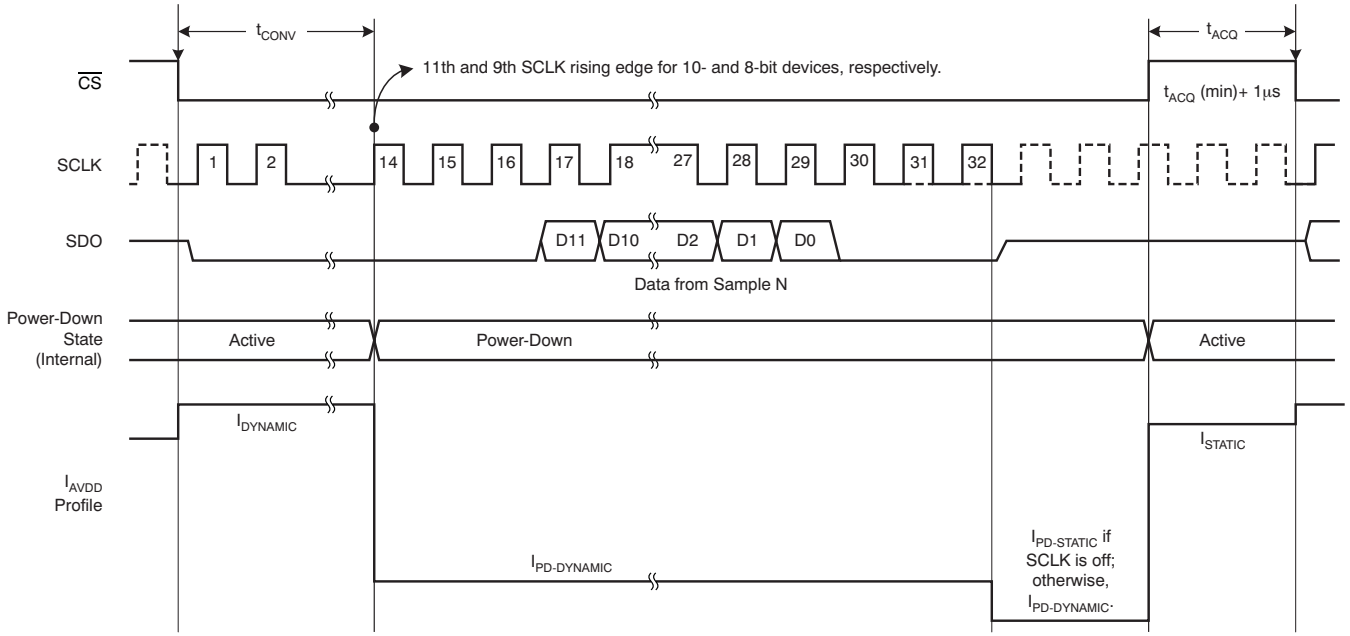


Figure 49. Operation with a 32-Clock Frame in Power-Down Mode (PDEN = 1)

On the $\overline{CS}$ falling edge, the devices start normal operation as previously described. The devices complete conversions on the 14th SCLK rising edge. (Conversions complete on the 11th and ninth SCLK rising edge for 10-bit and 8-bit devices, respectively.) The devices enter the power-down state immediately after conversions complete. However, the devices can still output data as per the timings described previously. The devices consume dynamic power-down current ($I_{PD\text{-}DYNAMIC}$) during data out operations. It is recommended to stop the clock after the 32nd SCLK falling edge to further save power down to the *static power-down current* level ($I_{PD\text{-}STATIC}$). The devices power up again on the SCLK rising edge. However, they require an extra 1µs to power up completely. $\overline{CS}$ must be high for the 1µs + t_{ACQ} (min) period.

In some applications, data collection is accomplished in burst mode. The system powers down after data collection. 16-clock mode is convenient for these applications. Figure 50 and Figure 51 detail power saving in 16-clock burst mode.

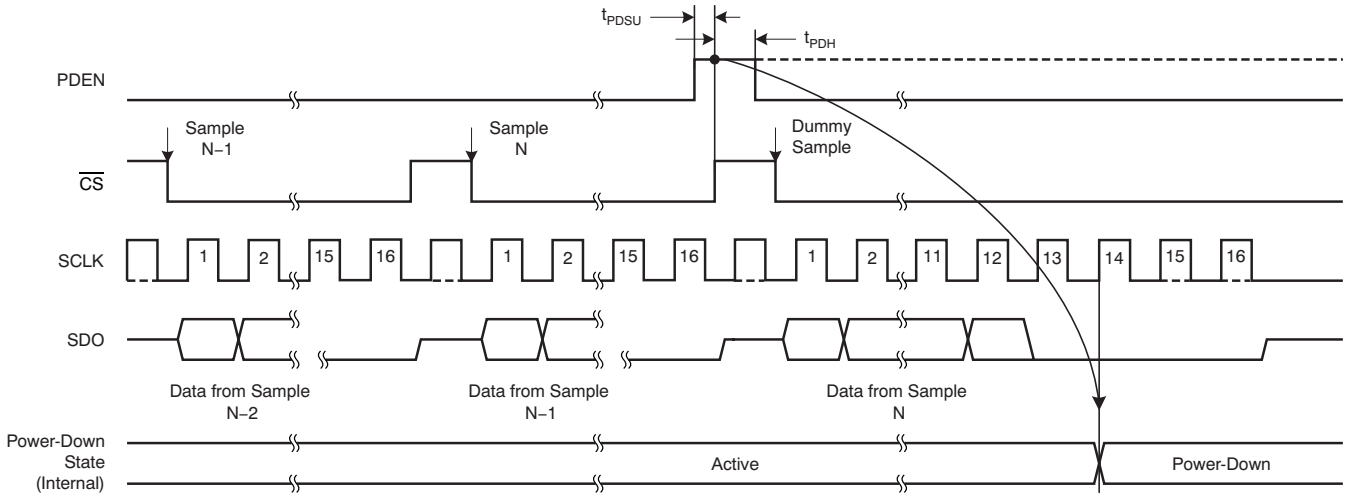


Figure 50. Entry Into Power-Down with 16-Clock Burst Mode

As shown in Figure 50, the two frames capturing the *N–1* and *Nth* samples are normal 16-clock frames. Keeping PDEN = 1 prior to the $\overline{CS}$ rising edge in the next frame ensures that the devices detect the power-down mode. Data from the Nth sample are read during this frame. It is expected that the Nth sample represents the last data of interest in the burst of conversions. The devices enter power-down state after the end of conversions. This is the 14th, 11th, or ninth SCLK rising edge for the 12-, 10-, and 8-bit devices, respectively. The clock may be stopped after the 14th SCLK falling edge; however, it is recommended to stop the clock after the 16th SCLK falling edge. Note that it is mandatory not to have more than 29 SCLK falling edges during the $\overline{CS}$ low period. This limitation ensures that the devices remain in 16-clock mode.

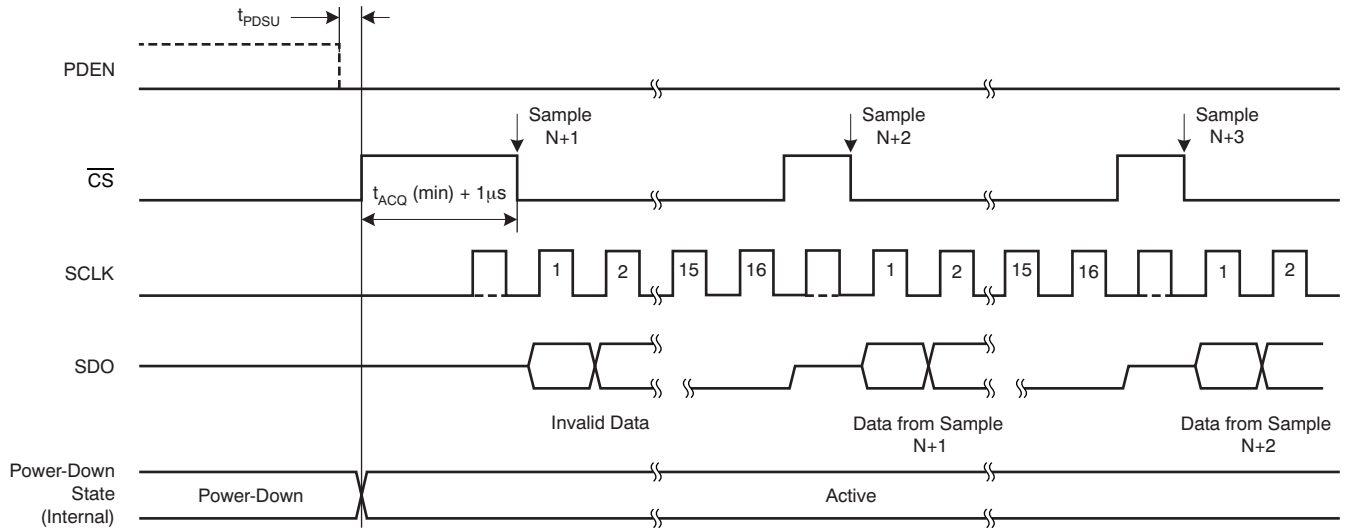


Figure 51. Exit From Power-Down with 16-Clock Burst Mode

The devices remain in a power-down state as long as $\overline{CS}$ is low. A $\overline{CS}$ rising edge with PDEN = 0 brings the devices out of the power-down state. It is necessary to ensure that the $\overline{CS}$ high time for the first sample after power up is more than 1µs + t_{ACQ} (min).

APPLICATION INFORMATION

The device employs a sample-and-hold stage at the input; see Figure 39 for a typical equivalent circuit of a sample-and-hold stage. The device connects a 32pF sampling capacitor during sampling. This configuration results in a glitch at the input terminals of the device at the start of the sample. The external circuit must be designed in such a way that the input can settle to the required accuracy during the sampling time chosen. Figure 52 shows a typical driving circuit for the analog inputs.

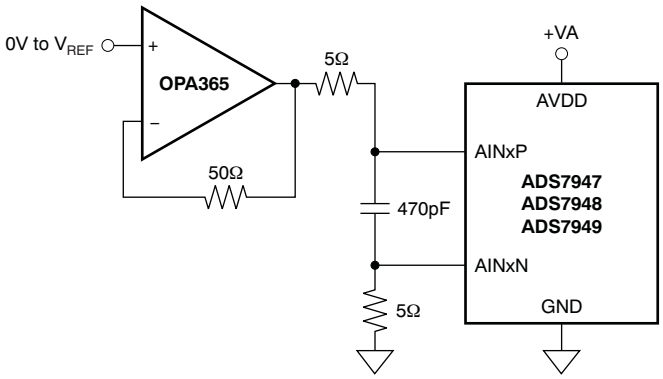


Figure 52. Typical Input Driving Circuit

The 470pF capacitor across the AINxP and AINxN terminals decouples the driving op amp from the sampling glitch. It is recommended to split the series resistance of the input filter in two equal values as shown in Figure 52. It is recommended that both input terminals see the same impedance from the external circuit. The low-pass filter at the input limits noise bandwidth of the driving op amp. Select the filter bandwidth so that the full-scale step at the input can settle to the required accuracy during the sampling time. Equation 1, Equation 2, and Equation 3 are useful for filter component selection.

$$\text{Filter Time Constant } (t_{AU}) = \frac{\text{Sampling Time}}{\text{Settling Resolution} \times \ln(2)}$$

Where:

Settling resolution is the accuracy in LSB to which the input needs to settle. A typical settling resolution for the 12-bit device is 13 or 14. (1)

$$\text{Filter Time Constant } (t_{AU}) = R \times C \quad (2)$$

$$\text{Filter Bandwidth} = \frac{1}{2 \times \pi \times t_{AU}} \quad (3)$$

Also, make sure the driving op amp bandwidth does not limit the signal bandwidth below filter bandwidth. In many applications, signal bandwidth may be much lower than filter bandwidth. In this case, an additional low-pass filter may be used at the input of the driving op amp. This signal filter bandwidth can be selected in accordance with the input signal bandwidth.

DRIVING AN ADC WITHOUT A DRIVING OP AMP

There are some low input signal bandwidth applications, such as battery power monitoring or mains monitoring. For these applications, it is not required to operate an ADC at high sampling rates and it is desirable to avoid using a driving op amp from a cost perspective. In this case, the ADC input sees the impedance of the signal source (such as a battery or mains transformer). This section elaborates the effects of source impedance on sampling frequency.

Equation 1 can be rewritten as Equation 4:

Sampling Time = Filter Time Constant × Settling Resolution × ln(2) (4)

As shown in Figure 53, it is recommended to use a bypass capacitor across the positive and negative ADC input terminals.

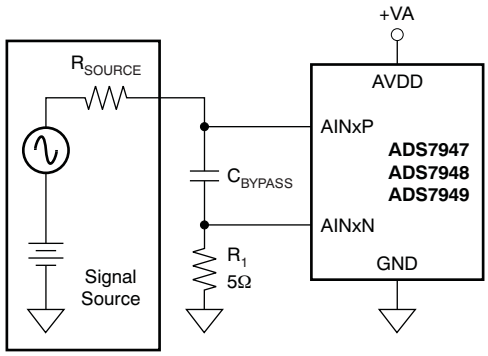


Figure 53. Driving an ADC Without a Driving Op Amp

Source impedance (R_{SOURCE} + R_1) with (C_{BYPASS} + C_{SAMPLE}) acts as a low-pass filter with Equation 5:

Filter Time Constant = (R_{SOURCE} + R_1) × (C_{BYPASS} + C_{SAMPLE})

Where:

C_{SAMPLE} is the internal sampling capacitance of the ADC (equal to 32pF). (5)

Table 1 lists the recommended bypass capacitor values and the filter time constant for different source resistances. It is recommended to use a 10pF bypass capacitor, at minimum.

Table 1. Filter Time Constant versus Source Resistance

R_{SOURCE} (Ω)	R_{SOURCE} + R_1	APPROXIMATE C_{BYPASS} (pF)	C_{BYPASS} + C_{SAMPLE} (pF)	FILTER TIME CONSTANT (ns)
15	20	370	400	8
25	30	235	267	8
50	55	115	145	8
100	105	44	76	8
180	185	10	43.2	8
250	255	10	42	10.7
1000	1005	10	42	42.2
5000	5005	10	42	210.2

Typically, settling resolution is selected as (ADC resolution + 2). For the ADS7947 (12-bit) the ideal settling resolution is 14. Using equations Equation 2 and Equation 3, the sampling time can be easily determined for a given source impedance. This allows 80ns of sampling time for a 12-bit ADC with 8ns of filter time constant, which matches the ADS7947 specifications. For source impedance above 180Ω, the filter time constant continues to increase beyond the 8ns required for an 80ns sampling time. This increases the minimum permissible sampling time for 12-bit settling and the device must be operated at a lower sampling rate.

The device sampling rate can be maximized by using a 34MHz clock even for lower throughputs. Table 2 shows typical calculations for the ADS7947(12-bit).

Table 2. Sampling Frequency versus Source Impedance for the ADS7947 (12-Bit)

R_{SOURCE} (Ω)	C_{BYPASS} (pF)	SAMPLING TIME, t_{ACQ} (ns)	CONVERSION TIME, t_{CONV} (ns)	CYCLE TIME, t_{ACQ} + t_{CONV} (ns)	SAMPLING RATE (MSPS)
180	10	80	397 (with 34MHz clock)	477	2
250	10	107	397 (with 34MHz clock)	504	1.98
1000	10	422	397 (with 34MHz clock)	819	1.2
5000	10	2102	397 (with 34MHz clock)	2499	0.4

It is necessary to allow 1000ns additional sampling time over what is shown in Table 2 if PDEN (pin 12) is set high.

PCB LAYOUT/SCHEMATIC GUIDELINES

ADCs are mixed-signal devices. For maximum performance, proper decoupling, grounding, and proper termination of digital signals is essential. Figure 54 shows the essential components around the ADC. All capacitors shown are ceramic. These decoupling capacitors must be placed close to the respective signal pins.

There is a 47Ω *source series termination* resistor shown on the SDO signal. This resistor must be placed as close to pin 15 as possible. Series terminations for SCLK and $\overline{CS}$ must be placed close to the host.

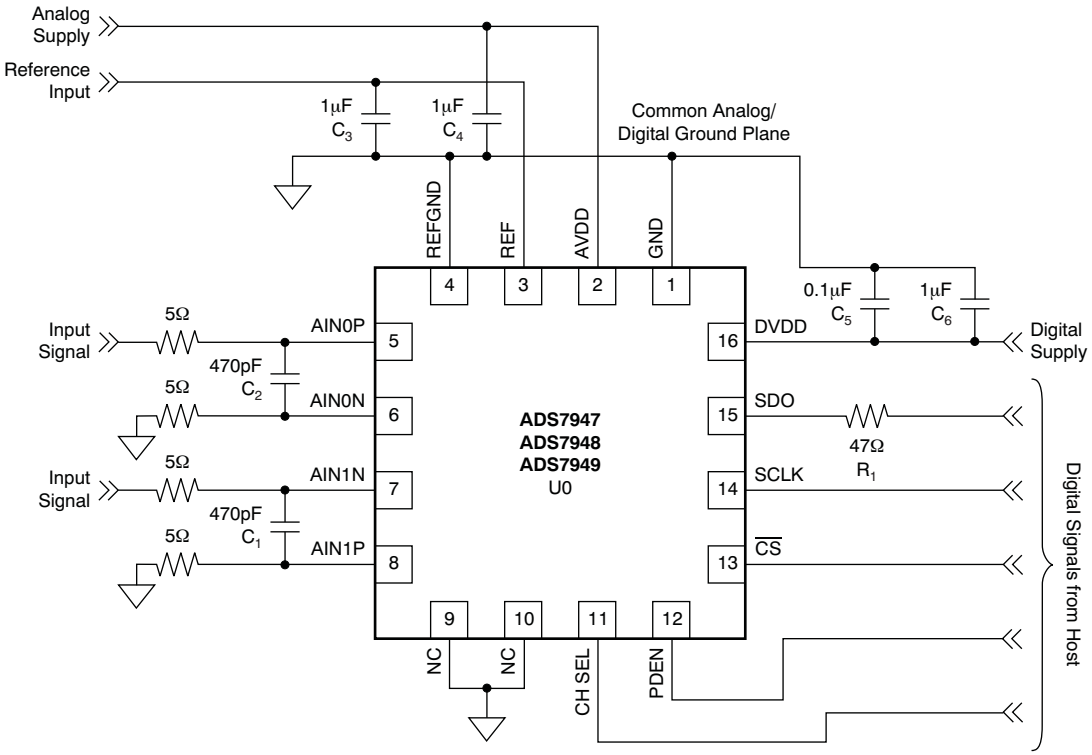


Figure 54. Recommended ADC Schematic

A common ground plane for both analog and digital often gives better results. Typically, the second PCB layer is the ground plane. The ADC ground pins are returned to the ground plane through multiple vias (PTH). It is a good practice to place analog components on one side and digital components on other side of the ADC (or ADCs). All signals must be routed, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then short both grounds to form a common ground plane. Figure 55 shows a typical layout around the ADC.

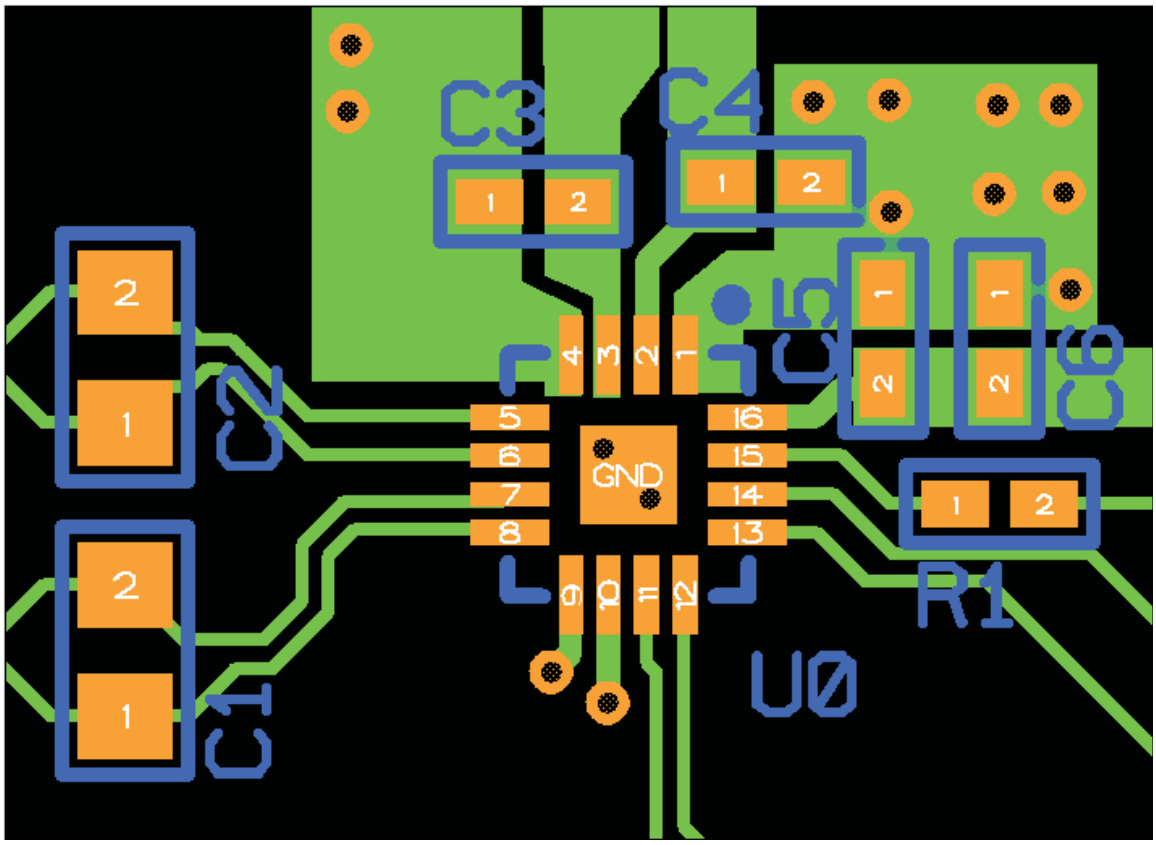


Figure 55. Recommended ADC Layout
(Only top layer is shown, second layer is common ground for analog and digital.)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7947SRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7947	Samples
ADS7947SRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7947	Samples
ADS7948SRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7948	Samples
ADS7948SRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7948	Samples
ADS7949SRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7949	Samples
ADS7949SRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7949	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

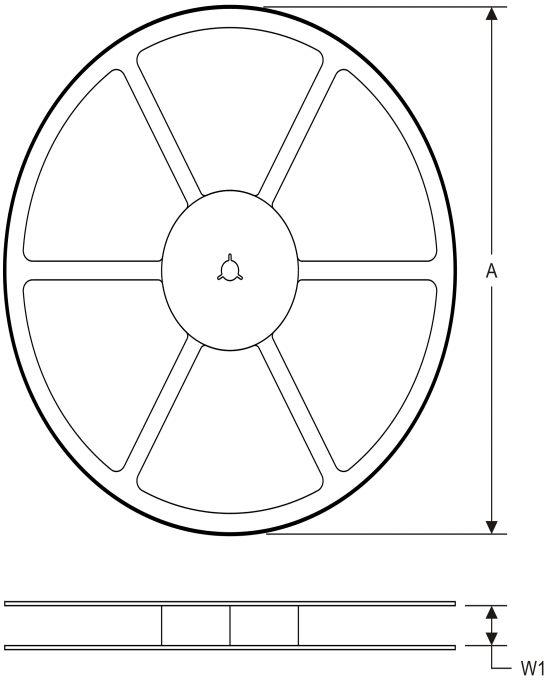
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

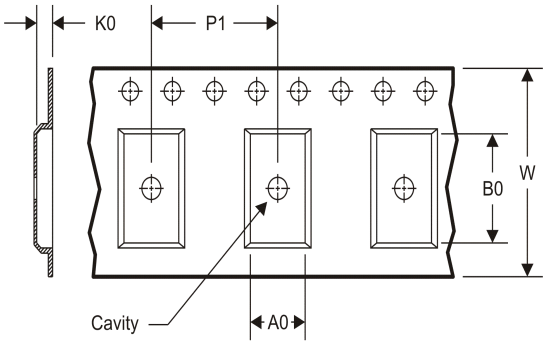
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



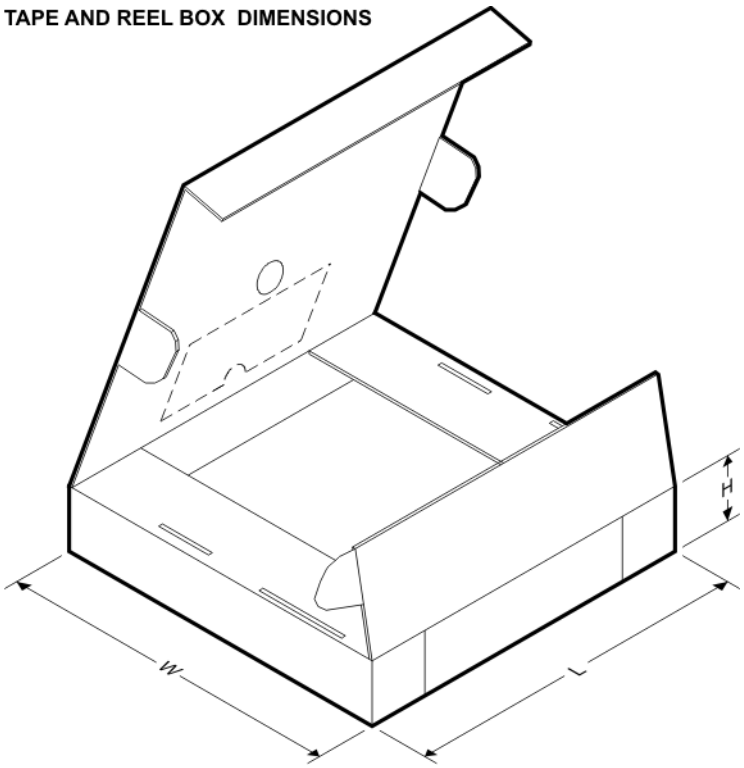
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7947SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7947SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7948SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7948SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7949SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7949SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

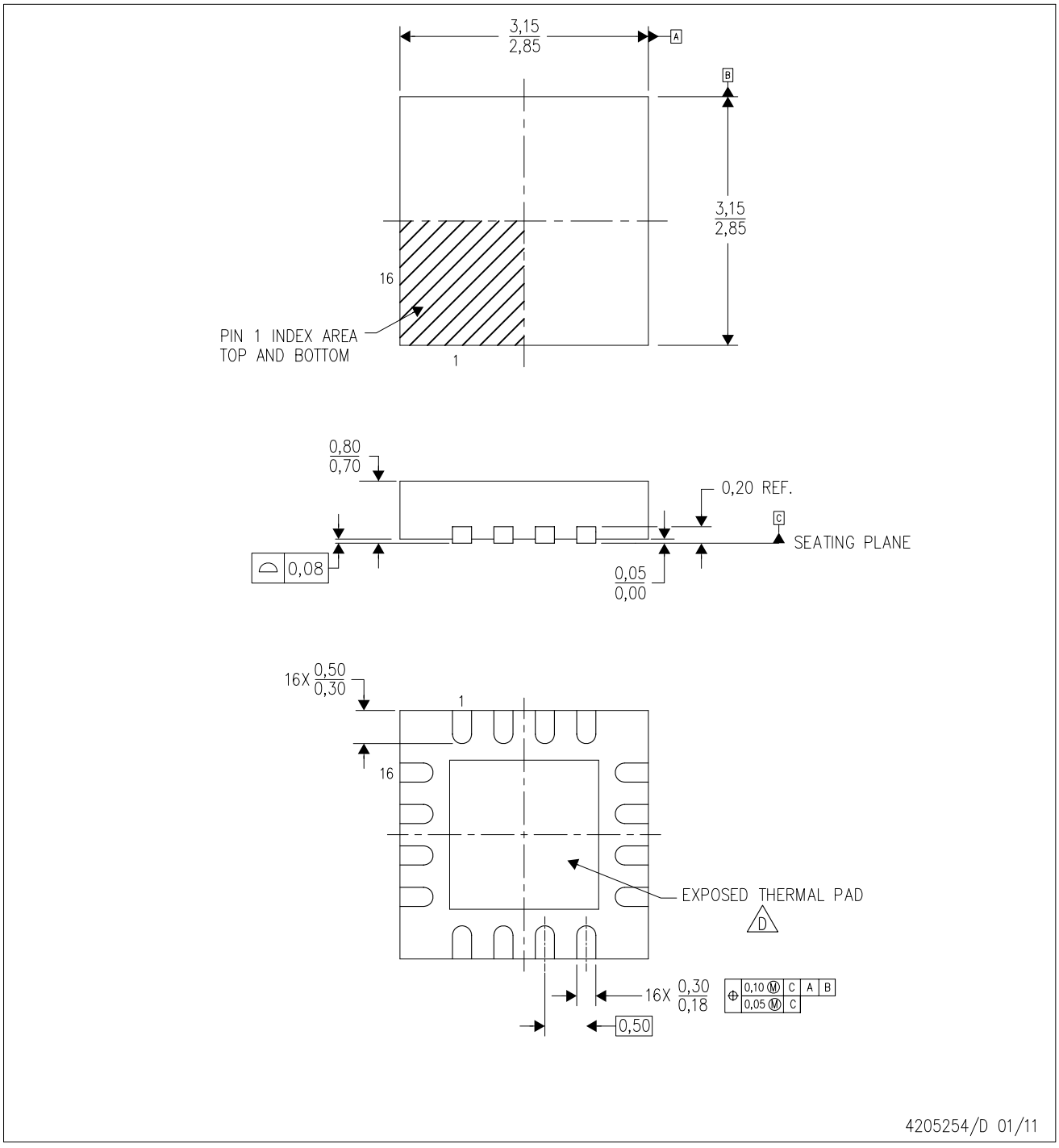
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7947SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7947SRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7948SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7948SRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7949SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7949SRTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

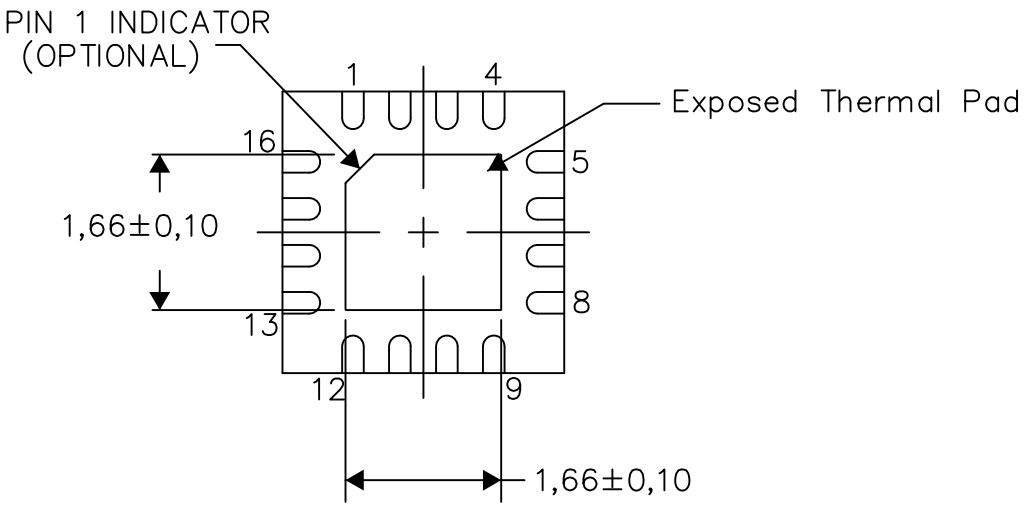
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



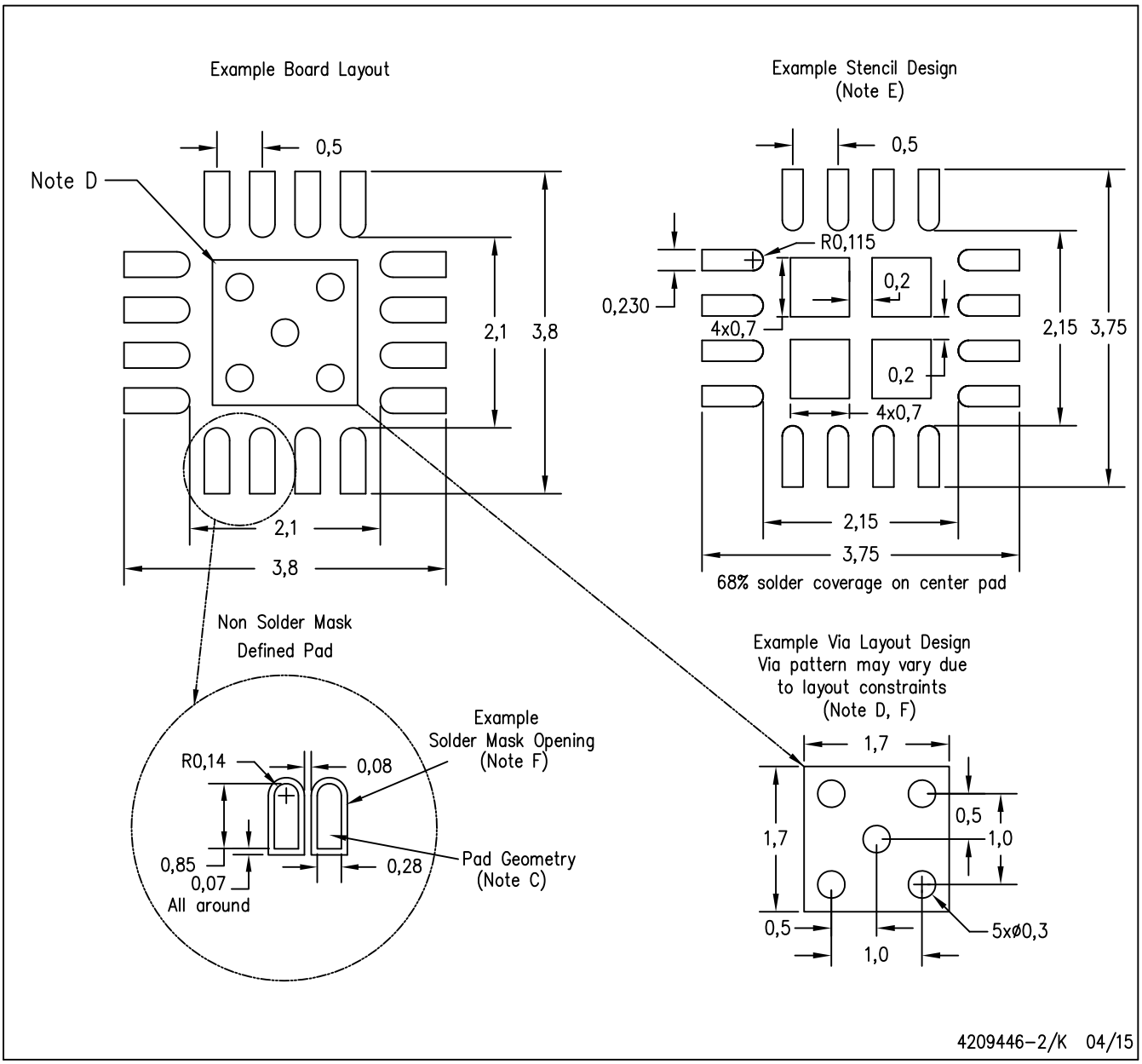
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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