



## 12-BIT 250-KSPS SAMPLING CMOS ANALOG-TO-DIGITAL CONVERTER

#### **FEATURES**

- 250-kHz Sampling Rate
- Standard ±10-V Input Range
- 73-dB SINAD With 45-kHz Input
- ±0.45 LSB Max INL
- ±0.45 LSB Max DNL
- 12 Bit No Missing Code
- ±1 LSB Bipolar Zero Errors
- ±0.4 PPM/°C Bipolar Zero Error Drift
- Single 5-V Supply Operation
- Pin-Compatible With ADS7804/05 (Low Speed) and 16-Bit ADS8505
- Uses Internal or External Reference
- Full Parallel Data Output
- 70-mW Typ Power Dissipation at 250 KSPS
- 28-Pin SOIC Package

#### **APPLICATIONS**

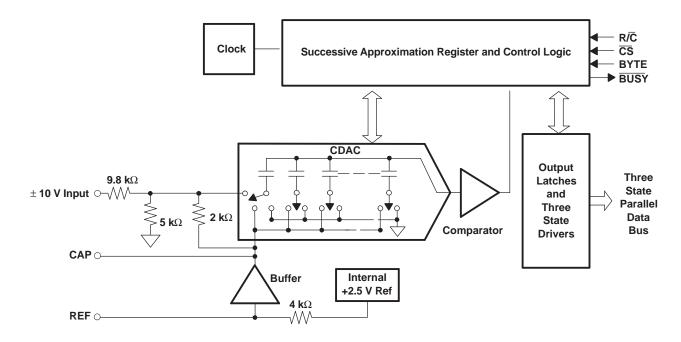
- Industrial Process Control
- Data Acquisition Systems
- Digital Signal Processing
- Medical Equipment
- Instrumentation

#### DESCRIPTION

The ADS8504 is a complete 12-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 12-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and 3-state output drivers.

The ADS8504 is specified at a 250-kHz sampling rate over the full temperature range. Precision resistors provide an industry standard ±10-V input range, while the innovative design allows operation from a single +5-V supply, with power dissipation under 100 mW.

The ADS8504 is available in a 28-pin SOIC package and is fully specified for operation over the industrial -40°C to 85°C temperature range.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### PACKAGE/ORDERING INFORMATION(1)

| PRODUCT   | MINIMUM<br>RELATIVE<br>ACCURACY<br>(LSB) | NO<br>MISSING<br>CODE | MINIMUM<br>SINAD<br>(dB) | SPECIFICATION<br>TEMPERATURE<br>RANGE PACKAGE<br>LEAD |       | PACKAGE<br>DESIGNATOR | ORDERING<br>NUMBER | TRANSPORT<br>MEDIA, QTY |
|-----------|--|-----------------------|--------------------------|---|-------|-----------------------|--------------------|-------------------------|
| ADS0E04ID | ±0.45                                    | 12                    | 72                       | -40°C to 85°C   | SO-28 | DW                    | ADS8504IBDW        | Tube, 20                |
| ADS8504IB | ±0.45                                    | ±0.45 12              | 12                       | -40 C to 65 C   | 30-26 | DVV                   | ADS8504IBDWR       | Tape and Reel, 1000     |

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

### ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)(2)

|                              |                                      | ADS8504   |
|------------------------------|--------------------------------------|---|
| Analog inputs                | V <sub>IN</sub>                      | ±25V  |
|                              | CAP                                  | +V <sub>ANA</sub> + 0.3 V to AGND2 - 0.3 V                  |
|                              | REF                                  | Indefinite short to AGND2, momentary short to $V_{\rm ANA}$ |
| Ground voltage differences   | DGND, AGND1, AGND2                   | ±0.3 V  |
|                              | V <sub>ANA</sub>                     | 6 V   |
|                              | V <sub>DIG</sub> to V <sub>ANA</sub> | 0.3 V   |
|                              | $V_{DIG}$                            | 6 V   |
| Digital inputs               |                                      | -0.3 V to +V <sub>DIG</sub> + 0.3 V                         |
| Maximum junction temperatu   | re                                   | 165°C   |
| Internal power dissipation   |                                      | 825 mW  |
| Lead temperature (soldering, | 1,6mm from case, 10 seconds)         | 260°C   |

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

 $T_A = -40^{\circ}C$  to 85°C,  $f_s = 250$  kHz,  $V_{DIG} = V_{ANA} = 5$  V, using internal reference (unless otherwise noted)

|       | PARAMETER                       | TEST CONDITIONS     | MIN   | TYP  | MAX  | UNIT               |
|-------|---------------------------------|---------------------|-------|------|------|--------------------|
|       | Resolution                      |                     |       |      | 12   | Bits               |
| ANALO | OG INPUT                        |                     |       |      |      |                    |
|       | Voltage range                   |                     |       | ±10  |      | V                  |
|       | Impedance                       |                     |       | 11.5 |      | kΩ                 |
|       | Capacitance                     |                     |       | 50   |      | pF                 |
| THROU | IGHPUT SPEED                    |                     |       |      |      |                    |
|       | Conversion cycle                | Acquire and convert |       |      | 4    | μs                 |
|       | Throughput rate                 |                     | 250   |      |      | kHz                |
| DC AC | CURACY                          |                     |       |      |      |                    |
| INL   | Integral linearity error        |                     | -0.45 |      | 0.45 | LSB <sup>(1)</sup> |
| DNL   | Differentiall linearity error   |                     | -0.45 |      | 0.45 | LSB <sup>(1)</sup> |
|       | No missing codes                |                     | 12    |      |      | Bits               |
|       | Transition noise <sup>(2)</sup> |                     |       | 0.1  |      | LSB                |

<sup>(1)</sup> LSB means least significant bit. For the 12-bit, ±10-V input ADS8504, one LSB is 4.88 mV.

<sup>(2)</sup> All voltage values are with respect to network ground terminal.

<sup>(2)</sup> Typical rms noise at worst case transitions and temperatures.



## **ELECTRICAL CHARACTERISTICS (continued)**

 $T_A = -40^{\circ}C$  to 85°C,  $f_s = 250$  kHz,  $V_{DIG} = V_{ANA} = 5$  V, using internal reference (unless otherwise noted)

|                 | PARAMETER  | TEST CONDITIONS  | MIN   | TYP  | MAX                     | UNIT              |
|-----------------|--|--|-------|------|-------------------------|-------------------|
|                 | Full-scale error <sup>(3)(4)</sup>   | Int. Ref.  | -0.25 |      | 0.25                    | %FSR              |
|                 | Full-scale error drift   | Int. Ref.  |       | ±7   |                         | ppm/°C            |
|                 | Full-scale error <sup>(3)(4)</sup>   | Ext. 2.5-V Ref.  | -0.25 |      | 0.25                    | %FSR              |
|                 | Full-scale error drift   | Ext. 2.5-V Ref.  |       | ±2   |                         | ppm/°C            |
|                 | Bipolar zero error <sup>(3)</sup>  |  | -1    |      | 1                       | LSB               |
|                 | Bipolar zero error drift   |  |       | ±0.4 |                         | ppm/°C            |
|                 | Power supply sensitivity (V <sub>DIG</sub> = V <sub>ANA</sub> = V <sub>D</sub> ) | +4.75 V < V <sub>D</sub> < +5.25 V                     | -0.5  |      | 0.5                     | LSB               |
| AC ACC          | URACY  |  |       |      |                         |                   |
| SFDR            | Spurious-free dynamic range  | f <sub>I</sub> = 45 kHz                                | 86    | 94   |                         | dB <sup>(5)</sup> |
| THD             | Total harmonic distortion  | f <sub>I</sub> = 45 kHz                                |       | -95  | -86                     | dB                |
| OINIAD          | O'constitute (asiana distantian)   | f <sub>I</sub> = 45 kHz                                | 72    | 73   |                         | dB                |
| SINAD           | Signal-to-(noise+distortion)   | -60-dB Input   |       | 32   |                         | dB                |
| SNR             | Signal-to-noise ratio  | f <sub>I</sub> = 45 kHz                                | 72    | 73   |                         | dB                |
|                 | Full-power bandwidth <sup>(6)</sup>  |  |       | 500  |                         | kHz               |
| SAMPLII         | NG DYNAMICS  |  |       |      | •                       |                   |
|                 | Aperture delay   |  |       | 5    |                         | ns                |
|                 | Transient response   | FS Step  |       |      | 2                       | μs                |
|                 | Overvoltage recovery <sup>(7)</sup>  |  |       | 150  |                         | ns                |
| REFERE          | NCE  |  |       |      | •                       |                   |
|                 | Internal reference voltage   |  | 2.48  | 2.5  | 2.52                    | V                 |
|                 | Internal reference source current (must use external buffer)                     |  |       | 1    |                         | μΑ                |
|                 | Internal reference drift   |  |       | 8    |                         | ppm/°C            |
|                 | External reference voltage range for specified linearity                         |  | 2.3   | 2.5  | 2.7                     | V                 |
|                 | External reference current drain   | Ext. 2.5-V Ref.  |       |      | 100                     | μΑ                |
| DIGITAL         | INPUTS   |  |       |      |                         |                   |
|                 | Logic levels   |  |       |      |                         |                   |
| V <sub>IL</sub> | Low-level input voltage  |  | -0.3  |      | 0.8                     | V                 |
| V <sub>IH</sub> | High-level input voltage   |  | 2.0   |      | V <sub>DIG</sub> +0.3 V | V                 |
| I <sub>IL</sub> | Low-level input current  |  |       |      | ±10                     | μΑ                |
| I <sub>IH</sub> | High-level input current   |  |       |      | ±10                     | μΑ                |
| DIGITAL         | OUTPUTS  |  |       |      |                         |                   |
|                 | Data format (Parallel 12-bits)   |  |       |      |                         |                   |
|                 | Data coding (Binary 2's complement)  |  |       |      |                         |                   |
| V <sub>OL</sub> | Low-level output voltage   | I <sub>SINK</sub> = 1.6 mA                             |       |      | 0.4                     | V                 |
| V <sub>OH</sub> | High-level output voltage  | I <sub>SOURCE</sub> = 500 μA                           | 4     |      |                         | V                 |
|                 | Leakage current  | Hi-Z state, V <sub>OUT</sub> = 0 V to V <sub>DIG</sub> |       |      | ±5                      | μΑ                |
|                 | Output capacitance   | Hi-Z state   |       |      | 15                      | pF                |
| DIGITAL         | TIMING   | 1  |       |      |                         |                   |
|                 | Bus access timing  |  |       |      | 83                      | ns                |

<sup>(3)</sup> As measured with fixed resistors shown in Figure 24. Adjustable to zero with external potentiometer.

<sup>(4)</sup> Full-scale error is the worst case of -full-scale or +full-scale deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.

<sup>(5)</sup> All specifications in dB are referred to a full-scale ±10-V input.

<sup>(6)</sup> Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB, or 10 bits of accuracy.

<sup>(7)</sup> Recovers to specified performance after 2 x FS input overvoltage.



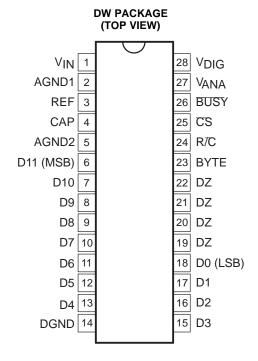
## **ELECTRICAL CHARACTERISTICS (continued)**

 $T_A = -40$ °C to 85°C,  $f_S = 250$  kHz,  $V_{DIG} = V_{ANA} = 5$  V, using internal reference (unless otherwise noted)

|                  | PARAMETER                        | TEST CONDITIONS            | MIN  | TYP | MAX  | UNIT |
|------------------|----------------------------------|----------------------------|------|-----|------|------|
|                  | Bus relinquish timing            |                            |      |     | 83   | ns   |
| POWER            | R SUPPLIES                       |                            |      |     |      |      |
| $V_{DIG}$        | Digital input voltage            |                            | 4.75 | 5   | 5.25 | V    |
| V <sub>ANA</sub> | Analog input voltage             | Must be < V                | 4.75 | 5   | 5.25 | V    |
| I <sub>DIG</sub> | Digital input current            | Must be ≤ V <sub>ANA</sub> |      | 4   |      | mA   |
| I <sub>ANA</sub> | Analog input current             |                            |      | 10  |      | mA   |
|                  | Power dissipation                | f <sub>S</sub> = 250 kHz   |      | 70  | 100  | mW   |
| TEMPE            | RATURE RANGE                     | ,                          | •    |     | •    |      |
|                  | Specified performance            |                            | -40  |     | 85   | °C   |
|                  | Derated performance (8)          |                            | -55  |     | 125  | °C   |
|                  | Storage                          |                            | -65  |     | 150  | °C   |
| THERM            | AL RESISTANCE (⊝ <sub>JA</sub> ) | -1                         | 1    |     |      |      |
|                  | SO                               |                            |      | 46  |      | °C/W |

<sup>(8)</sup> The internal reference may not be started correctly beyond the industrial temperature range (-40°C to 85°C), therefore use of an external reference is recommended.

#### **DEVICE INFORMATION**





## **DEVICE INFORMATION (continued)**

## **Terminal Functions**

| TERI             | MINAL  | DIGITAL | DECODIDATION   |
|------------------|--------|---------|--|
| NAME             | DW NO. | 1/0     | DESCRIPTION  |
| AGND1            | 2      |         | Analog ground. Used internally as ground reference point.  |
| AGND2            | 5      |         | Analog ground.   |
| BUSY             | 26     | 0       | At the start of a conversion, BUSY goes low and stays low until the conversion is completed and the digital outputs have been updated.   |
| BYTE             | 23     | I       | Selects 8 most significant bits (low) or 8 least significant bits (high).  |
| CAP              | 4      |         | Reference buffer capacitor. 2.2-μF tantalum capacitor to ground.   |
| CS               | 25     | I       | Internally ORed with R/C. If R/C low, a falling edge on CS initiates a new conversion.   |
| DGND             | 14     |         | Digital ground.  |
| D11 (MSB)        | 6      | 0       | Data bit 11. Most significant bit (MSB) of conversion results. Hi-Z state when $\overline{\text{CS}}$ is high, or when $R/\overline{C}$ is low.  |
| D10              | 7      | 0       | Data bit 10. Hi-Z state when $\overline{CS}$ is high, or when R/ $\overline{C}$ is low.  |
| D9               | 8      | 0       | Data bit 9. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| D8               | 9      | 0       | Data bit 8. Hi-Z state when CS is high, or when R/C is low.  |
| D7               | 10     | 0       | Data bit 7. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| D6               | 11     | 0       | Data bit 6. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| D5               | 12     | 0       | Data bit 5. Hi-Z state when CS is high, or when R/C is low.  |
| D4               | 13     | 0       | Data bit 4. Hi-Z state when CS is high, or when R/C is low.  |
| D3               | 15     | 0       | Data bit 3. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| D2               | 16     | 0       | Data bit 2. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| D1               | 17     | 0       | Data bit 1. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| D0 (LSB)         | 18     | 0       | Data bit 0. Least significant bit (LSB) of conversion results. Hi-Z state when $\overline{\text{CS}}$ is high, or when $R/\overline{\text{C}}$ is low.   |
| DZ               | 19     | 0       | Low when $\overline{\text{CS}}$ low, R/ $\overline{\text{C}}$ high. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| DZ               | 20     | 0       | Low when $\overline{\text{CS}}$ low, R/ $\overline{\text{C}}$ high. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| DZ               | 21     | 0       | Low when $\overline{\text{CS}}$ low, R/ $\overline{\text{C}}$ high. Hi-Z state when $\overline{\text{CS}}$ is high, or when R/ $\overline{\text{C}}$ is low.   |
| DZ               | 22     | 0       | Low when $\overline{CS}$ low, R/ $\overline{C}$ high. Hi-Z state when $\overline{CS}$ is high, or when R/ $\overline{C}$ is low.   |
| R/C              | 24     | I       | With $\overline{CS}$ low and $\overline{BUSY}$ high, a falling edge on R/ $\overline{C}$ initiates a new conversion. With $\overline{CS}$ low, a rising edge on R/ $\overline{C}$ enables the parallel output. |
| REF              | 3      |         | Reference input/output. 2.2-μF tantalum capacitor to ground.   |
| V <sub>ANA</sub> | 27     |         | Analog supply input. Nominally +5 V. Decouple to ground with 0.1-μF ceramic and 10-μF tantalum capacitors.   |
| $V_{DIG}$        | 28     |         | Digital supply input. Nominally +5 V. Connect directly to pin 27. Must be $\leq$ V <sub>ANA</sub> .  |
| V <sub>IN</sub>  | 1      |         | Analog input.  |



## **Typical Characteristics**

# SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

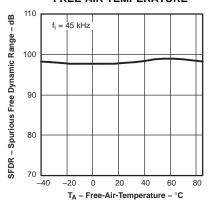


Figure 1.

## TOTAL HARMONIC DISTORTION VS FREE-AIR TEMPERATURE

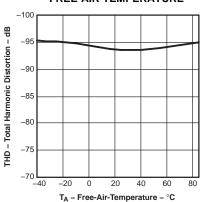


Figure 2.

SIGNAL-TO-NOISE RATIO VS FREE-AIR TEMPERATURE

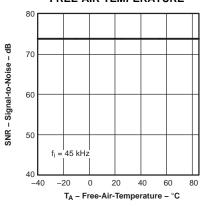


Figure 3.

SIGNAL-TO-NOISE AND DISTORTION



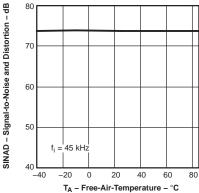


Figure 4.

## SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

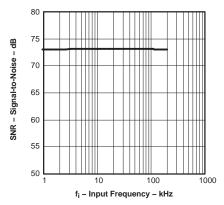


Figure 5.

#### SIGNAL-TO-NOISE AND DISTORTION VS INPUT FREQUENCY

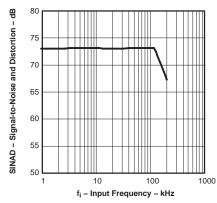


Figure 6.

# SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

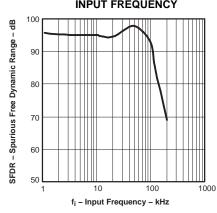


Figure 7.

## TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

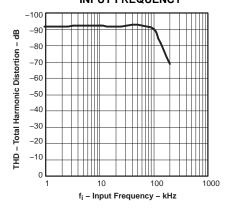


Figure 8.

#### BIPOLAR ZERO ERROR VS FREE-AIR TEMPERATURE

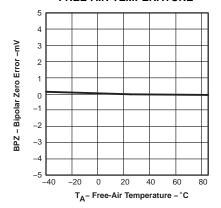
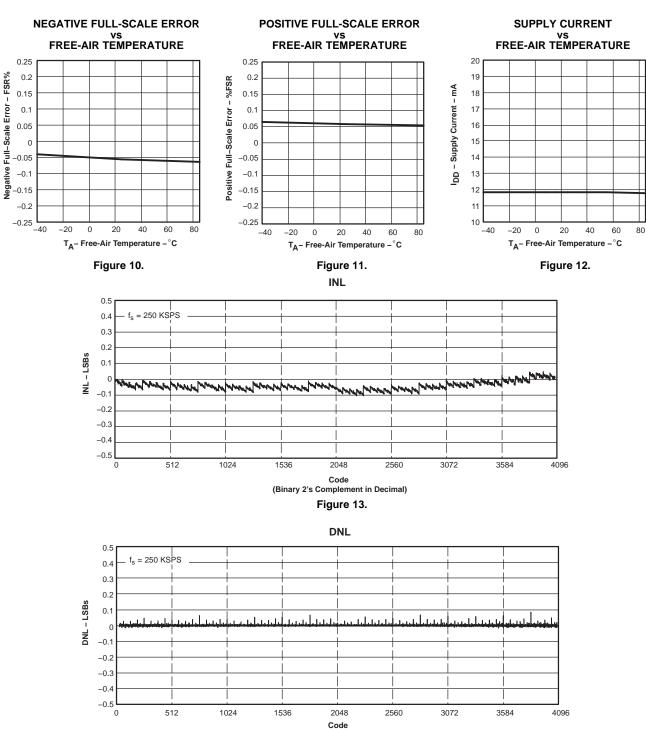


Figure 9.

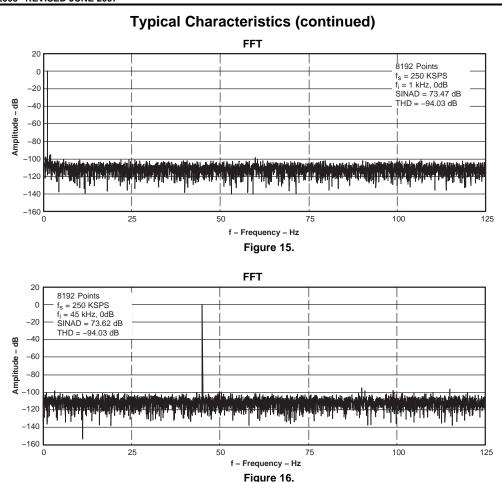


## **Typical Characteristics (continued)**



(Binary 2's Complement in Decimal) Figure 14.





#### **BASIC OPERATION**

Figure 17 shows a basic circuit to operate the ADS8504 with a full parallel data output. Taking  $R/\overline{C}$  (pin 24) low for a minimum of 40 ns (1.75 µs max if  $\overline{BUSY}$  is used to latch the data) initiates a conversion.  $\overline{BUSY}$  (pin 26) goes low and stays low until the conversion is completed and the output registers are updated. Data is output in binary 2's complement with the MSB on pin 6.  $\overline{BUSY}$  going high can be used to latch the data.

The ADS8504 begins tracking the input signal at the end of the conversion. Allowing 4 μs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the Calibration section).

#### STARTING A CONVERSION

The combination of  $\overline{CS}$  (pin 25) and  $R/\overline{C}$  (pin 24) low for a minimum of 40 ns immediately puts the sample/hold of the ADS8504 in the hold state and starts conversion n.  $\overline{BUSY}$  (pin 26) goes low and stays low until conversion n is completed and the internal output register has been updated. All new convert commands during  $\overline{BUSY}$  low will abort the conversion in progress and reset the ADC (see Figure 22).

The ADS8504 begins tracking the input signal at the end of the conversion. Allowing 4  $\mu$ s between convert commands assures accurate acquisition of a new signal. Refer to Table 1 for a summary of  $\overline{CS}$ ,  $R/\overline{C}$ , and  $\overline{BUSY}$  states and Figure 19, Figure 20, and Figure 21 for the timing diagrams.



#### **BASIC OPERATION (continued)**

 $\overline{\text{CS}}$  and  $\overline{\text{R/C}}$  are internally ORed and level triggered. There is not a requirement which input goes low first when initiating a conversion. If, however, it is critical that  $\overline{\text{CS}}$  or  $\overline{\text{R/C}}$  initiates conversion n, be sure the less critical input is low at least 10 ns prior to the initiating input.

To reduce the number of control pins,  $\overline{CS}$  can be tied low using R/ $\overline{C}$  to control the read and convert modes. The parallel output becomes active whenever R/ $\overline{C}$  goes high. Refer to the READING DATA section.

| CS           | R/C      | BUSY | OPERATION   |
|--------------|----------|------|---|
| 1            | Х        | Х    | None. Databus is in Hi-Z state.   |
| <b>\</b>     | 0        | 1    | Initiates conversion <i>n</i> . Databus remains in Hi-Z state.  |
| 0            | <b>\</b> | 1    | Initiates conversion <i>n</i> . Databus enters Hi-Z state.  |
| 0            | 1        | 1    | Conversion <i>n</i> completed. Valid data from conversion <i>n</i> on the databus.  |
| $\downarrow$ | 1        | 1    | Enables databus with valid data from conversion <i>n</i> .  |
| <b>\</b>     | 1        | 0    | Enables databus with valid data from conversion $n-1$ <sup>(1)</sup> . Conversion $n$ in progress.                            |
| 0            | 1        | 0    | Enables databus with valid data from conversion $n-1$ <sup>(1)</sup> . Conversion $n$ in progress.                            |
| 0            | 0        | 1    | Data is invalid. $\overline{\text{CS}}$ and/or R/ $\overline{\text{C}}$ must be high when $\overline{\text{BUSY}}$ goes high. |
| Х            | <b>\</b> | 0    | Conversion n is halted. Causes ADC to reset. (2)  |

Table 1. Control Line Functions for Read and Convert

- (1) See Figure 19 and Figure 20 for constraints on data valid from conversion n-1.
- (2) See Figure 22 for details on ADC reset.

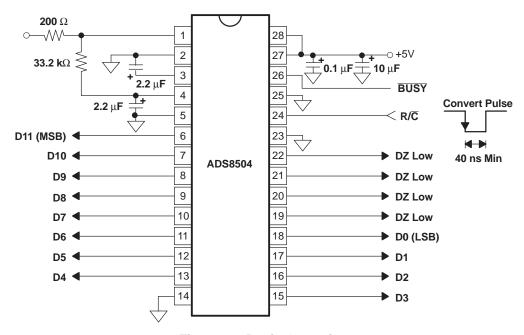


Figure 17. Basic Operation

#### **READING DATA**

The ADS8504 outputs full or byte-reading parallel data in binary 2's complement data output format. The parallel output is active when  $R/\overline{C}$  (pin 24) is high and  $\overline{CS}$  (pin 25) is low. Any other combination of  $\overline{CS}$  and  $R/\overline{C}$  3-states the parallel output. Valid conversion data can be read in a full parallel, 12-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table 2 for ideal output codes and Figure 18 for bit locations relative to the state of BYTE.



#### Table 2. Ideal Input Voltages and Output Codes

| DECORIDATION                | ANALOG INDUT | DIGITAL OUTPUT BINA | RY 2's COMPLEMENT |
|-----------------------------|--------------|---------------------|-------------------|
| DESCRIPTION                 | ANALOG INPUT | BINARY CODE         | HEX CODE          |
| Full-scale range            | ±10 V        |                     |                   |
| Least significant bit (LSB) | 4.88 mV      |                     |                   |
| Full scale (10 V-1 LSB)     | 9.99512 V    | 0111 1111 1111      | 7FF               |
| Midscale                    | 0 V          | 0000 0000 0000      | 000               |
| One LSB below midscale      | -4.88 mV     | 1111 1111 1111      | FFF               |
| -Full scale                 | -10 V        | 1000 0000 0000      | 800               |

### **PARALLEL OUTPUT (After a Conversion)**

After conversion n is completed and the output registers have been updated,  $\overline{\text{BUSY}}$  (pin 26) goes high. Valid data from conversion n is available on D11-D0 (pins 6-13 and 15-18).  $\overline{\text{BUSY}}$  going high can be used to latch the data. Refer to Table 3 and Figure 19, Figure 20, and Figure 21 for timing specifications.

#### PARALLEL OUTPUT (During a Conversion)

After conversion n has been initiated, valid data from conversion n-1 can be read and is valid up to  $t_2$  (2.2  $\mu$ s typ) after the start of conversion n. Do not attempt to read data from  $t_2$  (2.2  $\mu$ s typ) after the start of conversion n until  $\overline{\text{BUSY}}$  (pin 26) goes high; this may result in reading invalid data. Refer to Table 3 and Figure 19, Figure 20, and Figure 21 for timing specifications.

**Note:** For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tying  $\overline{CS}$  low while using the falling edge of R/ $\overline{C}$  to initiate conversions and the rising edge of R/ $\overline{C}$  to activate the output mode of the converter. See Figure 19.

**Table 3. Conversion Timing** 

| SYMBOL                               | DESCRIPTION   | MIN | TYP | MAX  | UNITS |
|--------------------------------------|---|-----|-----|------|-------|
| t <sub>w1</sub>                      | Pulse duration, convert                               | 40  |     | 1750 | ns    |
| t <sub>a</sub>                       | Access time, data valid after R/C low                 |     | 2.2 | 3.2  | μs    |
| t <sub>pd</sub>                      | Propagation delay time, BUSY from R/C low             |     | 15  | 25   | ns    |
| t <sub>w2</sub>                      | Pulse duration, BUSY low                              |     |     | 2.2  | μs    |
| t <sub>d1</sub>                      | Delay time, BUSY after end of conversion              |     | 5   |      | ns    |
| t <sub>d2</sub>                      | Delay time, aperture                                  |     | 5   |      | ns    |
| t <sub>conv</sub>                    | Conversion time                                       |     |     | 2.2  | μs    |
| t <sub>acq</sub>                     | Acquisition time                                      | 1.8 |     |      | μs    |
| t <sub>dis</sub>                     | Disable time, bus                                     | 10  | 30  | 83   | ns    |
| t <sub>d3</sub>                      | Delay time, BUSY after data valid                     | 35  | 50  |      | ns    |
| t <sub>v</sub>                       | Valid time, previous data remains valid after R/C low | 1.5 | 2   |      | μs    |
| t <sub>conv</sub> + t <sub>acq</sub> | Throughput time                                       |     |     | 4    | μs    |
| t <sub>su</sub>                      | Setup time, R/C to CS                                 | 10  |     |      | ns    |
| t <sub>c</sub>                       | Cycle time between conversions                        | 4   |     |      | μs    |
| t <sub>en</sub>                      | Enable time, bus                                      | 10  | 30  | 83   | ns    |
| t <sub>d4</sub>                      | Delay time, BYTE                                      | 5   | 10  | 30   | ns    |



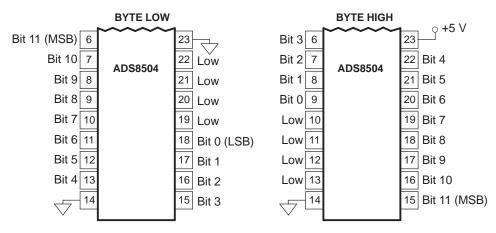


Figure 18. Bit Locations Relative to State of BYTE (Pin 23)

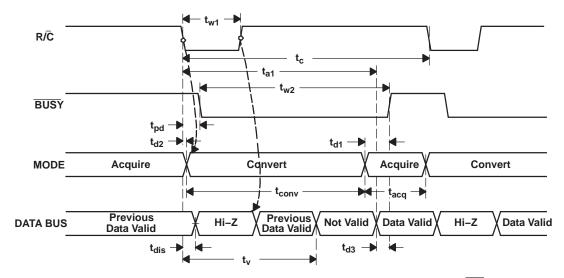


Figure 19. Conversion Timing with Outputs Enabled after Conversion (CS Tied Low)

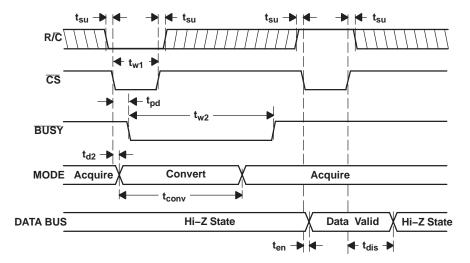


Figure 20. Using CS to Control Conversion and Read Timing



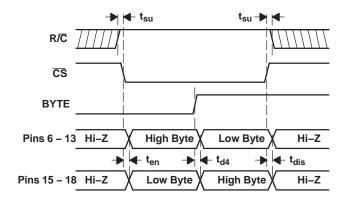


Figure 21. Using CS and BYTE to Control Data Bus

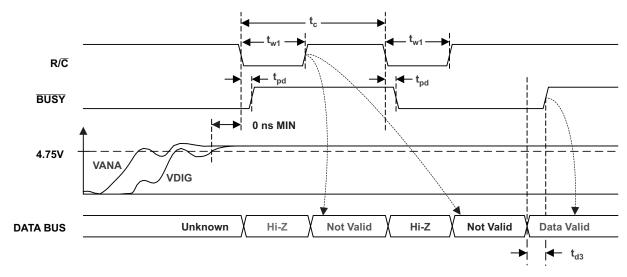


Figure 22. ADC Reset

#### **ADC RESET**

The ADC reset function of the ADS8504 can be used to terminate the current conversion cycle. Bringing  $R/\overline{C}$  low for at least 40 ns while BUSY is low will initiate the ADC reset. To initiate a new conversion,  $R/\overline{C}$  must return to the high state and remain high long enough to acquire a new sample (see Table 3,  $t_c$ ) before going low to initiate the next conversion sequence. In applications that do not monitor the BUSY signal, it is recommended that the ADC reset function be implemented as part of a system initialization sequence.

#### **INPUT RANGES**

The ADS8504 offers a standard ±10-V input range. Figure 24 shows the necessary circuit connections for the ADS8504 with and without hardware trim. Offset and full-scale error specifications are tested and specified with the fixed resistors shown in Figure 24(b). Full-scale error includes offset and gain errors measured at both +FS and -FS. Adjustments for offset and gain are described in the Calibration section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the Calibration section).



The nominal input impedance of 11.5 k $\Omega$  results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection assured to at least  $\pm 25$  V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

The input signal must be referenced to AGND1. This will minimize the ground loop problem typical to analog designs. The analog input should be driven by a low impedance source. A typical driving circuit using OPA627 or OPA132 is shown in Figure 23.

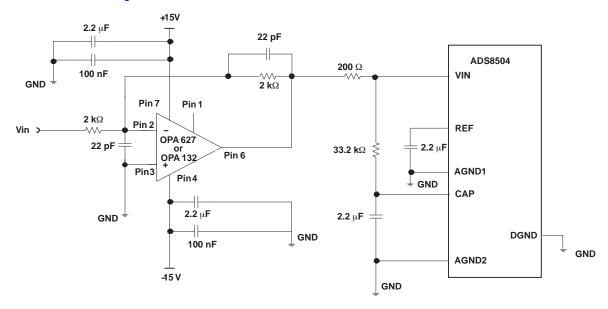


Figure 23. Typical Driving Circuitry (±10 V, No Trim)



#### **APPLICATION INFORMATION**

#### **CALIBRATION**

The ADS8504 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

#### **Hardware Calibration**

To calibrate the offset and gain of the ADS8504, install the proper resistors and potentiometers as shown in Figure 24(a).

#### **Software Calibration**

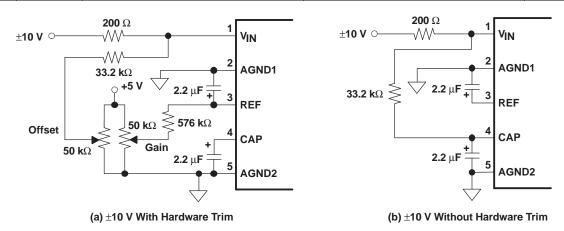
To calibrate the offset and gain of the ADS8504 in software, no external resistors are required. See the No Calibration section for details on the effects of the external resistors. Refer to Table 4 for range of offset and gain errors with and without external resistors.

#### No Calibration

See Figure 24(b) for circuit connections. The external resistors shown in Figure 24(b) may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Refer to Table 4 for range of offset and gain errors with and without external resistors.

Table 4. Typical Offset (Bipolar Zero Error, BPZ) and Gain Errors With and Without External Resistors

|            |             | WITH EXTERNAL RESISTORS | WITHOUT EXTERNAL RESISTORS | UNITS     |
|------------|-------------|-------------------------|----------------------------|-----------|
| BPZ        |             | -4.88 < BPZ < 4.88      | -56.6 < BPZ < -32.2        | mV        |
|            |             | -1 < BPZ < 1            | -11.6 < BPZ < -6.6         | LSBs      |
| O-i        | +Full scale | -0.25 < Error < 0.25    | -2.5 < Error < -1.25       | 0/ -4 ECD |
| Gain error | -Full scale | -0.25 < Error < 0.25    | -3.5 < Error < -2.25       | % of FSR  |



Note: Use 1% metal film resistors.

Figure 24. Circuit Diagram With and Without External Trim Hardware

#### REFERENCE

The ADS8504 can operate with its internal 2.5-V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full-scale error (FSE =  $\pm 0.5$ %).



#### **REF**

REF (pin 3) is an input for an external reference or the output for the internal 2.5-V reference. A 2.2-µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low-pass filter to bandlimit noise on the reference. Using a smaller value capacitor introduces more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external ac or dc loads.

The range for the external reference is 2.3 V to 2.7 V and determines the actual LSB size. Increasing the reference voltage increases the full-scale range and the LSB size of the converter which can improve the SNR.

#### CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2- $\mu$ F capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1  $\mu$ F can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2  $\mu$ F have little affect on improving performance. The ESR (equivalent series resistance) of these compensation capacitors is also critical. Keep the total ESR under 3  $\Omega$ . See the TYPICAL CHARACTERISTICS section for how performance is affected by ESR.

The output of the buffer is capable of driving up to 2 mA of current to a dc load. A dc load requiring more than 2 mA of current from the CAP pin begins to degrade the linearity of the ADS8504. Using an external buffer allows the internal reference to be used for larger dc loads and ac loads. Do not attempt to directly drive an ac load with the output voltage on CAP. This causes performance degradation of the converter.

#### **LAYOUT**

#### **POWER**

For optimum performance, tie the analog and digital power pins to the same +5-V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS8504 uses 90% of its power for the analog circuitry. The ADS8504 should be considered as an analog component.

The +5-V power for the A/D should be separate from the +5 V used for the system's digital logic. Connecting  $V_{DIG}$  (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5-V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12-V or +15-V supplies are present, a simple +5-V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both  $V_{DIG}$  and  $V_{ANA}$  should be tied to the same +5-V source.

#### **GROUNDING**

Three ground pins are present on the ADS8504. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

#### SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS8504, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application is sufficient to drive the ADS8504.

The resistive front end of the ADS8504 also provides an assured  $\pm 25$ -V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.



### LAYOUT (continued)

#### **INTERMEDIATE LATCHES**

The ADS8504 does have 3-state outputs for the parallel port, but intermediate latches should be used if the bus is to be active during conversions. If the bus is not active during conversion, the 3-state outputs can be used to isolate the A/D from other peripherals on the same bus. The 3-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS8504 has an internal LSB size of 610  $\mu$ V. Transients from fast switching signals on the parallel port, even when the A/D is 3-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.



## **Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| C | Changes from Original (June, 2005) to A Revision  |   |  |  |  |  |  |
|---|---|---|--|--|--|--|--|
| • | Deleted text from basic operation description     | 8 |  |  |  |  |  |
| • | Changed text in starting a conversion description | 8 |  |  |  |  |  |
| • | Changed operation descriptions and R/C in table   | 9 |  |  |  |  |  |
| • | Added SAR Reset Timing                            |   |  |  |  |  |  |
| • | Added ADC RESET section                           |   |  |  |  |  |  |



## PACKAGE OPTION ADDENDUM

24-Aug-2018

#### **PACKAGING INFORMATION**

| Orderable Device | Status | Package Type | _       | Pins | _    | Eco Plan                   | Lead/Ball Finish | MSL Peak Temp       | Op Temp (°C) | Device Marking | Samples |
|------------------|--------|--------------|---------|------|------|----------------------------|------------------|---------------------|--------------|----------------|---------|
|                  | (1)    |              | Drawing |      | Qty  | (2)                        | (6)              | (3)                 |              | (4/5)          |         |
| ADS8504IBDW      | ACTIVE | SOIC         | DW      | 28   | 20   | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR | -40 to 85    | ADS8504IB      | Samples |
| ADS8504IBDWR     | ACTIVE | SOIC         | DW      | 28   | 1000 | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR | -40 to 85    | ADS8504IB      | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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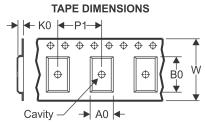
24-Aug-2018

PACKAGE MATERIALS INFORMATION

www.ti.com 12-Feb-2019

## TAPE AND REEL INFORMATION





| A0 |   |
|----|---|
| В0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

| Device       | Package<br>Type | Package<br>Drawing |    | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|--------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| ADS8504IBDWR | SOIC            | DW                 | 28 | 1000 | 330.0                    | 32.4                     | 11.35      | 18.67      | 3.1        | 16.0       | 32.0      | Q1               |

**PACKAGE MATERIALS INFORMATION** 

www.ti.com 12-Feb-2019



#### \*All dimensions are nominal

| Device |              | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |  |
|--------|--------------|--------------|-----------------|------|------|-------------|------------|-------------|--|
| I      | ADS8504IBDWR | SOIC         | DW              | 28   | 1000 | 350.0       | 350.0      | 66.0        |  |

DW (R-PDSO-G28)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.



## DW (R-PDSO-G28)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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