AMC1204 适用于分流测量的 20MHz 二阶隔离式 Δ-Σ 调制器

1 特性

- 针对分流电阻进行优化的 ±250mV 输入电压范围
- 经认证的数字隔离：
  - “通过 CSA、VDE V 0884-10 和 UL1577 认证”
  - 隔离电压：4250 $V_{峰值}$ (AMC1204B)
  - 工作电压：1200 $V_{峰值}$
  - 瞬态抗扰度：15kV/μs
- 隔离栅使用寿命较长（请参见应用报告 SLLA197）
- 高电磁场抗扰度（请参见应用注释SLLA181A）
- 出色的 AC 性能
  - 信噪比 (SNR)：84dB（最小值）
  - 总谐波失真 (THD)：-80dB（最大值）
- 出色的直流精度：
  - 积分非线性 (INL)：±8 最低有效位 (LSB)（最大值）
  - 增益误差：±2%（最大值）
- 用于简化同步操作的外部时钟输入
- 可在扩展工业温度范围内完全额定运行

2 应用

- 在下列应用中基于分流电阻器的电流感测：
  - 电机控制
  - 绿色环保能源
  - 逆变器 应用
  - 不间断电源

3 说明

AMC1204 和 AMC1204B 是 1 位数字输出、隔离式 Δ-Σ 调制器，时钟速率高达 20MHz。调制器输出的数字隔离功能由一个二氧化硅 (SiO_2) 隔离栅提供，具有极高的磁场抗扰度。根据 UL1577、VDE V 0884-10 和 CSA 标准或技术规范，该隔离栅经过认证可提供高达 4000 $V_{峰值}$(AMC1204) 和 4250 $V_{峰值}$ (AMC1204B) 的基本电流隔离。

AMC1204 和 AMC1204B 可为测量隔离栅中分流电阻的小信号提供单芯片解决方案。这些类型的电阻通常用于感测电机控制逆变器、低能耗生成系统以及其他工业应用的电流。AMC1204 和 AMC1204B 差分输入可轻松连接分流电阻或其他低电平信号源。内部基准可免除对外部组件的需要。当与适当的外部数字滤波器配合使用时，可在 78kSPS 数据速率下获得 14 个有效位数 (ENOB)。

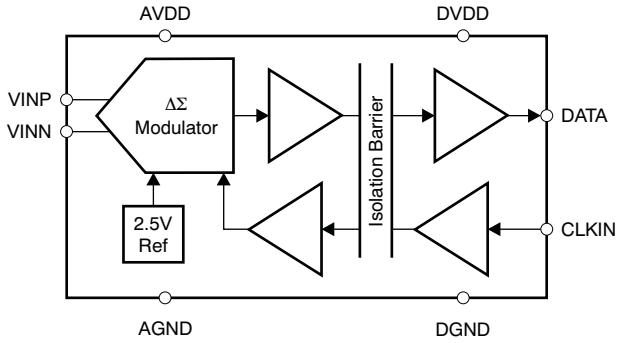
5V 模拟电源 (AVDD) 由调制器使用，而隔离式数字接口由 3V、3.3V 或 5V 电源 (DVDD) 供电运行。AMC1204 和 AMC1204B 采用小外形尺寸集成电路 (SOIC)-16 (DW) 封装，可在 -40°C 至 105°C 的温度范围内额定运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC1204	SOIC (16)	10.30mm x 7.50mm
	SOIC (8)	5.85mm × 7.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (December 2013) to Revision E — **Page**

- 已添加 *ESD 额定值表*，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已更改 *经认证的数字隔离*特性要点的第一个分项：已将“IEC60747-5-5”更改为“VDE V 0884-10” ... 1
- 已更改 “IEC60747-5-5”至“VDE V 0884-10”（*说明*部分的第一段） ... 1
- 已更改 Isolator to Package in title of Isolator Characteristics table ... 2
- Changed IEC60747-5-5 to VDE V 0884-10 in first row of *Regulatory Information* table ... 7
- Changed Isolator to Package in title of Isolator Characteristics table ... 9
- Changed Isolator to Package in title of Isolator Characteristics table ... 26

Changes from Revision C (August 2012) to Revision D — **Page**

- 已更改 *经认证的数字隔离*特性要点的第一个分项：已将“IEC60747-5-2”更改为“IEC60747-5-5” ... 1
- 已删除 芯片照片 ... 1
- 已添加 DWV (SSO-8) 封装至文档 ... 1
- 已更改 “IEC60747-5-2”至“IEC60747-5-5”（*说明*部分的第一段） ... 1
- 已更改 *说明*部分的最后一段 ... 1
- Added DWV pin out drawing ... 4
- Added DWV information to Pin Descriptions table ... 4
- Added DWV package to Thermal Information table ... 5
- Changed IEC60747-5-2 to IEC60747-5-5 in first row of *Regulatory Information* table ... 7
- Added DWV package row to *L(I01)* and *L(I02)* parameters in Isolator Characteristics table ... 9
- Changed first paragraph of *Digital Output* section: changed 78.1% to 89.06% and 21.9% to 10.94% ... 19

Changes from Revision B (August 2011) to Revision C **Page**

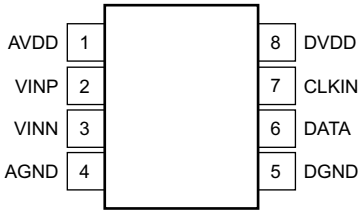
- 已更改 经认证的数字隔离中的“隔离电压”特性要点 ... 1
- 已添加 AMC1204B 至文档 ... 1
- 已更改 说明 部分以包括 AMC1204B ... 1
- Changed package name from TSSOP to SO ... 4
- Changed footnote 1 in *Electrical Characteristics* table ... 6
- Changed Analog Inputs, V_{CM} parameter minimum specification and unit in *Electrical Characteristics* table ... 6
- Changed Digital Output, C_{OUT} and C_{LOAD} parameters unit specifications in *Electrical Characteristics* table ... 7
- Added AMC1204B values to Isolation Characteristics table ... 9
- Changed AMC1204 V_{IOTM} t = 1s value in Isolation Characteristics table ... 9
- Changed CTI minimum specification in Isolator Characteristics table ... 9
- Updated Figure 51 ... 24
- Updated Figure 53 ... 25
- Updated Figure 54 ... 26

Changes from Revision A (April 2011) to Revision B **Page**

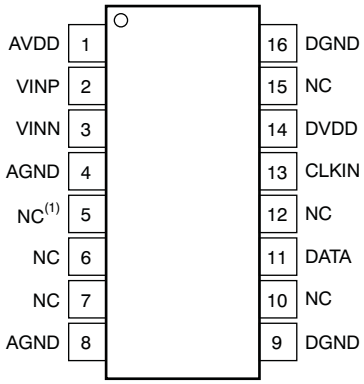
- Changed value of V_{IOSM} parameter in IEC 61000-4-5 Ratings table ... 8

5 Pin Configurations

DWV Package
8-Pin SOIC
Top View



DW Package
16-Pin SOIC
Top View



NC = no internal connection.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	8 PINS	16 PINS		
AVDD	1	1	Power	High-side power supply
VINP	2	2	Analog input	Noninverting analog input
VINN	3	3	Analog input	Inverting analog input
AGND	4	4, 8(1)	Power	High-side ground
DGND	5	9, 16	Power	Controller-side ground
DATA	6	11	Digital output	Modulator data output
CLKIN	7	13	Digital input	Modulator clock input
DVDD	8	14	Power	Controller-side power supply
NC	—	5-7, 10, 12, 15	—	No internal connection; can be tied to any potential or left unconnected

(1) Both pins are connected internally via a low-impedance path; thus, only one of the pins must be tied to the ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

Over the operating ambient temperature range, unless otherwise noted. (1)

	MIN	MAX	UNIT
Supply voltage, AVDD to AGND or DVDD to DGND	–0.3	6	V
Analog input voltage at VINP, VINN	AGND – 0.5	AVDD + 0.5	V
Digital input voltage at CLKIN	DGND – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Maximum virtual junction temperature, T_J		150	°C
Operating ambient temperature, T_{OA}	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electrical Characteristics* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per JEDEC standard 22, test method A114-C.01 (1)	±3000	V
	Charged-device model (CDM), per JEDEC standard 22, test method C101 (2)	±1500	
	Machine model (MM), per JEDEC standard 22, test method A115A	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	–40		105	°C
AVDD	High-side (analog) supply voltage	4.5	5	5.5	V
DVDD	Controller-side (digital) supply voltage	2.7	3.3	5.5	V

6.4 Thermal Information

THERMAL METRIC (1)		AMC1204, AMC1204B		UNIT
		DW (SOIC)	DWV (SOIC)	
		16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.5	106.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.3	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.2	60.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.5	18.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	58.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All minimum/maximum specifications at T_A = –40°C to 105°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
INL	Integral linearity error(1)	T_A = –40°C to 85°C	–8	±2	8	LSB
		T_A = –40°C to 105°C	–16	±5	16	LSB
DNL	Differential nonlinearity		–1		1	LSB
V_{OS}	Offset error(2)		–1	±0.1	1	mV
TCV_{OS}	Offset error thermal drift		–3.5	±1	3.5	µV/°C
G_{ERR}	Gain error(2)		–2%	±0.5%	2%	
TCG_{ERR}	Gain error thermal drift			±30		ppm/°C
PSRR	Power-supply rejection ratio			79		dB
ANALOG INPUTS						
FSR	Full-scale differential voltage input range	VINP – VINN		±320		mV
	Specified FSR		–250		250	mV
V_{CM}	Operating common-mode signal(3)		–160		AVDD	mV
C_I	Input capacitance to AGND	VINP or VINN		7		pF
C_{ID}	Differential input capacitance			3.5		pF
R_{ID}	Differential input resistance			12.5		kΩ
I_{IL}	Input leakage current	VINP – VINN = ±250 mV	–10		10	µA
		VINP – VINN = ±320 mV	–50		50	µA
CMTI	Common-mode transient immunity		15			kV/µs
CMRR	Common-mode rejection ratio	V_{IN} from 0 V to 5 V at 0 Hz		108		dB
		V_{IN} from 0 V to 5 V at 100 kHz		114		dB
EXTERNAL CLOCK						
t_{CLKIN}	Clock period		45.5	50	200	ns
f_{CLKIN}	Input clock frequency		5	20	22	MHz
$Duty_{CLKIN}$	Duty cycle	5 MHz ≤ f_{CLKIN} < 20 MHz	40%	50%	60%	
		20 MHz ≤ f_{CLKIN} ≤ 22 MHz	45%	50%	55%	
AC ACCURACY						
SINAD	Signal-to-noise + distortion	f_{IN} = 1kHz, T_A = –40°C to 85°C	78	87		dB
		f_{IN} = 1kHz, T_A = –40°C to 105°C	70	87		dB
SNR	Signal-to-noise ratio	f_{IN} = 1kHz, T_A = –40°C to 85°C	84	88		dB
		f_{IN} = 1kHz, T_A = –40°C to 105°C	83	88		dB
THD	Total harmonic distortion	f_{IN} = 1kHz, T_A = –40°C to 85°C		–96	–80	dB
		f_{IN} = 1kHz, T_A = –40°C to 105°C		–96	–70	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1kHz, T_A = –40°C to 85°C	82	96		dB
		f_{IN} = 1kHz, T_A = –40°C to 105°C	72	96		dB
DIGITAL INPUTS(3)						
I_{IN}	Input current	V_{IN} = DVDD to DGND	–10		10	µA
C_{IN}	Input capacitance			5		pF
CMOS logic family			CMOS with Schmitt-trigger			
V_{IH}	High-level input voltage	DVDD = 4.5V to 5.5V	0.7DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage	DVDD = 4.5V to 5.5V	–0.3		0.3DVDD	V
LVCMOS logic family			LVCMOS			
V_{IH}	High-level input voltage	DVDD = 2.7 V to 3.6 V	2		DVDD + 0.3	V

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified 500-mV input range.
(2) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(3) Ensured by design.

Electrical Characteristics (continued)

All minimum/maximum specifications at T_A = –40°C to 105°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	DVDD = 2.7 V to 3.6 V	–0.3		0.8	V
DIGITAL OUTPUTS(3)						
C_{OUT}	Output capacitance			5		pF
C_{LOAD}	Load capacitance				30	pF
CMOS logic family				CMOS		
V_{OH}	High-level output voltage	DVDD = 4.5 V, I_{OH} = –100 µA	4.4			V
V_{OL}	Low-level output voltage	DVDD = 4.5 V, I_{OL} = 100 µA			0.5	V
LVCMOS logic family				LVCMOS		
V_{OH}	High-level output voltage	I_{OH} = 20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA, 2.7 V ≤ DVDD ≤ 3.6 V	DVDD – 0.4			V
		I_{OH} = –4 mA, 4.5 V ≤ DVDD ≤ 5.5 V	DVDD – 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	V
POWER SUPPLY						
AVDD	High-side supply voltage		4.5	5	5.5	V
DVDD	Controller-side supply voltage		2.7	3.3	5.5	V
I_{AVDD}	High-side supply current	4.5 V ≤ AVDD ≤ 5.5 V		11	16	mA
I_{DVDD}	Controller-side supply current	2.7 V ≤ DVDD ≤ 3.6 V		2	4	mA
		4.5V ≤ DVDD ≤ 5.5 V		2.8	5	mA
P_D	Power dissipation	AVDD = 5.5 V, DVDD = 3.6 V		61.6	102.4	mW

6.6 Timing Requirements

Over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted. (See Figure 1)

		MIN	NOM	MAX	UNIT
t_{CLK}	CLKIN clock period	45.5	50	200	ns
t_{HIGH}	CLKIN clock high time	20	25	120	ns
t_{LOW}	CLKIN clock low time	20	25	120	ns
t_D	Delayed falling edge of CLKIN to DATA valid	2		15	ns

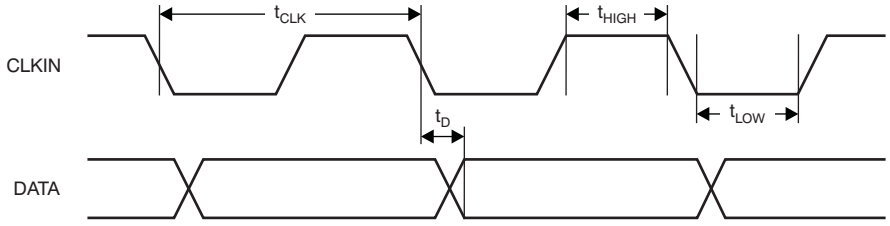


Figure 1. Modulator Output Timing

6.7 Regulatory Information

VDE/IEC	CSA	UL
Certified according to VDE V 0884-10	Approved under CSA component acceptance notice	Recognized under 1577 component recognition program
Certificate number: 40016131	File number: 2350550	File number: E181974

6.8 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.
The safety-limiting constraint is the operating virtual junction temperature range specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 78.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			10	mA
T_C	Maximum case temperature				150	°C

6.9 IEC 61000-4-5 Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Surge immunity	1.2/50-µs voltage surge and 8/20-µs current surge	±6000	V

6.10 IEC 60664-1 Ratings

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150V_{RMS}	I-IV
	Rated mains voltage < 300V_{RMS}	I-IV
	Rated mains voltage < 400V_{RMS}	I-III
	Rated mains voltage < 600V_{RMS}	I-III

6.11 Isolation Characteristics

PARAMETER		TEST CONDITIONS	AMC1204	AMC1204B	UNIT
V_{IORM}	Maximum working insulation voltage		1200	1200	V_{PEAK}
$V_{PD(t)}$	Partial discharge test voltage	t = 1 s (100% production test), partial discharge < 5 pC	2250	2250	V_{PEAK}
V_{IOTM}	Transient overvoltage	t = 60 s (qualification test)	4000	4250	V_{PEAK}
		t = 1 s (100% production test)	4800	5100	V_{PEAK}
R_S	Isolation resistance	V_{IO} = 500 V at T_S	> 10^9	> 10^9	Ω
PD	Pollution degree		2	2	Degrees

6.12 Package Characteristics

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	DWV package	8			mm
			DW package	7.9			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	DWV package	8			mm
			DW package	7.9			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 part 1		> 400			V
	Minimum internal gap (internal clearance)	Distance through the insulation		0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together to create a two-terminal device, T_A < 85°C			> 10^{12}		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A < T_A max			> 10^{11}		Ω
C_{IO}	Barrier capacitance input to output	V_I = 0.8 V_{PP} at 1 MHz			1.2		pF
C_I	Input capacitance to ground	V_I = 0.8 V_{PP} at 1 MHz			3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the *TI Isolation Glossary*. Techniques such as inserting grooves, ribs, or both on the PCB are used to help increase these specifications.

6.13 Typical Characteristics

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

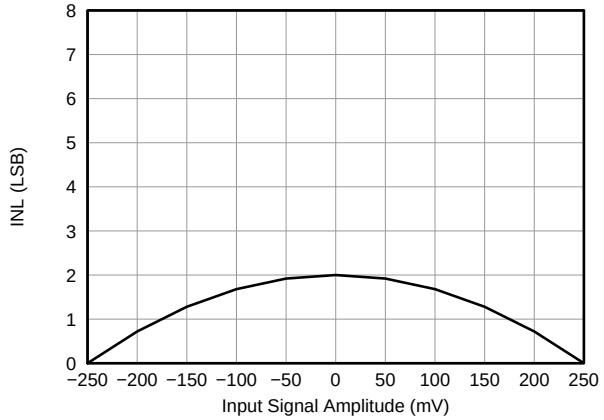


Figure 2. Integral Nonlinearity vs Input Signal Amplitude

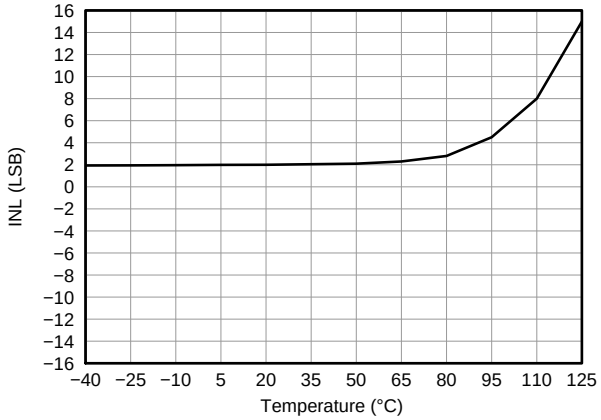


Figure 3. Integral Nonlinearity vs Temperature

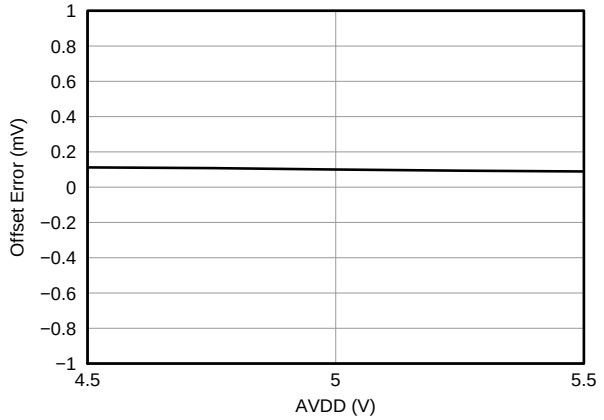


Figure 4. Offset Error vs Analog Supply Voltage

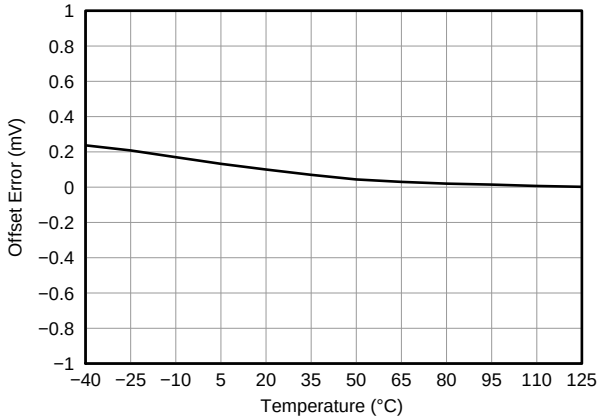


Figure 5. Offset Error vs Temperature

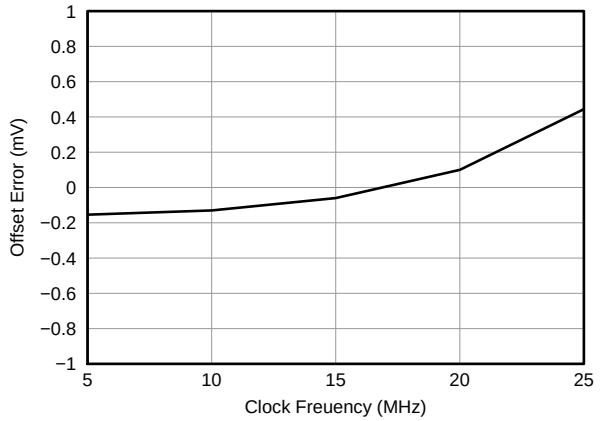


Figure 6. Offset Error vs Clock Frequency

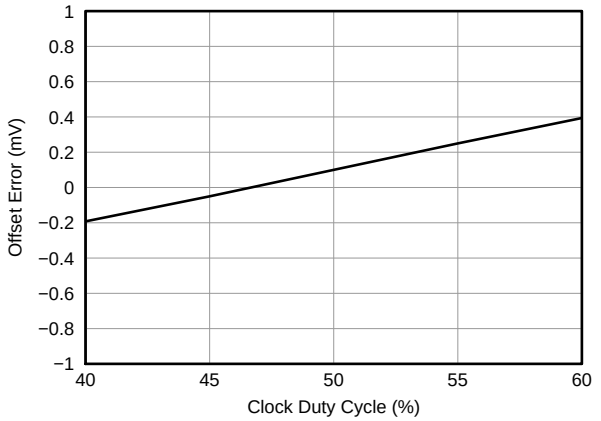


Figure 7. Offset Error vs Clock Duty Cycle

Typical Characteristics (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

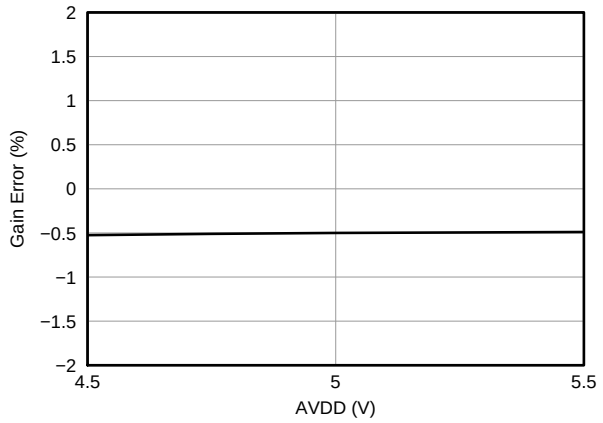


Figure 8. Gain Error vs Analog Supply Voltage

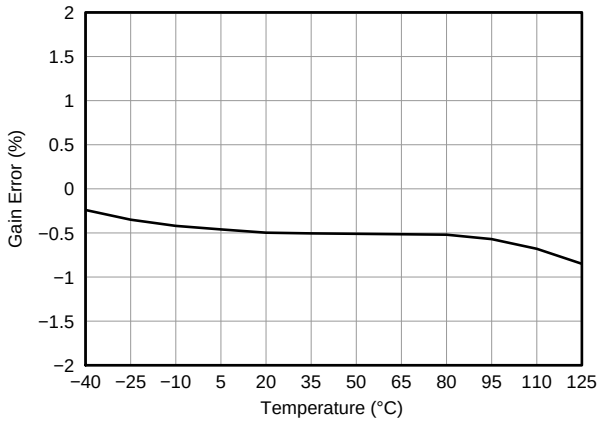


Figure 9. Gain Error vs Temperature

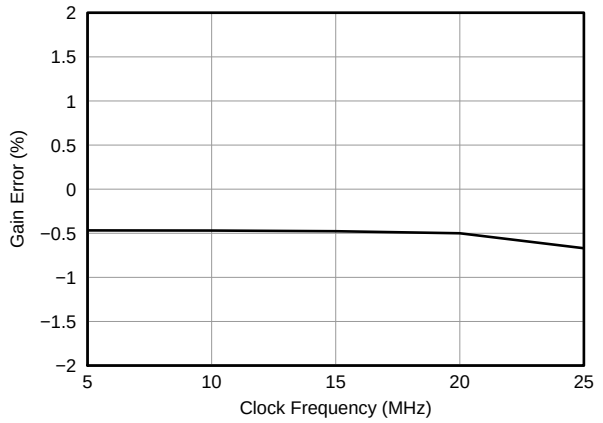


Figure 10. Gain Error vs Clock Frequency

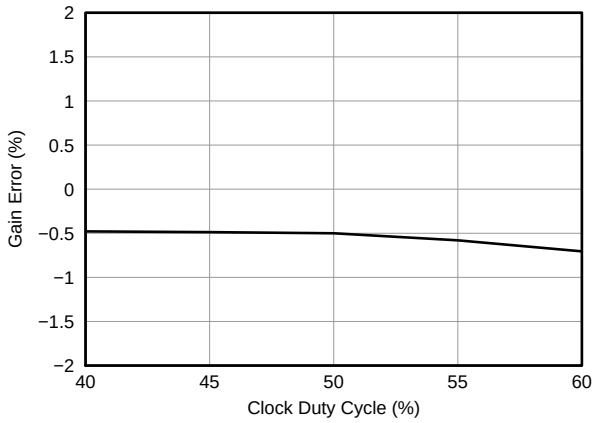


Figure 11. Gain Error vs Clock Duty Cycle

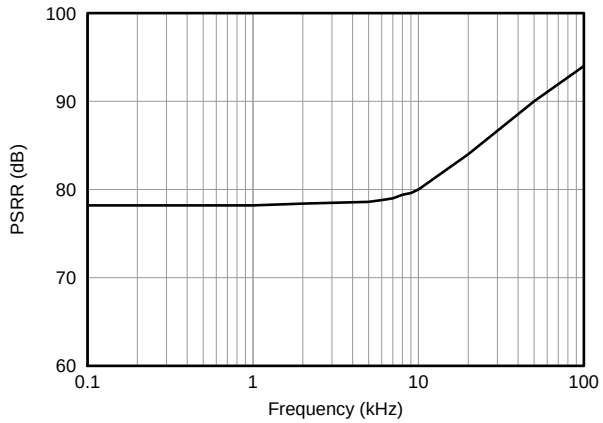


Figure 12. Power-Supply Rejection Ratio vs Frequency

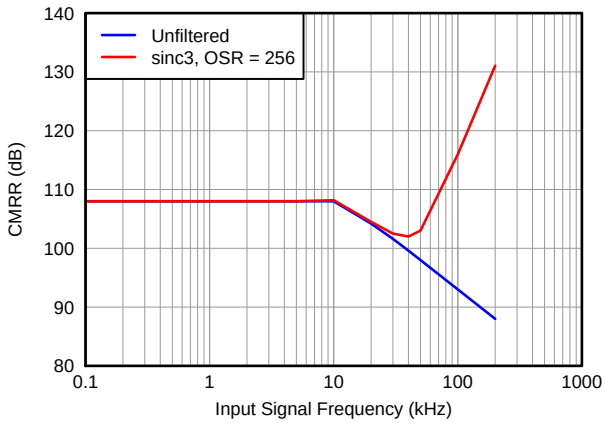


Figure 13. Common-Mode Rejection Ratio vs Input Signal Frequency

Typical Characteristics (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

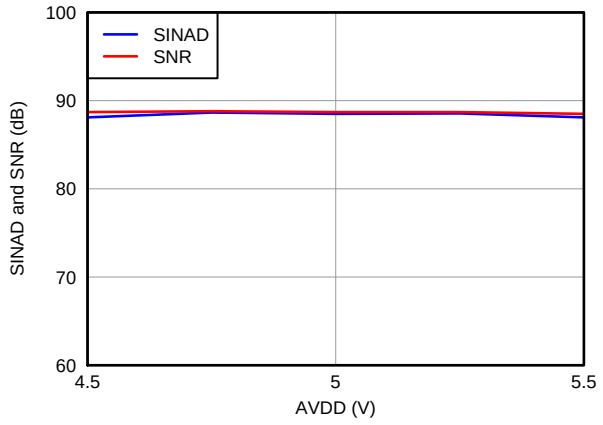


Figure 14. SINAD and SNR vs Analog Supply Voltage

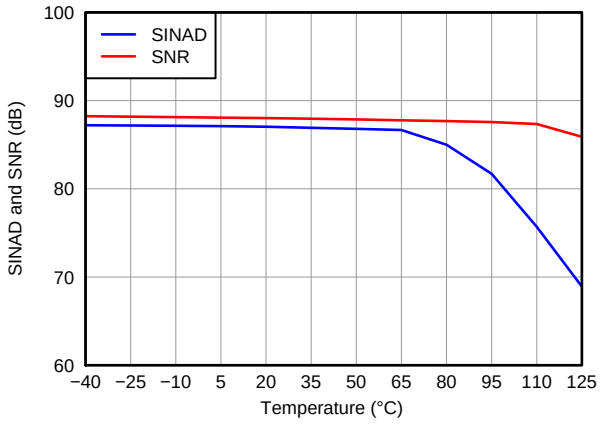


Figure 15. SINAD and SNR vs Temperature

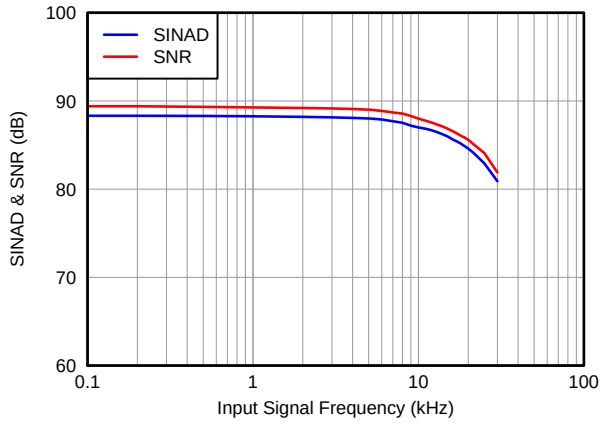


Figure 16. SINAD and SNR vs Input Signal Frequency

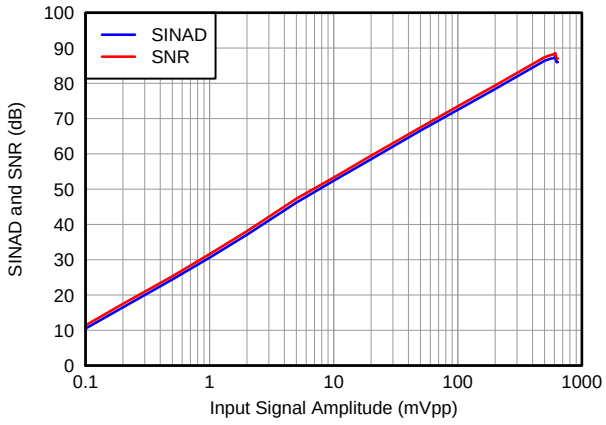


Figure 17. SINAD and SNR vs Input Signal Amplitude

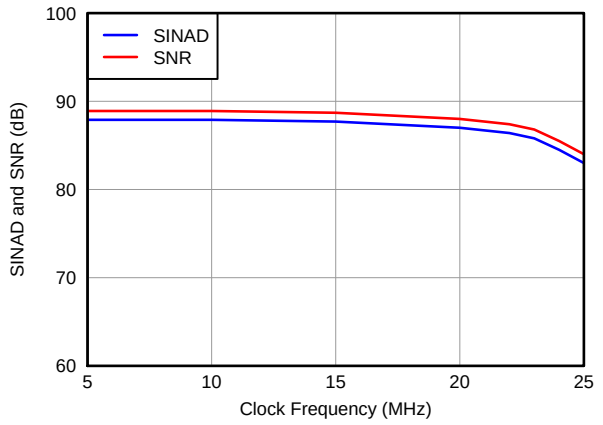


Figure 18. SINAD and SNR vs Clock Frequency

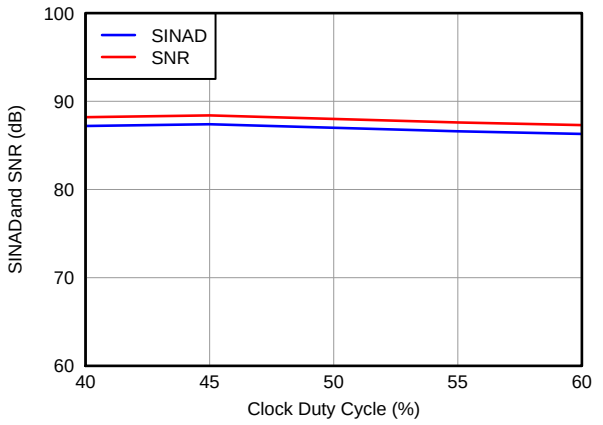


Figure 19. SINAD and SNR vs Clock Duty Cycle

Typical Characteristics (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

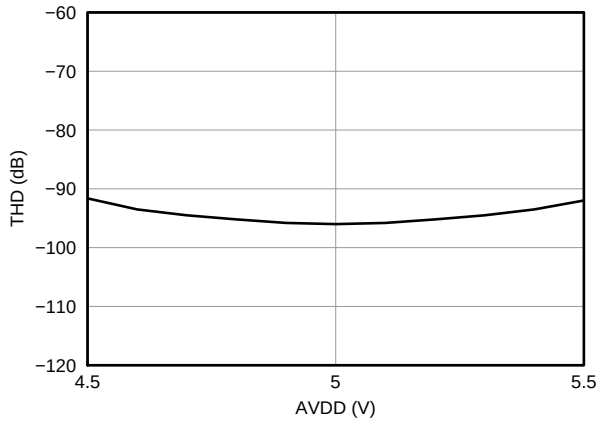


Figure 20. Total Harmonic Distortion vs Analog Supply Voltage

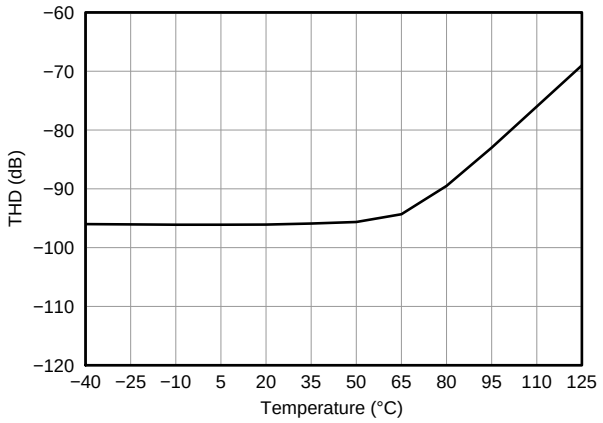


Figure 21. Total Harmonic Distortion vs Temperature

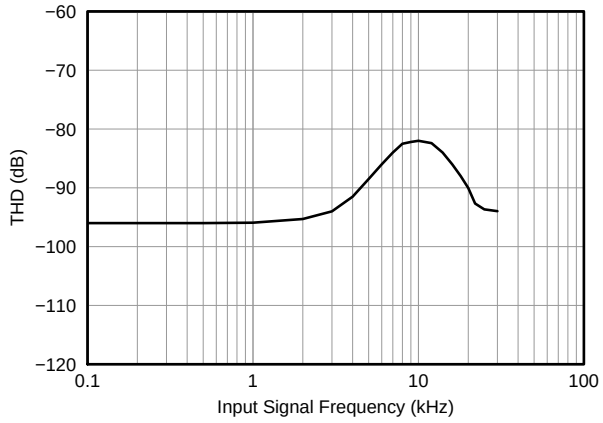


Figure 22. Total Harmonic Distortion vs Input Signal Frequency

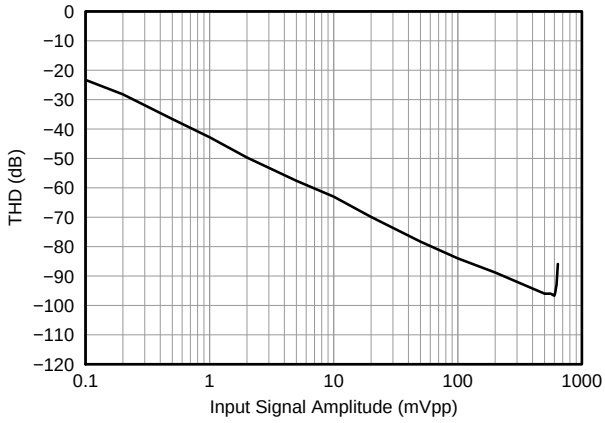


Figure 23. Total Harmonic Distortion vs Input Signal Amplitude

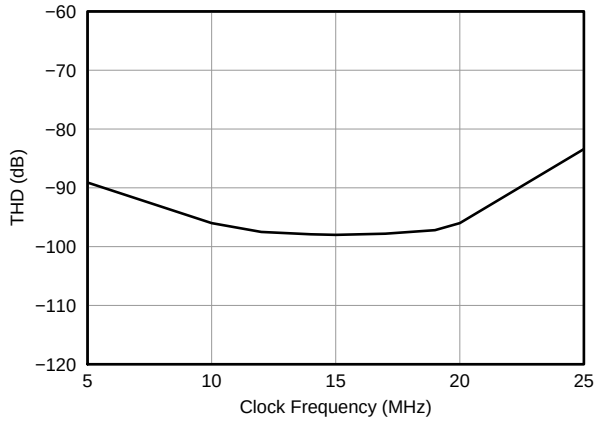


Figure 24. Total Harmonic Distortion vs Clock Frequency

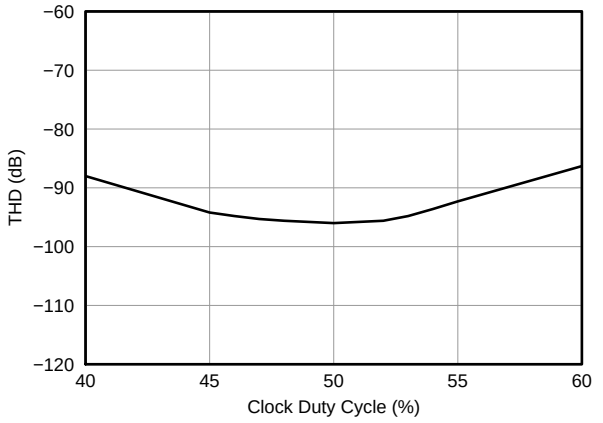


Figure 25. Total Harmonic Distortion vs Clock Duty Cycle

Typical Characteristics (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

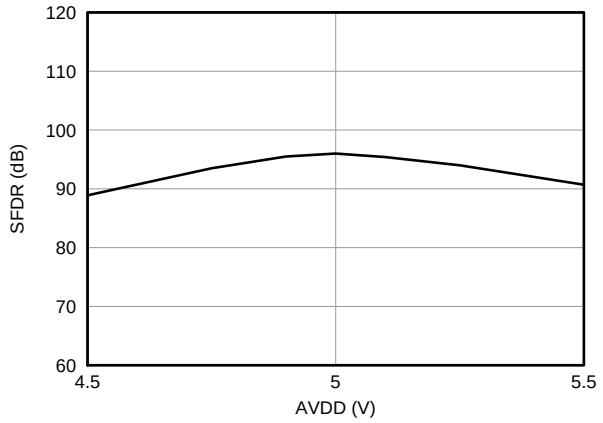


Figure 26. Spurious-Free Dynamic Range vs Analog Supply Voltage

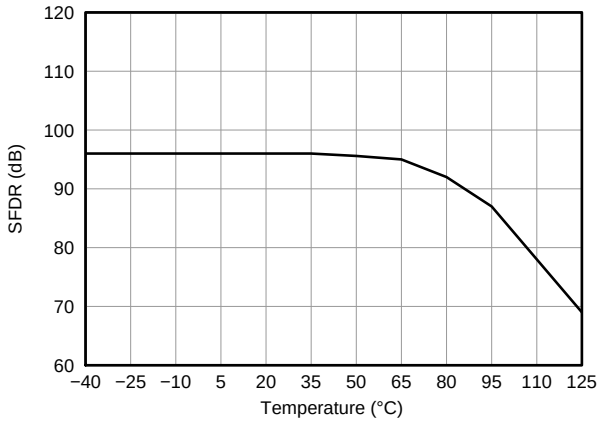


Figure 27. Spurious-Free Dynamic Range vs Temperature

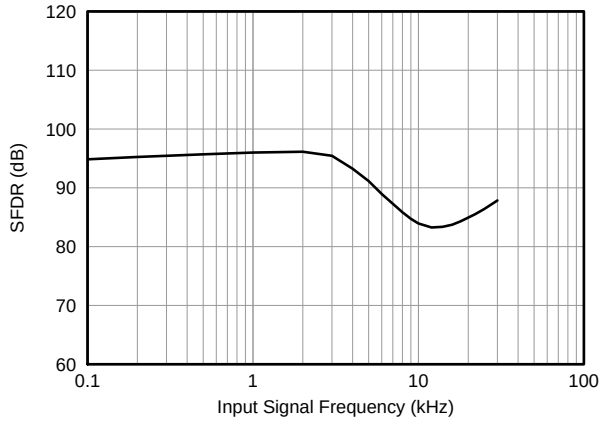


Figure 28. Spurious-Free Dynamic Range vs Input Signal Frequency

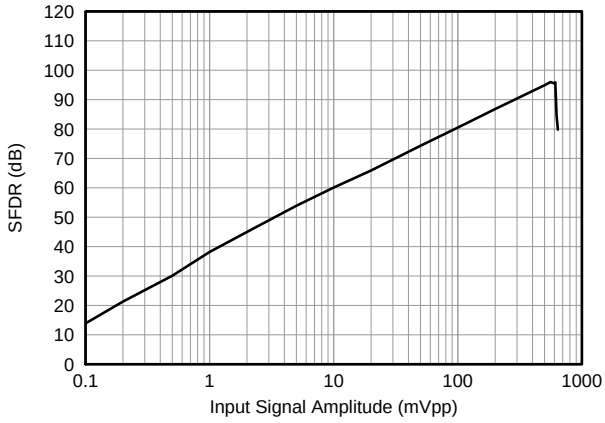


Figure 29. Spurious-Free Dynamic Range vs Input Signal Amplitude

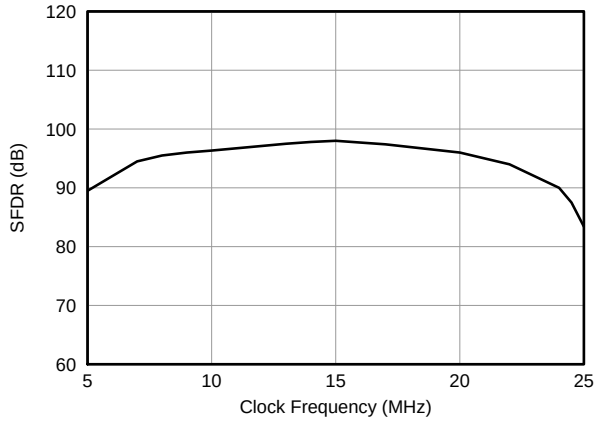


Figure 30. Spurious-Free Dynamic Range vs Clock Frequency

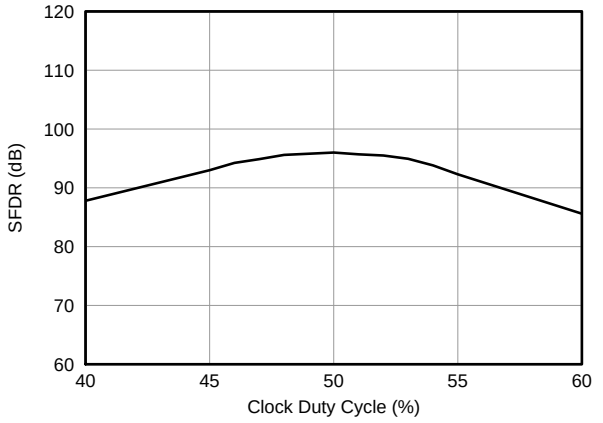


Figure 31. Spurious-Free Dynamic Range vs Clock Duty Cycle

Typical Characteristics (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

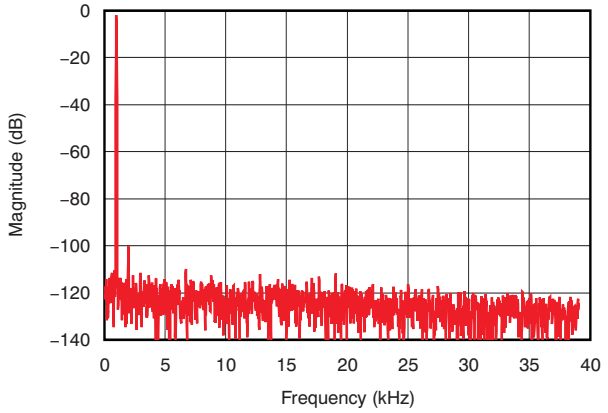


Figure 32. Frequency Spectrum (4096 Point FFT, f_{IN} = 1 kHz, 0.56 V_{PP})

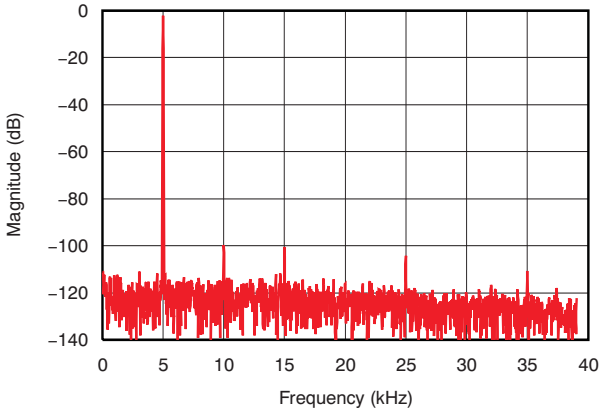


Figure 33. Frequency Spectrum (4096 Point FFT, f_{IN} = 5 kHz, 0.56 V_{PP})

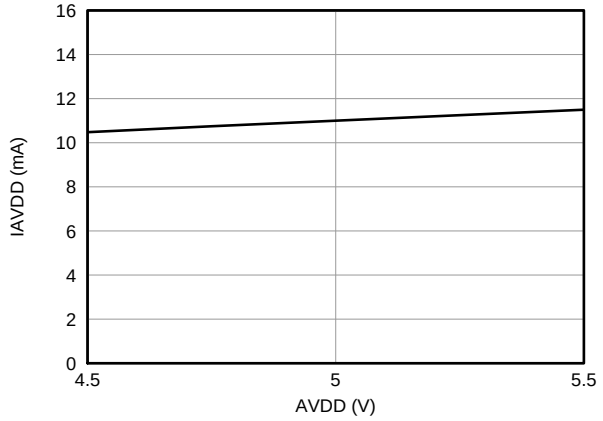


Figure 34. Analog Supply Current vs Analog Supply Voltage

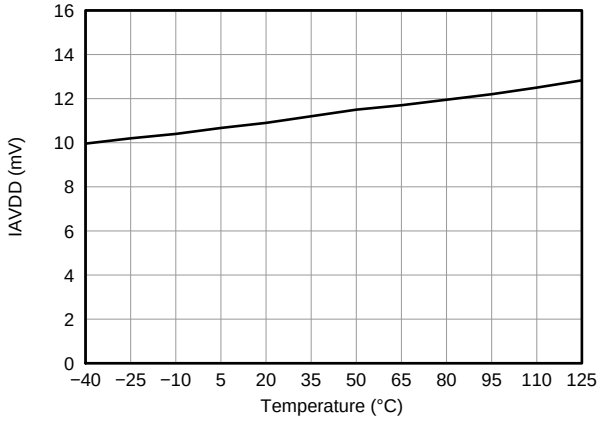


Figure 35. Analog Supply Current vs Temperature

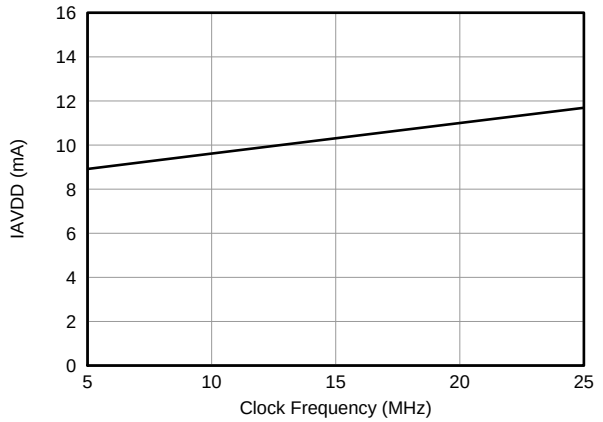


Figure 36. Analog Supply Current vs Clock Frequency

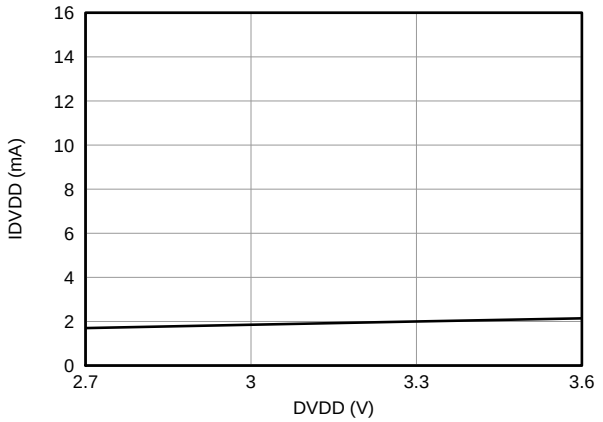


Figure 37. Digital Supply Current vs Digital Supply Voltage (3 V)

Typical Characteristics (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

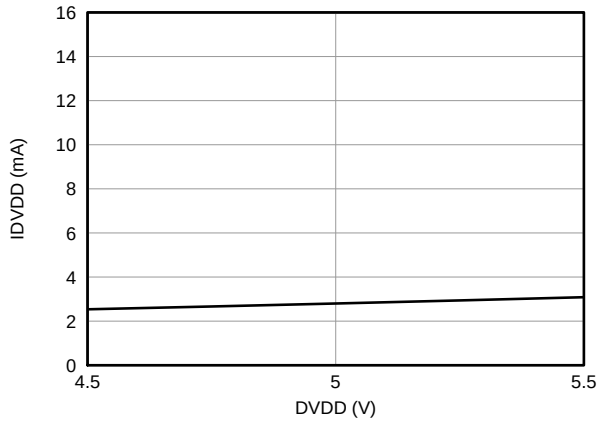


Figure 38. Digital Supply Current vs Digital Supply Voltage (5 V)

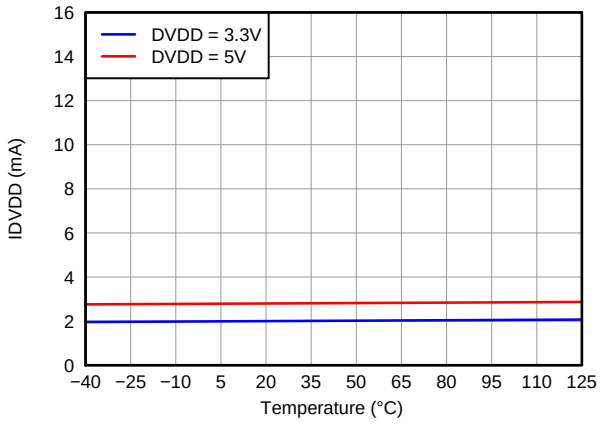


Figure 39. Digital Supply Current vs Temperature

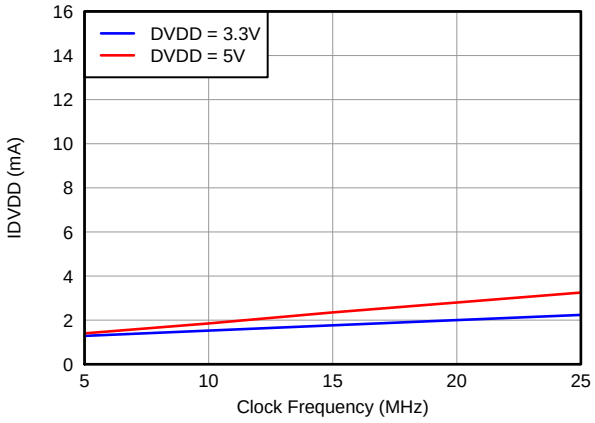


Figure 40. Digital Supply Current vs Clock Frequency

7 Detailed Description

7.1 Overview

The AMC1204 and AMC1204B are single-channel, second-order, delta-sigma (ΔΣ) modulators designed for medium- to high-resolution analog-to-digital conversions. The isolated output of the converter (DATA) provides a stream of digital ones and zeros accurately representing the analog input voltage over time. The time average of this serial output is proportional to the analog input voltage.

Functional Block Diagram shows a detailed block diagram of the AMC1204 and AMC1204B. The analog input range is tailored to directly accommodate the voltage drop across a shunt resistor used for current sensing. The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the application report *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181A). The external clock input simplifies the synchronization of multiple current sense channels on system level. The extended frequency range of up to 20 MHz supports higher performance levels compared to the other solutions available on the market.

7.2 Functional Block Diagram

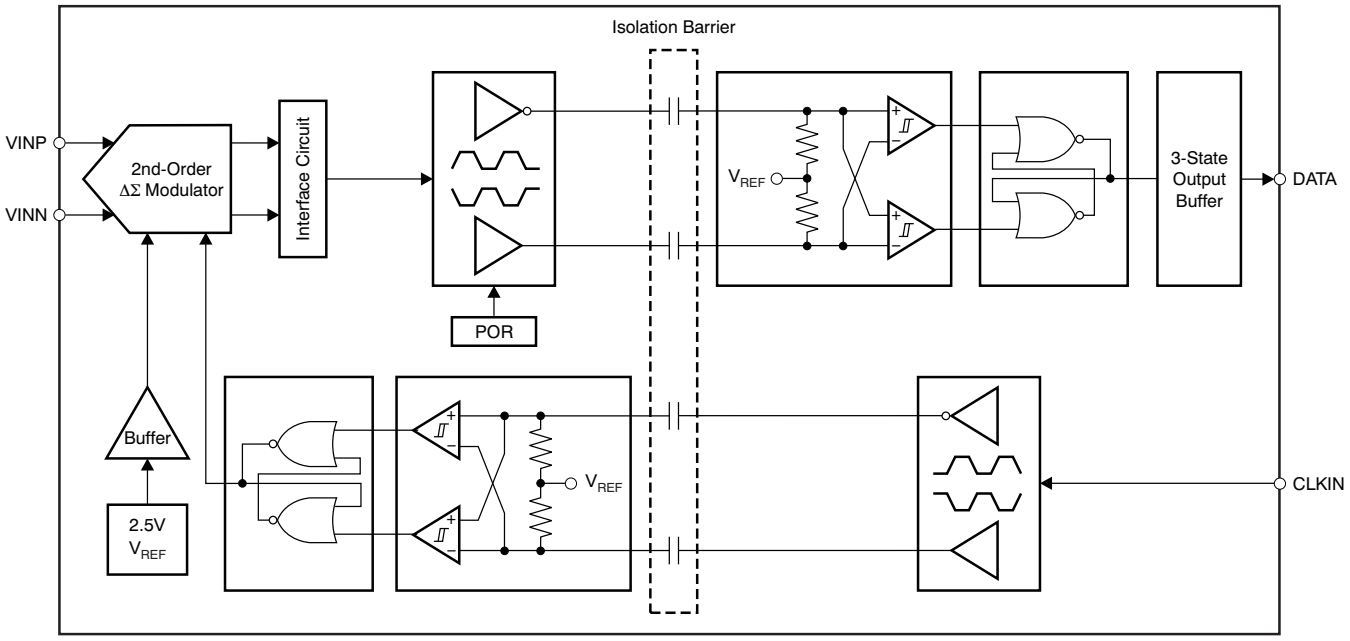


Figure 41. Detailed Block Diagram

7.3 Feature Description

7.3.1 Analog Input

The differential analog input of the AMC1204 and AMC1204B is implemented with a switched-capacitor circuit.

The AMC1204 and AMC1204B measure the differential input signal V_{IN} = (VINP – VINN) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged. Figure 42 shows the simplified schematic of the AMC1204 and AMC1204B input circuitry; the right side of Figure 42 illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit.

In Figure 42, the S_1 switches close during the input sampling phase. With the S_1 switches closed, C_{DIFF} charges to the voltage difference across VINP and VINN. For the discharge phase, both S_1 switches open first and then both S_2 switches close. C_{DIFF} discharges approximately to AGND + 0.8 V during this phase. This two-phase sample/discharge cycle repeats with a period of $t_{CLKIN} = 1/f_{CLKIN}$. f_{CLKIN} is the operating frequency of the modulator. The capacitors C_{IP} and C_{IN} are of parasitic nature and caused by bonding wires and the internal ESD protection structure.

Feature Description (continued)

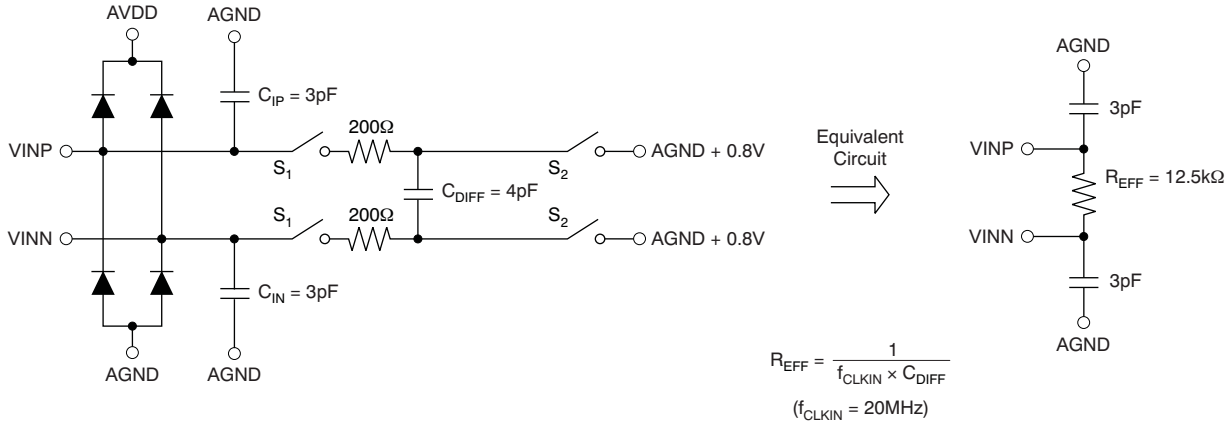


Figure 42. Equivalent Analog Input Circuit

There are two restrictions on the analog input signals VINP and VINN. First, if the input voltage exceeds the range AGND – 0.5 V to AVDD + 0.3 V, the input current must be limited to 10 mA because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV.

7.3.2 Modulator

The modulator topology of the AMC1204 and AMC1204B is fundamentally a second-order, switched-capacitor, ΔΣ modulator, such as the one conceptualized in Figure 43. The analog input voltage ($X_{(t)}$) and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage (X_2) at the input of the first integrator or modulator stage. The output of the first integrator is further differentiated with the DAC output; the resulting voltage (X_3) feeds the input of the second integrator stage. When the value of the integrated signal (X_4) at the output of the second stage equals the comparator reference voltage, the output of the comparator switches from high to low, or vice versa, depending on its previous state. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage (X_6), causing the integrators to progress in the opposite direction, while forcing the value of the integrator output to track the average of the input.

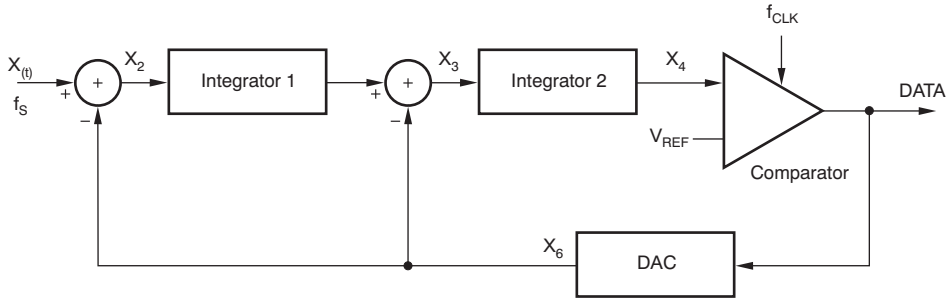


Figure 43. Block Diagram Of A Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 44; therefore, a low-pass digital filter should be used at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (μC), or field programmable gate array (FPGA) can be used to implement the filter.

Feature Description (continued)

TI's microcontroller family TMS320F28x7x offers a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1204, AMC1304 and AMC1305 devices. Also, the SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters, thus offering a system-level solution for multichannel isolated current sensing. Another option is to use a suitable application-specific device such as the AMC1210, a four-channel digital sinc-filter.

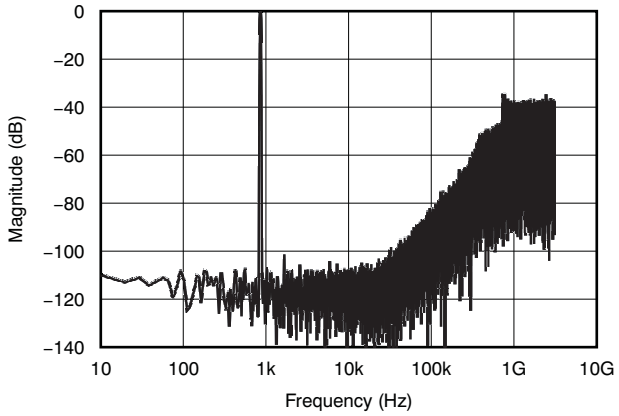


Figure 44. Quantization Noise Shaping

7.3.3 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of 250 mV produces a stream of ones and zeros that are high 89.06% of the time. A differential input of –250 mV produces a stream of ones and zeros that are high 10.94% of the time. This is also the specified linear input range of the modulator with the performance as specified in this data sheet. The range between 250 mV and 320 mV (absolute values) is the non-linear range of the modulator. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320 mV or with a stream of only ones with an input greater than or equal to 320 mV. The input voltage versus the output modulator signal is shown in Figure 45.

The system clock of the AMC1204 and AMC1204B is typically 20 MHz and is provided externally at the CLKIN pin. The data are synchronously provided at 20 MHz at the DATA output pin. The data are changing at the falling edge of CLKIN; for more details see the *Timing Requirements* section.

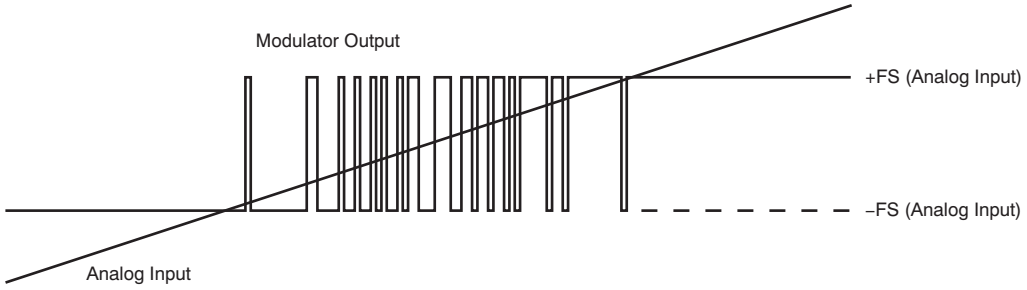


Figure 45. Analog Input Versus Amc1204 Modulator Output

7.4 Device Functional Modes

The AMC1204 is operational when the power supplies AVDD and DVDD are applied as specified in the *Recommended Operating Conditions* section.

The AMC1204 has no additional functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 1:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \quad (1)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates). For an oversampling rate (OSR) in the range of 16 to 256, this filter is a good choice. All the characterization in this document is also done with a sinc^3 filter with OSR = 256 and an output word width of 16 bits.

In a sinc^3 filter response (shown in Figure 46 and Figure 47), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3-dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type with different frequency response. Performance can be improved, for example, by using a cascaded filter structure. The first decimation stage could be built of a sinc^3 filter with a low OSR and the second stage using a high-order filter.

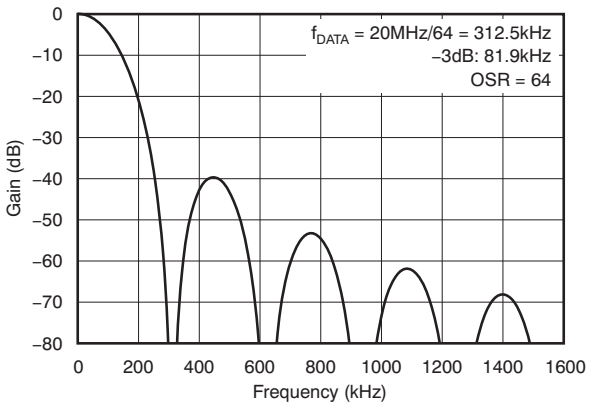


Figure 46. Frequency Response Of The Sinc^3 Filter

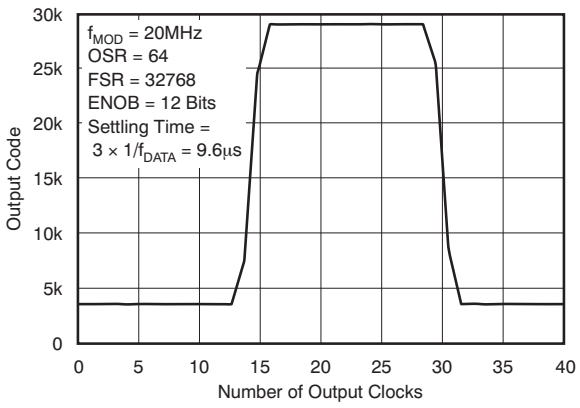


Figure 47. Pole Response Of The Sinc^3 Filter

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 49 illustrates the ENOB of the AMC1204 and AMC1204B with different oversampling ratios. In this data sheet, this number is calculated from SNR using Equation 2:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (2)$$

An example code for an implementation of a sinc^3 filter in an FPGA follows. For more information, see the application note, *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications*, (SBAA094), available for download at www.ti.com.

Application Information (continued)

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5 : out std_logic_vector(23 downto 0));
end FLT;

architecture RTL of FLT is
  signal DN0, DN1, DN3, DN5 : std_logic_vector(23 downto 0);
  signal CN1, CN2, CN3, CN4 : std_logic_vector(23 downto 0);
  signal DELTA1 : std_logic_vector(23 downto 0);
begin

process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;

process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;

process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;

CN3 <= DN0 - DN1;
CN4 <= CN3 - DN3;
CN5 <= CN4 - DN5;

end RTL;
```

8.2 Typical Application

8.2.1 Frequency Inverter Application

Because of their high AC and DC performance, isolated ΔΣ modulators are being widely used in new generation frequency inverter designs. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), electrical and hybrid vehicles, and other industrial applications. The input structure of the AMC1204 is optimized for use with low-impedance shunt resistors and is therefore tailored for isolated current sensing using shunts.

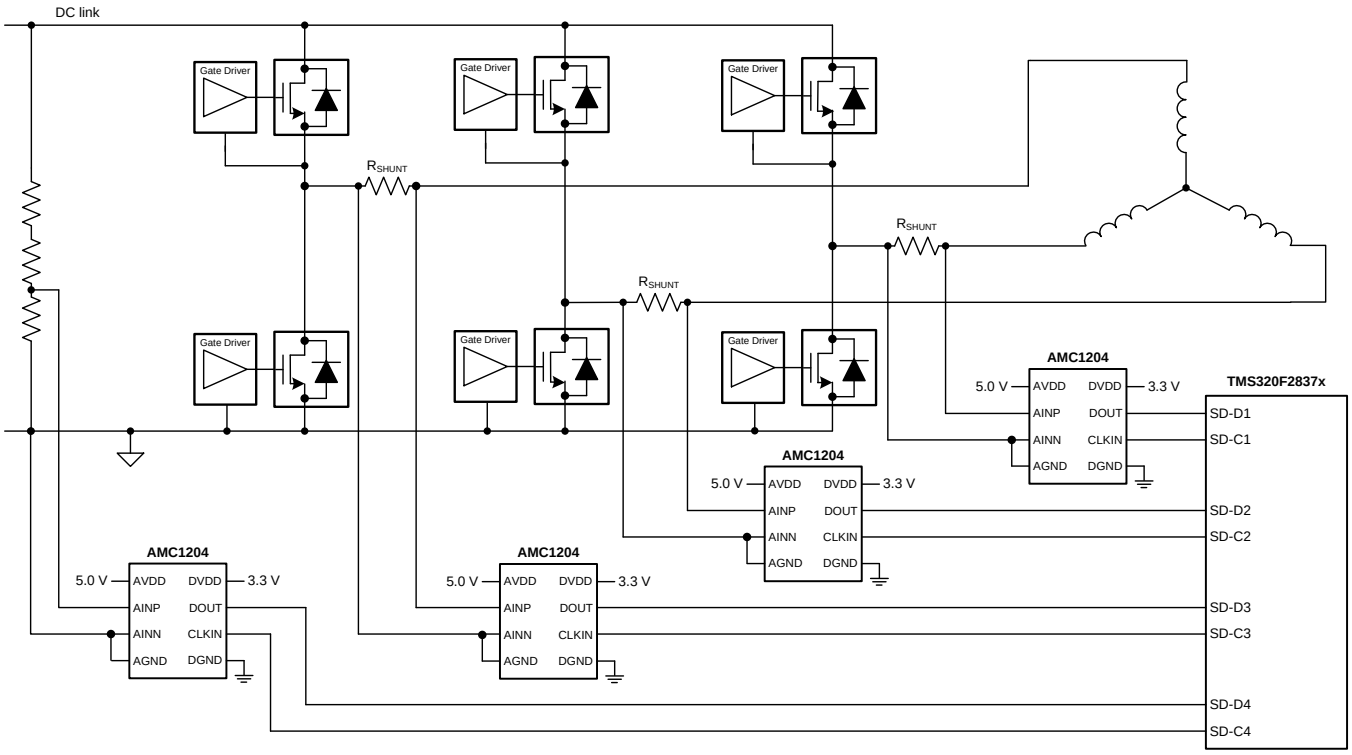


Figure 48. AMC1204 in a Frequency Inverter Application

8.2.1.1 Design Requirements

Figure 48 shows a diagram of the AMC1204 in a typical frequency inverter. When the inverter stage is part of a motor drive system, measurement of the motor phase current is done via the shunt resistors (R_{SHUNT}). Depending on the system design, either all three or only two phase currents are sensed.

In this example, an additional AMC1204 is used for isolated sensing of the DC link voltage. This high DC link voltage is reduced using a high-impedance resistive divider before being sensed by the AMC1204 across a smaller resistor. It is important to consider that the value of the resistor in the voltage divider can potentially degrade the performance of the measurement. Such phenomenon is described in the *Isolated Voltage Sensing* section.

8.2.1.2 Detailed Design Procedure

For modulator output bit-stream filtering, TI recommends a device from TI's TMS320F28x7x family of MCUs. This family supports up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

Typical Application (continued)

8.2.1.3 Application Curves

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on its order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK} / OSR$). Therefore, for overcurrent protection, filter types other than $sinc^3$ might be better choices. An alternative is, for example, the $sinc^2$ filter. Figure 50 compares the settling times of different filter orders.

Sincfast is a modified $sinc^2$ filter whose transfer function follows Equation 3.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 (1 + z^{-2OSR}) \quad (3)$$

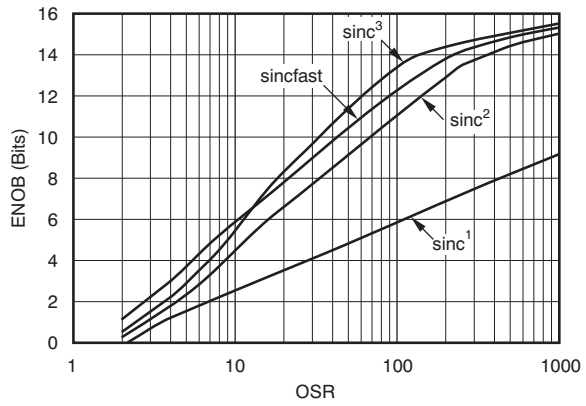


Figure 49. Measured Effective Number Of Bits Versus Oversampling Ratio

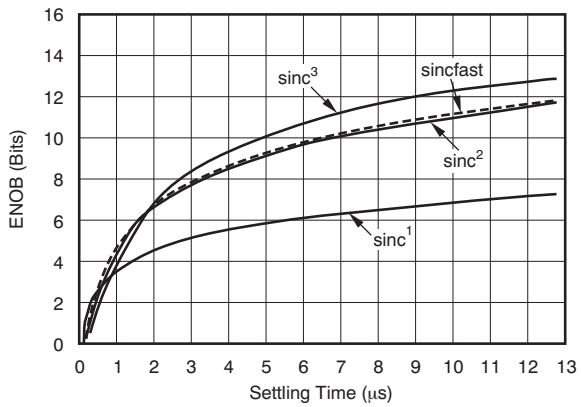


Figure 50. Measured Effective Number of Bits Versus Settling Time

In the case of a continuous signal fed into a sinc filter, the time delay for such signal corresponds to half of the settling time shown in Figure 50.

Typical Application (continued)

8.2.2 Example of a Resolver-Based Motor Control Analog Front End

Figure 51 shows an example of two AMC1204 and AMC1204B devices and one ADS1209 (a dual-channel, 10-MHz, non-isolated modulator) connected to an AMC1210, building the entire analog front end of a resolver-based motor control application.

For detailed information on the ADS1209 and AMC1210, visit the respective device product folders at www.ti.com.

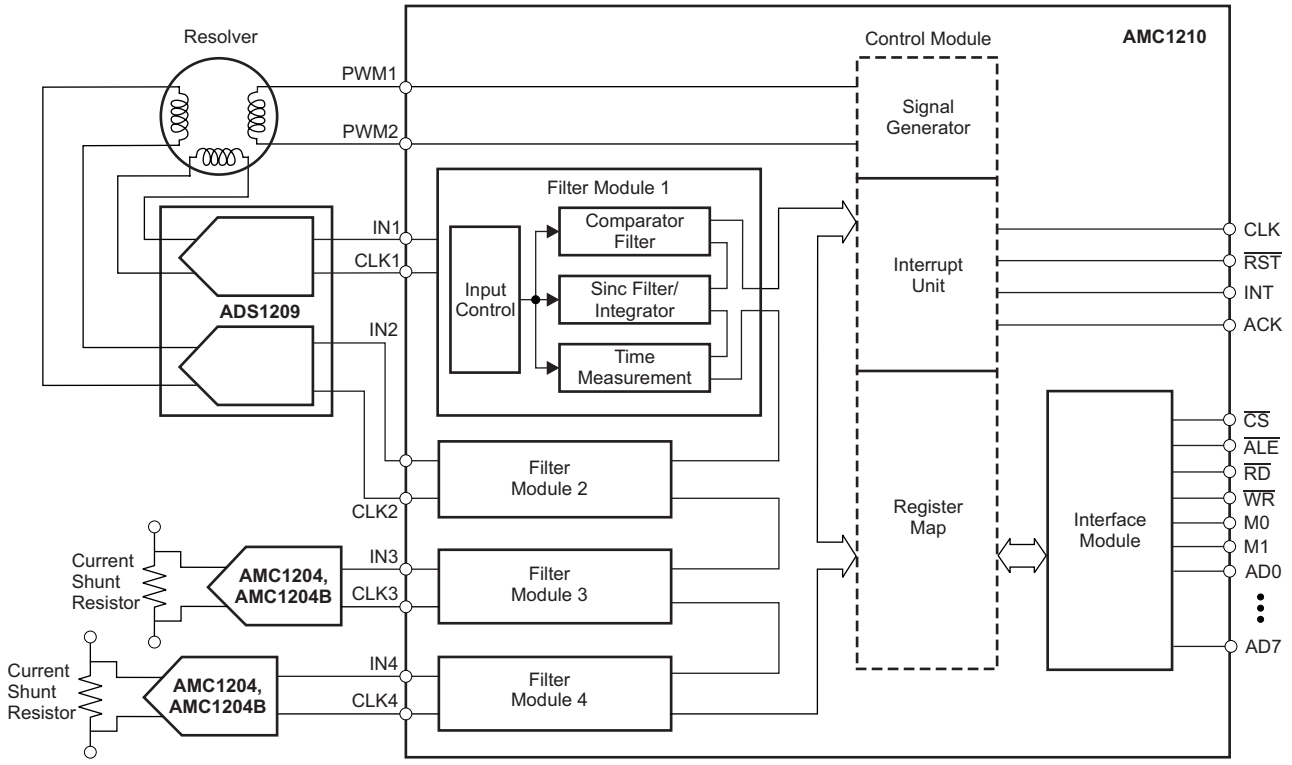


Figure 51. Example of a Resolver-Based Motor Control Analog Front End Schematic

8.2.3 Isolated Voltage Sensing

The AMC1204 is optimized for current-sensing applications using low-impedance shunts. However, the device can also be used in isolated voltage-sensing applications if the impact of the (usually higher) impedance of the resistor used in this case is considered. Figure 52 shows a simplified circuit typically used in high-voltage sensing applications.

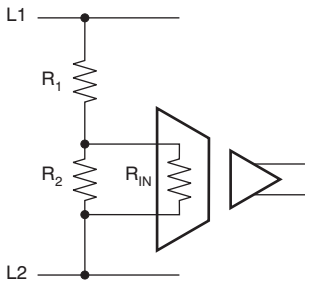


Figure 52. Voltage Measurement Application

Typical Application (continued)

8.2.3.1 Design Requirements

In such applications, a resistor divider (R_1 and R_2) is used to match the relatively small input voltage range of the AMC device. R_2 and the input resistance R_{IN} of the AMC1204 also create a resistor divider resulting in additional gain error. With the assumption that R_1 and R_{IN} have a considerably higher value than R_2, use Equation 4 to estimate the resulting total gain error.

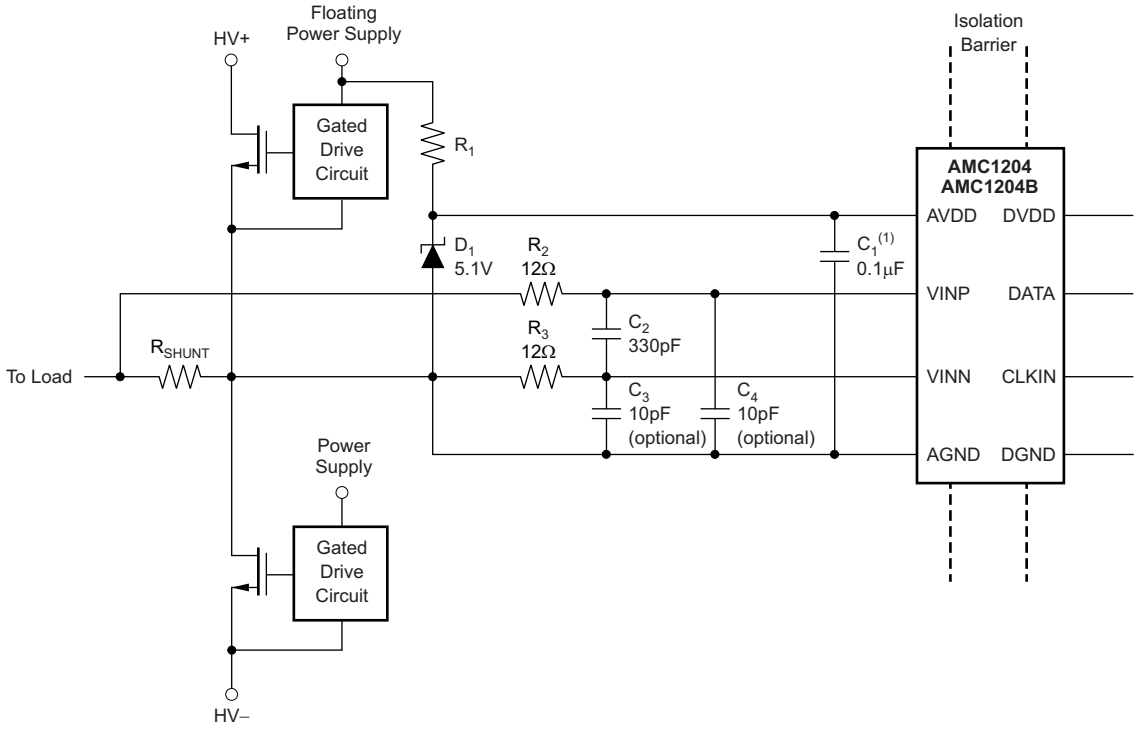
$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}} \quad (4)$$

where

- G_{ERR} = the gain error of AMC device.

9 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (AVDD) for the AMC1204 and AMC1204B is derived from the power supply of the upper gate driver. For lowest cost, a Zener diode can be used to limit the voltage to 5 V ±10%. TI recommends a decoupling capacitor of 0.1 µF for filtering this power-supply path. This capacitor (C_1 in Figure 53) should be placed as close as possible to the AVDD pin for best performance. If better filtering is required, an additional 1-µF to 10-µF capacitor can be used. The floating ground reference AGND is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the AMC1204 and AMC1204B. If a four-terminal shunt is used, the inputs of AMC1204 and AMC1204B are connected to the inner leads, while AGND is connected to one of the outer leads of the shunt. Both digital signals, CLKIN and DATA, can be directly connected to a digital filter.



(1) Place C_1 close to the AMC1204 and AMC1204B.

Figure 53. Zener-Diode-Based High-Side Power Supply

For better performance, the differential input signal is filtered using RC filters (components R_2, R_3, and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors: any mismatch in the capacitor values can cause a common-mode error at the input of the modulator.

10 Layout

10.1 Layout Guidelines

- Place the decoupling capacitors for AVDD and DVDD as close as possible to the AMC1204.
- Ensure that the traces that connect the shunt resistor to the RC filter on the VINP terminal are symmetrical to and have the same length as the traces connecting to the VINN terminal.
- The top and bottom PCB layers underneath the AMC1204 must be kept free of any conductive materials in order to comply with the creepage and clearance distances shown in the *Package Characteristics* section.

10.2 Layout Example

Figure 54 shows the recommended layout and placement of the decoupling capacitors and other components required by the AMC1204 and AMC1204B.

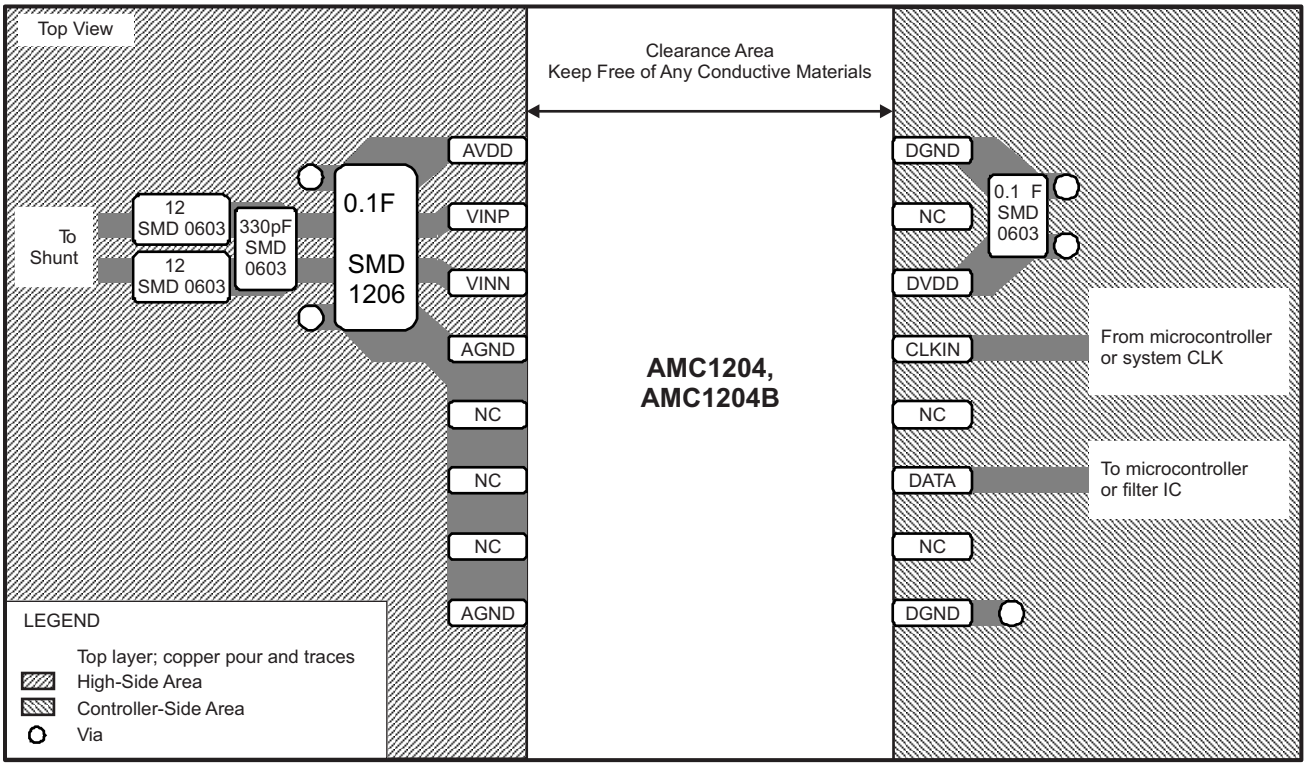


Figure 54. Recommended Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- *《ISO72x 数字隔离器磁场抗扰度》*，SLLA181
- *《使用 ADS1202 与 FPGA 数字滤波器的组合测量 电机控制应用的电流》*，SBAA094
- *《隔离相关术语》*，*SLLA353*

11.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
AMC1204	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
AMC1204B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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RFID 系统	www.ti.com.cn/rfidsys		
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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1204BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1204B	Samples
AMC1204BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	1204B	Samples
AMC1204BDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	AMC1204B	Samples
AMC1204BDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	AMC1204B	Samples
AMC1204DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1204	Samples
AMC1204DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1204	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AMC1204 :

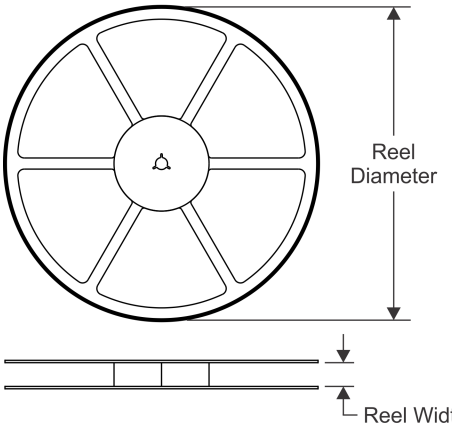
- Automotive: AMC1204-Q1

NOTE: Qualified Version Definitions:

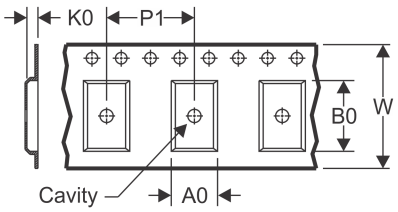
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

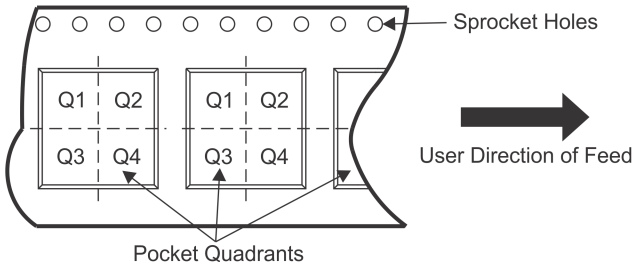


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

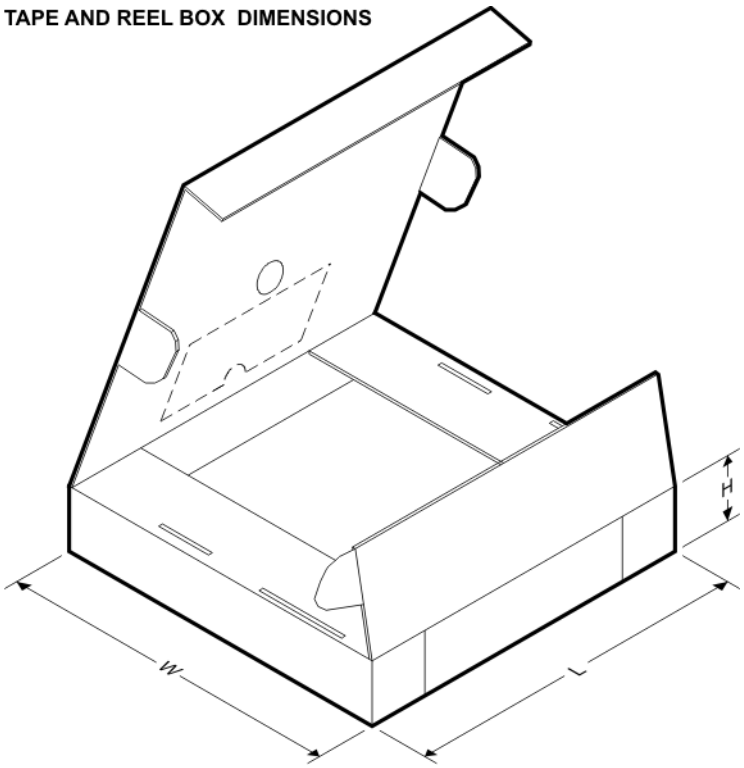
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

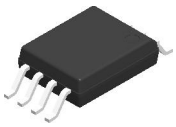
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1204BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC1204BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1204DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

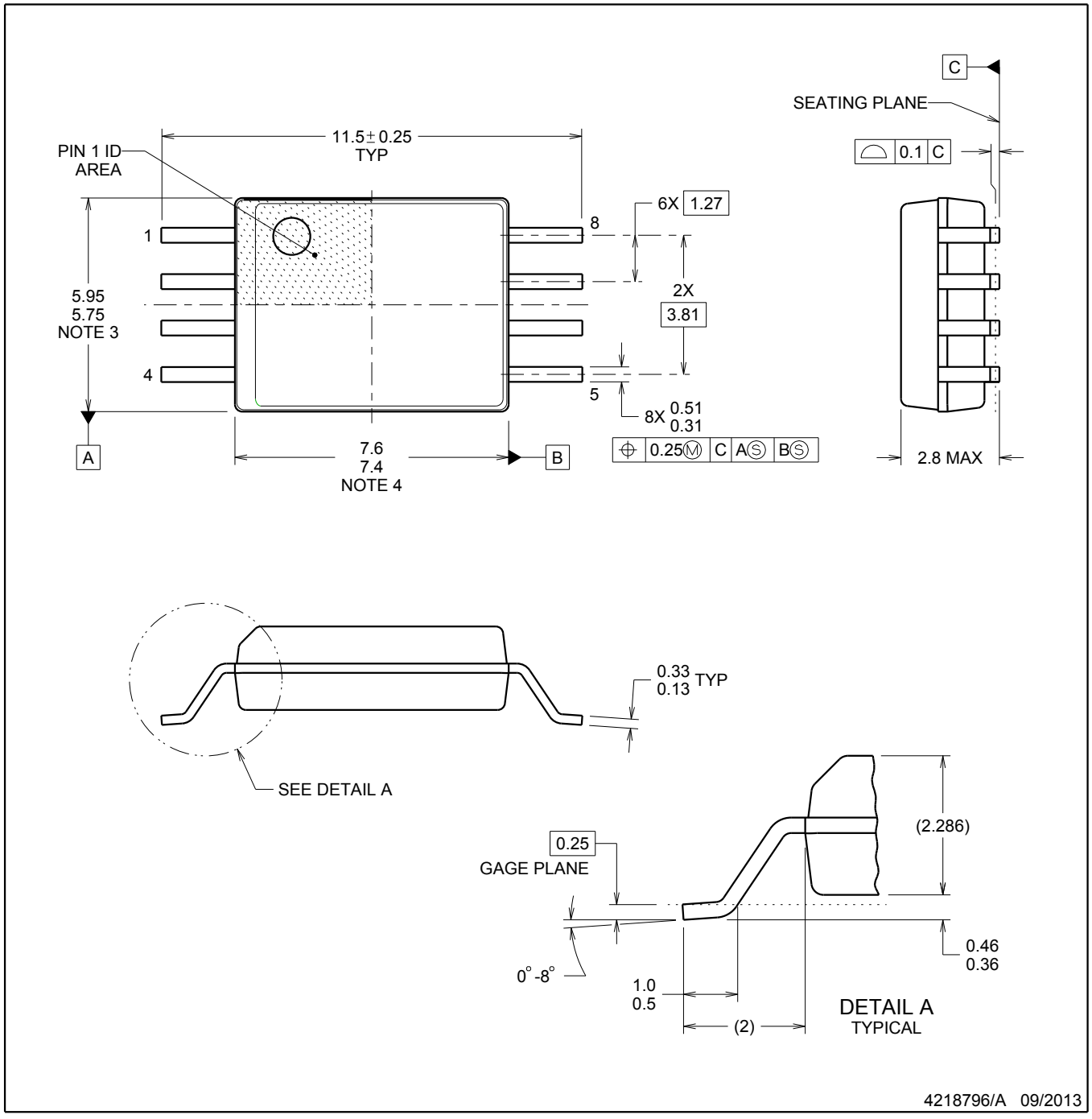
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1204BDWR	SOIC	DW	16	2000	350.0	350.0	43.0
AMC1204BDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1204DWR	SOIC	DW	16	2000	350.0	350.0	43.0



DWV0008A

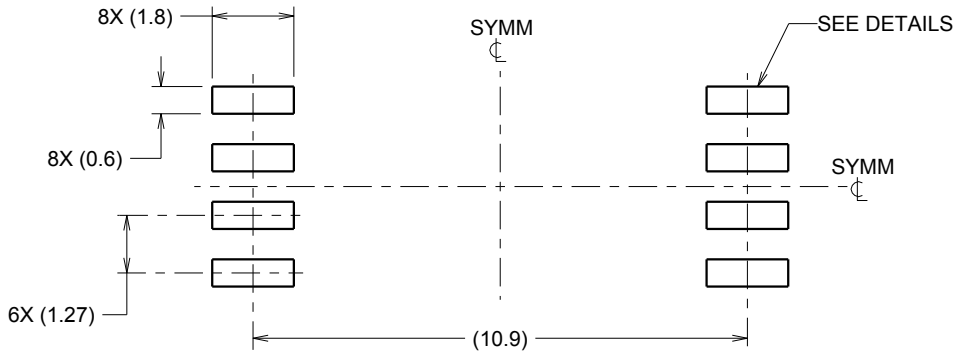
SOIC - 2.8 mm max height

SOIC

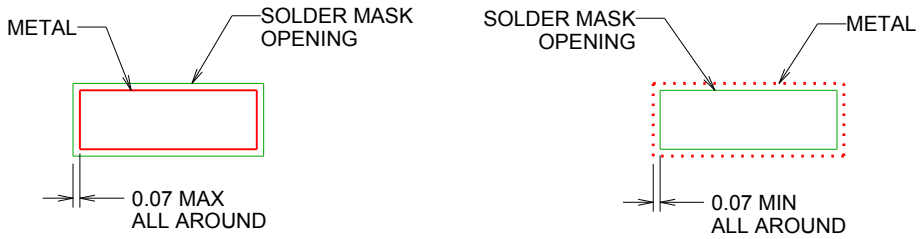


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

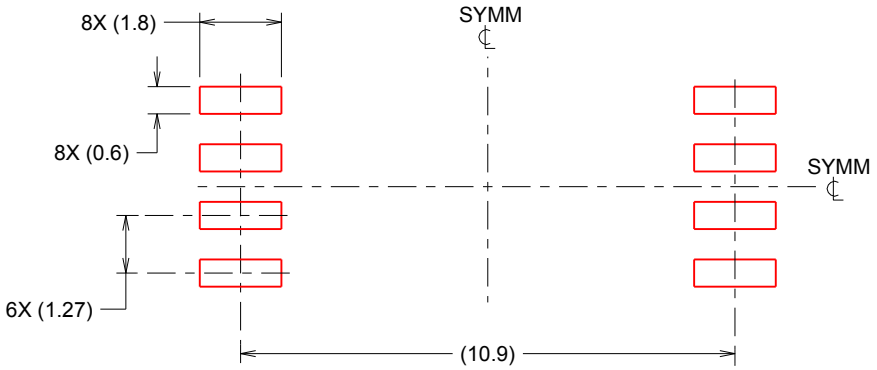
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

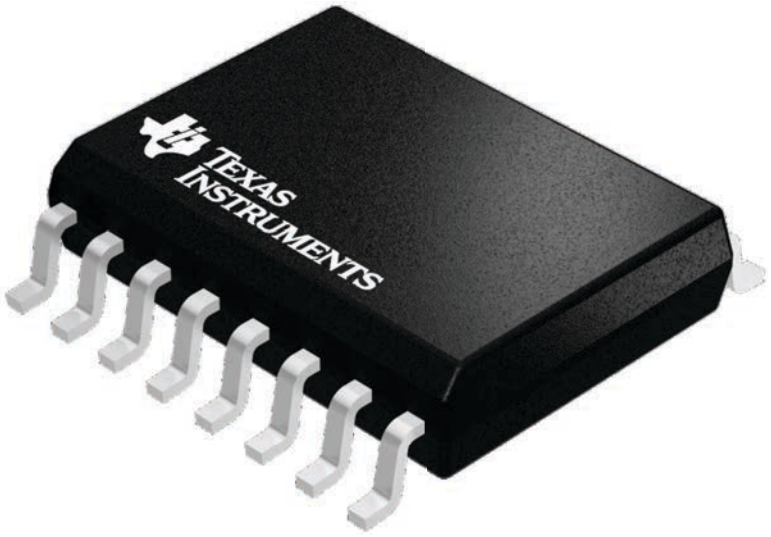
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

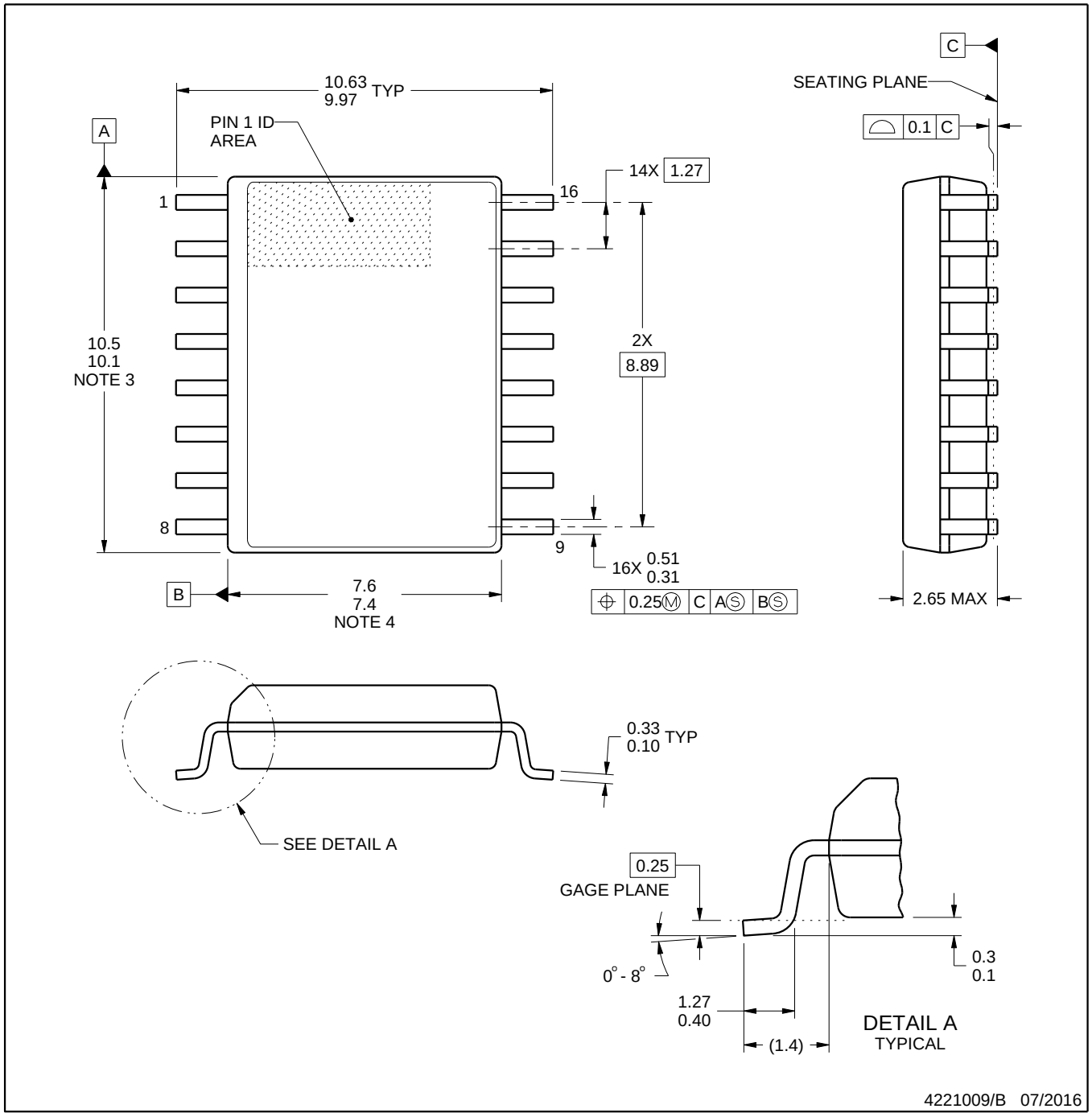
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



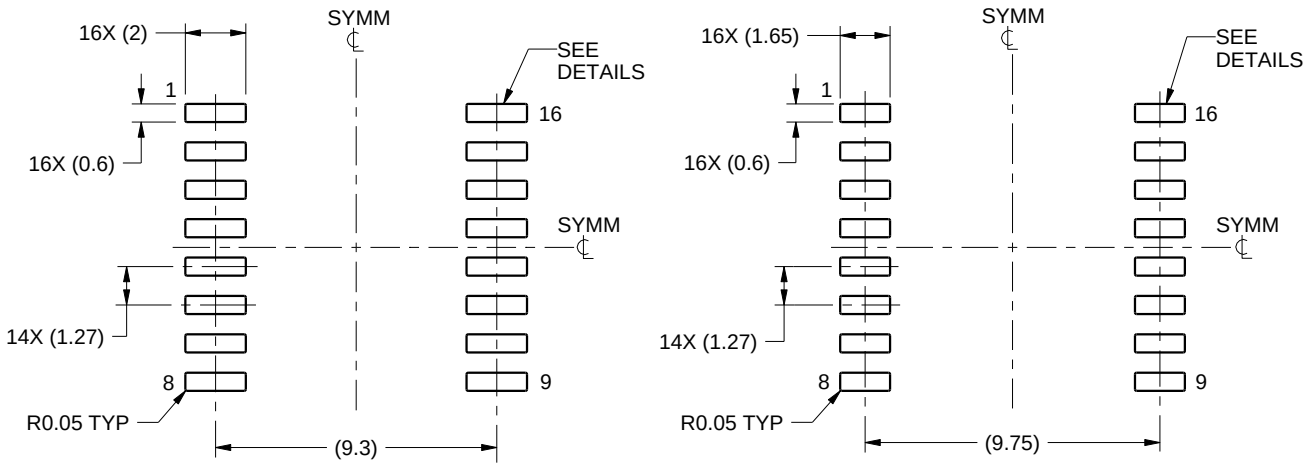
4224780/A

SOIC



NOTES:

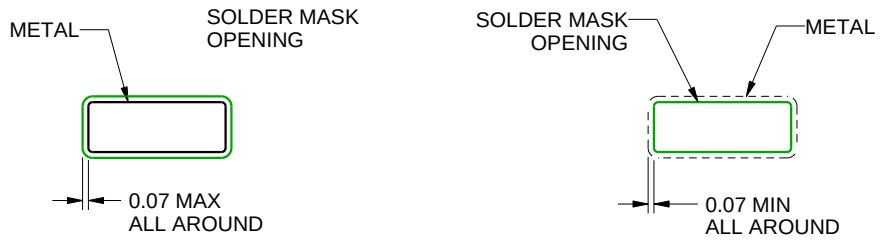
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

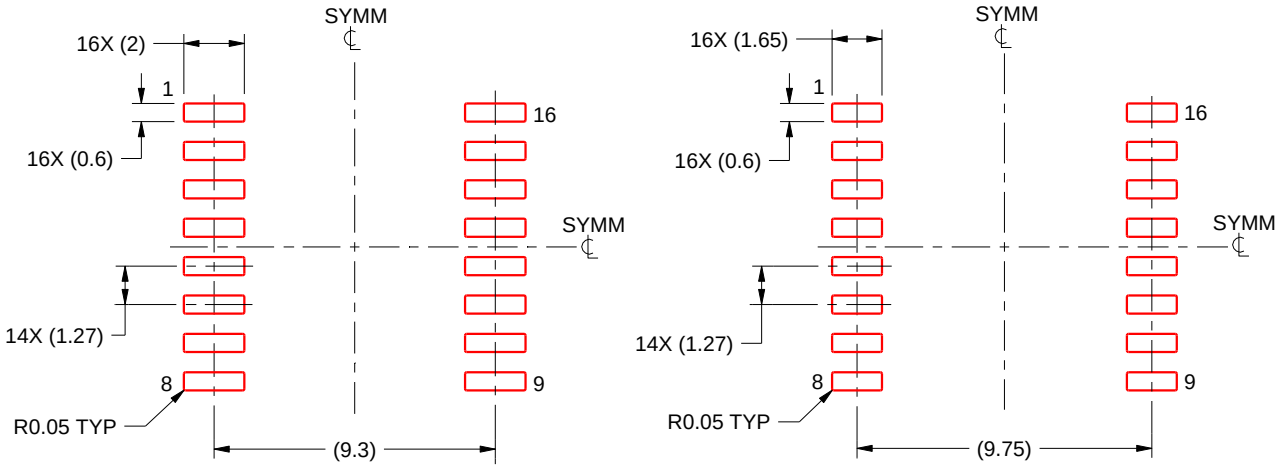
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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