具有 PGA 和电压基准的 ADS125H0x 宽输入范围、2 通道、40kSPS、24 位、Δ-Σ ADC

1 特性

- 宽输入范围、24 位、Δ-Σ ADC
- 1GΩ 输入阻抗 PGA
- 可编程输入电范围：±20mV 至 ±20V
- 绝对输入电压范围：±15.5V
- 高性能：
  - 100dB 共模抑制比
  - 5nV/°C 失调电压温漂
  - 1ppm/°C 增益漂移
  - 2ppm_{FSR} INL
- 可编程数据速率：2.5SPS 至 40000SPS
- 外部或内部 2.5V 基准操作
- 同步 50Hz 和 60Hz 抑制模式
- 信号和基准电压监控器
- 循环冗余校验 (CRC)
- 传感器激励电流源 (H02)
- 内部多路复用器驱动器 GPIOs (H02)
- 5mm × 5mm VQFN 封装

2 应用

- 宽共模电压测量
- 模拟输入 PLC 模块：±10V
- 测试和测量仪器
- 实验室仪表

3 说明

ADS125H01 和 ADS125H02 (ADS125H0x) 是具有宽输入范围、1GΩ 输入阻抗和可编程增益放大器 (PGA) 的 24 位、40kSPS、Δ-Σ 模数转换器 (ADC)。ADC 提供了宽输入范围、高分辨率测量系统，采用紧凑的 5mm × 5mm VQFN 封装。

ADC 将 ±18V PGA 与具有 24 位低噪声 ADC 的精密电压基准融合。ADC 提供了从 ±20mV 到 ±20V 的可编程输入范围，多数情况下无需外部衰减。差动输入 ADC 接受总测量分辨率损耗较少的单端输入配置。

数字滤波器提供同步 50Hz 与 60Hz 线路周期抑制，同时针对 20SPS 以及更低的数据速率进行单周期稳定转换。

信号和基准监控器、温度传感器和 CRC 数据验证可增强数据可靠性。

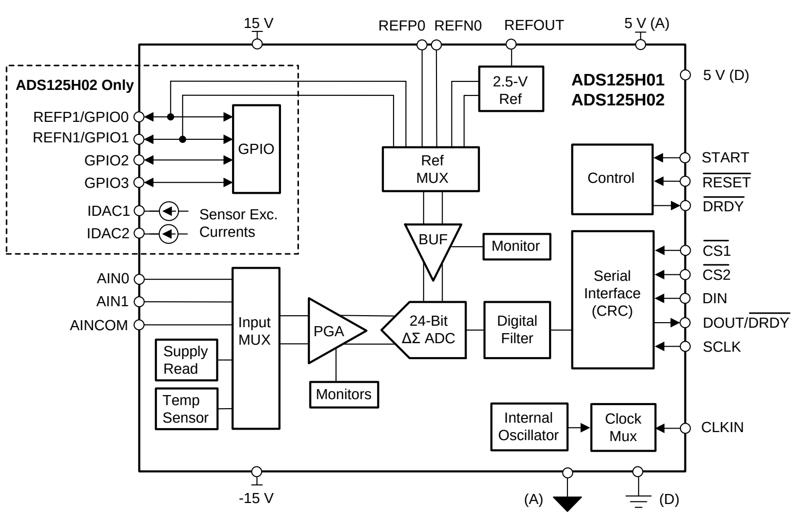
ADS125H01 和 ADS125H02 是引脚兼容器件，额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS125H0x	VQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

功能方框图



ADVANCE INFORMATION

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4 修订历史记录

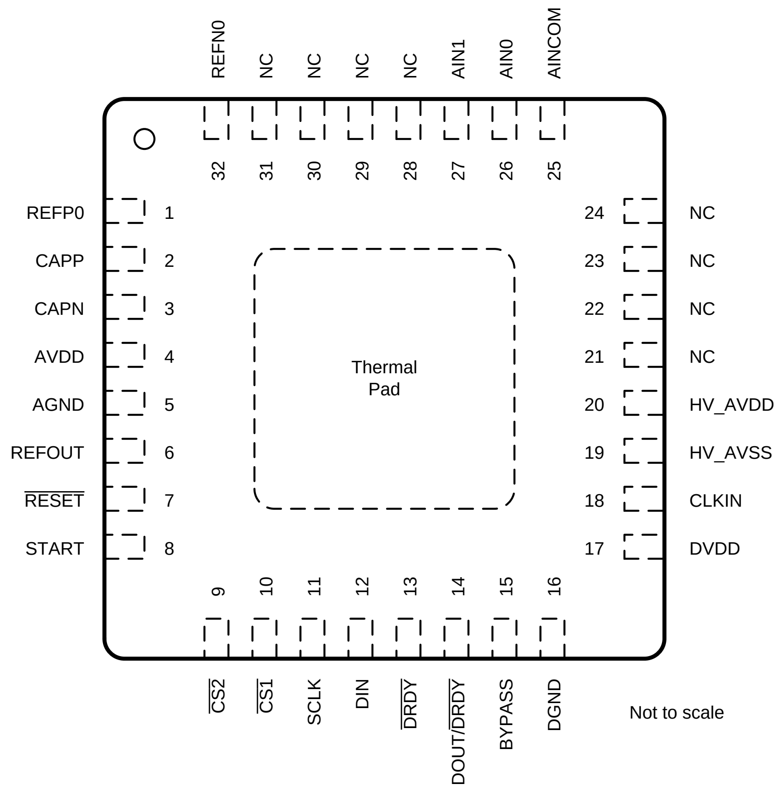
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (October 2018) to Revision A **Page**

- 已更改 *更改了特性 和说明部分的文本* ... 1
- Changed HV_AVSS to AGND minimum specification in *Absolute Maximum Ratings* ... 7
- Added note to Input Current specification in *Absolute Maximum Ratings* ... 7
- Changed HV_AVDD to AGND minimum specification in *Recommended Operating Conditions* ... 8
- Added maximum offset drift specification to *Electrical Characteristics* ... 9
- Added integral nonlinearity maximum specification for gains 64 and 128 in *Electrical Characteristics* ... 9
- Changed offset voltage minimum specification in *Electrical Characteristics* ... 9
- Added internal reference accuracy and drift specifications in *Electrical Characteristics* ... 9
- 已更改 *Effective Resolution* equation to Log_{10} format ... 15
- 已更改 *Typical Noise (e_n) in μV_{RMS} and (μV_{PP})* tables to list noise data under input voltage range ... 15
- 已更改 text of the *Functional Block Diagram* section, moved to *Overview* section ... 19
- 已更改 description of $\overline{CS1}$ and $\overline{CS2}$ operation in *Chip Selects ($\overline{CS1}$) and ($\overline{CS2}$)* section ... 43
- 已删除 Figure 36, *Chip Select Control Options* due to changed chip select operation ... 43
- 已更改 Figure 37, *Register Write Command Sequence* for changed chip select operation ... 47
- 已更改 text in *Input Signal Rate of Change* section ... 67
- 已添加 5-V to ±15-V DC-DC Converter to *Power Supply Recommendations* ... 71

5 Pin Configuration and Functions

RHB Package: ADS125H01
32-Pin VQFN
Top View



Pin Functions: ADS125H01

NO.	NAME	I/O	DESCRIPTION
1	REFP0	Analog input	Reference input 0 positive
2	CAPP	Analog output	PGA output P; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
3	CAPN	Analog output	PGA output N; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
4	AVDD	Analog	Low-voltage analog power supply (5 V)
5	AGND	Analog	Analog ground; connect to the ADC ground plane
6	REFOUT	Analog output	2.5-V reference output; connect a 10-µF capacitor to AGND
7	$\overline{\text{RESET}}$	Digital input	Reset; active low
8	START	Digital input	Conversion start, active high
9	$\overline{\text{CS2}}$	Digital input	Serial interface chip select 2 to select the PGA for communication
10	$\overline{\text{CS1}}$	Digital input	Serial interface chip select 1 to select the ADC for communication
11	SCLK	Digital input	Serial interface shift clock
12	DIN	Digital input	Serial interface data input
13	$\overline{\text{DRDY}}$	Digital output	Data-ready indicator; active low
14	DOUT/$\overline{\text{DRDY}}$	Digital output	Serial interface data output and data-ready indicator (active low)
15	BYPASS	Analog output	2-V subregulator output; connect a 1-µF capacitor to DGND
16	DGND	Digital	Digital ground; connect to the ADC ground plane
17	DVDD	Digital	Digital power supply (3 V to 5 V)
18	CLKIN	Digital input	Internal oscillator; connect to DGND
19	HV_AVSS	Analog	High-voltage negative analog power supply
20	HV_AVDD	Analog	High-voltage positive analog power supply

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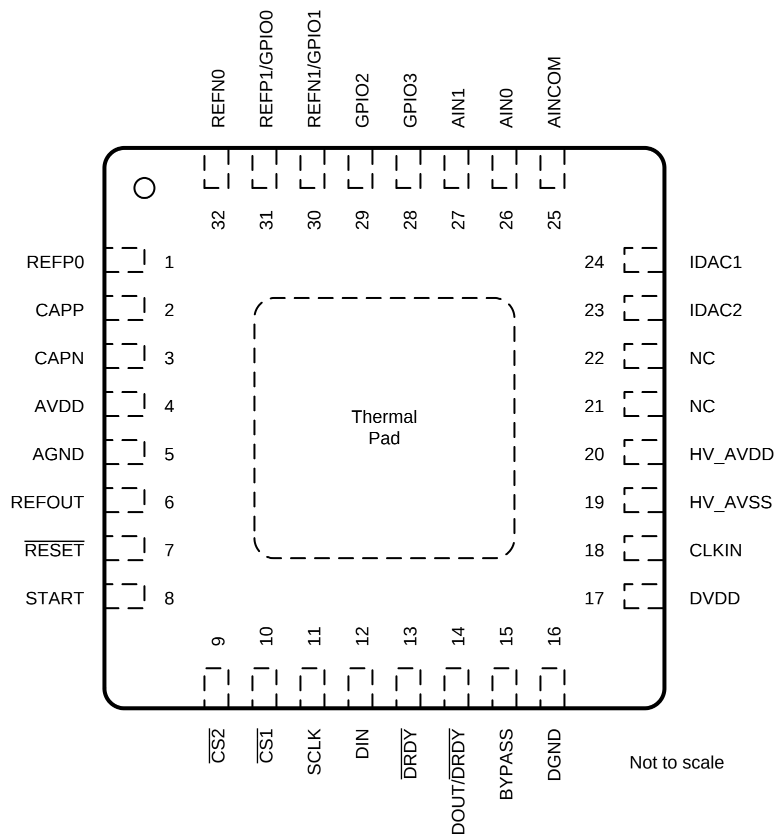
Pin Functions: ADS125H01 (continued)

NO.	NAME	I/O	DESCRIPTION
21, 22	NC	—	No connection; electrically float or tie to AGND
23	NC	Analog output	No connection; electrically float or tie to AGND
24	NC	Analog output	No connection; electrically float or tie to AGND
25	AINCOM	Analog input	Analog input common (single-ended common)
26	AIN0	Analog input	Analog input 0
27	AIN1	Analog input	Analog input 1
28-31	NC	Digital input/output	No connection; electrically float or tie to AGND
32	REFN0	Analog input	Reference input 0 negative
Thermal pad		—	Exposed thermal pad; connect to DGND; see the recommended PCB land pattern at end of the document

RHB Package: ADS125H02
32-Pin VQFN
Top View



Pin Functions: ADS125H02

NO.	NAME	I/O	DESCRIPTION
1	REFP0	Analog input	Reference input 0 positive
2	CAPP	Analog output	PGA output P; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
3	CAPN	Analog output	PGA output N; connect a 1-nF C0G dielectric capacitor from CAPP to CAPN
4	AVDD	Analog	Low-voltage analog power supply (5 V)
5	AGND	Analog	Analog ground; connect to the ADC ground plane
6	REFOUT	Analog output	2.5-V reference output; connect a 10-µF capacitor to AGND
7	$\overline{\text{RESET}}$	Digital input	Reset; active low
8	START	Digital input	Conversion start, active high
9	$\overline{\text{CS2}}$	Digital input	Serial interface chip select 2 to select the PGA for communication
10	$\overline{\text{CS1}}$	Digital input	Serial interface chip select 1 to select the ADC for communication
11	SCLK	Digital input	Serial interface shift clock
12	DIN	Digital input	Serial interface data input
13	$\overline{\text{DRDY}}$	Digital output	Data-ready indicator; active low
14	DOUT/$\overline{\text{DRDY}}$	Digital output	Serial interface data output and data-ready indicator (active low)
15	BYPASS	Analog output	2-V subregulator output; connect a 1-µF capacitor to DGND
16	DGND	Digital	Digital ground; connect to the ADC ground plane
17	DVDD	Digital	Digital power supply (3 V to 5 V)
18	CLKIN	Digital input	External clock; apply the clock input
19	HV_AVSS	Analog	High-voltage negative analog power supply
20	HV_AVDD	Analog	High-voltage positive analog power supply

ADVANCE INFORMATION

Pin Functions: ADS125H02 (continued)

NO.	NAME	I/O	DESCRIPTION
21, 22	NC	—	No connection; electrically float or tie to AGND
23	IDAC2	Analog output	Current source 2 output
24	IDAC1	Analog output	Current source 1 output
25	AINCOM	Analog input	Analog input common (single-ended common)
26	AIN0	Analog input	Analog input 0
27	AIN1	Analog input	Analog input 1
28	GPIO3	Digital input/output	General-purpose input/output 3
29	GPIO2	Digital input/output	General-purpose input/output 2
30	REFN1/GPIO1	Analog, digital input/output	Reference input 1 negative and general-purpose input/output 1
31	REFP1/GPIO0	Analog, digital input/output	Reference input 1 positive and general-purpose input/output 0
32	REFN0	Analog input	Reference input 0 negative
Thermal pad		—	Exposed thermal pad; connect to DGND; see the recommended PCB land pattern at end of the document

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Power-supply voltage	HV_AVDD to HV_AVSS	–0.3	38	V
	HV_AVSS to AGND	–19	0.3	
	AVDD to AGND	-0.3	6	
	DVDD to DGND	–0.3	6	
	AGND to DGND	–0.1	0.1	
Analog input voltage	AIN0, AIN1, AINCOM	HV_AVSS – 0.3	HV_AVDD + 0.3	V
	GPIO[3:0], REFP[1:0], REFN[1:0], IDAC[2:1]	AGND – 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, START, $\overline{RESET}$, CLKIN, $\overline{DRDY}$, DOUT/$\overline{DRDY}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous [(2)]	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to ±10 mA in the event the analog input voltage exceeds HV_AVDD + 0.3 V or HV_AVSS – 0.3 V, or if the reference input, GPIO, or IDAC voltage exceeds AVDD + 0.3 V or AGND – 0.3 V, or if the digital input voltage exceeds DVDD + 0.3 V or DGND – 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [(2)]	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ADVANCE INFORMATION

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-voltage analog power supplies	HV_AVDD to HV_AVSS	10		36	V
		HV_AVSS to AGND	–18		0	V
		HV_AVDD to AGND[(1)]	5		36	V
	Low-voltage analog power supply	AVDD to AGND	4.75	5	5.25	V
	Digital power supply	DVDD to DGND	2.7		5.25	V
SIGNAL INPUTS						
$V_{(AINX)}$	Absolute input voltage		See the *PGA Input Range* section			V
V_{IN}	Differential input voltage range[(2)]	$V_{IN} = V_{AINP} – V_{AINN}$	-20	$\pm V_{REF}$ / gain	20	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Reference voltage input	$V_{REF} = V_{(REFPx)} – V_{(REFNx)}$	0.9		AVDD	V
$V_{(REFNx)}$	Negative reference voltage		AGND – 0.05		$V_{(REFPx)}$ – 0.9	V
$V_{(REFPx)}$	Positive reference voltage		$V_{(REFNx)}$ + 0.9		AVDD + 0.05	V
GENERAL-PURPOSE INPUT/OUTPUTS (GPIOs)						
	Input voltage		AGND		AVDD	V
DIGITAL INPUTS (Other Than GPIOs)						
	Input voltage		DGND		DVDD	V
EXTERNAL CLOCK						
$f_{(CLK)}$	Frequency	2.5 SPS to 25600 SPS	1	7.3728	8	MHz
		40 kSPS	1	10.24	10.75	MHz
	Duty cycle		40%		60%	
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–45		125	°C

(1) HV_AVDD can be connected to AVDD if AVDD ≥ 5 V.
(2) The full available differential input voltage range is limited under certain operating conditions. See the *PGA Input Range* section for details.

6.4 Thermal Information

THERMAL METRIC[(1)]		ADS125H0x RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 V/V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	$V_{(AINx)}$ = 0 V		0.5		nA
	Absolute input current drift			10		pA/°C
	Differential input current	V_{IN} = 2.5 V, Standard mode		±0.1		nA
		V_{IN} = 2.5 V, Chop mode[1]		±5		nA
	Differential input current drift	V_{IN} = 2.5 V, T_A < 105°C		±10		pA/°C
	Differential input impedance			1		GΩ
	Crosstalk			1		µV/V
PGA						
	Gain			0.125, 0.1875, 0.25, 0.5, 1, 2, 4, 8, 16, 32, 64,128		V/V
	Antialias filter			230		kHz
PERFORMANCE						
	Resolution	No missing codes	24			Bits
DR	Data rate		2.5		40000	SPS
	Noise performance			See 表 1 and 表 2		
INL	Integral nonlinearity	Gain = 0.125 to 32		2	10	ppm
		Gain = 64, 128		6	12	ppm
V_{OS}	Offset voltage	T_A = 25°C	–30 - 300 / Gain	±10 + 100 / Gain	30 + 300 / Gain	µV
		Chop mode, T_A = 25°C	–0.5 - 0.5 / Gain	±0.5 / Gain	0.5 + 0.5 / Gain	µV
		After calibration		On the level of noise		
	Offset voltage drift	Gain = 0.125 to 8		200 / Gain	600 / Gain	nV/°C
		Gain = 16 to 128		10	50	nV/°C
		Chop mode		5 / Gain		nV/°C
GE	Gain error	T_A = 25°C, all gains	–0.7%	±0.1%	0.7%	
		After calibration		On the level of noise		
	Gain drift	All gains		1	4	ppm/°C
NMRR	Normal-mode rejection ratio[2]			See 表 7		
CMRR	Common-mode rejection ratio[3]	Data rate = 20 SPS		130		dB
		Data rate = 400 SPS	85	100		dB
PSRR	Power-supply rejection ratio[4]	HV_AVDD, HV_AVSS		2	15	µV/V
		AVDD		5	50	µV/V
		DVDD		3	20	µV/V
VOLTAGE REFERENCE INPUTS						
	Absolute input current			±250		nA
	Input current vs voltage			15		nA/V
	Input current drift			0.2		nA/°C
	Input impedance	Differential		30		MΩ

(1) Input current in chop mode operation scales with the data rate. See graph TBD.
(2) Normal-mode rejection ratio performance is dependent on the digital filter configuration.
(3) Common-mode rejection ratio is specified at 60 Hz.
(4) Power-supply rejection ratio is specified at dc.

ADVANCE INFORMATION

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCE(5)						
	Voltage			2.5		V
	Initial error	T_A = 25°C	-0.2%	±0.1%	0.2%	
	Temperature drift	T_A = 0°C to 85°C		2	9	ppm/°C
		T_A = –40°C to 125°C		5	15	
	Long term drift	T_A = 85°C, 1st 1000 hr		TBD		ppm
	Thermal hysteresis(6)	First 0°C to 105°C cycle		±70		ppm
		Second 0°C to 105°C cycle		±25		
	Output current		–10		10	mA
	Load regulation			20		µV/mA
	Start-up time	Settling to ±0.001% final value		100		ms
TEMPERATURE SENSOR						
	Voltage	T_A = 25°C		122.4		mV
	Temperature coefficient			420		µV/°C
EXCITATION CURRENT SOURCES (IDACS)						
	Currents		50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000			µA
	Compliance range	All currents	AGND		AVDD – 1.1	V
	Absolute error	All currents	–5%	±0.7%	5%	
	Match error	Same current magnitudes	–1.5%	±0.1%	1.5%	
		Different current magnitudes		±1%		
	Temperature drift	Absolute		100		ppm/°C
		Matched values		5	TBD	
PGA MONITORS (7)						
	Input low threshold			HV_AVSS + 2		V
	Input high threshold			HV_AVDD – 2		V
	Output low threshold			HV_AVSS + 2		V
	Output high threshold			HV_AVDD – 2		V
REFERENCE MONITOR						
	Low voltage threshold			0.4	0.6	V
INTERNAL OSCILLATOR						
f_{CLK}	Frequency	2.5-SPS to 25600-SPS operation		7.3728		MHz
		40-kSPS operation		10.24		
	Accuracy			±0.5%	±2%	
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × AVDD	V
V_{IH}	High-level input voltage		0.7 × AVDD		AVDD	V
V_{IL}	Low-level input voltage		AGND		0.3 × AVDD	V
	Input hysteresis			0.5		V

(5) Soldered to the PCB using the recommended PCB layout pattern and using the reflow profile as per JEDEC standard J-STD-020D.1
(6) Voltage reference hysteresis is measured by operating the device at 25°C, cycling the device to 0°C and 105°C, and returning the device to 25°C.
(7) See the *PGA Monitor* section for details.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at HV_AVDD = 15 V, HV_AVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and gain = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS (OTHER THAN GPIOs)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
		I_{OH} = 8 mA		0.75 × DVDD		
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 × DVDD	V
		I_{OL} = –8 mA		0.2 × DVDD		
V_{IH}	High-level input voltage		0.7 ×DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3 × DVDD	V
	Input hysteresis			0.1		V
	Input leakage				±1	µA
POWER SUPPLY						
I_{HV_AVDD} I_{HV_AVSS}	HV_AVDD, HV_AVSS supply current			1.1	1.8	mA
I_{AVDD}	AVDD supply current			2.8	4.6	mA
	Additional AVDD supply current (by function)	Voltage reference		0.2		mA
		40-kSPS operation		1		
		Current sources		As programmed		µA
I_{DVDD}	DVDD supply current			0.5	0.7	mA
		40-kSPS operation		0.7	0.9	
P_D	Power dissipation			50	80	mW

6.6 Timing Requirements

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V

		MIN	MAX	UNIT
SERIAL INTERFACE				
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS1}$ or $\overline{CS2}$ falling edge	50		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	25		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns
$t_{c(SC)}$	SCLK period	97		ns
$t_{w(SCH)}$, $t_{w(SCL)}$	Pulse duration, SCLK high or low	40		ns
$t_{d(SCCS)}$	Delay time, last SCLK falling edge before $\overline{CS1}$ or $\overline{CS2}$ rising edge	50		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS1}$ or $\overline{CS2}$ high to reset interface	25		ns
RESET				
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	4		1 / f_{CLK}
CONVERSION CONTROL				
$t_{w(STH)}$	Pulse duration, START high	4		1 / f_{CLK}
$t_{w(STL)}$	Pulse duration: START low	4		1 / f_{CLK}
$t_{su(STDR)}$	Set-up time, START low or STOP command before $\overline{DRDY}$ low to stop the next conversion (continuous mode)		100	1 / f_{CLK}
$t_{h(DRSP)}$	Hold time, START low or STOP command after $\overline{DRDY}$ low to continue the next conversion (continuous mode)	150		1 / f_{CLK}

ADVANCE INFORMATION

6.7 Switching Characteristics

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V, and DOUT/$\overline{DRDY}$ load = 20 pF || 100 kΩ to DGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE						
$t_{w(DRH)}$	Pulse duration: $\overline{DRDY}$ high		16			1 / f_{CLK}
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS1}$ or $\overline{CS2}$ falling edge to DOUT/$\overline{DRDY}$ driven		0		50	ns
$t_{p(SCDO1)}$	Propagation delay time, SCLK rising edge to valid DOUT/$\overline{DRDY}$				40	ns
$t_{h(SCDO1)}$	Hold time, SCLK rising edge to invalid DOUT/$\overline{DRDY}$		0			ns
$t_{h(SCDO2)}$	Hold time, last SCLK falling edge to invalid DOUT/$\overline{DRDY}$ data output function		15			ns
$t_{p(SCDO2)}$	Propagation delay time, last SCLK falling edge to DOUT/$\overline{DRDY}$ data-ready function				110	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS1}$ or $\overline{CS2}$ rising edge to DOUT/$\overline{DRDY}$ high impedance				50	ns
RESET						
$t_{p(RSCN)}$	Propagation delay time, $\overline{RESET}$ rising edge or RESET command to conversion start		512			1 / f_{CLK}
$t_{p(PRCM)}$	Propagation delay time, power-on threshold voltage to ADC communication			2^{16}		1 / f_{CLK}
$t_{p(CMCN)}$	Propagation delay time, ADC communication to conversion start		512			1 / f_{CLK}
AC EXCITATION						
$t_{d(ACX)}$	Delay time, phase-to-phase blank period			8		1 / f_{CLK}
$t_{c(ACX)}$	ACX period		2			t_{STDR}
CONVERSION CONTROL						
$t_{p(STDR)}$	Propagation delay time, START pin high or START command to $\overline{DRDY}$ high				2	1 / f_{CLK}

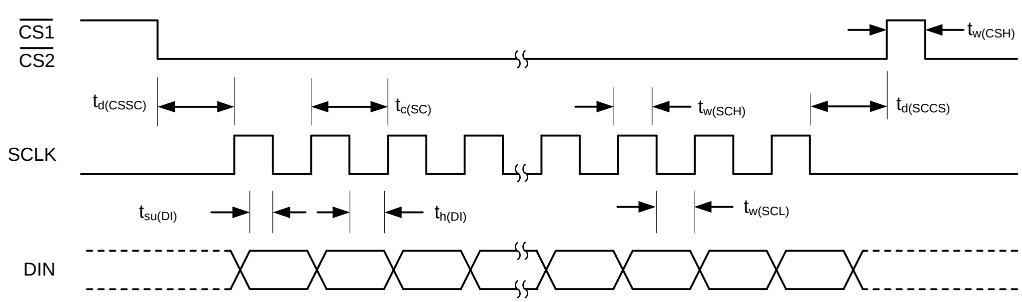
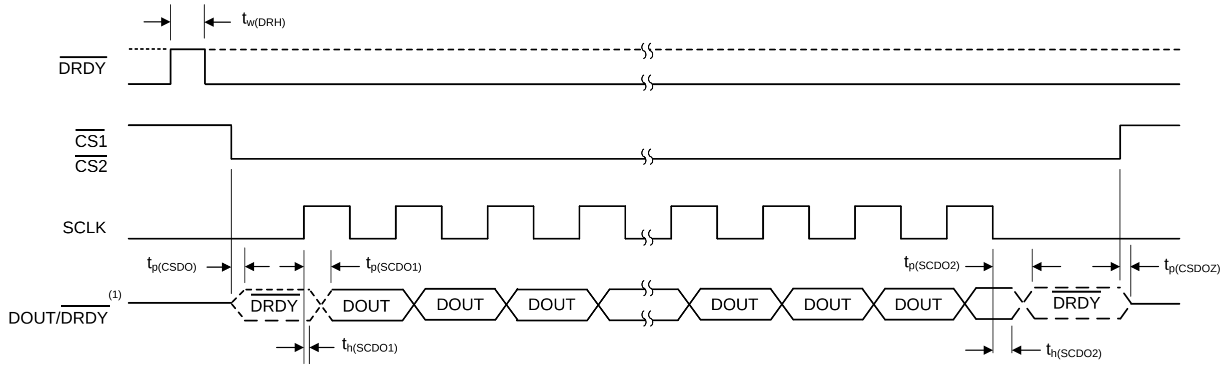


图 1. Serial Interface Timing Requirements



(1) DRDY is the data-ready functionality of this pin over the time interval between CS1 low and the first SCLK rising edge, and over the time interval between the last SCLK falling edge of the command to CS1 high. DOUT is the data-output functionality of this pin that occurs during the data-read operation.

图 2. Serial Interface Switching Characteristics

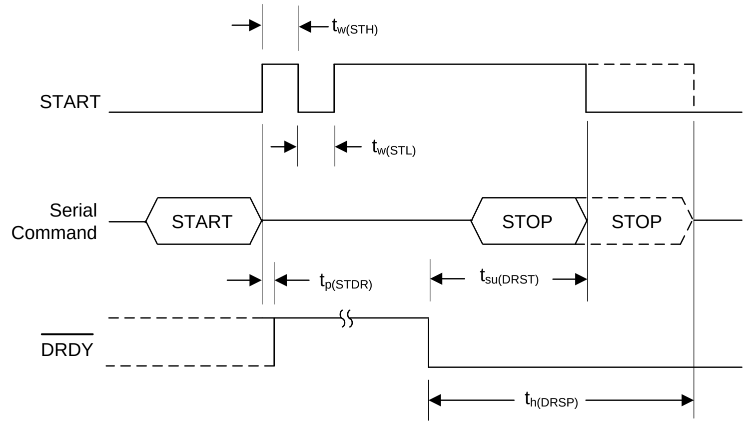


图 3. Conversion Control Timing Requirements

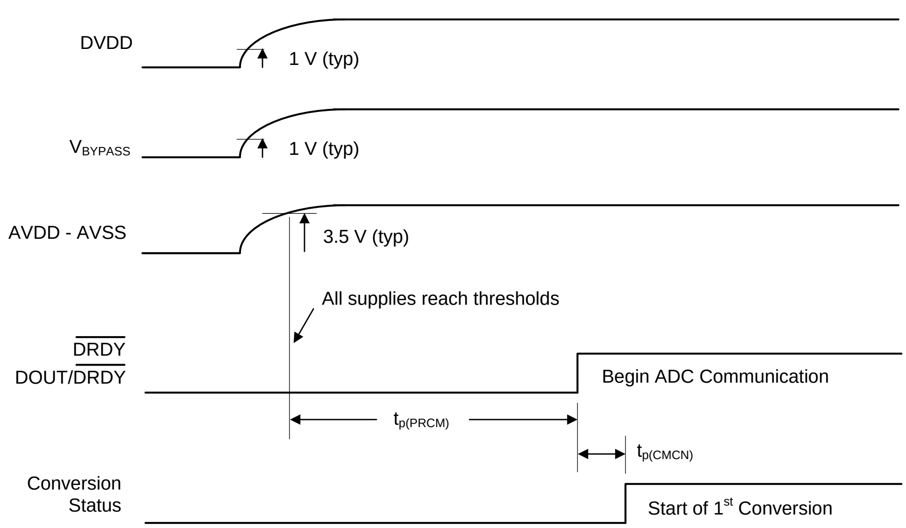


图 4. Power-Up Characteristics

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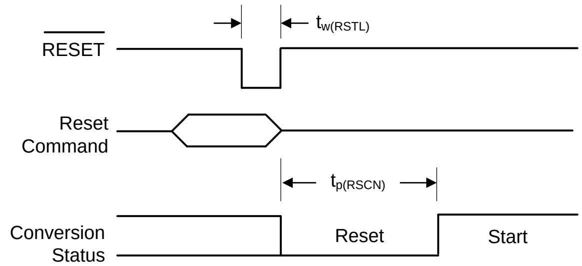

图 5. RESET Pin and Reset Command Timing Requirements

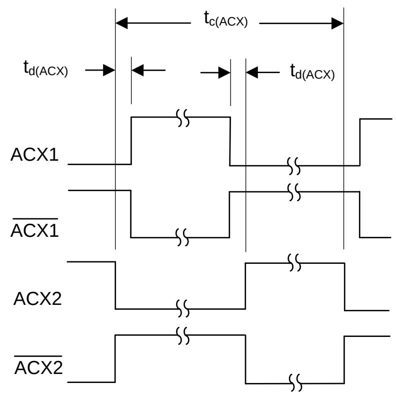

图 6. AC-Excitation Timing Characteristics

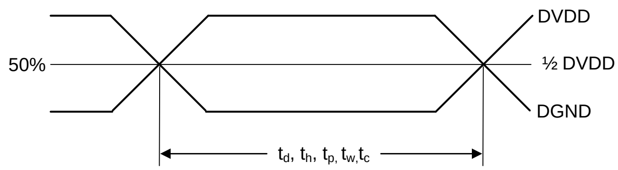

图 7. Timing Reference

7 Parameter Measurement Information

7.1 Noise Performance

The ADS125H0x noise performance depends on the device configuration: data rate, PGA gain, digital filter configuration, and chop mode. Two large factors on noise performance are data rate and PGA gain. Deceasing the data rate results in a proportional decrease in total noise because the noise profile of the ADC is predominantly white (flat versus frequency). Increasing the gain reduces noise when treated as an input-referred quantity because the noise of the PGA is lower than that of the ADC. Noise performance also depends on the digital filter and chop mode. As the order of the digital filter increases, the noise bandwidth correspondingly decreases, which results in lower noise. As a result of two-point data averaging in chop mode, noise performance improves by $\sqrt{2}$ compared to the normal operating mode.

表 1 shows noise performance for gains of 0.125 to 2 as input-referred values. 表 2 shows noise performance for gains of 4 to 128. The noise performance data are in units of μV_{RMS} (RMS = root mean square) under the conditions listed. Values in parenthesis are peak-to-peak values.

The data shown in the noise performance tables represent typical ADC performance at T_A = 25°C, 2.5-V reference voltage, and chop mode disabled. The noise-performance data are the standard deviation and peak-to-peak computations of the ADC data. The noise data are acquired with inputs shorted, based on consecutive ADC readings for a period of ten seconds or 8192 data points, whichever occurs first. Because of the statistical nature of noise, repeated noise measurements may yield higher or lower noise performance results. Long periods of data acquisition may result in increased peak-to-peak noise results.

Effective resolution (bits) and noise-free resolution (resolution with no code flicker) performance are calculated using 公式 1:

$$\text{Effective Resolution or Noise-Free Resolution (Bits)} = 3.32 \log (FSR / e_n) \quad (1)$$

where:

- FSR = Full-scale range = 2 · V_{REF} / Gain (see the *PGA Input Range* section for the corresponding gain for each range and conditions that limit FSR)
- e_n = Input-referred voltage noise (use the $e_{n(RMS)}$ value to calculate effective resolution, use the $e_{n(PP)}$ value to calculate noise-free resolution)

Use the noise values listed in 表 1 and 表 2 with the desired data rate, filter mode and input voltage range to determine effective resolution (bits). For example, at input voltage range = ±13.3 V, data rate = 20 SPS, and FIR filter mode, the typical RMS value of the input-referred noise voltage is 2.1 µV. The effective resolution with this ADC operation is 23.6 bits.

表 1. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}) for Input Voltage Ranges ±20 V to ±1.25 V

DATA RATE (SPS)	FILTER MODE	INPUT VOLTAGE RANGE					
		±20 V	±13.3 V	±10 V	±5 V	±2.5 V	±1.25 V
2.5	FIR	1.3 (4.8)	0.89 (3.6)	0.69 (2.1)	0.49 (1.9)	0.37 (1.5)	0.17 (0.67)
2.5	Sinc1	1.1 (4.2)	0.6 (2.4)	0.57 (2.4)	0.39 (1.5)	0.29 (1)	0.15 (0.63)
2.5	Sinc2	1 (3.6)	0.68 (2)	0.44 (1.8)	0.32 (1)	0.26 (0.97)	0.12 (0.52)
2.5	Sinc3	1.1 (3)	0.67 (2)	0.49 (1.5)	0.32 (1)	0.24 (0.89)	0.11 (0.41)
2.5	Sinc4	0.98 (3.6)	0.64 (2)	0.48 (1.2)	0.3 (1)	0.26 (0.97)	0.11 (0.41)
5	FIR	1.7 (6.6)	1.2 (4.8)	0.93 (4.2)	0.57 (2.5)	0.45 (2)	0.24 (1.2)
5	Sinc1	1.5 (6.6)	0.98 (3.6)	0.77 (3.6)	0.53 (2.2)	0.4 (1.9)	0.2 (0.93)
5	Sinc2	1.3 (4.8)	0.91 (4)	0.68 (2.4)	0.44 (1.8)	0.35 (1.6)	0.18 (0.82)
5	Sinc3	1.2 (4.8)	0.83 (3.2)	0.62 (2.4)	0.39 (1.6)	0.3 (1.3)	0.16 (0.75)
5	Sinc4	1.2 (3.6)	0.75 (3.2)	0.54 (2.1)	0.38 (1.5)	0.27 (1.2)	0.14 (0.56)
10	FIR	2.4 (11)	1.6 (7.9)	1.2 (5.7)	0.82 (4.3)	0.69 (3.3)	0.34 (1.7)
10	Sinc1	1.9 (9.5)	1.4 (6.8)	1.1 (5.4)	0.7 (3.4)	0.55 (2.7)	0.3 (1.5)
10	Sinc2	1.7 (8.9)	1.2 (5.6)	0.9 (4.5)	0.56 (2.7)	0.47 (2.3)	0.24 (1.2)
10	Sinc3	1.5 (6.6)	1.1 (5.2)	0.89 (4.2)	0.54 (2.7)	0.46 (2.5)	0.24 (1.1)
10	Sinc4	1.5 (6.6)	0.99 (4.4)	0.79 (3.6)	0.49 (2.4)	0.39 (1.9)	0.2 (1)
16.6	Sinc1	2.6 (11)	1.7 (8.7)	1.4 (6.6)	0.87 (4.5)	0.72 (3.5)	0.37 (2)

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Noise Performance (接下页)

表 1. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}) for Input Voltage Ranges ±20 V to ±1.25 V (接下页)

DATA RATE (SPS)	FILTER MODE	INPUT VOLTAGE RANGE					
		±20 V	±13.3 V	±10 V	±5 V	±2.5 V	±1.25 V
16.6	Sinc2	2.1 (10)	1.5 (7.5)	1.1 (5.7)	0.78 (3.7)	0.62 (3.2)	0.32 (1.6)
16.6	Sinc3	1.9 (9.5)	1.4 (7.2)	1.1 (5.1)	0.72 (3.6)	0.54 (2.5)	0.27 (1.3)
16.6	Sinc4	1.8 (7.7)	1.3 (6.4)	0.97 (4.8)	0.65 (3.1)	0.48 (2.5)	0.24 (1.2)
20	FIR	3 (15)	2.1 (11)	1.8 (8.6)	1.1 (5.2)	0.89 (4.8)	0.46 (2.6)
20	Sinc1	2.7 (13)	1.9 (9.5)	1.5 (7.5)	0.97 (5.5)	0.76 (4.2)	0.43 (2.3)
20	Sinc2	2.2 (11)	1.5 (7.2)	1.3 (6)	0.83 (4.2)	0.69 (3.7)	0.35 (1.8)
20	Sinc3	2.1 (10)	1.6 (8.3)	1.2 (5.4)	0.77 (4)	0.64 (3.1)	0.31 (1.6)
20	Sinc4	2 (9.5)	1.3 (6.8)	1.1 (4.8)	0.65 (3.1)	0.56 (2.7)	0.28 (1.4)
50	Sinc1	4.1 (24)	2.9 (17)	2.3 (14)	1.5 (7.7)	1.2 (7.5)	0.64 (3.7)
50	Sinc2	3.2 (18)	2.3 (12)	1.9 (11)	1.3 (7)	1.1 (5.8)	0.54 (3.1)
50	Sinc3	3.3 (18)	2.2 (13)	1.8 (9.2)	1.2 (6.7)	0.93 (5.3)	0.49 (3)
50	Sinc4	3.1 (17)	2 (11)	1.6 (8.3)	1 (5.8)	0.87 (4.7)	0.43 (2.4)
60	Sinc1	4.5 (27)	3.1 (17)	2.4 (13)	1.6 (9.2)	1.4 (8.3)	0.69 (3.8)
60	Sinc2	3.8 (23)	2.6 (14)	2.1 (11)	1.4 (7.3)	1.2 (5.9)	0.57 (3.1)
60	Sinc3	3.4 (19)	2.3 (13)	1.8 (9.2)	1.3 (6.9)	1 (5.4)	0.54 (3.1)
60	Sinc4	3.3 (18)	2.1 (12)	1.9 (9.8)	1.2 (6.6)	0.95 (5.2)	0.52 (2.8)
100	Sinc1	5.6 (34)	4.1 (23)	3.3 (20)	2.1 (12)	1.8 (9.7)	0.91 (5.7)
100	Sinc2	4.9 (30)	3.4 (21)	2.7 (16)	1.8 (11)	1.5 (8.7)	0.75 (4.4)
100	Sinc3	4.4 (26)	3.1 (18)	2.5 (14)	1.7 (10)	1.3 (8.2)	0.69 (4.2)
100	Sinc4	4.1 (24)	2.9 (17)	2.3 (14)	1.5 (8.5)	1.3 (7.7)	0.63 (4)
400	Sinc1	12 (74)	8.1 (55)	6.4 (43)	4.3 (27)	3.6 (25)	1.8 (11)
400	Sinc2	9.3 (60)	6.7 (44)	5.3 (32)	3.5 (23)	2.9 (19)	1.5 (10)
400	Sinc3	8.6 (54)	6.2 (39)	4.9 (32)	3.2 (20)	2.7 (17)	1.4 (9.1)
400	Sinc4	8 (52)	5.6 (37)	4.5 (30)	3 (20)	2.5 (16)	1.3 (8.3)
1200	Sinc1	20 (140)	14 (98)	11 (75)	7.3 (48)	6 (40)	3.1 (20)
1200	Sinc2	17 (110)	12 (78)	9.2 (62)	6.1 (41)	5 (33)	2.6 (18)
1200	Sinc3	15 (100)	11 (72)	8.4 (56)	5.6 (37)	4.6 (31)	2.4 (16)
1200	Sinc4	14 (95)	9.9 (68)	7.8 (51)	5.2 (37)	4.3 (29)	2.2 (15)
2400	Sinc1	27 (200)	19 (140)	15 (110)	10 (72)	8.3 (60)	4.2 (30)
2400	Sinc2	23 (180)	16 (120)	13 (97)	8.7 (62)	7 (53)	3.6 (26)
2400	Sinc3	21 (160)	15 (110)	12 (94)	7.9 (59)	6.5 (50)	3.3 (23)
2400	Sinc4	20 (140)	14 (100)	11 (78)	7.3 (53)	6 (43)	3.1 (22)
4800	Sinc1	37 (270)	26 (200)	21 (160)	14 (110)	11 (83)	5.6 (42)
4800	Sinc2	33 (250)	23 (170)	18 (140)	12 (88)	9.8 (73)	5 (40)
4800	Sinc3	31 (230)	21 (150)	17 (130)	11 (83)	9 (65)	4.7 (36)
4800	Sinc4	29 (220)	20 (150)	16 (120)	11 (81)	8.5 (63)	4.4 (33)
7200	Sinc1	44 (330)	31 (230)	24 (180)	16 (120)	13 (98)	6.5 (48)
7200	Sinc2	39 (300)	28 (210)	22 (170)	14 (100)	12 (90)	5.9 (46)
7200	Sinc3	37 (280)	26 (200)	21 (160)	13 (100)	11 (82)	5.5 (41)
7200	Sinc4	35 (260)	25 (180)	20 (150)	13 (95)	10 (81)	5.3 (41)
14400	Sinc5	53 (430)	36 (290)	29 (220)	18 (140)	14 (120)	7.4 (58)
19200	Sinc5	72 (560)	50 (390)	39 (320)	23 (180)	17 (130)	8.8 (71)
25600	Sinc5	150 (1300)	100 (870)	79 (640)	42 (350)	26 (220)	13 (110)
40000	Sinc5	250 (2000)	160 (1300)	120 (1000)	65 (530)	37 (310)	19 (150)

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表 2. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}) for Input Voltage Ranges ±625 mV to ±19.5 mV

DATA RATE (SPS)	FILTER MODE	INPUT VOLTAGE RANGE					
		±625 mV	±312 mV	±156 mV	±78.1 mV	±39.1 mV	±19.5 mV
2.5	FIR	0.082 (0.35)	0.051 (0.2)	0.032 (0.14)	0.027 (0.11)	0.027 (0.1)	0.029 (0.12)
2.5	Sinc1	0.088 (0.35)	0.05 (0.19)	0.024 (0.089)	0.024 (0.089)	0.023 (0.098)	0.024 (0.1)
2.5	Sinc2	0.059 (0.24)	0.037 (0.14)	0.021 (0.084)	0.018 (0.072)	0.017 (0.076)	0.019 (0.076)
2.5	Sinc3	0.06 (0.24)	0.034 (0.13)	0.019 (0.075)	0.017 (0.07)	0.016 (0.073)	0.018 (0.075)
2.5	Sinc4	0.054 (0.19)	0.034 (0.13)	0.019 (0.075)	0.016 (0.065)	0.015 (0.062)	0.016 (0.069)
5	FIR	0.12 (0.52)	0.071 (0.33)	0.046 (0.21)	0.038 (0.19)	0.039 (0.17)	0.037 (0.18)
5	Sinc1	0.11 (0.48)	0.061 (0.28)	0.038 (0.18)	0.029 (0.14)	0.029 (0.15)	0.029 (0.13)
5	Sinc2	0.093 (0.43)	0.048 (0.21)	0.029 (0.14)	0.024 (0.11)	0.026 (0.12)	0.023 (0.1)
5	Sinc3	0.081 (0.41)	0.044 (0.2)	0.03 (0.13)	0.023 (0.1)	0.022 (0.1)	0.022 (0.11)
5	Sinc4	0.066 (0.3)	0.043 (0.2)	0.027 (0.13)	0.022 (0.093)	0.022 (0.11)	0.021 (0.096)
10	FIR	0.19 (1)	0.099 (0.51)	0.064 (0.36)	0.053 (0.29)	0.051 (0.3)	0.054 (0.3)
10	Sinc1	0.16 (0.82)	0.086 (0.46)	0.054 (0.3)	0.045 (0.22)	0.043 (0.21)	0.044 (0.23)
10	Sinc2	0.12 (0.56)	0.068 (0.36)	0.044 (0.23)	0.037 (0.2)	0.034 (0.18)	0.033 (0.18)
10	Sinc3	0.11 (0.52)	0.066 (0.31)	0.042 (0.21)	0.032 (0.17)	0.032 (0.16)	0.032 (0.16)
10	Sinc4	0.096 (0.45)	0.059 (0.31)	0.039 (0.2)	0.032 (0.17)	0.031 (0.16)	0.03 (0.15)
16.6	Sinc1	0.19 (1)	0.11 (0.56)	0.075 (0.38)	0.054 (0.3)	0.055 (0.29)	0.056 (0.31)
16.6	Sinc2	0.16 (0.89)	0.086 (0.4)	0.054 (0.27)	0.044 (0.22)	0.049 (0.24)	0.046 (0.24)
16.6	Sinc3	0.15 (0.73)	0.084 (0.41)	0.053 (0.27)	0.041 (0.22)	0.04 (0.22)	0.041 (0.2)
16.6	Sinc4	0.13 (0.67)	0.076 (0.39)	0.053 (0.29)	0.042 (0.24)	0.04 (0.21)	0.036 (0.17)
20	FIR	0.24 (1.2)	0.14 (0.72)	0.088 (0.45)	0.072 (0.38)	0.071 (0.37)	0.074 (0.37)
20	Sinc1	0.22 (1.1)	0.12 (0.58)	0.079 (0.41)	0.064 (0.32)	0.061 (0.32)	0.06 (0.34)
20	Sinc2	0.18 (1)	0.1 (0.57)	0.062 (0.34)	0.049 (0.25)	0.049 (0.26)	0.047 (0.29)
20	Sinc3	0.16 (0.89)	0.089 (0.48)	0.063 (0.32)	0.046 (0.22)	0.045 (0.21)	0.045 (0.23)
20	Sinc4	0.15 (0.82)	0.083 (0.41)	0.056 (0.29)	0.045 (0.23)	0.042 (0.22)	0.046 (0.24)
50	Sinc1	0.35 (2.1)	0.19 (1.1)	0.12 (0.69)	0.097 (0.52)	0.096 (0.57)	0.098 (0.58)
50	Sinc2	0.28 (1.6)	0.15 (0.84)	0.099 (0.56)	0.075 (0.43)	0.077 (0.43)	0.076 (0.46)
50	Sinc3	0.25 (1.5)	0.14 (0.75)	0.093 (0.51)	0.074 (0.41)	0.07 (0.38)	0.071 (0.37)
50	Sinc4	0.23 (1.4)	0.13 (0.76)	0.087 (0.47)	0.066 (0.37)	0.065 (0.35)	0.065 (0.37)
60	Sinc1	0.38 (2.2)	0.21 (1.2)	0.14 (0.79)	0.11 (0.57)	0.1 (0.59)	0.1 (0.6)
60	Sinc2	0.3 (1.7)	0.17 (0.93)	0.11 (0.66)	0.085 (0.47)	0.084 (0.49)	0.083 (0.49)
60	Sinc3	0.27 (1.6)	0.15 (0.79)	0.097 (0.53)	0.078 (0.43)	0.078 (0.43)	0.076 (0.42)
60	Sinc4	0.27 (1.6)	0.14 (0.89)	0.092 (0.5)	0.075 (0.46)	0.076 (0.4)	0.073 (0.4)
100	Sinc1	0.49 (2.8)	0.27 (1.5)	0.17 (1)	0.14 (0.81)	0.14 (0.88)	0.13 (0.81)
100	Sinc2	0.39 (2.3)	0.22 (1.4)	0.14 (0.87)	0.11 (0.63)	0.11 (0.69)	0.11 (0.66)
100	Sinc3	0.35 (2.1)	0.2 (1.2)	0.13 (0.75)	0.1 (0.63)	0.1 (0.61)	0.1 (0.69)
100	Sinc4	0.32 (2)	0.18 (1.2)	0.13 (0.73)	0.094 (0.57)	0.092 (0.56)	0.093 (0.57)
400	Sinc1	0.94 (6)	0.53 (3.5)	0.34 (2.1)	0.27 (1.8)	0.27 (1.7)	0.27 (1.8)
400	Sinc2	0.78 (5.2)	0.44 (3.1)	0.29 (1.8)	0.22 (1.4)	0.22 (1.4)	0.22 (1.4)
400	Sinc3	0.72 (4.6)	0.4 (2.6)	0.26 (1.6)	0.2 (1.3)	0.2 (1.3)	0.2 (1.3)
400	Sinc4	0.67 (4.2)	0.37 (2.4)	0.24 (1.6)	0.19 (1.2)	0.19 (1.2)	0.19 (1.1)
1200	Sinc1	1.6 (12)	0.91 (6.3)	0.59 (4.1)	0.46 (3.1)	0.45 (3.1)	0.45 (3.1)
1200	Sinc2	1.3 (9.3)	0.76 (5.2)	0.49 (3.2)	0.39 (2.6)	0.38 (2.6)	0.38 (2.6)
1200	Sinc3	1.2 (8.2)	0.69 (4.7)	0.45 (3.1)	0.35 (2.4)	0.35 (2.4)	0.35 (2.2)
1200	Sinc4	1.2 (7.6)	0.64 (4.3)	0.41 (2.7)	0.33 (2.3)	0.32 (2.2)	0.32 (2.3)
2400	Sinc1	2.2 (17)	1.2 (8.9)	0.81 (5.8)	0.64 (4.5)	0.62 (4.5)	0.62 (4.6)
2400	Sinc2	1.9 (14)	1.1 (7.7)	0.68 (5)	0.54 (3.9)	0.54 (3.9)	0.54 (4)

表 2. Typical Noise (e_n) in μV_{RMS} and (μV_{PP}) for Input Voltage Ranges ±625 mV to ±19.5 mV (接下页)

DATA RATE (SPS)	FILTER MODE	INPUT VOLTAGE RANGE					
		±625 mV	±312 mV	±156 mV	±78.1 mV	±39.1 mV	±19.5 mV
2400	Sinc3	1.7 (14)	0.97 (7.1)	0.62 (4.4)	0.49 (3.5)	0.48 (3.4)	0.49 (3.5)
2400	Sinc4	1.6 (12)	0.91 (6.7)	0.59 (4.1)	0.46 (3.5)	0.46 (3.4)	0.46 (3.4)
4800	Sinc1	3 (23)	1.6 (13)	1.1 (7.8)	0.83 (6.2)	0.83 (6.2)	0.82 (6.1)
4800	Sinc2	2.6 (20)	1.5 (12)	0.95 (7.2)	0.75 (5.6)	0.74 (5.4)	0.73 (5.5)
4800	Sinc3	2.4 (19)	1.4 (10)	0.89 (6.4)	0.69 (5)	0.68 (5.2)	0.69 (5.5)
4800	Sinc4	2.3 (17)	1.3 (9.8)	0.82 (6.2)	0.64 (5)	0.65 (4.9)	0.64 (4.9)
7200	Sinc1	3.3 (25)	1.9 (15)	1.2 (9)	0.95 (7)	0.94 (6.9)	0.94 (7.1)
7200	Sinc2	3.1 (24)	1.7 (13)	1.1 (8.7)	0.87 (6.6)	0.86 (6.5)	0.86 (6.4)
7200	Sinc3	2.9 (22)	1.6 (12)	1.1 (7.9)	0.83 (6.1)	0.82 (6.2)	0.82 (6.4)
7200	Sinc4	2.8 (21)	1.6 (12)	1 (7.7)	0.79 (5.8)	0.78 (6)	0.78 (5.8)
14400	Sinc5	3.8 (29)	2.1 (17)	1.4 (11)	1.1 (8.4)	1.1 (8.1)	1 (8.4)
19200	Sinc5	4.6 (36)	2.5 (20)	1.6 (13)	1.2 (9.6)	1.2 (9.3)	1.2 (9.5)
25600	Sinc5	6.7 (56)	3.6 (29)	2.1 (17)	1.5 (13)	1.4 (12)	1.4 (12)
40000	Sinc5	9.6 (80)	5 (43)	2.9 (23)	2 (16)	1.8 (15)	1.8 (15)

8 Detailed Description

8.1 Overview

The ADS125H01 and ADS125H02 are two-channel, wide-range, 24-bit, 40-kSPS, delta-sigma (ΔΣ) analog-to-digital converters (ADCs). The devices feature 12 programmable input ranges from ±20 mV to ±20 V that are configurable as one differential input or two single-ended inputs. The devices include a programmable gain amplifier (PGA), signal monitors for overload conditions, and a voltage reference. The ADCs provide a compact one-chip measurement solution for a wide range of input voltages, including ±10-V and 20-mA transmitters (with an external shunt resistor), and provide the high resolution necessary for low-level sensors such as strain-gauge sensors, thermocouples, and resistance temperature detectors (RTDs). The ADS125H02 adds four general-purpose, input/output (GPIO) pins to expand the measurement channels (via the external multiplexer), two current sources (IDAC) pins for sensor biasing, and an additional reference input pin pair. The ADS125H01 and ADS125H02 are pin compatible.

In summary, these devices feature:

- 12 programmable input ranges: from ±20-mV up to ±20-V (differential)
- High-input impedance, low-noise, CMOS-input PGA
- 2.5-V voltage reference
- Internal or external reference
- Internal clock oscillator
- Input signal, voltage reference, and power-supply monitors
- Temperature sensor
- Serial peripheral interface (SPI)-compatible serial interface with CRC error check
- Two IDACs (ADS125H02)
- Four GPIOs (ADS125H02)

Analog inputs (AIN0, AIN1, AINCOM) connect to the input multiplexer (MUX) for input channel selection. The ADC supports one differential or two single-ended input configurations. The input channel multiplexer is supplied by the high-voltage power supplies (HV_AVDD and HV_AVSS).

The programmable gain amplifier (PGA) follows the input multiplexer. The PGA is a high input impedance, complementary metal oxide semiconductor (CMOS) differential input and output, programmable gain, and programmable attenuation amplifier. In the PGA attenuation mode, the PGA translates the high input voltage to match the low input voltage range of the ADC. In the PGA gain mode, the low-level input voltage is amplified to the match the input range of the ADC. The PGA output connects to the CAPP and CAPN pins to form the ADC antialias filter, combining the PGA output resistors with an external capacitor.

The internal circuit nodes of the PGA are monitored for signal overload. Status bits in the status register activate when the PGA overload condition is detected.

The ΔΣ modulator measures the input voltage relative to the reference voltage to produce the 24-bit conversion result. The input range of the ADC is $\pm V_{REF}$ / Gain, where gain is programable from 0.125 V/V to 128 V/V.

The digital filter averages and performs data rate reduction on the modulator output data to yield the output conversion result. The sinc filter mode of the digital filter provides a programmable order (sinc1 through sinc5) providing optimization of conversion cycle time, conversion noise, and line-cycle rejection. The finite impulse response (FIR) filter mode provides single-cycle settled data and provides simultaneous rejecting 50-Hz and 60-Hz frequencies at a data rate of 20 SPS.

The ADC reference voltage is either internal (2.5 V) or is provided externally. REFOUT provides the buffered, 2.5-V internal reference output. The reference is monitored for out-of-range operation. The ADS125H02 provides two voltage reference input pin pairs.

The ADS125H02 includes two current sources (IDAC1, IDAC2), that are referenced to the AVDD analog power supply. The IDACs are constant-current sources providing excitation current to resistive sensors or for other sensors that require constant-current excitation. Additionally, the ADS125H02 provides four GPIO pins to control an external signal multiplexer and for general-purpose I/O of logic signals.

The ADC has an internal temperature sensor for internal device temperature monitoring. The high-voltage power supply is available for internal readback for system-level diagnostics.

Overview (接下页)

The SPI-compatible serial interface is used to read the conversion data and to configure the ADC. Communication integrity is validated by a CRC. The serial interface consists of the following signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, and DOUT/$\overline{DRDY}$ (see the *Chip-Select Pins (CS1 and CS2)* section for details). The dual-function DOUT/$\overline{DRDY}$ pin combines the serial data output and the data-ready functions into one pin. $\overline{DRDY}$ is the dedicated data-ready output.

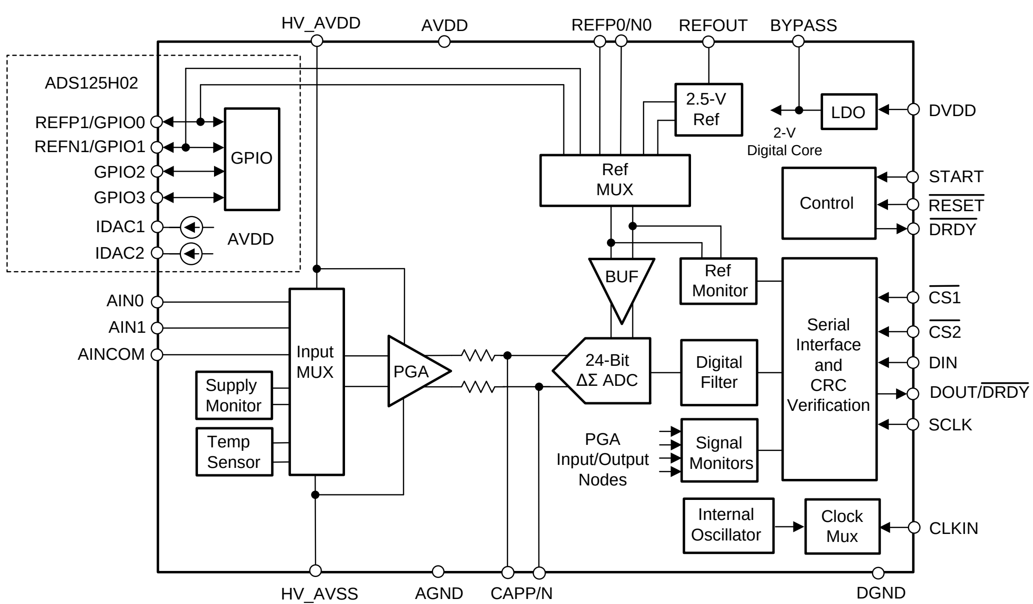
The ADC clock is either the internal oscillator or is external. The external clock is selected automatically. The clock frequency is 7.3728 MHz (10.24 MHz in 40-kSPS operation).

ADC conversions are controlled by the START pin or by the START command. The ADC is programmable for continuous mode or one-shot conversions.

The ADC is automatically reset at power-up, by the $\overline{RESET}$ input, or by the RESET command.

The input signal multiplexer and PGA are powered by the high-voltage power supplies (HVAVDD and HV_AVSS). The high-voltage power supplies are configurable to either bipolar or unipolar modes (up to ±18 V, or up to 36 V). The modulator, voltage reference, and excitation current sources are powered by the AVDD power supply (5 V). The digital I/O is powered by DVDD (3-V to 5-V range). An internal subregulator powers the ADC digital core. A external bypass capacitor is required to connect to the subregulator output (BYPASS).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs

As shown in 图 8, the analog inputs of the ADC consist of electrostatic discharge (ESD) protection diodes and an input multiplexer. The multiplexer supports three external input and three internal measurement configurations.

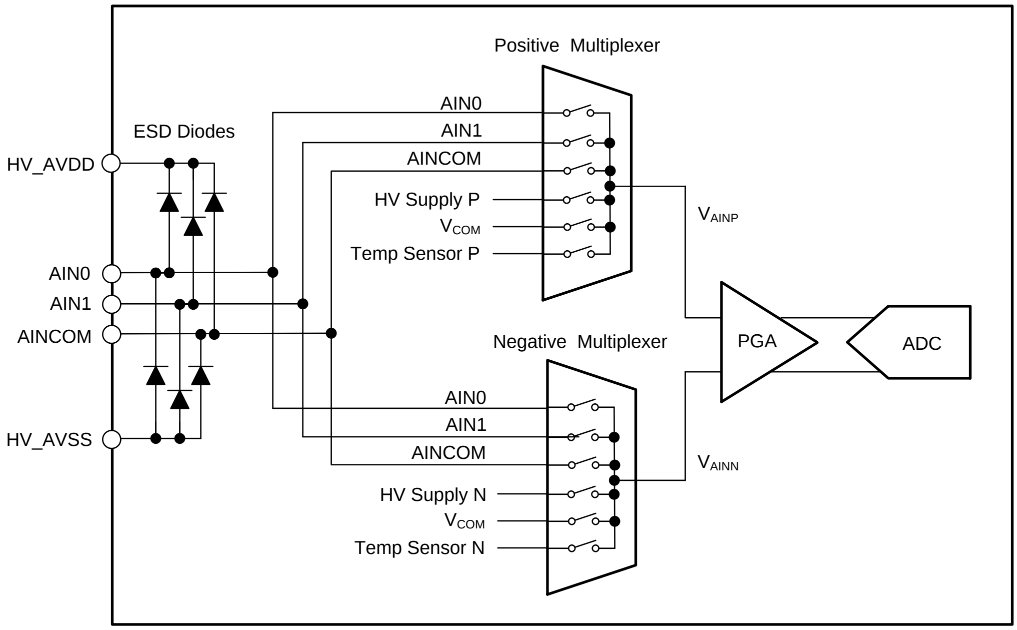


图 8. Analog Input Diagram

8.3.1.1 ESD Diodes

ESD diodes are incorporated to protect the ADC inputs from possible ESD events occurring during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. For system-level ESD protection, consider the use of external ESD protection devices for pins that are exposed to ESD, including the analog inputs.

If either input is driven below HV_AVSS – 0.3 V, or above HV_AVDD + 0.3 V, the internal protection diodes can conduct. If these conditions are possible, input current can flow into the inputs. Use external clamp diodes, series resistors, or both to limit the input current to the specified maximum value.

Feature Description (接下页)

8.3.1.2 Input Multiplexer

The input multiplexer selects the signal for measurement. The ADC supports two single-ended measurements (AIN0 – AINCOM, or AIN1 – AINCOM) and one differential input measurement (AIN1 – AIN0). The multiplexer is programmed by the MUX[2:0] bits of the MODE4 register (address = 10h). 表 3 lists the multiplexer settings to use to select the inputs.

表 3. Input Multiplexer Settings

MUX[2:0] BITS OF REGISTER MODE4 (10h)	MEASUREMENT (P – N)
000	AIN1 – AIN0
001	AIN0 – AIN1 (reserved for use with final silicon)
010	AIN1 – AINCOM
011	AIN0 – AINCOM
100	HV supply readback: (HV_AVDD – HV_AVSS) / 36
101	PGA inputs connected to V_{COM}: (HV_AVDD + HV_AVSS) / 2 (default)
110	Temperature sensor
111	Reserved

8.3.2 Temperature Sensor

The ADC has an internal temperature sensor that is comprised of two internal diodes with one diode having 80 times the current density of the other. The difference in current density of the diodes yields a differential output voltage that is proportional to absolute temperature. To measure the temperature sensor, write 110b to select the temperature sensor and then start a new ADC conversion. 公式 2 shows how to convert the temperature sensor reading to degrees Celsius (°C):

$$\text{Temperature (°C)} = [(\text{Temperature Reading (µV)} – 122{,}400) / 420\ \text{µV/°C}] + 25\text{°C} \quad (2)$$

When measuring the temperature sensor, set the gain equal to 1 and disable the chop and AC-excitation modes. As a result of the low package-to-PCB thermal resistance, the internal temperature closely tracks the PCB temperature. Be aware that device self-heating increases the internal temperature relative to the surrounding PCB.

8.3.3 High-Voltage Power-Supply Readback

Read the high-voltage power supply by selection through the input multiplexer. The supply voltage is internally divided by 36 for measurement. 公式 3 shows the supply voltage scaling.

$$\text{High-Voltage Power Supply (V)} = (\text{HV\_AVDD} – \text{HV\_AVSS}) / 36 \quad (3)$$

Measure the high-voltage power supply using the internal or external reference. To measure, disable the chop and AC-excitation modes. Write 100b to the multiplexer control bits to select the input multiplexer and then start a new conversion.

8.3.4 Internal V_{COM} Connection (Default)

For this multiplexer configuration, the external inputs are open and the PGA inputs connect to an internal V_{COM} voltage as defined by (HV_AVDD + HV_AVSS) / 2. Use this mode to measure the ADC noise performance and offset voltage, or to short the inputs for offset calibration. Be aware that shorting the inputs to the system yields the best calibration results. Short the V_{COM} input connection by writing 101b to the multiplexer control register. Using the desired ADC configuration, start a new conversion with the inputs shorted.

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8.3.5 Programmable Gain Amplifier (PGA)

The PGA is a low-noise, programmable gain and programmable attenuation, CMOS differential-input, differential-output amplifier. The PGA operates in gain or attenuation mode depending on the programming. Program the PGA for gain mode when the signal is less than the reference voltage. Program the PGA for attenuation mode when the signal is greater than the reference voltage.

图 9 shows the PGA block diagram. The PGA consists of two stages. The first stage is a high input impedance, CMOS differential input, differential output, noninverting input amplifier. The stage is powered by the high-voltage analog power supplies (HV_AVDD and HV_AVSS). The first stage provides gains of 1 V/V to 128 V/V.

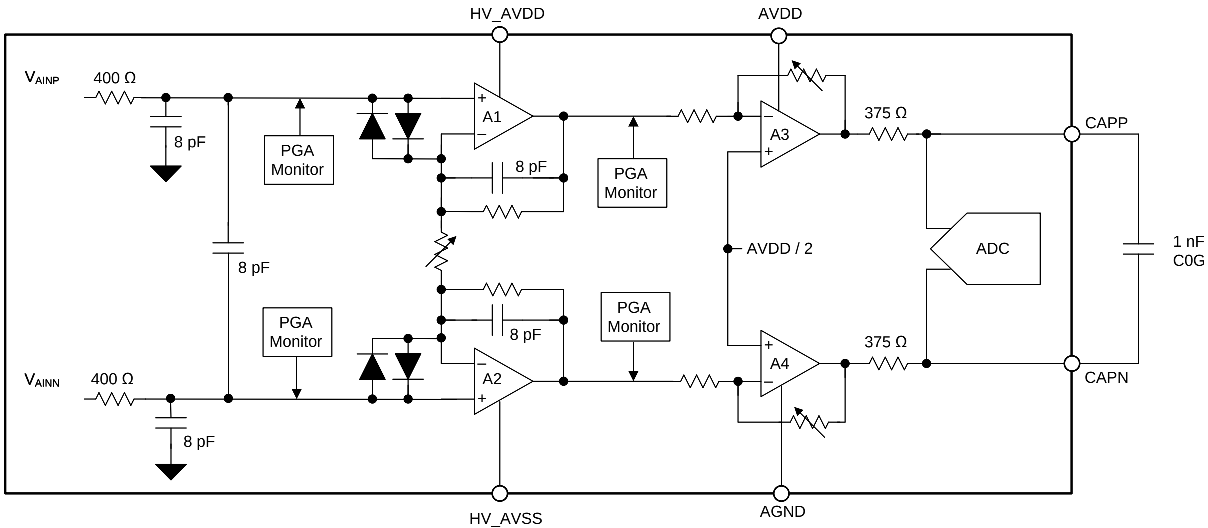

图 9. PGA Block Diagram

The second stage is a differential input, differential output, inverting amplifier powered by the low-voltage analog supply (AVDD). The second stage provides attenuations from 0.5 V/V to 0.125 V/V. The common-mode voltage of the second stage is regulated to AVDD / 2. The second stage output drives the ADC inputs. The output connects to the CAPP and CAPN pins. Connect an external 1-nF capacitor to these pins to form the ADC antialias filter. The filter also provides a bypass for the modulator sampling pulses. The CAPP and CAPN nodes are sensitive to interference from noise. As a result, place the capacitor close to the pins using short, direct traces. Avoid running clock traces or other digital traces in the vicinity of these pins.

Amplifiers A1 and A2 are protected by inverse-parallel diodes connected across the amplifier inputs. The diodes are in addition to the input ESD-protection diodes. When the signal to the PGA is out-of-range, causing the amplifiers to saturate, the diodes may conduct resulting in current flow through the inputs. Additionally, high dV/dt signal conditions (such as those caused by the switching of a signal multiplexer), may cause a transient turn-on of the protection diodes. Use an RC filter on the PGA inputs to limit the dV/dt of the signal to eliminate transient diode turn-on.

The PGA incorporates filters to improve rejection by radio frequency interference (RFI) and electromagnetic interference (EMI) noise interference. Key nodes of the PGA input and output circuit are monitored for possible out-of-range conditions. If an out-of-range condition is detected, the monitors set the appropriate alarm bits in the status register.

8.3.5.1 PGA Input Range

The reference voltage and the PGA gain setting determine the full-scale input range of the ADC. 表 4 lists the full-scale input range verses gain when operating with a 2.5-V reference. The full-scale input range scales with changes to the reference voltage. 表 4 lists example signal ranges for differential and single-ended input configurations. The example input range includes an overrange margin. The 24-bit ADC allows single-ended configurations with little loss of signal resolution.

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表 4. Input Voltage Range

GAIN[2:0] BITS	GAIN (V/V)	DIFFERENTIAL INPUT RANGE(1)	EXAMPLE DIFFERENTIAL INPUT	EXAMPLE SINGLE-ENDED INPUT (2)
0000	0.125	±20 V(3)	±18 V	0 V to ±15.5 V
0001	0.1875	±13.3 V	±12.5 V	0 V to ±10 V
0010	0.25	±10 V	±8 V	0 V to ±8 V
0011	0.5	±5 V	±4 V	0 V to ±4 V
0100	1	±2.5 V	±2 V	0 V to ±2V
0101	2	±1.25 V	±1 V	0 V to ±1 V
0110	4	±0.625 V	±0.5 V	0 V to ±0.5 V
0111	8	±0.312 V	±0.25 V	0 V to ±0.25 V
1000	16	±0.156 V	±0.125 V	0 V to ±0.125 V
1001	32	±0.0781 V	±0.062 V	0 V to ±0.062 V
1010	64	±0.0391 V	±0.031 V	0 V to ±0.031 V
1011	128	±0.0195 V	±0.015 V	0 V to ±0.015 V

(1) Reference voltage = 2.5 V and HV_AVDD, HV_AVSS = ±18 V.
(2) Bipolar supply operation.
(3) At a gain of 0.125, the maximum differential input range is limited at ±20 V, irrespective of reference voltage.

As with many amplifiers, the PGA has limits for the maximum input voltage that must not be exceeded. The *absolute input voltage* is defined as the signal and common-mode voltages combined. The maximum input voltage depends on the PGA gain, the maximum expected differential voltage (V_{IN}), and the minimum expected high-voltage power supply. Maintain the absolute input voltage within range, as given by 公式 4, for linear operation of the PGA:

$$HV\_AVSS + 2.5 + V_{IN} \times (Gain - 1) / 2 < V_{(AINx)} < HV\_AVDD - 2.5 - V_{IN} \times (Gain - 1) / 2$$

where:

- For gain < 1, use gain = 1 in the equation
- $V_{(AINx)}$ = Absolute input voltage
- V_{IN} = Maximum differential input voltage = $V_{AINP} - V_{AINN}$ (4)

The full available differential input voltage is also limited under certain operating conditions. The first condition is operation with reference voltage > AVDD – 1 V (all gains and attenuations). In this case, the differential input voltage is limited to $V_{IN} < \pm (AVDD - 1\ V) / gain$. Additionally, the maximum differential input voltage is limited to ±20 V, irrespective of gain (attenuation) factor or reference voltage.

图 10 and 图 11 illustrate the relationship between the PGA input to PGA output. In attenuation mode, the first PGA stage is configured as a unity-gain follower. The second PGA stage attenuates the differential input and establishes the common-mode output voltage of the signal to AVDD / 2.

In gain mode, the first PGA stage amplifies the differential signal. 图 10 and 图 11 illustrate the output voltage of each PGA stage that must be maintained within the voltage headroom.

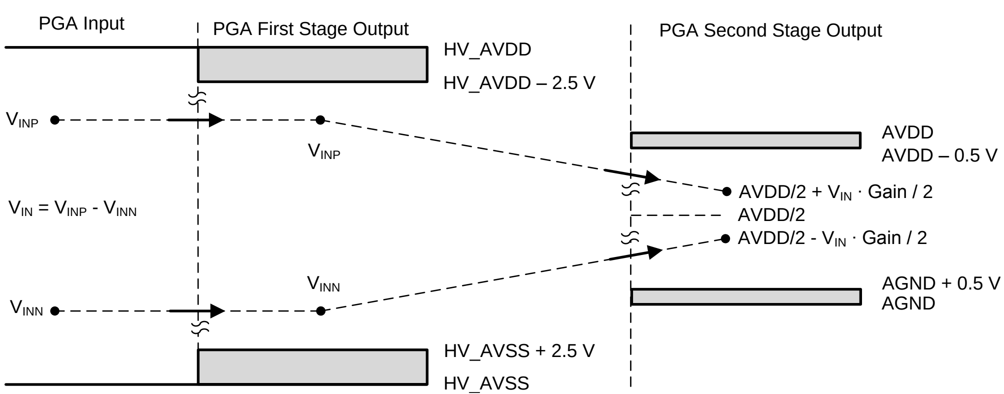


图 10. PGA: Attenuation Mode

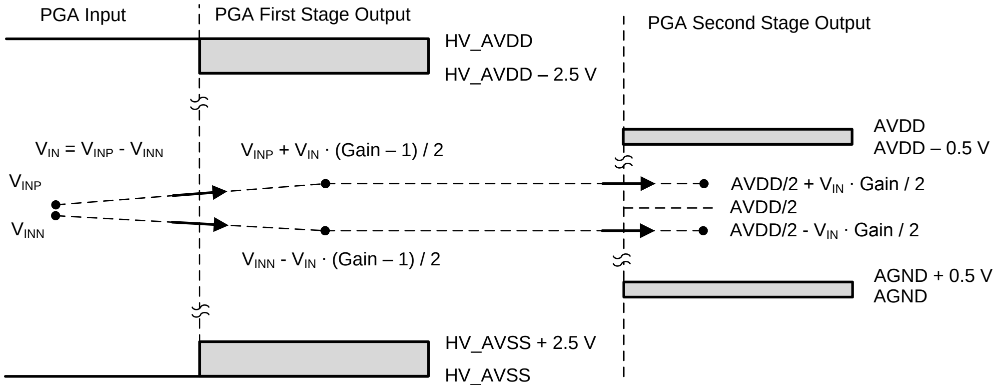


图 11. PGA: Gain Mode

8.3.5.2 PGA Monitor

The PGA has a linear operating range that must not be exceeded, otherwise the conversion data are not valid. The ADC includes PGA monitors that flag when the amplifier is in a overload condition. As shown in 图 12, the input and output nodes of the PGA first stage are monitored by high and low voltage detectors. As 图 13 shows, the low threshold is HV_AVDD – 2 V and the high threshold is HV_AVSS + 2 V. There are four nodes that are monitored, each with high or low alarm states for a total of eight monitor flags that are reported in the status byte.

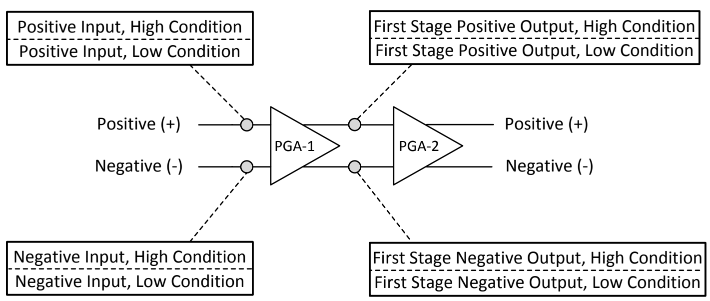


图 12. PGA Monitors

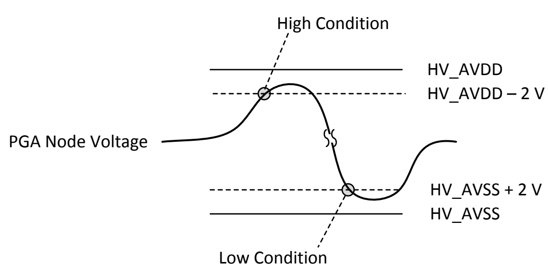


图 13. PGA Monitor Thresholds

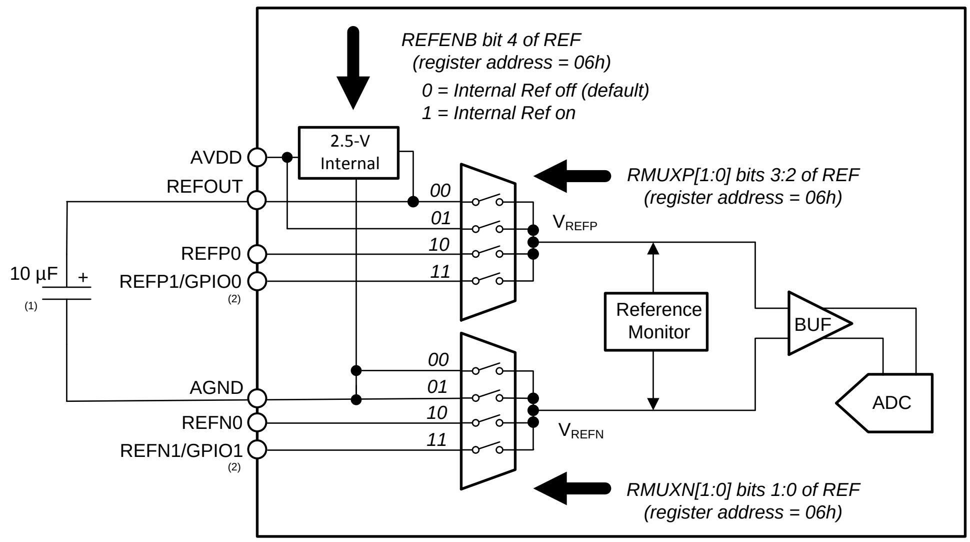
Monitor for possible PGA overload conditions by polling the STAT12 bit (bit 4) of the STATUS0 byte. This flag indicates if one or more PGA alarm flags are set or if a CRC-2 error occurred. Poll the STATUS1 and STATUS2 registers (11h and 12h) to determine the source of the error. If the PGA is in an overload condition, the flag bits of the STATUS1 register are set. The PGA status flags are latched in the STATUS1 register. The flags are reset by the read operation (clear-on-read operation). The PGA overload flags and the CRC1ERR and CRC2ERR flags must be cleared to clear the global error flag, STAT12. See the STATUS1 register for a description of the PGA alarm bits.

The PGA monitors are fast-responding analog comparators. Therefore, the monitors are capable of detecting short-transient overload conditions. Short-duration PGA overload events may not result in clipped conversion values because of the data integration operations (averaging) of the digital filter.

Certain input overload conditions can trigger input alarms without necessarily triggering the corresponding output alarms.

8.3.6 Reference Voltage

The ADC reference voltage is either a 2.5-V internal voltage, one of two external reference pin pairs, or the AVDD power supply (5 V). The reference voltage is defined as $V_{REF} = V_{REFP} – V_{REFN}$, where V_{REFP} and V_{REFN} are the positive and negative reference voltages, respectively. The polarity of V_{REF} must always be positive. 图 14 shows the block diagram of the reference multiplexer.



(1) The internal reference requires a 10-µF capacitor be connected to the REFOUT and AGND pins.

(2) The ADS125H02 only provides the second reference input pin pairs.

图 14. Reference Multiplexer Diagram

Program the RMUXP[1:0] and RMUXN[1:0] bits of the REF register to select the positive and negative reference voltages, respectively. The positive reference options are internal reference positive, external REFP0, external REFP1, or AVDD. The negative selections are internal reference negative, external REFN0, external REFN1, or AGND.

The reference voltage is monitored for low voltage conditions; see the *Reference Monitor* section.

8.3.6.1 Internal Reference

The ADC includes a precision 2.5-V reference. Program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to 00 to select the internal reference. The REF_ENB bit of the REF register controls the reference bias (default = off). Enable the reference if using the current sources. A 10-µF capacitor is required between the REFOUT and AGND pins in order to filter the reference noise. The capacitor is not required if not using the internal reference.

Be aware of AVDD inrush current when the reference is enabled as a result of charging the 10-µF REFOUT capacitor. Also, when the reference is enabled, be aware of the time for reference stabilization before beginning conversions or before calibrating the ADC. REFOUT is the reference output and AGND is the reference return. Use a star layout connection for the reference return and make this connection close to the AGND pin.

8.3.6.2 External Reference

Use an external reference by applying the reference voltage to one of the reference input pin pairs. The reference inputs are differential with positive and negative inputs. Program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to 10 or 11 to select the inputs (REFP0, REFN0) and (REFP1, REFN1), respectively. The REFP1, REFN1 pins are available with the ADS125H02 only. Follow the specified absolute and differential reference voltage operating conditions; see the *Recommended Operating Conditions* table. Use a

10-nF bypass capacitor across the reference input pins to filter noise. The reference inputs include input current that can lead to voltage errors if large reference impedances are present. When the impedances are present, consider the impact of the error to the reference voltage.

8.3.6.3 AVDD Power-Supply Reference

Use the AVDD power supply as a reference by setting the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to 01 (default mode of operation). For 6-wire load cell applications with excitation sense connections, or AC-excitation mode, connect the sense voltage to the reference inputs and program the ADC for external reference operation.

8.3.6.4 Reference Monitor

The ADC incorporates a reference monitor to detect a low or missing reference voltage. As shown in 图 15 and 图 16, if the reference voltage (V_{REF} = V_{REFP} – V_{REFN}) is below 0.4 V, the REFALM bit is set in the STATUS0 byte. The alarm is read-only and resets at the next conversion after the condition is removed. Use the reference monitor to detect a missing or failed reference voltage.

To implement the reference alarm, use a 100-kΩ resistor across the reference inputs. The resistor biases the P and N reference inputs to 0 V if either input is not connected. Poll bit 3 (REFALM) of the STATUS0 byte to determine if the reference alarm is set.

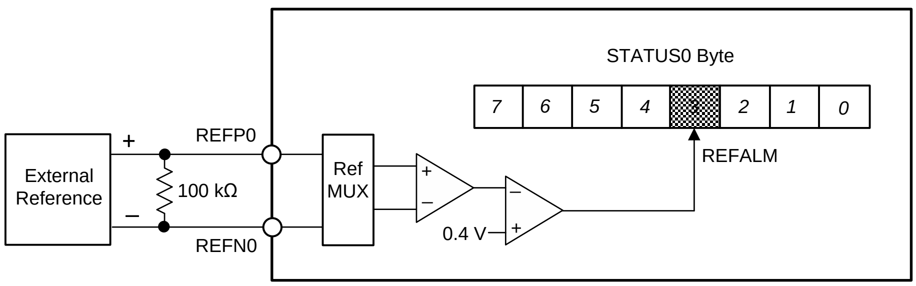


图 15. Reference Monitor

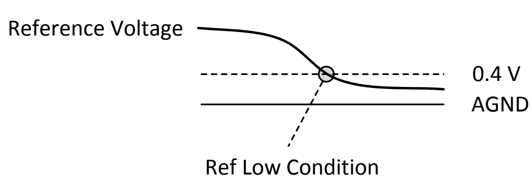


图 16. Reference Monitor Threshold

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8.3.7 Current Sources (IDAC1 and IDAC2)

The ADS125H02 incorporates two current sources designed to provide excitation current to the RTD, thermistor, diode, and other sensor types that require constant-current biasing. The current source outputs are on the IDAC1 and IDAC2 pins. The voltage compliance range is governed by the AVDD analog supply (5 V). The currents are individually programmed over the 50-µA to 3000-µA range. As shown in 图 17, the I_MUX register controls the pin connections.

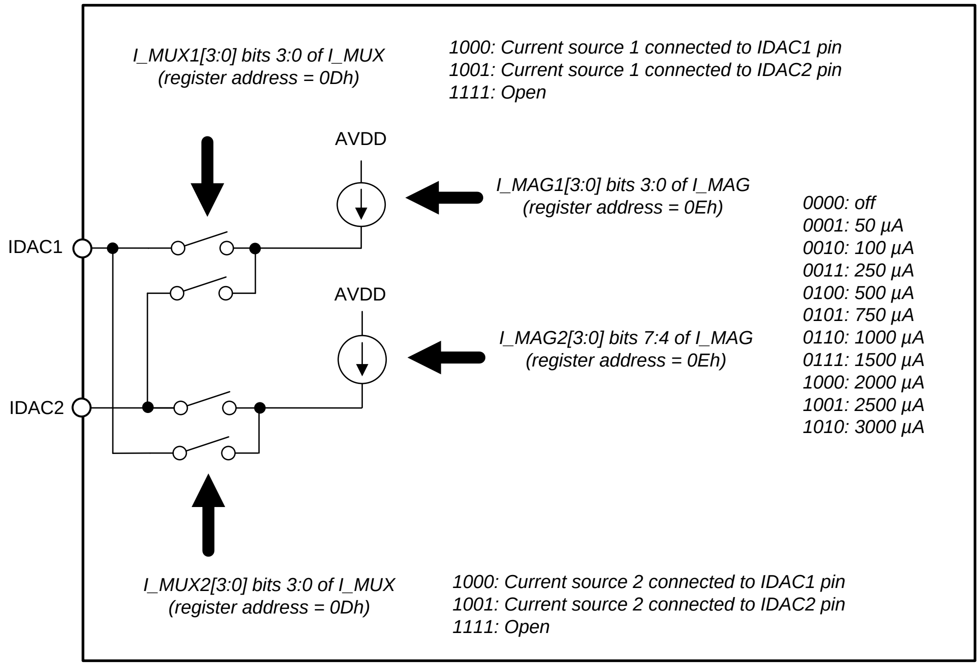

图 17. Current Source Output Diagram

Enable the internal voltage reference to operate the current sources. Double the current value or produce an intermediate current value by connecting the current source output pins together. Maintain the compliance voltage of the current sources as specified in the *Electrical Characteristics* table.

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8.3.8 General-Purpose Inputs and Outputs (GPIOs)

The ADS125H02 provides four GPIO pins (GPIO3 through GPIO0), two of which are multiplexed with the external reference REFP1 and REFN1 input pins. The GPIO are digital inputs and outputs with values that are read and written by the GPIO_DAT bits of the MODE3 register. The GPIO input and output levels are referred to the 5-V analog supply (AVDD and AGND). As 图 18 shows, the input threshold values between values logic 0 and logic 1 are AVDD / 2 (typical). The GPIO_CON[3:0] bits set the GPIO connection to the designated pin (1 = connected). The GPIO_DIR bits program the direction of the GPIO as an input (1) or output (0). The GPIO_DAT[3:0] bits are the data values for the GPIO. If a GPIO pin is programmed as an output, the value read is the register data that is written.

The GPIO provides the output drive signals of the AC-excitation mode; see the *AC-Excitation Mode* section.

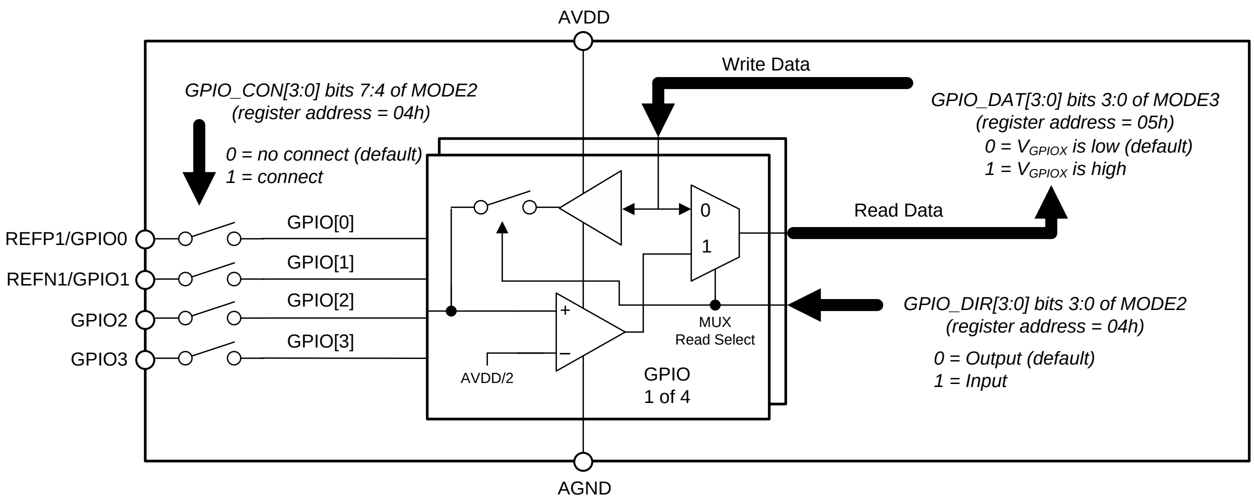

图 18. GPIO Block Diagram

8.3.9 ADC Modulator

The modulator is an inherently stable, fourth-order, 2 + 2 pipelined ΔΣ modulator. The modulator samples the analog input voltage at a high sample rate (f_{MOD} = f_{CLK} / 8) and converts the analog input to a ones density bit stream for processing by the digital filter.

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8.3.10 Digital Filter

The digital filter processes the modulator output data to produce the high-resolution conversion result. The digital filter low-pass filters and decimates the data (data rate reduction), which yields the final data output. By adjusting the type of filtering, tradeoffs are made between resolution, data rate, and line cycle rejection.

The digital filter has two operating modes, as shown in 图 19: sin (x) / x (sinc) mode and finite impulse response (FIR) mode. The sinc mode provides data rates of 2.5 SPS through 40 kSPS with a selectable filter order of sinc1 through sinc5. The FIR filter provides single-cycle settled conversions and simultaneous rejection of 50-Hz and 60-Hz signal interference frequencies with data rates of 2.5 SPS through 20 SPS.

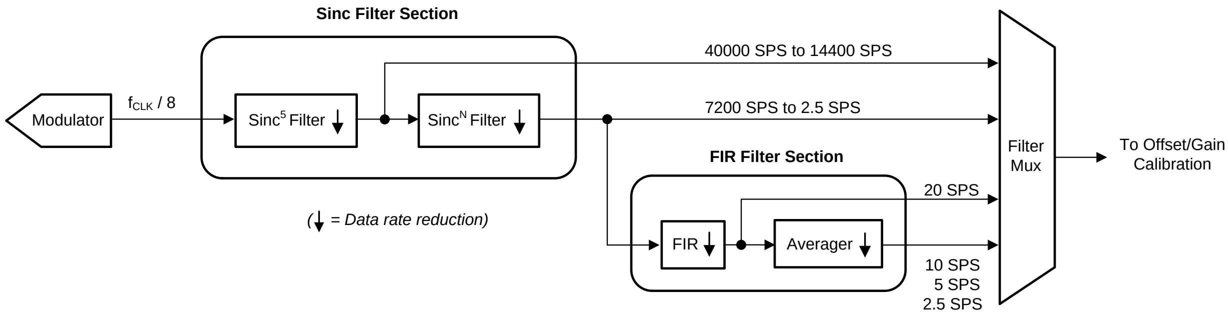

图 19. Digital Filter Block Diagram

8.3.10.1 Sinc Filter Mode

The sinc filter consists of two stages: a variable-decimation sinc5 filter followed by a variable-decimation, variable-order sinc filter. The first stage sinc5 filter averages and down-samples the modulator data (f_{CLK} / 8) to produce 40 kSPS, 25600 SPS, 19200 SPS, and 14400 SPS by using decimation ratios of 32, 36, 48, and 64, respectively. These data outputs bypass the second filter stage and as a result have response characteristics of the first-stage sinc5 filter. The second stage receives the first stage output data at 14400 SPS and filters or decimates the data to yield data rates of 7200 SPS to 2.5 SPS. The second stage is a programmable order sinc filter.

The data rate is programmed by the DR[4:0] bits of the register MODE0. The filter mode is programmed by the FILTER[2:0] bits of the MODE0 register.

8.3.10.1.1 Sinc Filter Frequency Response

The digital filter reduces noise present in the signal and noise from within the ADC. Adjusting the filter by changing the data rate and filter order changes the filter bandwidth. Through these changes, tradeoffs are made among the filter attributes (noise, bandwidth, and conversion latency).

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As shown in 图 20 and 图 21, the first-stage sinc5 filter has frequency response nulls occurring at N × f_{DATA} (where N = 1, 2, 3, and so on). At the null frequencies, the filter has zero gain.

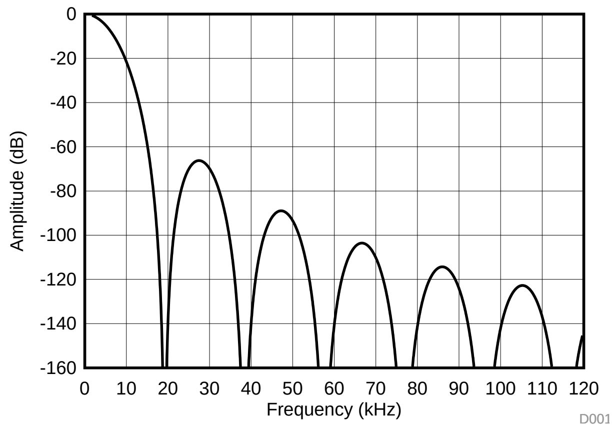

图 20. Sinc Frequency Response (19200 SPS)

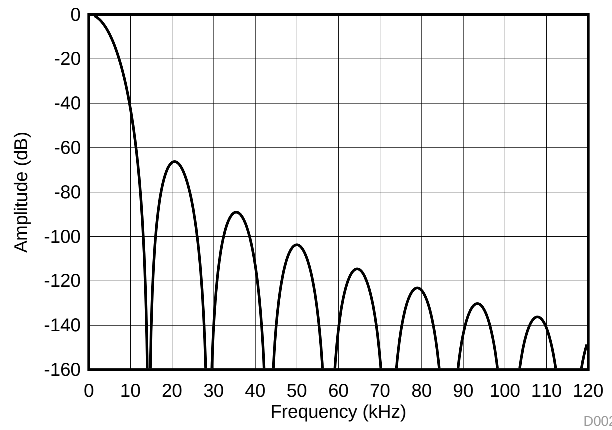

图 21. Sinc Frequency Response (14400 SPS)

The second stage superimposes additional nulls to the frequency response with the nulls that are produced by the first stage. The first of the superimposed nulls occurs at the output data rate, and by nulls occurring at multiples of the data rate.

图 22 shows the frequency response of the combined filter stages at 2400 SPS. This data rate has five equally-spaced nulls residing between the larger nulls at 14400-Hz multiples that are produced by the first stage. This frequency response is similar to that of data rates 2.5 SPS to 7200 SPS. 图 23 shows the frequency response nulls at 10 SPS.

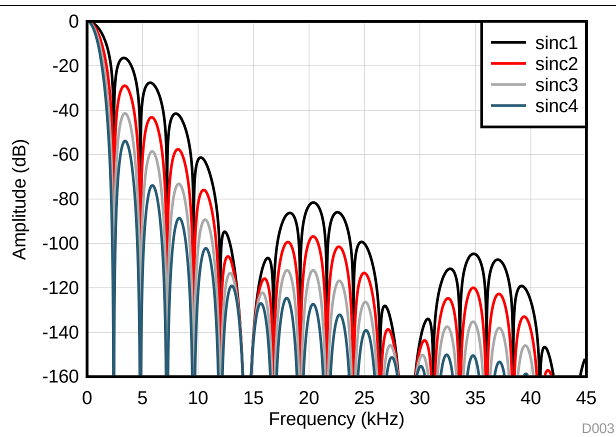

图 22. Sinc Frequency Response (2400 SPS)

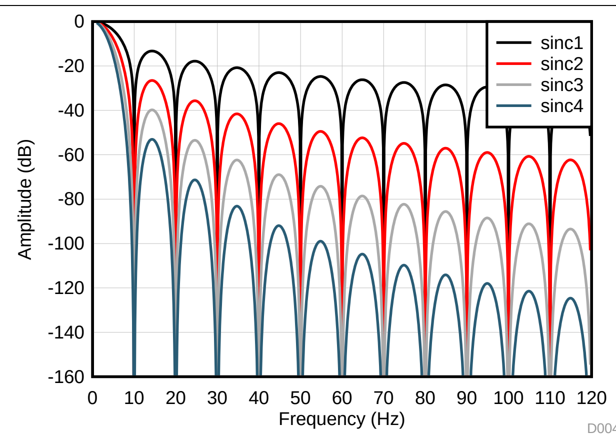

图 23. Sinc Frequency Response (10 SPS)

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图 24 and 图 25 show the frequency response of data rates 50 SPS and 60 SPS, respectively. The frequency response is plotted to the 50-Hz 12th harmonic (10th harmonic for 60 Hz). The 50-Hz or 60-Hz fundamental and harmonic noise of the signal are reduced by increasing the filter order of the second stage.

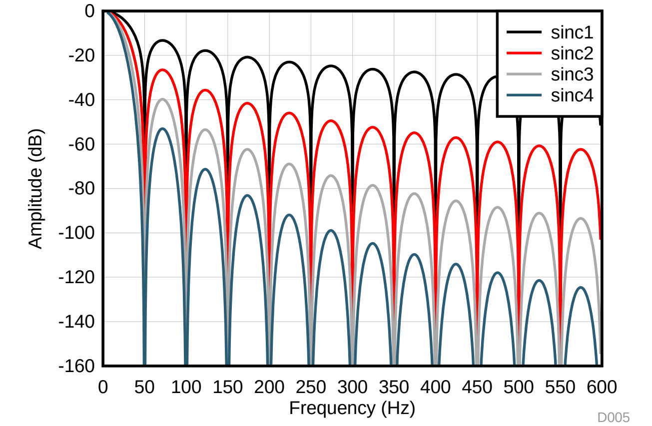

图 24. Sinc Frequency Response (50 SPS)

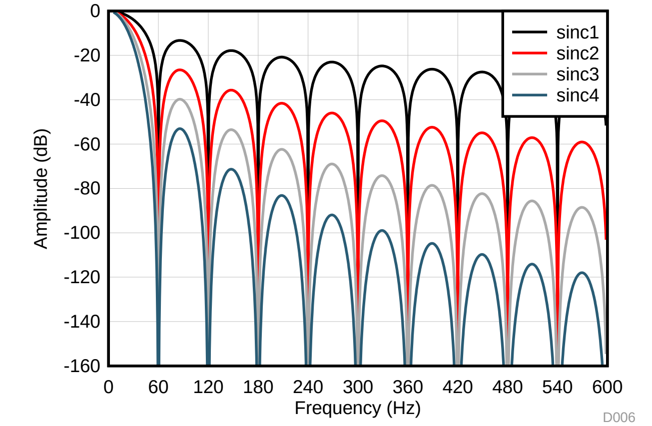

图 25. Sinc Frequency Response (60 SPS)

图 26 and 图 27 plot the detailed frequency response of the 50-SPS and 60-SPS data rates and show various orders of the sinc filter. The high-order sinc filter increases the frequency width of the null, which improves line cycle rejection. As shown in 图 26 and 图 27, the best 50-Hz or 60-Hz rejection occurs using the sinc4 order.

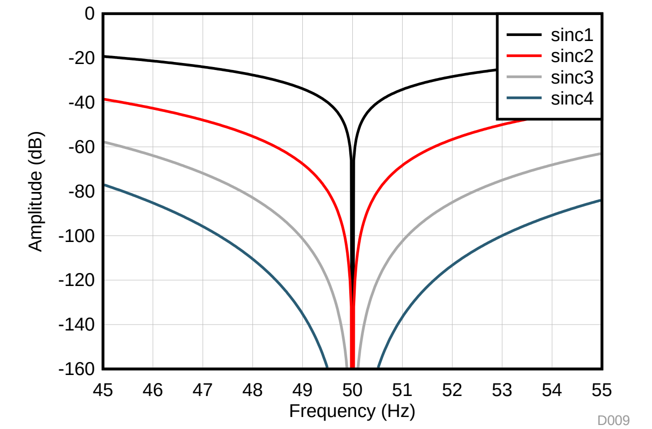

图 26. Sinc Frequency Response, Detailed (50 SPS)

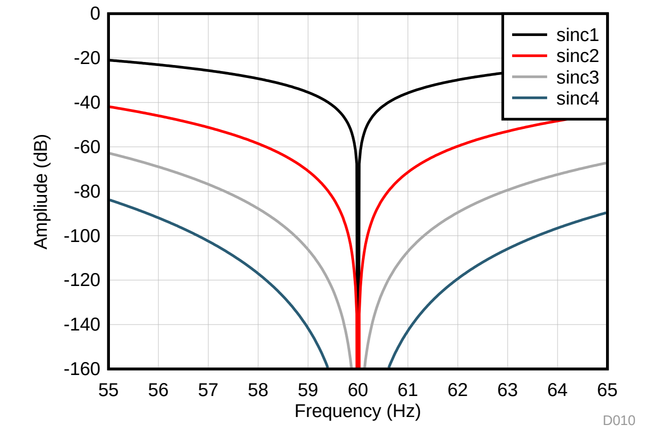

图 27. Sinc Frequency Response, Detailed (60 SPS)

The sinc filter has an overall low-pass response that rolls off high-frequency components of the signal. The filter bandwidth depends on the output data rate and the order of the output data rate. The overall system bandwidth is the combined responses of the digital filter, the PGA antialias filter, and external filters. 表 5 lists the –3-dB bandwidth of the sinc filter. Be aware of the reduced signal bandwidth pertaining to the high-order sinc filters.

表 5. Sinc Filter Bandwidth

	-3-dB BANDWIDTH (Hz)				
DATA RATE (SPS)	SINC1	SINC2	SINC3	SINC4	SINC5
2.5	1.10	0.80	0.65	0.58	—
5	2.23	1.60	1.33	1.15	—
10	4.43	3.20	2.62	2.28	—
16.6	7.38	5.33	4.37	3.80	—
20	8.85	6.38	5.25	4.63	—
50	22.1	16.0	13.1	11.4	—
60	26.6	19.1	15.7	13.7	—
100	44.3	31.9	26.2	22.8	—
400	177	128	105	91.0	—
1200	525	381	314	273	—
2400	1015	751	623	544	—
4800	1798	1421	1214	1077	—
7200	2310	1972	1750	1590	—
14400	—	—	—	—	2940
19200	—	—	—	—	3920
25600	—	—	—	—	5227
40000	—	—	—	—	8167

8.3.10.2 FIR Filter

The finite impulse response (FIR) filter is a coefficient-based filter that provides an overall low-pass filter function. The filter provides simultaneous rejection of 50-Hz and 60-Hz line cycle frequencies and harmonics at data rates of 2.5 SPS, 5 SPS, 10 SPS, and 20 SPS. The conversion latency of the FIR filter is a single cycle. (See 表 8 for latency of all filter settings). As illustrated in 图 19, the FIR filter section receives data from the second-stage sinc filter at 600 Hz. The FIR filter section decimates by 30 to yield the output data rate of 20 SPS. A first-order variable average (sinc1) yields 10 SPS, 5 SPS, and 2.5 SPS.

As shown in 图 28 and 图 29, the FIR filter frequency response has a series of response nulls that are placed close to 50 Hz and 60 Hz. The response nulls repeat near the harmonics of 50 Hz and 60 Hz.

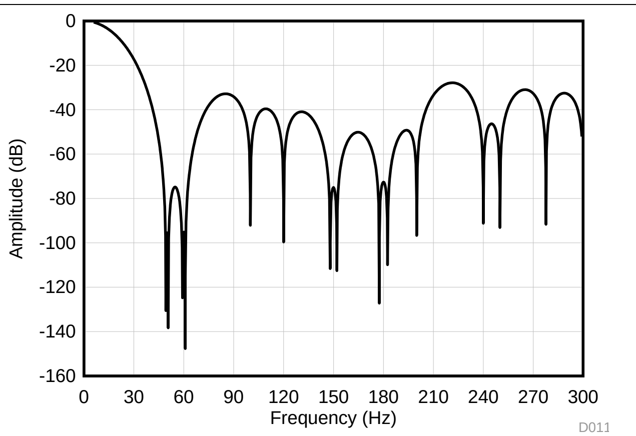

图 28. FIR Frequency Response (20 SPS)

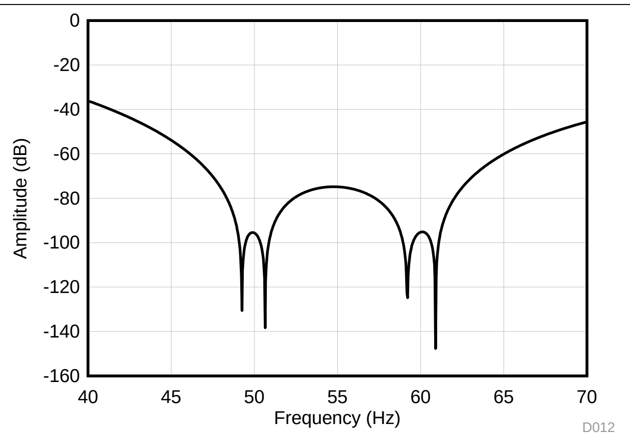

图 29. FIR Frequency Response Detail (20 SPS)

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图 30 shows the FIR filter response at 10 SPS. New frequency nulls are superimposed to the nulls in 图 28 as a result of the variable average. The first of the combined response nulls occurs at 10 Hz. Additional nulls occur at folded frequencies around multiples of 20 Hz. The first of the 10 SPS folded null frequencies is shown in 图 30 at 10 Hz, 30 Hz, 70 Hz, 90 Hz, and so on.

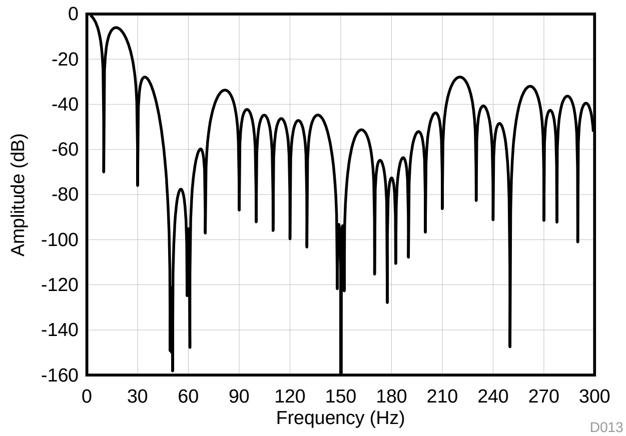

图 30. FIR Frequency Response (10 SPS)

Similar to the response of the sinc filter, the overall FIR filter frequency has a low-pass response that rolls off high frequencies. The response is such that the FIR filter limits the bandwidth of the input signal. The signal bandwidth depends on the output data rate. 表 6 lists the –3-dB filter bandwidth of the FIR filter. The total system bandwidth is the combined response of the digital filter, the PGA antialias filter, and external filters.

表 6. FIR Filter Bandwidth

DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)
2.5	1.2
5	2.4
10	4.7
20	13

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8.3.10.3 50-Hz and 60-Hz Normal Mode Rejection

To reduce 50-Hz and 60-Hz noise interference, configure the conversion period to reject the noise at 50 Hz and 60 Hz. 50-Hz and 60-Hz noise rejection depends on the filter type and filter order. 表 7 summarizes the 50-Hz and 60-Hz noise rejection versus data rate and filter type. The table values are based on 2% and 6% tolerance of noise frequency to ADC clock frequency. For the sinc filter mode, 50-Hz and 60-Hz noise rejection is increased by increasing the order of the filter. Common-mode noise is also rejected at these frequencies.

表 7. 50-Hz and 60-Hz Normal Mode Rejection

DIGITAL FILTER AMPLITUDE (dB)					
DATA RATE (SPS)	FILTER TYPE	50 Hz (±2%)	60 Hz (±2%)	50 Hz (±6%)	60 Hz (±6%)
2.5	FIR	–113	–99	–88	–80
2.5	Sinc1	–36	–37	–40	–37
2.5	Sinc2	–72	–74	–80	–74
2.5	Sinc3	–108	–111	–120	–111
2.5	Sinc4	–144	–148	–160	–148
5	FIR	–111	–95	–77	–76
5	Sinc1	–34	–34	–30	–30
5	Sinc2	–68	–68	–60	–60
5	Sinc3	–102	–102	–90	–90
5	Sinc4	–136	–136	–120	–120
10	FIR	–111	–94	–73	–68
10	Sinc1	–34	–34	–25	–25
10	Sinc2	–68	–68	–50	–50
10	Sinc3	–102	–102	–75	–75
10	Sinc4	–136	–136	–100	–100
16.6	Sinc1	–34	–21	–24	–21
16.6	Sinc2	–68	–42	–48	–42
16.6	Sinc3	–102	–63	–72	–63
16.6	Sinc4	–136	–84	–96	–84
20	FIR	–95	–94	–66	–66
20	Sinc1	–18	–34	–18	–24
20	Sinc2	–36	–68	–36	–48
20	Sinc3	–54	–102	–54	–72
20	Sinc4	–72	–136	–72	–96
50	Sinc1	–34	–15	–24	–15
50	Sinc2	–68	–30	–48	–30
50	Sinc3	–102	–45	–72	–45
50	Sinc4	–136	–60	–96	–60
60	Sinc1	–13	–34	–12	–24
60	Sinc2	–27	–68	–24	–48
60	Sinc3	–40	–102	–36	–72
60	Sinc4	–53	–136	–48	–96

8.4 Device Functional Modes

8.4.1 Conversion Control

The START pin or the START command controls the conversions. If using commands to control conversions, keep the START pin low to avoid contention between the pin and commands. Commands take affect on the 32nd falling SCLK edge. See the *Switching Characteristics* table for details on conversion control timing.

The ADC has two conversion control operating modes: continuous-conversion mode and pulse-conversion mode. The continuous-conversion mode performs conversions indefinitely until the user stops the conversions. Pulse-conversion mode performs one conversion and then stops. The CONVRT (bit 4 of the MODE1 register) programs the mode.

8.4.1.1 Continuous-Conversion Mode

This conversion mode performs continuous conversions until the user stops conversions. To start conversions, take the START pin high or send the START command. $\overline{\text{DRDY}}$ is driven high when the conversion is started. $\overline{\text{DRDY}}$ is driven low when the conversion data are ready. Conversion data are available to read at that time. Take the START pin low or send a STOP command to stop conversions. When conversions are stopped, the conversion in progress runs to completion. To restart a conversion that is in progress, toggle the START pin low-then-high or send a new START command.

8.4.1.2 Pulse-Conversion Mode

In pulse-conversion mode, the ADC performs one conversion when START is taken high or when the START command is sent. When the conversion completes, further conversions stop. The $\overline{\text{DRDY}}$ output is driven high to indicate the conversion is in progress and is driven low when the conversion data are ready. Conversion data are read at that time. To restart a conversion in progress, toggle the START pin low-then-high or send a new START command. Driving START low or sending the stop command does not interrupt the current conversion.

8.4.1.3 Conversion Latency

The digital filter averages data from the modulator to produce the conversion result. The individual stages of the digital filter must have settled data to provide fully settled output data. The order and the decimation ratio of the digital filter determine the amount of data averaged that affects the latency of the conversion data. The FIR and sinc1 filter modes are zero latency because the ADC provides the conversion result in one conversion cycle. Latency time is an important consideration for data throughput in multiplexed applications.

表 8 lists the conversion latency values of the ADC. Conversion latency is defined as the time from the start of the first conversion by taking the START pin high or sending the start command to when the conversion data are ready. The ADC is designed to provide fully settled data under this condition. The conversion latency values listed in 表 8 include the programmable start-conversion delay = 50 µs before the digital filter starts but does include overhead time for final data processing. After the first conversion completes in continuous conversion mode, the period of the next conversions are equal to 1 / f_{DATA}. The first conversion latency in chop and AC-excitation modes are twice the values listed in 表 8. The period of the next conversions are equal to the values listed in 表 8.

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Device Functional Modes (接下页)

表 8. Conversion Latency

DATA RATE (SPS)	CONVERSION LATENCY ($t_{(STDR)}$)[1] (ms)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	400.4	800.4	1,200	1,600	—	402.2
5	200.4	400.4	600.4	800.4	—	202.2
10	100.4	200.4	300.4	400.4	—	102.2
16.6	60.35	120.4	180.4	240.4	—	—
20	50.35	100.4	150.4	200.4	—	52.22
50	20.35	40.42	60.42	80.42	—	—
60	17.02	33.76	50.42	67.09	—	—
100	10.35	20.42	30.42	40.42	—	—
400	2.855	5.424	7.924	10.42	—	—
1200	1.188	2.091	2.924	3.758	—	—
2400	0.771	1.258	1.674	2.091	—	—
4800	0.563	0.8409	1.049	1.258	—	—
7200	0.494	0.702	0.841	0.980	—	—
14400	—	—	—	—	0.424	—
19200	—	—	—	—	0.337	—
25600	—	—	—	—	0.271	—
40000	—	—	—	—	0.179	—

(1) Chop mode off, conversion-start time delay = 50 µs (DELAY[3:0] = 0001).

As shown in 图 31, if the input signal changes during the conversion phase, the conversion data are a mix of old and new data. After an input change, the number of conversion periods required to provide fully settled output data are calculated by dividing the conversion latency by the nominal period plus one conversion period. In the chop mode and AC-excitation modes, use twice the latency values.

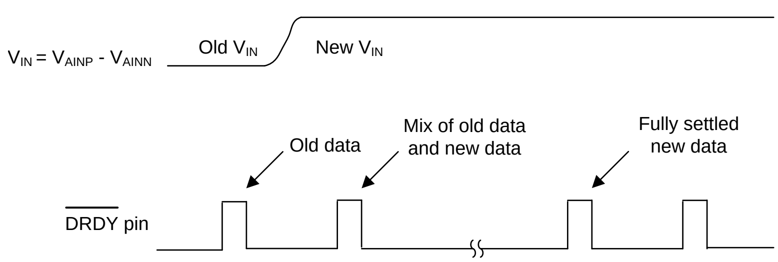

图 31. Input Change During Conversions

8.4.1.4 Start-Conversion Delay

At the start of a conversion, the ADC provides a programmable delay to allow for PGA settling or to provide delay for input and configuration changes. The default value is 50 µs and provides the settling time for the PGA antialiasing filter. Use additional delay time as needed to provide settling time for external components. The latency values listed in 表 8 are with a start-conversion delay value = 0 µs. As an alternative to this parameter, delay the start of conversion after the input and configuration changes.

Start-conversion delay is an important consideration when operating in AC-excitation mode. In this mode, the signal and reference inputs are reversed for each conversion and, as a result, this parameter allows for settling of the PGA antialias filter and external filter components. As a general guideline, set the delay time to approximately 15 times the time constant of the signal and reference filters.

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8.4.2 Chop Mode

The PGA and modulator are chopper-stabilized at high frequency to reduce offset voltage, offset voltage drift, and 1/f noise. These artifacts are modulated to high frequency and removed by the digital filter. Although chop reduces offset to very low levels, an optional, lower speed chop mode virtually removes all traces of offset errors.

In this mode, the ADC alternates the polarity of consecutive conversions by reversing the input signal. The ADC subtracts the results of two alternate-phase conversions to yield the final conversion data. The results of subtraction remove the offset. Chop mode is available only for the AIN0 and AIN1 inputs. 图 32 shows the chop mode block diagram.

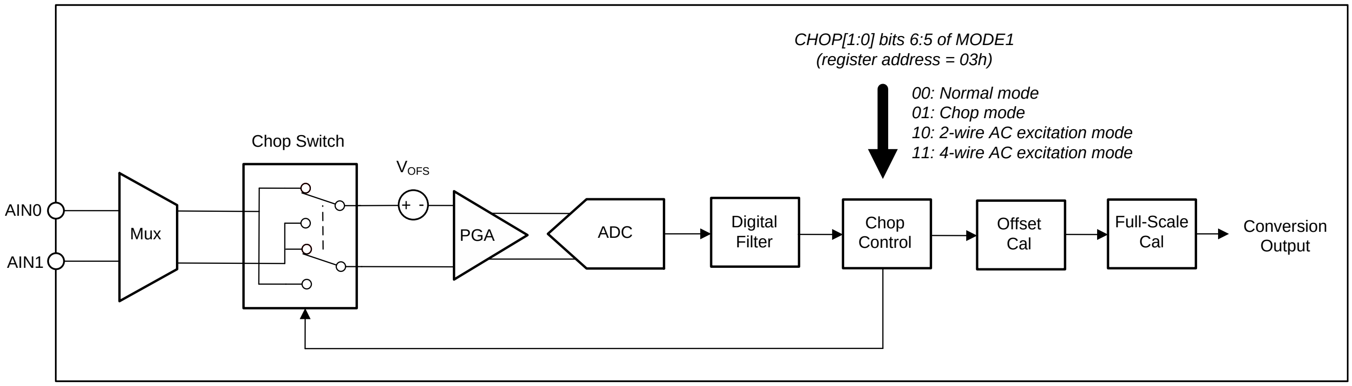

图 32. Chop Mode

V_{OFS} models the internal offset voltage. Chop operation is as follows:

Internal conversion C1: AIN1 – AIN0 + V_{OFS}

(First output withheld)

Internal conversion C2: AIN0 – AIN1 + V_{OFS}

Output 1 = (C1 – C2) / 2 = AIN1 – AIN0

Internal conversion C3: AIN1 – AIN0 + V_{OFS}

Output 2 = (C3 – C2) / 2 = AIN1 – AIN0

Internal conversion C4: AIN0 – AIN1 + V_{OFS}

Output 3 = (C3 – C4) / 2 = AIN1 – AIN0

The sequence repeats for all conversions. Chop mode changes the normal data rate. The order of the sinc filter determines the new data rate. As 表 8 describes, the new data rate is equal to 1 / latency and the first conversion latency is 2 × latency.

The consequence of averaging two data readings in chop is that noise is reduced by $\sqrt{2}$. Divide the noise data in and by 1.4 for the new noise performance data in chop mode. The null frequencies of the digital filter response do not change in chop mode. New null frequencies appear at multiples of f_{DATA} / 2.

8.4.3 AC-Excitation Mode

There are several methods to provide the excitation supply to a resistive bridge: voltage or current, and DC or AC. The AC method can be a sine wave or switched DC voltage or current. Constant DC voltage is the most common technique. AC excitation in this context refers to reversing the polarity of a DC excitation voltage by the use of external switching components. Similar in operation to chop mode, the result of voltage reversal removes offset voltage from the bridge, including residual offset voltage of the ADC itself. The ADS125H02 provides the signals to drive the external components to reverse the bridge voltage.

The timing of the drive signals is synchronized to the ADC conversion phase. During one conversion phase, the voltage polarity is positive. On the alternate conversion phases the voltage polarity is negative. The ADC compensates the negative polarity by reversing the internal reference voltage. The ADC subtracts the data corresponding to the positive and negative phases to mathematically remove offset voltage from the input.

The ADC output drive signals do not overlap to avoid bridge commutation that otherwise can occur during voltage reversal. The AC excitation switching rate is the same as the conversion latency values listed in 表 8. This switch rate avoids unnecessary fast switching. 图 6 illustrates the output drive timing.

表 9 shows the AC-excitation drive signals and the associated GPIO pins. Program the AC-excitation mode using the CHOP[1:0] bits in the MODE1 register. AC excitation is programmed for two-wire or four-wire operation. For two-wire operation, the ADC provides two drive signals. If required, use two external inverters to derive four signals to drive discrete transistors. The GPIO drive levels are referred to the 5-V analog supply. AC-excitation mode changes the normal data rate; see the *Chop Mode* section for details of the new data rate.

表 9. AC-Excitation Drive Pins

DEVICE PIN	GPIO	2-WIRE MODE (CHOP[1:0] = 10)	4-WIRE MODE (CHOP[1:0] = 11)
REFP1/GPIO0	GPIO[0]	$\overline{\text{ACX1}}$	$\overline{\text{ACX1}}$
REFN1/GPIO1	GPIO[1]	$\overline{\text{ACX2}}$	$\overline{\text{ACX2}}$
GPIO2	GPIO[2]	—	ACX1
GPIO3	GPIO[3]	—	ACX2

8.4.4 Clock Mode

Operate the ADC with an external clock or with the internal oscillator. For external clock operation, apply the clock signal to CLKIN. The ADC detects the presence of the external clock and selects the clock automatically. As described in 表 10, the frequency of the external clock depends on the data rate used. Be sure the external clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. For internal clock operation, connect CLKIN to DGND. Be aware of the accuracy of the internal oscillator as described in the *Electrical Characteristics* table. The internal oscillator begins operating immediately at device power-on. Read the CLOCK bit in the STATUS0 register to verify the clock mode.

表 10. External Clock vs Data Rate

DATA RATE	CLOCK FREQUENCY
2.5 SPS to 25600 SPS	7.3728 MHz
40 kSPS	10.24 MHz

8.4.5 Reset

The ADC is reset in three ways: by a power-on reset, via the $\overline{\text{RESET}}$ pin, or by the RESET command.

At reset, the serial interface, conversion-control logic, digital filter, and register map values are reset. The RESET bit of the STATUS0 register is set to indicate which reset occurs. Clear the bit to detect the next device reset. If the START pin is high after reset, the ADC begins conversions.

8.4.5.1 Power-On Reset

At power-on, the ADC is reset and 2^{16} f_{CLK} cycles later the ADC is ready for communication after all the supply voltages cross the respective reset voltage thresholds. Until this time, $\overline{\text{DRDY}}$ is held low. $\overline{\text{DRDY}}$ is then driven high to indicate when ADC communication begins. The conversion cycle starts 512 / f_{CLK} cycle after $\overline{\text{DRDY}}$ asserts high. 图 4 illustrates the power-on reset behavior.

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8.4.5.2 Reset by Pin

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low for a minimum of four f_{CLK} cycles, and then return the pin high. After reset, the conversion starts 512 / f_{CLK} cycles later. See 图 5 for $\overline{\text{RESET}}$ pin timing.

8.4.5.3 Reset by Command

Reset the ADC through the serial interface by the RESET command. Toggle $\overline{\text{CS1}}$ high-to-low first to reset the serial interface before sending the command. After reset, the conversion starts 512 / f_{CLK} cycles later. See 图 5 for the reset command timing.

8.4.6 Calibration

The ADC incorporates calibration registers and associated commands to calibrate offset and full-scale errors. Calibrate the ADC by using calibration commands, or calibrate by writing to the calibration registers directly (user calibration). To calibrate by command, send the offset or full-scale calibration commands. To user calibrate, write to the calibration registers with values based on collecting conversion data. Perform offset calibration before full-scale calibration.

8.4.6.1 Offset and Full-Scale Calibration

Use the offset and full-scale (gain) registers to correct offset or full-scale errors, respectively. As shown in 图 33, the offset calibration register is subtracted from the output data before multiplication by the full-scale register, which is divided by 400000h. After the calibration operation, the final value of the output data is clipped to 24 bits.

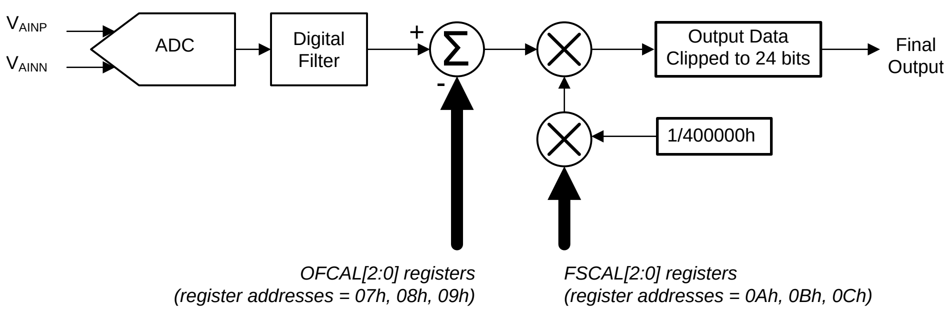

图 33. Calibration Block Diagram

公式 5 shows the internal calibration.

$$\text{Final Output Data} = (\text{Pre Data} – \text{OFCAL[2:0]}) \times \text{FSCAL[2:0]} / 400000\text{h} \quad (5)$$

8.4.6.1.1 Offset Calibration Registers

The offset calibration word, as listed in 表 11, is 24 bits consisting of three 8-bit registers. The offset value is subtracted from the conversion result. The offset value is in two's-complement format with a maximum positive value equal to 7FFFFFh and a maximum negative value equal to 800000h. A register value equal to 000000h has no offset correction. Although the calibration registers provide a wide range of offset values, the input signal cannot exceed ±106% of the precalibrated range; otherwise the ADC is overranged. 表 12 lists example values of the offset register.

表 11. Offset Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
OFCAL0	LSB	07h	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFCAL1	MID	08h	B15	B14	B13	B12	B11	B10	B9	B8
OFCAL2	MSB	09h	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

表 12. Offset Calibration Register Values

OFCAL[2:0] REGISTER VALUE	OFFSET CALIBRATED OUTPUT VALUE
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h

8.4.6.1.2 Full-Scale Calibration Registers

The full-scale calibration word, as listed in 表 13, is 24 bits consisting of three 8-bit registers. The full-scale calibration value is straight binary and normalized to a unity-gain at a value of 400000h. 表 14 lists register values for selected gain factors. Gain errors greater than unity are corrected by full-scale values less than 400000h. Although the calibration registers provide a wide range of possible values, the input signal must not exceed ±106% of the precalibrated input range; otherwise the ADC is overranged.

表 13. Full-Scale Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
FSCAL0	LSB	0Ah	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSCAL1	MID	0Bh	B15	B14	B13	B12	B11	B10	B9	B8
FSCAL2	MSB	0Ch	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

表 14. Full-Scale Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
433333h	1.05
400000h	1
3CCCCCh	0.95

8.4.6.2 Offset Calibration (OFSCAL)

The offset calibration command corrects offset errors. To calibrate offset errors, short the inputs to the ADC or short the inputs to the system. When the command is sent, the ADC averages 16 conversion results to reduce conversion noise to improve calibration accuracy. When calibration is complete, the ADC performs one conversion using the new calibration value. The new calibration value is written to the offset calibration register.

8.4.6.3 Full-Scale Calibration (GANCAL)

The full-scale calibration command corrects gain errors. To calibrate, apply a positive calibration voltage to the ADC, wait for the signal to settle, and then send the command. The ADC averages 16 conversion results to reduce conversion noise to improve calibration accuracy. The ADC computes the full-scale calibration value so that the applied calibration voltage is scaled to an equal positive full-scale output code. The computed result is written to the calibration register. The ADC then performs one new conversion using the new calibration value.

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8.4.6.4 Calibration Command Procedure

Use the following calibration procedure using the calibration commands. The register-lock mode must be UNLOCK prior to using the calibration commands. When calibrating at power-on, make sure the reference voltage has stabilized. Perform an offset calibration operation prior to full-scale calibration.

1. Select the desired input channel, gain, reference mode, and related ADC configurations as required.
2. Apply the appropriate calibration signal (zero or full-scale) to the system inputs.
3. Take the START pin high or send the START command to start conversions. $\overline{\text{DRDY}}$ is driven high.
4. Before the first conversion completes, send the appropriate calibration command. Keep $\overline{\text{CS1}}$ low; otherwise the command is cancelled. Do not send other commands during the calibration period.
5. The calibration time, as described in 表 15, depends on the data rate and digital filter mode. $\overline{\text{DRDY}}$ is driven low when calibration is complete. As a result, offset or full-scale calibration registers are updated with new values. New conversion data are available immediately using the new calibration value.

表 15. Calibration Time (ms)

DATA RATE (SPS)	FILTER MODE(1)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	6801	7601	8401	9201	—	6805
5	3401	3801	4201	4601	—	3405
10	1701	1901	2101	2300	—	1705
16.6	1021	1141	1261	1381	—	—
20	850.7	951	1051	1151	—	854.5
50	340.9	380.9	421	460.9	—	—
60	284.1	317.7	350.9	384.4	—	—
100	170.8	190.9	210.9	230.8	—	—
400	43.27	48.43	53.42	58.41	—	—
1200	14.93	16.72	18.4	20.07	—	—
2400	7.845	8.816	9.643	10.48	—	—
4800	4.302	4.858	5.276	5.692	—	—
7200	3.123	3.534	3.815	4.095	—	—
14400	—	—	—	—	1.941	—
19200	—	—	—	—	1.49	—
25600	—	—	—	—	1.133	—
40000	—	—	—	—	0.738	—

(1) Nominal clock frequency. Chop and AC-excitation modes are disabled.

8.4.6.5 User Calibration Procedure

To user calibrate, apply the calibration voltage, acquire conversion data, and compute the calibration value. Write the computed value to the corresponding calibration registers. Before starting calibration, preset the offset and full-scale registers to 000000h and 400000h, respectively.

To offset calibrate, short the inputs to the system and average *n* number of the conversion data. Averaging conversion data reduces noise to increase calibration accuracy. Write the average value of the conversion data to the offset registers.

To gain calibrate using a full-scale calibration signal, temporarily reduce the full-scale register by 95% to avoid any output clipped codes (set FSCAL[2:0] to 3CCCCCh). Acquire *n* number of conversions and average the conversions to increase calibration accuracy. Compute the full-scale calibration value as shown in 公式 6:

Full-Scale Calibration Value = (Expected Code / Actual Code × 400000h

where:

- Expected code = 799998h using full-scale calibration signal and 95% precalibration scale factor (6)

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8.5 Programming

8.5.1 Serial Interface

The SPI-compatible serial interface is used to read conversion data, to configure the device registers, and to control ADC operation. The CRC is used to validate error-free transmission of input and output data flow. The serial interface consists of the following control signals: $\overline{CS1}$, $\overline{CS2}$, SCLK, DIN, and DOUT/$\overline{DRDY}$. Most microcontroller SPI peripherals can operate with the ADC. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated or changed on the SCLK rising edges; data are latched or read on the SCLK falling edges. Timing details of the SPI protocol are provided in 图 1 and 图 2.

8.5.1.1 *Chip-Select Pins ($\overline{CS1}$ and $\overline{CS2}$)*

The ADS125H0x devices are implemented as multi-chip modules (MCM), consisting of discrete chips for the PGA and the ADC. The PGA and ADC chips have independent serial interfaces, with SPI signals SCLK, DIN, and DOUT/$\overline{DRDY}$ connected in common. The serial interfaces are enabled by $\overline{CS1}$ and $\overline{CS2}$. $\overline{CS1}$ enables communication to the ADC chip and $\overline{CS2}$ enables communication to the PGA chip. Communicate to the device by driving one chip-select pin low at a time, corresponding to the PGA or the ADC.

Chip-select pins $\overline{CS1}$ and $\overline{CS2}$ are active low. One chip-select pin must be low and remain low for the duration the command operation. Take the chip-select pin high after the command operation. When the chip-select pin is taken high, the corresponding serial interface resets and SCLK activity is ignored (thus blocking any applicable commands). When both chip-select pins are high, DOUT/$\overline{DRDY}$ enters the high-impedance state. $\overline{CS1}$ must be low in order to monitor the conversion data-ready function of DOUT/$\overline{DRDY}$. $\overline{DRDY}$ is active regardless of the state of either chip-select pin.

8.5.1.2 *Serial Clock (SCLK)*

SCLK is an input that clocks data into and out of the ADC. Output data are updated on the rising edge of SCLK and input data are latched by the device on the falling edge of SCLK. Return SCLK low after the data operation is completed. SCLK is a Schmidt-triggered input designed to provide noise immunity. Even though SCLK is noise resistant, keep SCLK noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. Use a series termination resistor at the SCLK drive pin to reduce ringing.

8.5.1.3 *Data Input (DIN)*

DIN is the ADC serial data input. DIN inputs commands and register data to the ADC. Input data are latched by the device on the falling edge of SCLK.

8.5.1.4 *Data Output/Data Ready (DOUT/$\overline{DRDY}$)*

The DOUT/$\overline{DRDY}$ pin is a dual-function data output pin. The functions are data output and conversion-data ready. The functionality changes depending on whether a read data (or read register) operation is in progress. When not in communication with the device and with $\overline{CS1}$ low, the pin indicates data ready by asserting low. During a read data or read register operation, the pin provides output data. After the read operation is completed, the function of the pin returns to the conversion-data ready mode. Data are updated on the SCLK rising edge, therefore the user latches the data on the falling edge.

$\overline{CS1}$ must be low for DOUT/$\overline{DRDY}$ to provide the data-ready function. When both chip-select pins are high, DOUT/$\overline{DRDY}$ is in high-impedance mode (tri-state).

8.5.2 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ asserts low to indicate that new conversion data are ready for readback. The operation of $\overline{DRDY}$ depends on the mode (continuous or pulse) and whether or not the conversion data are retrieved.

8.5.2.1 *$\overline{DRDY}$ in Continuous-Conversion Mode*

In continuous-conversion mode, $\overline{DRDY}$ is driven high when conversions are started and is driven low when conversion data are ready. During data readback, $\overline{DRDY}$ returns high, which signals completion of the read operation. If the conversion data are not read, $\overline{DRDY}$ pulses high 16 f_{CLK} cycles prior to the next falling edge.

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To read back the current (old) conversion data before the next conversion completes, send the read data command 16 f_{CLK} cycles prior to the next DRDY falling edge. If the readback command is sent *less than* 16 f_{CLK} cycles prior to the DRDY falling edge, *either* old or new conversion data are provided. Whether old or new data are provided for readback depends on the timing of the command. In the case that old data are provided, the assertion of DRDY corresponding to the new data is delayed until after the read data operation has completed. In this case, the DRDY bit of the STATUS0 byte is cleared to indicate the old data has been read. In the case that new conversion data are provided, DRDY transitions low with no delay. In this case, the DRDY bit of the STATUS0 byte is set to 1 to indicate new data are read. To ensure readback of new conversion data, wait until DRDY asserts low before starting the data read operation.

8.5.2.2 DRDY in Pulse-Conversion Mode

DRDY is driven high at conversion start and is driven low when the conversion data are ready. DRDY remains low until a new conversion is started.

图 34 shows DRDY operation with and without data retrieval in two conversion modes.

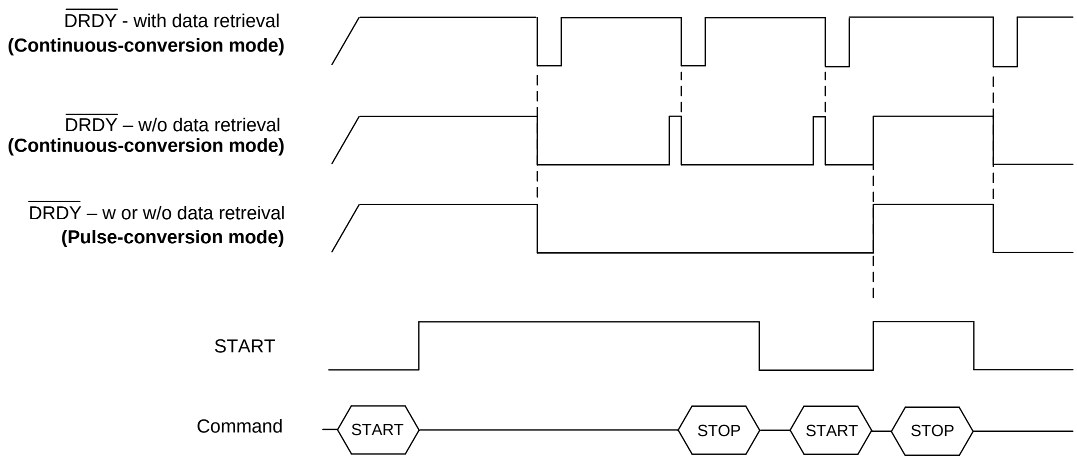

图 34. DRDY Operation

8.5.2.3 Data Ready by Software Polling

The DRDY bit in the STATUS word can optionally be polled by user software instead of having hardware poll the DRDY pin. To software poll, read the STATUS0 byte and poll the DRDY bit. In order to not miss conversion data when in free-running operation, poll the bit at least as often as the period of the data rate. If the DRDY bit is set, then conversion data are new since the last data read operation. If the DRDY bit is clear, conversion data are not new since the last data read operation. In this case, the previous conversion data are returned.

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8.5.3 Conversion Data

Conversion data are read by the RDATA command. To read data, take $\overline{CS1}$ low and issue the read data command. The conversion data field consists of an optional STATUS0 byte, three data bytes, and the CRC byte. The CRC byte is computed over the combination of STATUS0 byte and conversion data bytes. See the *RDATA Command* section for details on reading conversion data.

8.5.3.1 Main Status Byte (STATUS0)

The status byte contains information on the operating state of the ADC. The STATUS0 byte is optionally included with the conversion data by enabling the STATENB bit of the MODE3 register. Read the STATUS0 register directly to read status information without the need to read conversion data with the optional embedded status information.

8.5.3.2 Conversion Data Format

The conversion data are 24 bits, in two's-complement format to represent positive and negative values. The data begins with the most significant bit (sign bit) first. The data are scaled so that V_{IN} = 0 V results in an uncalibrated code value of 000000h, the positive full-scale input is equal to an uncalibrated value of 7FFFFFh and the negative full-scale input is equal to an uncalibrated code value of 800000h. 表 16 shows the code values. The data are clipped to 7FFFFFh and 800000h during positive and negative signal overdrive, respectively.

表 16. ADC Conversion Data Codes

DESCRIPTION	INPUT SIGNAL (V)	24-BIT CONVERSION DATA (1)
Positive full scale	$\geq V_{REF}$ / Gain × (2^{23} – 1) / 2^{23}	7FFFFFh
1 LSB	V_{REF} / (Gain × 2^{23})	000001h
Zero scale	0	000000h
–1 LSB	$-V_{REF}$ / (Gain × 2^{23})	FFFFFFh
Negative full scale	$\leq -V_{REF}$ / Gain	800000h

(1) Ideal (calibrated) output code.

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8.5.4 Cyclic Redundancy Check (CRC)

Cyclic redundancy check (CRC) is an error detection byte value that detects communication errors to and from the host and ADC. CRC is the division remainder of the payload data by the prescribed CRC polynomial. The payload data are 1, 2, 3, or 4 bytes depending on the data transfer operation.

The host computes the CRC over the two required command bytes and appends the CRC to the command string (3rd byte). A 4th, zero-value byte completes the command field to the ADC. The ADC performs the CRC calculation and compares the result to the CRC transmitted by the host. If the host and ADC CRC values match, the command executes and the ADC responds by transmitting the valid CRC during the 4th byte of the command. If the operation is data read, the ADC responds with a second CRC that is computed for the requested data byte payload. The response data payload is 1, 3, or 4 bytes depending on the type of operation.

If the host and ADC CRC values *do not* match, the command does not execute and the ADC responds with an *inverted* CRC value, calculated over the received command bytes. The inverted CRC is intended to signal the host of the failed operation. The host terminates transmission of further bytes to stop the command operation. The CRC1ERR bit is set in the STATUS0 register when a error pertaining to ADC registers occur. The STAT12 and CRC2ERR flags are set when an error pertaining to PGA registers occur.

The ADC is ready to accept the next command after all required bytes are transmitted when no CRC error occurs, or after a CRC error occurs when terminated at the end of the 4th command byte.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X + 1$. The nine binary polynomial coefficients are: 100000111b.

The following is a general procedure to compute the CRC value:

1. Left shift the concatenated 1-, 2-, 3-, or 4-byte argument (if required) to create a new 40-bit data value (the starting data value). The shifted data are padded with ones to the right of the argument.
2. Align the MSB of the CRC polynomial (100000111) to the left-most, logic-one value of the data.
3. Perform an XOR operation on the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter length value. The bits of the data values that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result.
4. When the XOR result is less than 100000000b, the procedure ends, yielding the 8-bit CRC value. Otherwise, continue with the XOR operation shown in step 2 using the current data value. The number of loop iterations depends on the value of the initial data.

The following sections detail the input and output data of each command. In the descriptions that follow, these CRC mnemonics apply:

- **CRC-2**: Input the CRC of command bytes 1 and 2. Except for the WREG command, the value of byte 2 is arbitrary.
- **Out CRC-1**: Output the CRC of one register data byte.
- **Out CRC-2:** Output the CRC of two command bytes, inverted value if an input CRC error is detected.
- **Out CRC-3:** Output the CRC of three conversion data bytes.
- **Out CRC-4:** Output the CRC of three conversion data bytes plus the STATUS0 byte.
- **Echo Byte 1:** Echo of received input byte 1.
- **Echo Byte 2:** Echo of received input byte 2.

8.5.5 Commands

Commands are used to read conversion data, control the device, and read and write register data. 表 17 provides a list of commands and the corresponding command byte sequence. Only send the commands that are listed in 表 17. The column labeled *SECTION* shows the commands that apply to the device ADC section and that apply to the device PGA section. Take CS1 low to enable the interface to the ADC section. Take CS2 low to enable the interface to the PGA section. See the *Chip-Select Pins (CS1 and CS2)* section for details of chip-select operation. The ADS125H0x device validates command operations by the CRC sent from the host. If a CRC error occurs, the ADC rejects the command.

表 17. Command Byte Summary

MNEMONIC	SECTION(1)	DESCRIPTION	BYTE 1	BYTE 2(2)	BYTE 3	BYTE 4
CONTROL COMMANDS						
NOP	----	No operation	00h	Arbitrary	CRC-2	00h
RESET	ADC	Reset	06h	Arbitrary	CRC-2	00h
START	ADC	Start conversion	08h	Arbitrary	CRC-2	00h
STOP	ADC	Stop conversion	0Ah	Arbitrary	CRC-2	00h
READ DATA COMMAND						
RDATA	ADC	Read conversion data	12h	Arbitrary	CRC-2	00h
CALIBRATION COMMANDS						
OFSCAL	ADC	Offset calibration	16h	Arbitrary	CRC-2	00h
GANCAL	ADC	Gain calibration	17h	Arbitrary	CRC-2	00h
REGISTER COMMANDS						
RREG	ADC, PGA	Read register data	20h + rrh(3)	Arbitrary	CRC-2	00h
WREG	ADC, PGA	Write register data	40h + rrh(3)	Register data	CRC-2	00h
PROTECTION COMMANDS						
LOCK	ADC, PGA	Register data lock	F2h	Arbitrary	CRC-2	00h
UNLOCK	ADC, PGA	Register data unlock	F5h	Arbitrary	CRC-2	00h

(1) CS1 enables commands directed to the ADC section. CS2 enables commands directed to the PGA section.
(2) Excluding the write-register command, the value of the second byte is arbitrary (any value) but *is* included in the CRC calculation.
(3) rrh = 5-bit register address.

8.5.5.1 General Command Format

The ADC executes the command after transmission of the 4th byte in the sequence. The value of the second command byte is arbitrary but is included in the CRC calculation (two-byte CRC payload). Forcing the chip-select pin high before the command completes results in termination of the command. 图 35 shows an example of the register write operation by writing data to register address 02h (command opcode 42h). The host calculates the CRC of the two command bytes. The out CRC-2 byte is the output (ADC calculated) CRC based on the received command bytes. Because the example shows access to register address = 02h (which belongs to the ADC register block), take CS1 low, or optionally, take both CS1 and CS2 low. The first byte output from the ADC is always 0FFh. The chip-select input must be toggled between command operations.

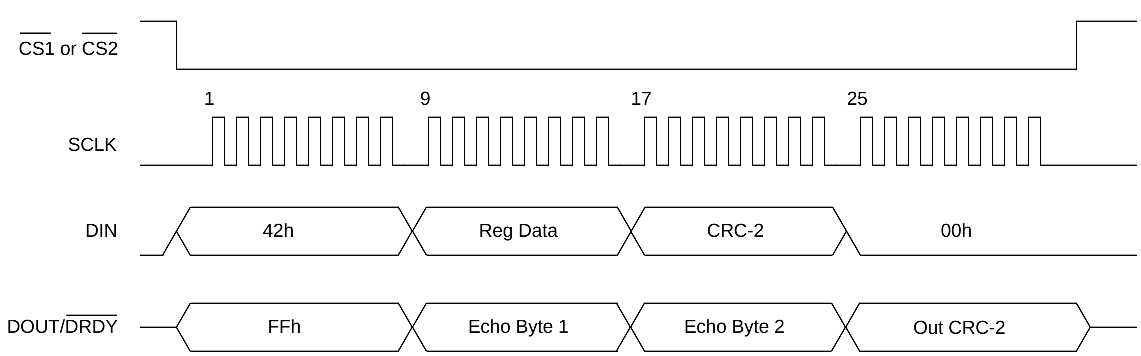

图 35. Register Write Command Sequence (Address = 02h)

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The following sections detail the input and output byte sequence corresponding to each command. See the *Cyclic Redundancy Check (CRC)* section for the notation used for the CRC.

8.5.5.2 NOP Command

This command has no operation. Use the NOP command to validate the CRC response byte and error detection without affecting normal operation. 表 18 shows the NOP command byte sequence.

表 18. NOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	00h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.3 RESET Command

The RESET command resets the ADC operation and resets all registers to default. See the *Reset by Command* section for details. 表 19 lists the RESET command byte sequence.

表 19. RESET Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	06h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.4 START Command

This command starts a conversions. See the *Conversion Control* section for details. 表 20 lists the START command byte sequence.

表 20. START Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	08h	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.5 STOP Command

This command is used to stop conversions. See the *Conversion Control* section for details. 表 21 lists the STOP command byte sequence.

表 21. STOP Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	0Ah	Arbitrary	CRC-2	00h
DOUT/$\overline{DRDY}$	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.6 RDATA Command

This command reads conversion data. Because the data are buffered, the data can be read at any time during the conversion sequence. If data are read *near* the completion of the conversion phase, old or new conversion data are returned. See the *Data Ready ($\overline{DRDY}$)* section for details.

The response data of the ADC varies in length depending on inclusion of the optional STATUS0 byte. See the *Conversion Data Format* section for details of the format of the conversion data. 表 22 and 图 36 describe the RDATA command byte sequence that includes the STATUS0 byte.

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表 22. RDATA Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
DIN	12h	Arbitrary	CRC-2	00h	00h	00h	00h	00h	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2	STATUS0(1)	MSB data	MID data	LSB data	Out CRC-3 or Out CRC-4(2)

(1) Optional STATUS0 byte shown.
(2) Out CRC-4 (4-byte CRC = STATUS0 + data) if the STATUS0 byte is included in the data packet.

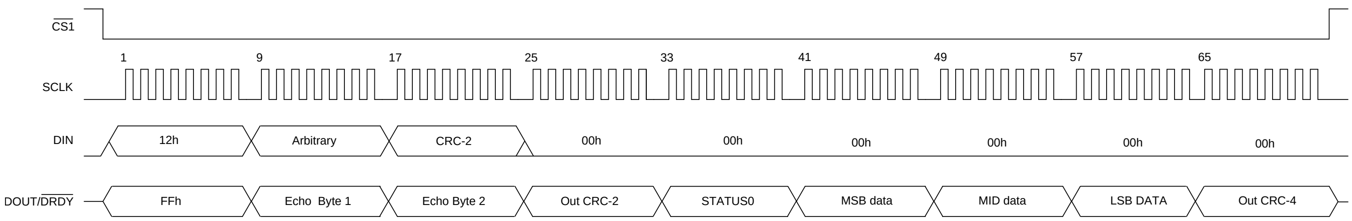

图 36. Conversion Data Read Operation

8.5.5.7 OFSCAL Command

This command is used for offset calibration. See the *Calibration* section for details. 表 23 lists the OFSCAL command byte sequence.

表 23. OFSCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	16h	Arbitrary	CRC-2	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.8 GANCAL Command

This command is used for gain calibration. See the *Calibration* section for details. 表 24 lists the GANCAL command byte sequence.

表 24. GANCAL Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	17h	Arbitrary	CRC-2	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.9 RREG Command

Use the RREG command to read register data. Take CS1 low to access registers within the ADC register block. Take CS2 low to access registers within the PGA register block (see the *Register Map* section for the register block map). Register data are read one byte at a time using the RREG command for each operation. Add the register address (rrh) to the base opcode (20h) to complete the command byte (20h + rrh). 表 25 lists the RREG command byte sequence. The ADC responds with the register data byte, most significant bit first. Data for registers addressed outside the range is 00h. Out CRC-2 is the output CRC corresponding to the received command bytes. Out CRC-1 is the output CRC corresponding to the single register data byte.

表 25. RREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
DIN	20h + rrh	Arbitrary	CRC-2	00h	00h	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2	Register data	Out CRC-1

8.5.5.10 WREG Command

Use the WREG command to write register data. Take CS1 low to access registers within the ADC register block. Take CS2 low to access registers within the PGA register block (see the *Register Map* section for the register block map). The WREG command writes the register data one byte at a time using the WREG command for each operation. Add the register address (rrh) to the base opcode (40h) to complete the command byte (40h + rrh). 表 26 lists the WREG command byte sequence. Writing to certain registers results in conversion restart. 表 29 lists the affected registers. Do not write to registers outside the address range.

Register-write access is enabled and disabled by the UNLOCK and LOCK commands, respectively. The default mode is register UNLOCK. See the *LOCK Command* section.

表 26. WREG Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	40h + rrh	Register data	CRC-2	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.11 LOCK Command

Use the LOCK command to prevent write operations with unintended data. The ADC register blocks and PGA register blocks are locked and unlocked from write access by assertion of the corresponding chip-select pin. Locking the registers disables register write access including the calibration registers. The default mode is unlocked. Register reads are allowed in LOCK mode. 表 27 lists the LOCK command byte sequence.

表 27. LOCK Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	F2h	Arbitrary	CRC-2	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.5.5.12 UNLOCK Command

Use the UNLOCK command to allow writing register data. The ADC register blocks and PGA register blocks are locked and unlocked from write access by assertion of the corresponding chip-select pin. Register unlock allows register write access including calibration registers. 表 28 lists the UNLOCK command byte sequence.

表 28. UNLOCK Command

DIRECTION	BYTE 1	BYTE 2	BYTE 3	BYTE 4
DIN	F5h	Arbitrary	CRC-2	00h
DOUT/DRDY	FFh	Echo byte 1	Echo byte 2	Out CRC-2

8.6 Register Map

The register map consists of 19 single-byte registers. Collectively, the registers are used to configure the ADC to the desired operating mode. Access the registers by using the RREG and WREG commands (register-read and register-write, respectively). Register data are accessed one register byte at a time for each command operation. The register addresses are assigned to either the ADC register block or to the PGA register block. $\overline{CS1}$ selects registers within the ADC register block 1. $\overline{CS2}$ selects registers within the PGA register block. As shown in the *Default* column of 表 29, the registers reset to their default values at power-on. Changing the data of certain registers results in restart of conversions in progress. The *ADC Restart* column in 表 29 lists these registers.

表 29. Register Map Summary

ADDRESS	REGISTER	DEFAULT	RESTART	BLOCK	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	xxh		ADC	DEV_ID[3:0]				REV_ID1[3:0]			
01h	STATUS0	01h		ADC	LOCK1	CRC1ERR	0	STAT12	REFALM	DRDY	CLOCK	RESET
02h	MODE0	24h	Yes	ADC	DR[4:0]					FILTER[2:0]		
03h	MODE1	01h	Yes	ADC	0	CHOP[1:0]		CONVRT	DELAY[3:0]			
04h	MODE2	00h		ADC	GPIO_CON[3:0]				GPIO_DIR[3:0]			
05h	MODE3	00h		ADC	0	STATENB	0	0	GPIO_DAT[3:0]			
06h	REF	05h	Yes	ADC	0	0	0	REFENB	RMUXP[1:0]		RMUXN[1:0]	
07h	OFCAL0	00h		ADC	OFC[7:0]							
08h	OFCAL1	00h		ADC	OFC[15:8]							
09h	OFCAL2	00h		ADC	OFC[23:16]							
0Ah	FSCAL0	00h		ADC	FSC[7:0]							
0Bh	FSCAL1	00h		ADC	FSC[15:8]							
0Ch	FSCAL2	40h		ADC	FSC[23:16]							
0Dh	I_MUX	FFh		ADC	I_MUX2[3:0]				I_MUX1[3:0]			
0Eh	I_MAG	00h		ADC	I_MAG2[3:0]				I_MAG1[3:0]			
0Fh	RESERVED	00h		ADC	00h							
10h	MODE4	50h		PGA	0	MUX[2:0]			GAIN[3:0]			
11h	STATUS1	xxh		PGA	PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
12h	STATUS2	0xh		PGA	0	0	LOCK2	CRC2ERR	REV_ID2[3:0]			

表 30 lists the access codes for the ADS125H0x registers.

表 30. ADS125H0x Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R/W	R-W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 Device Identification (ID) Register (address = 00h) [reset = xxh]

ID is shown in 图 37 and described in 表 31.

Return to Register Map Summary.

图 37. ID Register(1)

7	6	5	4	3	2	1	0
DEV_ID[3:0]				REV_ID1[3:0]			
R-xh				R-xh			

(1) Reset values are dependent on the device.

表 31. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DEV_ID[3:0]	R	xh	**Device ID** 0100: ADS125H01 0110: ADS125H02
3:0	REV_ID1[3:0]	R	xh	**Revision ID1** There are two revision ID fields: REV_ID1 and REV_ID2. The revision IDs can change without notification.

ADVANCE INFORMATION

8.6.2 Main Status (STATUS0) Register (address = 01h) [reset = 01h]

STATUS0 is shown in 图 38 and described in 表 32.

Return to Register Map Summary.

图 38. STATUS0 Register

7	6	5	4	3	2	1	0
LOCK1	CRC1ERR	0	STAT12	REFALM	DRDY	CLOCK	RESET
R-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-xh	R/W-1h

表 32. STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOCK1	R	0h	**ADC Register Block Lock1 Status** This bit indicates the lock status of the ADC section register block. Writes to the ADC register block are locked by the LOCK command and unlocked by the UNLOCK command. 0: ADC section registers not locked (default) 1: ADC section registers block locked See the STATUS2 register for the PGA section of the register block status.
6	CRC1ERR	R/W	0h	**ADC Register Block CRC1 Error** Indicates CRC1 errors to commands addressing the ADC block of the device. Write 0 to clear the CRC1 error. 0: No CRC1 error to ADC block of device 1: CRC1 error to the ADC block of the device See STATUS2 register for the PGA section CRC error status.
5	0	R	0h	**Reserved** Always write 0.
4	STAT12	R	0h	**STAT12 Error Flag** Indicates one or more error bits are logged to the PGA error registers STATUS1 or STATUS2. Read the STATUS1 and STATUS2 registers to determine the source of the error. This bit clears after the errors are cleared. 0: No error 1: Error logged to the STATUS1 or STATUS2 registers
3	REFALM	R	0h	**Reference Alarm** This alarm is set if the reference voltage is < 0.4 V. The alarm updates at each new conversion cycle (auto-reset). 0: No reference low alarm 1: Reference low alarm
2	DRDY	R	0h	**Data Ready** Indicates new conversion data. 0: Conversion data are not new from the last data read 1: Conversion data are newfrom the last data read
1	CLOCK	R	xh	**Clock** Indicates internal or external clock mode. The ADC automatically selects the clock mode. 0: ADC clock is internal 1: ADC clock is external
0	RESET	R/W	1h	**Reset** Indicates an ADC reset has occurred. Clear the bit to detect the next device reset. 0: No reset 1: Reset (default)

8.6.3 Mode 0 (MODE0) Register (address = 02h) [reset = 24h]

MODE0 is shown in 图 39 and described in 表 33.

Return to Register Map Summary.

图 39. MODE0 Register

7	6	5	4	3	2	1	0
DR[4:0]					FILTER[2:0]		
R/W-4h					R/W-4h		

表 33. MODE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	DR[4:0]	R/W	4h	**Data Rate** These bits select the data rate. 00000: 2.5 SPS 00001: 5 SPS 00010: 10 SPS 00011: 16.$\overline{6}$ SPS 00100: 20 SPS (default) 00101: 50 SPS 00110: 60 SPS 00111: 100 SPS 01000: 400 SPS 01001: 1200 SPS 01010: 2400 SPS 01011: 4800 SPS 01100: 7200 SPS 01101: 14400 SPS 01110: 19200 SPS 01111: 25600 SPS 10000 - 11111: 40 kSPS (f_{CLK} = 10.24 MHz)
2:0	FILTER[2:0]	R/W	4h	**Digital Filter** (see the *Digital Filter* section) These bits select the digital filter mode. 000: Sinc1 001: Sinc2 010: Sinc3 011: Sinc4 100: FIR (default) 101-111: Reserved

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8.6.4 Mode 1 (MODE1) Register (address = 03h) [reset = 01h]

MODE1 is shown in 图 40 and described in 表 34.

Return to Register Map Summary.

图 40. MODE1 Register

7	6	5	4	3	2	1	0
0	CHOP[1:0]		CONVRT	DELAY[3:0]			
R/W-0h	R/W-0h		R/W-0h	R/W-1h			

表 34. MODE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	**Reserved** Always write 0
6:5	CHOP[1:0]	R/W	0h	**Chop and AC-Excitation Modes** Select the chop or ac-excitation operating modes. See the *Chop Mode* and *AC-Excitation Mode* sections. 00: Normal mode (default) 01: Chop mode 10: 2-wire AC-excitation mode (ADS125H02 only) 11: 4-wire AC-excitation mode (ADS125H02 only)
4	CONVRT	R/W	0h	**Conversion Mode** Select the ADC conversion mode. See the *Conversion Control* section. 0: Continuous conversions (default) 1: Pulse (one shot) conversion
3:0	DELAY[3:0]	R/W	1h	**Conversion Start Delay** Program the time delay at conversion start. See the *Start-Conversion Delay* section. 0000: 0 µs (not for 25600-SPS or 40-kSPS operation) 0001: 50 µs (default) 0010: 59 µs 0011: 67 µs 0100: 85 µs 0101: 119 µs 0110: 189 µs 0111: 328 µs 1000: 605 µs 1001: 1.16 ms 1010: 2.27 ms 1011: 4.49 ms 1100: 8.93 ms 1101: 17.8 ms 1110-1111: Reserved

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8.6.5 Mode 2 (MODE2) Register (address = 04h) [reset = 00h]

MODE2 is shown in 图 41 and described in 表 35.

Return to Register Map Summary.

图 41. MODE2 Register

7	6	5	4	3	2	1	0
GPIO_CON[3:0]				GPIO_DIR[3:0]			
R/W-0h				R/W-0h			

表 35. MODE2 Register Field Descriptions(1)

Bit	Field	Type	Reset	Description
7	GPIO_CON[3]	R/W	0h	**GPIO[3] Pin Connection** Connect GPIO[3] to the GPIO3 pin. 0: GPIO[3] not connected to GPIO3 (default) 1: GPIO[3] connected to GPIO3
6	GPIO_CON[2]	R/W	0h	**GPIO[2] Pin Connection** Connect GPIO[2] to the GPIO2 pin. 0: GPIO[2] not connected to GPIO2 (default) 1: GPIO[2] connected to GPIO2
5	GPIO_CON[1]	R/W	0h	**GPIO[1] Pin Connection** Connect GPIO[1] to the REFN1/GPIO1 pin. 0: GPIO[1] not connected to REFN1/GPIO1 (default) 1: GPIO[1] connected to REFN1/GPIO1
4	GPIO_CON[0]	R/W	0h	**GPIO[0] Pin Connection** Connect GPIO[0] to the REFP1/GPIO0 pin. 0: GPIO[0] not connected to REFP1/GPIO0 (default) 1: GPIO[0] connected to REFP1/GPIO0
3	GPIO_DIR[3]	R/W	0h	**GPIO[3] Pin Direction** Configure GPIO[3] as a GPIO input or output to the GPIO3 pin. 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
2	GPIO_DIR[2]	R/W	0h	**GPIO[2] Pin Direction** Configure GPIO[2] as a GPIO input or output to the GPIO2 pin. 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
1	GPIO_DIR[1]	R/W	0h	**GPIO[1] Pin Direction** Configure GPIO[1] as a GPIO input or output to the REFN1/GPIO1 pin. 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
0	GPIO_DIR[0]	R/W	0h	**GPIO[0] Pin Direction** Configure GPIO[0] as a GPIO input or output to the REFP1/GPIO0 pin. 0: GPIO[0] is an output (default) 1: GPIO[0] is an input

(1) ADS125H02 only.

8.6.6 Mode 3 (MODE3) Register (address = 05h) [reset = 00h]

MODE3 is shown in 图 42 and described in 表 36.

Return to Register Map Summary.

图 42. MODE3 Register

7	6	5	4	3	2	1	0
0	STATENB	0	0	GPIO_DAT[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

表 36. MODE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	**Reserved** Always write 0h.
6	STATENB	R/W	0h	**STATUS0 Byte Enable** Enable the STATUS0 byte for inclusion during conversion data read operation. 0: Exclude STATUS0 byte during conversion data read (default) 1: Include STATUS0 byte during conversion data read
5,4	0	R/W	0h	**Reserved** Always write 0h.
3	GPIO_DAT[3]	R/W	0h	**GPIO[3] Data**(1) Read or write the GPIO data on the GPIO3 pin. 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	GPIO_DAT[2]	R/W	0h	**GPIO[2] Data**(1) Read or write the GPIO data on the GPIO2 pin. 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	GPIO_DAT[1]	R/W	0h	**GPIO[1] Data**(1) Read or write the GPIO data on the REFN1/GPIO1 pin. 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	GPIO_DAT[0]	R/W	0h	**GPIO[0] Data**(1) Read or write the GPIO data on the REFP1/GPIO0 pin. 0: GPIO[0] is low (default) 1: GPIO[0] is high

(1) ADS125H02 only.

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8.6.7 Reference Configuration (REF) Register (address = 06h) [reset = 05h]

REF is shown in 图 43 and described in 表 37.

Return to Register Map Summary.

图 43. REF Register

7	6	5	4	3	2	1	0
0	0	0	REFENB	RMUXP[1:0]		RMUXN[1:0]	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h		R/W-1h	

表 37. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	0	R/W	0h	**Reserved** Always write 0h.
4	REFENB	R/W	0h	**Internal Reference Enable** Enable the internal reference. 0: Internal reference disabled (default) 1: Internal reference enabled
3:2	RMUXP[1:0]	R/W	1h	**Reference Positive Input** (see the *Reference Voltage* section) Select the positive reference input. 00: Internal reference positive 01: AVDD (default) 10: REFP0 external 11: REFP1/GPIO0 external(1)
1:0	RMUXN[1:0]	R/W	1h	**Reference Negative Input** (see the *Reference Voltage* section) Select the negative reference input. 00: Internal reference negative 01: AGND (default) 10: REFN0 external 11: REFN1/GPIO1 external(1)

(1) ADS125H02 only.

8.6.8 Offset Calibration (OFCALx) Registers (address = 07h, 08h, 09h) [reset = 00h, 00h, 00h]

OFCALx is shown in 图 44 and described in 表 38.

Return to Register Map Summary.

图 44. OFCAL0, OFCAL1, OFCAL2 Registers

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

表 38. OFCAL0, OFCAL1, OFCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration** These three registers are the 24-bit offset calibration word. The offset calibration is in two's-complement data format. The offset value is subtracted from the conversion result before the full-scale operation.

8.6.9 Full-Scale Calibration (FSCALx) Registers (address = 0Ah, 0Bh, 0Ch) [reset = 00h, 00h, 40h]

FSCALx is shown in 图 45 and described in 表 39.

Return to Register Map Summary.

图 45. FSCAL0, FSCAL1, FSCAL2 Registers

7	6	5	4	3	2	1	0
FSCAL[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSCAL[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSCAL[23:16]							
R/W-40h							

表 39. FSCAL0, FSCAL1, FSCAL2 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	FSCAL[23:0]	R/W	400000h	**Full-Scale Calibration** These three registers are the 24-bit full-scale calibration word. The full-scale calibration is in straight binary data format. The full-scale value is divided by 400000h and multiplied with the conversion data. The scaling operation occurs after the offset operation.

8.6.10 Current Source Multiplexer (I_MUX) Register (address = 0Dh) [reset = FFh]

I_MUX is shown in 图 46 and described in 表 40.

Return to Register Map Summary.

图 46. I_MUX Register

7	6	5	4	3	2	1	0
I_MUX2[3:0]				I_MUX1[3:0]			
R/W-Fh				R/W-Fh			

表 40. I_MUX Register Field Descriptions(1)

Bit	Field	Type	Reset	Description
7:4	I_MUX2[3:0]	R/W	Fh	**Current Source 2 Output Multiplexer** These bits select the IDAC2 pin connection. 0000-0111: No connection 1000: Connect current source 2 to pin IDAC1 1001: Connect current source 2 to pin IDAC2 1010-1111: No connection (default = 1111)
3:0	I_MUX1[3:0]	R/W	Fh	**Current Source 1 Output Multiplexer** These bits select the IDAC1 pin connection. 0000-0111: No connection 1000: Connect current 1 to pin IDAC1 1001: Connect current 1 to pin IDAC2 1010-1111: No connection (default = 1111)

(1) ADS125H02 only.

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8.6.11 Current Source Magnitude (I_MAG) Register (address = 0Eh) [reset = 00h]

I_MAG is shown in 图 47 and described in 表 41.

Return to Register Map Summary.

图 47. I_MAG Register

7	6	5	4	3	2	1	0
I_MAG2[3:0]				I_MAG1[3:0]			
R/W-0h				R/W-0h			

表 41. I_MAG Register Field Descriptions[(1)]

Bit	Field	Type	Reset	Description
7:4	I_MAG2[3:0]	R/W	0h	**Current Source 2 Magnitude** These bits select current source 2 magnitude. 0000: Off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011-1111: Off
3:0	I_MAG1[3:0]	R/W	0h	**Current Source 1 Magnitude** These bits select current source 1 magnitude. 0000: Off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011-1111: Off

(1) ADS125H02 only.

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8.6.12 Reserved (RESERVED) Register (address = 0Fh) [reset = 00h]

RESERVED is shown in 图 48 and described in 表 42.

Return to Register Map Summary.

图 48. RESERVED Register

7	6	5	4	3	2	1	0
00h							
R/W-00h							

表 42. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	0	R	0h	**Reserved bits** Always write 00h.

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8.6.13 MODE4 (MODE4) Register (address = 10h) [reset = 50h]

MODE4 is shown in 图 49 and described in 表 43.

Return to Register Map Summary.

图 49. MODE4 Register

7	6	5	4	3	2	1	0
0	MUX[2:0]			GAIN[3:0]			
R/W-0h	R/W-5h			R/W-0h			

表 43. MODE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R	0h	**Reserved** Always write 0h.
6:4	MUX[2:0]	R/W	5h	**Input Multiplexer** These bits set the input multiplexer control. 000: AIN1 – AIN0 001: AIN0 – AIN1 (reserved for use with final silicon) 010: AIN1 – AINCOM 011: AIN0 – AINCOM 100: HV supply readback (HV_AVDD – HV_AVSS) / 36 101: Internal short to V_{COM} (HV_AVDD + HV_AVSS) / 2 (default) 110: Temperature sensor reading 111: Reserved
3:0	GAIN[3:0]	R/W	0h	**PGA Gain** These bits set the PGA gain setting. 0000: 0.125 V/V (default) 0001: 0.1875 V/V 0010: 0.25 V/V 0011: 0.5 V/V 0100: 1 V/V 0101: 2 V/V 0110: 4 V/V 0111: 8 V/V 1000: 16 V/V 1001: 32 V/V 1010: 64 V/V 1011: 128 V/V 1100-1111: reserved

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8.6.14 PGA Alarm (STATUS1) Register (address = 11h) [reset = xxh]

STATUS1 is shown in 图 50 and described in 表 44.

Return to Register Map Summary.

图 50. STATUS1 Register

7	6	5	4	3	2	1	0
PGA_ONL	PGA_ONH	PGA_OPL	PGA_OPH	PGA_INL	PGA_INH	PGA_IPL	PGA_IPH
R-xxh							

表 44. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGA_ONL	R	xh	**PGA Output Negative Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
6	PGA_ONH	R	xh	**PGA Output Negative High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
5	PGA_OPL	R	xh	**PGA Output Positive Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
4	PGA_OPH	R	xh	**PGA Output Positive High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
3	PGA_INL	R	xh	**PGA Input Negative Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
2	PGA_INH	R	xh	**PGA Input Negative High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
1	PGA_IPL	R	xh	**PGA Input Positive Low Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active
0	PGA_IPH	R	xh	**PGA Input Positive High Alarm** This bit is cleared on register read (clear-on-read). 0: No alarm 1: Alarm active

8.6.15 Status 2 (STATUS2) Register (address = 12h) [reset = 0xh]

STATUS2 is shown in 图 51 and described in 表 45.

Return to Register Map Summary.

图 51. STATUS2 Register

7	6	5	4	3	2	1	0
0	0	LOCK2	CRC2ERR	REV_ID2[3:0]			
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-xh			

表 45. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	0	R/W	0h	**Reserved** Always write 0.
5	LOCK2	R	0h	**PGA Register Block Lock2 Status** This bit indicates the lock status of the PGA section of the register block. Writes to the PGA register block are locked by the LOCK command and unlocked by the UNLOCK command. 0: PGA registers not locked (default) 1: PGA registers block locked See the STATUS0 register for the ADC section of the register block status.
4	CRC2ERR	R/W	0h	**CRC2 Error** Indicates a CRC2 error to the PGA section of the device. The CRC2 error is latched until cleared by the user. Write 0 to clear the error. 0: No error 1: CRC2 error
3:0	REV_ID2[3:0]	R	x	**Revision ID2** Revision ID 2 field. The revision ID1 and ID2 can change without notification.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Range

Linear PGA operation requires that the maximum and minimum input signal voltage not be exceeded. The following example shows how to verify the ADC input range specification. For this example, the input signal is ±10 V with 15% overrange. The negative input lead of the sensor is connected to AGND. The ADC gain is 0.1875 V/V using a 2.5-V reference voltage and ±15-V power supplies with 5% tolerance. The summary of conditions to verify the ADC range are:

- $V_{(AINx\_MAX)}$ = 11.5 V
- $V_{(AINx\_MIN)}$ = –11.5 V
- $V_{(AINCOM)}$= AGND
- HV_AVDD = 14.25 V
- HV_AVSS = –14.25 V
- Gain = 0.1875
- V_{REF} = 2.5 V

The evaluation of 公式 4 (case of gain < 1) results in:

–11.75 V < –11.5 V and 11.5 V < **11.75 V**

The inequality is satisfied, and as a result, the absolute input voltage is within the ADC input range requirement.

9.1.2 Input Overload

The input overvoltage precautions as described in the *ESD Diodes* section. If an overvoltage condition occurs on an unused channel, the overvoltage channel may crosstalk to the measurement channel. One solution, as shown in 图 52, is to externally clamp the inputs with low-forward voltage diodes. The external diodes shunt the overvoltage current flow around the ADC inputs. Be aware of the reverse leakage current that can cause measurement errors.

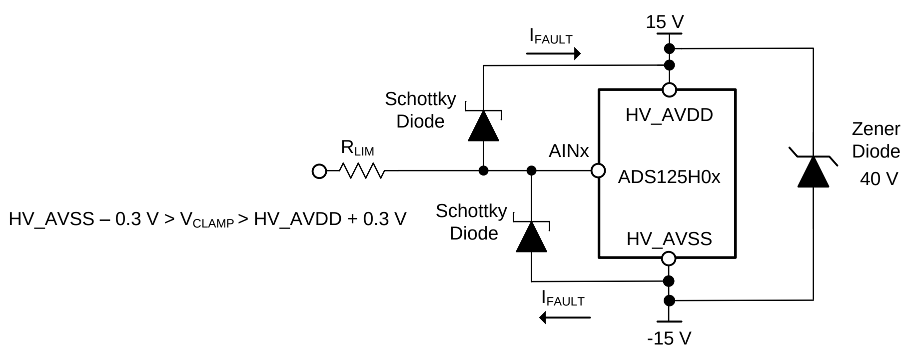

图 52. Optional Diode Clamps

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Application Information (接下页)

9.1.2.1 Input Signal Rate of Change (dV/dt)

High dV/dt conditions at the ADC input can lead to transient turn-on of the inverse-parallel connected, PGA input diodes. Turn-on of the PGA input diodes results in transient current flow from the PGA output to the analog input that can cause a disturbance in the measurement channel. For example, a high dV/dt voltage condition can be generated at the output of a signal multiplexer after a channel change that may result in the transient input current. Use an RC filter between the multiplexer output and the ADC input to limit the rate of voltage change (dV/dt).

9.1.3 Unused Inputs and Outputs

- **Analog Inputs**

  To minimize input current leakage, connect unused analog inputs to AGND when operating the device with bipolar supplies, or connect unused inputs to AVDD when operating the device with a unipolar supply. Connect unused reference inputs to AVDD (do not connect reference inputs to the HV power supplies).
- **Analog Outputs**

  A capacitor is not required for REFOUT if the internal reference or IDAC current sources are not used. Otherwise, connect a 10-µF capacitor between REFOUT and AGND.
- **Digital I/O**

  The ADC is operational using a subset of the digital I/O. Tie any unused digital inputs high or low (DVDD or DGND, as appropriate). Do not float (tri-state) the digital inputs or unpredictable operation can result. The following is a summary of digital I/O with optional connections:
  - **CLKIN:** Tie CLKIN to DGND to operate the ADC using the internal oscillator. The internal oscillator stops operation if CLKIN is connected to DVDD, resulting in loss of ADC functionality. Connect CLKIN to an external clock source to operate with an external clock.
  - **START:** Tie START low in order to control conversions entirely by command. Tie START high to free-run conversions when programmed to the continuous-conversion mode. Connect START to the host to control conversions directly by the pin.
  - **$\overline{\text{RESET}}$:** Tie $\overline{\text{RESET}}$ high if desired. An external RC reset on the $\overline{\text{RESET}}$ input pin is not necessary because the ADC resets at power on. The ADC can also be reset by the RESET command. Connect the $\overline{\text{RESET}}$ pin to the host to pin-control the ADC reset.
  - **$\overline{\text{DRDY}}$:** Data ready is also a function provided by the DOUT/$\overline{\text{DRDY}}$ pin. $\overline{\text{CS1}}$ must be low to use DOUT/$\overline{\text{DRDY}}$ to indicate when data are ready. Indication of data ready is also possible by polling the DRDY bit of the STATUS0 byte. For these methods, the host connection of $\overline{\text{DRDY}}$ is not necessary and can be left unconnected.
- **GPIO**

  Program unused GPIO as outputs (default setting). If any GPIOs are programmed as inputs, the GPIO must not be allowed to float (unconnected), otherwise AVDD power-supply leakage current may result.

9.2 Typical Application

图 53 illustrates an circuit example of a ±10-V analog input programmable logic controller (PLC) module using the ADS125H02. The ±10-V input signal from the field transmitter is first clamped by external ESD diodes to help protect the ADC inputs. The positive input signal is connected to the ADC input AIN1 through an RC filter to help filter RFI interference that can be picked up in noisy environments. The resistor also acts to limit input current in the event of an overvoltage event or during loss of module power when the signal is present. The negative input signal is connected to input AIN0, which is also connected to AGND.

The ADC is programmed to measure between the AIN1 and AIN0 inputs. This input configuration allows the input voltage to swing from 10 V to –10 V above and below AGND. In this example, the high-voltage ADC power-supply voltage is ±15 V. This ±15-V power-supply operation allows an input signal headroom of up to ±12.5 V. Using a reference voltage of 2.5 V and a gain of 0.1875 yields a nominal full-scale input range of ±13.3 V, except as limited by the input signal headroom.

Connect a 10-µF capacitor to the REFOUT pin as illustrated in 图 53 if the internal reference is used. Otherwise, apply an external reference to the REFP0 and REFN0 pins. A 100-kΩ resistor biases the differential reference voltage to 0 V in the event the reference fails. The resistor allows the ADC to detect a failed or missing reference voltage condition.

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Typical Application (接下页)

The excitation current sources and GPIOs are not used in this example and are left unconnected.

The ADC internal clock is activated by connecting the CLKIN input pin to ground. The serial interface and ADC control lines are connected to the host.

The zener diode clamps the high-voltage supply (HV_AVDD – HV_AVSS) to 40 V to provide protection to the ADC from possible overvoltage supply conditions.

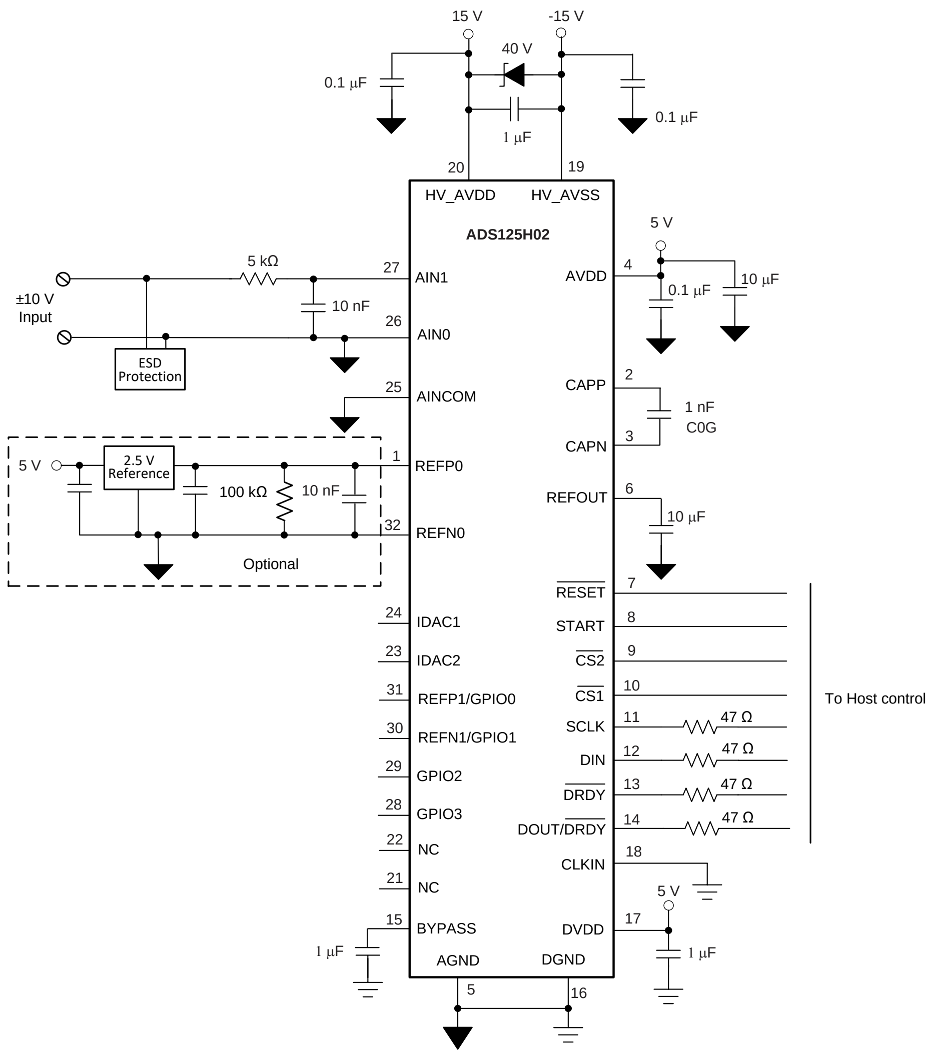


图 53. ±10-V Analog Input PLC Module

Typical Application (接下页)

9.2.1 Design Requirements

表 46 shows the design goals of the analog input PLC module. The ADC programmability allows tradeoffs of sample rate, conversion noise, and conversion latency. 表 47 shows the design parameters of the analog input PLC module.

表 46. Design Goals

DESIGN GOAL	VALUE
Accuracy (0°C to +85°C)	±0.1%
Basic resolution	>0.01%
Sample rate	>20000 SPS
Conversion latency	< 500 µs

表 47. Design Parameters

DESIGN PARAMETER	VALUE
Input signal range	±10 V
Overrange	±12 V
Input impedance	>100 MΩ
Overvoltage tolerance	±35 V

9.2.2 Detailed Design Procedure

A key consideration in the design of an analog input module is to evaluate the ADC parameters that affect accuracy for operation over the specified temperature range. 表 48 shows the key ADC parameters that effect accuracy. The values shown in 表 48 are after calibration at T_A = 25°C. As summarized by the total accuracy calculation, the target accuracy value of ±0.1% is met by the ADC. The maximum ADC parameter values, however, are estimates. Contact Texas Instruments to obtain final maximum values.

表 48. ADC Accuracy

PARAMETER	ACCURACY OVER 0°C TO +105°C
Offset drift	0.001%
Gain drift	0.03%
Reference drift	0.06%
Total accuracy	0.091%

表 1 describes the conversion noise performance data for a gain of 0.1875 expressed as an input-referred noise quantity. This table lists various tradeoffs among gain, sample rate, and digital filter order. Noise performance is optimized for a given design by considering the various parameters. In this example, the ADC configuration that yields the lowest noise while meeting the sample rate and settling time requirement is 25600 SPS and a gain of 0.1875 V/V (default sinc5 filter mode). This data rate yields a conversion latency value of 250 µs.

The input-referred noise under this ADC configuration is <100 µV RMS. The ADC noise yields a basic resolution of 100 µV / ±10 V = 0.001%.

The ADC gain is programmed to a gain of 0.1875 V/V, and when used with a 2.5-V reference this gain yields a nominal ADC input range of ±2.5 V / 0.1875 = ±13.3 V. However, in this example with ±15-V power supplies, the input signal headroom is limited to ±12.5 V (excluding the tolerance of the ±15-V power supplies). The input range satisfies the overrange design target requirement of ±12 V. The input impedance is typically 1 GΩ because the ADC input is a CMOS-input buffer.

ADVANCE INFORMATION

9.3 Initialization Setup

图 54 shows a general configuration and measurement procedure.

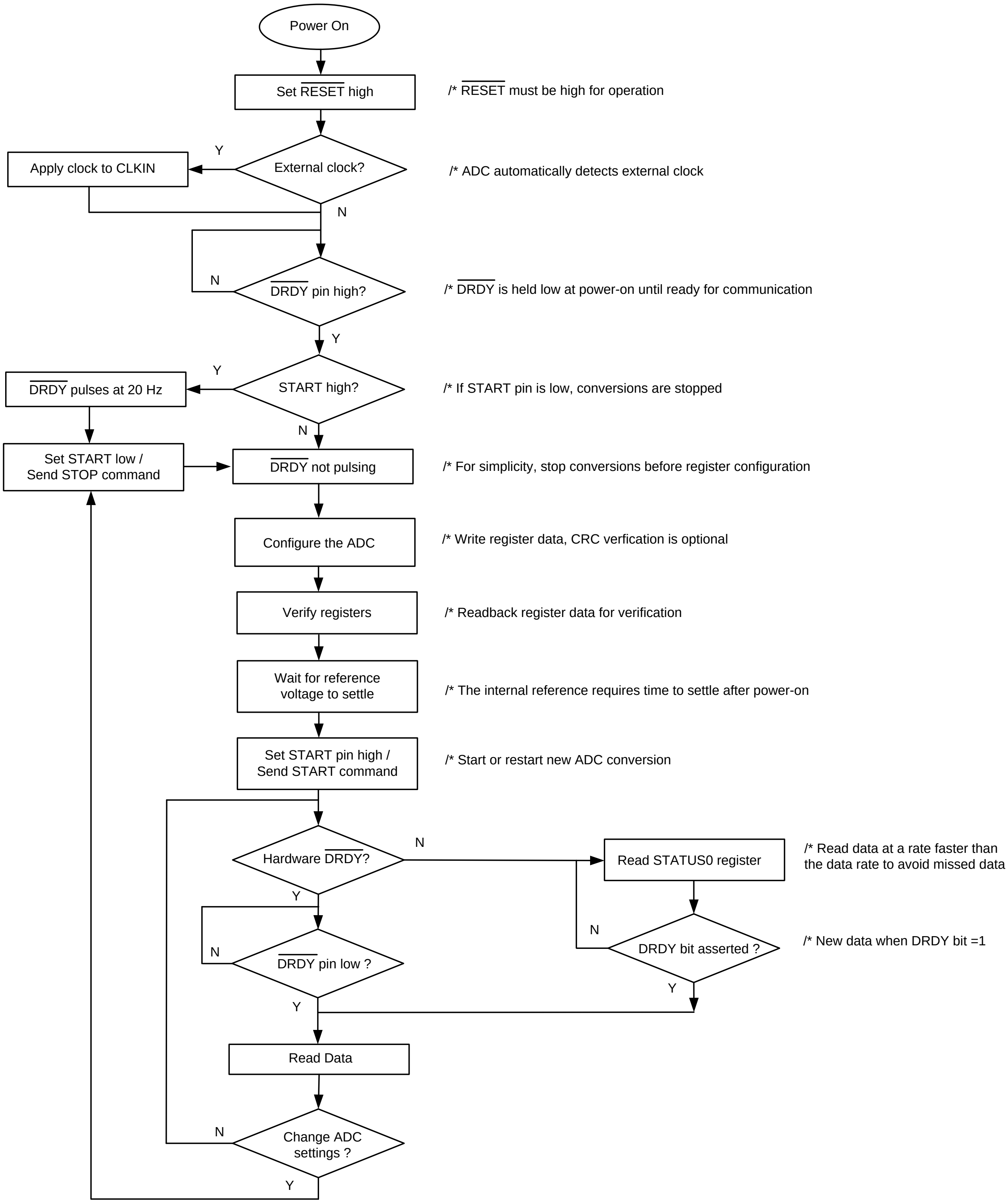


图 54. ADC Configuration and Measurement Procedure

ADVANCE INFORMATION

10 Power Supply Recommendations

The ADC requires three analog power supplies (high-voltage supplies HV_AVDD and HV_AVSS, and low-voltage AVDD) and a digital power supply (DVDD). The high-voltage analog power-supply configuration is either bipolar (±5 V to ±18 V) or unipolar (10 V to 36 V, with HV_AVSS connected to AGND). The AVDD power supply is 5 V. The digital supply range is 2.7 V to 5.25 V. AVDD and DVDD can be tied together as long as the 5-V power supply is free from excessive noise and glitches that can affect conversion results. An internal low-dropout regulator (LDO) powers the digital core via the DVDD power supply. DVDD is the digital I/O voltage. Keep in mind that the GPIO pins are at AVDD and AGND voltage potentials.

Voltage ripple produced by switch-mode power supplies can interfere with the ADC conversion accuracy. Use LDOs at the switching regulator output to reduce power-supply ripple.

AVDD inrush current is possible when the internal reference is enabled as a result of charging the 10-µF external capacitor at the reference output pin (REFOUT). Be sure the AVDD voltage transient droop is not below 4.5 V under this condition.

10.1 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve optimum performance. Power supplies must be decoupled close to the power supply. For the high voltage analog supply (HV_AVDD and HV_AVSS), place a 1-µF capacitor between the pins and place 0.1-µF capacitors from each supply to the ground plane. Connect 0.1-µF and 10-µF capacitors in parallel at AVDD to the ground plane. Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and equivalent series inductance (ESL) characteristics for power-supply decoupling purposes.

10.2 Analog Power-Supply Clamp

Circumstances must be evaluated when an input signal is present with the ADC, both powered and unpowered. When the input signal exceeds the power-supply voltage, the analog power-supply voltage can be backdriven with the input signal through a conduction path of the internal ESD diodes. Backdriving the ADC power supply can also occur when the power-supply is on. The backdrive fault-current path is illustrated in 图 52. Depending on how the power supply responds during a backdrive condition, the maximum-rated ADC supply voltage can be exceeded. The ADC voltage must not be exceeded at all times. One solution is to clamp the analog supply to a safe voltage using an external Zener diode.

10.3 Power-Supply Sequencing

The power supplies can be sequenced in any order, but do not allow analog or digital voltage inputs to exceed the respective analog or digital power-supplies without providing a limit to possible input fault currents.

10.4 5-V to ±15-V DC-DC Converter

图 55 illustrates a 5-V to ±15-V DC/DC converter for use with the ADS125H0x device. The DC/DC converter generates ±15-V supply voltages from 5-V power. The SN6505B is a push-pull transformer driver that drives the transformer primary from 5-V power. The typical switching frequency of the driver is 424 kHz, and when combined with the driver spread-spectrum clocking operation, reduces interference to the ADC as well as system-level EMI emissions. The output of the 2:1 step-up transformer is rectified in such a configuration that quadruples the 5-V primary voltage to the half-wave rectified and filtered secondary outputs of 20 V and –20 V. The rectified voltages are regulated by the TPS7A39 high-PSRR, dual positive and negative regulator to provide the ±15-V supply voltages.

ADVANCE INFORMATION

5-V to ±15-V DC-DC Converter (接下页)

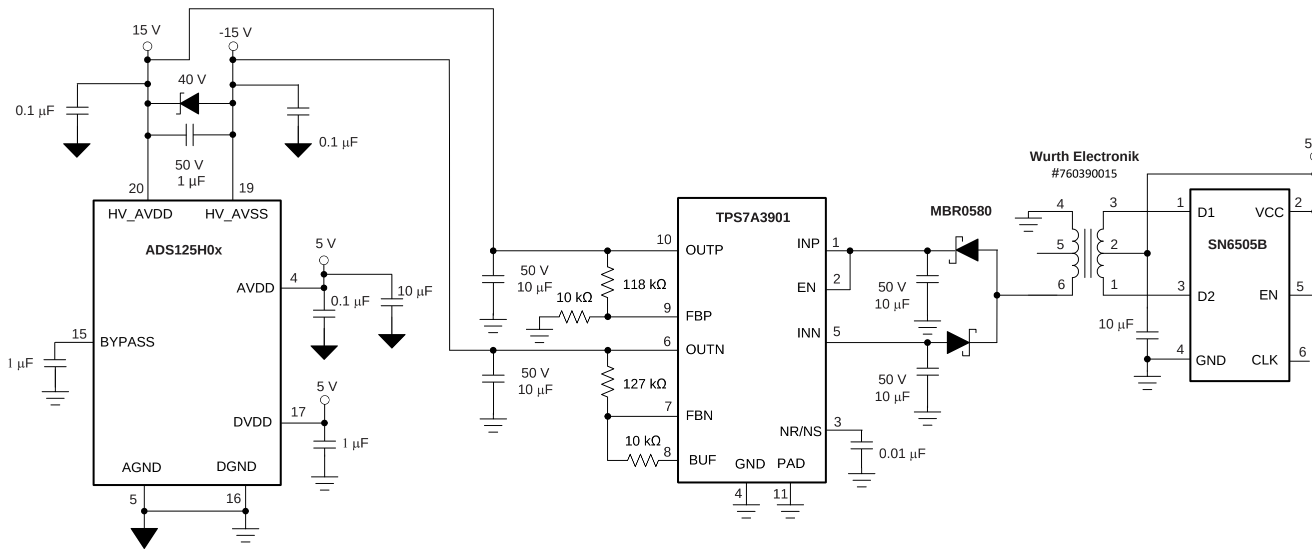


图 55. 5-V to ±15-V DC/DC Converter

11 Layout

11.1 Layout Guidelines

Good layout practices are crucial to realize the full performance of the ADC. Poor grounding can quickly degrade the noise performance. This section discusses layout recommendations that help provide the best results.

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a direct connection of the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital traces away from the CAPP and CAPN pins, away from the REFOUT pin, and away from all analog inputs and associated components in order to minimize interference.

Avoid long traces on DOUT/$\overline{\text{DRDY}}$, because high capacitance on this pin can lead to increased ADC noise levels. Use a series resistor or a buffer if long traces are used.

The internal reference output return shares the same pin as the AGND pin. To minimize coupling between the power supply and reference-return trace, route the traces separately; ideally, as a star connection to the AGND pin.

Use C0G capacitors on the analog inputs and for the CAPP to CAPN capacitor. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. The REFOUT pin requires a 10-µF capacitor and can be either ceramic or tantalum type. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

ADVANCE INFORMATION

11.2 Layout Example

图 56 shows an example layout of the ADS125H02, requiring a minimum of three PCB layers. The example circuit is shown with bipolar supply operation (±15 V) and using the internal reference. In this example, the inner layer is dedicated to the ground plane and the outer layers are used for signal and power traces. If a four-layer PCB is used, dedicate the additional inner layer as the power plane. In this example, the ADC is oriented in such a way to minimize crossover of the analog and digital signal traces.

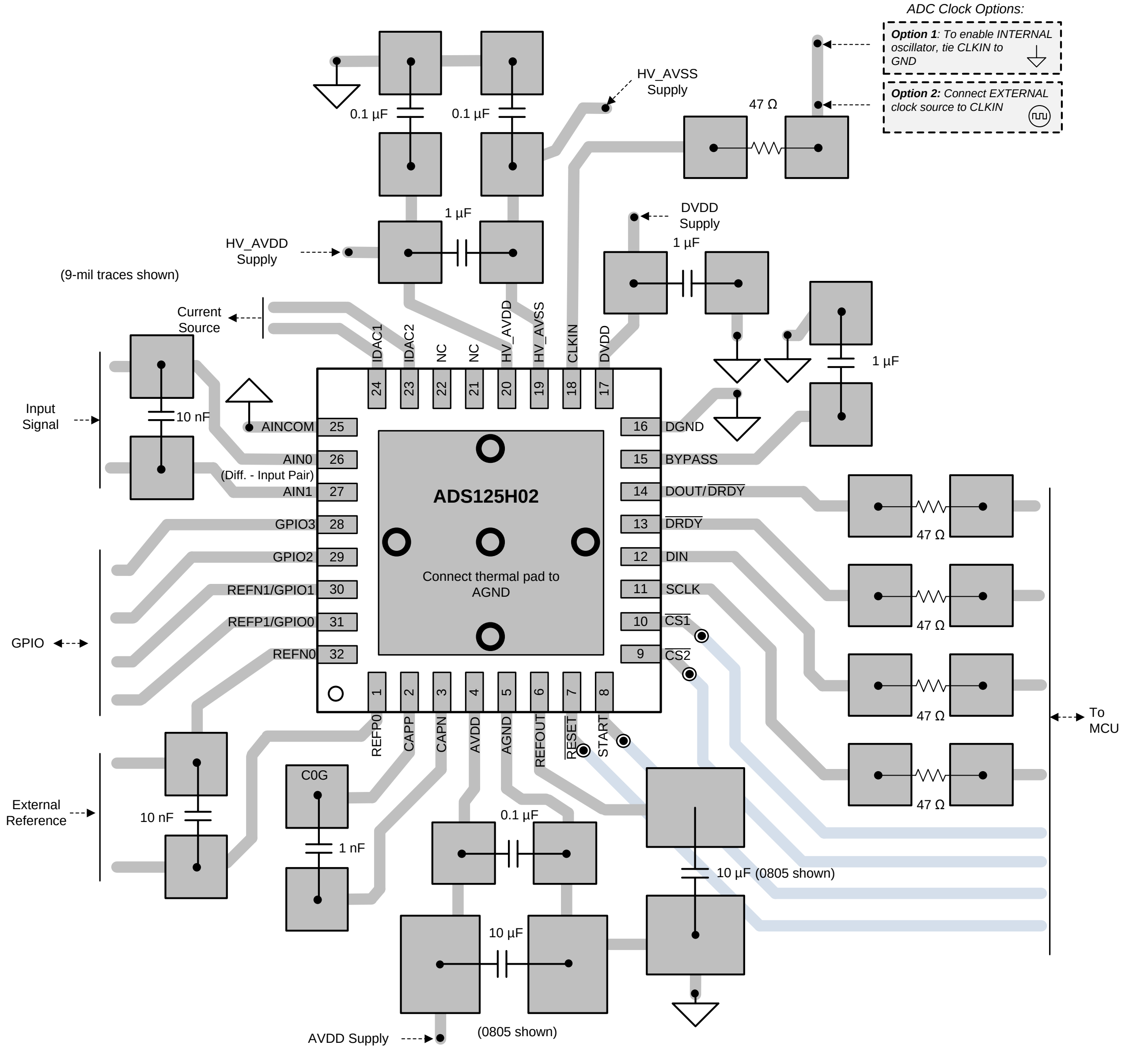


图 56. PCB Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《用于隔离电源的 SN6505x 低噪声 1A 变压器驱动器》*数据表
- 德州仪器 (TI)，*《TPS7A39 双路、150mA、宽输入电压正负 LDO 稳压器》*数据表

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **49.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
ADS125H01	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS125H02	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区*。**此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

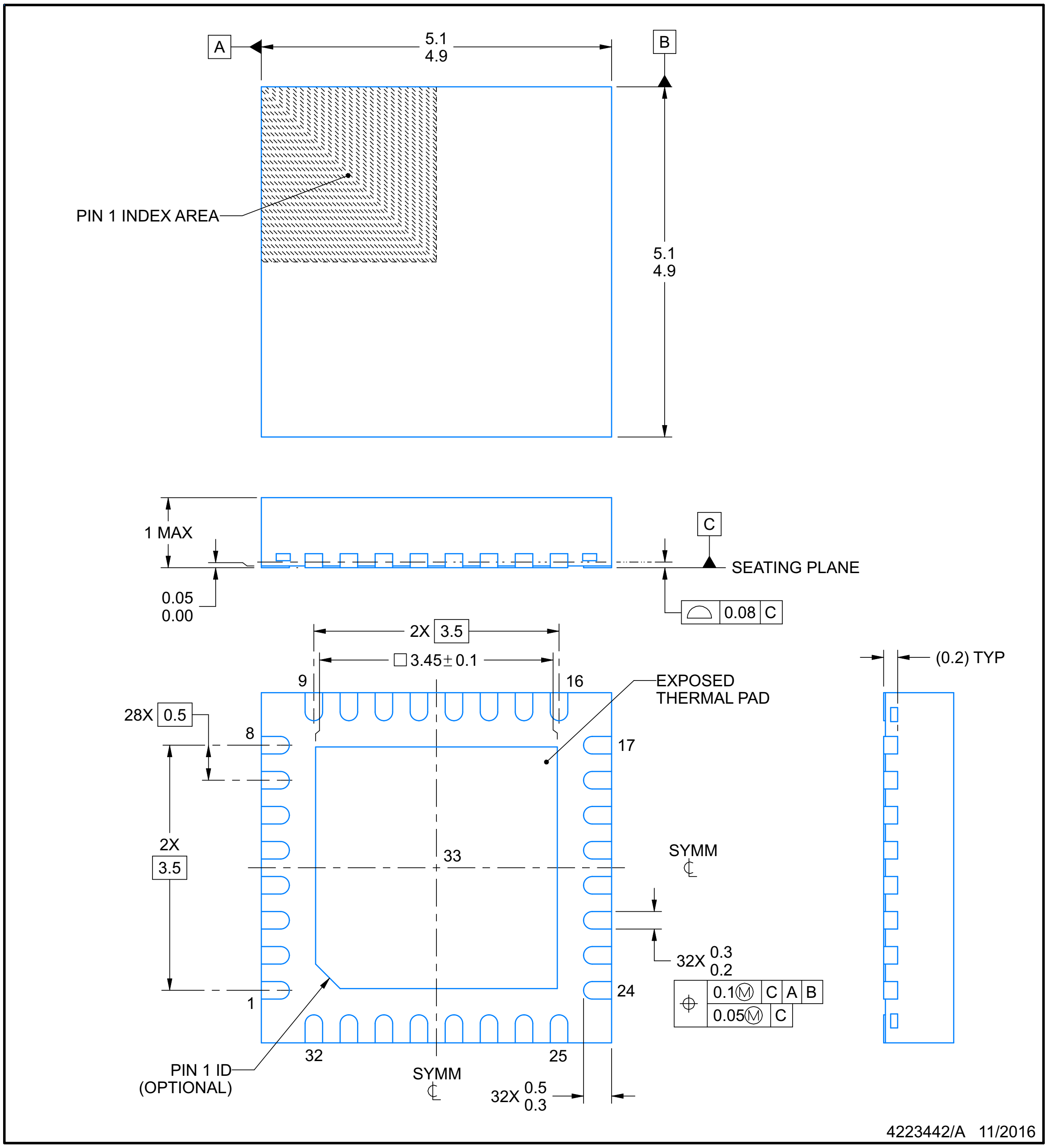
ADVANCE INFORMATION

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

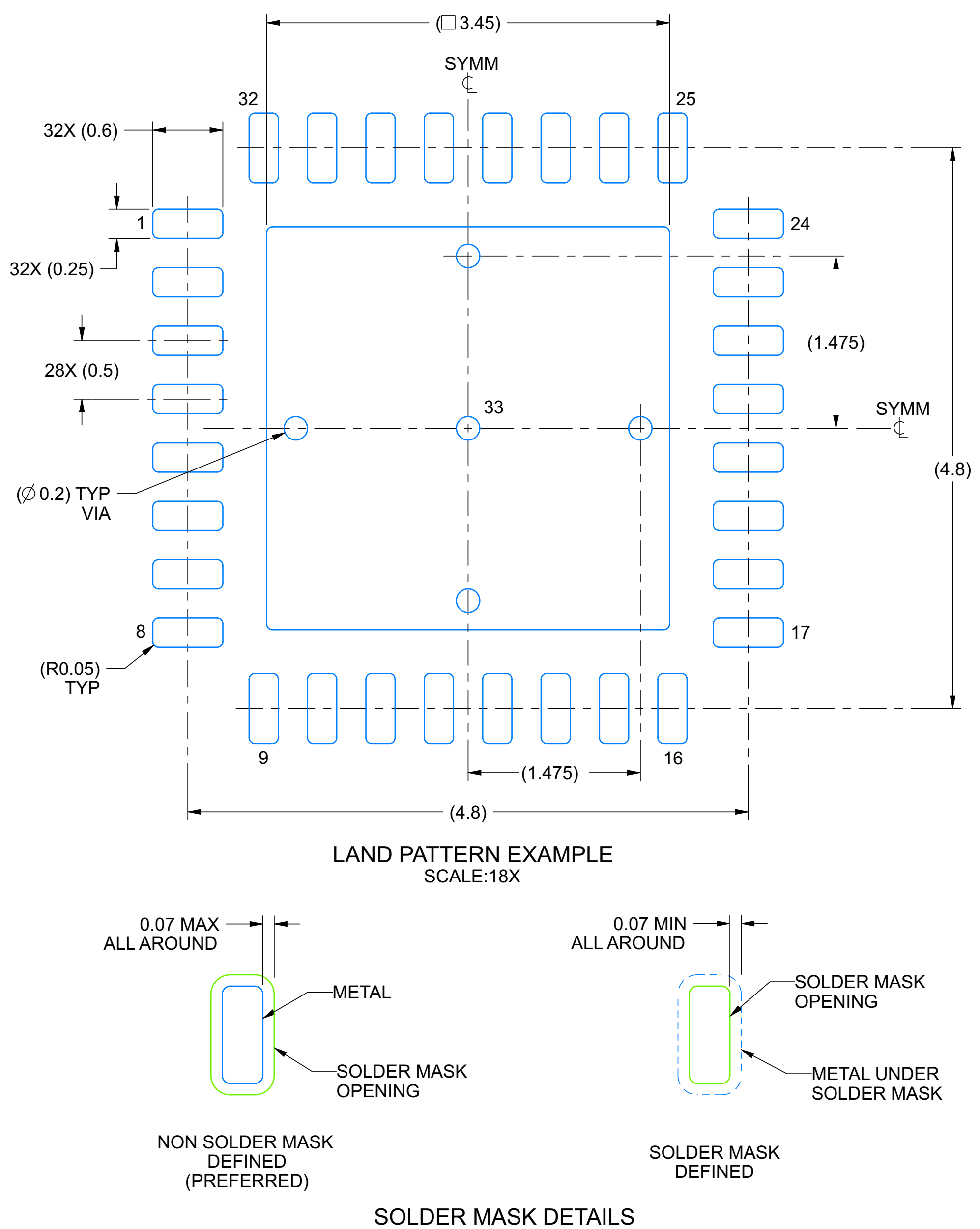
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

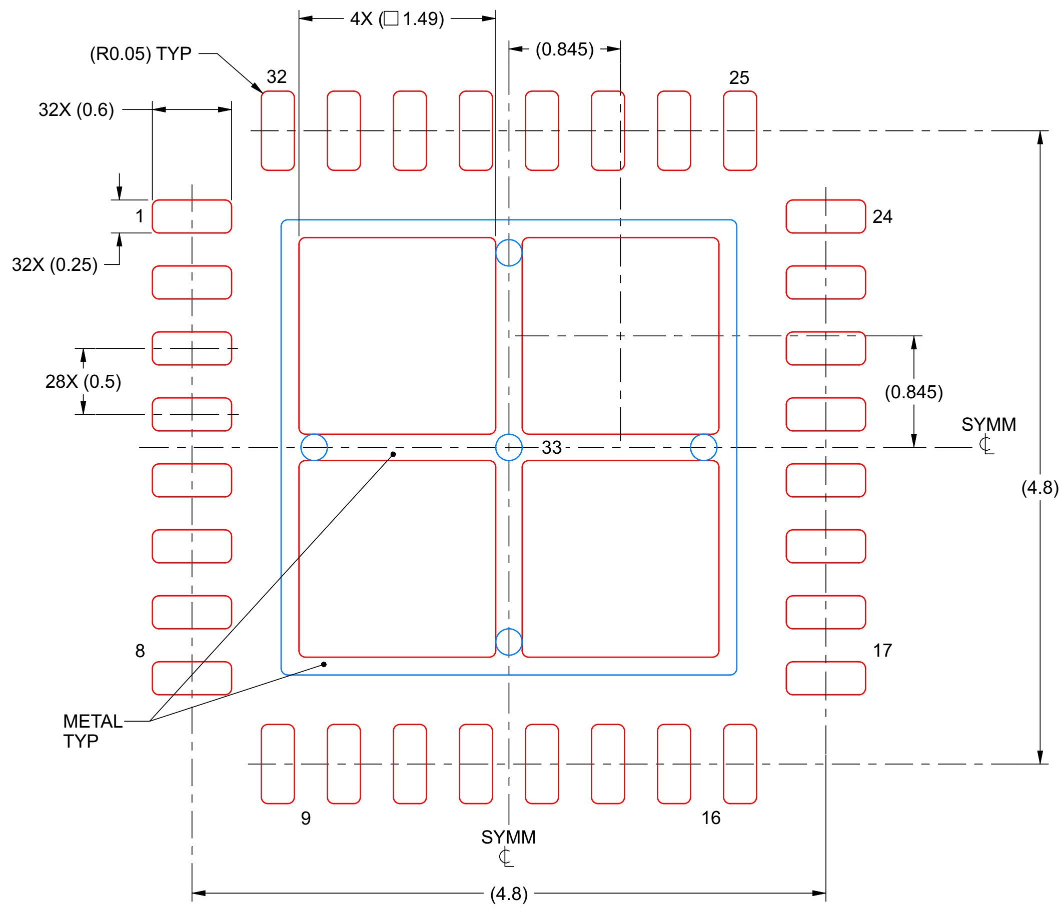
www.ti.com

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RHB0032E **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS125H02IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 125H02	Samples
ADS125H02IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 125H02	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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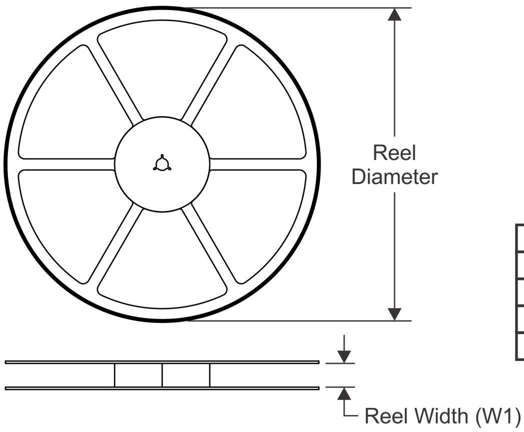
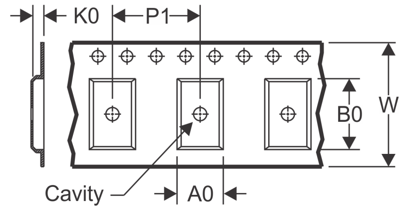
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

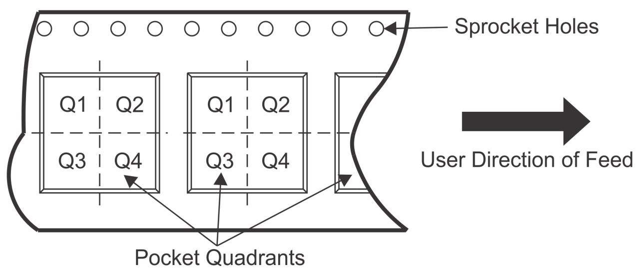


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

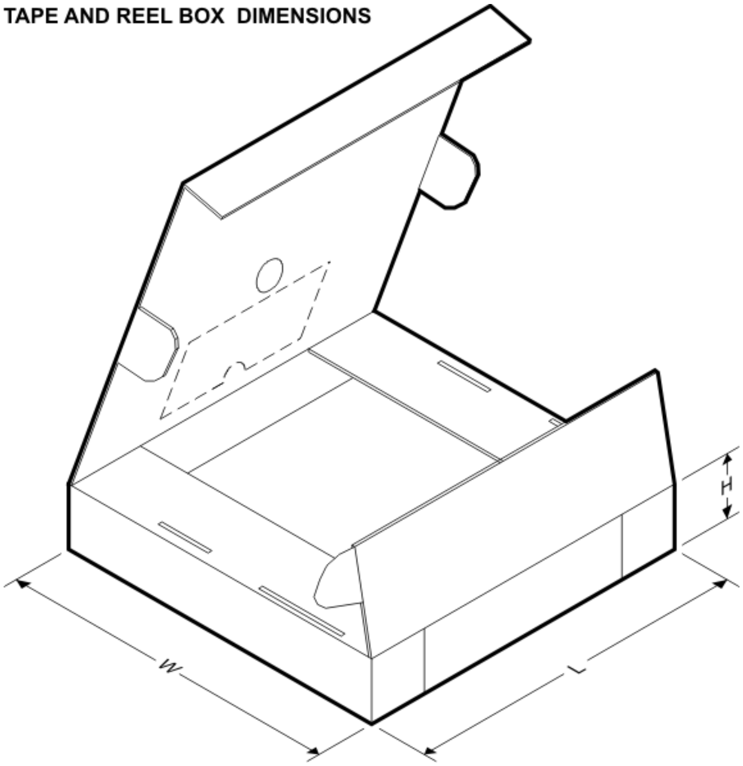
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS125H02IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS125H02IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS125H02IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS125H02IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

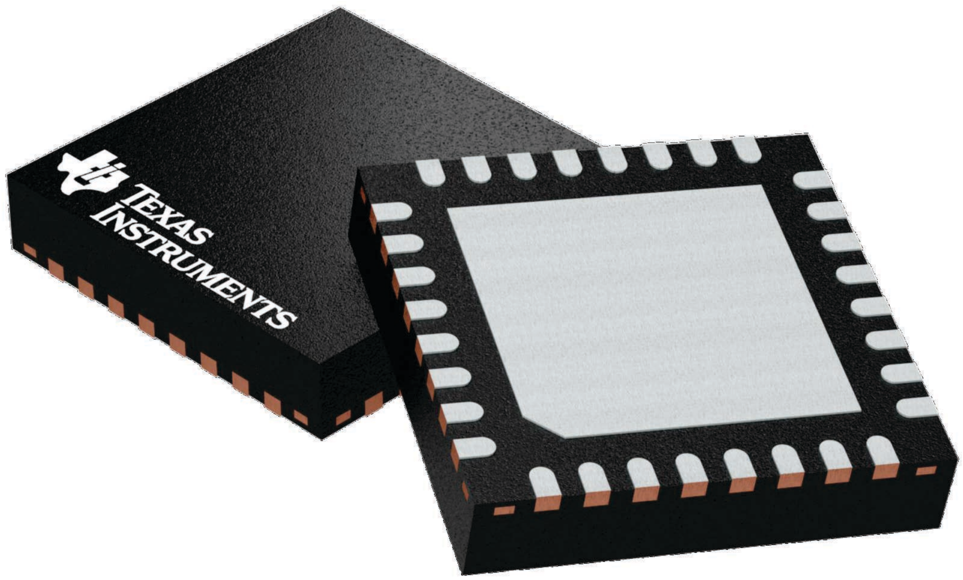
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

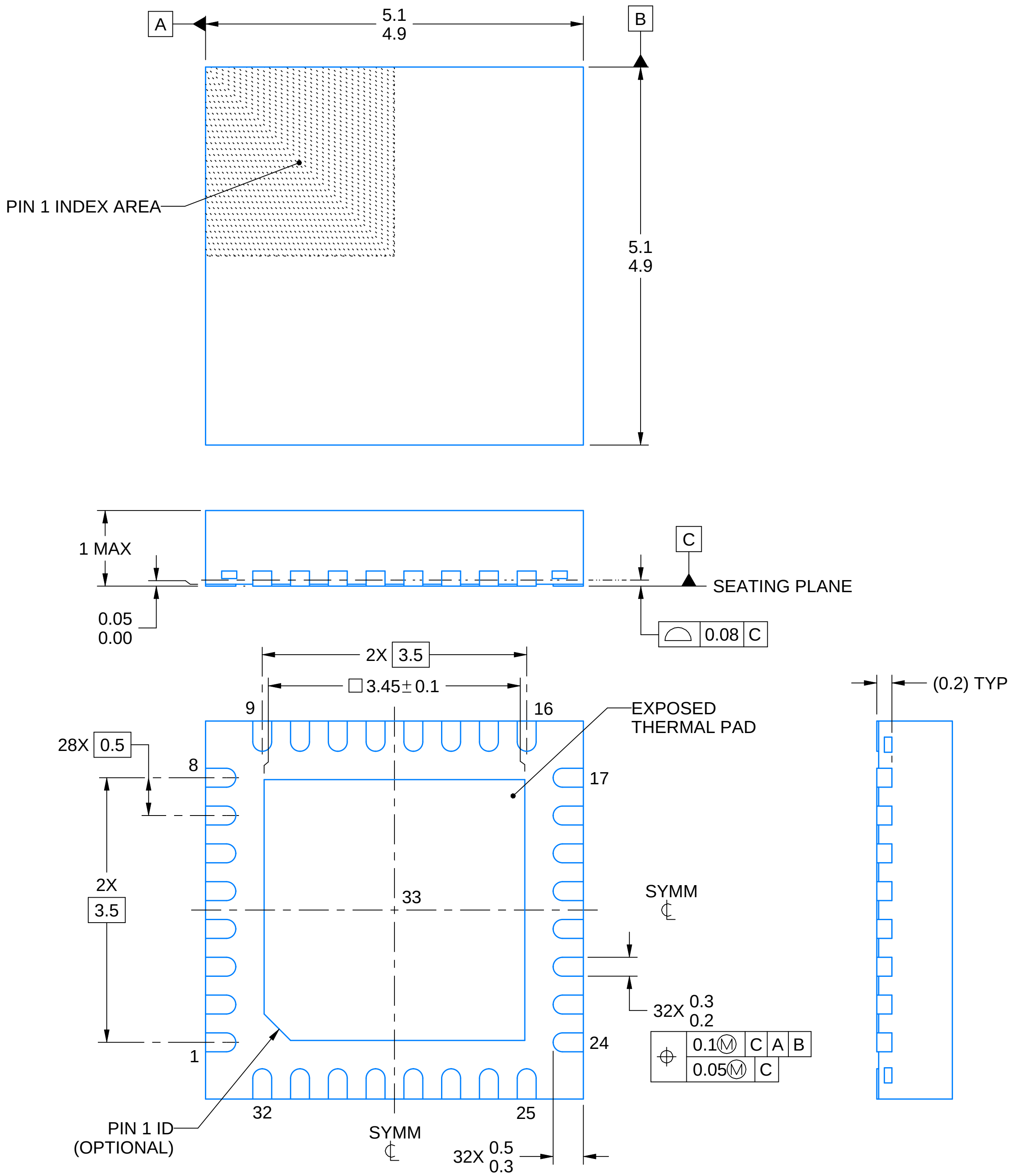
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

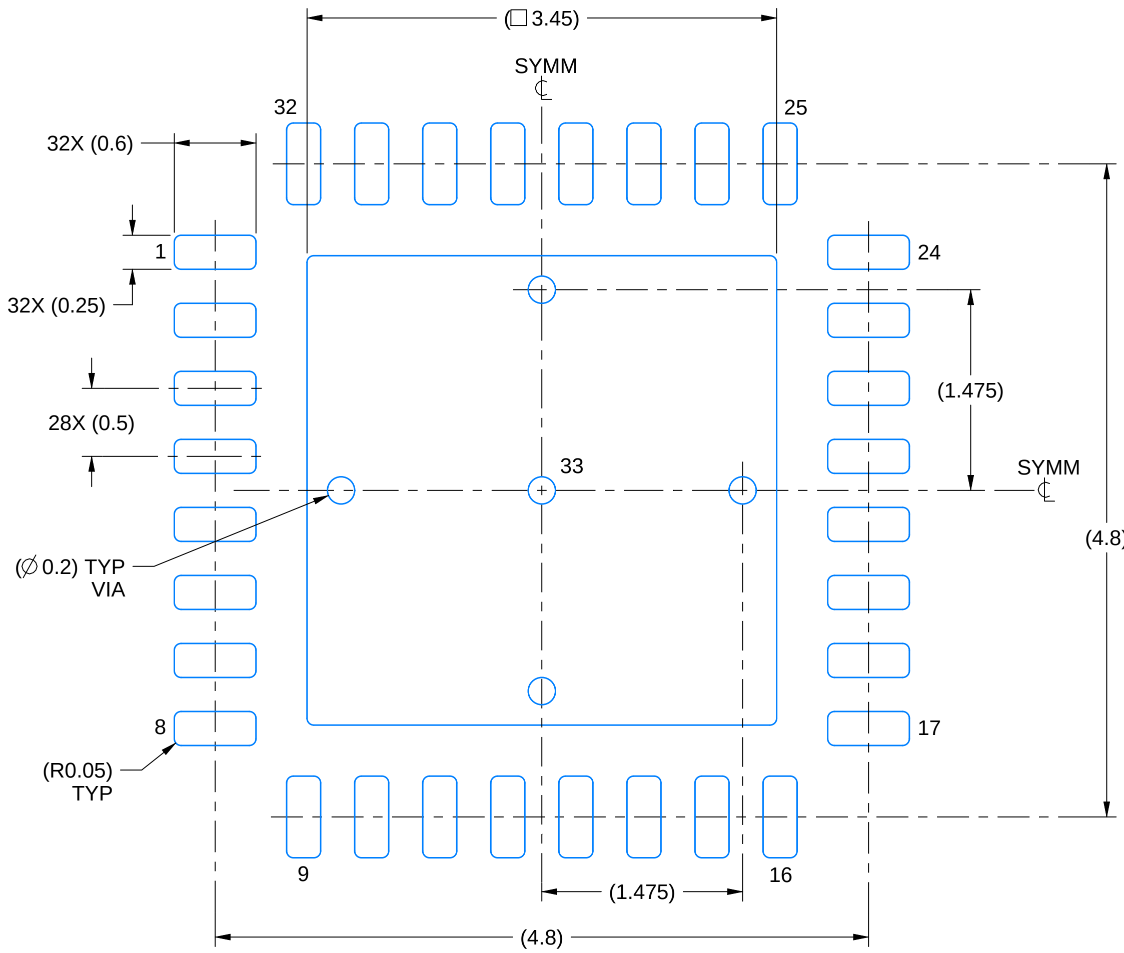
4224745/A



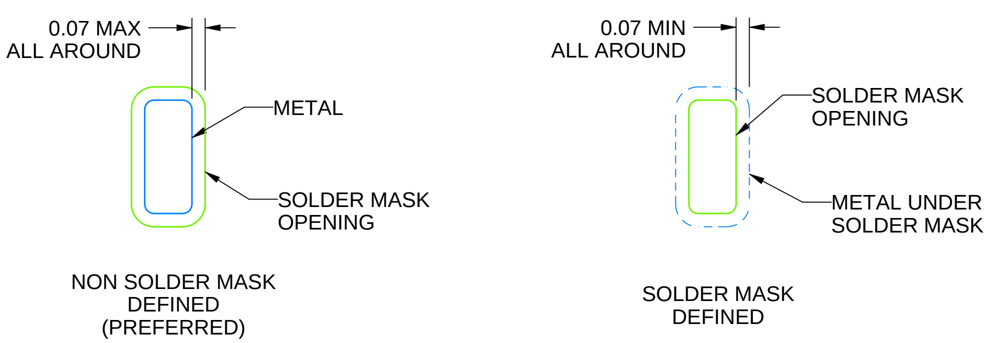
4223442/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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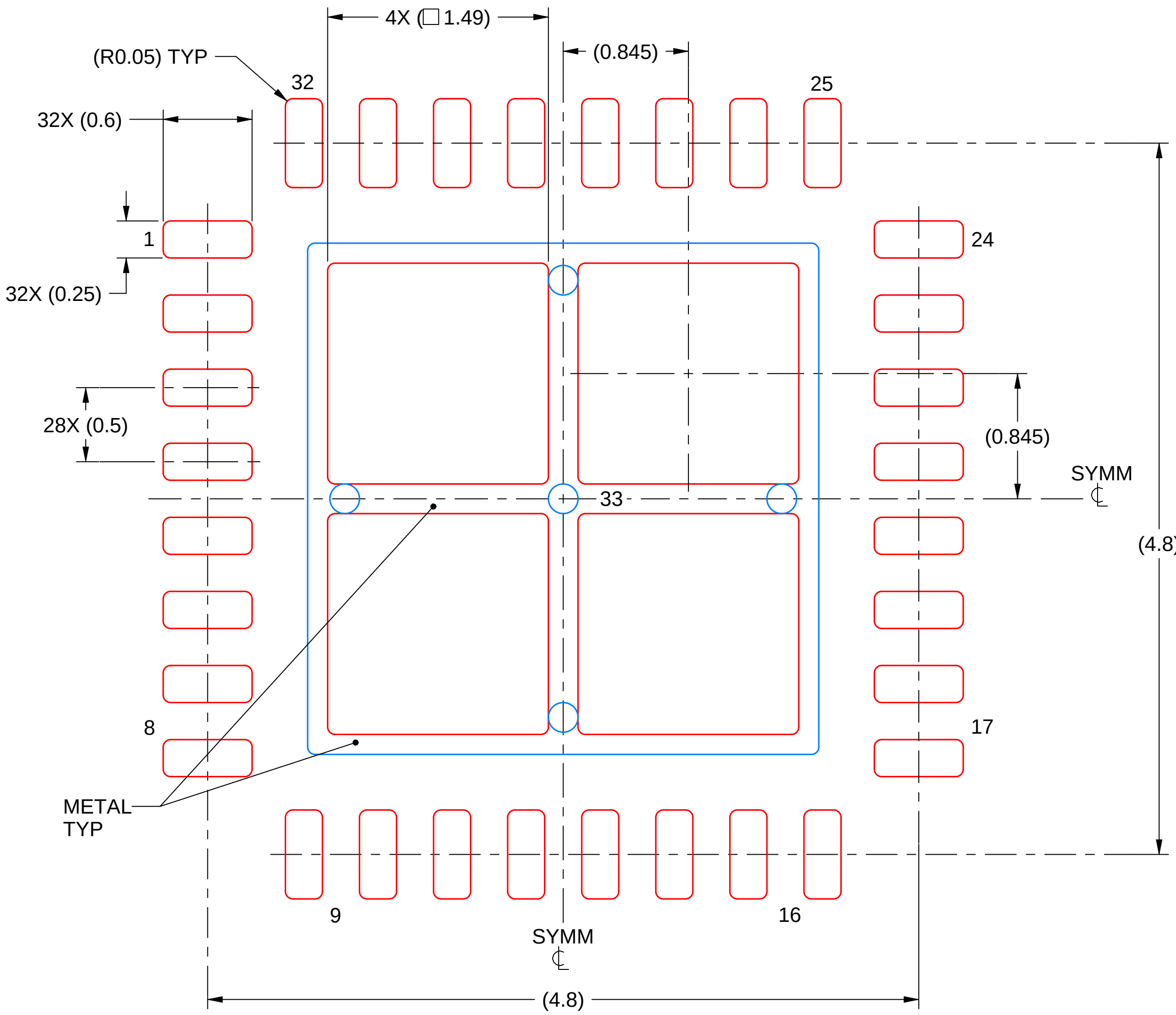
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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