LMH6550 Differential, High-Speed Operational Amplifier

1 Features

- 400 MHz −3-dB Bandwidth (V_{OUT} = 0.5 V_{PP})
- 90 MHz 0.1-dB Bandwidth
- 3000 V/µs Slew Rate
- 8 ns Settling Time to 0.1%
- −92/−103 dB HD2/HD3 at 5 MHz
- 10 ns Shutdown/Enable

2 Applications

- Differential AD Driver
- Video Over Twisted-Pair
- Differential Line Driver
- Single End to Differential Converter
- High-Speed Differential Signaling
- IF/RF Amplifier
- SAW Filter Buffer/Driver

3 Description

The LMH6550 device is a high-performance voltage feedback differential amplifier. The LMH6550 has the high speed and low distortion necessary for driving high-performance ADCs as well as the current handling capability to drive signals over balanced transmission lines like CAT 5 data cables. The LMH6550 can handle a wide range of video and data formats.

With external gain set resistors, the LMH6550 can be used at any desired gain. Gain flexibility coupled with high speed makes the LMH6550 suitable for use as an IF amplifier in high-performance communications equipment.

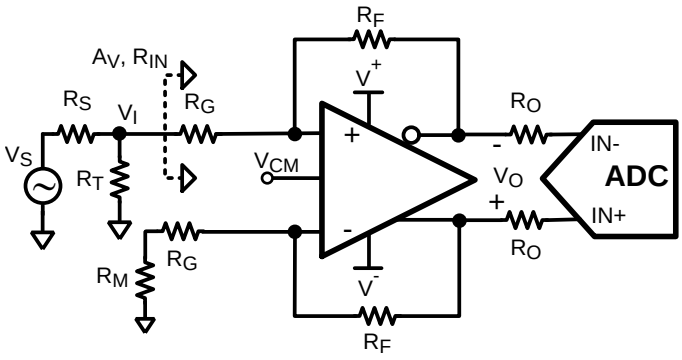
The LMH6550 is available in the space-saving SOIC and VSSOP packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6550	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Schematic



For $R_M << R_G$:

$$A_v = \frac{V_O}{V_I} \cong \frac{R_F}{R_G}$$

$$R_{IN} \cong \frac{2R_G(1+A_v)}{2+A_v}$$

Design Target :

1) Set $R_T = \dfrac{1}{\dfrac{1}{R_S} - \dfrac{1}{R_{IN}}}$

2) Set $R_M = R_T \,||\, R_S$

Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2013) to Revision I — **Page**

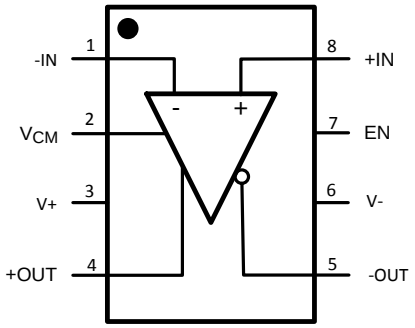
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision G (March 2013) to Revision H — **Page**

- Changed layout of National Data Sheet to TI format ... 22

6 Pin Configuration and Functions

D Package / DGK Package
8 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	7	I	Enable
-IN	1	I	Negative Input
+IN	8	I	Positive Input
-OUT	5	O	Negative Output
+OUT	4	O	Positive Output
V-	6	P	Negative Supply
V+	3	P	Positive Supply
VCM	2	I	Output Common-Mode Input

7 Specifications

7.1 Absolute Maximum Ratings (1)(2)(3)

	MIN	MAX	UNIT
Supply Voltage		13.2	V
Common-Mode Input Voltage		$\pm V_S$	V
Maximum Input Current (pins 1, 2, 7, 8)		30	mA
Maximum Output Current (pins 4, 5)		(4)	
Maximum Junction Temperature		150	°C
Storage Temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For Soldering Information, see Product Folder at www.ti.com and SNOA549.
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Machine model (MM)	±200	

(1) Human body model: 1.5 kΩ in series with 100 pF. Machine model: 0 Ω in series with 200 pF.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating Temperature	−40		85	°C
Total Supply Voltage	4.5		12	V

7.4 Thermal Information

THERMAL METRIC(1)		LMH6550		UNIT
		D	DGK	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	150	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} — T_A)/ \theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

7.5 Electrical Characteristics: ±5 V(1)

Single-ended in differential out, T_A = 25°C, V_S = ±5 V, V_{CM} = 0 V, $R_F = R_G$ = 365 Ω, R_L = 500 Ω; unless specified.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
AC PERFORMANCE (DIFFERENTIAL)							
SSBW	Small Signal −3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}			400		MHz
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}			380		MHz
	Large Signal −3 dB Bandwidth	V_{OUT} = 4 V_{PP}			320		MHz
	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}			90		MHz
	Slew Rate	4-V Step (4)		2000	3000		V/µs
	Rise/Fall Time	2-V Step			1		ns
	Settling Time	2-V Step, 0.1%			8		ns
V_{CM} PIN AC PERFORMANCE (COMMON-MODE FEEDBACK AMPLIFIER)							
	Common-Mode Small Signal Bandwidth	V_{CM} Bypass Capacitor Removed			210		MHz
	Slew Rate	V_{CM} Bypass Capacitor Removed			200		V/µs
DISTORTION AND NOISE RESPONSE							
HD2	2nd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L = 800 Ω			−92		dBc
		V_O = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω			−78		
		V_O = 2 V_{PP}, f = 70 MHz, R_L = 800 Ω			−59		
HD3	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L = 800 Ω			−103		dBc
		V_O = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω			−88		
		V_O = 2 V_{PP}, f = 70 MHz, R_L = 800 Ω			−50		
e_n	Input Referred Voltage Noise	f ≥ 1 MHz			6.0		nV/√Hz
i_n	Input Referred Noise Current	f ≥ 1 MHz			1.5		pA/√Hz
INPUT CHARACTERISTICS (DIFFERENTIAL)							
V_{OSD}	Input Offset Voltage	Differential Mode, V_{ID} = 0, V_{CM} = 0			1	±4	mV
			At extreme temperatures			±6	
	Input Offset Voltage Average Temperature Drift	(5)			1.6		µV/°C
I_{BI}	Input Bias Current	(6)		0	-8	−16	µA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Slew Rate is the average of the rising and falling edges.
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device.

Electrical Characteristics: ±5 V(1) (continued)

Single-ended in differential out, T_A = 25°C, V_S = ±5 V, V_{CM} = 0 V, R_F = R_G = 365 Ω, R_L = 500 Ω; unless specified.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
	Input Bias Current Average Temperature Drift	(5)			9.6		nA/°C
	Input Bias Difference	Difference in Bias Currents Between the Two Inputs			0.3		µA
CMRR	Common-Mode Rejection Ratio	DC, V_{CM} = 0 V, V_{ID} = 0 V		72	82		dBc
R_{IN}	Input Resistance	Differential			5		MΩ
C_{IN}	Input Capacitance	Differential			1		pF
CMVR	Input Common-Mode Voltage Range	CMRR > 53 dB		+3.1 −4.6	+3.2 −4.7		V
V_{CM} PIN INPUT CHARACTERISTICS (COMMON-MODE FEEDBACK AMPLIFIER)							
V_{OSC}	Input Offset Voltage	Common Mode, V_{ID} = 0			1	±5	mV
			At extreme temperatures			±8	
	Input Offset Voltage Average Temperature Drift	(5)			25		µV/°C
	Input Bias Current	(6)			−2		µA
	V_{CM} CMRR	V_{ID} = 0 V, 1-V Step on V_{CM} Pin, Measure V_{OD}		70	75		dB
	Input Resistance				25		kΩ
	Common-Mode Gain	$\Delta V_{O,CM}/\Delta V_{CM}$		0.995	0.997	1.005	V/V
OUTPUT PERFORMANCE							
	Output Voltage Swing	Peak to Peak, Differential		7.38	7.8		V
			At extreme temperatures	7.18			
	Output Common-Mode Voltage Range	V_{ID} = 0 V,		±3.69	±3.8		V
I_{OUT}	Linear Output Current	V_{OUT} = 0 V		±63	±75		mA
I_{SC}	Short Circuit Current	Output Shorted to Ground V_{IN} = 3 V Single-Ended (7)			±200		mA
	Output Balance Error	ΔV_{OUT} Common Mode /ΔV_{OUT} Differential, V_{OUT} = 1 V_{PP} Differential, f = 10 MHz			−68		dB
MISCELLANEOUS PERFORMANCE							
	Enable Voltage Threshold	Pin 7		2.0			V
	Disable Voltage Threshold	Pin 7				1.5	V
	Enable Pin Current	V_{EN} =0 V (6)			-250		µA
		V_{EN} =4 V (6)			55		
	Enable/Disable Time				10		ns
A_{VOL}	Open Loop Gain	Differential			70		dB
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1 V		74	90		dB
	Supply Current	R_L = ∞		18	20	24	mA
			At extreme temperatures			27	
	Disabled Supply Current				1	1.2	mA

(7) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

7.6 Electrical Characteristics: 5 V(1)

Single-ended in differential out, T_A = 25°C, A_V = +1, V_S = 5 V, V_{CM} = 2.5 V, R_F = R_G = 365 Ω, R_L = 500 Ω; unless specified.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
SSBW	Small Signal −3 dB Bandwidth	R_L = 500 Ω, V_{OUT} = 0.5 V_{PP}			350		MHz
LSBW	Large Signal −3 dB Bandwidth	R_L = 500 Ω, V_{OUT} = 2 V_{PP}			330		MHz
	0.1 dB Bandwidth				60		MHz
	Slew Rate	2-V Step (4)			1500		V/µs
	Rise/Fall Time, 10% to 90%	1-V Step			1		ns
	Settling Time	1-V Step, 0.05%			12		ns
V_{CM} PIN AC PERFORMANCE (COMMON-MODE FEEDBACK AMPLIFIER)							
	Common-Mode Small Signal Bandwidth				185		MHz
	Slew Rate				180		V/µs
DISTORTION AND NOISE RESPONSE							
HD2	2nd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L = 800 Ω			−89		dBc
		V_O = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω			−88		
HD3	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L = 800 Ω			−85		dBc
		V_O = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω			−70		
e_n	Input Referred Noise Voltage	f ≥ 1 MHz			6.0		nV/√Hz
i_n	Input Referred Noise Current	f ≥ 1 MHz			1.5		pA/√Hz
INPUT CHARACTERISTICS (DIFFERENTIAL)							
V_{OSD}	Input Offset Voltage	Differential Mode, V_{ID} = 0, V_{CM} = 0			1	±4	mV
			At extreme temperatures			±6	
	Input Offset Voltage Average Temperature Drift	(5)			1.6		µV/°C
I_{BIAS}	Input Bias Current	(6)		0	−8	−16	µA
	Input Bias Current Average Temperature Drift	(5)			9.5		nA/°C
	Input Bias Current Difference	Difference in Bias Currents Between the Two Inputs			0.3		µA
CMRR	Common-Mode Rejection Ratio	DC, V_{ID} = 0 V		70	80		dBc
	Input Resistance	Differential			5		MΩ
	Input Capacitance	Differential			1		pF
V_{ICM}	Input Common-Mode Range	CMRR > 53 dB		+3.1 +0.4	+3.2 +0.3		
V_{CM} PIN INPUT CHARACTERISTICS (COMMON-MODE FEEDBACK AMPLIFIER)							
	Input Offset Voltage	Common-Mode, V_{ID} = 0			1	±5	mV
			At extreme temperatures			±8	
	Input Offset Voltage Average Temperature Drift				18.6		µV/°C
	Input Bias Current				3		µA
	V_{CM} CMRR	V_{ID} = 0, 1-V Step on V_{CM} Pin, Measure V_{OD}		70	75		dB
	Input Resistance	V_{CM} Pin to Ground			25		kΩ

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Slew Rate is the average of the rising and falling edges.
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device.

Electrical Characteristics: 5 V(1) (continued)

Single-ended in differential out, T_A = 25°C, A_V = +1, V_S = 5 V, V_{CM} = 2.5 V, R_F = R_G = 365 Ω, R_L = 500 Ω; unless specified.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
	Common-Mode Gain	$\Delta V_{O,CM}/\Delta V_{CM}$			0.991		V/V
OUTPUT PERFORMANCE							
V_{OUT}	Output Voltage Swing	Peak to Peak, Differential, V_S = ±2.5 V, V_{CM} = 0 V		2.4	2.8		V
I_{OUT}	Linear Output Current	V_{OUT} = 0-V Differential		±54	±70		mA
I_{SC}	Output Short Circuit Current	Output Shorted to Ground V_{IN} = 3 V Single-Ended (7)			250		mA
CMVR	Common-Mode Voltage Range	V_{ID} = 0, V_{CM} Pin = 1.2 V and 3.8 V		3.72 1.23	3.8 1.2		V
	Output Balance Error	ΔV_{OUT} Common Mode /ΔV_{OUT} DIfferential, V_{OUT} = 1 V_{PP} Differential, f = 10 MHz			−65		dB
MISCELLANEOUS PERFORMANCE							
	Enable Voltage Threshold	Pin 7		2.0			V
	Disable Voltage Threshold	Pin 7				1.5	V
	Enable Pin Current	V_{EN} =0 V (6)			-250		µA
		V_{EN} =4 V (6)			55		
	Enable/Disable Time				10		ns
	Open Loop Gain	DC, Differential			70		dB
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±0.5 V		72	77		dB
I_S	Supply Current	R_L = ∞		16.5	19	23.5	mA
			At extreme temperatures			26.5	
I_{SD}	Disabled Supply Current				1	1.2	mA

(7) The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

7.7 Typical Characteristics

(T_A = 25°C, V_S = ±5 V, R_L = 500 Ω, R_F = R_G = 365 Ω; unless specified).

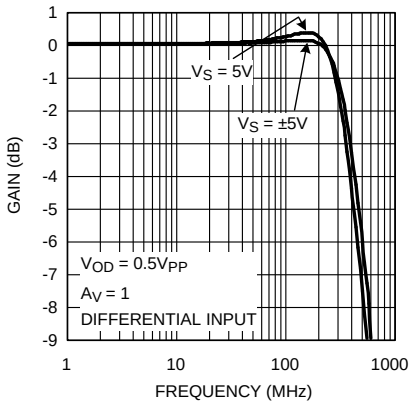


Figure 1. Frequency Response vs Supply Voltage

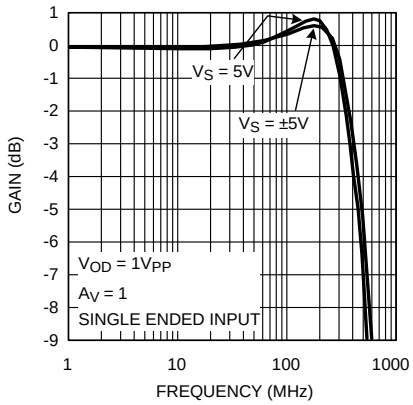


Figure 2. Frequency Response

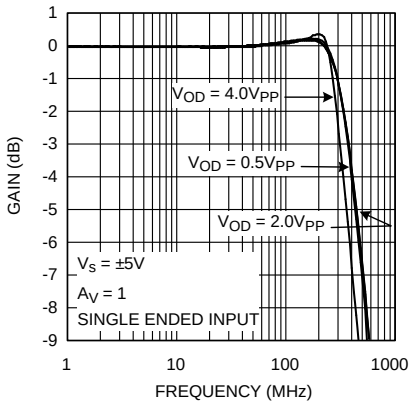


Figure 3. Frequency Response vs V_{OUT}

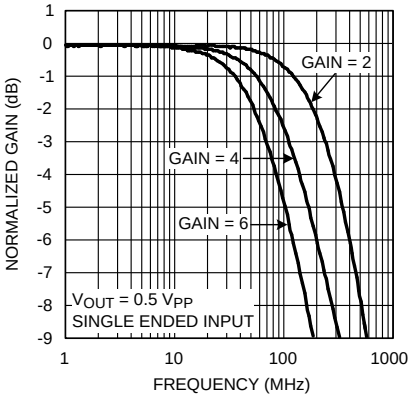


Figure 4. Frequency Response vs Gain

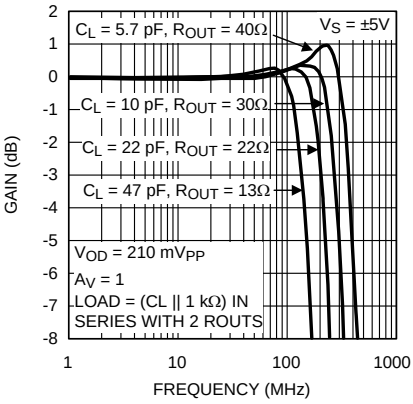


Figure 5. Frequency Response vs Capacitive Load

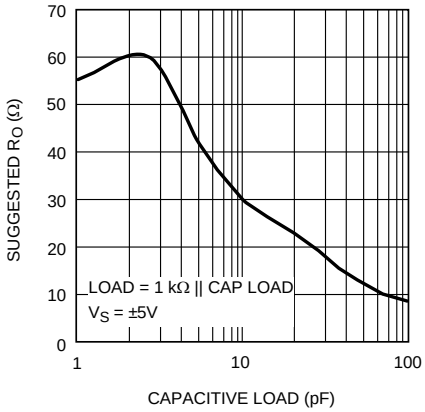


Figure 6. Suggested R_{OUT} vs Cap Load

Typical Characteristics (continued)

(T_A = 25°C, V_S = ±5 V, R_L = 500 Ω, R_F = R_G = 365 Ω; unless specified).

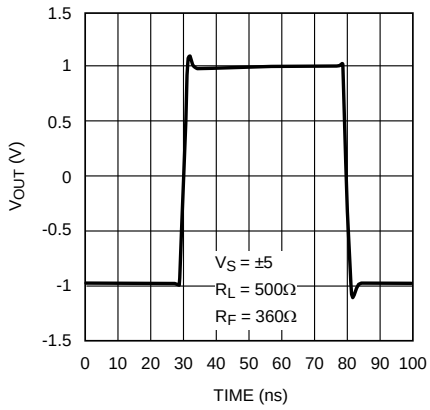


Figure 7. 2 V_{PP} Pulse Response Single-Ended Input

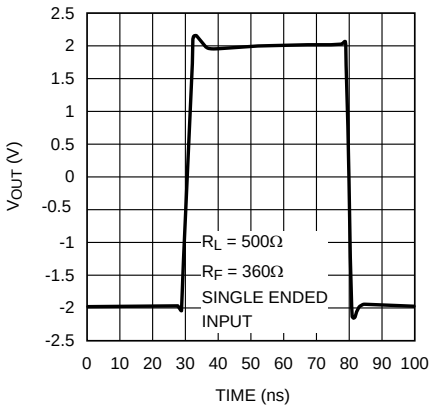


Figure 8. Large Signal Pulse Response

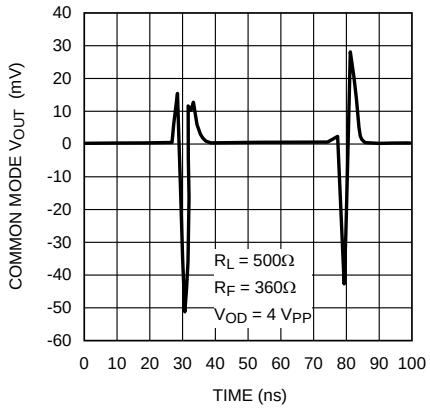


Figure 9. Output Common-Mode Pulse Response

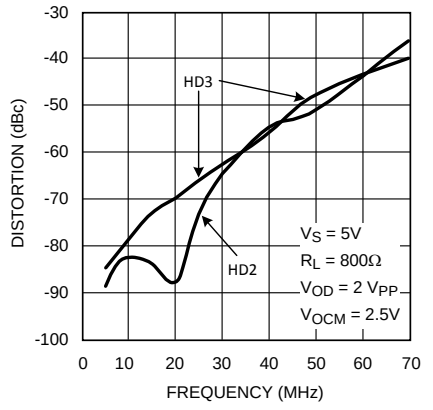


Figure 10. Distortion vs Frequency Single-Ended Input

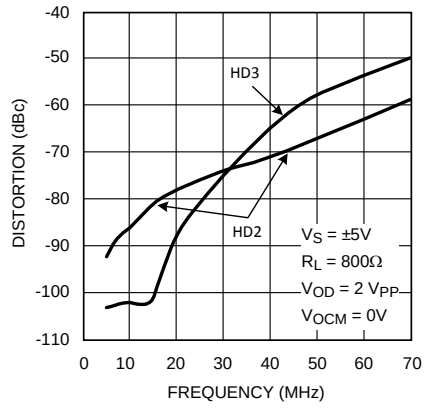


Figure 11. Distortion vs Frequency Single-Ended Input

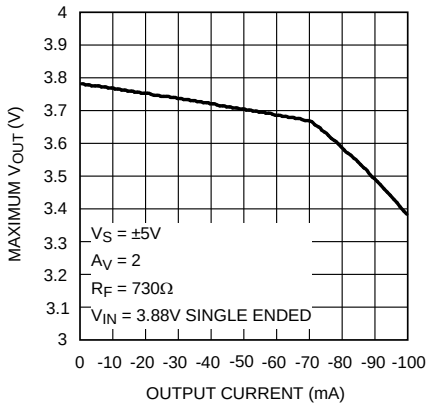


Figure 12. Maximum V_{OUT} vs I_{OUT}

Typical Characteristics (continued)

(T_A = 25°C, V_S = ±5 V, R_L = 500 Ω, R_F = R_G = 365 Ω; unless specified).

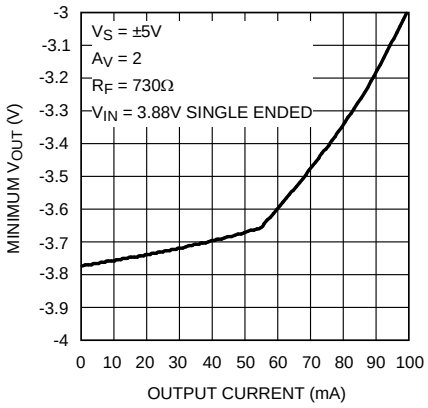


Figure 13. Minimum V_{OUT} vs I_{OUT}

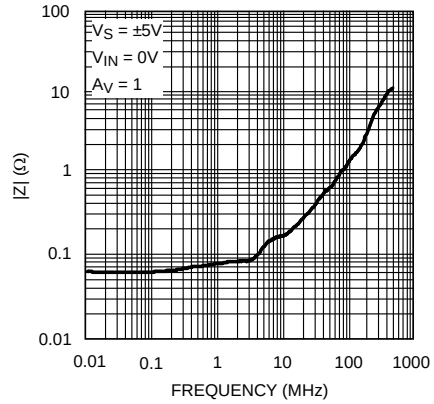


Figure 14. Closed-Loop Output Impedance

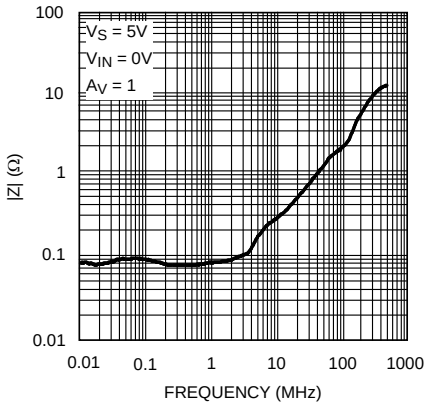


Figure 15. Closed-Loop Output Impedance

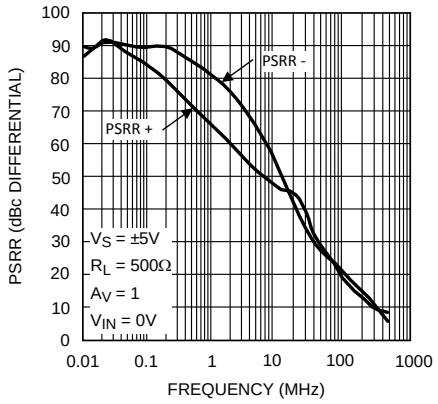


Figure 16. PSRR

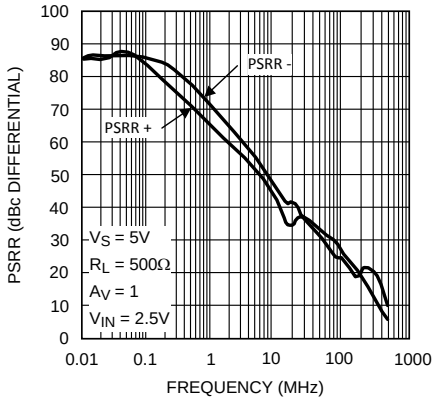


Figure 17. PSRR

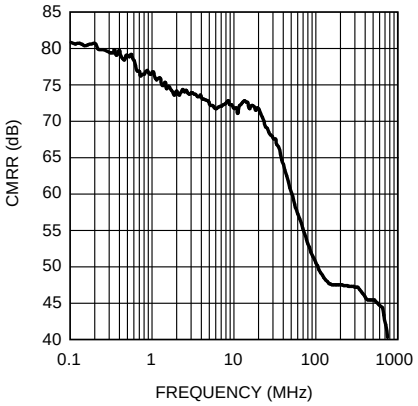


Figure 18. CMRR

Typical Characteristics (continued)

(T_A = 25°C, V_S = ±5 V, R_L = 500 Ω, R_F = R_G = 365 Ω; unless specified).

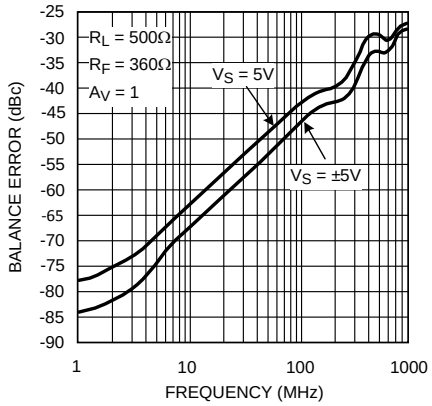


Figure 19. Balance Error

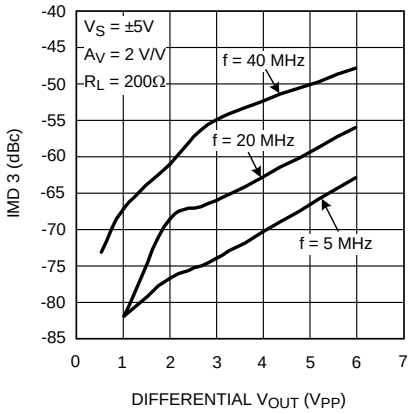


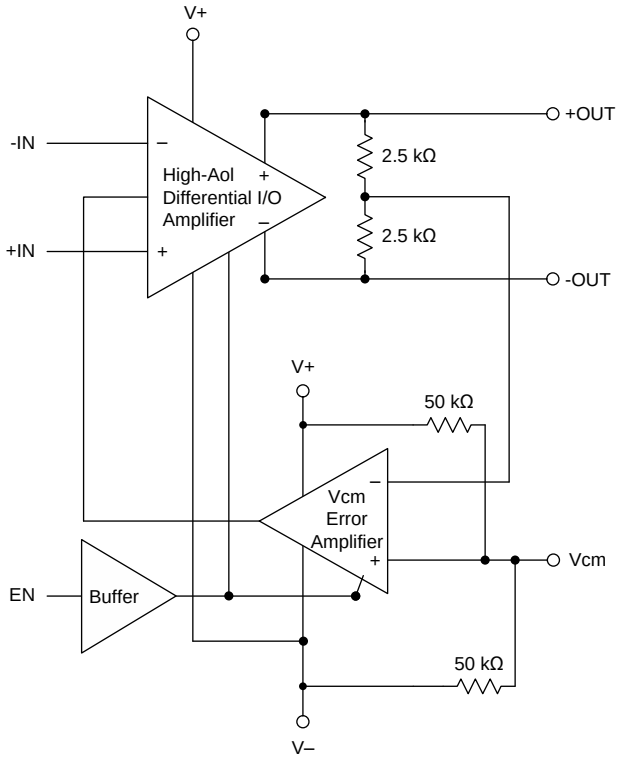
Figure 20. Third-Order Intermodulation Products vs V_{OUT}

8 Detailed Description

8.1 Overview

The LMH6550 is a fully differential amplifier designed to provide low distortion amplification to wide bandwidth differential signals. The LMH6550, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the V+ and V− signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths. The third channel is the common-mode feedback circuit. This is the circuit that sets the output common mode as well as driving the V+ and V− outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common-mode feedback circuit allows single-ended to differential operation.

8.2 Functional Block Diagram



8.3 Feature Description

The LMH6550 combines a core differential I/O, high-gain block with an output common-mode sense that is compared to a reference voltage and then fed back into the main amplifier block to control the average output to that reference. The differential I/O block is a classic, high open-loop gain stage. The high-speed differential outputs include an internal averaging resistor network to sense the output common-mode voltage. This voltage is compared by a separate Vcm error amplifier to the voltage on the Vocm pin. If floated, this reference is at half the total supply voltage across the device using two 50-kΩ resistors. This Vcm error amplifier transmits a correction signal into the main amplifier to force the output average voltage to meet the target voltage on the Vocm pin.

8.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the PD pin asserted to a voltage greater than Vs– + 1.7 V, or turned *off* by asserting PD low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors. The Vocm control pin sets the output average voltage. Left open, Vocm defaults to an internal midsupply value. Driving this high-impedance input with a voltage reference within its valid range sets a target for the internal Vcm error amplifier.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMH6550 is a fully differential amplifier designed to provide low distortion amplification to wide bandwidth differential signals. The LMH6550, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the V^+ and V^- signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths. The third channel is the common-mode feedback circuit. This is the circuit that sets the output common mode as well as driving the V^+ and V^- outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common-mode feedback circuit allows single-ended to differential operation.

The LMH6550 is a voltage feedback amplifier with gain set by external resistors. Output common-mode voltage is set by the V_{CM} pin. This pin should be driven by a low impedance reference and should be bypassed to ground with a 0.1-µF ceramic capacitor. Any signal coupling into the V_{CM} will be passed along to the output and will reduce the dynamic range of the amplifier.

The LMH6550 is equipped with a ENABLE pin to reduce power consumption when not in use. The ENABLE pin floats to logic high. If this pin is not used it can be left floating. The amplifier output stage goes into a high impedance state when the amplifier is disabled. The feedback and gain set resistors will then set the impedance of the circuit. For this reason input to output isolation will be poor in the disabled state.

9.2 Typical Applications

9.2.1 Typical Fully Differential Application

The LMH6550 performs best when used with split supplies and in a fully differential configuration. See Figure 21 and Figure 22 for recommend circuits.

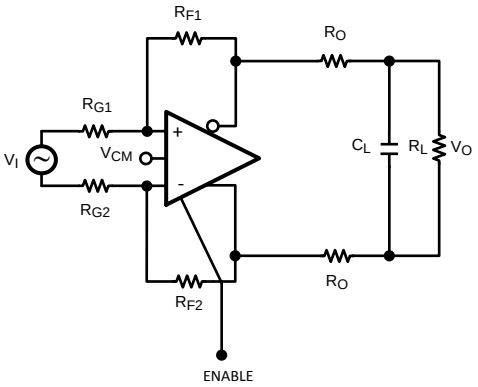


Figure 21. Typical Fully Differential Application Schematic

9.2.1.1 Design Requirements

Applications using fully differential amplifiers have several requirements. The main requirements are high linearity and good signal amplitude. Linearity is accomplished by using well matched feedback and gain set resistors as well as an appropriate supply voltage. The signal amplitude can be tailored by using an appropriate gain. In this design the gain is set for a gain of 2 (R_F=500/ R_G=250) and the distortion criteria is better than -90 dBc at a frequency of 5 Mhz. The supply voltages are set to +5 V and -5 V and the output common mode is 0 V. The LMH6550 can be placed into shutdown to reduce power dissipation to 10 mW.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

The power supplies for this design are symmetrical ±5-V supplies (not shown for simplicity). The ADC input common mode is 1 V which is within the optimum operating range for the LMH6550 when used on ±5-V split supplies. The gain of this circuit is equal to RF/RG and due to the split supplies can be set to gains of 15 V/V or less. Higher gains will result in values of RF that are too large for high speed operation.

9.2.1.2.1 Fully Differential Operation

The circuit shown in is a typical fully differential application as might be used to drive an ADC. In this circuit closed loop gain, (A_V) = V_{OUT}/ V_{IN} = R_F/R_G. For all the applications in this data sheet V_{IN} is presumed to be the voltage presented to the circuit by the signal source. For differential signals this will be the difference of the signals on each input (which will be double the magnitude of each individual signal), while in single-ended inputs it will just be the driven input signal.

The resistors R_O help keep the amplifier stable when presented with a load C_L as is typical in an analog to digital converter (ADC). When fed with a differential signal, the LMH6550 provides excellent distortion, balance and common-mode rejection provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With a DC CMRR of over 80 dB, the DC and low frequency CMRR of most circuits will be dominated by the external resistors and board trace resistance. At higher frequencies board layout symmetry becomes a factor as well. Precision resistors of at least 0.1% accuracy are recommended and careful board layout will also be required.

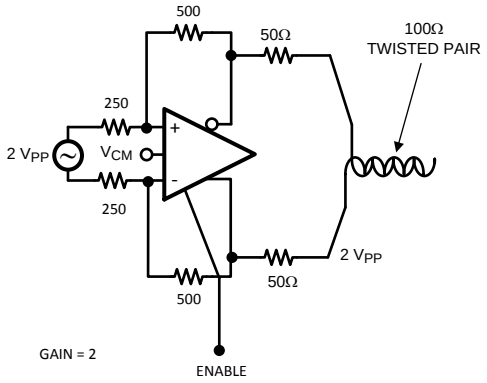


Figure 22. Fully Differential Cable Driver

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current the LMH6550 makes an excellent cable driver as shown in Figure 22. The LMH6550 is also suitable for driving differential cables from a single-ended source.

The LMH6550 requires supply bypassing capacitors as shown in Figure 23 and Figure 24. The 0.01 µF and 0.1 µF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. The SMT capacitors should be connected directly to a ground plane. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} pin to ground. The V_{CM} pin is a high impedance input to a buffer which sets the output common-mode voltage. Any noise on this input is transferred directly to the output. Output common-mode noise will result in loss of dynamic range, degraded CMRR, degraded Balance and higher distortion. The V_{CM} pin should be bypassed even if the pin in not used. There is an internal resistive divider on chip to set the output common-mode voltage to the mid point of the supply pins. The impedance looking into this pin is approximately 25 kΩ. If a different output common-mode voltage is desired drive this pin with a clean, accurate voltage reference.

Typical Applications (continued)

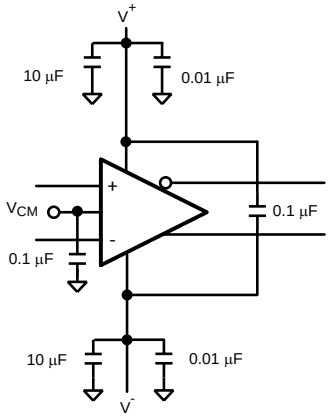


Figure 23. Split Supply Bypassing Capacitors

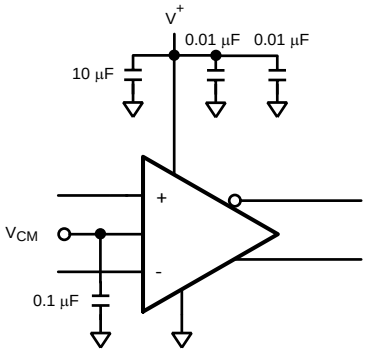


Figure 24. Single Supply Bypassing Capacitors

9.2.1.2.2 Capacitive Drive

As noted in *Driving Analog-to-Digital Converters*, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500 Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000 Ω or higher. If driving a transmission line, such as 50-Ω coaxial or 100-Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance. For other applications see Figure 6 and Figure 25 in *Typical Characteristics*.

9.2.1.2.3 Application Curves

Many application circuits have capacitive loading. As shown in Figure 25, amplifier bandwidth is reduced with increasing capacitive load, so parasitic capacitance should be strictly limited.

To ensure stability, resistance should be added between the capacitive load and the amplifier output pins. The value of the resistor is dependent on the amount of capacitive load as shown in Figure 26. This resistive value is a suggestion. System testing will be required to determine the optimal value. Using a smaller resistor will retain more system bandwidth at the expense of overshoot and ringing, while larger values of resistance will reduce overshoot but will also reduce system bandwidth.

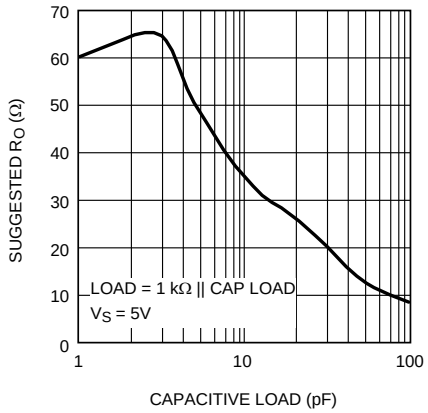


Figure 25. Suggested R_{OUT} vs Cap Load

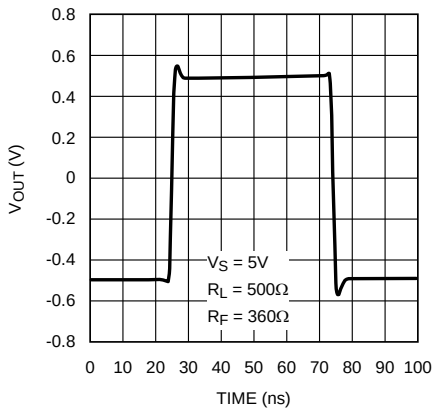


Figure 26. 1 V_{PP} Pulse Response Single-Ended Input

Typical Applications (continued)

9.2.2 Driving Analog-to-Digital Converters

Analog-to-digital converters (ADC) present challenging load conditions. They typically have high-impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. Figure 27 shows a typical circuit for driving an ADC. The two 56-Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors form part of a low pass filter which helps to provide anti alias and noise reduction functions. The two 39-pF capacitors help to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the low pass filtering of the ADC input. In the circuit of Figure 27 the cutoff frequency of the filter is 1/ (2*π*56 Ω *(39 pF + 14 pF)) = 53 MHz (which is slightly less than the sampling frequency). Note that the ADC input capacitance must be factored into the frequency response of the input filter, and that being a differential input the effective input capacitance is double. Also as shown in Figure 27 the input capacitance to many ADCs is variable based on the clock cycle. See the data sheet for your particular ADC for details.

The amplifier and ADC should be located as closely together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the Nyquist range (DC to Fs/2). See AN-236 for more details on the subsampling process and the requirements this imposes on the filtering necessary in your system.

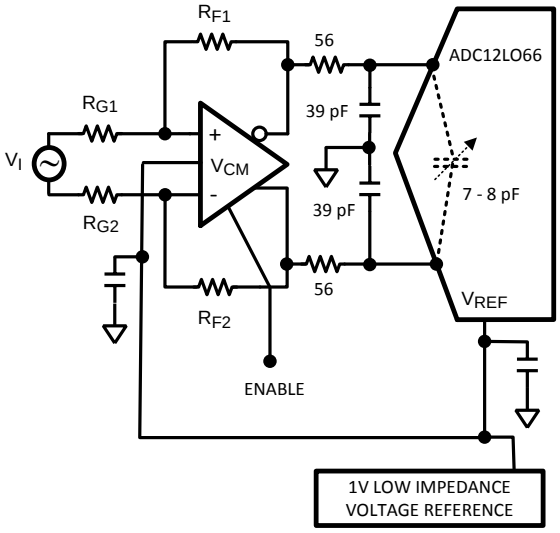


Figure 27. Driving an ADC

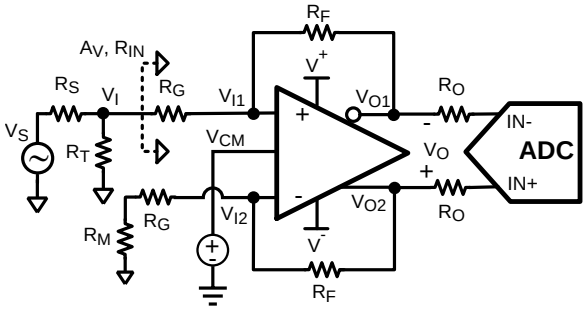
Typical Applications (continued)

9.2.3 Single-Ended Input to Differential Output

The LMH6550 provides excellent performance as an active balun transformer. Figure 28 shows a typical application where an LMH6550 is used to produce a differential signal from a single-ended source.

In single-ended input operation the output common-mode voltage is set by the V_{CM} pin as in fully differential mode. Also, in this mode the common-mode feedback circuit must recreate the signal that is not present on the unused differential input pin. Figure 19 is the measurement of the effectiveness of this process. The common-mode feedback circuit is responsible for ensuring balanced output with a single-ended input. Balance error is defined as the amount of input signal that couples into the output common mode. It is measured as a the undesired output common-mode swing divided by the signal on the input. Balance error can be caused by either a channel to channel gain error, or phase error. Either condition will produce a common-mode shift. Figure 19 measures the balance error with a single-ended input as that is the most demanding mode of operation for the amplifier.

Supply and V_{CM} pin bypassing are also critical in this mode of operation. See the above section on for bypassing recommendations and also see Figure 23 and Figure 24 for recommended supply bypassing configurations.



Conditions :

$R_S = R_T \,||\, R_{IN}$

$R_M = R_T \,||\, R_S$

Definitions :

$$\beta_1 = \frac{R_G}{R_G + R_F}$$

$$\beta_2 = \frac{R_G + R_M}{R_G + R_M + R_F}$$

$$A_v = \frac{V_O}{V_I} = \frac{2(1-\beta_1)}{\beta_1 + \beta_2} \cong \frac{R_F}{R_G} \text{ for } R_M << R_G$$

$$R_{IN} = \frac{2R_G + R_M(1-\beta_2)}{1+\beta_2} = \frac{R_G\left(1+\frac{\beta_2}{\beta_1}\right)}{1+\beta_2} \cong \frac{2R_G(1+A_v)}{2+A_v} \text{ for } R_M << R_G$$

$$V_{OCM} = V_{CM} = \frac{V_{O1} + V_{O2}}{2} \text{ (by design)}$$

$$V_{ICM} = \frac{V_{I1} + V_{I2}}{2} = V_{OCM} \cdot \beta_2 \cong \frac{V_{OCM}}{1+A_v} \text{ for } R_M << R_G$$

Figure 28. Single-Ended Input to Differential Output Schematic

Typical Applications (continued)

9.2.4 Single Supply Operation

The input stage of the LMH6550 has a built in offset of 0.7 V towards the lower supply to accommodate single supply operation with single-ended inputs. As shown in Figure 28, the input common-mode voltage is less than the output common voltage. It is set by current flowing through the feedback network from the device output. The input common-mode range of 0.4 V to 3.2 V places constraints on gain settings. Possible solutions to this limitation include AC coupling the input signal, using split power supplies and limiting stage gain. AC coupling with single supply is shown in Figure 29.

In Figure 28 closed loop gain = V_O / V_I ≅ R_F / R_G, where V_I =V_S / 2, as long as R_M << R_G. Note that in single-ended to differential operation V_I is measured single-ended while V_O is measured differentially. This means that gain is really 1/2 or 6 dB less when measured on either of the output pins separately. Additionally, note that the input signal at R_T (labeled as V_I) is 1/2 of V_S when R_T is chosen to match R_S to R_{IN}.

V_{ICM} = Input common-mode voltage = (V_{I1}+V_{I2}) / 2.

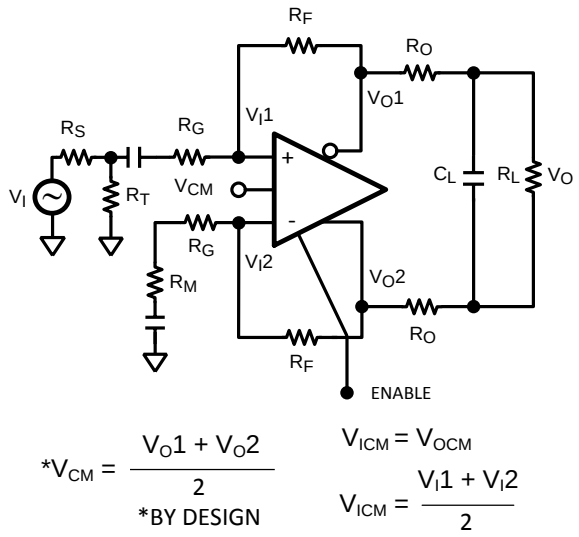


Figure 29. AC-Coupled for Single Supply Operation

Typical Applications (continued)

9.2.5 Using Transformers

Transformers are useful for impedance transformation as well as for single to differential, and differential to single-ended conversion. A transformer can be used to step up the output voltage of the amplifier to drive very high impedance loads as shown in Figure 30. Figure 32 shows the opposite case where the output voltage is stepped down to drive a low-impedance load.

Transformers have limitations that must be considered before choosing to use one. Compared to a differential amplifier, the most serious limitations of a transformer are the inability to pass DC and balance error (which causes distortion and gain errors). For most applications the LMH6550 will have adequate output swing and drive current and a transformer will not be desirable. Transformers are used primarily to interface differential circuits to 50-Ω single-ended test equipment to simplify diagnostic testing.

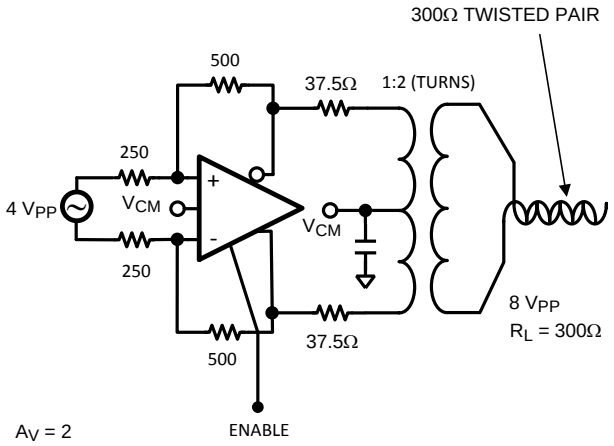


Figure 30. Transformer Out High-Impedance Load

$$V_L = \frac{V_{IN} * A_V * N}{\left(\frac{2\,R_{OUT} * N^2}{R_L} + 1\right)}$$

WHERE V_{IN} = DIFFERENTIAL INPUT VOLTAGE

$$N = \text{TRANSFORMER TURNS RATIO} = \left(\frac{\text{SECONDARY}}{\text{PRIMARY}}\right)$$

A_V = CLOSED LOOP AMPLIFIER GAIN

R_{OUT} = SERIES OUTPUT MATCHING RESISTOR

R_L = LOAD RESISTOR

V_L = VOLTAGE ACROSS LOAD RESISTOR

Figure 31. Calculating Transformer Circuit Net Gain

Typical Applications (continued)

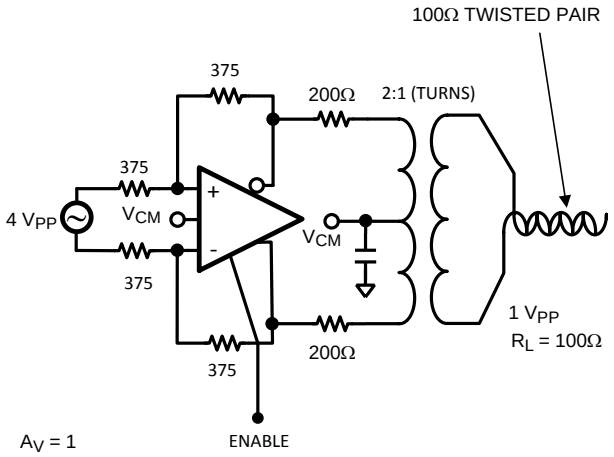
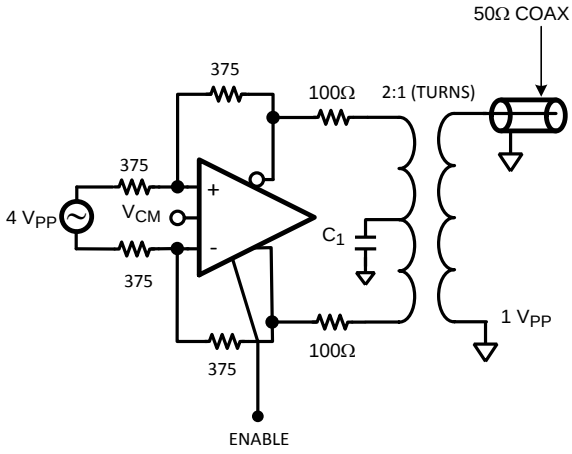


Figure 32. Transformer Out Low-Impedance Load



GAIN = 1

C_1 IS NOT REQUIRED IF V_{CM} = GROUND

Figure 33. Driving 50-Ω Test Equipment

10 Power Supply Recommendations

The LMH6550 can be used with any combination of positive and negative power supplies as long as the combined supply voltage is between 4.5 V and 12 V. The LMH6550 will provide best performance when the output voltage is set at the mid supply voltage, and when the total supply voltage is between 9 V and 12 V. When selecting a supply voltage that is less than 9 V it is important to consider both the input common-mode voltage range as well as the output voltage range.

Power supply bypassing as shown in Figure 23 and Figure 24 is important and power supply regulation should be within 5% or better when using a supply voltage near the edges of the operating range.

11 Layout

11.1 Layout Guidelines

The LMH6550 is a very high performance amplifier. To get maximum benefit from the differential circuit architecture, board layout and component selection is very critical. The circuit board should have low a inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3-4 mm of the amplifier as should the supply bypass capacitors. The LMH730154 evaluation board is an example of good layout techniques.

The LMH6550 is sensitive to parasitic capacitances on the amplifier inputs and to a lesser extent on the outputs as well. Ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry will contribute to distortion and balance errors.

TI offers evaluation boards to aid in device testing and characterization and as a guide for proper layout. Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see *OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, SNOA367, for more information).

11.2 Layout Example

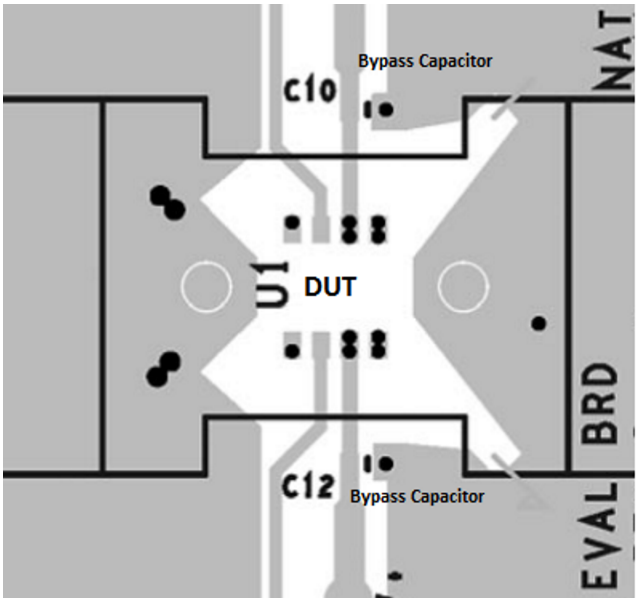


Figure 34. EVM Layout (Top)

Layout Example (continued)

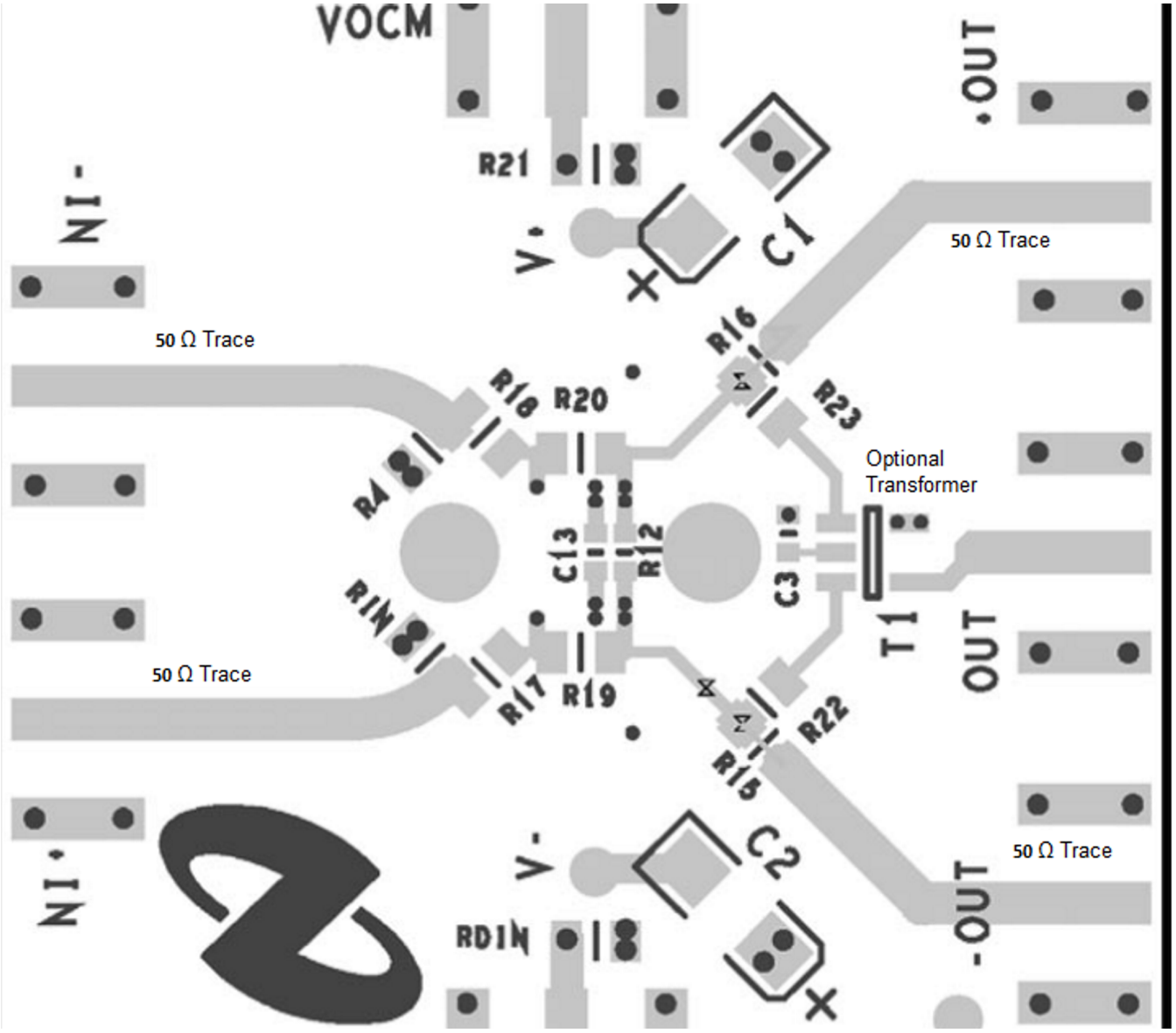


Figure 35. EVM Layout (Bottom)

11.3 Power Dissipation

The LMH6550 is optimized for maximum speed and performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} of 150°C is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6550:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* (V_S)$, where $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid rail.)
2. Calculate the RMS power dissipated in each of the output stages: P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$, where V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single-ended amplifiers and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6550 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150° - T_{AMB})/ \theta_{JA} \quad (1)$$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SOIC package θ_{JA} is 150°C/W
- For the VSSOP package θ_{JA} is 235°C/W

NOTE

If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

11.4 ESD Protection

The LMH6550 is protected against electrostatic discharge (ESD) on all pins. The LMH6550 will survive 2000 V Human Body model and 200 V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6550 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers, SNOA367

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6550MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH65 50MA	
LMH6550MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 50MA	Samples
LMH6550MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 50MA	Samples
LMH6550MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AL1A	Samples
LMH6550MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	AL1A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

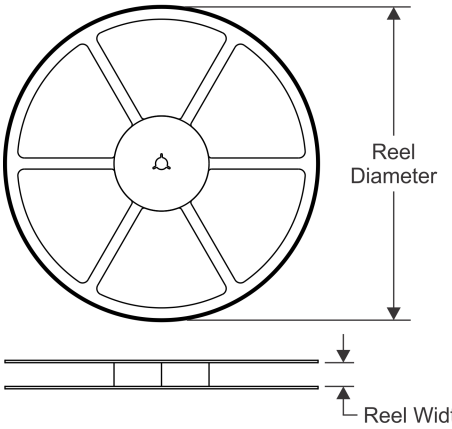
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

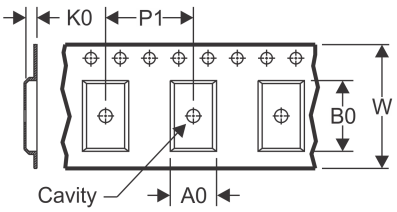
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

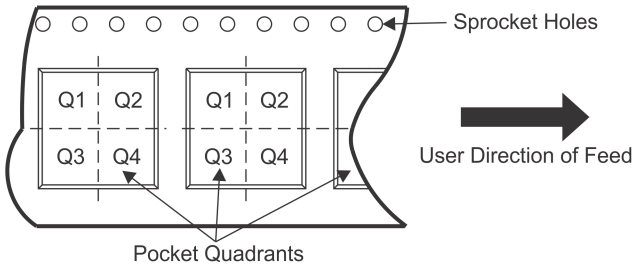


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

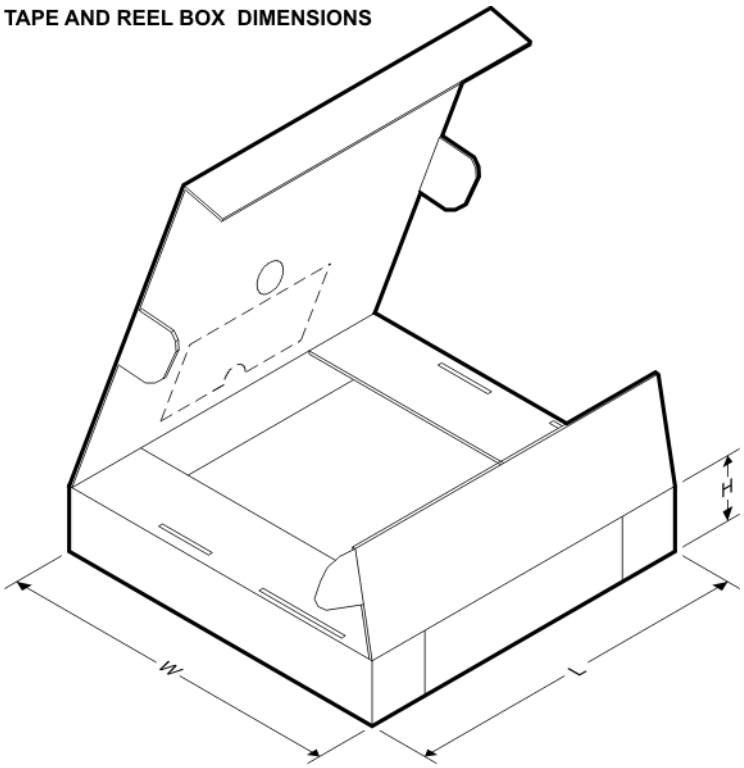
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

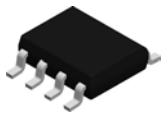
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6550MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6550MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6550MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6550MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6550MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6550MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

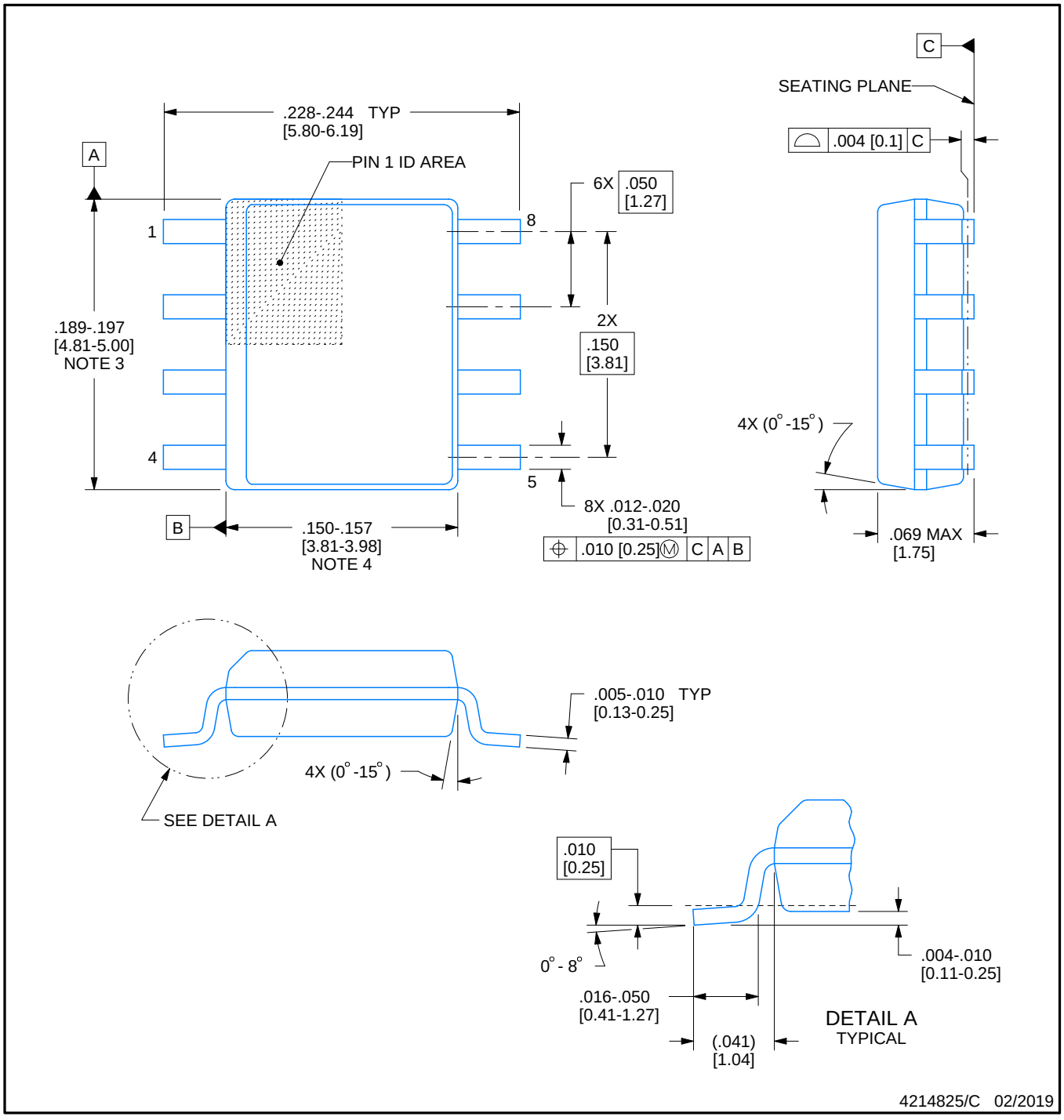


PACKAGE OUTLINE

D0008A

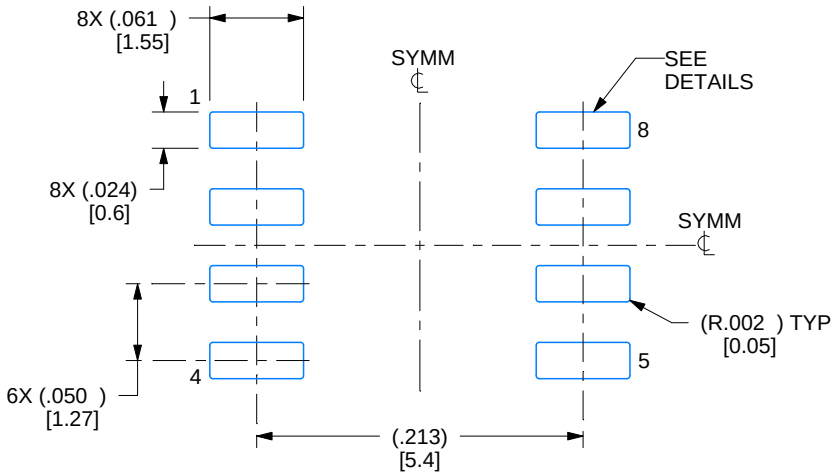
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

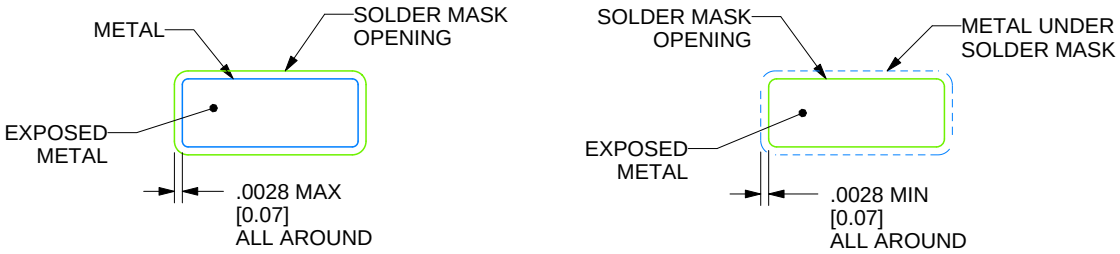


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

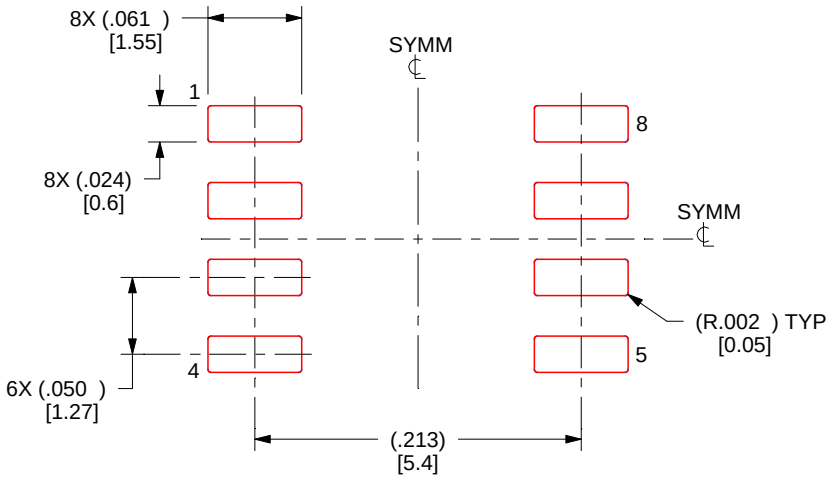
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



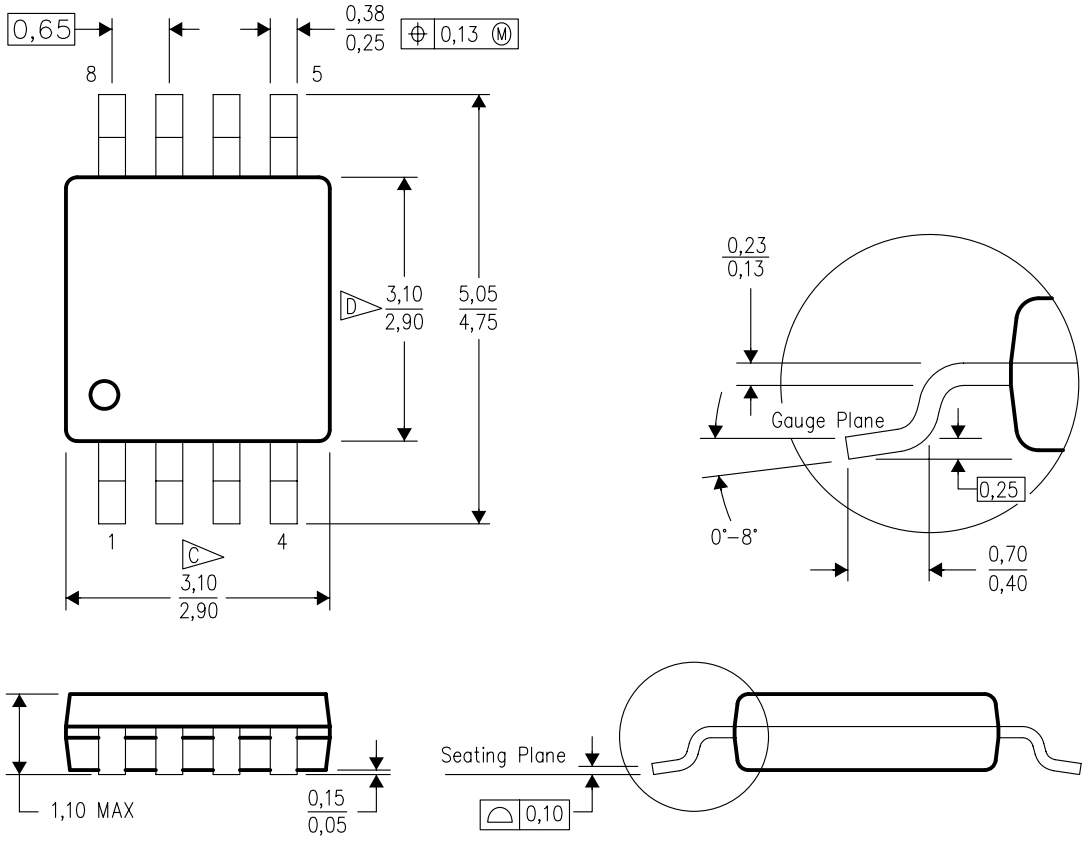
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

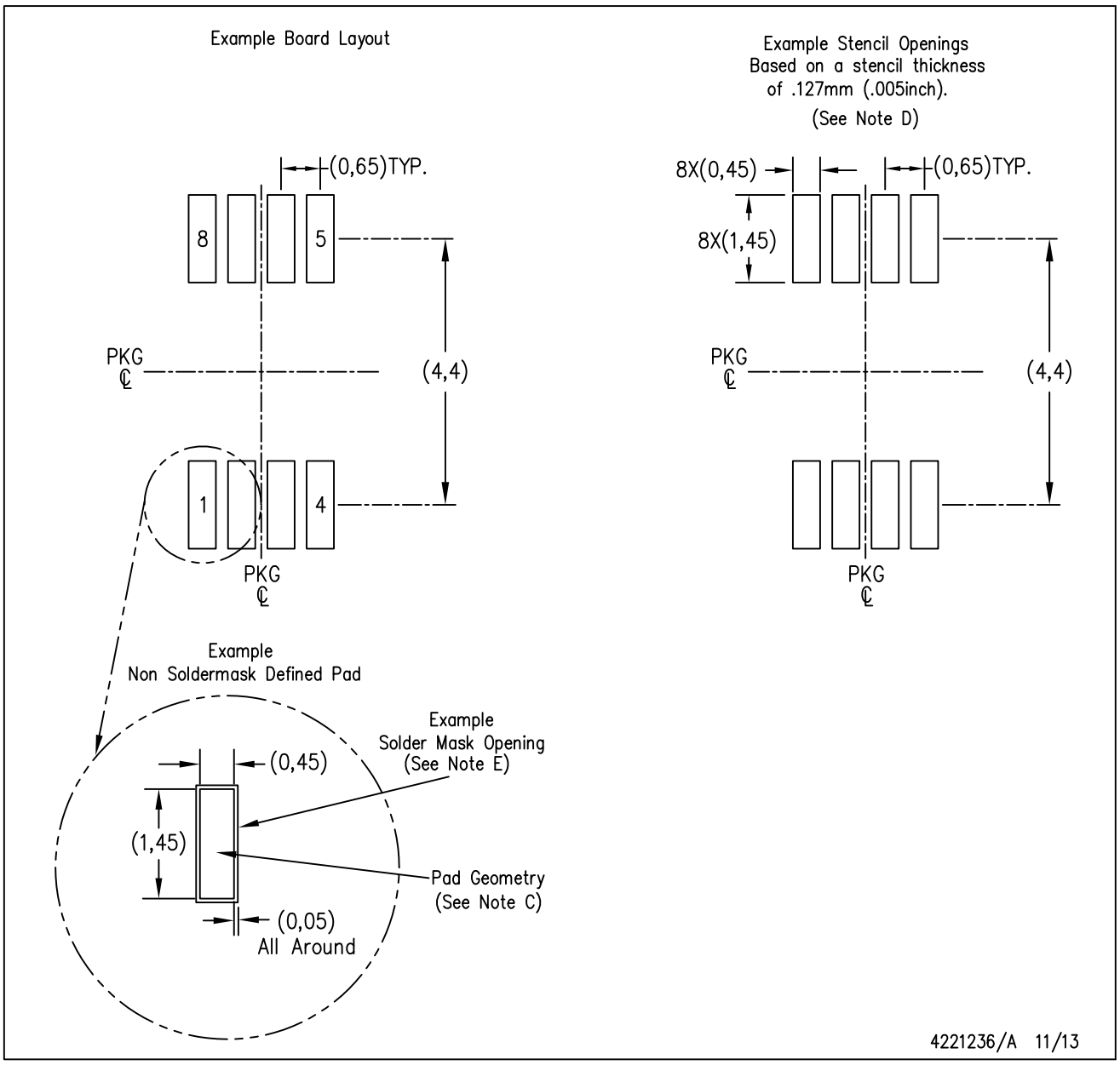
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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