Freescale Semiconductor
Technical Data

Document Number: MHT1003N
Rev. 0, 12/2014

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 250 W CW RF power transistor is designed for consumer and commercial cooking applications operating in the 2450 MHz ISM band.

Typical Performance: V_{DD} = 32 Vdc, I_{DQ} = 25 mA

Frequency (MHz)	Signal Type	G_{ps} (dB)	PAE (%)	P_{out} (W)
2400	CW	15.0	57.0	250
2450		15.9	59.0	250
2500		14.9	55.0	250

Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage	Result
2450	CW	> 10:1 at all Phase Angles	14 (3 dB Overdrive)	32	No Device Degradation

Features

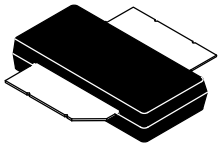
- Characterized with series equivalent large-signal impedance parameters and common source S-parameters
- Internally pre-matched for ease of use
- Qualified for operation at 32 Vdc
- Integrated ESD protection
- 150°C case operating temperature
- 225°C die temperature capability

Typical Applications

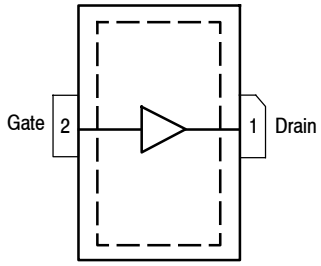
- Consumer cooking
- Commercial cooking

MHT1003NR3

2450 MHz, 250 W CW, 32 V
RF POWER LDMOS TRANSISTOR
FOR CONSUMER AND
COMMERCIAL COOKING



OM-780-2L
PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

freescale

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	769 3.85	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 98°C, 250 W CW, 32 Vdc, I_{DQ} = 100 mA, 2450 MHz	$R_{\theta JC}$	0.26	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2, passes 2500 V
Machine Model (per EIA/JESD22–A115)	B, passes 250 V
Charge Device Model (per JESD22–C101)	IV, passes 2000 V

Table 4. Moisture Sensitivity Level (MSL)

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 303 μAdc)	$V_{GS(th)}$	0.9	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 30 Vdc, I_D = 100 mAdc)	$V_{GS(Q)}$	—	1.6	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3.7 Adc)	$V_{DS(on)}$	0.1	0.19	0.4	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.

(continued)

Table 6. Typical Performance

In Freescale Reference Circuit, 50 ohm system, V_{DD} = 32 Vdc, I_{DQ} = 25 mA, P_{out} = 250 W, f = 2450 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	—	15.9	—	dB
Power Added Efficiency	PAE	—	59.0	—	%
P_{out} @ 1 dB Compression Point	P1dB	—	263	—	W
P_{out} @ 3 dB Compression Point	P3dB	—	294	—	W
Gain Variation over Temperature (+25°C to +125°C)	ΔG	—	–0.016	—	dB/°C
Output Power Variation over Temperature (+25°C to +125°C)	ΔP1dB	—	–0.0064	—	dB/°C

Table 7. Load Mismatch/Ruggedness

In Freescale Reference Circuit, 50 ohm system, I_{DQ} = 100 mA

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
2450	CW	> 10:1 at all Phase Angles	14 (3 dB Overdrive)	32	No Device Degradation

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 32 Vdc, I_{DQ} = 136 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.11 – j5.09	1.25 + j5.36	1.17 – j4.69	16.4	55.2	330	53.8	52.5
2450	1.25 – j5.68	1.58 + j5.88	1.28 – j4.82	16.4	55.1	321	53.7	52.4
2500	1.41 – j5.96	1.91 + j6.34	1.25 – j4.90	16.5	55.1	327	55.2	54.0

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.11 – j5.09	1.22 + j5.53	1.15 – j4.80	14.2	55.9	387	53.6	51.5
2450	1.25 – j5.68	1.58 + j6.10	1.31 – j4.99	14.2	55.8	377	53.6	51.6
2500	1.41 – j5.96	1.96 + j6.63	1.26 – j5.07	14.2	55.8	383	54.2	52.1

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

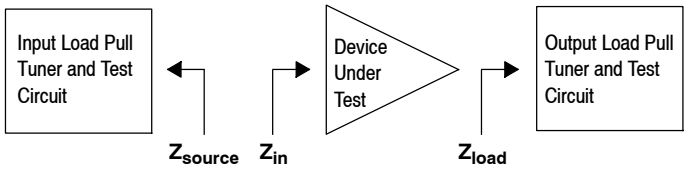
Table 9. Load Pull Performance — Maximum Power Added Efficiency Tuning

V_{DD} = 32 Vdc, I_{DQ} = 136 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Power Added Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.11 – j5.09	1.20 + j5.33	1.93 – j4.01	17.7	54.1	255	60.8	59.7
2450	1.25 – j5.68	1.49 + j5.88	1.90 – j3.82	17.9	53.7	235	60.5	59.5
2500	1.41 – j5.96	1.80 + j6.34	1.65 – j3.79	18.1	53.7	233	63.1	62.1

			Max Power Added Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	PAE (%)
2400	1.11 – j5.09	1.19 + j5.50	1.83 – j4.47	15.3	55.2	329	58.8	57.1
2450	1.25 – j5.68	1.52 + j6.09	1.94 – j4.29	15.6	54.9	309	59.3	57.7
2500	1.41 – j5.96	1.88 + j6.62	1.82 – j4.14	15.8	54.8	299	61.3	59.7

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P3dB - TYPICAL LOAD PULL CONTOURS — 2450 MHz

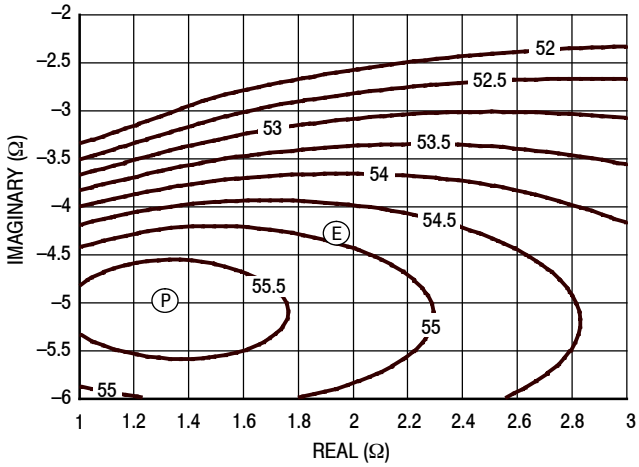


Figure 2. P3dB Load Pull Output Power Contours (dBm)

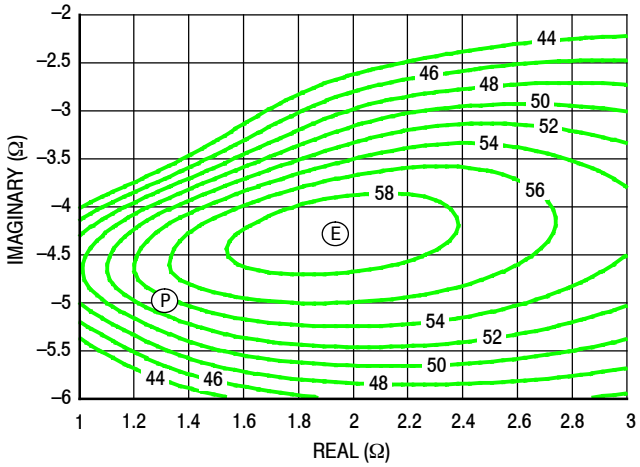


Figure 3. P3dB Load Pull Efficiency Contours (%)

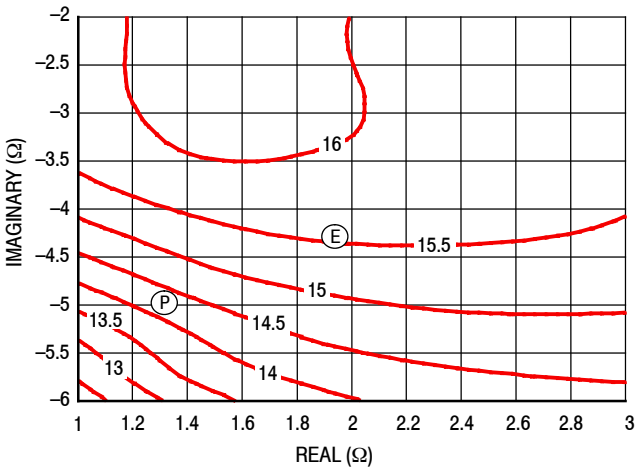


Figure 4. P3dB Load Pull Gain Contours (dB)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Power Added Efficiency

Gain

Power Added Efficiency

Output Power

2400–2500 MHz REFERENCE CIRCUIT — 2″ × 3″

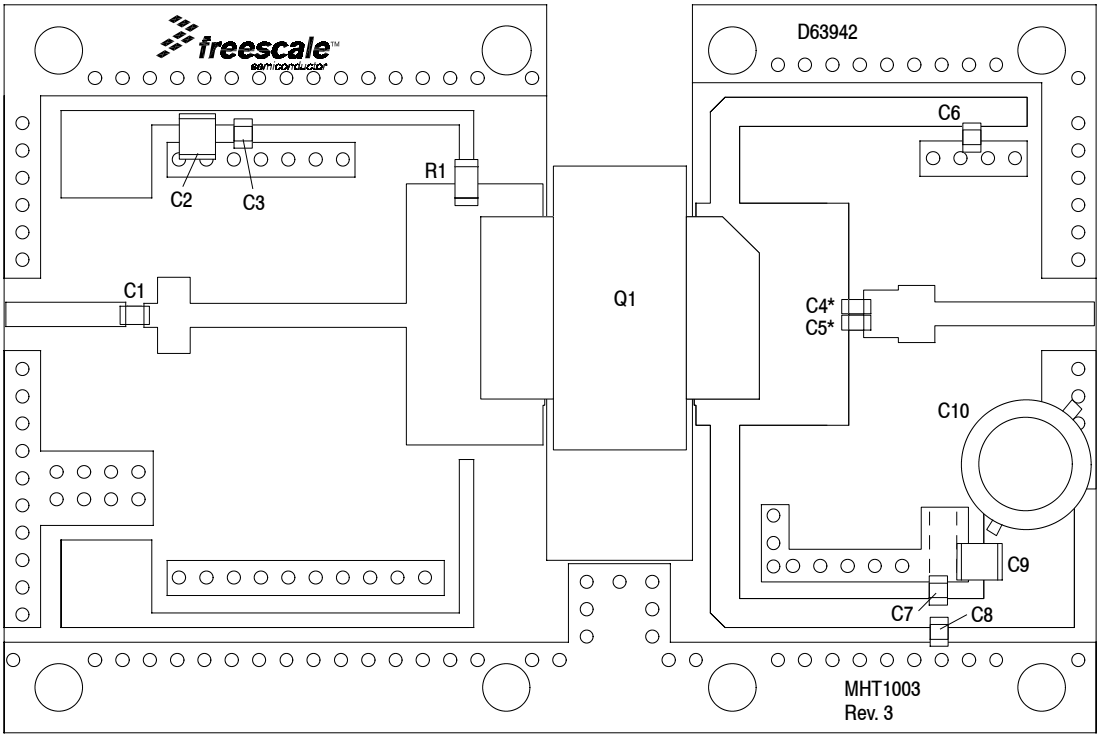
Table 10. 2400–2500 MHz Performance (In Freescale Reference Circuit, 50 ohm system)
V_{DD} = 32 Vdc, I_{DQ} = 25 mA, T_C = 25°C

Frequency (MHz)	P_{in} (W)	G_{ps} (dB)	η_D (%)	PAE (%)	P_{out} (W)
2400	8.0	15.0	58.5	57.0	253
2450	6.5	15.9	60.6	59.1	251
2500	8.0	15.0	57.2	55.4	250

Table 11. Load Mismatch/Ruggedness (In Freescale Reference Circuit)

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
2450	CW	> 10:1 at all Phase Angles	14 (3 dB Overdrive)	32	No Device Degradation

2400–2500 MHz REFERENCE CIRCUIT — 2″ × 3″



*C4 and C5 are mounted vertically.

Figure 5. MHT1003NR3 Reference Circuit Component Layout — 2400–2500 MHz

Table 12. MHT1003NR3 Reference Circuit Component Designations and Values — 2400–2500 MHz

Part	Description	Part Number	Manufacturer
C1, C3, C4, C5, C6, C7, C8	27 pF Chip Capacitors	ATC600F270JT250XT	ATC
C2, C9	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
C10	220 μF, 50 V Electrolytic Capacitor	227CKE050M	Illinois Capacitor
Q1	RF Power LDMOS Transistor	MHT1003NR3	Freescale
R1	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
PCB	Rogers RT6035HTC, 0.030″, ε_r = 3.66	D63942	MTL

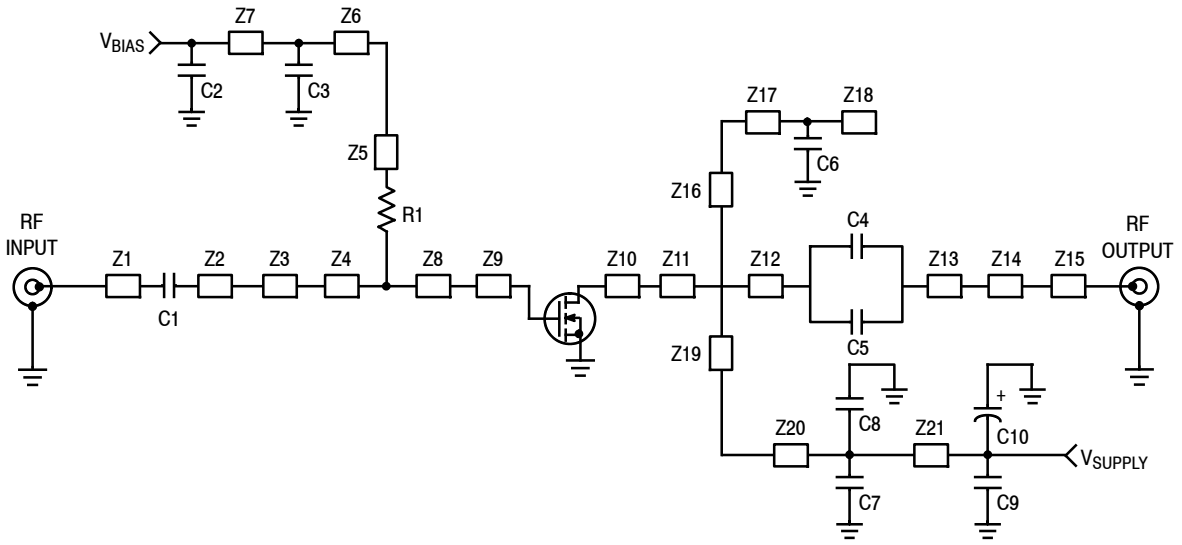


Figure 6. MHT1003NR3 Reference Circuit Schematic — 2400–2500 MHz

Table 13. MHT1003NR3 Reference Circuit Microstrips — 2400–2500 MHz

Microstrip	Description
Z1	0.329″ × 0.066″ Microstrip
Z2	0.037″ × 0.066″ Microstrip
Z3	0.090″ × 0.210″ Microstrip
Z4	0.593″ × 0.066″ Microstrip
Z5	0.161″ × 0.040″ Microstrip
Z6	0.569″ × 0.040″ Microstrip
Z7	0.051″ × 0.040″ Microstrip
Z8	0.376″ × 0.718″ Microstrip
Z9	0.005″ × 0.500″ Microstrip
Z10	0.005″ × 0.500″ Microstrip
Z11	0.040″ × 0.610″ Microstrip

Microstrip	Description
Z12	0.300″ × 0.610″ Microstrip
Z13	0.096″ × 0.130″ Microstrip
Z14	0.100″ × 0.156″ Microstrip
Z15	0.439″ × 0.066″ Microstrip
Z16	0.291″ × 0.080″ Microstrip
Z17	0.613″ × 0.080″ Microstrip
Z18	0.127″ × 0.080″ Microstrip
Z19	0.555″ × 0.080″ Microstrip
Z20	0.670″ × 0.080″ Microstrip
Z21	0.2497″ × 0.3302″ Microstrip

TYPICAL CHARACTERISTICS — 2400–2500 MHz REFERENCE CIRCUIT

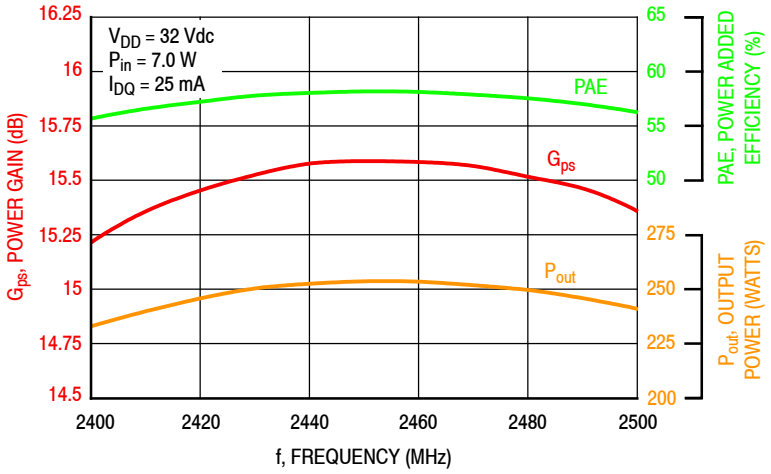


Figure 7. Power Gain, Power Added Efficiency and Output Power versus Frequency at a Constant Input Power

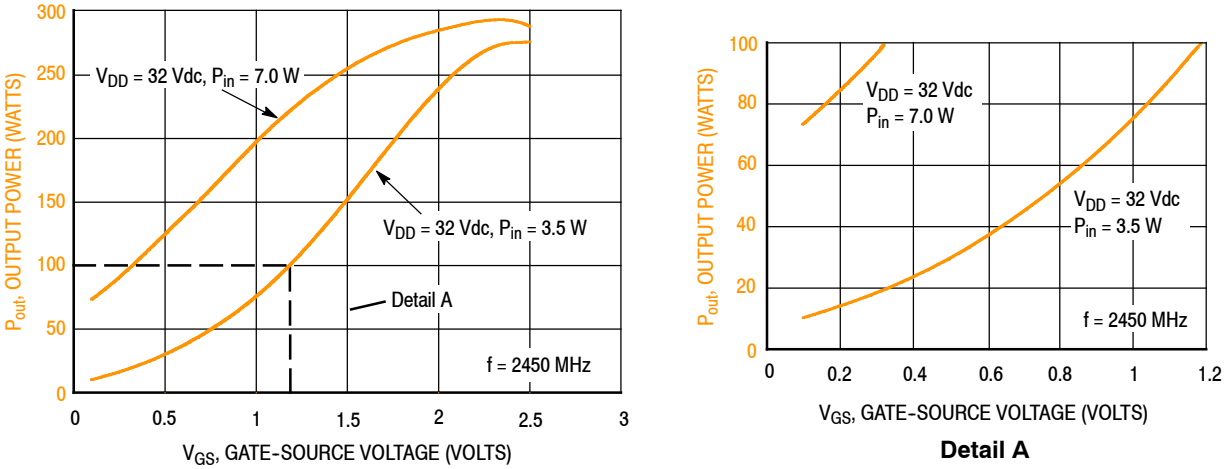


Figure 8. Output Power versus Gate-Source Voltage

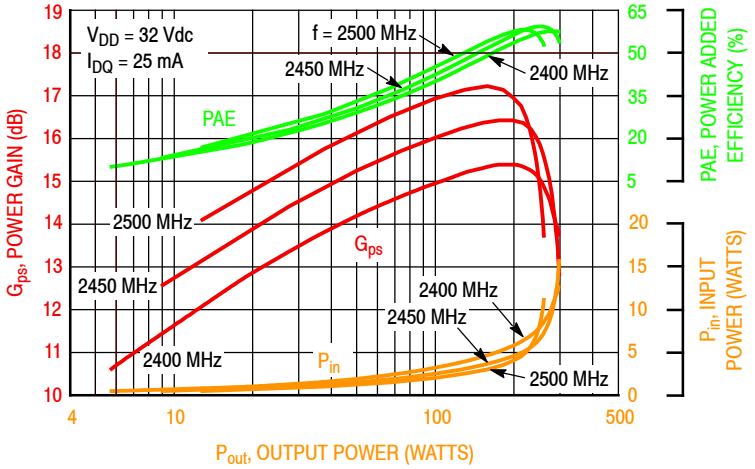


Figure 9. Power Gain, Power Added Efficiency and Input Power versus Output Power and Frequency

TYPICAL CHARACTERISTICS — 2400–2500 MHz REFERENCE CIRCUIT

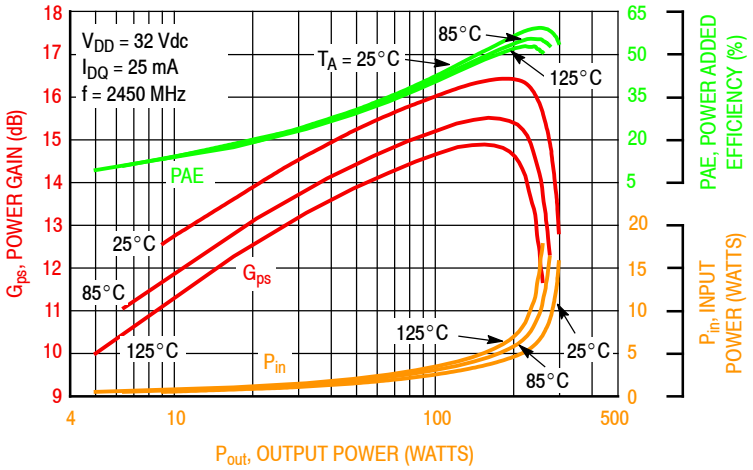
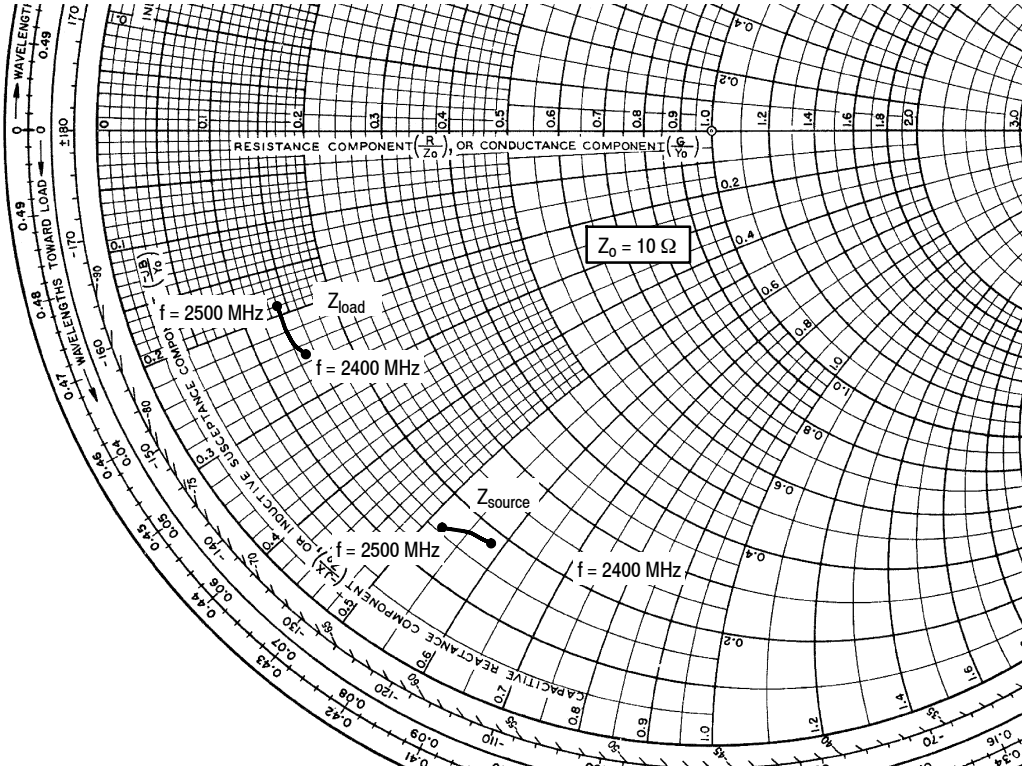


Figure 10. Power Gain, Power Added Efficiency and Input Power versus Output Power and Temperature

2400–2500 MHz REFERENCE CIRCUIT



f MHz	Z_{source} Ω	Z_{load} Ω
2400	1.76 – j5.76	1.49 – j2.45
2450	1.66 – j5.50	1.43 – j2.18
2500	1.56 – j5.23	1.36 – j1.90

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

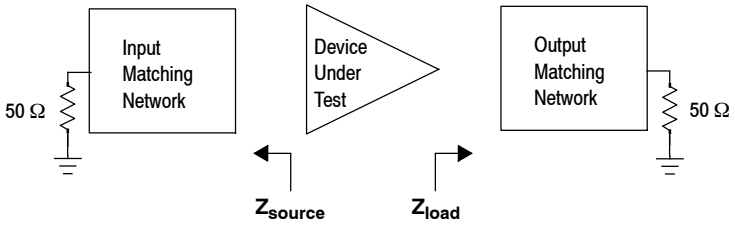
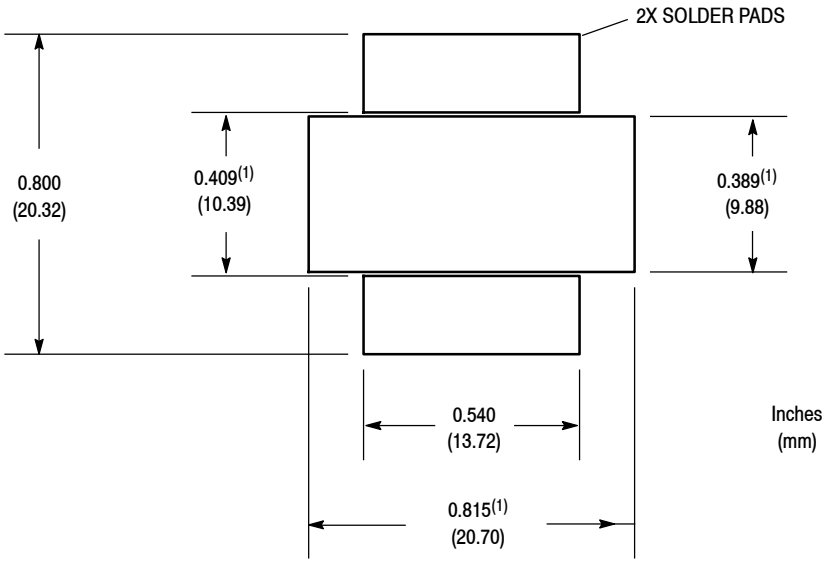


Figure 11. Series Equivalent Source and Load Impedance — 2400–2500 MHz



1. Slot dimensions are minimum dimensions and exclude milling tolerances

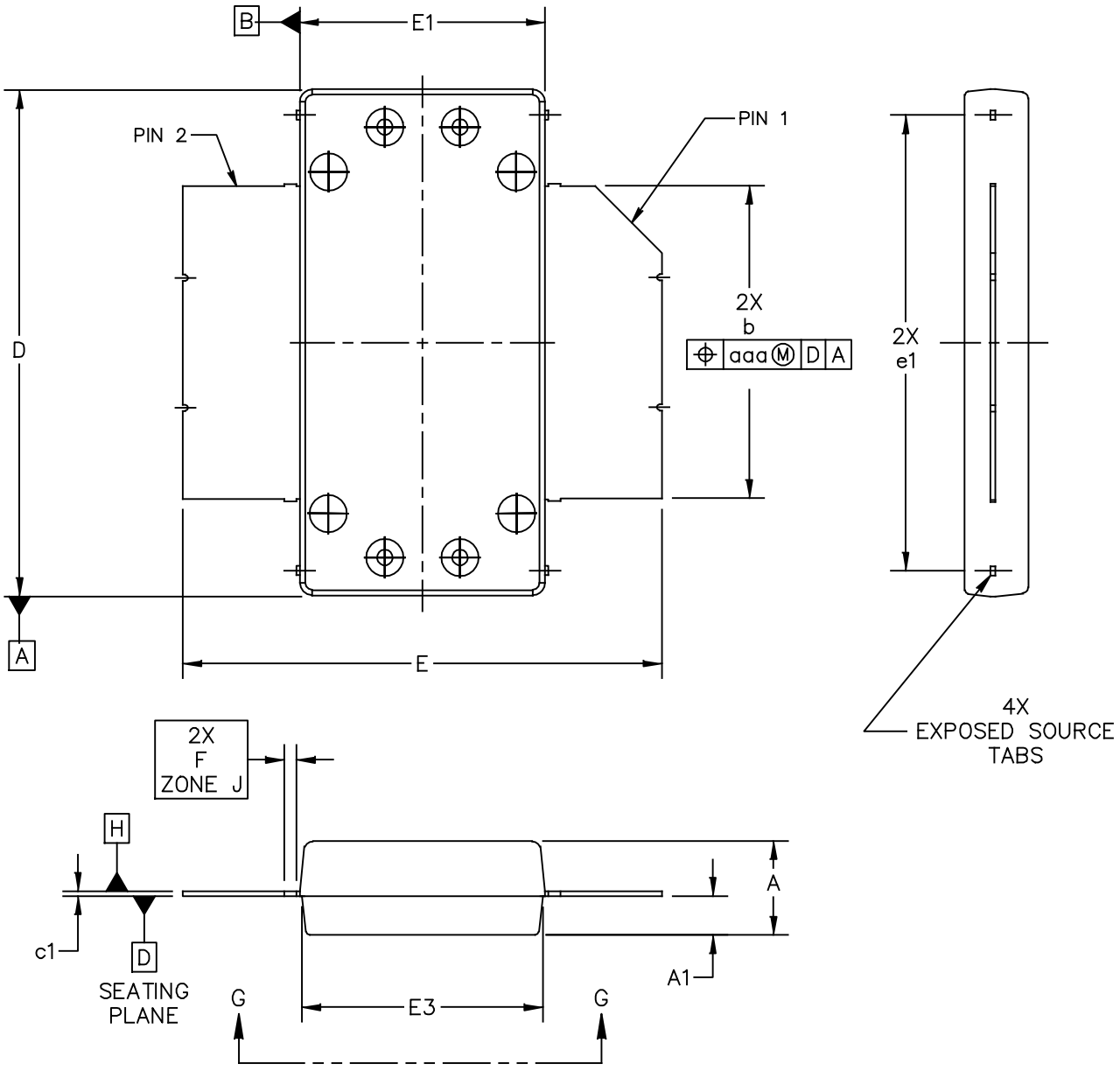
Figure 12. PCB Pad Layout for OM-780-2L

Figure 13. Product Marking

Table 14. Ordering Information

Device	Tape and Reel Information	Package
MHT1003NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-2L

PACKAGE DIMENSIONS



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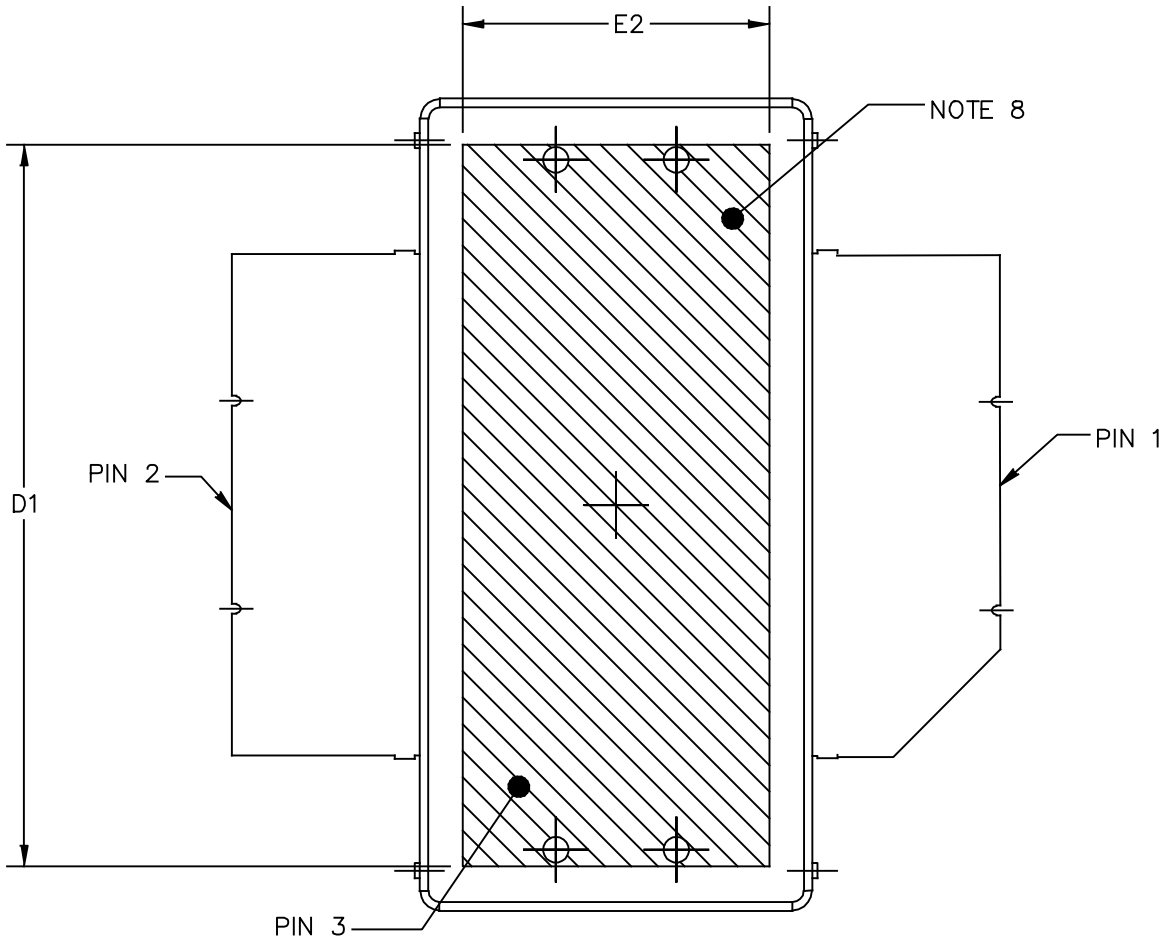
	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	



BOTTOM VIEW
VIEW G–G

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	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

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TITLE:	DOCUMENT NO: 98ASA10831D	REV: B
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	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2014	• Initial Release of Data Sheet

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Document Number: MHT1003N
Rev. 0, 12/2014