

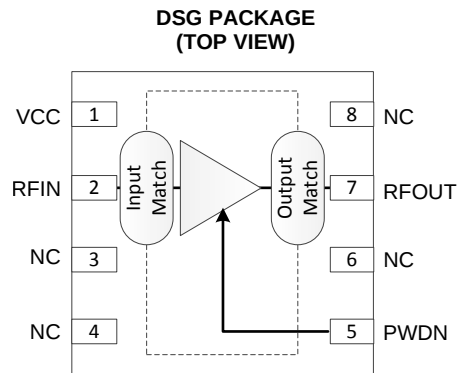
目录

1	特性	1	7.2	Functional Block Diagram	8
2	应用范围	1	7.3	Feature Description	8
3	说明	1	7.4	Device Functional Modes	8
4	修订历史记录	2	8	Applications and Implementation	9
5	Pin Configuration and Functions	3	8.1	Application Information	9
6	Specifications	4	8.2	Typical Application	9
6.1	Absolute Maximum Ratings	4	9	Power Supply Recommendations	10
6.2	Handling Ratings	4	10	Layout	11
6.3	Recommended Operating Conditions	4	10.1	Layout Guidelines	11
6.4	Thermal Information	4	10.2	Layout Example	11
6.5	Electrical Characteristics	5	11	器件和文档支持	12
6.6	Timing Requirements	5	11.1	Trademarks	12
6.7	Typical Characteristics	6	11.2	Electrostatic Discharge Caution	12
7	Detailed Description	8	11.3	Glossary	12
7.1	Overview	8	12	机械封装和可订购信息	12

4 修订历史记录

日期	修订版本	注释
2014 年 5 月	*	最初发布。

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
VCC	1	DC Bias.
RFIN	2	RF input. Connect to an RF source through a DC-blocking capacitor. Internally matched to 50 Ω .
NC	3, 4, 6, 8	No electrical connection. Connect pad to GND for board level reliability integrity.
PWDN	5	When high the device is in power down state. When LOW or NC the device is in active state. Internal pulldown resistor to GND.
RFOUT	7	RF Output and DC Bias (V_{CC}). Connect to DC supply through an RF choke inductor. Connect to output load through a DC-blocking capacitor. Internally matched to 50 Ω .
GND	PowerPAD™	RF and DC GND. Connect to PCB ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply Input voltage		–0.3	6	V
Input Power	With recommended R _{bias} resistor		10	dBm
Operating virtual junction temperature range		–40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T _{STG}	Storage temperature range		–65	150	°C
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	–1	1	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	–1	1	kV

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply Voltage, V _{CC}		4.5	5	5.25	V
Operating junction temperature, T _J		–40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DSG	UNIT
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	79.3	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	110	
R _{θJB}	Junction-to-board thermal resistance	49	
ψ _{JT}	Junction-to-top characterization parameter	6	
ψ _{JB}	Junction-to-board characterization parameter	49.4	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	19.2	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

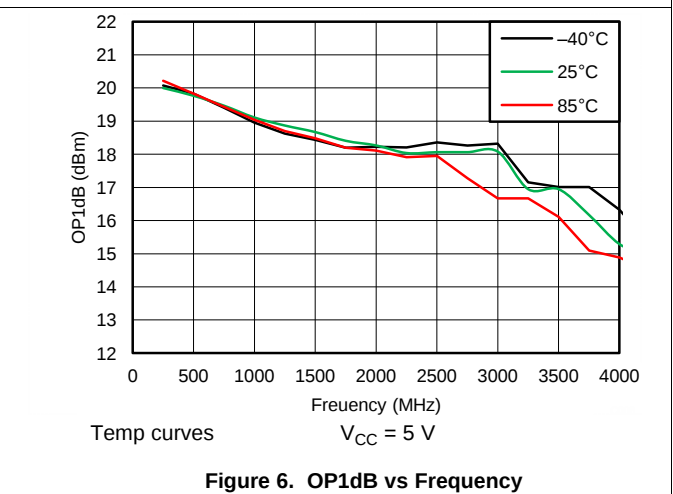
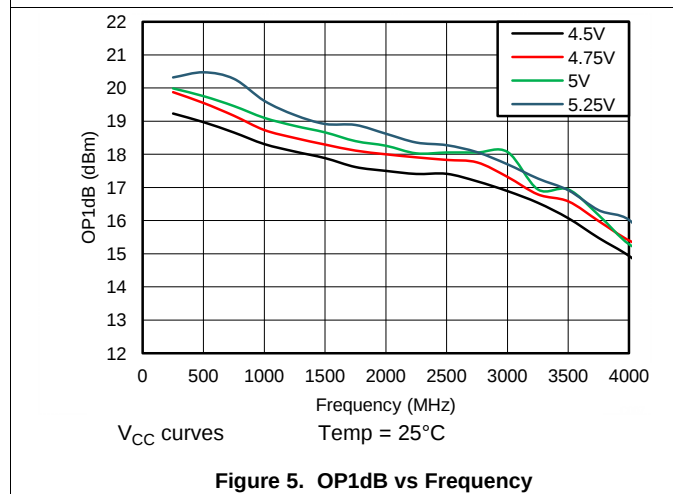
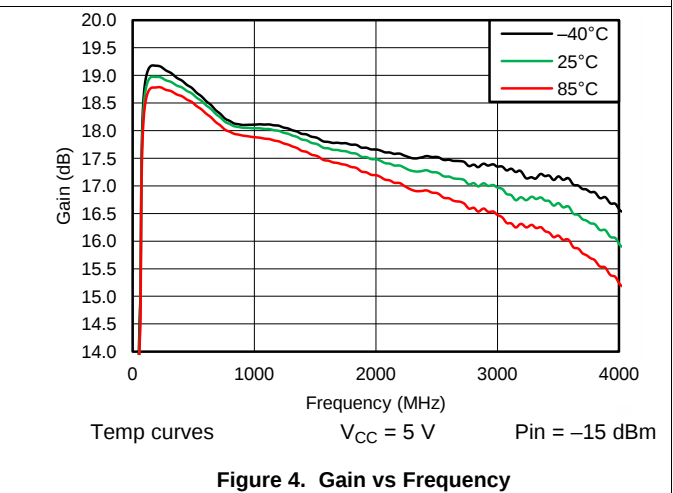
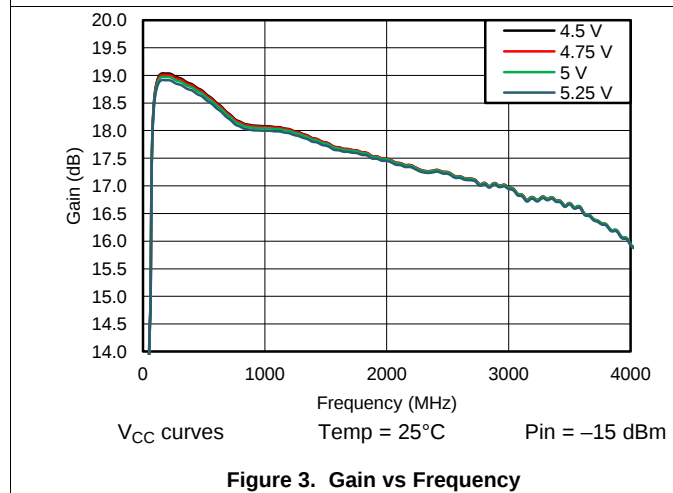
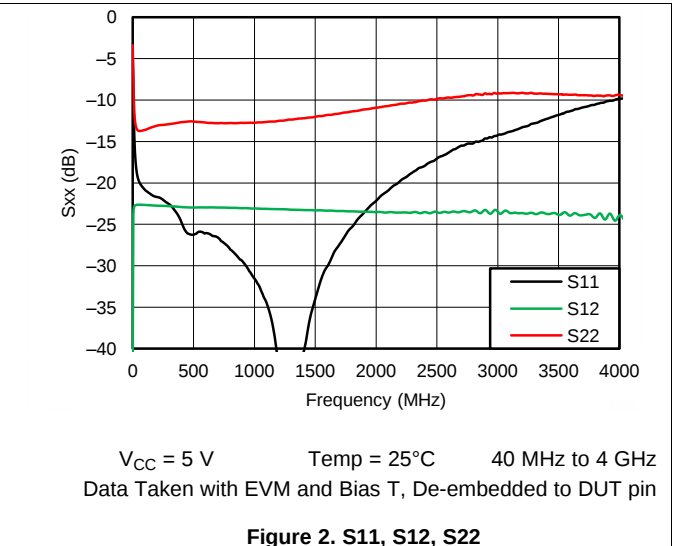
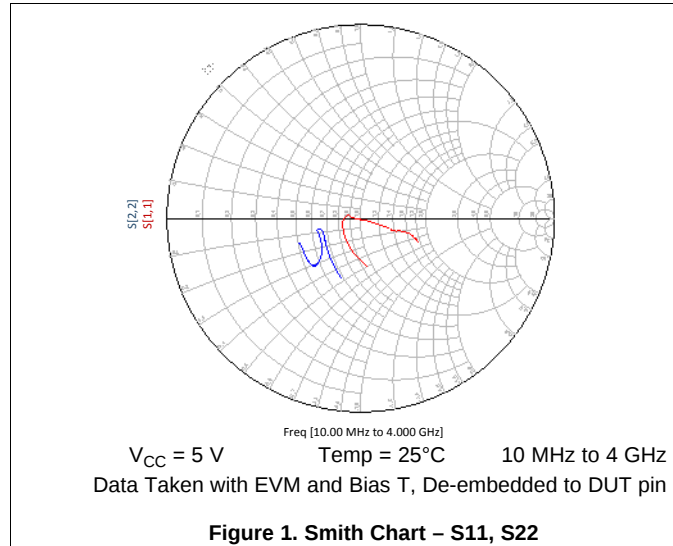
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $PWDN = \text{Low}$, $R_{BIAS} = 6.8\ \Omega$, $L_{OUT} = 100\text{ nH}$, $C1 = C2 = 1000\text{ pF}$, $Z_S = Z_L = 50\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Parameters						
I_{CC}	Total supply current			85		mA
	Power down current	$PWDN = \text{High}$		125		μA
P_{diss}	Power dissipation			0.425		W
RF Frequency Range						
	Frequency range		40		4000	MHz
G	Small signal gain	$f_{RF} = 400\text{ MHz}$		18.8		dB
		$f_{RF} = 2000\text{ MHz}$		17.5		dB
		$f_{RF} = 3000\text{ MHz}$		17		dB
		$f_{RF} = 4000\text{ MHz}$		16		dB
OP1dB	Output 1dB compression point	At 2000 MHz		18		dBm
OIP3	Output 3rd order intercept point	At 2000 MHz, 2-tone 10MHz apart		34		dBm
NF	Noise figure	At 2000 MHz		3.5		dB
$R_{(LI)}$	Input return loss			22		dB
$R_{(LO)}$	Output return loss			11		dB
PWDN Pin						
V_{IH}	High level input level		2			V
V_{IL}	Low level input level				0.8	V
I_{IH}	High level input current			30		μA
I_{IL}	Low level input current			1		μA

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
PWDN Pin						
t_{ON}	Turn-on Time	50% TTL to 90% P_{OUT}		0.6		μs
t_{OFF}	Turn-off Time	50% TTL to 10% P_{OUT}		1.4		μs

6.7 Typical Characteristics



Typical Characteristics (continued)

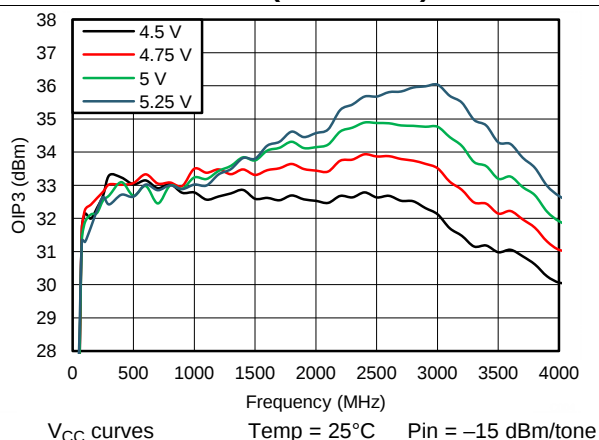


Figure 7. OIP3 vs Frequency

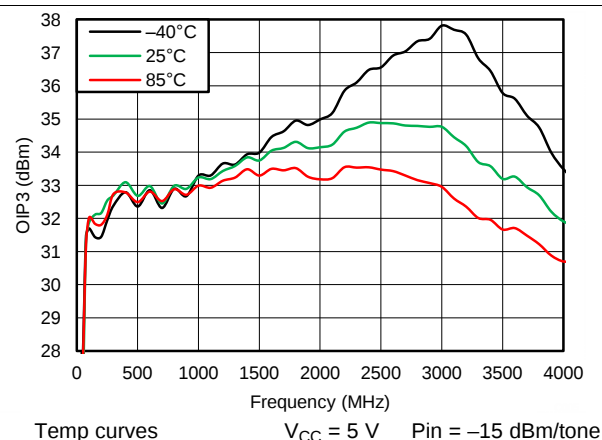


Figure 8. OIP3 vs Frequency

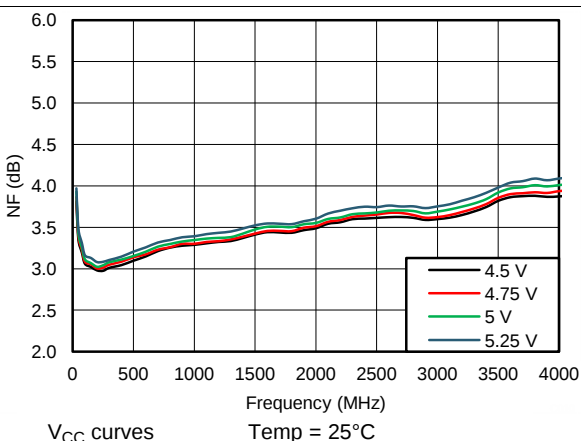


Figure 9. NF vs Frequency

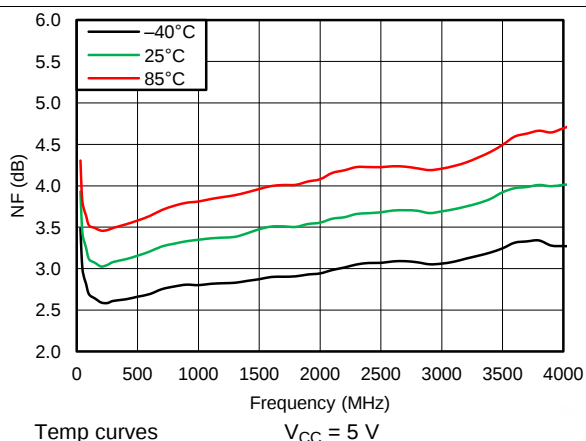


Figure 10. NF vs Frequency

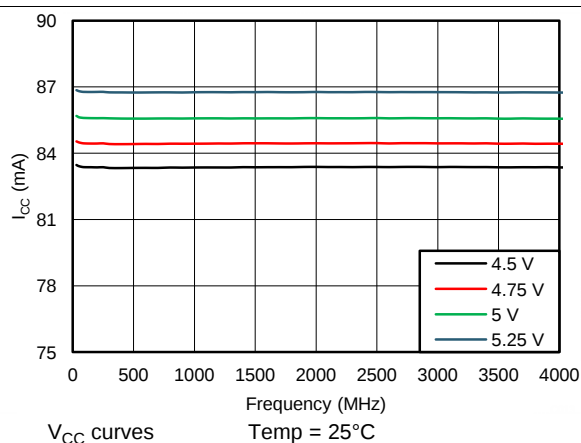


Figure 11. I_{CC} vs Frequency

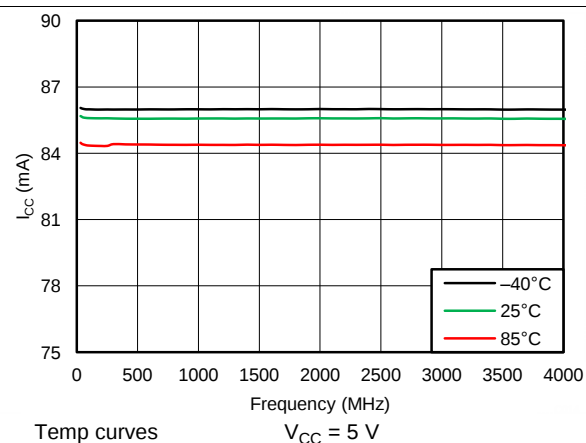


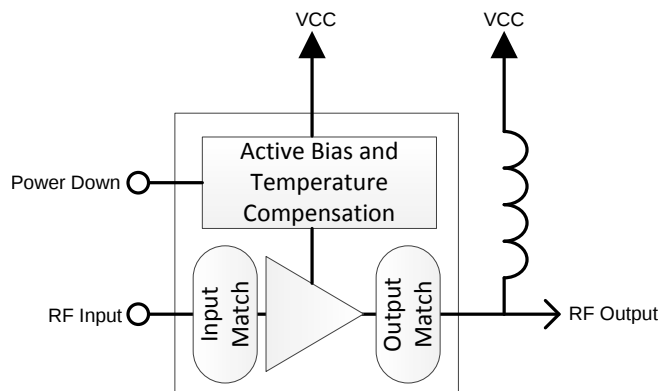
Figure 12. I_{CC} vs Frequency

7 Detailed Description

7.1 Overview

The device is a 5 V general purpose RF gain block. It is a SiGe Darlington amplifier with integrated 50 Ω input and output matching. The device contains an active bias circuit to maintain performance over a wide temperature and voltage range. The included power down function allows the amplifier to shut down saving power when the amplifier is not needed. Fast shut down and start up enable the amplifier to be used in a host of time division duplex applications.

7.2 Functional Block Diagram



7.3 Feature Description

The TRF37C75 is a fixed gain RF amplifier. It is internally matched to 50 Ω on both the input and output. It is a fully cascable general purpose amplifier. The included active bias circuitry ensures the amplifier performance is optimized over the full operating temperature and voltage ranges.

7.4 Device Functional Modes

7.4.1 Power Down

The TRF37C75 PWDN pin can be left unconnected for normal operation or a logic-high for disable mode operation. For applications that use the power down mode, normal 5 V TLL levels are supported.

8 Applications and Implementation

8.1 Application Information

The TRF37C75 is a wideband high performance general purpose RF amplifier. To maximize its performance, good RF layout and grounding techniques should be employed.

8.2 Typical Application

The TRF37C75 device is typically placed in a system as illustrated in [Figure 13](#).

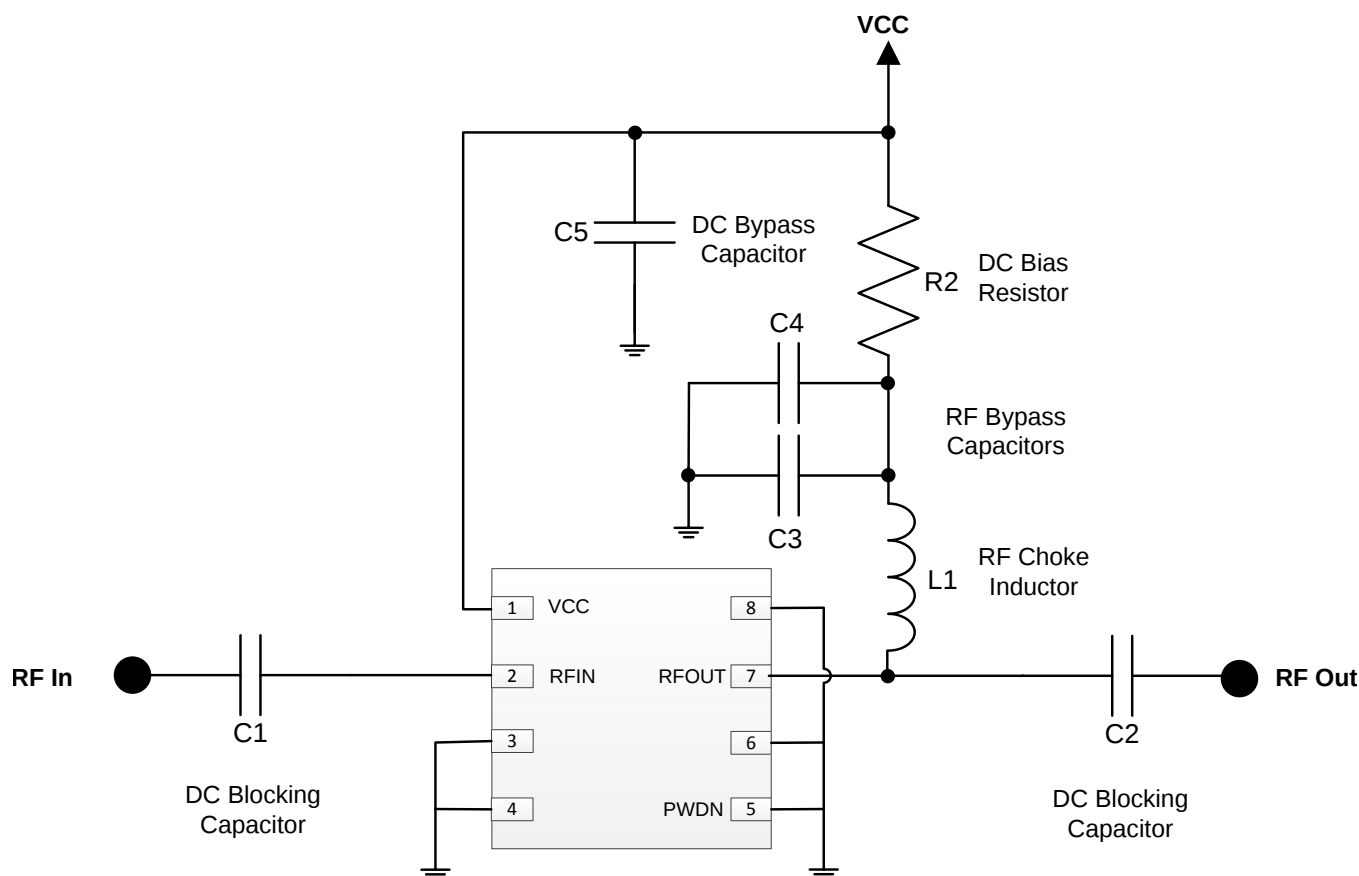


Figure 13. Typical Application Schematic for TRF37C75

8.2.1 Design Requirements

Table 1. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input power range	< 3 dBm
Output power	< 18 dBm
Operating frequency range	40 — 4000 MHz

8.2.2 Detailed Design Procedure

The TRF37C75 is a simple to use internally matched and cascable RF amplifier. Following the recommended RF layout with good quality RF components and local DC bypass capacitors will ensure optimal performance is achieved. TI provides various support materials including S-Parameter and ADS models to allow the design to be optimized to the user's particular performance needs.

8.2.3 Application Curves

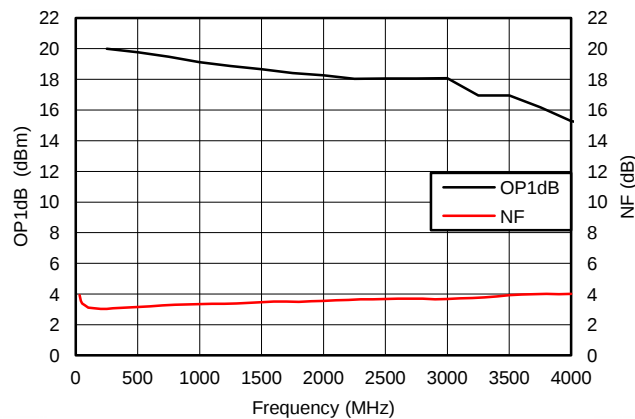


Figure 14. OP1dB and NF vs Frequency

9 Power Supply Recommendations

All supplies may be generated from a common nominal 5 V source but should be isolated through decoupling capacitors placed close to the device. The typical application schematic in [Figure 13](#) is an excellent example. Select capacitors with self-resonant frequency near the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device. Expensive tantalum capacitors are not needed for optimal performance.

10 Layout

10.1 Layout Guidelines

Good layout practice helps to enable excellent linearity and isolation performance. An example of good layout is shown in Figure 15. In the example, only the top signal layer and its adjacent ground reference plane are shown.

- Excellent electrical connection from the PowerPAD™ to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include solder mask under the pad.
- Connect pad ground to device terminal ground on the top board layer.
- Verify that the return DC and RF current path have a low impedance ground plane directly under the package and RF signal traces into and out of the amplifier.
- Ensure that ground planes on the top and any internal layers are well stitched with vias.
- Do not route RF signal lines over breaks in the reference ground plane.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes. Ground is the best reference, although clean power planes can serve where necessary.
- Place supply decoupling close to the device.

10.2 Layout Example

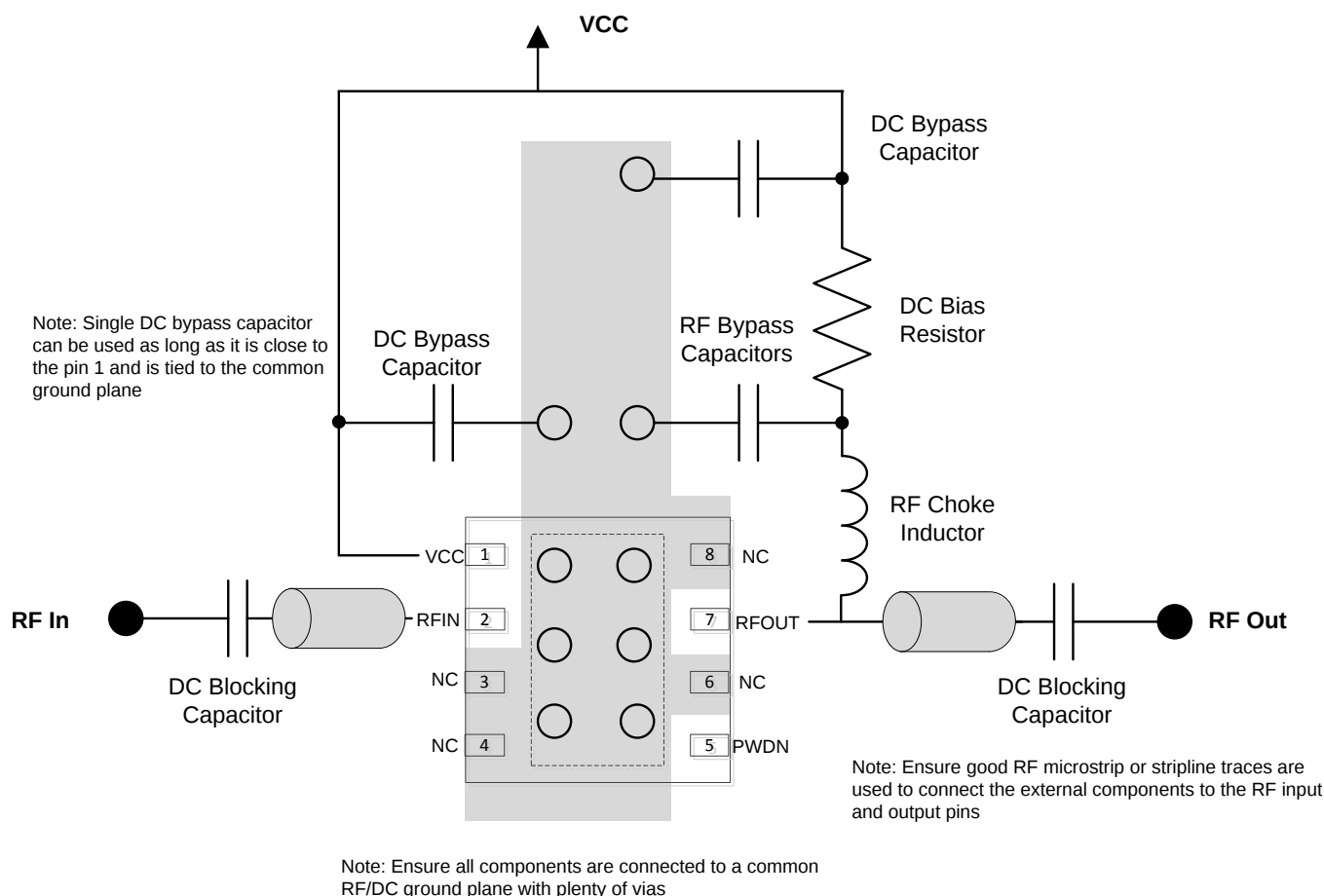


Figure 15. Layout

11 器件和文档支持

11.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用的 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568 号, 中建大厦32 楼邮政编码: 200122
Copyright © 2014, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF37C75IDSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C75I	Samples
TRF37C75IDSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C75I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

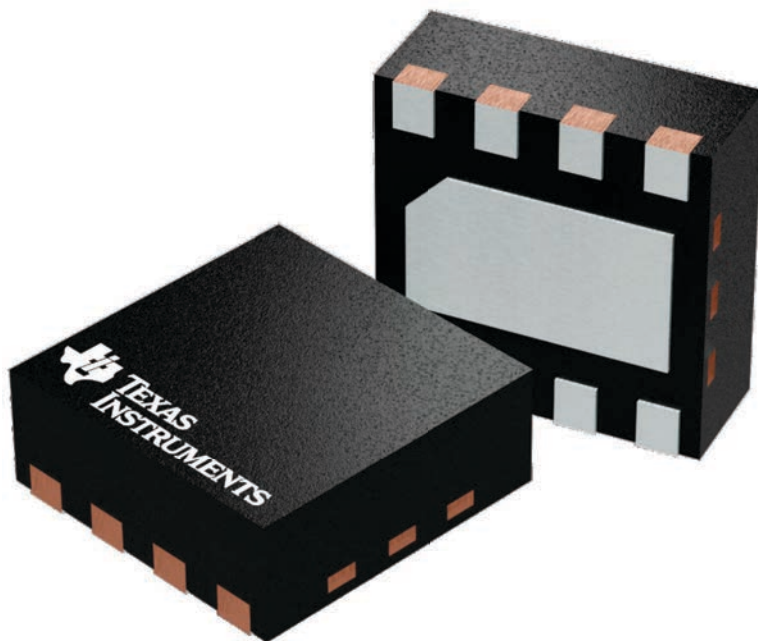
DSG 8

WSON - 0.8 mm max height

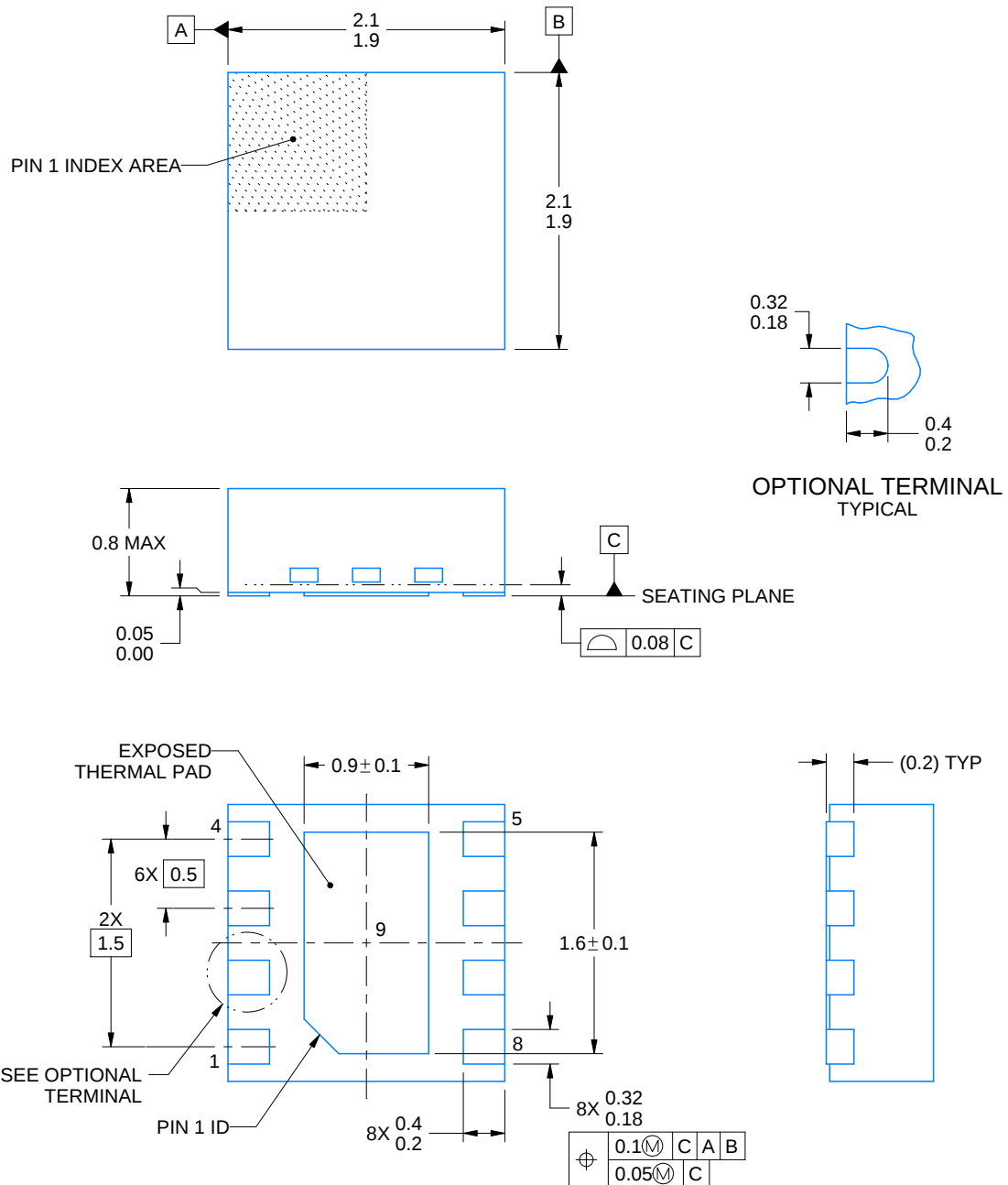
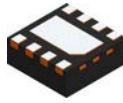
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A



4218900/C 04/2019

NOTES:

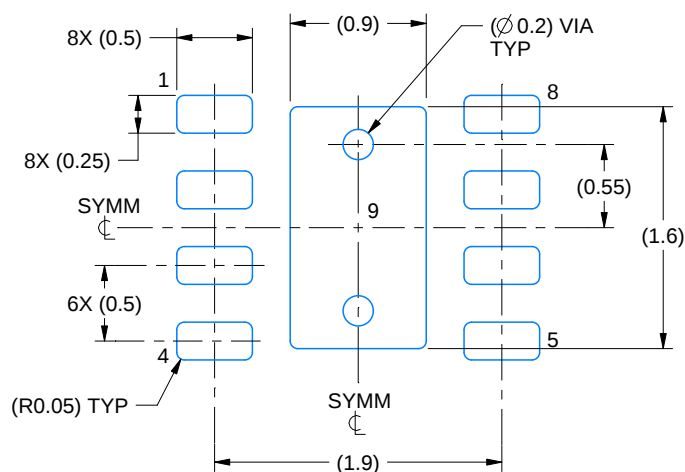
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

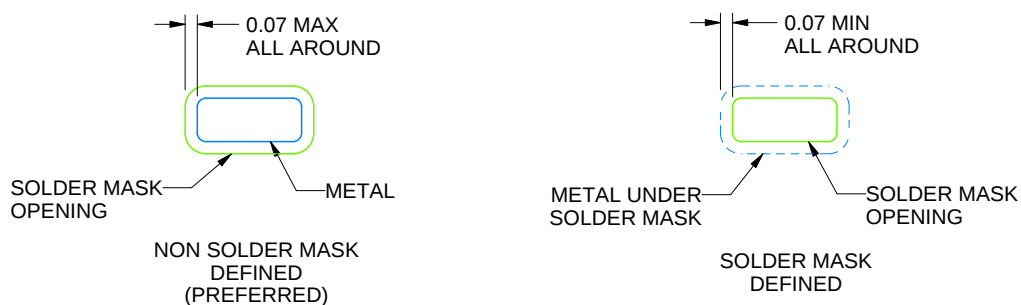
DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

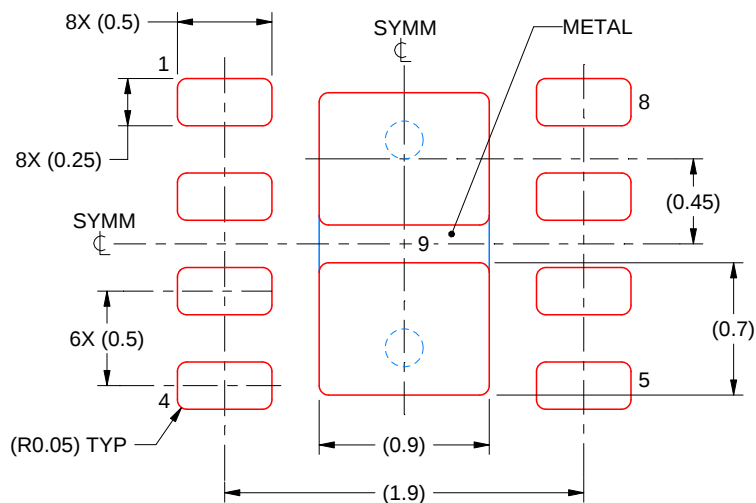
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司