

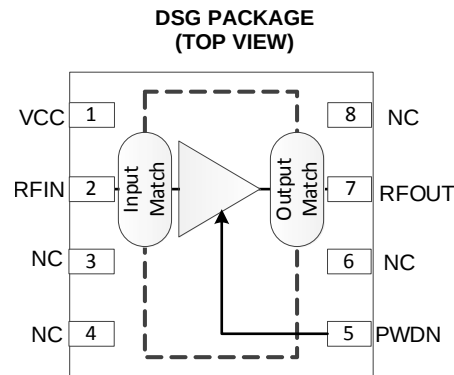
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4 修订历史记录

日期	修订版本	注释
2014 年 5 月	*	最初发布。

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
VCC	1	DC Bias.
RFIN	2	RF input. Connect to an RF source through a DC-blocking capacitor. Internally matched to 50 Ω .
NC	3, 4, 6, 8	No electrical connection. Connect pad to GND for board level reliability integrity.
PWDN	5	When high the device is in power down state. When LOW or NC the device is in active state. Internal pulldown resistor to GND.
RFOUT	7	RF Output and DC Bias (V_{CC}). Connect to DC supply through an RF choke inductor. Connect to output load through a DC-blocking capacitor. Internally matched to 50 Ω .
GND	PowerPAD™	RF and DC GND. Connect to PCB ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply Input voltage		–0.3	6	V
Input Power	With recommended R _{bias} resistor		10	dBm
Operating virtual junction temperature range		–40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T _{STG}	Storage temperature range		–65	150	°C
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	–1	1	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	–1	1	kV

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage, V _{CC}	4.5	5	5.25	V
Operating junction temperature, T _J	–40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DSG	UNIT
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	79.3	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	110	
R _{θJB}	Junction-to-board thermal resistance	49	
ψ _{JT}	Junction-to-top characterization parameter	6	
ψ _{JB}	Junction-to-board characterization parameter	49.4	
R _{θJCbott}	Junction-to-case (bottom) thermal resistance	19.2	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $PWDN = \text{Low}$, $R_{BIAS} = 3.9\ \Omega$, $L_{OUT} = 100\text{ nH}$, $C1 = C2 = 1000\text{ pF}$, $Z_S = Z_L = 50\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Parameters						
I_{CC}	Total supply current			85		mA
	Power down current	$PWDN = \text{High}$		125		μA
P_{diss}	Power dissipation			0.425		W
RF Frequency Range						
	Frequency range		40		4000	MHz
G	Small signal gain	$f_{RF} = 400\text{ MHz}$		15.5		dB
		$f_{RF} = 2000\text{ MHz}$		14.75		dB
		$f_{RF} = 3000\text{ MHz}$		14.75		dB
		$f_{RF} = 4000\text{ MHz}$		14.75		dB
OP1dB	Output 1dB compression point	At 2000 MHz		17.5		dBm
OIP3	Output 3rd order intercept point	At 2000 MHz, 2-tone 10 MHz apart		32.5		dBm
NF	Noise figure	At 2000 MHz		3.8		dB
$R_{(LI)}$	Input return loss			19		dB
$R_{(LO)}$	Output return loss			12		dB
PWDN Pin						
V_{IH}	High level input level		2			V
V_{IL}	Low level input level				0.8	V
I_{IH}	High level input current			30		μA
I_{IL}	Low level input current			1		μA

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
PWDN Pin						
t_{ON}	Turn-on Time	50% TTL to 90% P_{OUT}		0.6		μs
t_{OFF}	Turn-off Time	50% TTL to 10% P_{OUT}		1.4		μs

6.7 Typical Characteristics

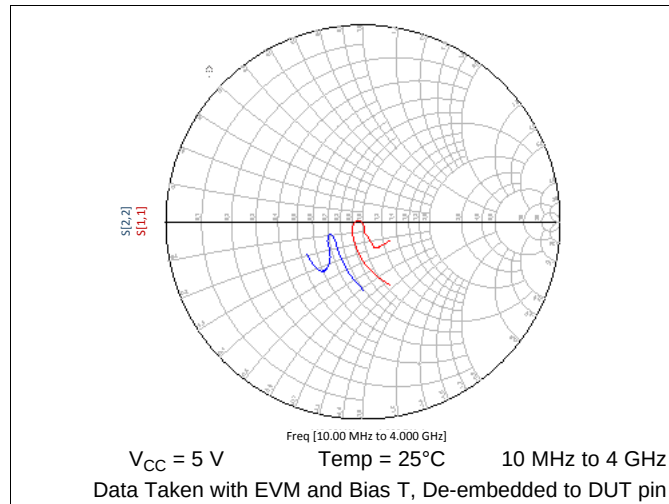


Figure 1. Smith Chart – S11, S22

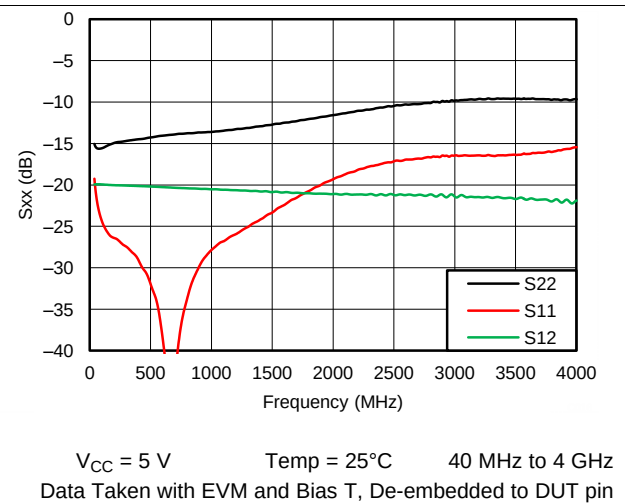


Figure 2. S22, S11, S12

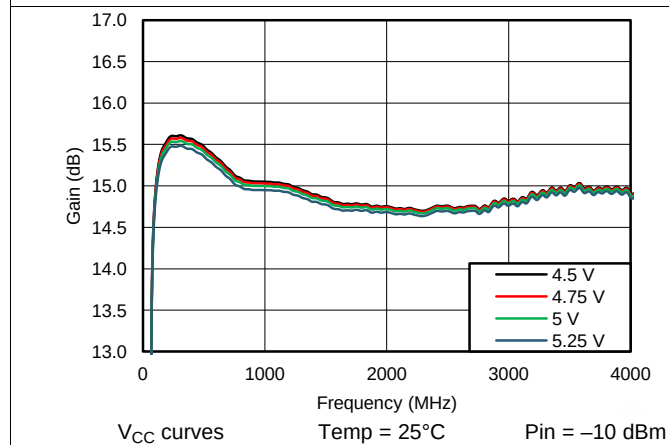


Figure 3. Gain vs Frequency

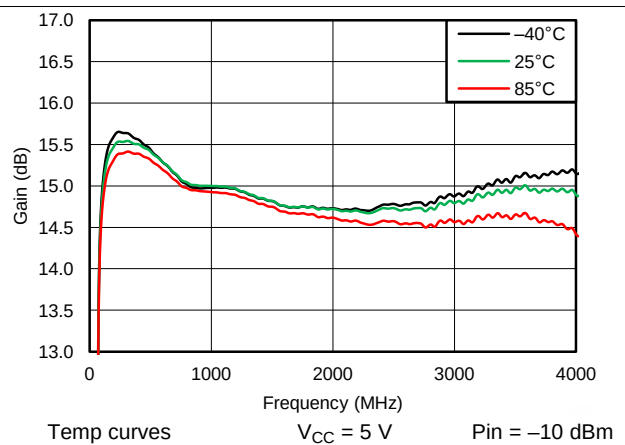


Figure 4. Gain vs Frequency

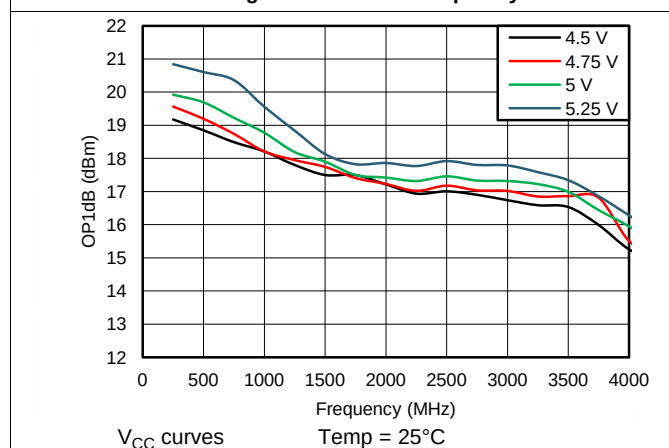


Figure 5. OP1dB vs Frequency

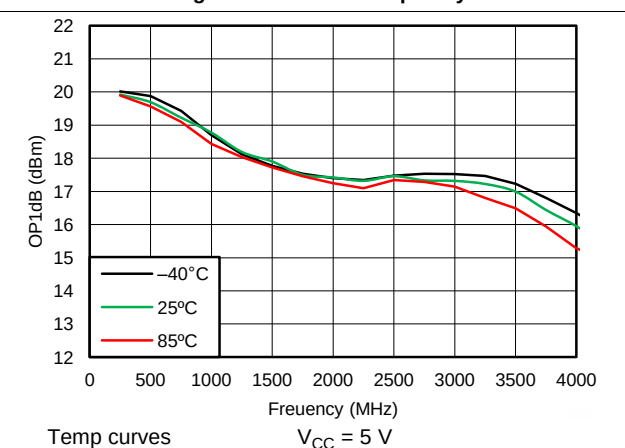


Figure 6. OP1dB vs Frequency

Typical Characteristics (continued)

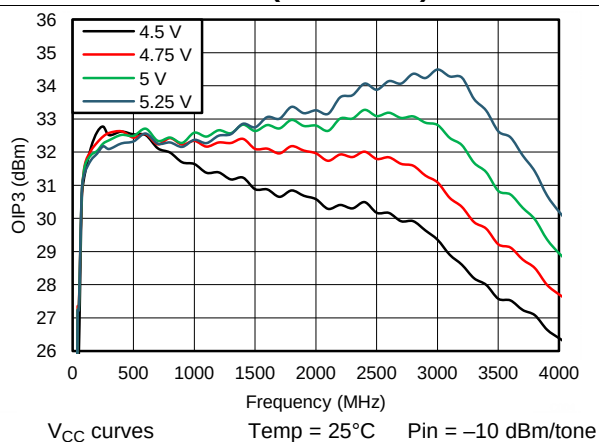


Figure 7. OIP3 vs Frequency

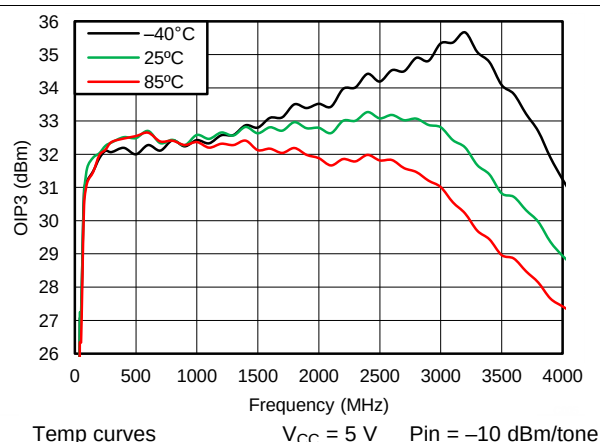


Figure 8. OIP3 vs Frequency

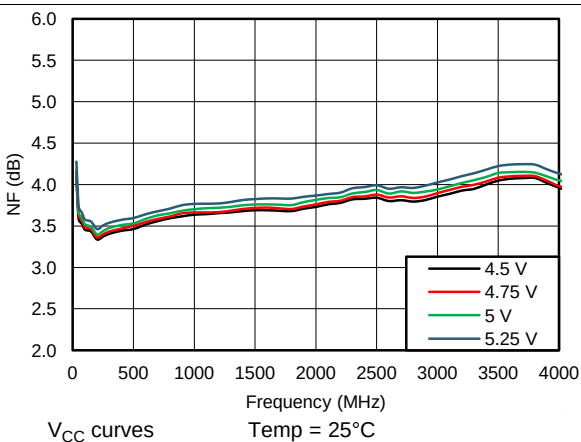


Figure 9. NF vs Frequency

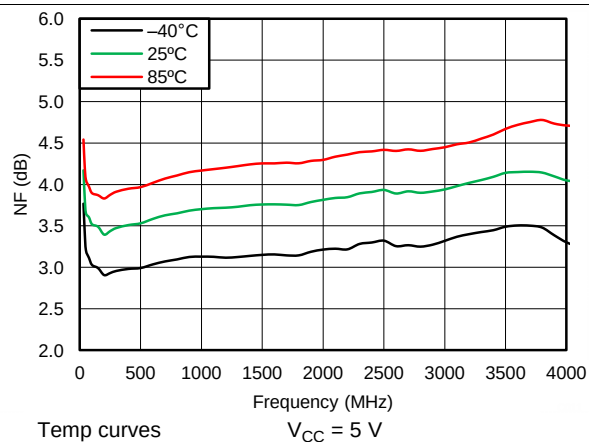


Figure 10. NF vs Frequency

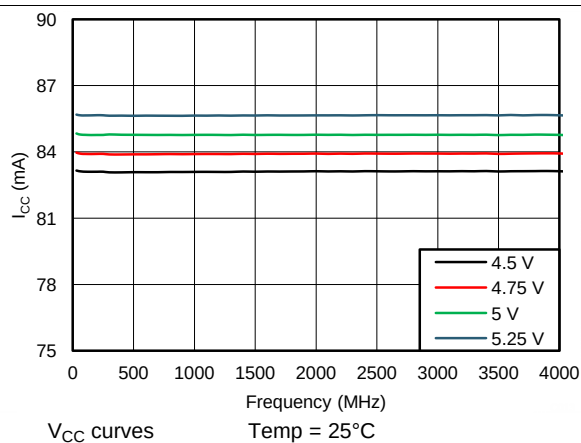


Figure 11. I_{CC} vs Frequency

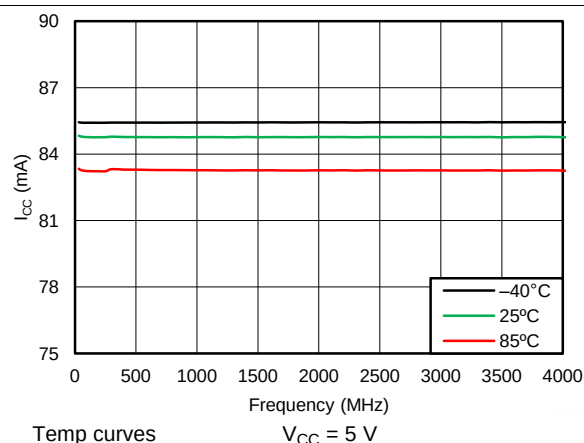


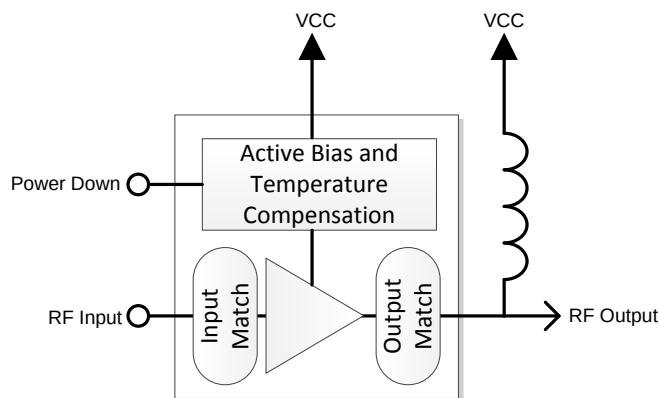
Figure 12. I_{CC} vs Frequency

7 Detailed Description

7.1 Overview

The device is a 5 V general purpose RF gain block. It is a SiGe Darlington amplifier with integrated 50 Ω input and output matching. The device contains an active bias circuit to maintain performance over a wide temperature and voltage range. The included power down function allows the amplifier to shut down saving power when the amplifier is not needed. Fast shut down and start up enable the amplifier to be used in a host of time division duplex applications.

7.2 Functional Block Diagram



7.3 Feature Description

The TRF37B75 is a fixed gain RF amplifier. It is internally matched to 50 Ω on both the input and output. It is a fully cascadable general purpose amplifier. The included active bias circuitry ensures the amplifier performance is optimized over the full operating temperature and voltage ranges.

7.4 Device Functional Modes

7.4.1 Power Down

The TRF37B75 PWDN pin can be left unconnected for normal operation or a logic-high for disable mode operation. For applications that use the power down mode, normal 5 V TLL levels are supported.

8 Applications and Implementation

8.1 Application Information

The TRF37B75 is a wideband high performance general purpose RF amplifier. To maximize its performance, good RF layout and grounding techniques should be employed.

8.2 Typical Application

The TRF37B75 device is typically placed in a system as illustrated in [Figure 13](#).

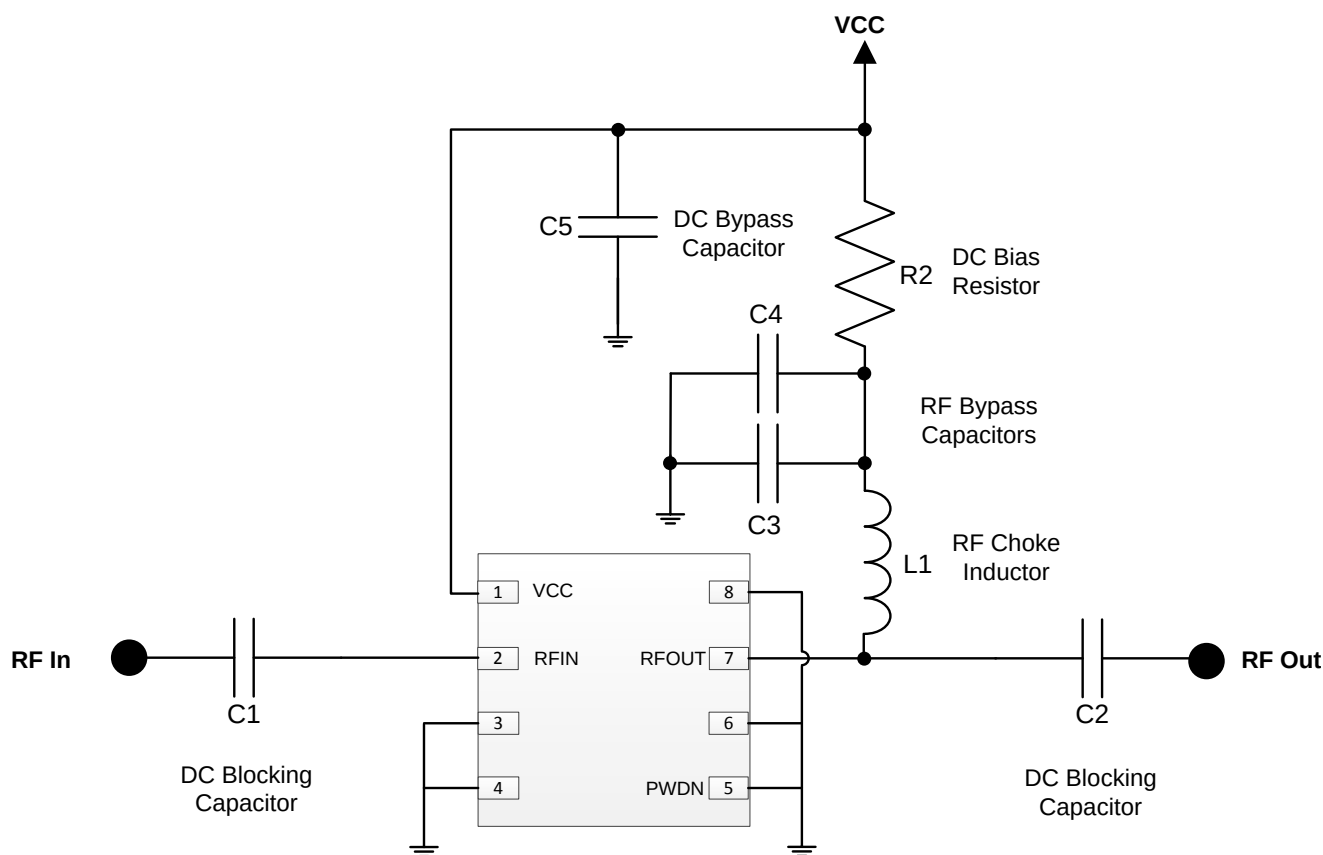


Figure 13. Typical Application Schematic for TRF37B75

8.2.1 Design Requirements

Table 1. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input power range	< 3 dBm
Output power	< 18 dBm
Operating frequency range	40 — 4000 MHz

8.2.2 Detailed Design Procedure

The TRF37B75 is a simple to use internally matched and cascable RF amplifier. Following the recommended RF layout with good quality RF components and local DC bypass capacitors will ensure optimal performance is achieved. TI provides various support materials including S-Parameter and ADS models to allow the design to be optimized to the user's particular performance needs.

8.2.3 Application Curve

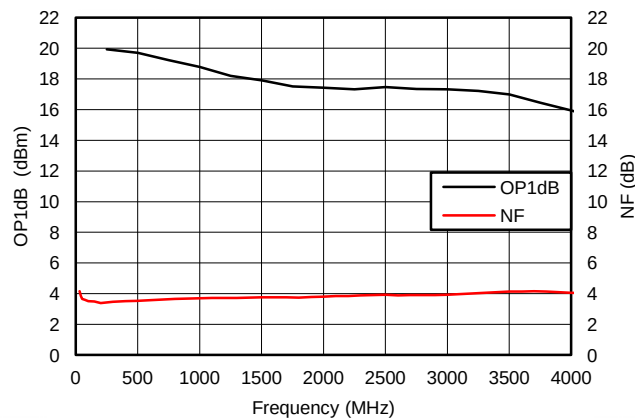


Figure 14. OP1dB and NF vs Frequency

9 Power Supply Recommendations

All supplies may be generated from a common nominal 5 V source but should be isolated through decoupling capacitors placed close to the device. The typical application schematic in [Figure 13](#) is an excellent example. Select capacitors with self-resonant frequency near the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device. Expensive tantalum capacitors are not needed for optimal performance.

10 Layout

10.1 Layout Guidelines

Good layout practice helps to enable excellent linearity and isolation performance. An example of good layout is shown in Figure 15. In the example, only the top signal layer and its adjacent ground reference plane are shown.

- Excellent electrical connection from the PowerPAD™ to the board ground is essential. Use the recommended footprint, solder the pad to the board, and do not include solder mask under the pad.
- Connect pad ground to device terminal ground on the top board layer.
- Verify that the return DC and RF current path have a low impedance ground plane directly under the package and RF signal traces into and out of the amplifier.
- Ensure that ground planes on the top and any internal layers are well stitched with vias.
- Do not route RF signal lines over breaks in the reference ground plane.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes. Ground is the best reference, although clean power planes can serve where necessary.
- Place supply decoupling close to the device.

10.2 Layout Example

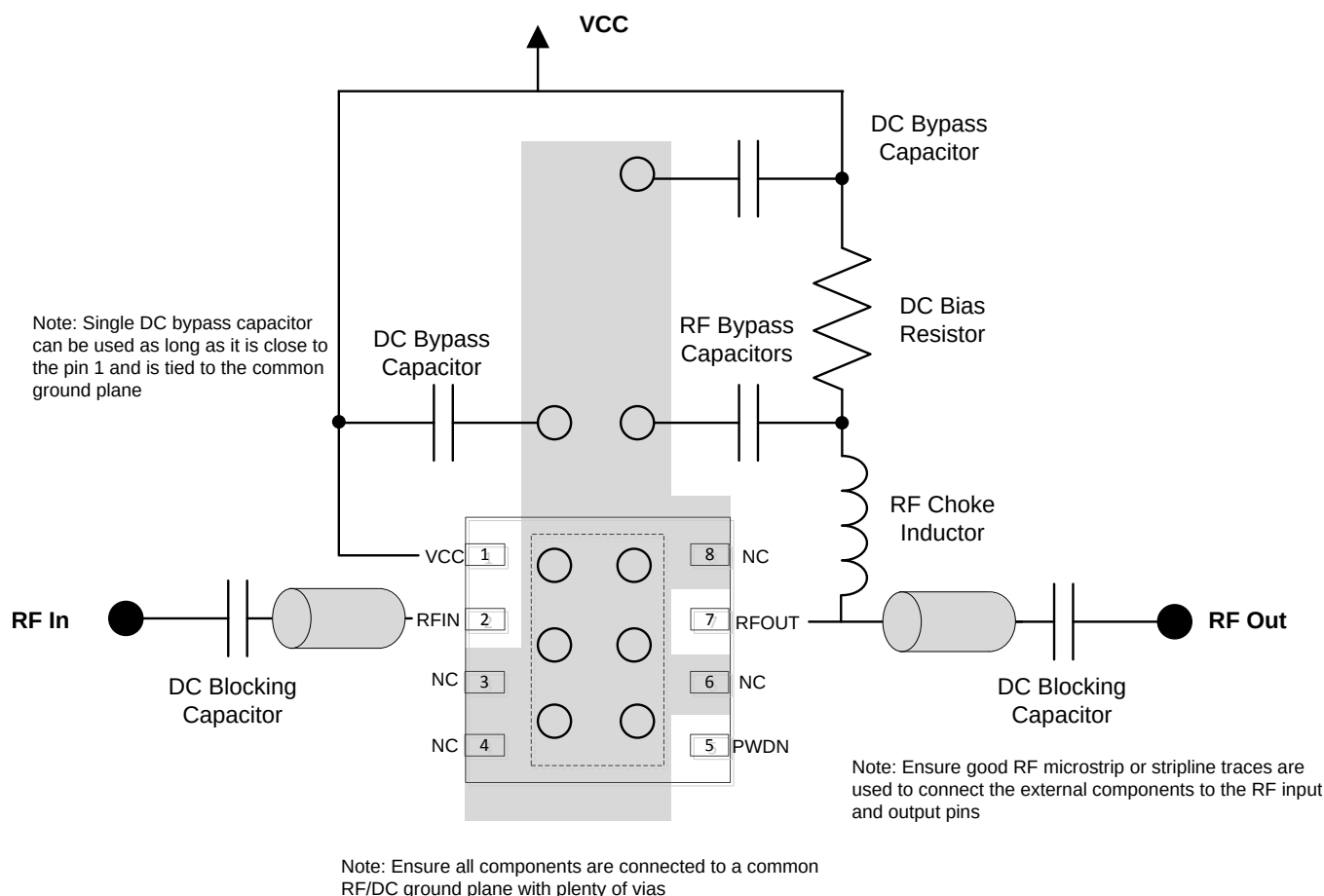


Figure 15. Layout

11 器件和文档支持

11.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF37B75IDSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B75I	Samples
TRF37B75IDSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B75I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

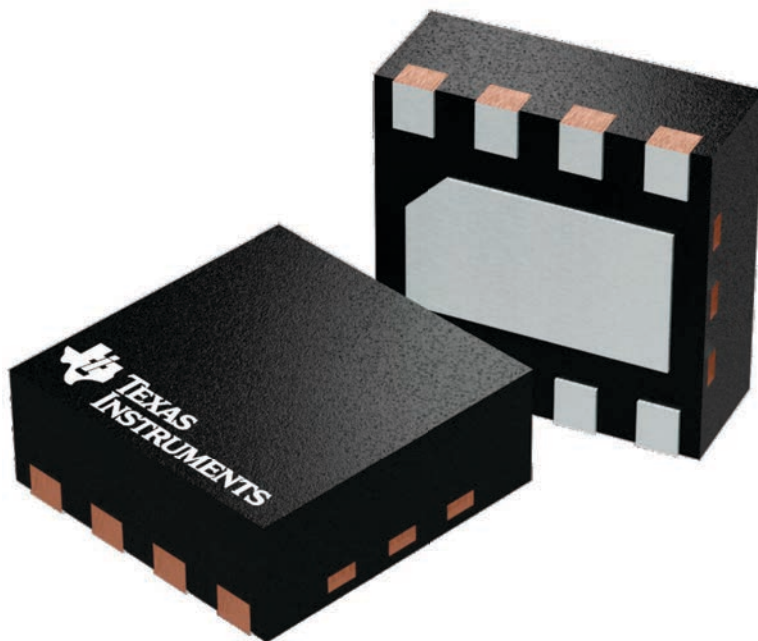
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



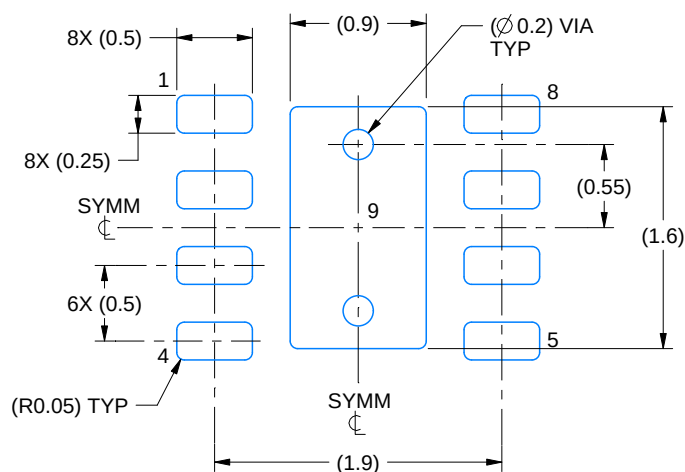
4224783/A

EXAMPLE BOARD LAYOUT

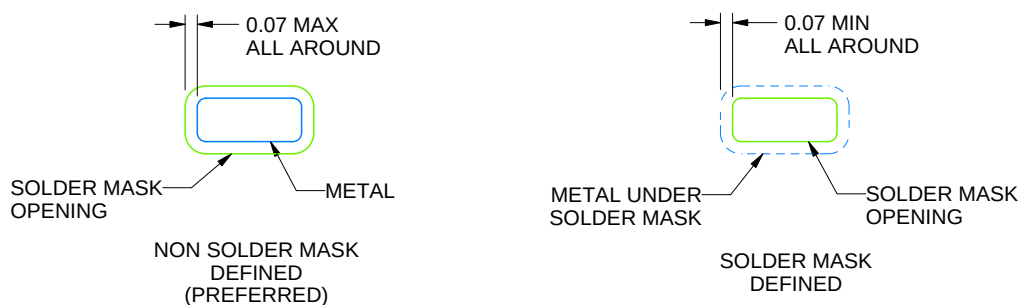
DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

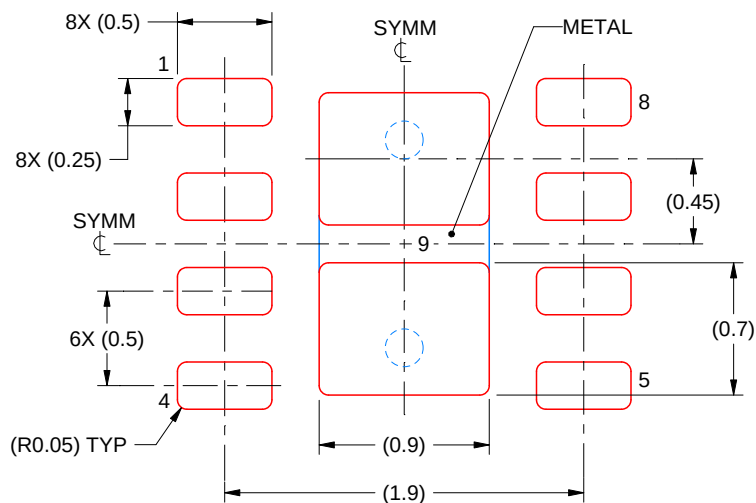
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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