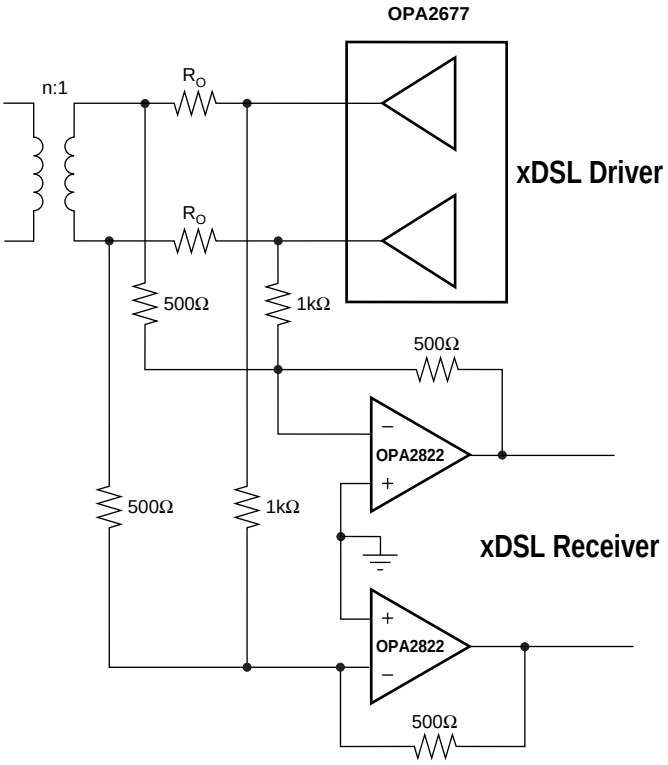
Dual, Wideband, Low-Noise Operational Amplifier

FEATURES

- LOW INPUT NOISE VOLTAGE: 2.0nV/√Hz
- HIGH UNITY GAIN BANDWIDTH: 500MHz
- HIGH GAIN BANDWIDTH PRODUCT: 240MHz
- HIGH OUTPUT CURRENT: 90mA
- SINGLE +5V TO +12V OPERATION
- LOW SUPPLY CURRENT: 4.8mA/ch

APPLICATIONS

- xDSL DIFFERENTIAL LINE RECEIVERS
- HIGH DYNAMIC RANGE ADC DRIVERS
- LOW NOISE PLL INTEGRATORS
- TRANSIMPEDANCE AMPLIFIERS
- PRECISION BASEBAND I/Q AMPLIFIERS
- ACTIVE FILTERS



DESCRIPTION

The OPA2822 offers very low 2.0nV/√Hz input noise in a wideband, unity-gain stable, voltage-feedback architecture. Intended for xDSL receiver applications, the OPA2822 also supports this low input noise with exceptionally low harmonic distortion, particularly in differential configurations. Adequate output current is provided to drive the potentially heavy load of a passive filter between this amplifier and the codec. Harmonic distortion for a $2V_{PP}$ differential output operating from +5V to +12V supplies is ≤ –100dBc through 1MHz input frequencies. Operating on a low 4.8mA/ch supply current, the OPA2822 can satisfy all xDSL receiver requirements over a wide range of possible supply voltages—from a single +5V condition, to ±5V, up to a single +12V design.

General-purpose applications on a single +5V supply will benefit from the high input and output voltage swing available on this reduced supply voltage. Low-cost precision integrators for PLLs will also benefit from the low voltage noise and offset voltage. Baseband I/Q receiver channels can achieve almost perfect channel match with noise and distortion to support signals through 5MHz with > 14-bit dynamic range.

OPA2822 RELATED PRODUCTS

FEATURES	SINGLES	DUALS	TRIPLES
High Slew Rate	OPA690	OPA2690	OPA3690
R/R Input/Output	OPA353	OPA2353	—
1.3nV Input Noise	OPA846	OPA2686	—
1.5nV Input Noise	—	THS6062	—

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2822U	SO-8 Surface-Mount	D	–40°C to +85°C	OPA2822U	OPA2822U	Rails, 100
"	"	"	"	"	OPA2822U/2K5	Tape and Reel, 2500
OPA2822E	MSOP-8 Surface-Mount	DGK	–40°C to +85°C	D22	OPA2822E/250	Tape and Reel, 250
"	"	"	"	"	OPA2822E/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range	–65°C to +125°C
Lead Temperature (SO-8)	+260°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	200V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

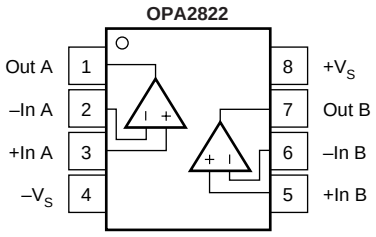
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Texas Instruments recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

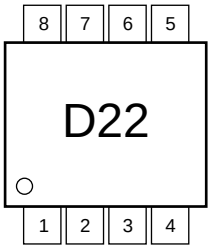
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION / MSOP PACKING MARKING

Top View **SO**



MSOP PACKAGE MARKING



ELECTRICAL CHARACTERISTICS: $V_S = \pm 6V$

Boldface limits are tested at **+25°C.**

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA2822U, E						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	G = +1, $V_O = 0.1V_{PP}$, $R_F = 0\Omega$	400				MHz	typ	C
	G = +2, $V_O = 0.1V_{PP}$	200	120	110	105	MHz	min	B
	G = +10, $V_O = 0.1V_{PP}$	24	15	13	12	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	240	150	130	125	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O < 0.1V_{PP}$	16				MHz	typ	C
Peaking at a Gain of +1	$V_O < 0.1V_{PP}$	5				dB	typ	C
Large-Signal Bandwidth	G = +2, $V_O = 2V_{PP}$	27				MHz	typ	C
Slew Rate	G = +2, 4V Step	170	110	105	100	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.2V Step	1.5				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	35				ns	typ	C
0.1%	G = +2, V_O = 2V Step	32				ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 200\Omega$	–91	–88	–87	–86	dBc	max	B
	$R_L \geq 500\Omega$	–95	–91	–90	–89	dBc	max	B
3rd-Harmonic	$R_L = 200\Omega$	–100	–95	–92	–91	dBc	max	B
	$R_L \geq 500\Omega$	–105	–99	–96	–95	dBc	max	B
Input Voltage Noise	f > 10kHz	2.0	2.2	2.3	2.5	nV/√Hz	max	B
Input Current Noise	f > 10kHz	1.6	2.0	2.1	2.3	pA/√Hz	max	B
Differential Gain	G = +2, PAL, V_O = 1.4Vp, $R_L = 150$	0.02				%	typ	C
Differential Phase	G = +2, PAL, V_O = 1.4Vp, $R_L = 150$	0.03				deg	typ	C
Channel-to-Channel Crosstalk	f = 1MHz, Input Referred	–95				dBc	typ	C
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, $R_L = 100\Omega$	100	**85**	82	80	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.2	**±1.2**	±1.4	±1.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			5	5	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	–9	**–18**	–19	–21	µA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 0V			50	50	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±100	**±400**	±600	±700	nA	max	A
Average Offset Current Drift	V_{CM} = 0V			5	5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±4.8	**±4.5**	±4.4	±4.4	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V	110	**85**	82	80	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0	18 ‖ 0.6				kΩ ‖ pF	typ	C
Common-Mode	V_{CM} = 0	7 ‖ 1				MΩ ‖ pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.9	**±4.7**	±4.6	±4.6	V	min	A
	100Ω Load	±4.7	**±4.5**	±4.4	±4.4	V	min	A
Current Output, Sourcing	V_O = 0, Linear Operation	+150	**+90**	+85	+80	mA	min	A
Current Output, Sinking	V_O = 0, Linear Operation	–150	**–90**	–85	–80	mA	min	A
Short-Circuit Current	Output Shorted to Ground	220				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.01				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±6				V	typ	C
Maximum Operating Voltage Range			**±6.3**	±6.3	±6.3	V	max	A
Max Quiescent Current	V_S = ±6V, both channels	9.6	**11.8**	11.9	12.0	mA	max	A
Min Quiescent Current	V_S = ±6V, both channels	9.6	**8.2**	8.1	8.0	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	95	**85**	82	80	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range U, E Package		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U SO-8		125				°C/W	typ	C
E MSOP		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications.

(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature tested specifications.

(3) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.

(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 402Ω, R_L = 100Ω to V_S/2, and G = +2, (see Figure 3 for AC performance only), unless otherwise noted.

		OPA2822U, E						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth	G = +1, V_O = 0.1V_{PP}, R_F = 0Ω	350				MHz	typ	C
	G = +2, V_O = 0.1V_{PP}	180	105	102	100	MHz	min	B
	G = +10, V_O = 0.1V_{PP}	20	13	11	10	MHz	min	B
Gain-Bandwidth Product	G > 20	200	130	110	105	MHz	min	B
Peaking at a Gain of +1	V_O < 0.1V_{PP}	6				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	20				MHz	typ	C
Slew Rate	G = +2, 2V Step	120	90	85	80	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.2V Step	2.0	2.7	3.2	3.3	ns	max	B
Settling Time to 0.02%	G = +2, V_O = 2V Step	40				ns	typ	C
0.1%	G = +2, V_O = 2V Step	38				ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 200Ω to V_S/2	–85	–82	–81	–80	dBc	max	B
	R_L = 500Ω to V_S/2	–87	–83	–82	–81	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–99	–94	–91	–90	dBc	max	B
	R_L = 1500Ω to V_S/2	–103	–98	–95	–94	dBc	max	B
Input Voltage Noise	f > 1MHz	2.1	2.3	2.4	2.6	nV/$\sqrt{Hz}$	max	B
Input Current Noise	f > 1MHz	1.5	1.9	2.0	2.1	pA/$\sqrt{Hz}$	max	B
DC PERFORMANCE[4]								
Open-Loop Voltage Gain	V_O = 0V, R_L = 200Ω to 2.5V	90	**81**	78	76	dB	min	A
Input Offset Voltage	V_{CM} = 2.5V	±0.3	**±1.3**	±1.5	±1.6	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			5.5	5.5	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	–8	**–16**	–19	–20	µA	max	A
Average Bias Current Drift	V_{CM} = 2.5V			50	50	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±100	**±400**	±600	±700	nA	max	A
Average Offset Current Drift	V_{CM} = 2.5V			5	5	nA/°C	max	B
INPUT								
Least Positive Input Voltage		1.2	**1.5**	1.6	1.65	V	min	A
Most Positive Input Voltage		3.8	**3.5**	3.4	3.35	V	max	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = +2.5V	110	**85**	82	80	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = +2.5V	15 || 1				kΩ || pF	typ	C
Common-Mode	V_{CM} = +2.5V	5 || 1.3				MΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	3.9	**3.8**	3.6	3.5	V	min	A
	R_L = 100Ω to 2.5V	3.7	**3.5**	3.4	3.35	V	min	A
Least Positive Output Voltage	No Load	1.3	**1.4**	1.5	1.55	V	min	A
	R_L = 100Ω to 2.5V	1.4	**1.5**	1.6	1.65	V	min	A
Current Output, Sourcing		+150	**+90**	+85	+80	mA	min	A
Current Output, Sinking		–150	**–90**	–85	–80	mA	min	A
Short-Circuit Current	Output Shorted to Either Supply	200				mA	typ	C
Closed-Loop Output Impedance	G = +1, f = 100kHz	0.01				Ω	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			**12.6**	12.6	12.6	V	max	A
Max Quiescent Current	V_S = +5V, both channels	8	**10**	10.2	10.4	mA	max	A
Min Quiescent Current	V_S = +5V, both channels	8	**7.2**	7.0	6.9	mA	min	A
Power-Supply Rejection Ratio	Input Referred	90				dB	typ	C
THERMAL CHARACTERISTICS								
Specified Operating Range U, E Package		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U SO-8		125				°C/W	typ	C
E MSOP		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C tested specifications.

(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature tested specifications.

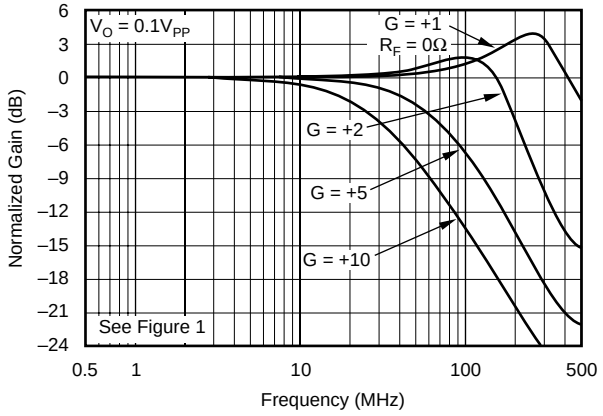
(3) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.

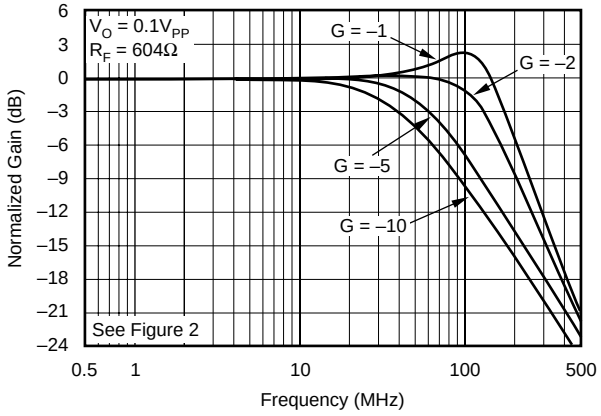
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

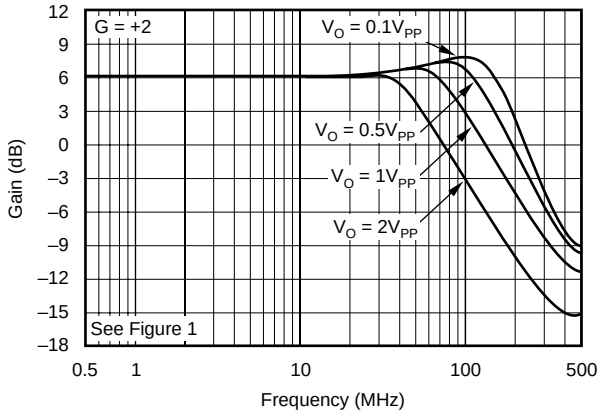
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



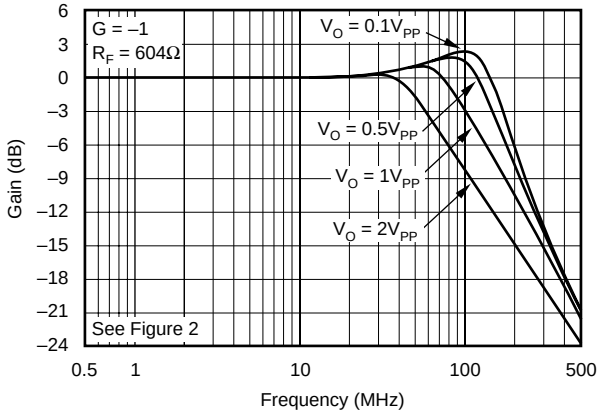
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



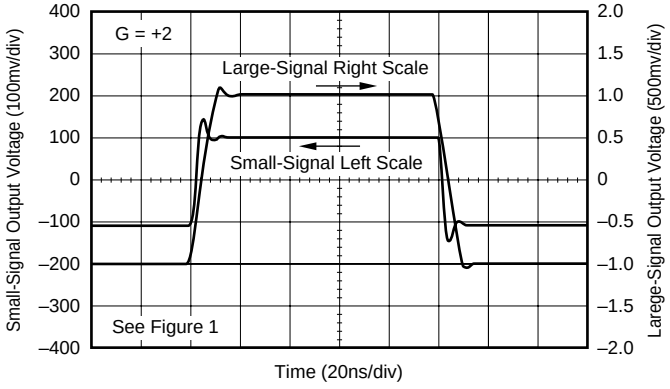
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



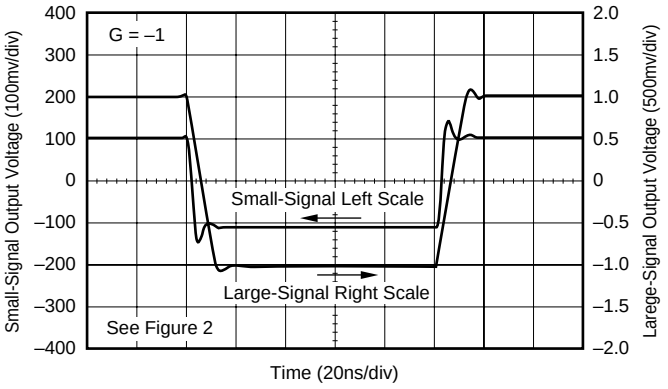
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



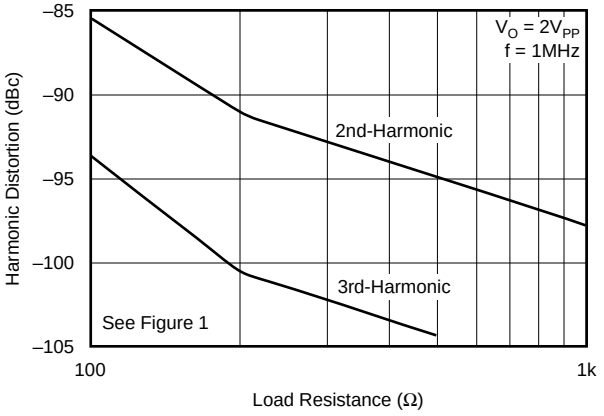
INVERTING PULSE RESPONSE



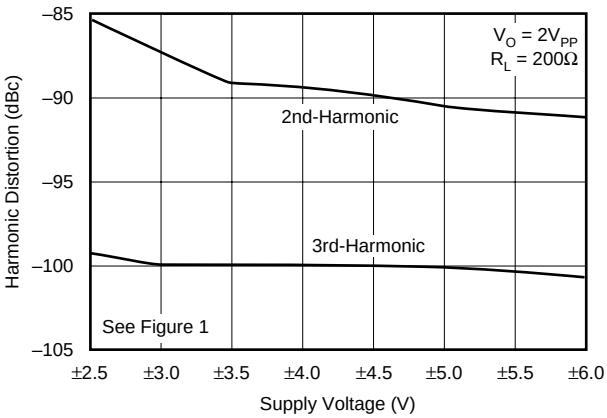
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

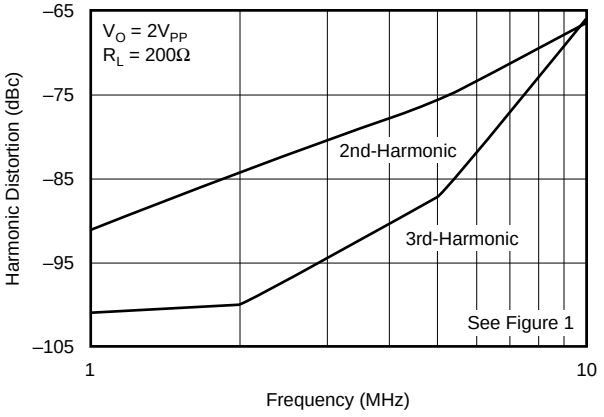
HARMONIC DISTORTION vs LOAD RESISTANCE



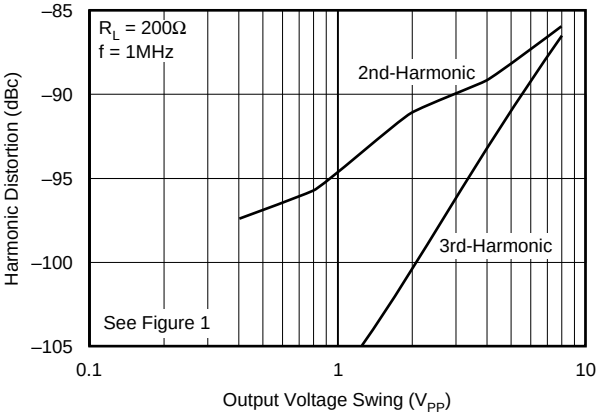
1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



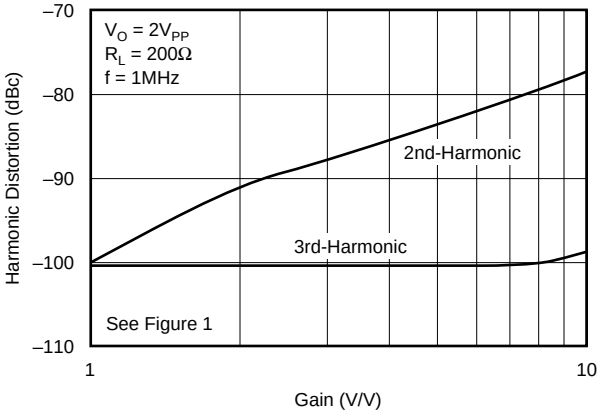
HARMONIC DISTORTION vs FREQUENCY



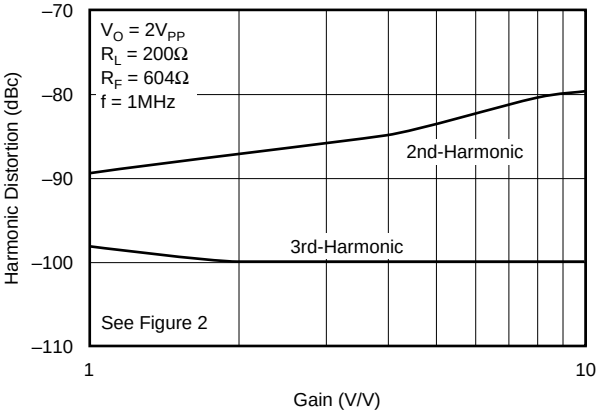
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



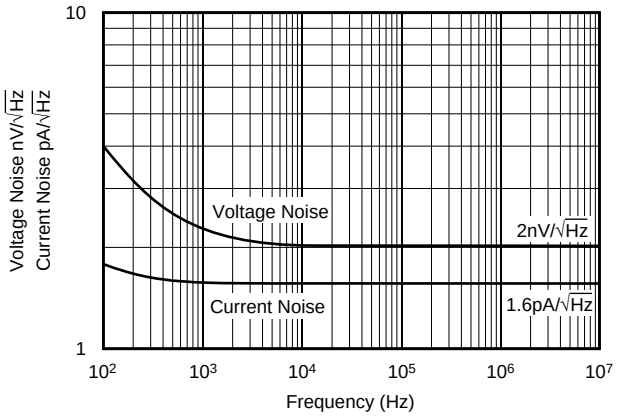
HARMONIC DISTORTION vs INVERTING GAIN



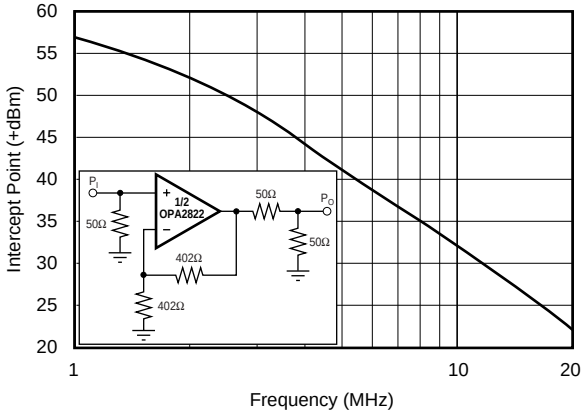
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

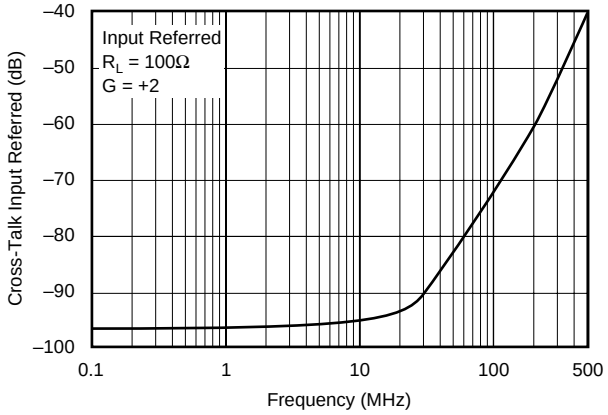
INPUT VOLTAGE AND CURRENT NOISE DENSITY



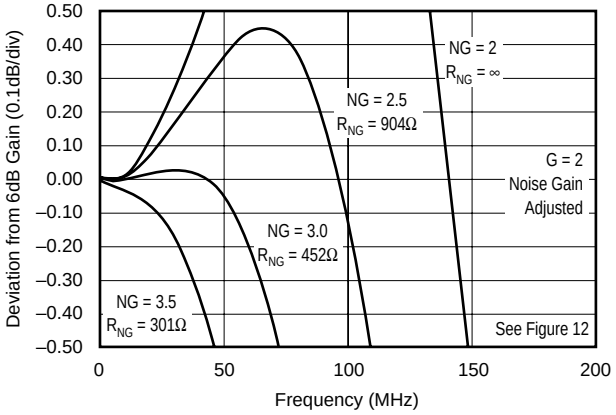
2-TONE, 3rd-ORDER
INTERMODULATION INTERCEPT



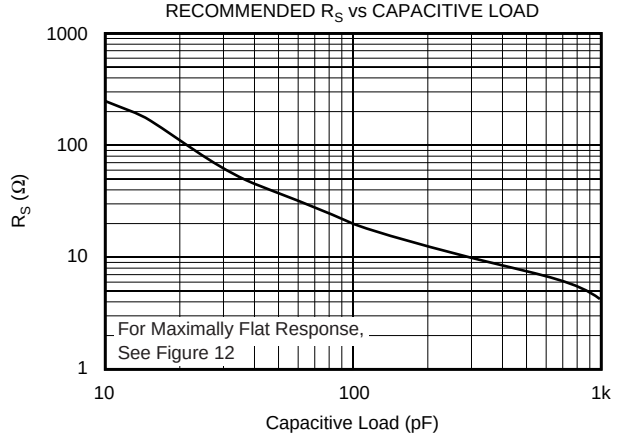
CHANNEL-TO-CHANNEL CROSSTALK



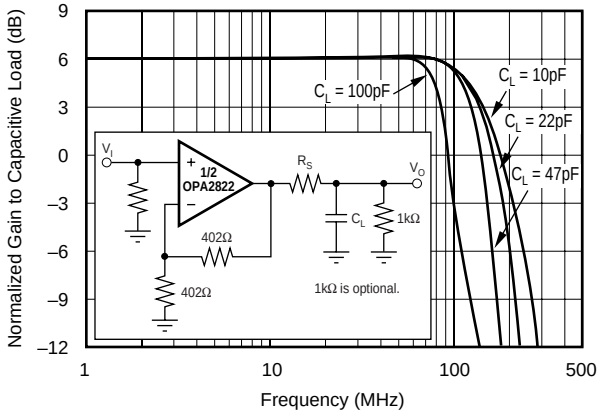
GAIN FLATNESS



RECOMMENDED R_S vs CAPACITIVE LOAD



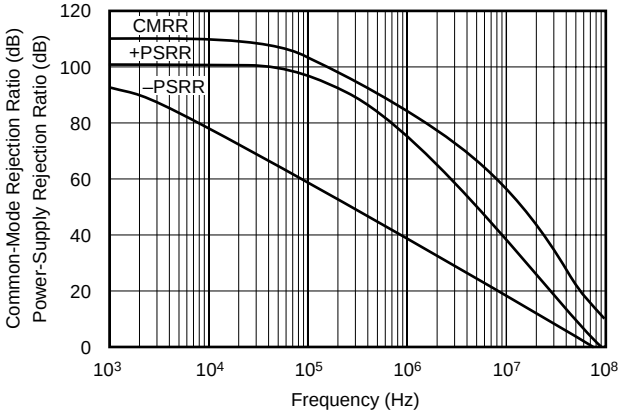
FREQUENCY RESPONSE vs CAPACITIVE LOAD



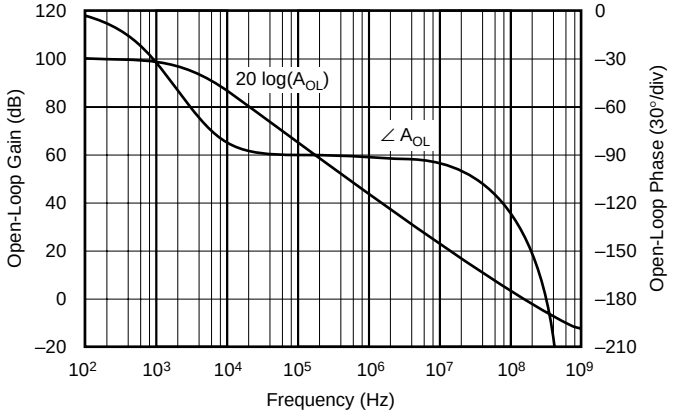
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (Cont.)

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

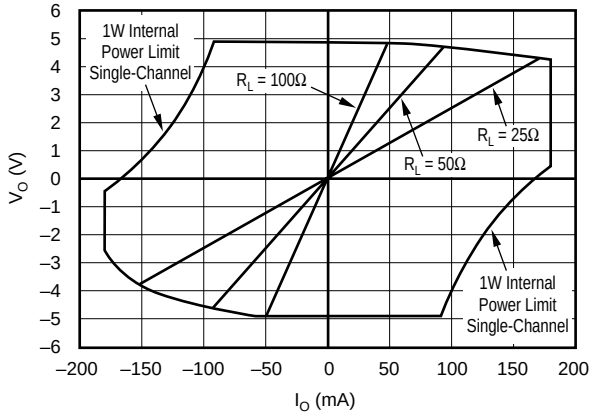
CMRR AND PSRR vs FREQUENCY



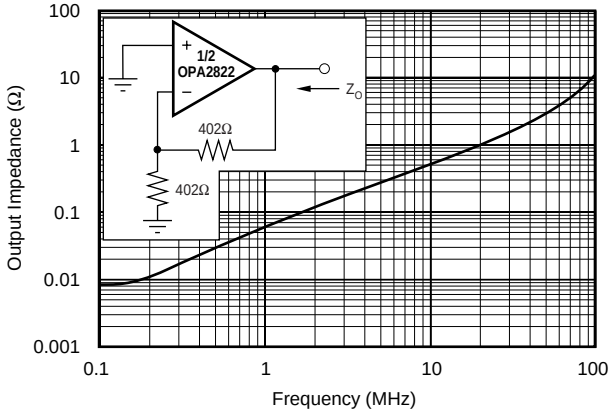
OPEN-LOOP GAIN AND PHASE



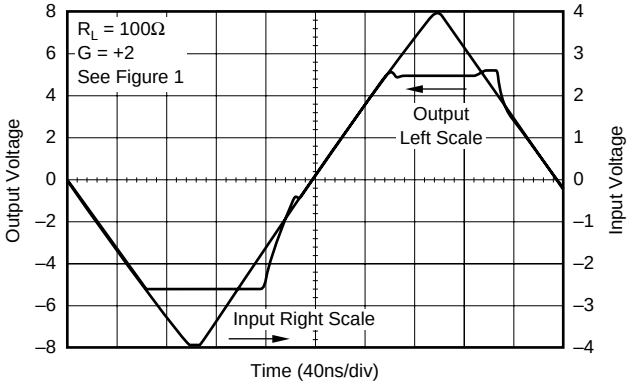
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



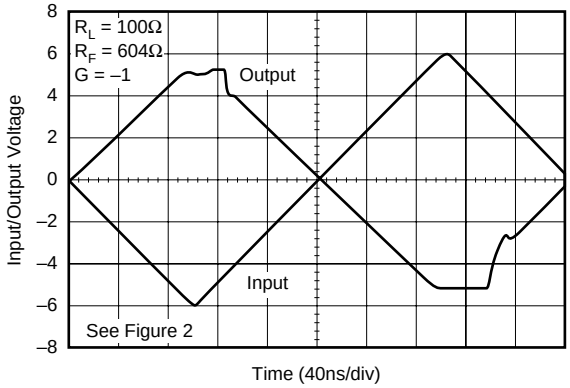
CLOSED-LOOP OUTPUT IMPEDANCE
vs FREQUENCY



NONINVERTING OVERDRIVE RECOVERY



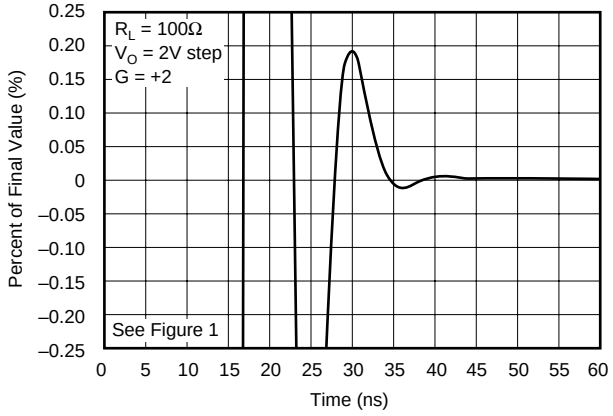
INVERTING OVERDRIVE RECOVERY



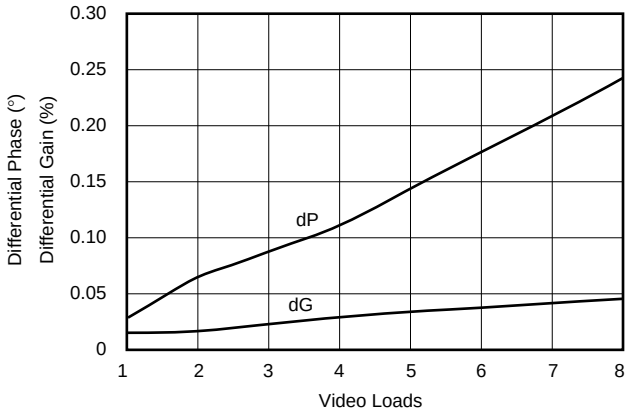
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T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

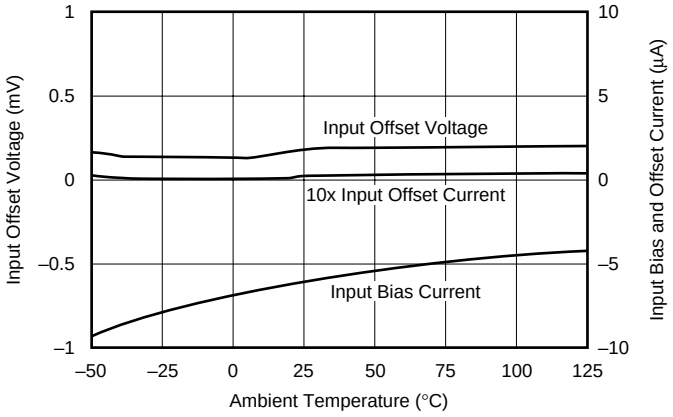
SETTLING TIME



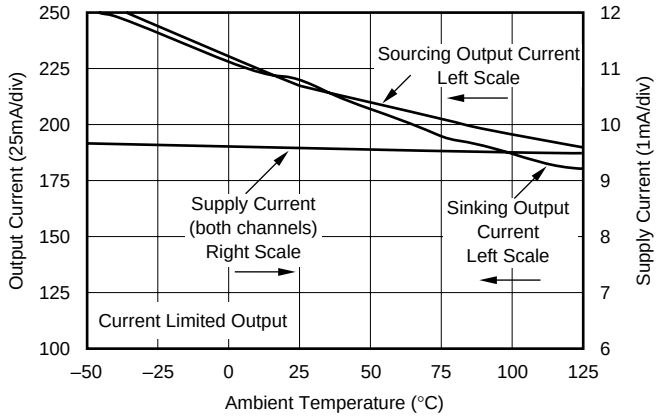
VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE



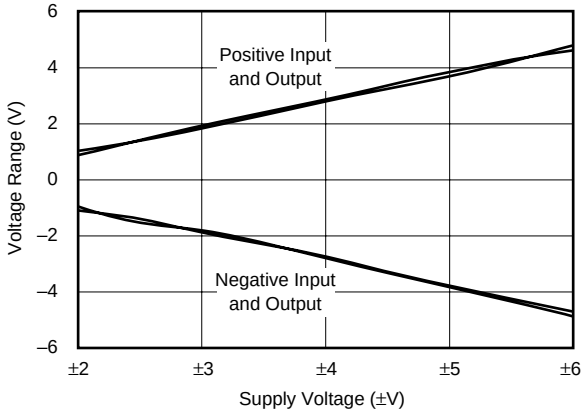
TYPICAL DC DRIFT OVER TEMPERATURE



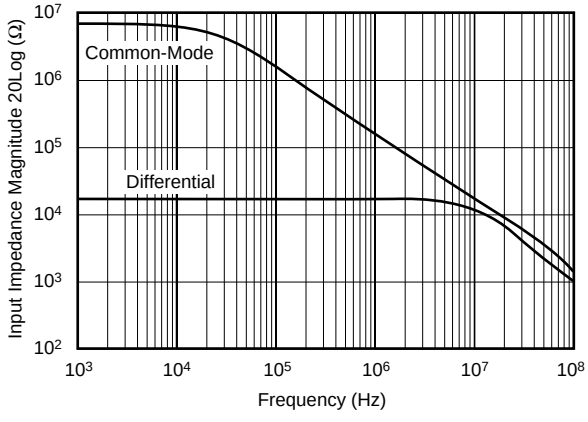
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



COMMON-MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



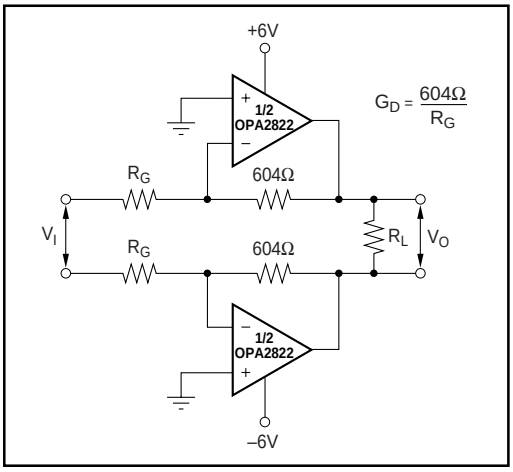
COMMON-MODE AND DIFFERENTIAL INPUT IMPEDANCE



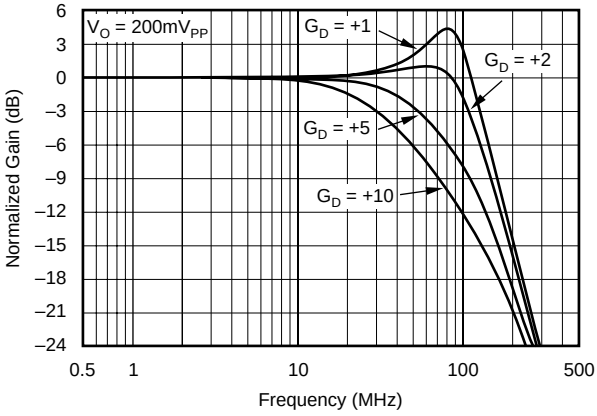
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

T_A = +25°C, Differential Gain = 2, R_F = 604Ω, and R_L = 400Ω, unless otherwise noted.

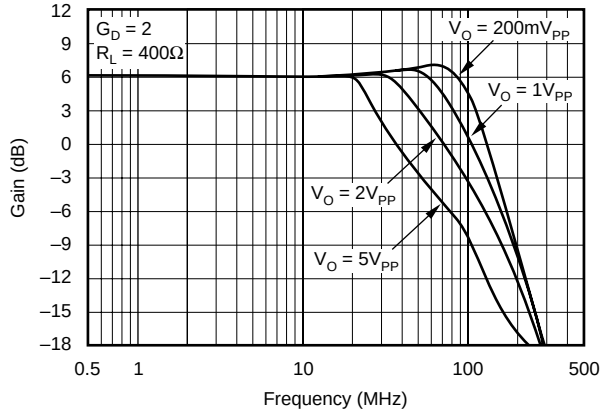
DIFFERENTIAL PERFORMANCE
TEST CIRCUIT



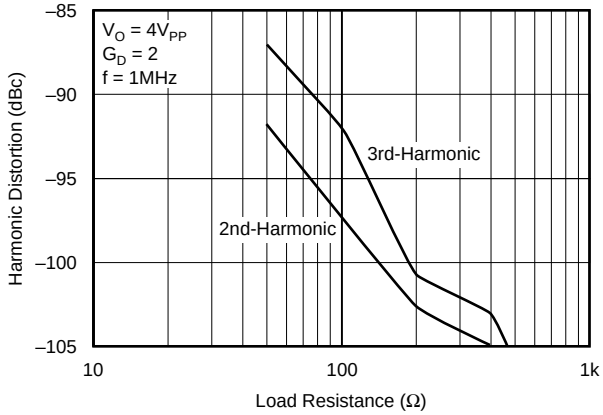
DIFFERENTIAL SMALL-SIGNAL
FREQUENCY RESPONSE



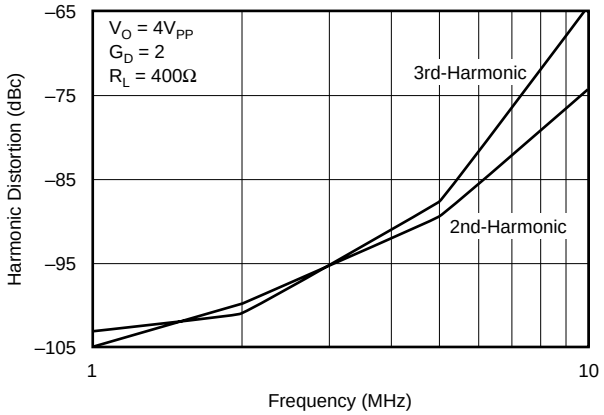
DIFFERENTIAL LARGE-SIGNAL
FREQUENCY RESPONSE



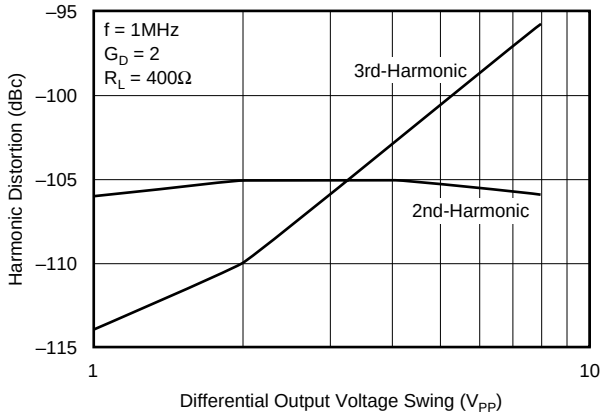
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



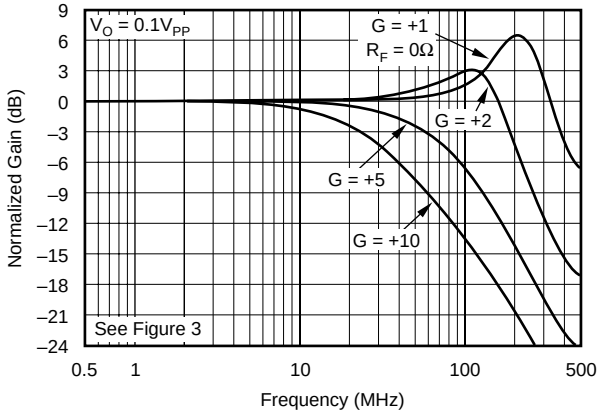
DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



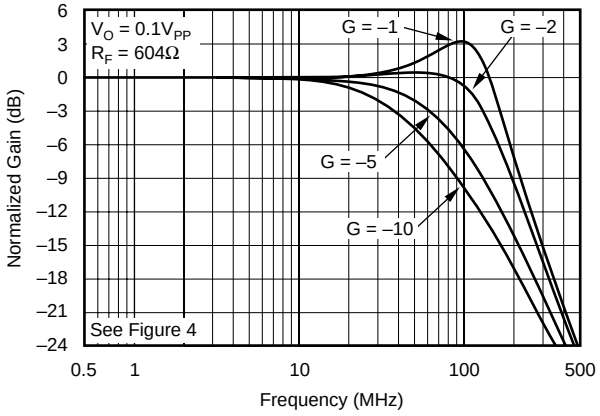
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T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

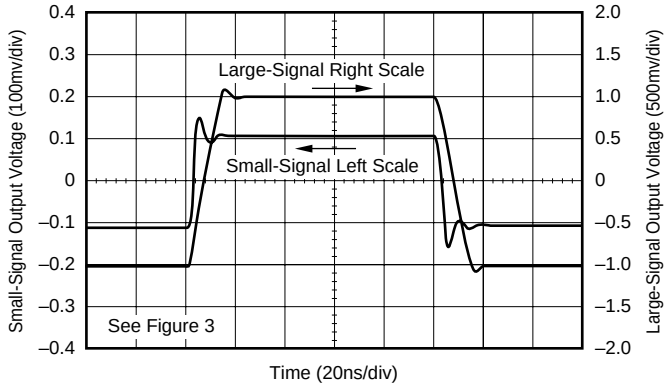
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



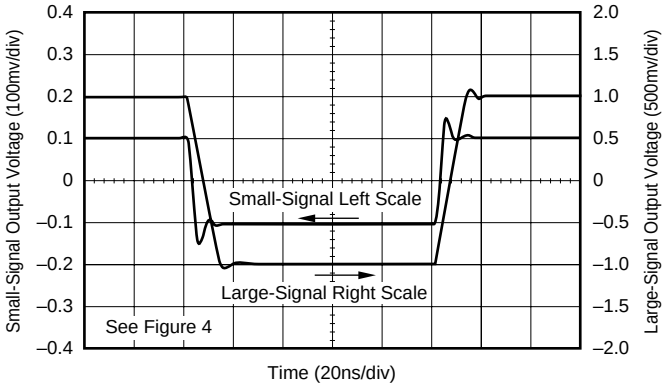
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



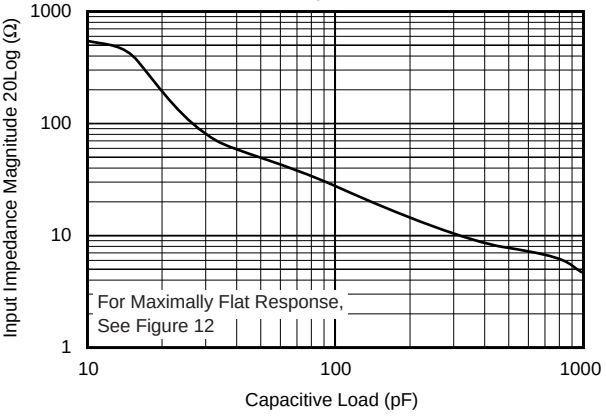
NONINVERTING PULSE RESPONSE



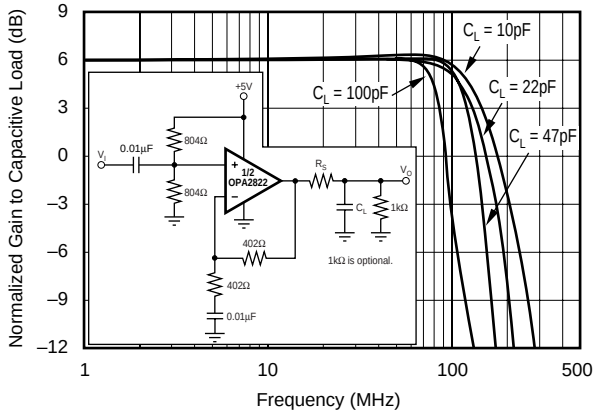
INVERTING PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



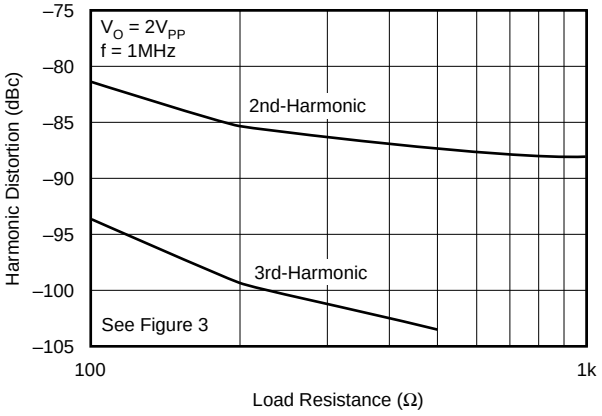
FREQUENCY RESPONSE vs CAPACITIVE LOAD



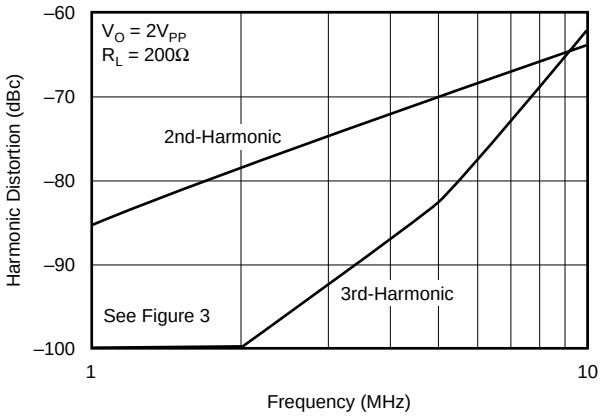
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T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

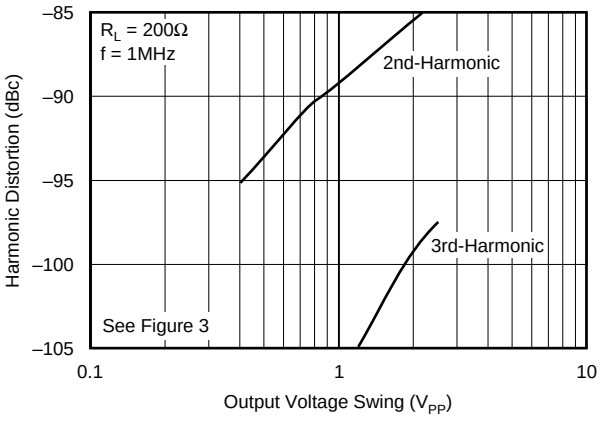
HARMONIC DISTORTION vs LOAD RESISTANCE



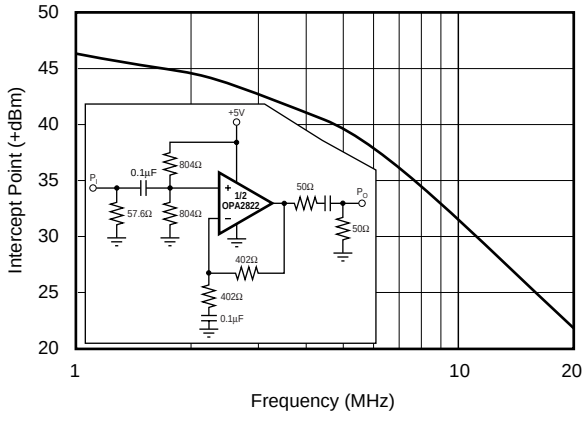
HARMONIC DISTORTION vs FREQUENCY



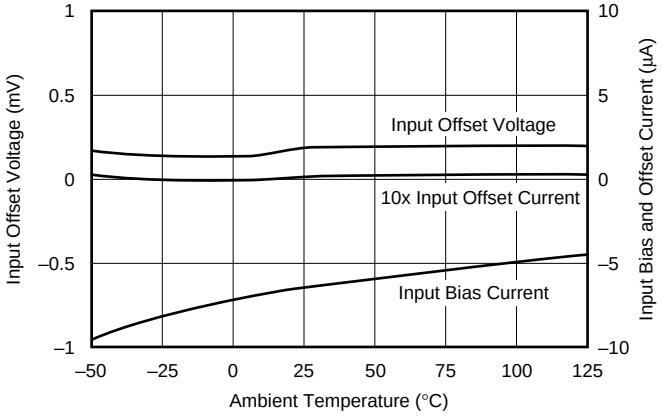
HARMONIC DISTORTION vs OUTPUT VOLTAGE



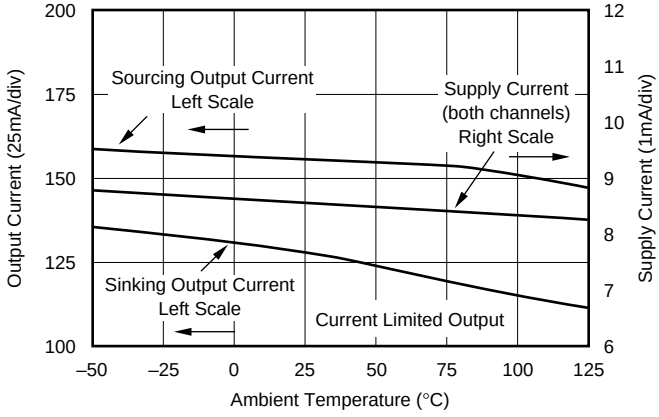
2-TONE, 3rd-ORDER
INTERMODULATION INTERCEPT



TYPICAL DC DRIFT OVER TEMPERATURE



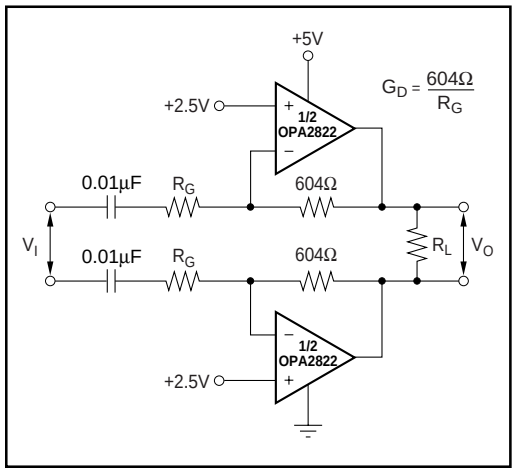
SUPPLY AND OUTPUT CURRENT
vs TEMPERATURE



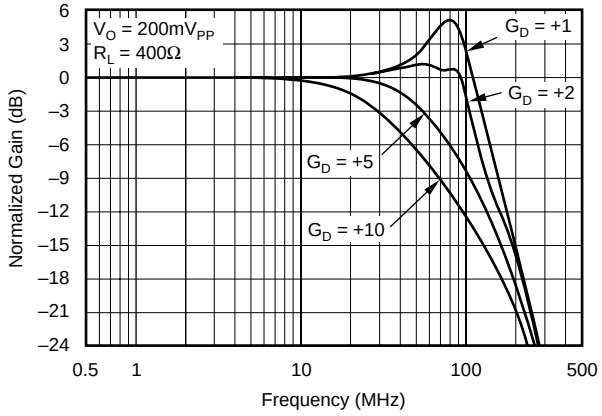
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, Differential Gain = +2, R_F = 604Ω, and R_L = 400Ω, unless otherwise noted.

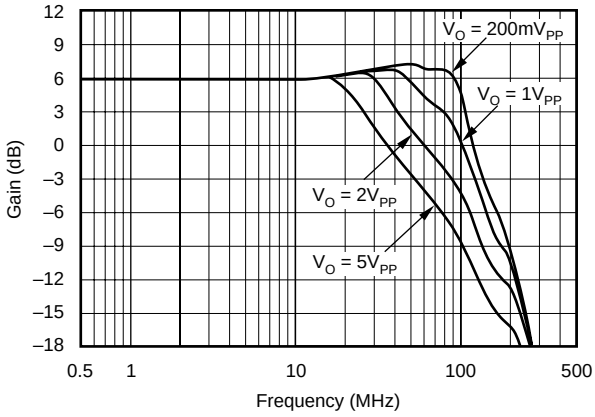
DIFFERENTIAL PERFORMANCE
TEST CIRCUIT



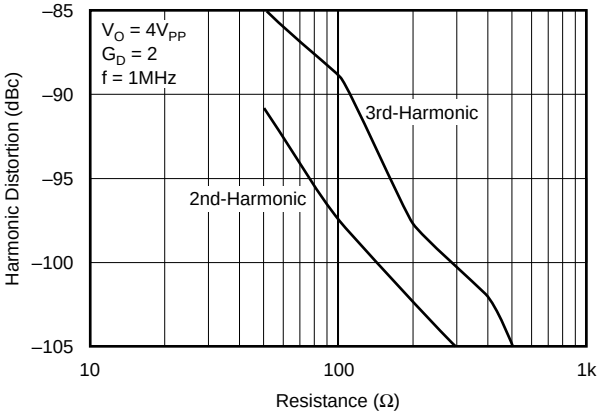
DIFFERENTIAL SMALL-SIGNAL
FREQUENCY RESPONSE



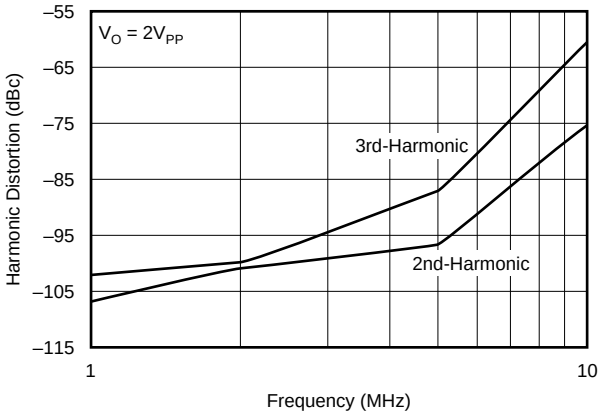
DIFFERENTIAL LARGE-SIGNAL
FREQUENCY RESPONSE



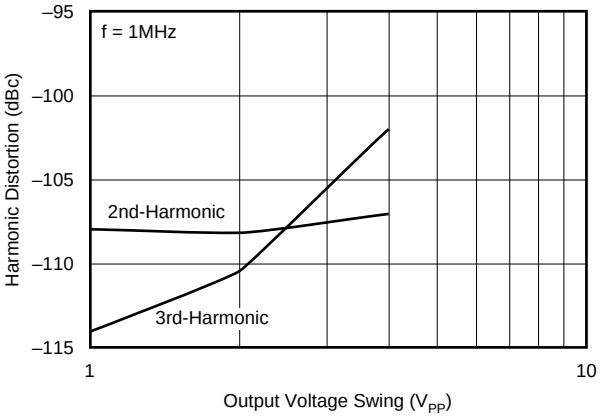
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND NONINVERTING OPERATION

The OPA2822 provides a unique combination of features in a wideband dual, unity-gain stable, voltage-feedback amplifier to support the extremely high dynamic range requirements of emerging communications technologies. Combining low 2nV/$\sqrt{Hz}$ input voltage noise with harmonic distortion performance that can exceed 100dBc SFDR through 2MHz, the OPA2822 provides the highest dynamic range input interface for emerging high speed 14-bit (and higher) converters. To achieve this level of performance, careful attention to circuit design and board layout is required.

Figure 1 shows the gain of +2 configuration used as the basis for the Electrical Characteristics table and most of the Typical Characteristics at ±6V operation. While the characteristics are given using split ±6V supplies, most of the electrical and typical characteristics also apply to a single-supply +12V design where the input and output operating voltages are centered at the midpoint of the +12V supply. Operation at ±5V will very nearly match that shown for the ±6V operating point. Most of the reference curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test signal generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1), while output power (dBm) specifications are at the matched 50Ω load. The total 100Ω load at the output, combined with the total 804Ω total feedback network load for the noninverting configuration of Figure 1, presents the OPA2822 with an effective output load of 89Ω. While this is a good load value for frequency response measurements, distortion will improve rapidly with lighter output loads. Keeping the same feedback network and increasing the load to 200Ω will result in a total load of 160Ω for the distortion performance reported in the Electrical Characteristics table.

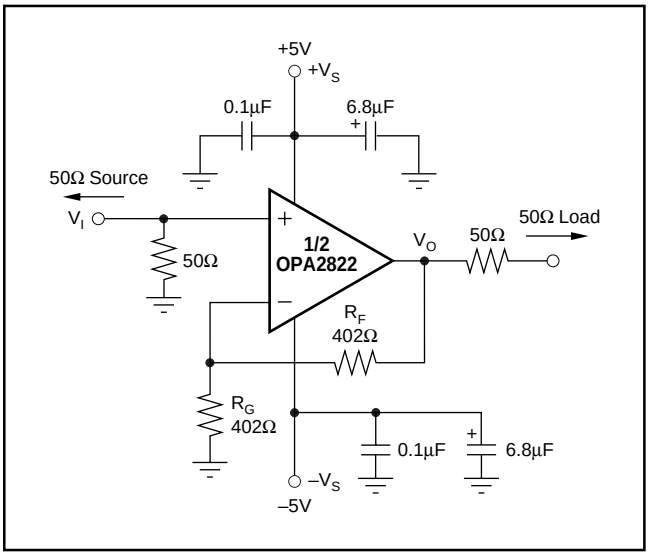


FIGURE 1. Noninverting G = +2 Specification and Test Circuit.

For higher gains, the feedback resistor (R_F) was held at 402Ω and the gain resistor (R_G) adjusted to develop the Typical Characteristics.

Voltage-feedback op amps, unlike current-feedback designs, can use a wide range of resistor values to set their gains. A low-noise part like the OPA2822 will deliver low total output noise only if the resistor values are kept relatively low. For the circuit of Figure 1, the resistors contribute an input-referred voltage noise component of 1.8nV/$\sqrt{Hz}$, which is approaching the value of the amplifier's intrinsic 2nV/$\sqrt{Hz}$. For a more complete description of the feedback network's impact on noise, see the Setting Resistor Values to Minimize Noise section later in this data sheet. In general, the parallel combination of R_F and R_G should be < 300Ω to retain the low-noise performance of the OPA2822. However, setting these values too low can impair distortion performance due to output loading, as shown in the distortion versus load data in the Typical Characteristics.

WIDEBAND INVERTING OPERATION

Operating the OPA2822 as an inverting amplifier has several benefits and is particularly appropriate as part of the hybrid design in an xDSL receiver application. Figure 2 shows the inverting gain of –1 circuit used as the basis of the inverting mode Typical Characteristics.

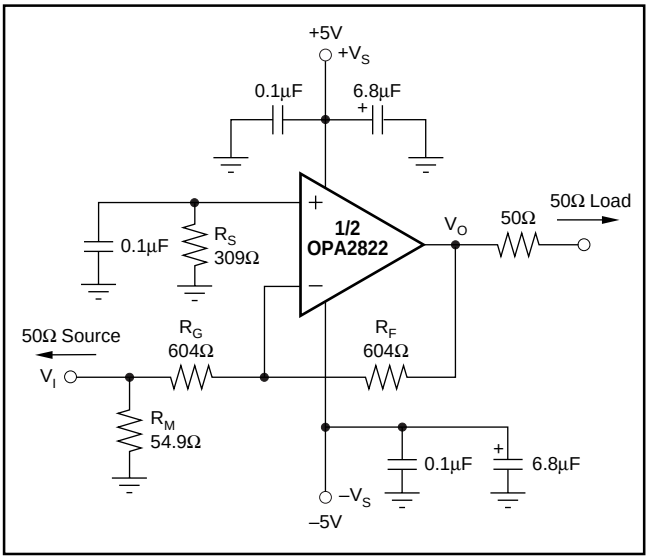


FIGURE 2. Inverting G = –1 Specification and Test Circuit.

In the inverting case, only the R_F element of the feedback network appears as part of the total output load in parallel with the actual load. For the 100Ω load used in the Typical Characteristics, this gives an effective load of 86Ω in this inverting configuration. Gain resistor R_G is set to achieve the desired inverting gain (in this case 604Ω for a gain of –1), while an additional input matching resistor (R_M) can be used to set the total input impedance equal to the source if desired. In this case, R_M = 54.9Ω in parallel with the 604Ω gain setting resistor yields a matched input impedance of 50Ω. R_M is needed only when the input must be matched to a source impedance, as in the characterization testing done using the circuit of Figure 2.

To take full advantage of the OPA2822's excellent DC input accuracy, the total DC impedance seen at of each of the input terminals must be matched to get bias current cancellation. For the circuit of Figure 2, this requires the grounded 309Ω resistor on the noninverting input. The calculation for this resistor value assumes a DC-coupled 50Ω source impedance along with R_G and R_M. While this resistor will provide cancellation for the input bias current, it must be well decoupled (0.1µF in Figure 2) to filter the noise contribution of the resistor itself and of the amplifier's input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 2 will far exceed the bandwidth at the same gain magnitude for the noninverting circuit of Figure 1. This occurs due to the lower noise gain for the circuit of Figure 2 when the 50Ω source impedance is included in the analysis. For example, at a signal gain of –12 (R_G = 50Ω, R_M = open, R_F = 604Ω) the noise gain for the circuit of Figure 2 will be 1 + 604Ω/(50Ω + 50Ω) = 7, due to the addition of the 50Ω source in the noise gain equation. This will give considerably higher bandwidth than the noninverting gain of +12.

SINGLE-SUPPLY NONINVERTING OPERATION

The OPA2822 can also support single +5V operation with its exceptional input and output voltage swing capability. While not a rail-to-rail input/output design, both inputs and outputs can swing to within 1.2V of either supply rail. For a single amplifier channel, this gives a very clean $2V_{PP}$ output capability on a single +5V supply, or $4V_{PP}$ output for a differential configuration using both channels together. Figure 3 shows the AC-coupled noninverting gain of +2 used as the basis of the Electrical Characteristics table and most of the Typical Characteristics for single +5V supply operation.

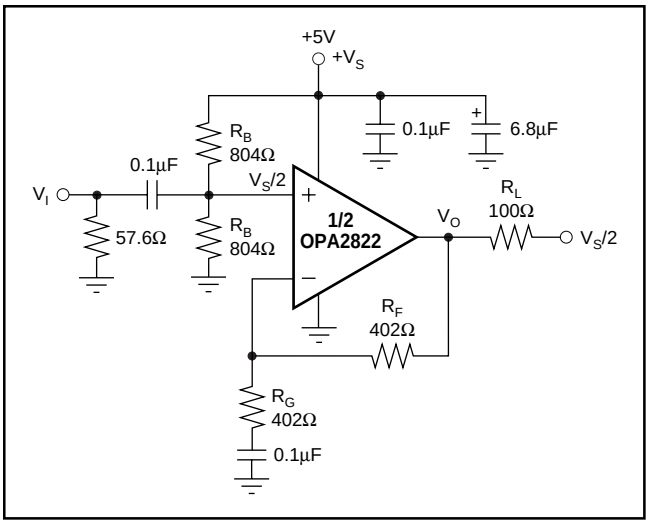


FIGURE 3. AC-Coupled, G = +2, Single-Supply Operation: Specification and Test Circuit.

The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage range at both input and output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 804Ω resistors). These two resistors are selected to provide DC bias current cancellation because their parallel combination matches the DC impedance looking out of the inverting node, which equals R_F. The gain setting resistor is not part of the DC impedance looking out of the inverting node, due to the blocking capacitor in series with it. The input signal is then AC-coupled into the midpoint voltage bias. The input impedance matching resistor (57.6Ω) is selected for testing to give a 50Ω input match (at high frequencies) when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving a DC gain of +1. This centers the output also at the input midpoint bias voltage (V_S/2). While this circuit is shown using a +5V supply, this same circuit may be applied for single-supply operation as high as +12V.

SINGLE-SUPPLY INVERTING OPERATION

For those single +5V Typical Characteristics that require inverting gain of –1 operation, the test circuit in Figure 4 was used.

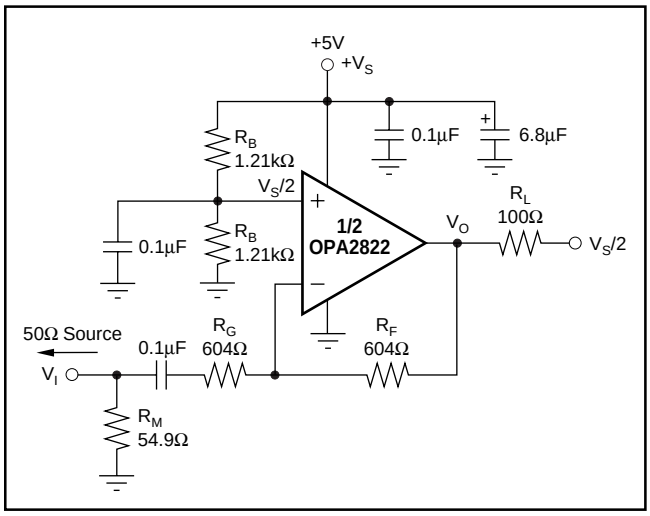


FIGURE 4. AC-Coupled, G = –1, Single-Supply Operation: Specification and Test Circuit.

As with the circuit of Figure 2, the feedback resistor (R_F) has been increased to 604Ω to reduce the loading effect it has in parallel with the 100Ω actual load. The noninverting input is biased at V_S/2 (2.5V in this case) using the two 1.21kΩ resistors for R_B. The parallel combination of these two resistors (605Ω) provides input bias current cancellation by matching the DC impedance looking out of the inverting input node. The noninverting input bias is also well decoupled using the 0.1µF capacitor to both reduce both power-supply noise and the resistor and bias current noise at this input.

The gain resistor (R_G) is set to equal the feedback resistor (R_F) at 604Ω to achieve the desired gain of –1 from V_I to V_O. A DC blocking capacitor is included in series with R_G to reduce the DC gain for the noninverting input bias and offset voltages to +1. This places the $V_S/2$ bias voltage at the output pin and reduces the output DC offset error terms. The signal input impedance is matched to the 50Ω source using the additional R_M resistor set to 54.9Ω. At higher frequencies, the parallel combination of R_M and R_G provides the input impedance match at 50Ω. This is principally used for test and characterization purposes—system applications do not necessarily require this input impedance match, particularly if the source device is physically near the OPA2822 and/or does not require a 50Ω input impedance match. At higher gains, the signal source impedance will start to materially impact the apparent noise gain (and hence, bandwidth) of the OPA2822.

ADSL RECEIVE AMPLIFIER

One of the principal applications for the OPA2822 is as a low-power, low-noise receive amplifier in ADSL modem designs. Applications ranging from single +5V, ±5V, and up to single +12V supplies can be well supported by the OPA2822. For higher supplies, consider the dual, low-noise THS6062 ADSL receive amplifier that can support up to ±15V supplies. Figure 5 shows a typical ADSL receiver design where the OPA2822 is used as an inverting summing amplifier to provide both driver output signal cancellation and receive channel gain. In the circuit of Figure 5, the driver differential output voltage is shown as V_D, while the receiver channel output is shown as V_R.

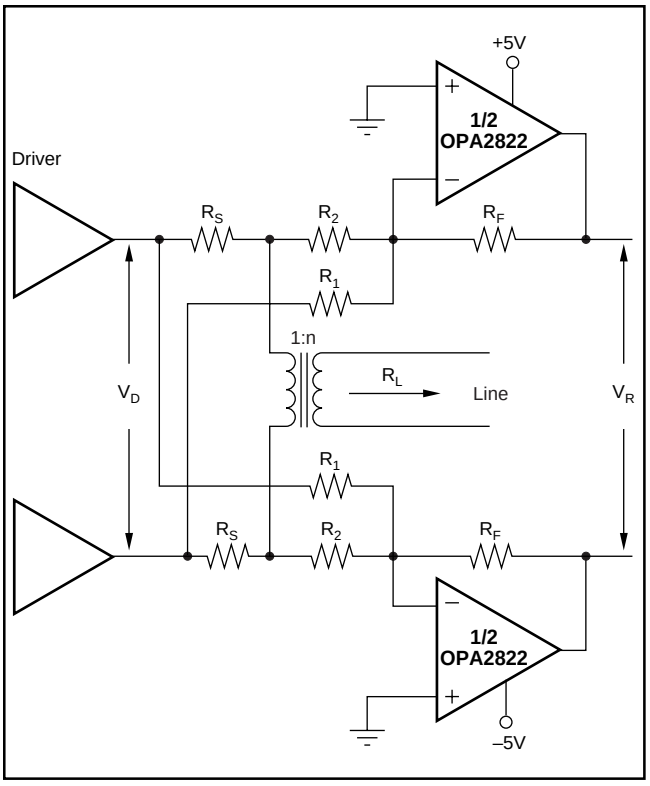


FIGURE 5. Example ADSL Receiver Amplifier.

The two sets of resistors, R_1 and R_2, are set to provide the desired gain from the transformer windings for the signal arriving on the line side of the transformer, and also to provide nominal cancellation for the driver output signal (V_D) to the receiver output. Typically, the two R_S resistors are set to provide impedance matching through the transformer. This is accomplished by setting $R_S = 0.5 \bullet (R_L/N^2)$, where N is the turns ratio used for the line driver design. If R_S is set in this fashion, and the actual twisted pair line shows the expected R_L impedance value, the voltage swing produced at V_D will be cut in half at the transformer input. In this case, setting $R_1 = 2 \bullet R_2$ will achieve cancellation of the driver output signal at the output of the receiver. Essentially, the driver output voltage produces a current in R_1 that is exactly matched by the current pulled out of R_2 due to the attenuated and inverted version of the output signal at the transformer input. In actual practice, R_1 and R_2 are usually RC networks to achieve cancellation over the frequency varying line impedance.

As the transformer turns ratio changes to support different line driver and supply voltage combinations, the impact of receiver amplifier noise changes. Typically, DSL systems incur a line referred noise contribution for the receiver that can be computed for the circuit of Figure 5. For example, targeting an overall gain of 1 from the line to the receiver output, and picking the input resistor R_2, the remaining resistors will be set by the driver cancellation and gain requirements. With the resistor values set, a line referred noise contribution due to the OPA2822 can be computed. R_1 will be set to 2x the value of R_2, and the feedback resistor will be set to recover the gain loss through the transformer. Table I shows the total line referred noise floor (in dBm/Hz) using three different values for R_2 over a range of transformer turns ratio (where the amplifier gain is adjusted at each turns ratio).

TABLE I. Line Referred Noise dBm/Hz, Due to Receiver Op Amp.

N	R_2 = 200	R_2 = 500	R_2 = 1000
1	–151.5	–150.2	–148.5
1.5	–149.1	–147.6	–145.8
2	–147.2	–145.6	–143.7
2.5	–145.6	–144.0	–142.1
3	–144.3	–142.7	–140.7
3.5	–143.2	–141.5	–139.5
4	–142.2	–140.5	–138.4
4.5	–141.3	–139.5	–137.5
5	–140.4	–138.7	–136.6

Table I shows that a lower transformer turns ratio results in reduced line referred noise, and that the resistor noise will start to degrade the noise at higher values—particularly in going from 500Ω to 1kΩ. In general, line referred noise floor due to the receiver channel will not be the limit to ADSL modem performance, if it is lower than –145dBm.

ACTIVE FILTER APPLICATIONS

As a low-noise, low-distortion, unity-gain stable, voltage-feedback amplifier, the OPA2822 provides an ideal building block for high-performance active filters. With two channels available, it can be used either as a cascaded 2-stage active filter or as a differential filter. Figure 6 shows a 6th-order bandpass filter cascaded with two 2nd-order Sallen-Key sections, with transmission zeroes along with a passive post filter made up of a high-pass and a low-pass section. The first amplifier provides a 2nd-order high-pass stage while the second amplifier provides the 2nd-order low-pass stage. Figure 7 shows the frequency response for this example filter.

A differential active filter is shown in Figure 8. This circuit shows a single-supply, 2nd-order high-pass filter with the corner frequencies set to provide the required high-pass function for an ADSL CPE modem application. To use this circuit, the hybrid would be implemented as a passive summing circuit at the input to this filter. For +5V only ADSL designs, it is preferable to implement a portion of the filtering prior to the amplifier, thus limiting the amplitude of the uncancelled line driver signals. This type of receiver stage would typically then drive a low-pass filter prior to the codec setting the high-frequency cutoff of the ADC (Analog-to-Digital Converter) input signal. Figure 9 shows the frequency response for the high-pass circuit of Figure 8.

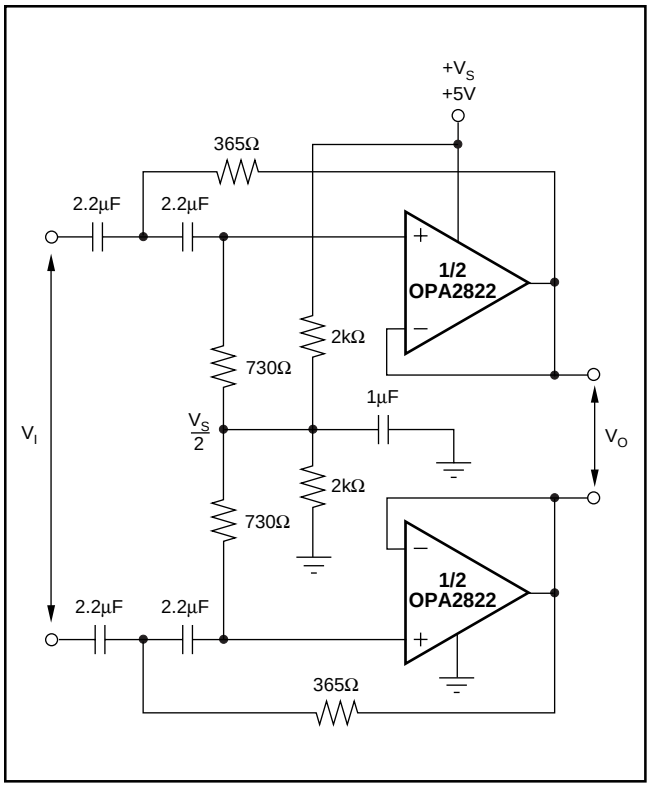


FIGURE 8. Single-Supply, 2nd-Order High-Pass Active Filter with Differential I/O.

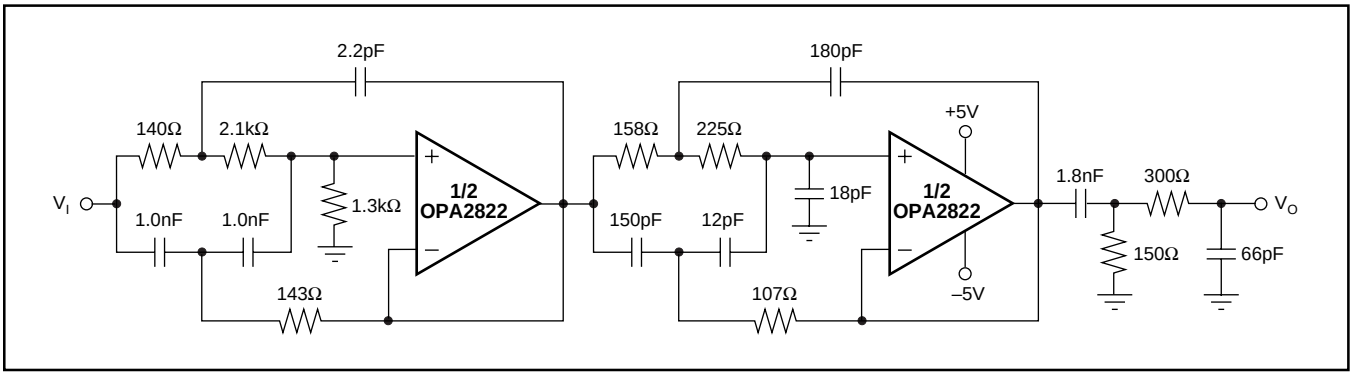


FIGURE 6. 6th-Order Bandpass Filter.

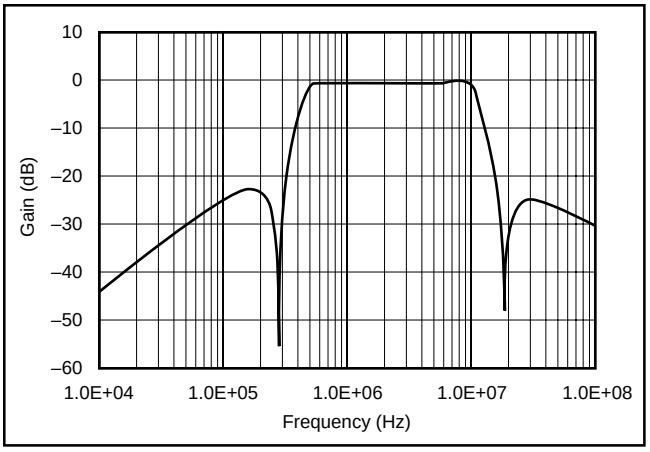


FIGURE 7. Frequency Response for the Filter in Figure 6.

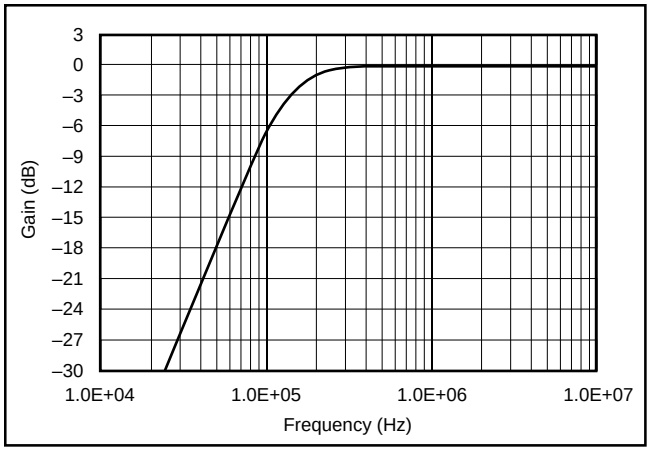


FIGURE 9. Frequency Response for the Filter in Figure 8.

HIGH DYNAMIC RANGE ADC DRIVER

Numerous circuit approaches exist to provide the last stage of amplification before the ADC in high-performance applications. For very high dynamic range applications where the signal channel can be AC-coupled, the circuit shown in Figure 10 provides exceptional performance. Most very high performance ADCs > 12-bit performance require differential inputs to achieve the dynamic range. The circuit of Figure 10 converts a single-ended source to differential via a 1:2 turns ratio transformer, which then drives the inverting gain setting resistors (R_G). These resistors are fixed at 100Ω to provide input matching to a 50Ω source on the transformer primary side. The gain can then be adjusted by setting the feedback resistor values. For best performance, this circuit operates with a ground centered output on ±5V supplies, although a +12V supply can also provide excellent results. Since most high-performance converters operate on a single +5V supply, the output is level shifted through an AC blocking capacitor to the common-mode input voltage (V_{CM}) for the converter input, and then low-pass filtered prior to the input of the converter. This circuit is intended for inputs from 10kHz to 10MHz, so the output high-pass corner is set to 1.6kHz, while the low-pass cutoff is set to 20MHz. These are example cutoff frequencies; the actual filtering requirements would be set by the specific application.

The 1:2 turns ratio transformer also provides an improvement in input referred noise figure. Equation 1 shows the Noise Figure (NF) calculation for this circuit, where R_G has been constrained to provide an input match to R_S (through the transformer) and then R_F is set to get the desired overall gain. With these constraints (and 0Ω on the noninverting inputs), the noise figure equation simplifies considerably.

$$NF = 10 \log \left[2 + \frac{4}{\alpha} + \frac{2\left(e_n\left(\frac{1}{2} + \frac{1}{\alpha}\right)/n\right)^2 + \frac{1}{2}(i_n n R_S)^2}{kTR_S} \right] \quad (1)$$

where $R_G = 1/2\ n^2 R_S$

n = Transformer Turns Ratio

$\alpha = R_F/R_G$

e_n = Op Amp Input Voltage Noise

i_n = Inverting Input Current Noise

kT = 4E – 21J[T = 290°K]

Gain (dB) = 20 log[nα]

TABLE II. Noise Figure versus Gain with n = 2 Transformer.

TOTAL GAIN (V/V)	LOG GAIN (dB)	REQUIRED AMPLIFIER GAIN (α)	NOISE FIGURE (dB)
4	12.0	2	11.2
5	14.0	2.5	10.4
6	15.6	3	9.9
7	16.9	3.5	9.5
8	18.1	4	9.1
9	19.1	4.5	8.9
10	20.0	5	8.6

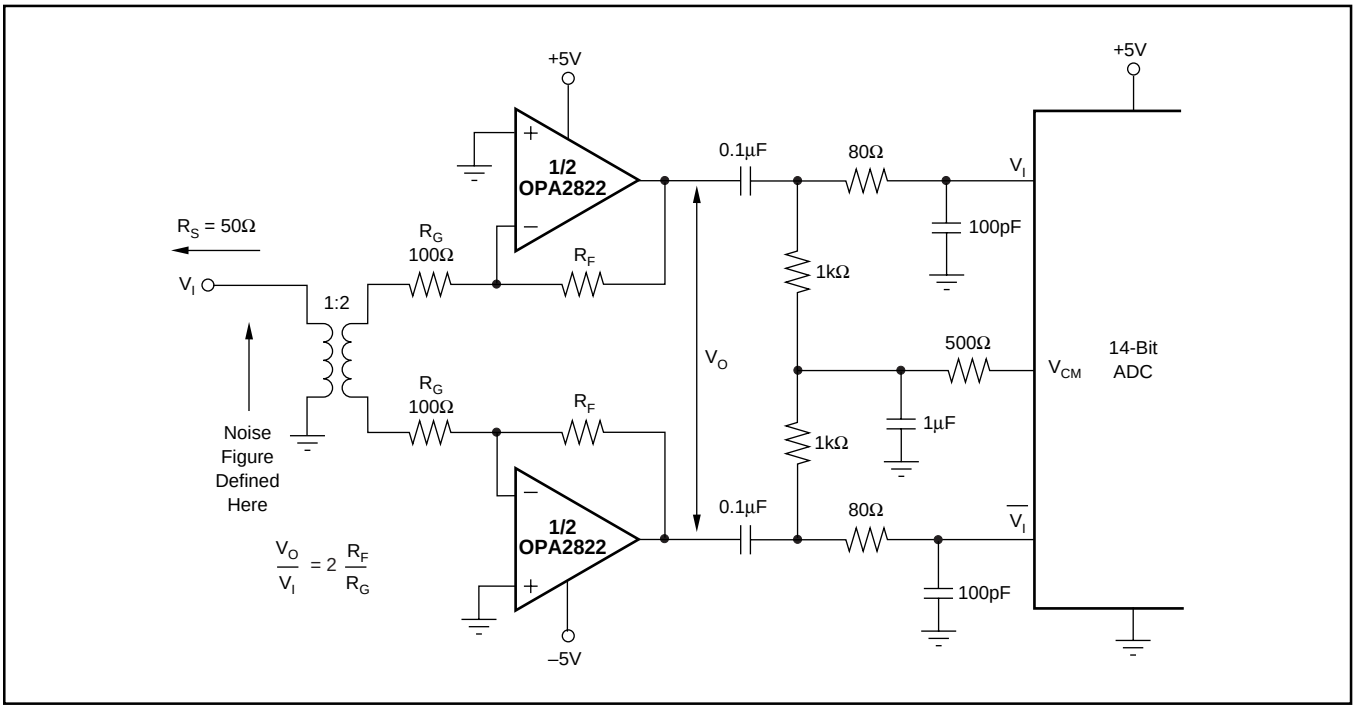


FIGURE 10. Single-Ended to Differential High Dynamic Range ADC Driver.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2822 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table III.

TABLE III. Demonstration Fixtures by Package.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2822U	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2822E	MSOP-8	DEM-OPA-MSOP-2A	SBOU004

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2822 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA2822 in its intended application. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the OPA2822 is available through the TI web site (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

Getting the full advantage of the OPA2822's low input noise requires careful attention to the external gain setting and DC biasing networks. The feedback resistor is part of the overall output load (which can begin to degrade distortion if set too low). With this in mind, a good starting point for design is to select the feedback resistor as low as possible (consistent with loading distortion concerns), then continue with the design, and set the other resistors as needed. To retain full performance, setting the feedback resistor in the range of 200Ω to 750Ω can provide a good start to the design. Figure 11 shows the full output noise analysis model for any op amp.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage terms. Equation 2 shows the general form of this output noise voltage expression using the terms shown in Figure 11.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

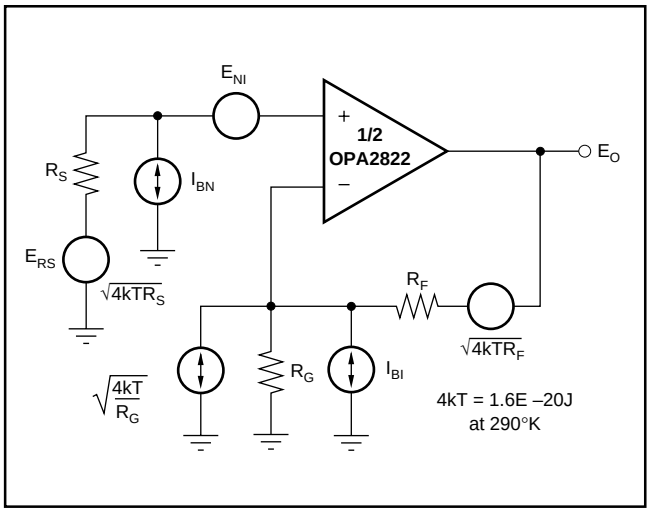


FIGURE 11. Op Amp Noise Analysis Model.

Dividing this expression by the noise gain (NG = 1 = R_F/R_G) will give the total equivalent spot noise voltage referred to the noninverting input, as shown in Equation 3:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (3)$$

Inserting high resistor values into Equation 3 can quickly dominate the total equivalent input referred voltage noise. A 250Ω source impedance on the noninverting input will add as much noise as the amplifier itself. If the noninverting input is a DC bias path (as in inverting or in some single-supply applications), it is critical to include a noise shunting capacitor with that resistor to limit the added noise impact of those resistors (see the example in Figure 2).

FREQUENCY RESPONSE CONTROL

Voltage-feedback op amps such as the OPA2822 exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, NG) will predict the closed-loop bandwidth. In practice, this principle holds true only when the phase margin approaches 90°, as it does in higher gain configurations. At low gains, most high-speed amplifiers will show a more complex response with lower phase margin and higher bandwidth than predicted by the GBP. The OPA2822 is compensated to give a slightly peaked frequency response at a gain of +2 (see the circuit in Figure 1). The 200MHz typical bandwidth at a gain of +2 far exceeds that predicted by dividing the GBP of 240MHz by a gain of 2. The bandwidth predicted by the GBP is more closely correct as the gain increases. As shown in the Typical Characteristics, at a gain of +10, the –3dB bandwidth of 24MHz matches that predicted by dividing the GBP by 10.

Inverting operation offers some interesting opportunities to increase the available signal bandwidth. When the source impedance is matched by the gain resistor (Figure 10 for example), the signal gain is ($1 + R_F/R_G$) while the noise gain is ($1 + R_F/2R_G$). This reduces the noise gain almost by half, extending the signal bandwidth and increasing the loop gain. For instance, setting $R_F = 500\Omega$ in Figure 10 will give a signal gain for the amplifier of 5V/V. However, including the 50Ω source impedance reflected through the 1:2 transformer will give an additional 100Ω source impedance for the noise gain analysis for each of the amplifiers. This reduces the noise gain to 1 + 500Ω/200Ω = 3.5V/V and results in an amplifier bandwidth of at least 240MHz/3.5 = 68MHz.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2822 can be very susceptible to decreased stability and closed-loop frequency response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness with low noise and distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but instead shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. For the OPA2822 operating at a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. One way to reduce the required R_S value is to use the noise gain adjustment circuit of Figure 12.

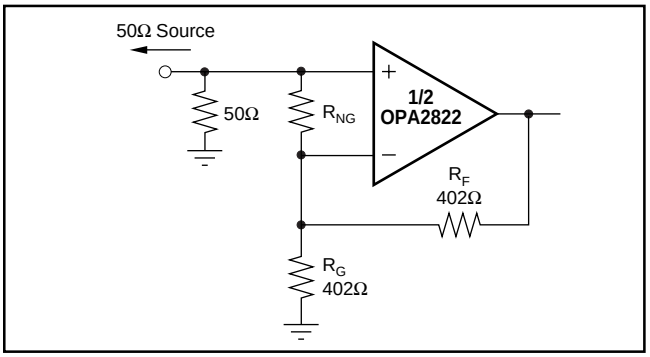


FIGURE 12. Noise Gain Tuning for Noninverting Circuit.

The resistor across the two inputs, R_{NG}, can be used to increase the noise gain while retaining the desired signal gain. This can be used either to improve flatness at low gains or to reduce the required value of R_S in capacitive load driving applications. This circuit was used with R_{NG} adjusted to produce the gain flatness curve in the Typical Characteristics. As shown in that curve, an R_{NG} of 452Ω will give an NG of 3 giving exceptional frequency response flatness at a signal gain of +2. Equation 4 shows the calculation for R_{NG} given a target noise gain (NG) and signal gain (G):

$$R_{NG} = \frac{R_F + R_S G}{NG - G} \quad (4)$$

where R_S = Total Source Impedance on the Noninverting Input [25Ω in Figure 12]

G = Signal Gain [$1 + (R_F/R_G)$]

NG = Noise Gain Target

Using this technique to get initial frequency response flatness will significantly reduce the required series resistor value to get a flat response at the capacitive load. Using the best-case noise gain of 3 with a signal gain of 2 allows the required R_S to be reduced, as shown in Figure 13. Here, the required R_S versus Capacitive Load is replotted along with data from the Typical Characteristics. This demonstrates that the use of $R_{NG} = 452\Omega$ across the inputs results in much lower required R_S values to achieve a flat response.

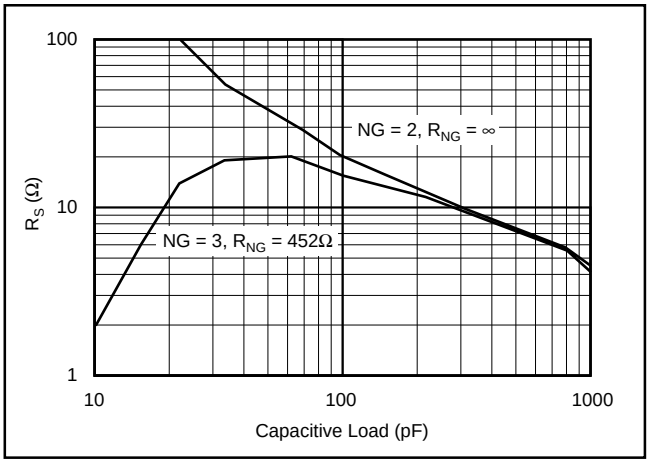


FIGURE 13. Required R_S vs Noise Gain.

DISTORTION PERFORMANCE

The OPA2822 is capable of delivering exceptionally low distortion through approximately 5MHz signal frequency. While principally intended to provide very low noise and distortion through the maximum ADSL frequency of 1.1MHz, the OPA2822 in a differential configuration can deliver lower than –85dBc distortions for a $4V_{PP}$ swing through 5MHz. For applications requiring extremely low distortion through higher frequencies, consider higher slew rate amplifiers such as the OPA687 or OPA2681.

As the Typical Characteristics show, until the fundamental signal reaches very high frequencies or power levels, the limit to SFDR will be 2nd-harmonic distortion rather than the negligible 3rd-harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. However, operating differentially offers the most significant improvement in even-order distortion terms. For example, the Electrical Characteristics show that a single channel of the OPA2822, delivering $2V_{PP}$ at 1MHz into a 200Ω load, will typically show a 2nd-harmonic product at –92dBc versus the 3rd-harmonic at –102dBc. Changing the configuration to a differential driver where each output still drives $2V_{PP}$ results in a $4V_{PP}$ total differential output into a 400Ω differential load, giving the same single-ended load of 200Ω for each amplifier. This configuration drops the 2nd-harmonic to –103dBc and the 3rd-harmonic to approximately –105dBc—an overall dynamic range improvement of more than 10dB.

For general distortion analysis, remember that the total loading on the amplifier includes the feedback network; in the noninverting configuration, this is the sum of $R_F + R_G$, while in the inverting configuration this additional loading is simply R_F. Increasing the output voltage swing increases the harmonic distortion directly. A 6dB increase in the output swing will generally increase the 2nd-harmonic 12dB and the 3rd-harmonic 18dB. Increasing the signal gain will also generally increase both the 2nd- and 3rd-harmonics because the loop gain decreases at higher gains. Again, a 6dB increase in voltage gain will increase the 2nd-harmonic distortion by approximately 6dB. The distortion characteristic curves for the OPA2822 show little change in the 3rd-harmonic distortion versus gain. Finally, the overall distortion generally increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies, down to the dominant open-loop pole at approximately 50kHz. This will give essentially unmeasurable levels of harmonic distortion in the audio band.

The OPA2822 exhibits an extremely low 3rd-order harmonic distortion. This also gives exceptionally good 2-tone 3rd-order intermodulation intercept as shown in the Typical Characteristics. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to RF MMIC devices. This network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA2822 drives directly into the input of a high-impedance device, such as an ADC, this 6dB attenuation does not occur. Under these conditions, the intercept will improve by at least 6dBm. The intercept is used to predict the intermodulation spurs for two closely spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta_F = |f_2 – f_1|$, the two, 3rd-order, close-in spurious tones will appear at $f_O \pm 3 \bullet \Delta_F$. The difference between two equal test-tone power levels and the spurious intermodulation power levels is given by $\Delta dBc = 2 \bullet (IM3 – P_O)$, where IM3 is the intercept taken from the Typical Specification and P_O is the power level in dBm at the 50Ω load for either one of the two closely spaced test frequencies. For example, at 1MHz in a gain of +2 configuration, the OPA2822 exhibits an intercept of 57dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$, each tone will be set to 4dBm. The 3rd-order intermodulation spurious tones will then be $2 \bullet (57 – 4) = 106$dBc below the test-tone power level (–102dBm). If this same $2V_{PP}$ 2-tone envelope were delivered directly into the input of an ADC without the matching loss or loading of the 50Ω network, the intercept would increase to at least 63dBm. With the same signal and gain conditions but now driving directly into a light load, the spurious tones would then be at least $2 \bullet (63 – 4) = 118$dBc below the test-tone power levels.

DC ACCURACY AND OFFSET CONTROL

The OPA2822 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of the low input offset voltage (±1.2mV maximum at 25°C), careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA2822 has relatively high input bias current (8µA typical into the pins) but with a very close match between the two input currents, typically 100nA input offset current. The total output offset voltage may be reduced considerably by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 175Ω series resistor into the noninverting input from the 50Ω terminating resistor. If the 50Ω source resistor is DC coupled, this will increase the source impedance for the noninverting input bias current to 200Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F \parallel R_G$), the circuit will cancel the bias current effects, leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402Ω feedback resistor, the output DC error due to the input bias currents will now be less than $0.7\mu A \bullet 402\Omega = 0.28$mV over the full temperature range. This is significantly lower than the contribution due to the input offset voltage. At a gain of +2, the maximum input offset voltage is 1.5mV, giving a total maximum output offset of (±3mV ± 0.28mV) = ±3.3mV over the –40°C to +85°C temperature range (for the circuit of Figure 1, including the additional 175Ω resistor at the noninverting input).

THERMAL ANALYSIS

The OPA2822 will not require heatsinking or airflow under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D\theta_{JA}$. The total internal power dissipation (P_D) is the sum of the quiescent power (P_{DO}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required

output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to half of either supply voltage (assuming equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J for the OPA2822E with both channels operating at A_V = +2, R_L = 100Ω, R_F = 400Ω, $\pm V_S$ = ±5V, and at the specified maximum T_A = 85°C.

$$P_D = 10V \bullet 11.4mA + 2 \bullet (5^2)/(4 \bullet (100 \parallel 804)) = 255mW$$

$$\text{Maximum } T_J = 85°C + 0.255W \bullet 150°C/W = 123°C$$

This calculation represents a worst-case combination of conditions to reach a maximum possible operating junction temperature. Under most operating conditions, the junction temperature will be far lower than the 123°C calculated here.

The output current is limited in the OPA2822 to protect against damage under short-circuit conditions. This current-limited output of approximately 220mA exceeds the rated typical output current of 150mA. The typical and minimum output current limits are set for linear operation while the maximum output shown in the Typical Characteristics is nonlinear limited performance.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the OPA2822 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the device pins and the decoupling capacitors. The primary power-supply connections (on pins 4 and 8) should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2822. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with parasitic load, distortion, and noise considerations. The 402Ω feedback used in the Typical Characteristics is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S versus capacitive load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2822 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This will not preserve signal integrity as

well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2822 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2822 onto the board.

INPUT AND ESD PROTECTION

The OPA2822 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low due to these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Rating table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 14.

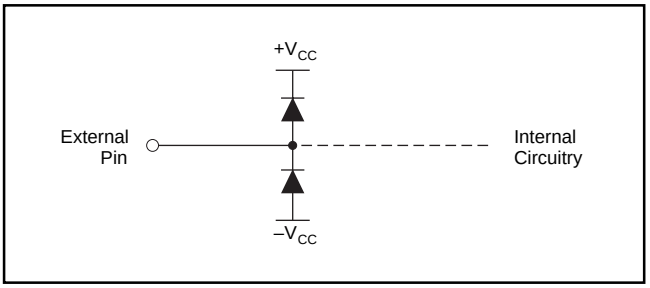


FIGURE 14. Internl ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2822), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
8/08	E	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125°C to –65°C to +125°C.
5/06	D	8	Typical Characteristics	Axis text change on, Closed-Loop Output Impedance vs Frequency.
		19	Design-In Tools	Demonstration fixture numbers changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2822E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D22	Samples
OPA2822E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D22	Samples
OPA2822U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2822U	Samples
OPA2822U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2822U	Samples
OPA2822UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2822U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

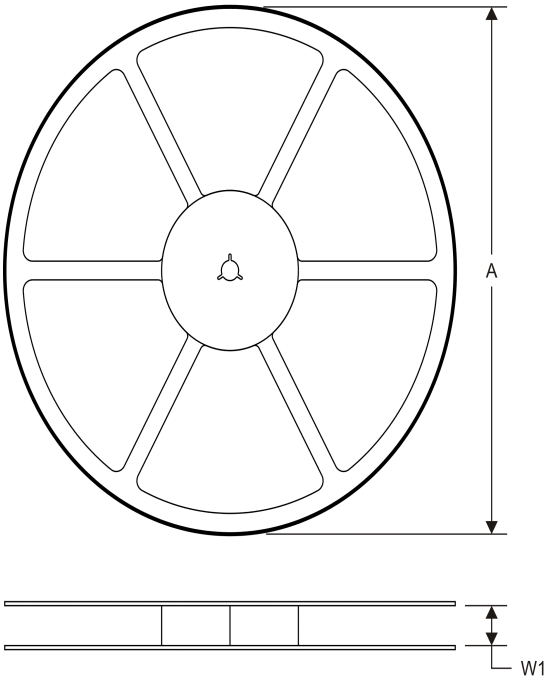
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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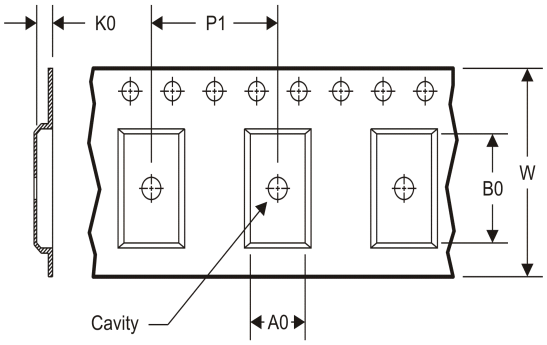
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



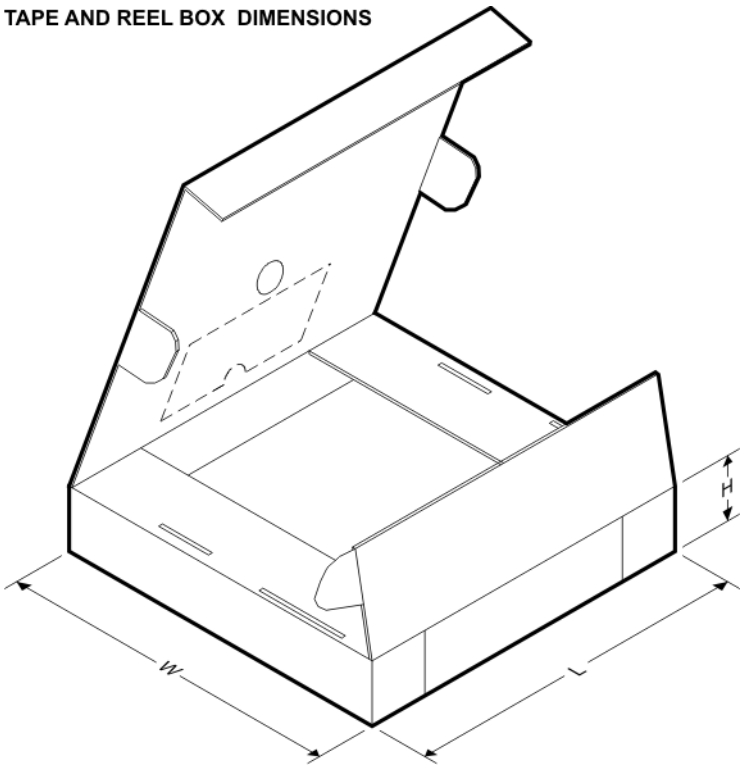
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

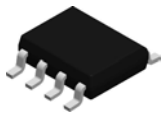
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2822E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2822E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2822U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2822E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2822E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2822U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

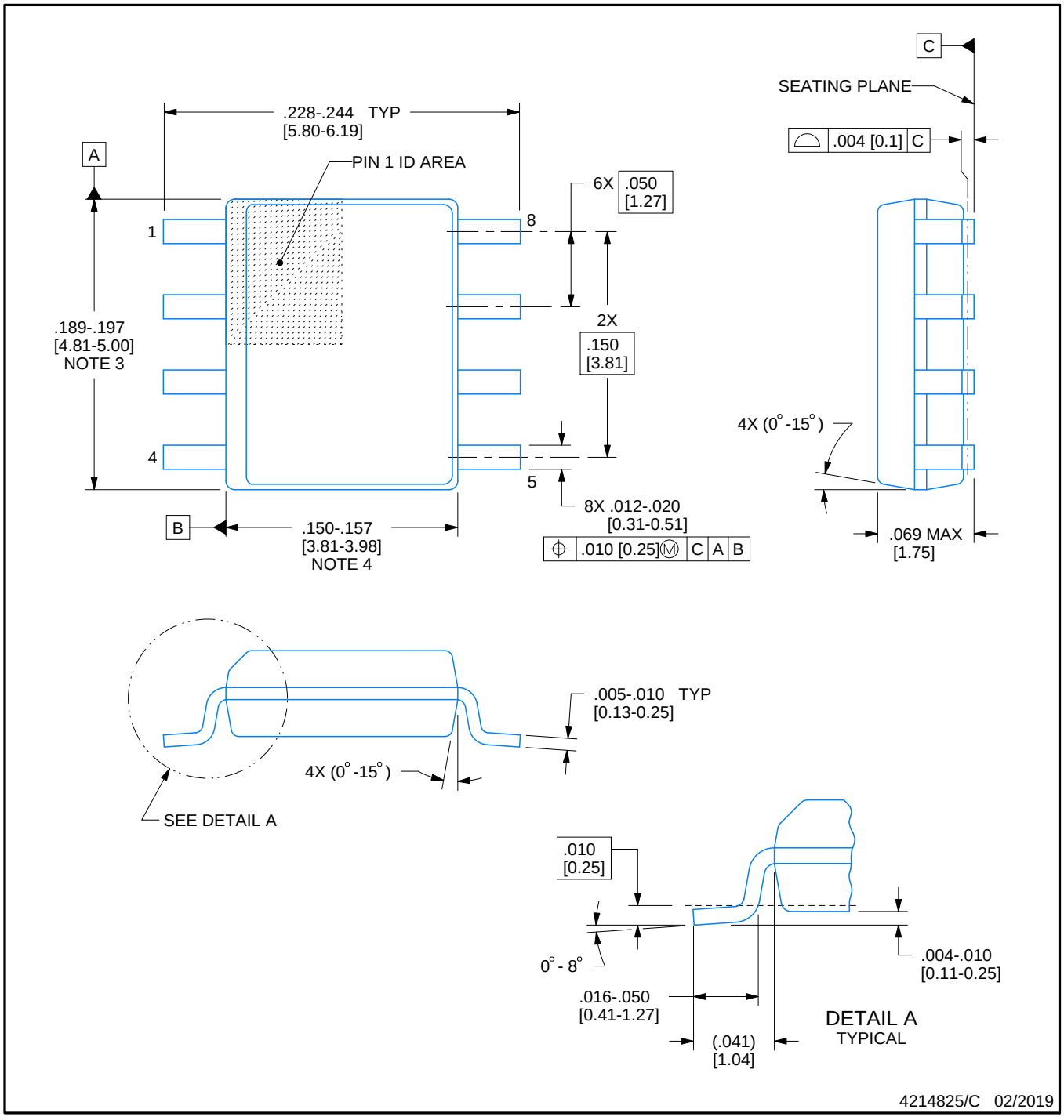


PACKAGE OUTLINE

D0008A

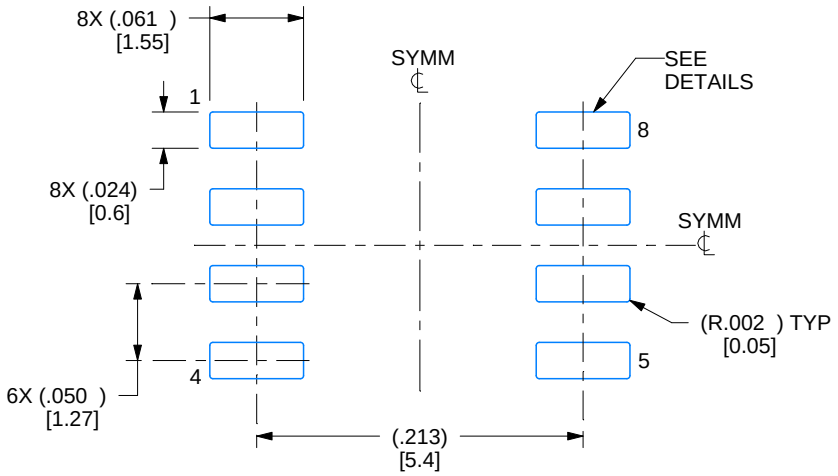
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

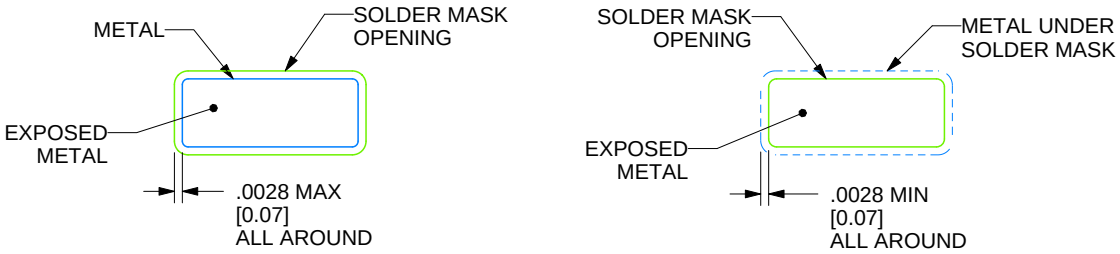


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

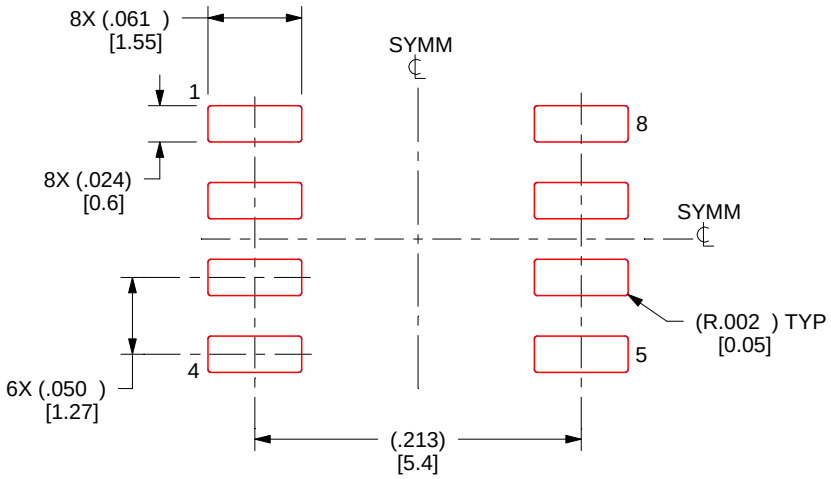
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



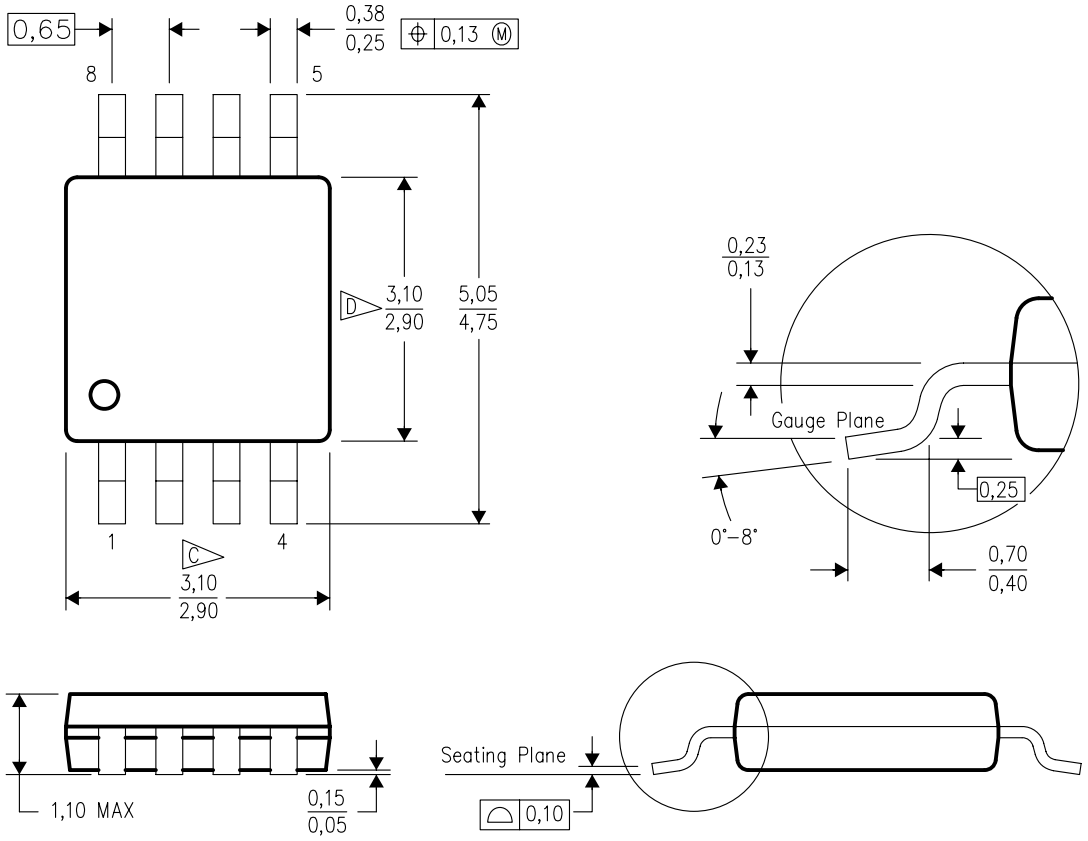
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

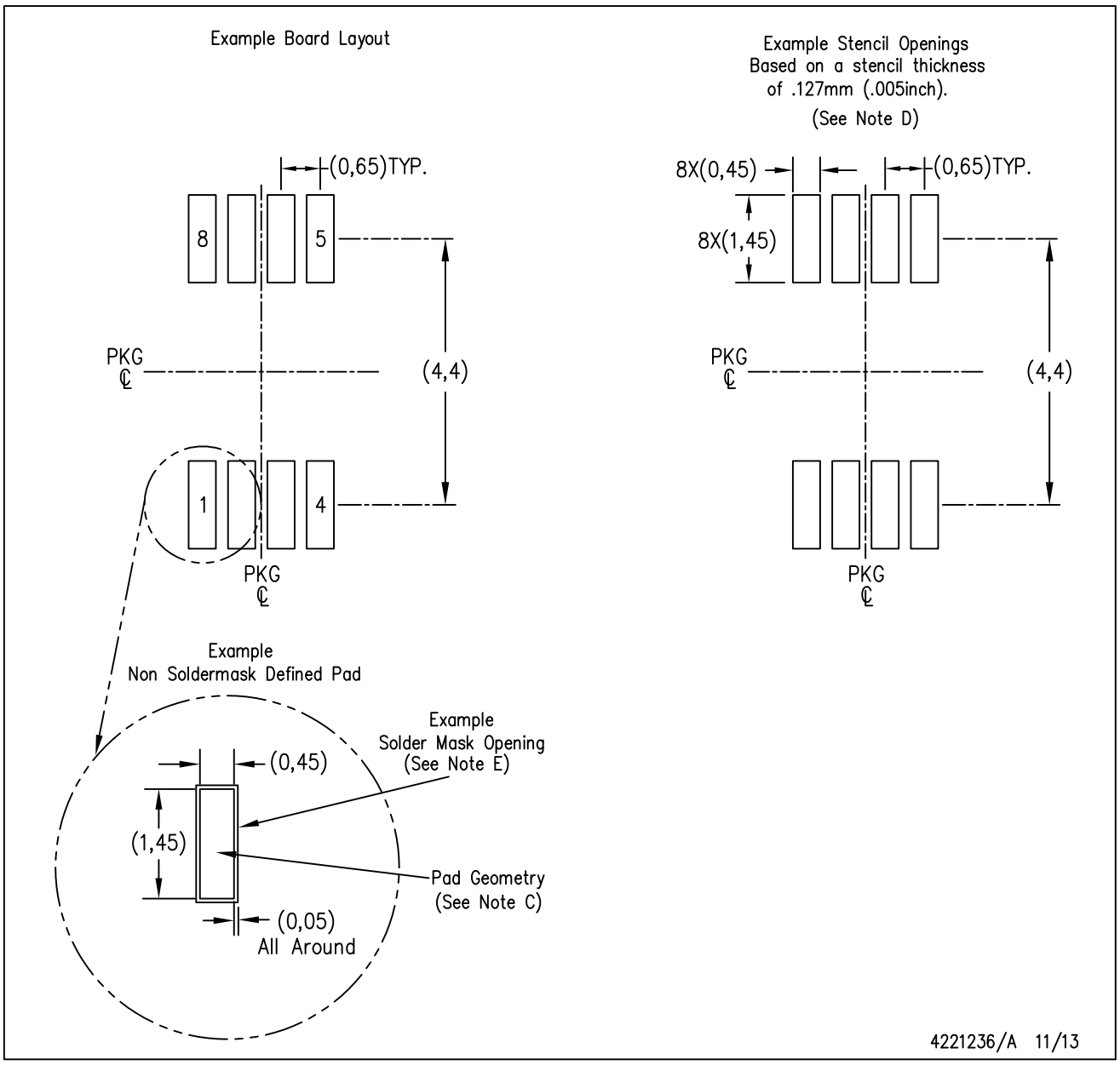
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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