# LOW-NOISE, HIGH-SPEED, CURRENT FEEDBACK AMPLIFIERS

**Check for Samples: THS3112, THS3115**

## FEATURES

- **Low Noise:**
  - **2.9-pA/√Hz Noninverting Current Noise**
  - **10.8-pA/√Hz Inverting Current Noise**
  - **2.2-nV/√Hz Voltage Noise**
- **Wide Supply Voltage Range: ±5 V to ± 15 V**
- **Wide Output Swing:**
  - **25-$V_{PP}$ Output Voltage, $R_L$ = 100 Ω, ±15-V Supply**
- **High Output Current: 150 mA (Min)**
- **High Speed:**
  - **110-MHz (–3-dB BW, G = 1, ±15 V)**
  - **1550-V/µs Slew Rate (G = 2, ±15 V)**
- **Low Distortion (G = 2):**
  - **–78 dBc (1 MHz, 2 $V_{PP}$, 100-Ω Load)**
- **Low-Power Shutdown (THS3115)**
  - **300-µA Shutdown Quiescent Current per Channel**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD Packages**
- **Evaluation Module Available**

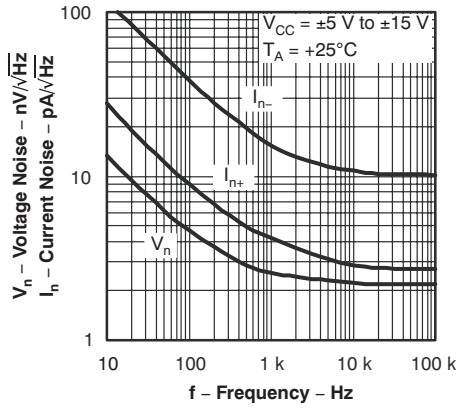
## APPLICATIONS

- **Communication Equipment**
- **Video Distribution**
- **Motor Drivers**
- **Piezo Drivers**

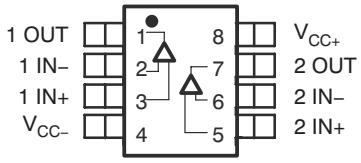
## DESCRIPTION

The THS3112/5 are low-noise, high-speed current feedback amplifiers, ideal for any application requiring high output current. The low noninverting current noise of 2.9 pA/√Hz and the low inverting current noise of 10.8 pA/√Hz increase signal-to-noise ratios for enhanced signal resolution. The THS3112/5 can operate from ±5-V to ±15-V supply voltages, while drawing as little as 4.5 mA of supply current per channel. It offers low –78-dBc total harmonic distortion driving 2 $V_{PP}$ into a 100-Ω load. The THS3115 features a low-power shutdown mode, consuming only 300-µA shutdown quiescent current per channel. The THS3112/5 are packaged in standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD packages.

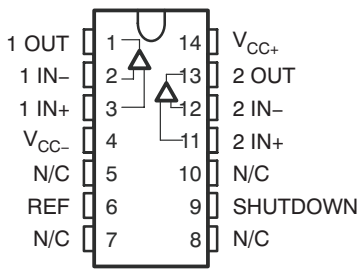
**VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY**




**THS3112 SOIC (D) AND SOIC PowerPAD™ (DDA) PACKAGE (TOP VIEW)**




**THS3115 SOIC (D) AND TSSOP PowerPAD™ (PWP) PACKAGE (TOP VIEW)**




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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## AVAILABLE OPTIONS(1)

| $T_A$ | PACKAGED DEVICE | | | | EVALUATION MODULES |
|---|---|---|---|---|---|
| | SOIC-8 (D) | SOIC-8 PowerPAD (DDA) | SOIC-14 (D) | TSSOP-14 (PWP) | |
| 0°C to +70°C | THS3112CD | THS3112CDDA | THS3115CD | THS3115CPWP | THS3112EVM THS3115EVM |
| 40°C to +85°C | THS3112ID | THS3112IDDA | THS3115ID | THS3115IPWP | |

(1) For the most current specification and package information, refer to the Package Option Addendum located at the end of this data sheet or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature (unless otherwise noted).

| | | UNIT |
|---|---|---|
| Supply voltage, $V_{CC+}$ to $V_{CC-}$ | | 33 V |
| Input voltage | | $\pm V_{CC}$ |
| Output current (see (2)) | | 275 mA |
| Differential input voltage | | ±4 V |
| Maximum junction temperature | | +150°C |
| Total power dissipation at (or below) +25°C free-air temperature | | See Dissipation Ratings Table |
| Operating free-air temperature, $T_A$ | Commercial | 0°C to +70°C |
| | Industrial | –40°C to +85°C |
| Storage temperature, $T_{stg}$ | Commercial | –65°C to +125°C |
| | Industrial | –65°C to +125°C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The THS3122 and THS3125 may incorporate a PowerPAD™ on the underside of the chip. This pad acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally-enhanced package.

## DISSIPATION RATINGS TABLE

| PACKAGE | $\theta_{JA}$ | $T_A$ = +25°C POWER RATING |
|---|---|---|
| D-8 | 95°C/W(1) | 1.32 W |
| DDA | 67°C/W | 1.87 W |
| D-14 | 66.6°C/W(1) | 1.88 W |
| PWP | 37.5°C/W | 3.3 W |

(1) These data were taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the $\theta_{JA}$ is 168°C/W for the D-8 package and 122.3°C/W for the D-14 package.


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## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC+}$ to $V_{CC-}$ | Dual supply | ±5 | | ±15 | V |
| | Single supply | 10 | | 30 | |
| Operating free-air temperature, $T_A$ | C-suffix | 0 | | +70 | °C |
| | I-suffix | –40 | | +85 | |

## ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, $T_A$ = +25°C, $V_{CC}$ = ±15 V, $R_F$ = 750 Ω, and $R_L$ = 100 Ω (unless otherwise noted).

**DYNAMIC PERFORMANCE**

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| BW | Small-signal bandwidth (–3 dB) | $R_L$ = 100Ω | $R_F$ = 1 kΩ, G = 1 | $V_{CC}$ = ±5 V | | 95 | | MHz |
| | | | | $V_{CC}$= ±15 V | | 110 | | |
| | | $R_L$ = 100 Ω | $R_F$ = 750 Ω, G = 2 | $V_{CC}$ = ±5 V | | 103 | | |
| | | | | $V_{CC}$= ±15 V | | 110 | | |
| | Bandwidth (0.1 dB) | $R_F$ = 750 Ω, G = 2 | | $V_{CC}$ = ±5 V | | 25 | | |
| | | | | $V_{CC}$= ±15 V | | 48 | | |
| SR | Slew rate(1), G = 8 | G = 2, $R_F$ = 680Ω | $V_O$= 10 $V_{PP}$ | $V_{CC}$ = ±15 V | | 1550 | | V/µs |
| | | | $V_O$ = 5 $V_{PP}$ | $V_{CC}$ = ±5 V | | 820 | | |
| | | | | $V_{CC}$= ±15 V | | 1300 | | |
| $t_s$ | Settling time to 0.1% | G = –1 | $V_O$ = 2 $V_{PP}$ | $V_{CC}$ = ±5 V | | 50 | | ns |
| | | | $V_O$= 5 $V_{PP}$ | $V_{CC}$ = ±15 V | | 63 | | |

(1) Slew rate is defined from the 25% to the 75% output levels.

**NOISE/DISTORTION PERFORMANCE**

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion | | G = 2, $R_F$ = 680 Ω, $V_{CC}$= ±15 V, f = 1 MHz | $V_{O(PP)}$ = 2 V | | –78 | | dBc |
| | | | | $V_{O(PP)}$ = 8 V | | –75 | | |
| | | | G = 2, $R_F$ = 680 Ω, $V_{CC}$= ±5 V, f = 1 MHz | $V_{O(PP)}$= 2 V | | –76 | | |
| | | | | $V_{O(PP)}$= 6 V | | –74 | | |
| $V_n$ | Input voltage noise | | $V_{CC}$ = ±5 V, ±15 V | f = 10 kHz | | 2.2 | | nV/√Hz |
| $I_n$ | Input current noise | Noninverting Input | $V_{CC}$ = ±5 V, ±15 V | f = 10 kHz | | 2.9 | | pA/√Hz |
| | | Inverting Input | | | | 10.8 | | |
| | Crosstalk | | G = 2, f = 1 MHz, $V_O$ = 2 $V_{PP}$ | $V_{CC}$ = ±5 V | | –67 | | dBc |
| | | | | $V_{CC}$= ±15 V | | –67 | | |
| | Differential gain error | | G = 2, $R_L$ = 150 Ω 40 IRE modulation ±100 IRE Ramp NTSC and PAL | $V_{CC}$ = ±5 V | | 0.01 | | % |
| | | | | $V_{CC}$= ±15 V | | 0.01 | | |
| | Differential phase error | | | $V_{CC}$ = ±5 V | | 0.011 | | degrees |
| | | | | $V_{CC}$= ±15 V | | 0.011 | | |

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## ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, $T_A$ = +25°C, $V_{CC}$ = ±15 V, $R_F$ = 750 Ω, and $R_L$ = 100 Ω (unless otherwise noted).

| DC PERFORMANCE | | | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
| $V_{IO}$ | Input offset voltage | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $T_A$ = +25°C | | 6 | 10 | mV |
| | | | $T_A$ = full range | | | 13 | |
| | Channel offset voltage matching | | $T_A$ = +25°C | | 1 | 3 | |
| | | | $T_A$ = full range | | | 4 | |
| | Offset drift | | $T_A$ = full range | | 10 | | µV/°C |
| $I_{IB}$ | IN- Input bias current | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $T_A$ = +25°C | | | 23 | µA |
| | | | $T_A$ = full range | | | 30 | |
| | IN+ Input bias current | | $T_A$ = +25°C | | 0.33 | 2 | |
| | | | $T_A$ = full range | | | 3 | |
| $I_{IO}$ | Input offset current | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $T_A$ = +25°C | | 4 | 22 | µA |
| | | | $T_A$ = full range | | | 30 | |
| $Z_{OL}$ | Open-loop transimpedance | $V_{CC}$ = ±5 V, $V_{CC}$ = ±15 V | $R_L$ = 1 kΩ | | 1 | | MΩ |

| INPUT CHARACTERISTICS | | | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
| $V_{ICR}$ | Input common-mode voltage range | $V_{CC}$ = ±5 V | $T_A$ = full range | ±2.5 | ±2.7 | | V |
| | | $V_{CC}$= ±15 V | | ±12.5 | ±12.7 | | |
| CMRR | Common-mode rejection ratio | $V_{CC}$ = ±5 V, $V_I$ = –2.5 V to 2.5 V | $T_A$ = +25°C | 56 | 62 | | dB |
| | | | $T_A$ = full range | 54 | | | |
| | | $V_{CC}$ = ±15 V, $V_I$ = –12.5 V to 12.5 V | $T_A$ = +25°C | 63 | 67 | | |
| | | | $T_A$ = full range | 60 | | | |
| $R_I$ | Input resistance | IN+ | | | 1.5 | | MΩ |
| | | IN– | | | 15 | | Ω |
| $C_I$ | Input capacitance | | | | 2 | | pF |

| OUTPUT CHARACTERISTICS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
| $V_O$ | Output voltage swing | G = 4, $V_I$ = 1 V, $V_{CC}$ = ±5 V, | $R_L$ = 1 kΩ | $T_A$ = +25°C | | 3.9 | | V |
| | | | $R_L$ = 100Ω | $T_A$ = +25°C | 3.6 | 3.8 | | |
| | | | | $T_A$ = full range | 3.4 | | | |
| | | G = 4, $V_I$ = 3.4 V, $V_{CC}$= ±15 V, | $R_L$ = 1 kΩ | $T_A$ = +25°C | | 13.5 | | V |
| | | | $R_L$ = 100Ω | $T_A$ = +25°C | 12.2 | 13.3 | | |
| | | | | $T_A$ = full range | 12 | | | |
| $I_O$ | Output current drive | G = 4, $V_I$ = 0.9 V, $V_{CC}$= ±5 V, | $R_L$ = 25 Ω | $T_A$ = +25°C | 100 | 130 | | mA |
| | | G = 4, $V_I$ = 1.7 V, $V_{CC}$ = ±15 V, | $R_L$ = 25 Ω | $T_A$ = +25°C | 175 | 270 | | mA |
| $r_o$ | Output resistance | Open loop | | | | 14 | | Ω |


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## ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, $T_A$ = +25°C, $V_{CC}$ = ±15 V, $R_F$ = 750 Ω, and $R_L$ = 100 Ω (unless otherwise noted).

| POWER SUPPLY | | | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
| $I_{CC}$ | Quiescent current (per channel) | $V_{CC}$ = ±5 V | $T_A$ = +25°C | | 4.4 | 5.5 | mA |
| | | | $T_A$ = full range | | | 6 | |
| | | $V_{CC}$ = ±15 V | $T_A$ = +25°C | | 4.9 | 6.5 | |
| | | | $T_A$ = full range | | | 7.5 | |
| PSRR | Power-supply rejection ratio | $V_{CC}$ = ±5 V | $T_A$ = +25°C | 53 | 60 | | dB |
| | | | $T_A$ = full range | 50 | | | |
| | | $V_{CC}$ = ±15 V | $T_A$ = +25°C | 60 | 69 | | |
| | | | $T_A$ = full range | 55 | | | |

| SHUTDOWN CHARACTERISTICS (THS3115 Only) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $V_{REF}$ | REF pin voltage level | | $V_{CC-}$ | | $V_{CC+}$ – 4 | V |
| $V_{SHDN}$ | SHUTDOWN pin voltage level | Enable | | | REF + 0.8 | V |
| | | Disable | REF + 2 | | | V |
| $I_{CC(SHDN)}$ | Shutdown quiescent current (per channel) | REF = 0 V, $V_{CC}$= ±5 V to ±15 V | | 0.3 | 0.45 | mA |
| $t_{DIS}$ | Disable time (1) | $V_{CC}$= ±15 V | | 200 | | ns |
| $t_{EN}$ | Enable time (1) | $V_{CC}$= ±15 V | | 300 | | ns |
| $I_{IL(SHDN)}$ | Shutdown pin low level leakage current | $V_{CC}$= ±5 V to ±15 V, $V_{SHDN}$ = 0 V, REF = 0 V | | 18 | 25 | µA |
| $I_{IH(SHDN)}$ | Shutdown pin high level leakage current | $V_{CC}$= ±5 V to ±15 V, $V_{SHDN}$ = 3.3 V, REF = 0 V | | 110 | 130 | µA |

(1) Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

## TYPICAL CHARACTERISTICS

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## TYPICAL CHARACTERISTICS

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

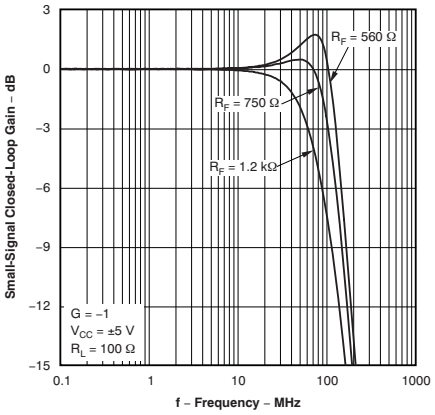



Figure 1.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

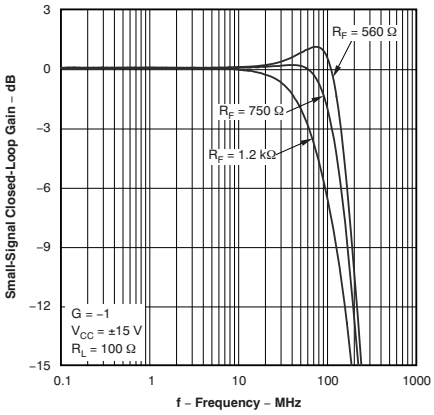



Figure 2.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

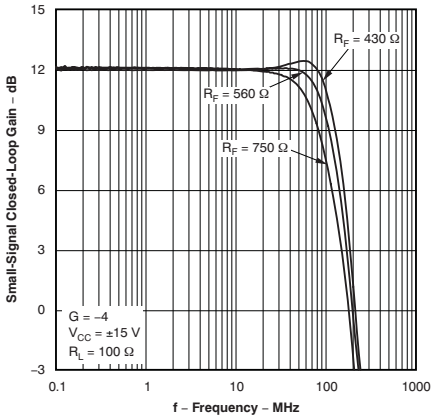



Figure 3.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

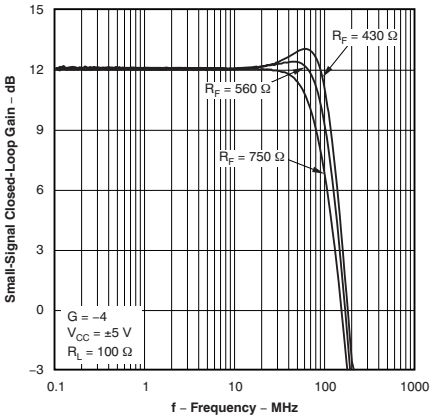



Figure 4.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

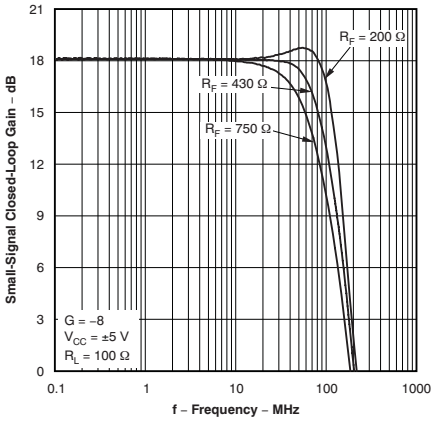



Figure 5.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

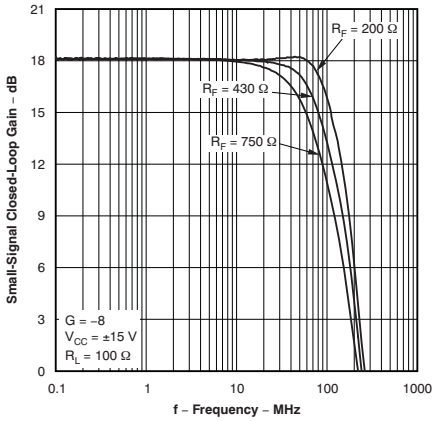



Figure 6.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

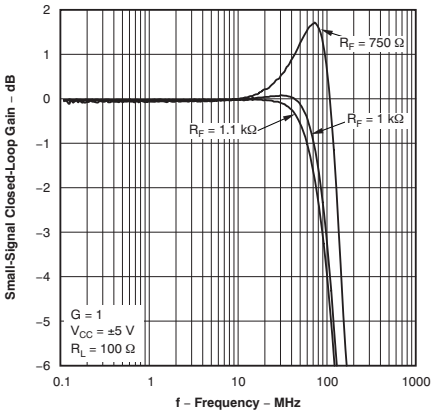



Figure 7.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

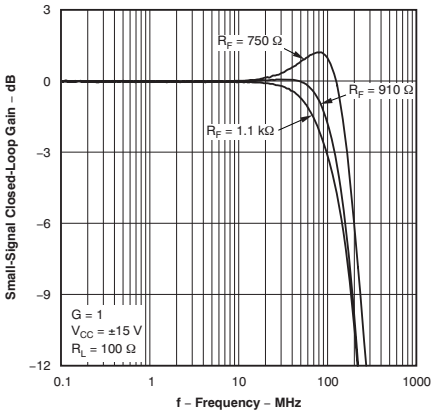



Figure 8.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

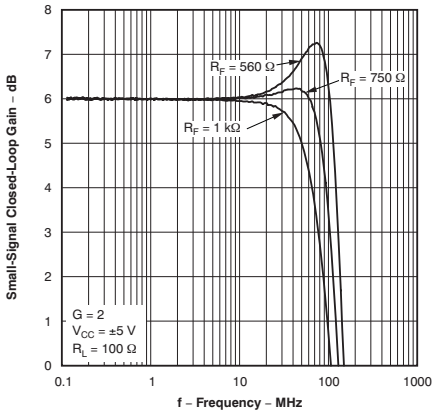



Figure 9.


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## TYPICAL CHARACTERISTICS (continued)

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

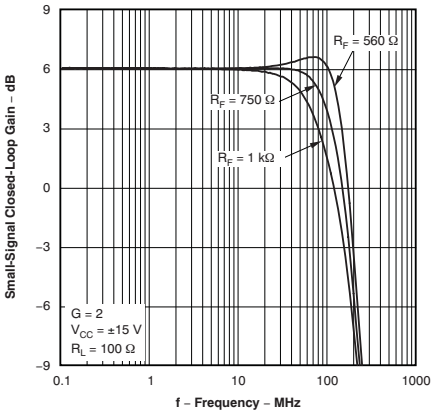



Figure 10.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

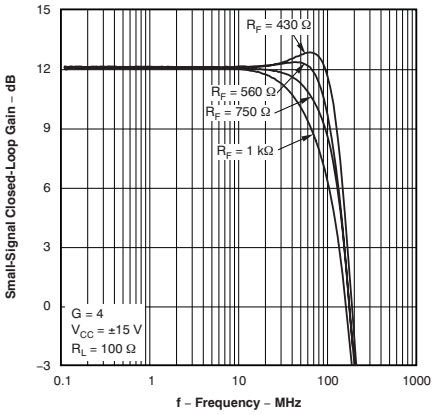



Figure 11.

### GAIN AND PHASE vs FREQUENCY

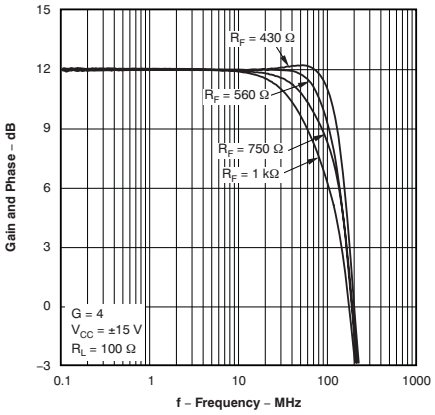



Figure 12.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

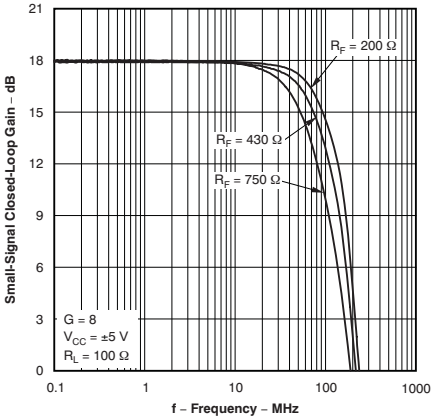



Figure 13.

### SMALL-SIGNAL CLOSED-LOOP GAIN vs FREQUENCY

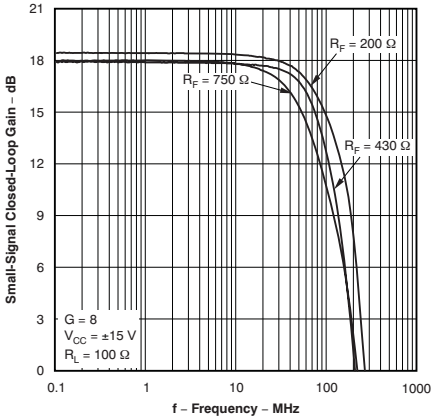



Figure 14.

### SMALL-SIGNAL CLOSED-LOOP NONINVERTING GAIN vs FREQUENCY

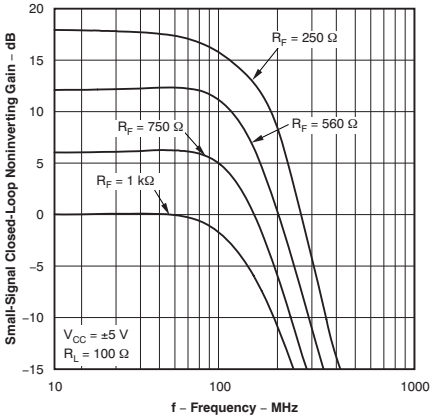



Figure 15.

### SMALL-SIGNAL CLOSED-LOOP NONINVERTING GAIN vs FREQUENCY

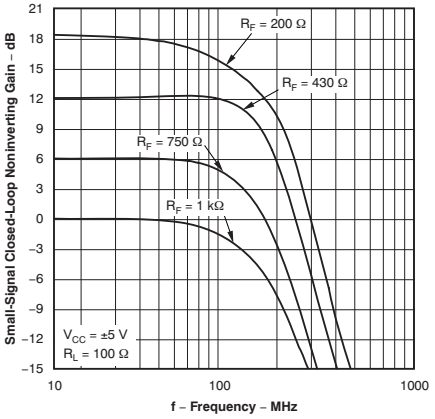



Figure 16.

### SMALL-SIGNAL CLOSED-LOOP INVERTING GAIN vs FREQUENCY

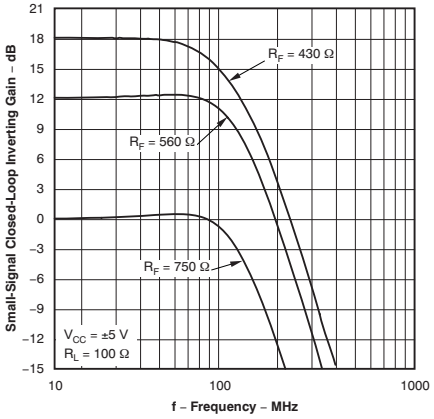



Figure 17.

### SMALL-SIGNAL CLOSED-LOOP INVERTING GAIN vs FREQUENCY

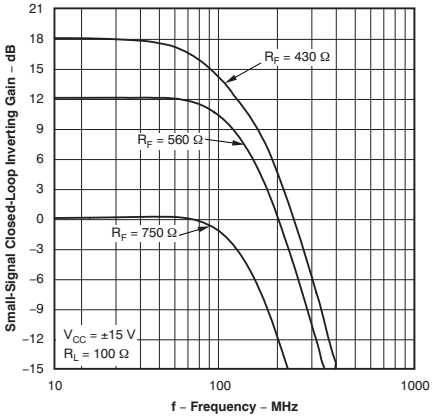



Figure 18.

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## TYPICAL CHARACTERISTICS (continued)

### SMALL- AND LARGE-SIGNAL OUTPUT vs FREQUENCY

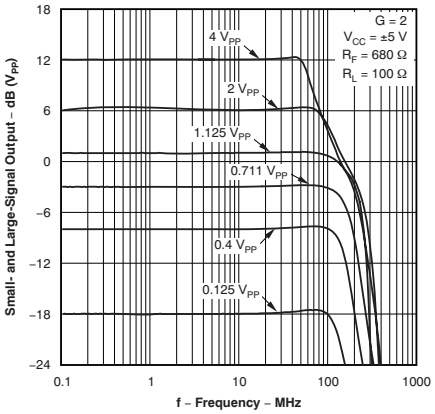



Figure 19.

### SMALL- AND LARGE-SIGNAL OUTPUT vs FREQUENCY

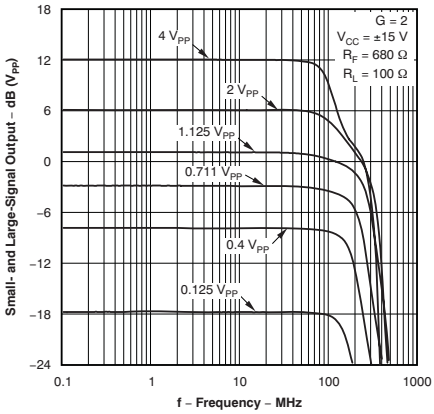



Figure 20.

### HARMONIC DISTORTION vs FREQUENCY

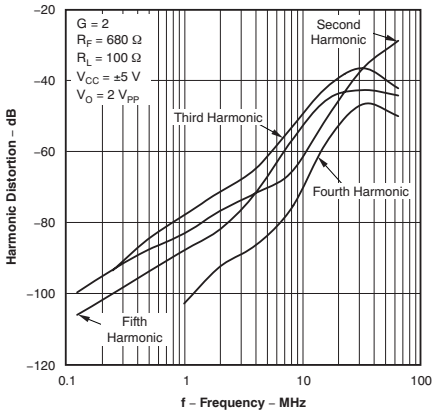



Figure 21.

### HARMONIC DISTORTION vs FREQUENCY

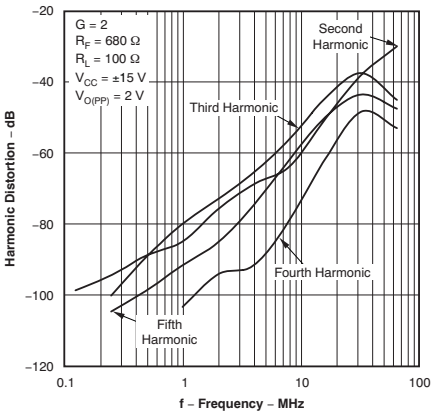



Figure 22.

### HARMONIC DISTORTION vs PEAK-TO-PEAK OUTPUT VOLTAGE

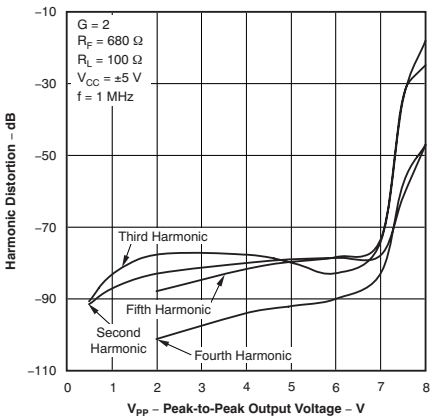



Figure 23.

### HARMONIC DISTORTION vs PEAK-TO-PEAK OUTPUT VOLTAGE

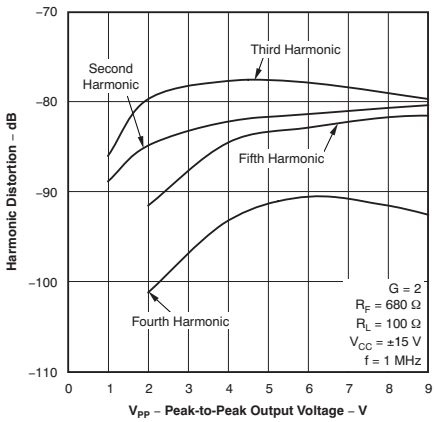



Figure 24.

### VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

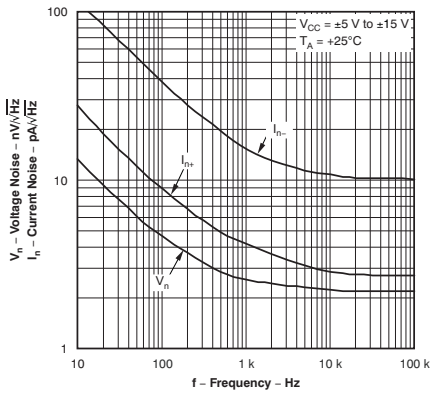



Figure 25.

### COMMON-MODE REJECTION RATIO vs FREQUENCY

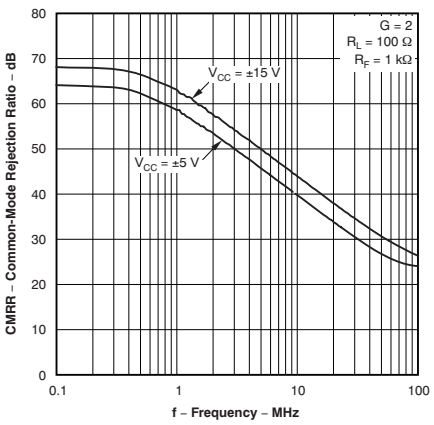



Figure 26.

### POWER-SUPPLY REJECTION RATIO vs FREQUENCY

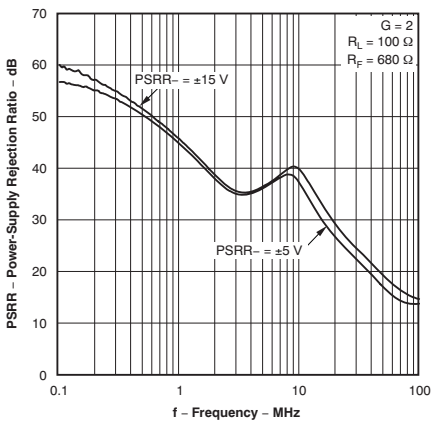



Figure 27.


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## TYPICAL CHARACTERISTICS (continued)

### CROSSTALK vs FREQUENCY

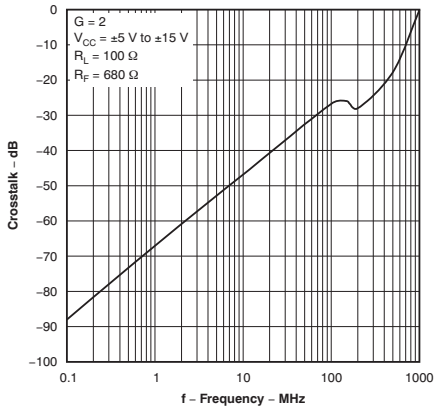



Figure 28.

### OUTPUT IMPEDANCE vs FREQUENCY

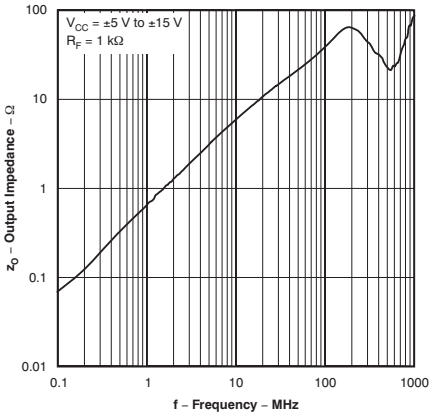



Figure 29.

### SLEW RATE vs OUTPUT VOLTAGE STEP

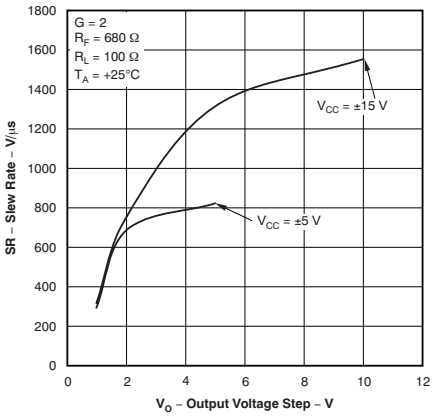



Figure 30.

### INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

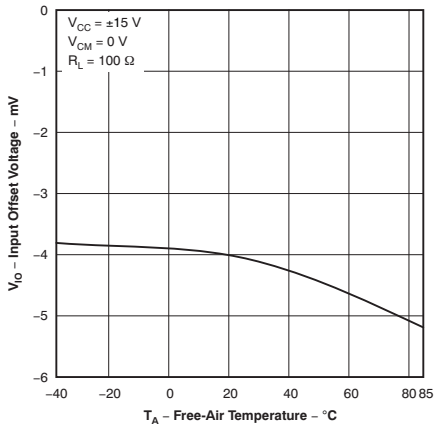



Figure 31.

### INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

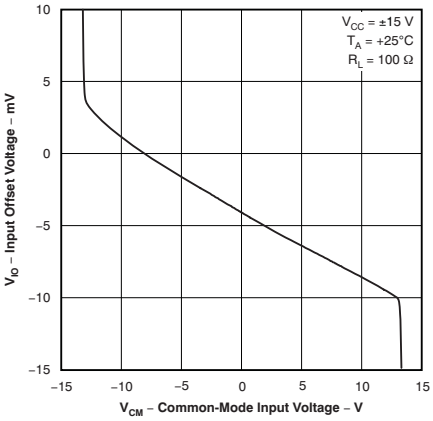



Figure 32.

### INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

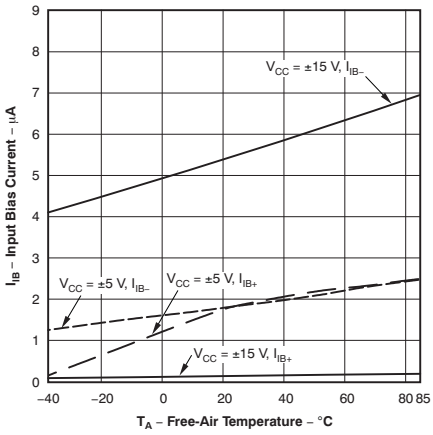



Figure 33.

### OUTPUT VOLTAGE vs OUTPUT CURRENT

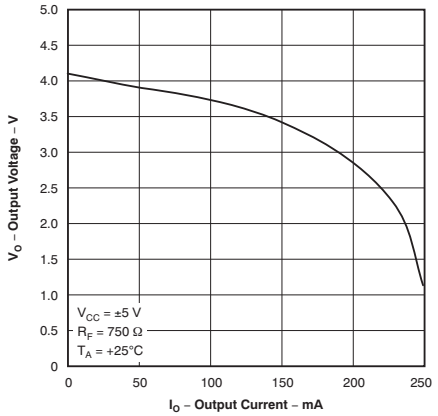



Figure 34.

### OUTPUT VOLTAGE vs OUTPUT CURRENT

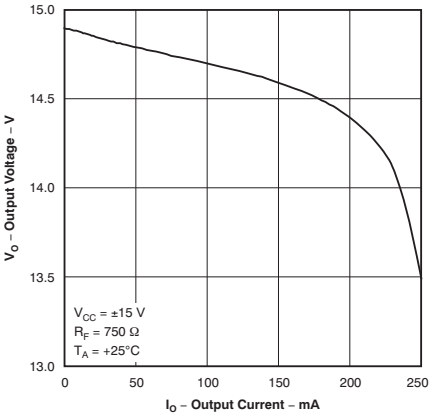



Figure 35.

### OUTPUT VOLTAGE HEADROOM vs OUTPUT CURRENT

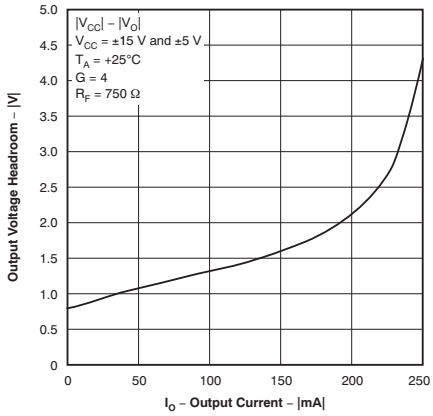



Figure 36.

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## TYPICAL CHARACTERISTICS (continued)

**SUPPLY CURRENT (PER CHANNEL) vs SUPPLY VOLTAGE**

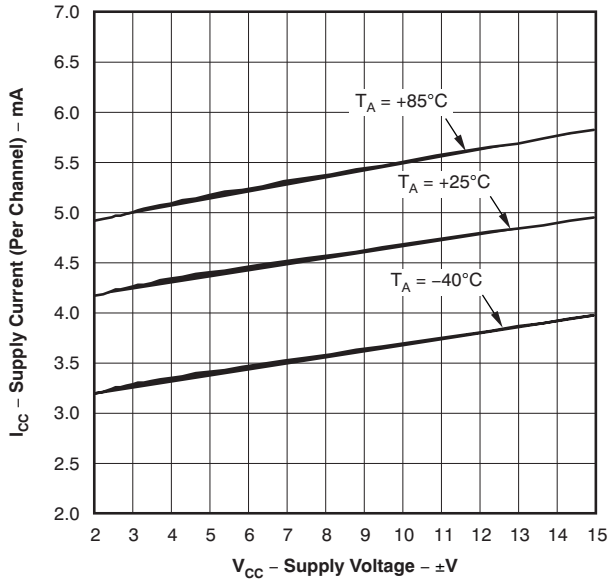



**Figure 37.**

**SHUTDOWN RESPONSE**

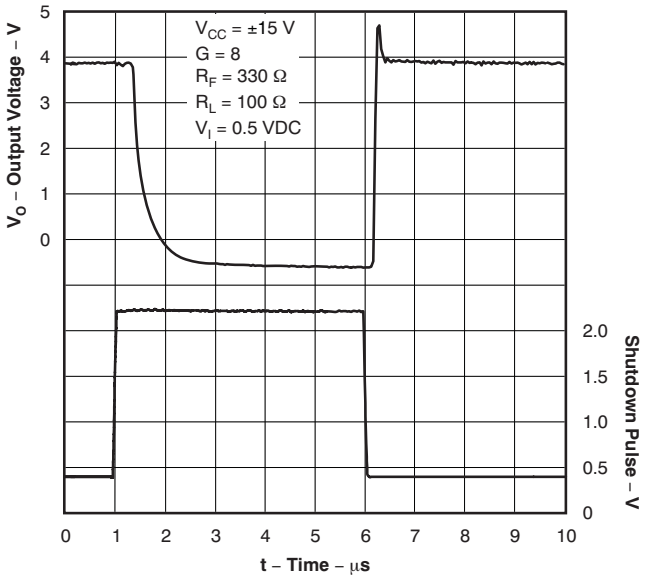



**Figure 38.**


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## APPLICATION INFORMATION

### Maximum Slew Rate for Repetitive Signals

The THS3115 and THS3112 are recommended for high slew rate pulsed applications where the internal nodes of the amplifier have time to stabilize between pulses. It is recommended to have at least a 20-ns delay between pulses.

The THS3115 and THS3112 are not recommended for applications with repetitive signals (sine, square, sawtooth, or other) that exceed 900 V/µs. Using the part in these applications results in excessive current draw from the power supply and possible device damage.

For applications with high slew rate, repetitive signals, the THS3091 and THS3095 (single versions), or THS3092 and THS3096 (dual versions) are recommended.

### Wideband, Noninverting Operation

The THS3115 and THS3112 are unity gain stable 100-MHz current-feedback operational amplifiers, designed to operate from a ±5-V to ±15-V power supply.

Figure 39 shows the THS3115 in a noninverting gain of 2-V/V configuration used to generate the typical characteristic curves. Most of the curves were characterized using signal sources with 50-Ω source impedance and with measurement equipment that presents a 50-Ω load impedance.

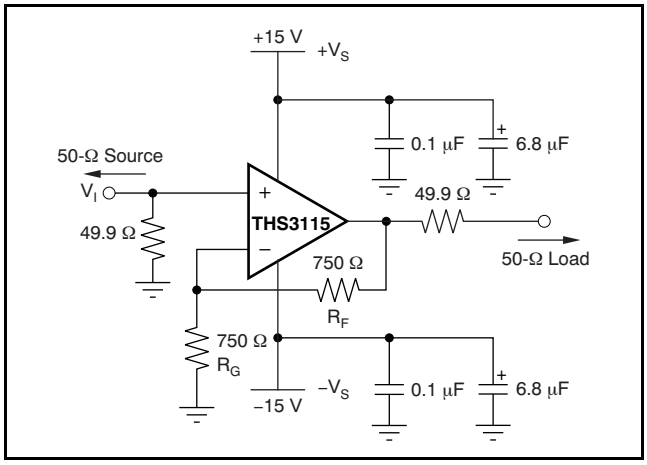



**Figure 39. Wideband, Noninverting Gain Configuration**

Current-feedback amplifiers are highly dependent on the feedback resistor $R_F$ for maximum performance and stability. Table 1 shows the optimal gain setting resistors $R_F$ and $R_G$ at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for $R_F$. Conversely, increasing $R_F$ decreases the bandwidth, but stability is improved.

**Table 1. Recommended Resistor Values for Optimum Frequency Response**

| THS3115 and THS3112 $R_F$ and $R_G$ VALUES FOR MINIMAL PEAKING WITH $R_L$ = 50 Ω, ±5-V to ±15-V POWER SUPPLY | | |
|---|---|---|
| GAIN (V/V) | $R_G$ (Ω) | $R_F$ (Ω) |
| 1 | — | 1 k |
| 2 | 750 | 750 |
| 4 | 187 | 560 |
| 8 | 28.7 | 200 |
| –1 | 750 | 750 |
| –4 | 140 | 560 |
| –8 | 53.6 | 430 |

### Wideband, Inverting Operation

Figure 40 shows the THS3115 in a typical inverting gain configuration designed for 50-Ω input/output.

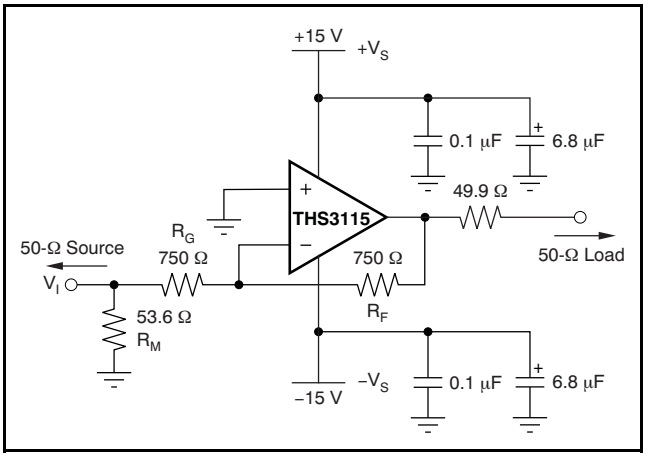



**Figure 40. Wideband, Inverting Gain Configuration**

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## Single-Supply Operation

The THS3115 and THS3112 have the capability to operate from a single supply voltage ranging from 10 V to 30 V. When operating from a single power supply, biasing the input and output at mid-supply allows for the maximum output voltage swing. The circuits in Figure 41 show inverting and noninverting amplifiers configured for single-supply operation.

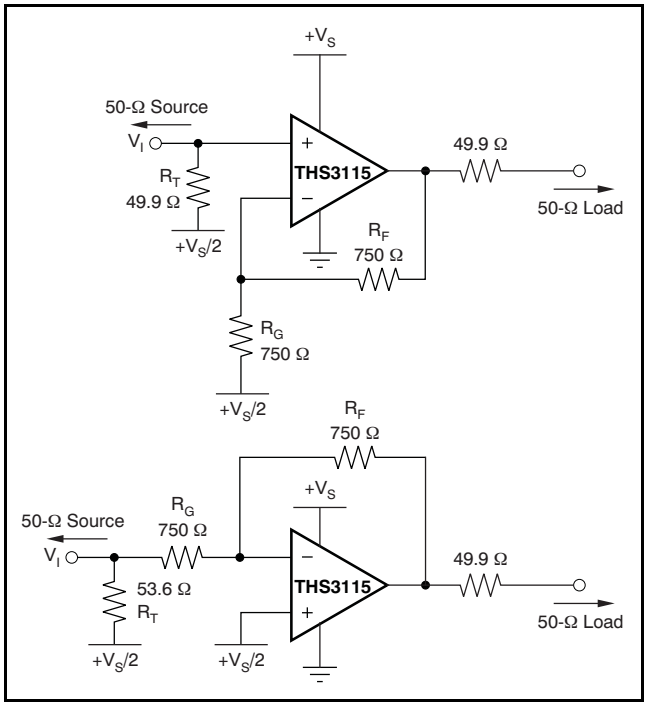



**Figure 41. DC-Coupled, Single-Supply Operation**

## Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3115 and THS3112 match the demands for video distribution to deliver video signals down multiple cables. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal, and supports component video and RGB video signals that require fast transition times and fast settling times for high signal quality. Figure 42 illustrates a typical video distribution amplifier application configuration.

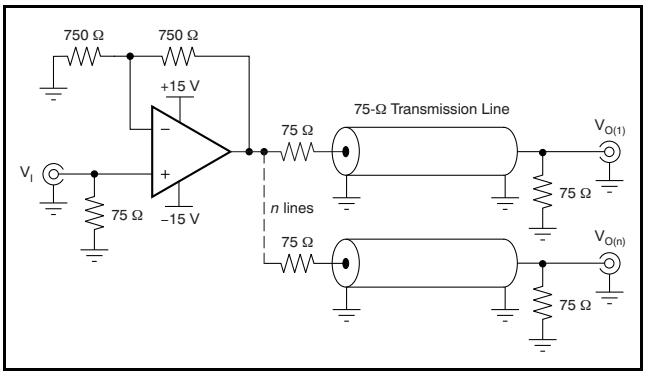



**Figure 42. Video Distribution Amplifier Application**

## Driving Capacitive Loads

Applications such as FET drivers and line drivers can be highly capacitive and cause stability problems for high-speed amplifiers.

Figure 43 through Figure 49 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier feedback path. See Figure 43 for recommended resistor values versus capacitive load.

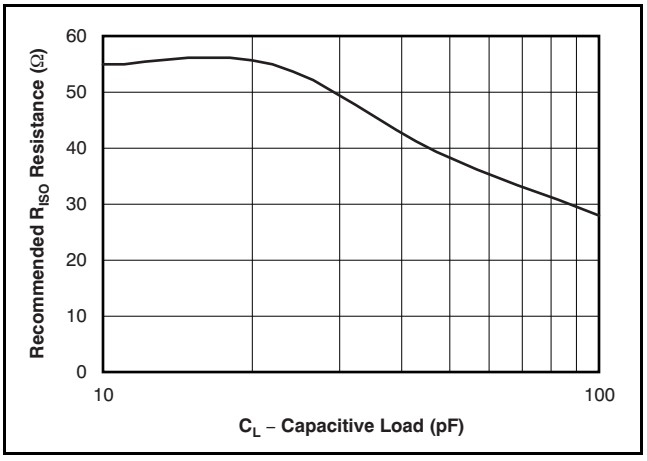



**Figure 43. Recommended $R_{ISO}$ vs Capacitive Load**


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Placing a small series resistor, $R_{ISO}$, between the amplifier output and the capacitive load, as shown in Figure 44, is an easy way of isolating the load capacitance.

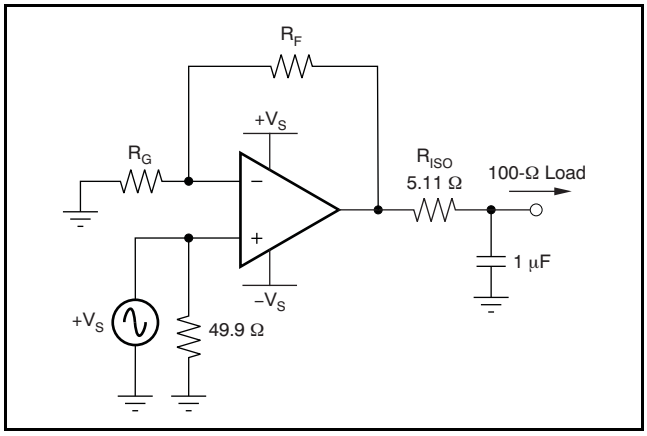



**Figure 44. Resistor to Isolate Capacitive Load**

Using a ferrite chip in place of $R_{ISO}$, as Figure 45 shows, is another approach of isolating the output of the amplifier. The ferrite impedance characteristic versus frequency is useful to maintain the low frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. Use a ferrite with similar impedance to $R_{ISO}$, 20 Ω to 50 Ω, at 100 MHz and low impedance at dc.

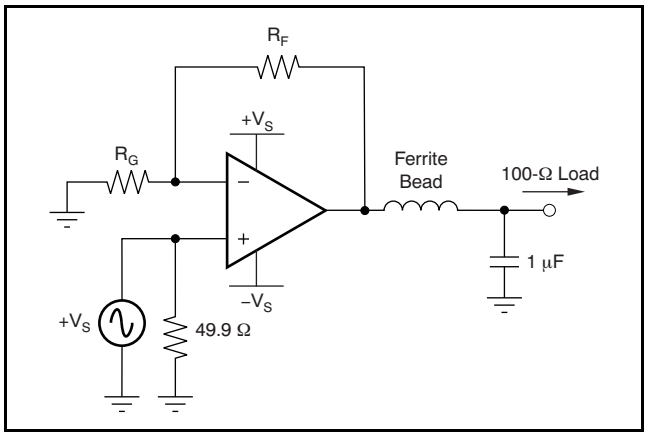



**Figure 45. Ferrite Bead to Isolate Capacitive Load**

Figure 46 shows another method used to maintain the low-frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. At low frequency, feedback is mainly from the load side of $R_{ISO}$. At high frequency, the feedback is mainly via the 27-pF capacitor. The resistor $R_{IN}$ in series with the negative input is used to stabilize the amplifier and should be equal to the recommended value of $R_F$ at unity gain. Replacing $R_{IN}$ with a ferrite of similar impedance at about 100 MHz as shown in Figure 47 gives similar results with reduced dc offset and low frequency noise.

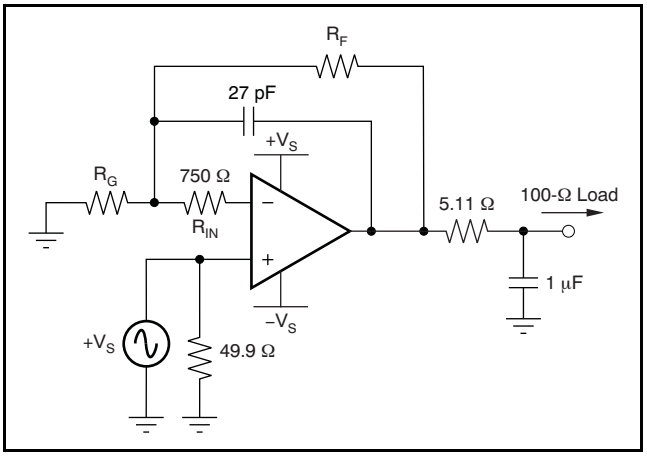



**Figure 46. Feedback Technique with Input Resistor for Capacitive Load**

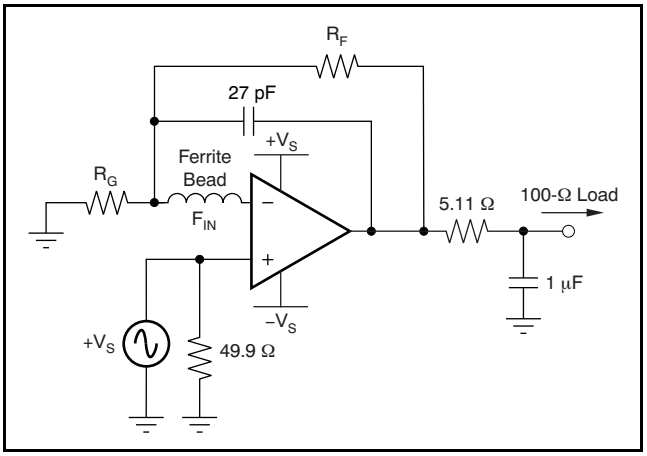



**Figure 47. Feedback Technique with Input Ferrite Bead for Capacitive Load**

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Figure 48 shows a configuration that uses two amplifiers in parallel to double the output drive current to larger capacitive loads. This technique is used when more output current is needed to charge and discharge the load faster as when driving large FET transistors.

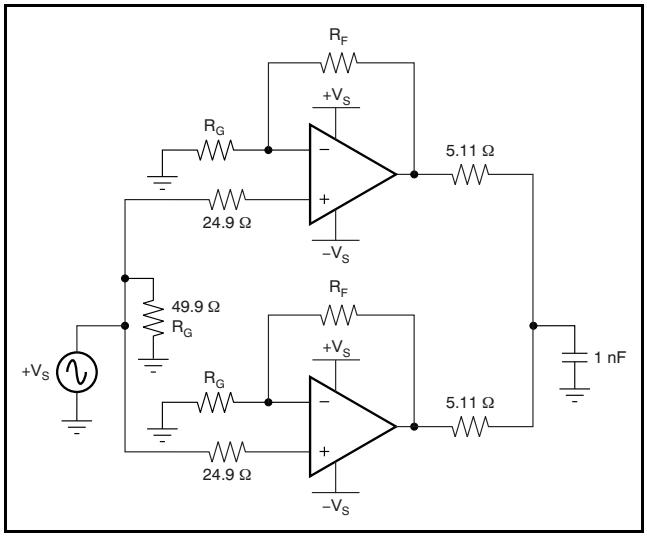



**Figure 48. Parallel Amplifiers for Higher Output Drive**

Figure 49 shows a push-pull FET driver circuit typical of ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

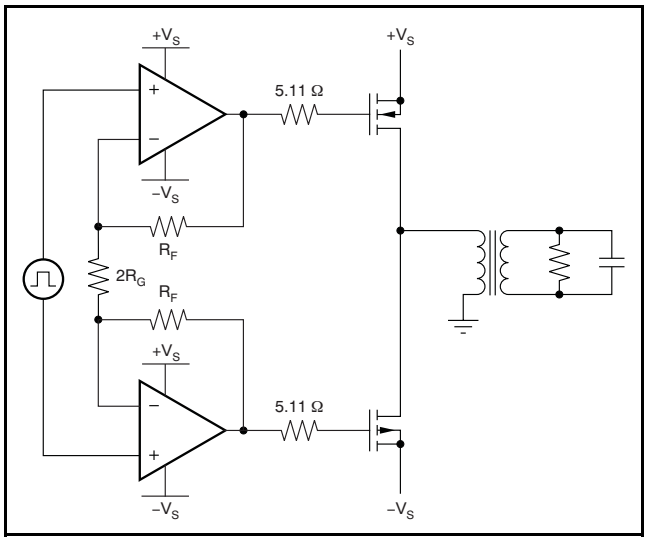



**Figure 49. PowerFET Drive Circuit**

## Saving Power with Shutdown Functionality and Setting Threshold Levels with the Reference Pin

The THS3115 features a shutdown pin (SHUTDOWN) that lowers the quiescent current from 4.9 mA/amp down to 300 µA/amp, ideal for reducing system power.

The shutdown pin of the amplifier defaults to the REF pin voltage in the absence of an applied voltage, putting the amplifier in the normal on mode of operation. To turn off the amplifier in an effort to conserve power, the shutdown pin can be driven towards the positive rail. The threshold voltages for power-on and power-down (or shutdown) are relative to the supply rails and are given in the *Shutdown Characteristics* table. Below the *Enable* threshold voltage, the device is on. Above the *Disable* threshold voltage, the device is off. Behavior between these threshold voltages is not specified.

Note that this shutdown functionality is self-defining: the amplifier consumes less power in shutdown mode. The shutdown mode is not intended to provide a high-impedance output. In other words, the shutdown functionality is not intended to allow use as a 3-state bus driver. When in shutdown mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

As with most current feedback amplifiers, the internal architecture places some limitations on the system when in shutdown mode. Most notably is the fact that the amplifier actually turns *on* if there is a ±0.7 V or greater difference between the two input nodes (IN+ and IN–) of the amplifier. If this difference exceeds ±0.7 V, the output of the amplifier creates an output voltage equal to approximately [(IN+ – IN–) – 0.7V] × Gain. Also, if a voltage is applied to the output while in shutdown mode, the IN– node voltage is equal to $V_{O(applied)} \times R_G/(R_F + R_G)$ . For low gain configurations and a large applied voltage at the output, the amplifier may actually turn on because of the behavior described here.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.


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## Power-Down Reference Pin Operation

In addition to the shutdown pin, the THS3115 features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the SHUTDOWN pin. In most split-supply applications, the reference pin is connected to ground. In either case, the user needs to be aware of voltage-level thresholds that apply to the shutdown pin. Table 2 shows examples and illustrate the relationship between the reference voltage and the shutdown thresholds. In the table, the threshold levels are derived by the following equations:

SHUTDOWN ≤ REF + 0.8 V for enable

SHUTDOWN ≥ REF + 2V for disable

Where the usable range at the REF pin is:

$V_{CC-} \le V_{REF} \le (V_{CC+} - 4V)$

The recommended mode of operation is to tie the REF pin to midrail, therefore setting the enable/disable thresholds to $V_{(midrail)}$ + 0.8 V and $V_{(midrail)}$ = 2 V, respectively.

**Table 2. Shutdown Threshold Voltage Levels**

| SUPPLY VOLTAGE (V) | REFERENCE PIN VOLTAGE (V) | ENABLE LEVEL (V) | DISABLE LEVEL (V) |
|---|---|---|---|
| ±15, ±5 | 0 | 0.8 | 2.0 |
| ±15 | 2.0 | 2.8 | 4.0 |
| ±15 | –2.0 | –1.2 | 0 |
| ±5 | 1.0 | 1.8 | 3.0 |
| ±5 | –1.0 | –0.2 | 1.0 |
| +30 | 15.0 | 15.8 | 17 |
| +10 | 5.0 | 5.8 | 7.0 |

Note that if the REF pin is left unterminated, it floats to the positive rail and falls outside of the recommended operating range given above $V_{CC-} \le V_{REF} \le (V_{CC+} - 4V)$. As a result, it no longer serves as a reliable reference for the SHUTDOWN pin, and the enable/disable thresholds given above no longer apply. If the SHUTDOWN pin is also left unterminated, it floats to the positive rail and the device is disabled. If balanced, split supplies are used ($\pm V_{CC}$) and the REF and SHUTDOWN pins are grounded, the device is enabled.

## Printed-Circuit Board Layout Techniques for Optimal Performance

Achieving optimum performance with high-frequency amplifiers such as the THS3115 and THS3112 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance [0.25 inch, (6,4 mm)] from the power-supply pins to high-frequency 0.1-µF and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (6.8 µF or more) tantalum decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the printed circuit board (PCB).
- Careful selection and placement of external components preserve the high-frequency performance of the THS3115 and THS3112. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep the leads and PCB trace length as short as possible. Never use wirebound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance that shunts the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can affect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.

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- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces [0.05 inch (1,3 mm) to 0.1 inch (2,54 mm)] should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (less than 4 pF) may not need an $R_S$ because the THS3115 and THS3112 are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_S$ are allowed as the signal gain increases (thus increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3115/THS3112 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.
- Socketing a high-speed device such as the THS3115 and THS3112 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3115/THS3112 amplifiers directly onto the board.

## PowerPAD™ Design Considerations

The THS3115 and THS3112 are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 50(a) and Figure 50(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 50(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that devices such as the THS311x have no electrical connection between the PowerPAD and the die.

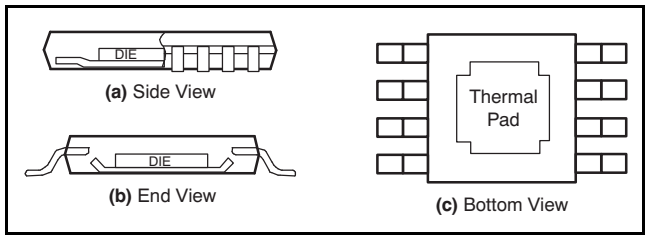


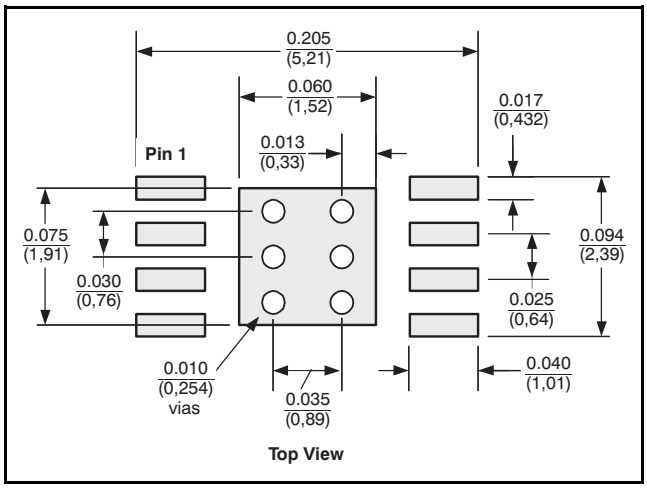

**Figure 50. Views of Thermally-Enhanced Package**

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.


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## PowerPAD™ Layout Considerations




Dimensions are in inches (millimeters).

**Figure 51. DGN PowerPAD PCB Etch and Via Pattern**

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

1. PCB with a top side etch pattern as shown in Figure 51.
2. Place five holes in the area of the thermal pad. These holes should be 0.01 inch (0,254 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the THS3115/THS3112 IC. These additional vias may be larger than the 0.01-inch (0,254-mm) diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane. Note that the PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage, such as $V_{S-}$, is acceptable as there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application; however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3115/THS3112 PowerPAD package should make the connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This procedure results in a part that is properly installed.

## Power Dissipation and Thermal Considerations

The THS3115 and THS3112 incorporate automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately +160°C. When the junction temperature reduces to approximately +140°C, the amplifier turns on again. However, for maximum performance and reliability, the designer must take care to ensure that the design does not exceed a junction temperature of +125°C. Between +125°C and +150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{DMax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:

- $P_{DMax}$ is the maximum power dissipation in the amplifier (W)
- $T_{max}$ is the absolute maximum junction temperature (°C)
- $T_A$ is the ambient temperature (°C)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

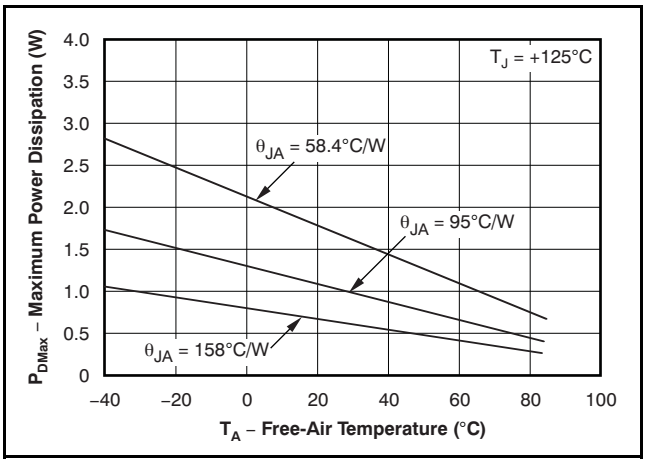
where:

- $\theta_{JC}$ is the thermal coefficient from the silicon junctions to the case (°C/W)
- $\theta_{CA}$ is the thermal coefficient from the case to ambient air (°C/W)

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For systems where heat dissipation is more critical, the THS3115 and THS3112 are also available in an 8-pin MSOP with PowerPAD package that offers even better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in Figure 52 for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines discussed above and detailed in the PowerPAD application note (literature number SLMA002). Figure 52 also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially, which may cause serious heat and performance issues. Always solder the PowerPAD to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this type of dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.




Results shown are with no air flow and PCB size of 3 in × 3 in (76,2 mm × 76,2 mm).

- $\theta_{JA}$ = 58.4°C/W for 8-pin MSOP with PowerPAD (DGN package)
- $\theta_{JA}$ = 95°C/W for 8-pin SOIC High-K test PCB (D package)
- $\theta_{JA}$ = 158°C/W for 8-pin MSOP with PowerPAD without solder

**Figure 52. Maximum Power Dissipation vs Ambient Temperature**


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## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (October, 2009) to Revision C** **Page**

- Corrected pin designations for TSSOP pinout drawing ..... 1
- Deleted *Shutdown pin input levels* parameters from Recommended Operating Conditions table ..... 3
- Added $V_{REF}$ parameter to Shutdown Characteristics table ..... 5
- Added $V_{SHDN}$ parameter to Shutdown Characteristics table ..... 5
- Changed reference to GND pin to "REF" in *Shutdown quiescent current* parameter test conditions in Shutdown Characteristics table ..... 5
- Added REF = 0 V to test conditions for $I_{IL(SHDN)}$ parameter in Shutdown Characteristics table ..... 5
- Added REF = 0 V to test conditions for $I_{IH(SHDN)}$ parameter in Shutdown Characteristics table ..... 5
- Revised *Saving Power with Shutdown Functionality and Setting Threshold Levels with the Reference Pin* section ..... 14
- Updated *Power-Down Reference Pin Operation* section; changed references to $V_{S–}$, $V_{S+}$ to $V_{CC–}$, $V_{CC+}$ ..... 15

**Changes from Revision A (January, 2009) to Revision B** **Page**

- Updated document format to conform to current standards ..... 1
- Deleted lead temperature specification from *Absolute Maximum Ratings* table ..... 2
- Added *Application Information* section ..... 11

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| THS3112CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3112C | Samples |
| THS3112CDDA | ACTIVE | SO PowerPAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | 0 to 70 | 3112C | Samples |
| THS3112CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3112C | Samples |
| THS3112CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3112C | Samples |
| THS3112ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3112I | Samples |
| THS3112IDDA | ACTIVE | SO PowerPAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 3112I | Samples |
| THS3112IDDAR | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 3112I | Samples |
| THS3115CPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | HS3115C | Samples |
| THS3115CPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | HS3115C | Samples |
| THS3115ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | THS3115I | Samples |
| THS3115IPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HS3115I | Samples |
| THS3115IPWPG4 | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HS3115I | Samples |
| THS3115IPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HS3115I | Samples |
| THS3115IPWPRG4 | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HS3115I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

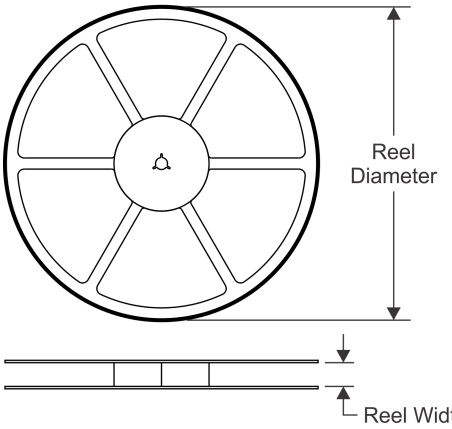
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

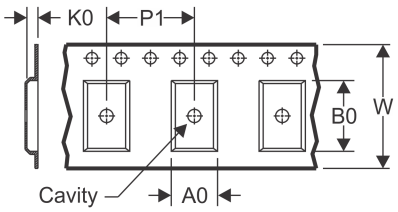
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

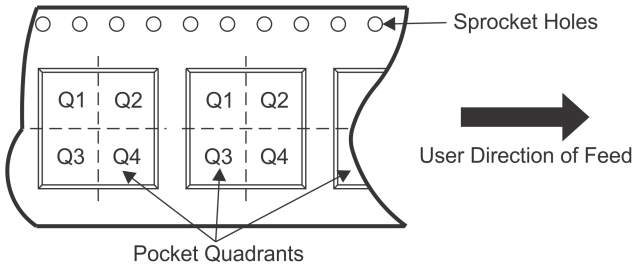



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

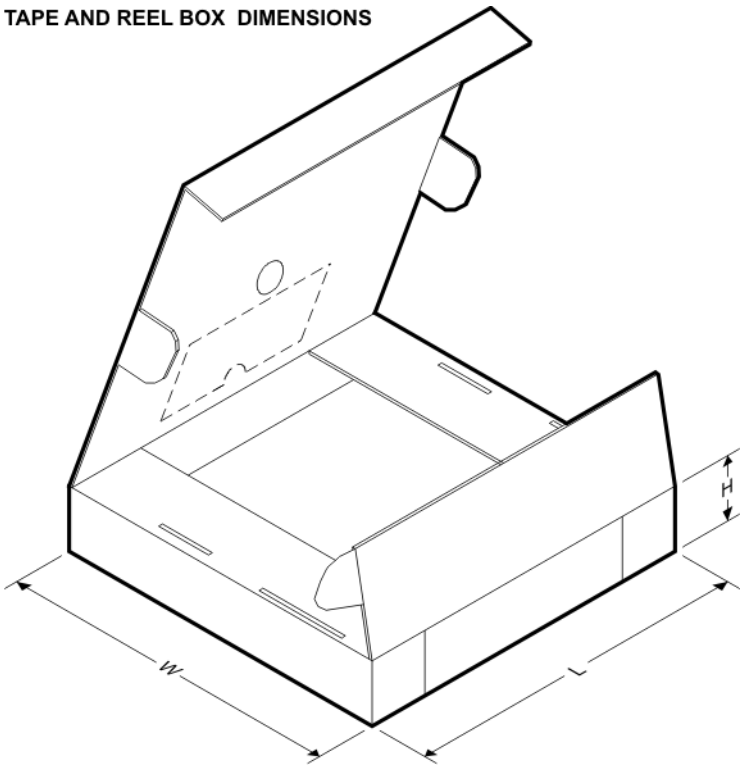
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THS3112CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS3112IDDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| THS3115CPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| THS3115IPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

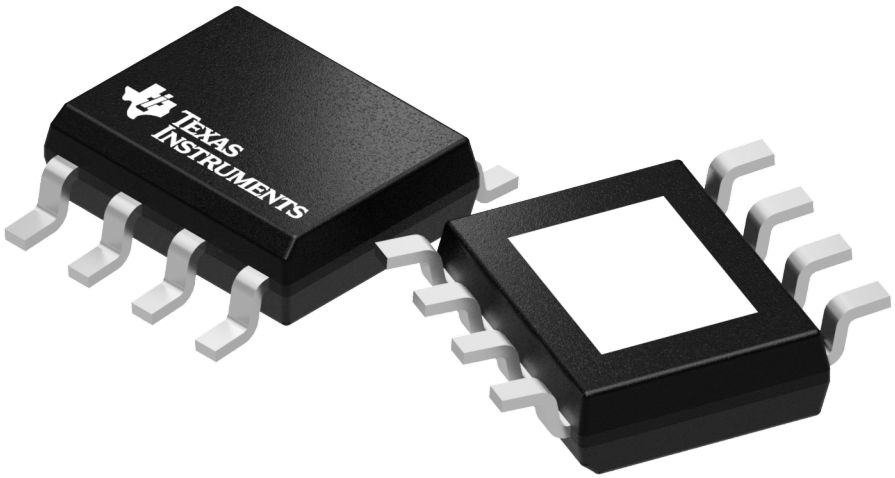



*All dimensions are nominal

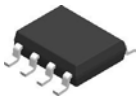
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THS3112CDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| THS3112IDDAR | SO PowerPAD | DDA | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| THS3115CPWPR | HTSSOP | PWP | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| THS3115IPWPR | HTSSOP | PWP | 14 | 2000 | 350.0 | 350.0 | 43.0 |

# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

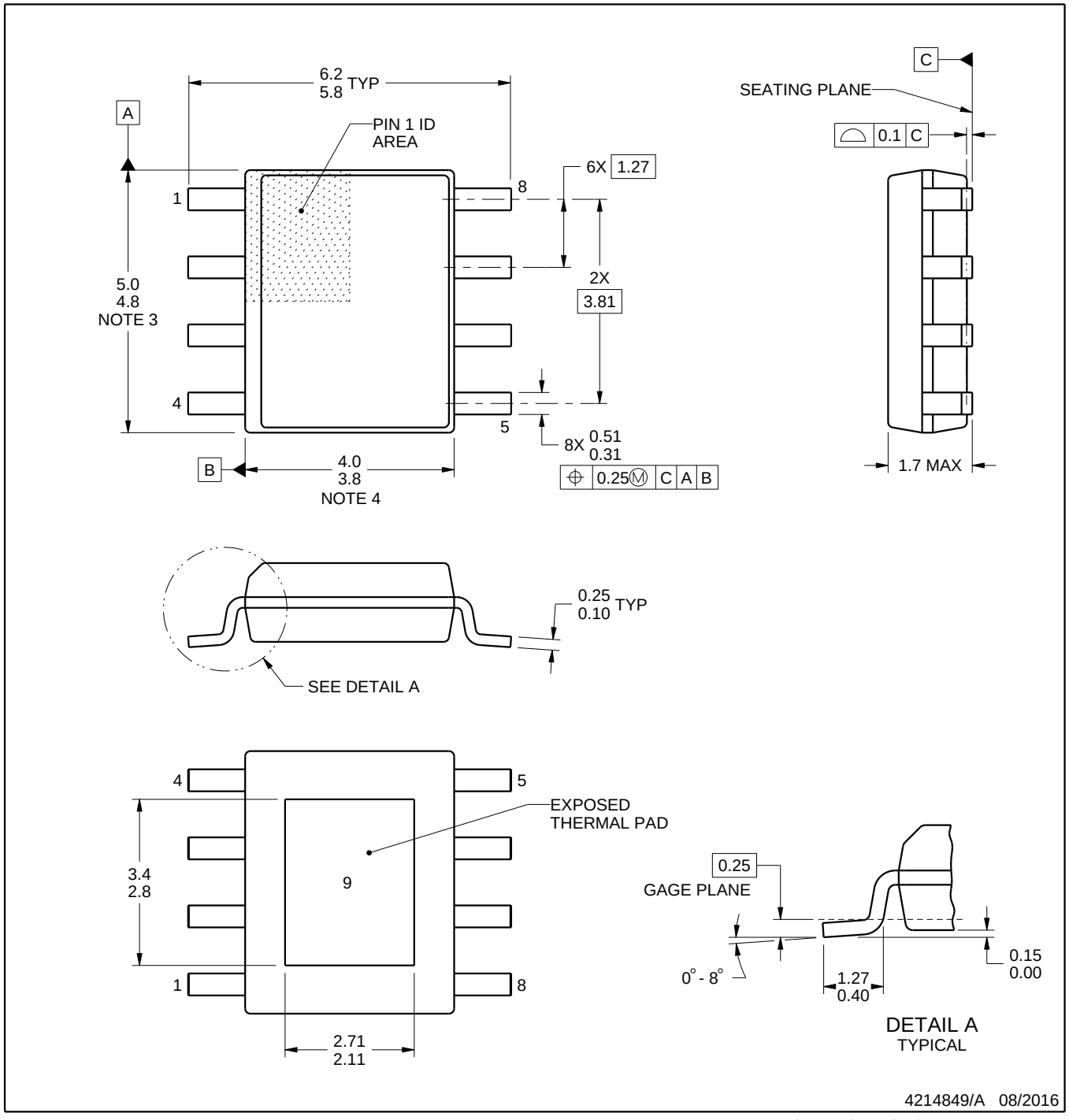


# PACKAGE OUTLINE

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

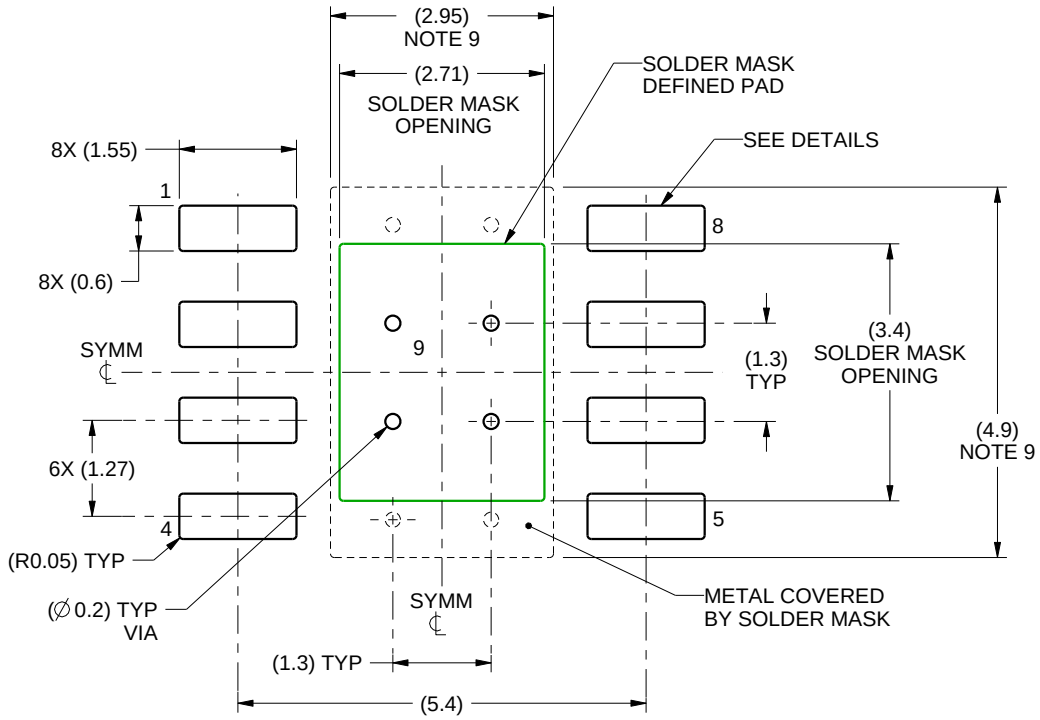
PLASTIC SMALL OUTLINE



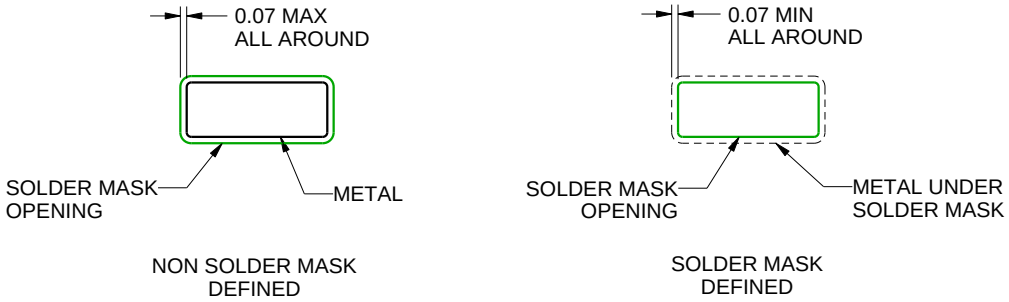

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

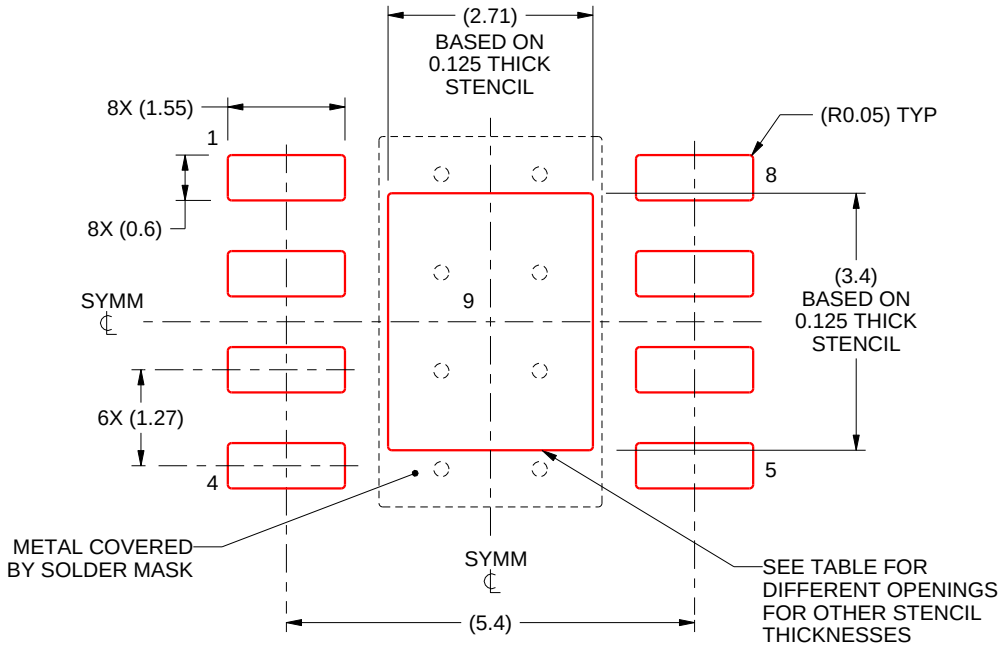
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

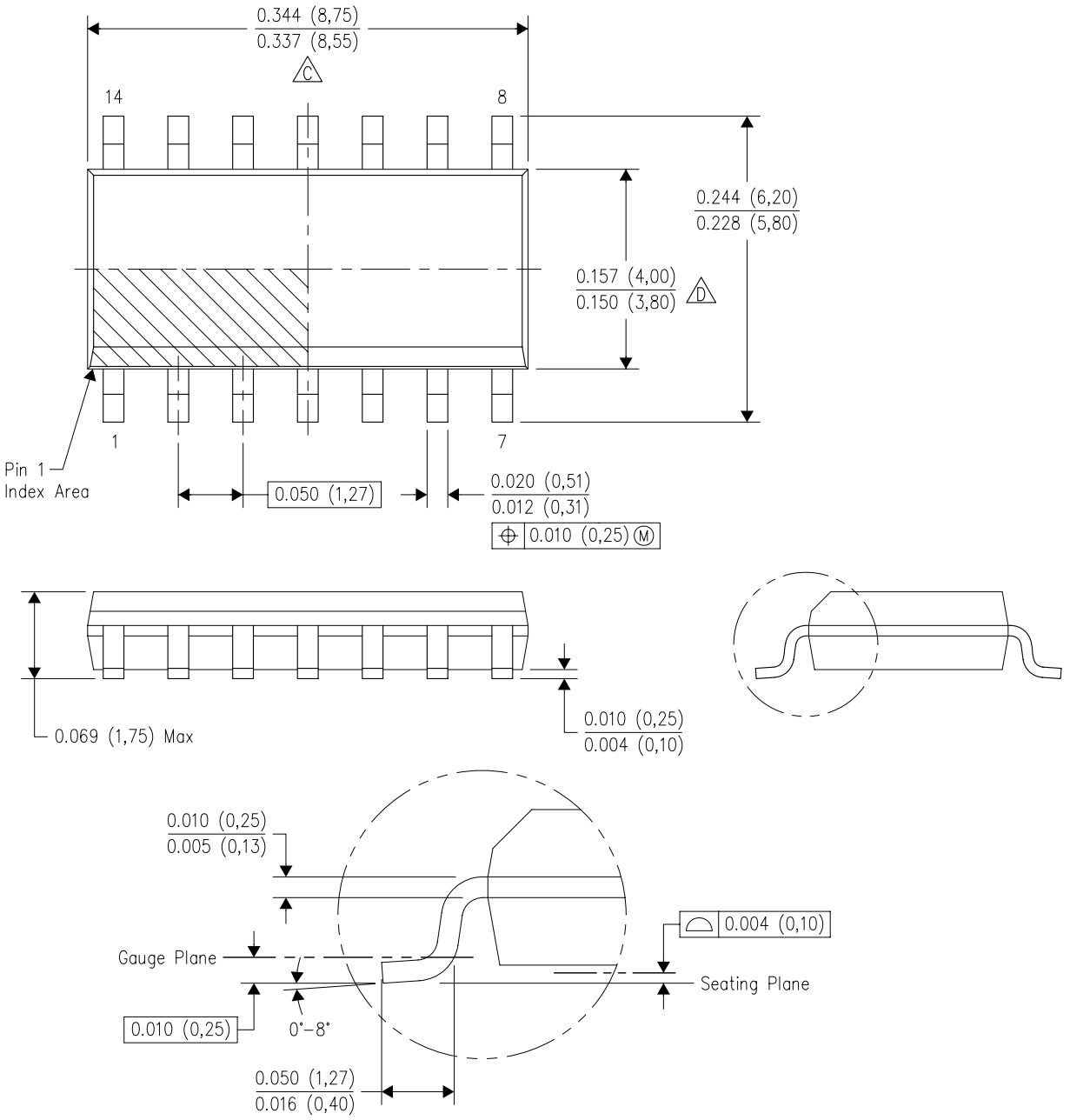
| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

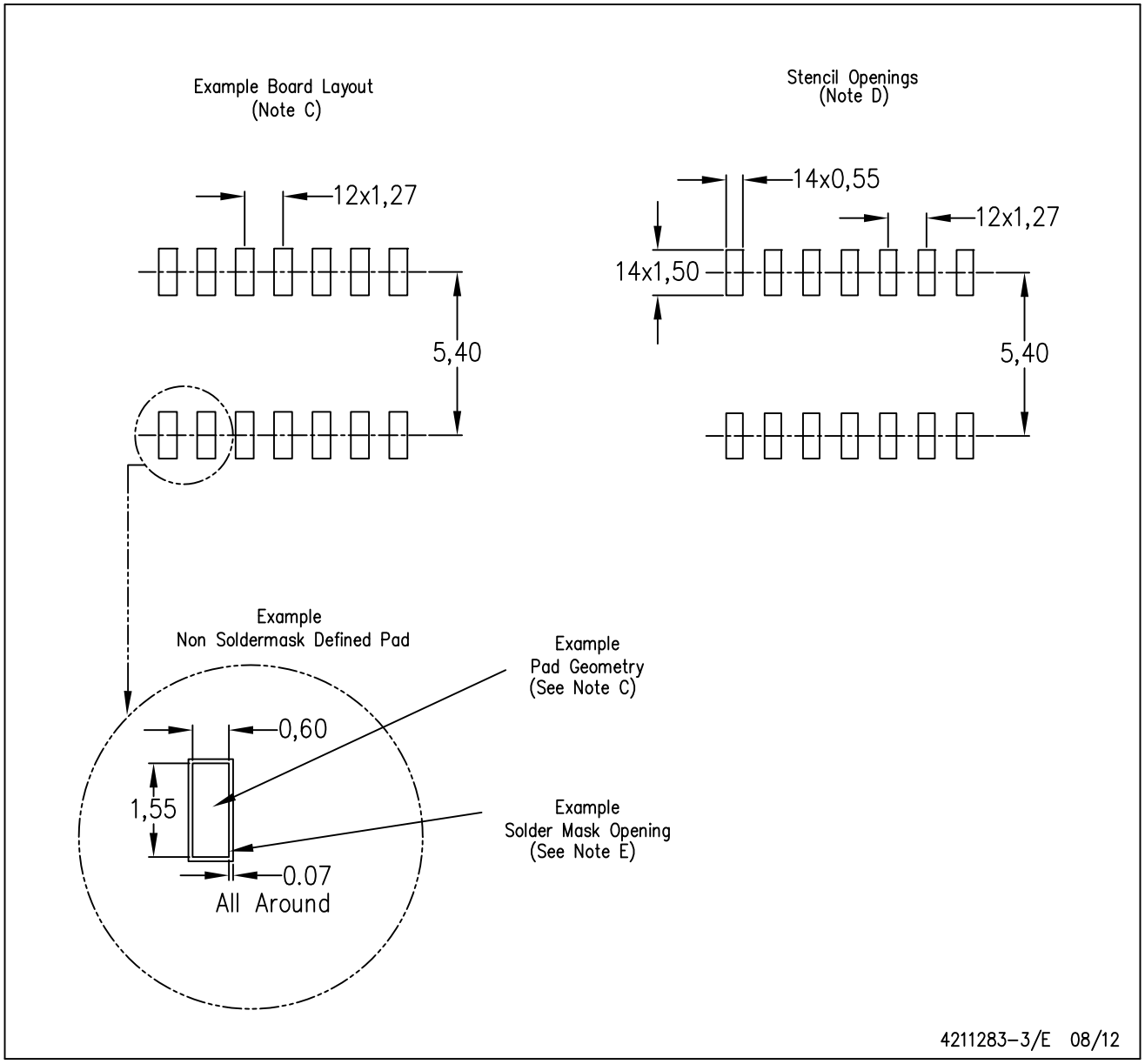
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



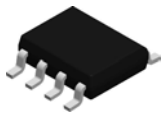

4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

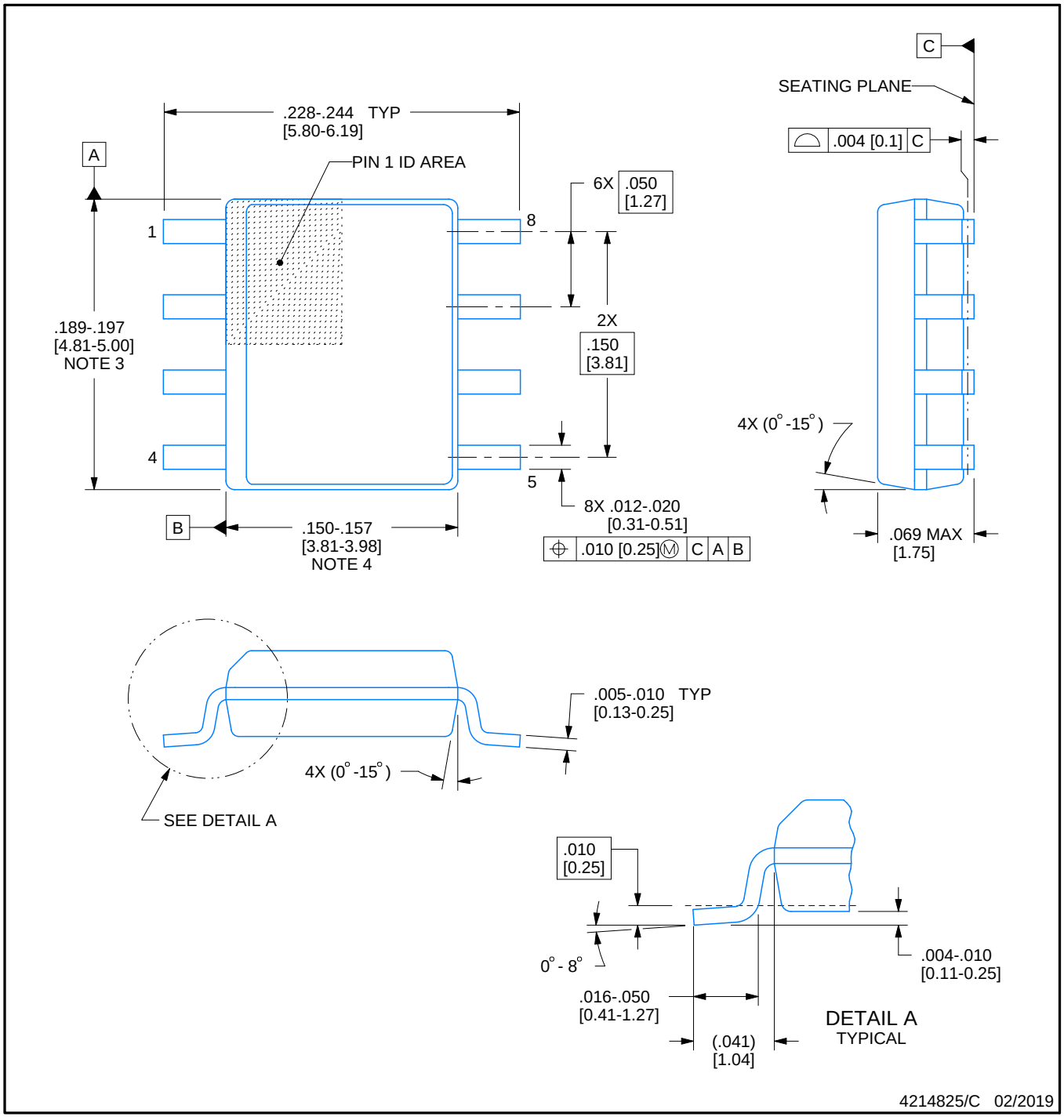


# PACKAGE OUTLINE

## D0008A

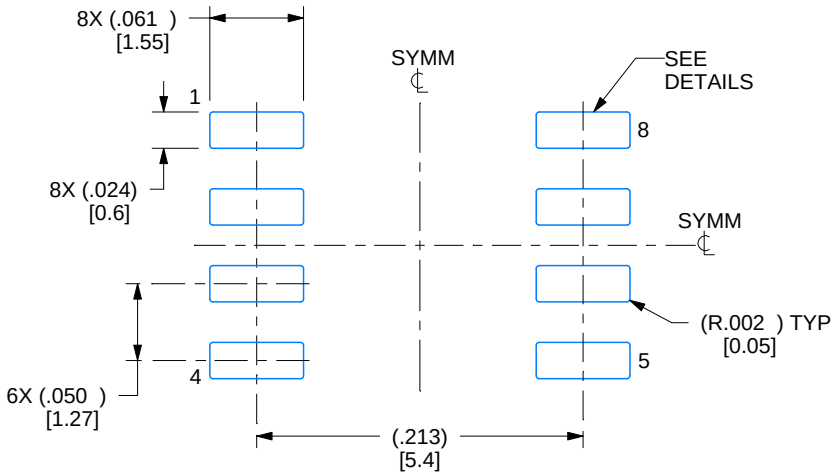
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

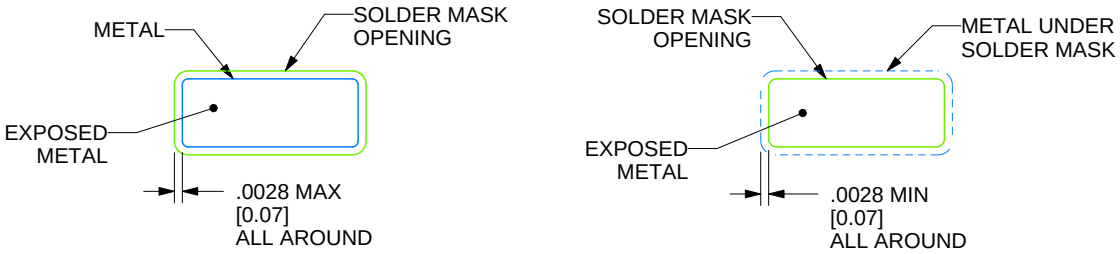



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

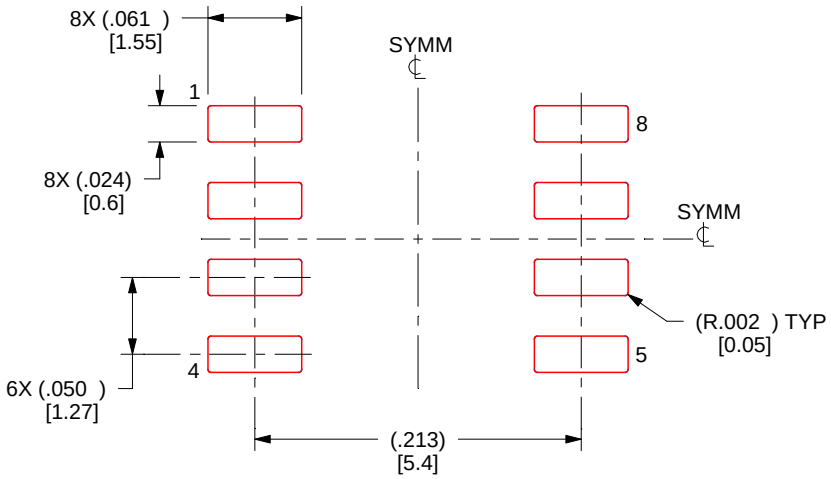
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



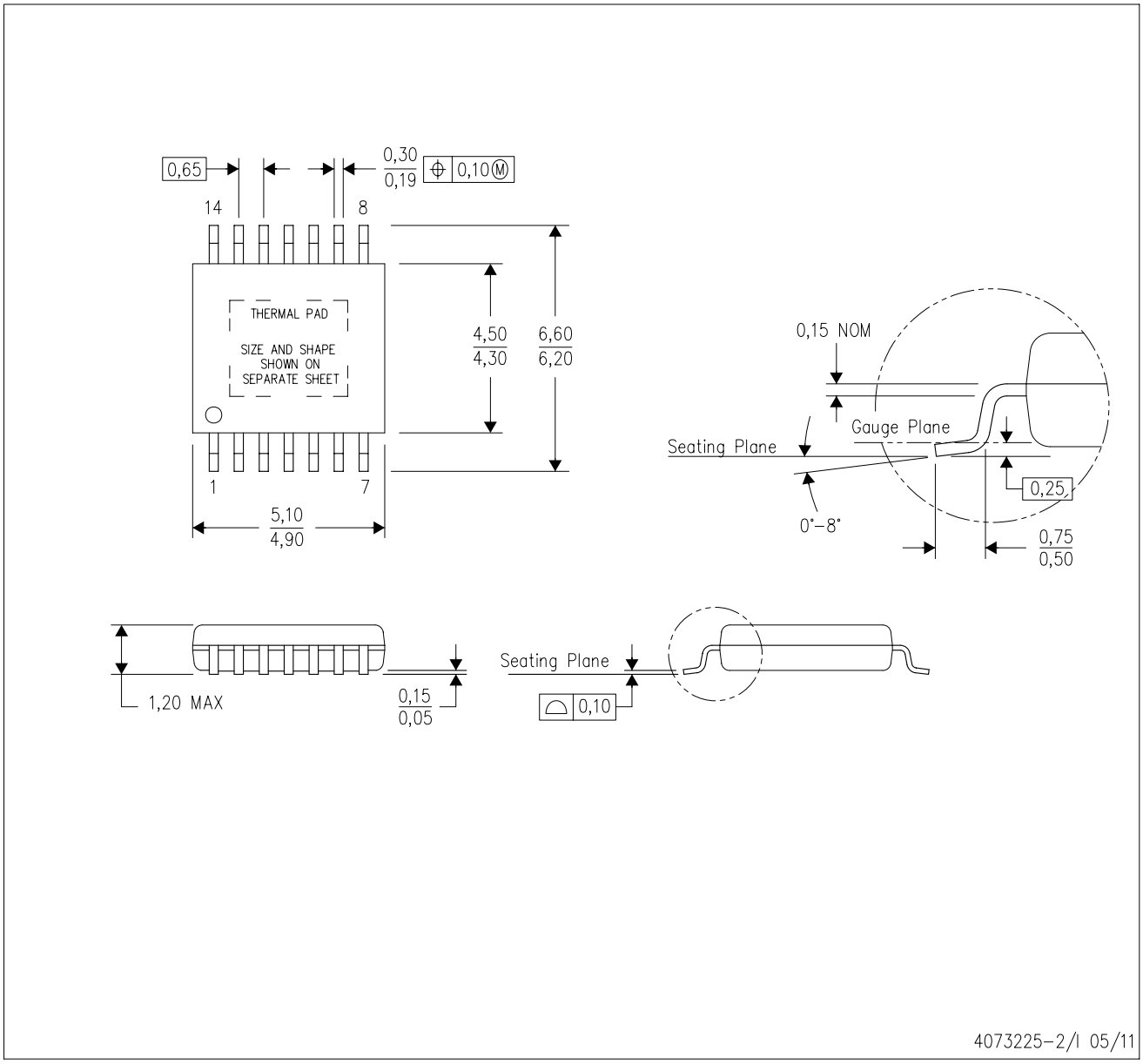

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

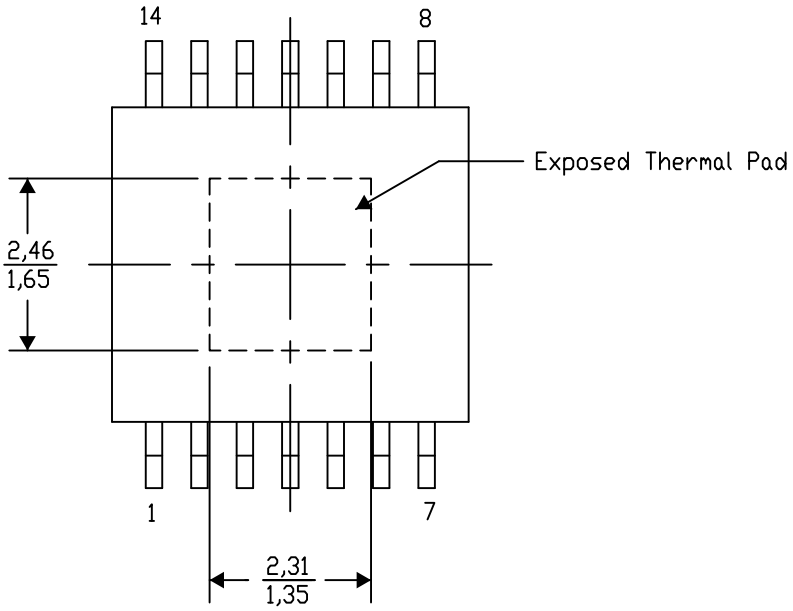
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

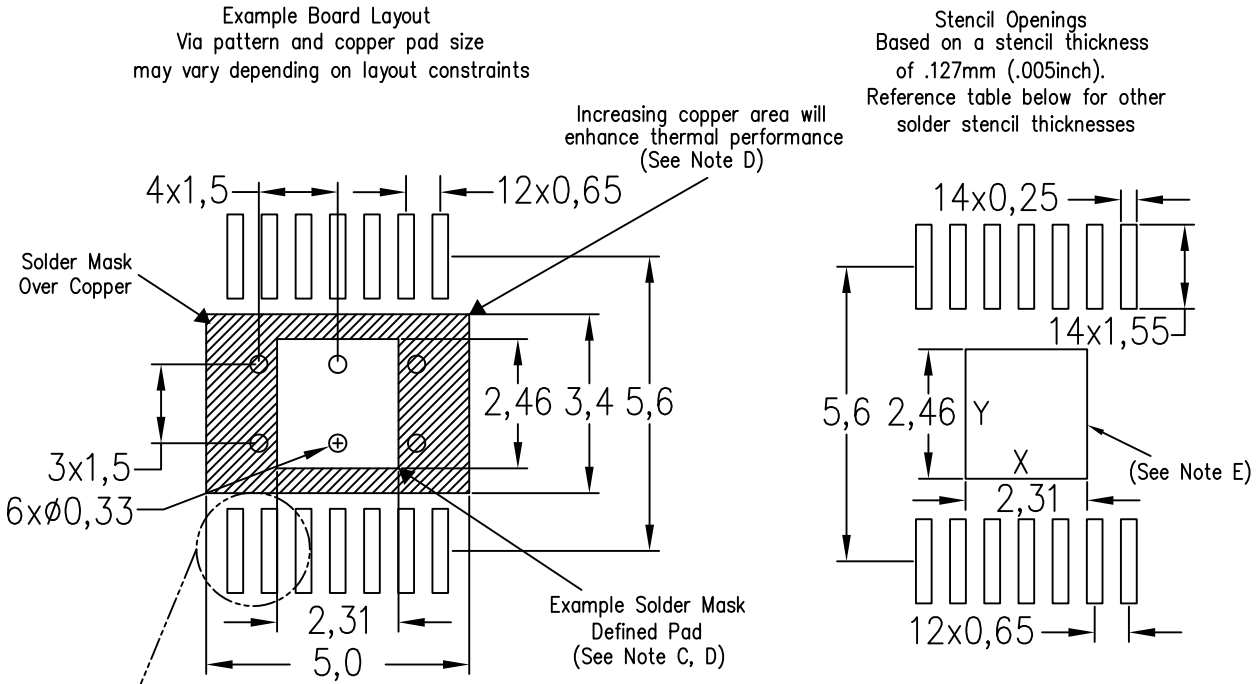
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

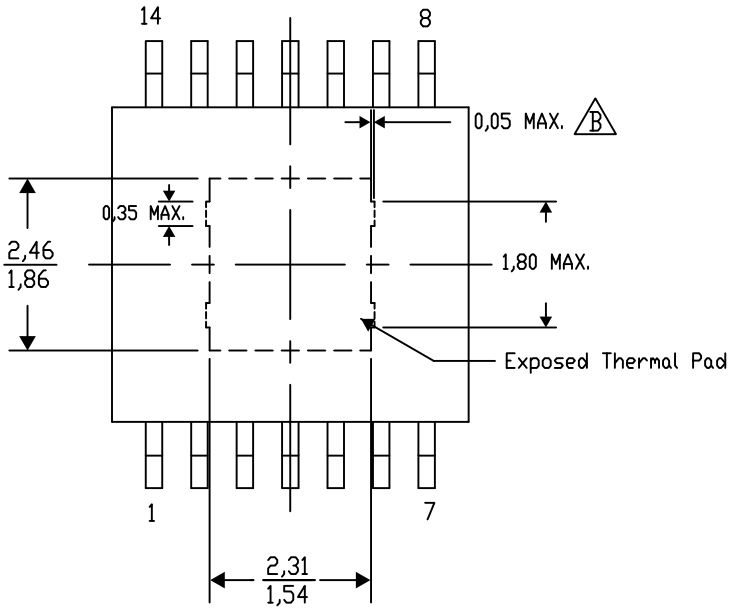
# PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

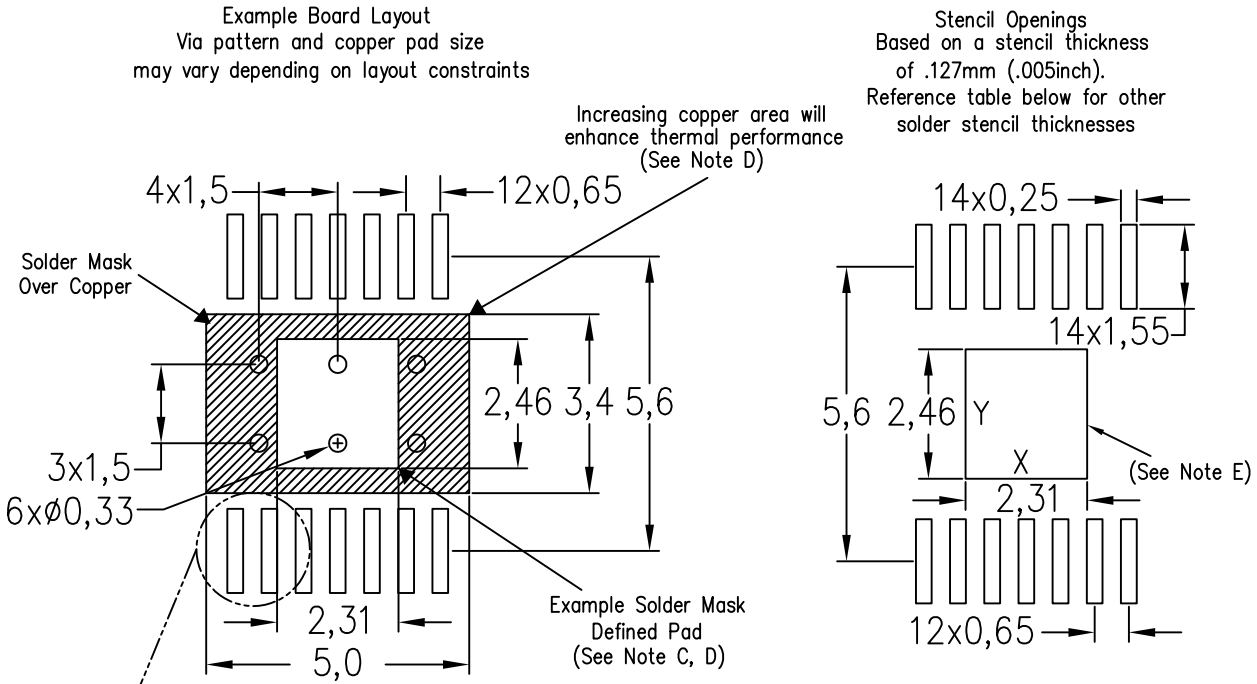
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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